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# Plasma charging damage during contact hole etch in high-density plasma etcher

Bing-Yue Tsui [a,*], Shyue-Shyh Lin [b], Chia-Shone Tsai [c], Chin C. Hsia [b]

[a] Department of Electronics Engineering, National Chiao-Tung University, 1001, Ta-Hsueh Road, Hsinchu, Taiwan, ROC

[b] Deep Sub-micron Technology Division, ERSO/ITRI, Hsinchu, Taiwan, ROC

[c] Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan, ROC

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**Abstract**

Plasma process induced damage from high-density plasma dielectric etcher was studied comprehensively. It was observed that PMOS devices were damaged more readily than NMOS devices. Low field gate current is the most sensitive parameter to reflect the permanent damages. Some permanent damages become hidden defects after backend of line processes. These latent damages in the form of gate oxide traps result in poor oxide integrity during Fowler–Nordheim stress or hot carrier stress. The damage shows good correlation with the total exposed contact area. The safe antenna ratio is much lower than that at the conductor etch, although no electron shading effect was observed. Thus, plasma damage during contact or via hole etch in high-density plasma system must be considered carefully. © 2000 Elsevier Science Ltd. All rights reserved.

## 1. Introduction

Plasma process had been widely used in integrated circuit (IC) manufacturing. Since plasma system has charged and accelerated particles, several kinds of damage may be induced during plasma process. The damages can be divided into four categories: (a) physical damage due to ion bombardment, (b) metal contamination from chamber and gas piping, (c) radiation damage due to glow discharge and ion bombardment, and (d) charging damage due to unbalanced charge in plasma [1]. Among these damages, charging damage has attracted much more attention in the past 10 years because the damage may be magnified by the total exposed conducting area. It is the so-called antenna effect [2–26].

In the past, much work has been devoted to antenna effect during conducting layer etch, e.g. poly-Si layer and metal layer [2–17]. Basic mechanisms, damage modes, impacts on device and circuit, test structures, and measurement techniques have been discussed widely. From these fundamental understandings, low damage process, protection strategy, and new plasma reactor were proposed [18–26]. It is also well accepted that plasma process induced damage (PPID) can be withstood after optimizing process and circuit design.

Dielectric etch becomes more and more important in deep sub-micron era, because the aspect ratio of contact and via hole becomes larger and larger for DRAM process [27]. On the other hand, dual damascene process becomes the main stream for metal patterning as Cu interconnect is used instead of Al interconnect [27]. Conventional metal etch is replaced by dielectric etch in damascene process. Therefore, dielectric etch is more and more important in IC manufacture especially at the backend of line (BEOL) processes. Unfortunately, less work has been done in the field of PPID of dielectric etch [28–32]. In Ref. [28], the authors reported that only the gate current was degraded by PPID. But only fresh device characteristics were measured and only area antenna effect was discussed. In Refs. [29–31], the authors discussed the contact etch damage on various thickness oxides. But the contact size is as large as 4 μm$^2$.

* Corresponding author. Tel.: +886-3-5712121, ext.: 54170; fax: +886-3-5724361.

*E-mail address:* bytsui@cc.nctu.edu.tw (B.-Y. Tsui).

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In Ref. [32], the authors studied the PPID of damascene process, but the etcher used is not a high-density plasma system.

In this paper, we report a comprehensive assessment of the PPID during dielectric etch in a high-density plasma (HDP) etcher. A set of test structures with various contact number, contact size, and contact space was designed. Various device parameters were measured before and after the stress to separate the latent damages from the permanent defects. Hot carrier resistance was also evaluated. It is observed that under the same area antenna ratio, dielectric etch induces more severe damage to gate oxide than the conductor etch does. Thus, PPID during dielectric etch must be considered carefully.

## 2. Experiments

Both NMOS and PMOS devices were fabricated by a standard 0.25 μm single-poly-triple-metal CMOS technology using shallow trench isolation structure. Gate oxide was thermally grown to 5 nm thick. $N^+$ and $P^+$ doped-Si was used as gate electrode for NMOS and PMOS devices, respectively. All devices used to monitor damage are identical and the channel length and channel width is 0.24 and 5 μm, respectively. In order to place more contacts to poly-Si gate, and to exclude the effect of different antenna ratio during poly-Si etch, the antenna ratio of poly-Si pad area to gate oxide area was set to 2 K for all devices. Devices with contact number of 125, 625, 1275, and 2875 corresponding to the area antenna ratio (AAR) of 7, 37, 75, and 170, respectively, were designed. The typical contact size is $0.3 \times 0.3$ $\mu m^2$ and the contact space is 0.3 μm. For some test structures the contact size and contact space are changed to study the effect of contact size and contact density, respectively. Contact etch was performed in a high-density plasma system with inductively coupled plasma (ICP) source. The plasma density at wafer surface is about $10^{11}$ ions/cm$^2$. All devices were protected by P–N diode and connected by the first layer metal to avoid damages from other plasma processes. Fig. 1 shows the schematic diagram of the test structure used in this work.

Low field leakage current of gate oxide ($I_g$) at 2.5 V, linear region threshold voltage ($V_{th}$), transconductance ($g_m$), sub-threshold swing ($S$) were all measured before and after Fowler–Nordheim (F–N) stress to separate the latent damages from the permanent defects. The specification of $I_g$ is 10 pA which is a typical limitation of the noise and leakage current of the automatic measurement system. The F–N stress was performed in inversion polarity at the current density of 1 mA/cm$^2$ for 10 s. Channel hot carrier stress was performed on NMOSFET devices at maximum substrate current and PMOSFET devices at maximum gate current to evaluate the impact of damages on device integrity.

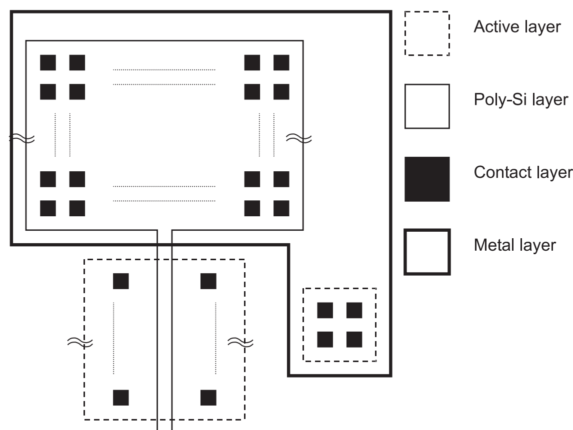



Fig. 1. Schematic diagram of the test structure used to study the plasma process induced damage during contact hole etch. The area antenna ratio at poly-Si layer is 1000. Structures with various contact number, contact size, and contact density are all designed and measured.

## 3. Results and discussion

Since the poly-Si area must be large enough to contain more contact holes, the damage level at poly-Si etch step must be examined first. Four device parameters, $I_g$, $V_{th}$, $g_m$, and $S$, were all measured on NMOS and PMOS devices with various AAR at poly-Si layer. The contact number is one and the metal pad is connected to a protection diode. It is observed that even if the AAR of poly-Si is as high as 10 K, no degradation of any parameters were observed. These results imply that the poly-Si AAR of 2 K used for contact hole etch experiments will not introduce damage during poly-Si etch. Furthermore, the protection diode at metal-1 level is effective to avoid damage at metal etch step. All damages observed for higher contact hole AAR must be attributed to the contact hole etch step.

### 3.1. Damage observation

Fig. 2(a)–(c) shows the cumulative probability plots of $I_g$, $V_{th}$, and $g_m$ of NMOS devices with various contact number before F–N stress, respectively. Although slight difference of mean value of $I_g$ is observed, all of them are within the specification. The slight difference of $I_g$ may arise from the different surface leakage current, since various structures are placed at various position of the test chip. Neither yield nor deviation degrades with the increase of contact number for all parameters. Fig. 3(a)–(c) shows the cumulative probability plots of $I_g$, $V_{th}$, and

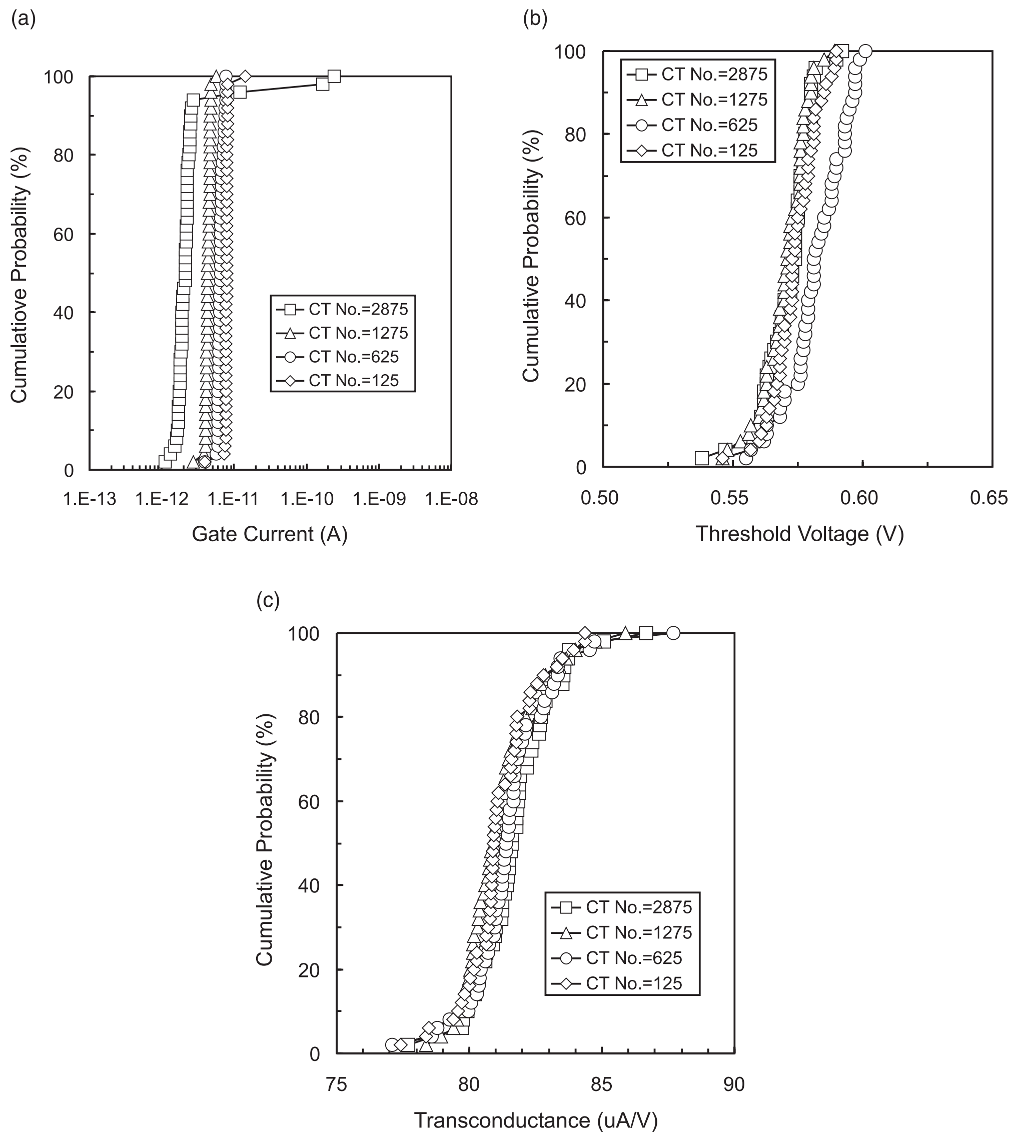



Fig. 2. Cumulative probability plots of (a) gate current $I_g$, (b) threshold voltage $V_{th}$, and (c) transconductance $g_m$ of NMOS devices with various contact number before F–N stress.

$g_m$ of PMOS devices with various contact number before F–N stress, respectively. PMOS devices with large contact number show wider spread of $I_g$. Although the distribution of $V_{th}$ and $g_m$ of PMOS devices do not show any contact number dependence, the obvious correlation between $I_g$ distribution and contact number reflects that PPID occurred and resulted in permanent damage to PMOS devices during contact etch. Sub-threshold swing was also measured, but no contact number dependence was observed for both NMOS and PMOS devices.

From the direct measurement results, two important phenomena were observed. At first, $I_g$ is the most sensitive parameter to reveal damage among the measured DC parameters of devices. This can be easily understood. Oxide charges induced by PPID can be neutralized after BEOL processes. However, most of the trap sites cannot be removed at the relatively low process temperature (around 400°C). Low field $I_g$ is related to oxide trap sites while the other device parameters are related to the trapped charges. Therefore, $I_g$ can reflect PPID more sensitively. The current–voltage characteristics of high $I_g$ devices show stress induced leakage current (SILC). This confirms the existence of oxide trap sites. This result is similar to that reported in Refs. [29–31,33]. Secondly, PMOS device is damaged more easily than NMOS device. This may be due to the

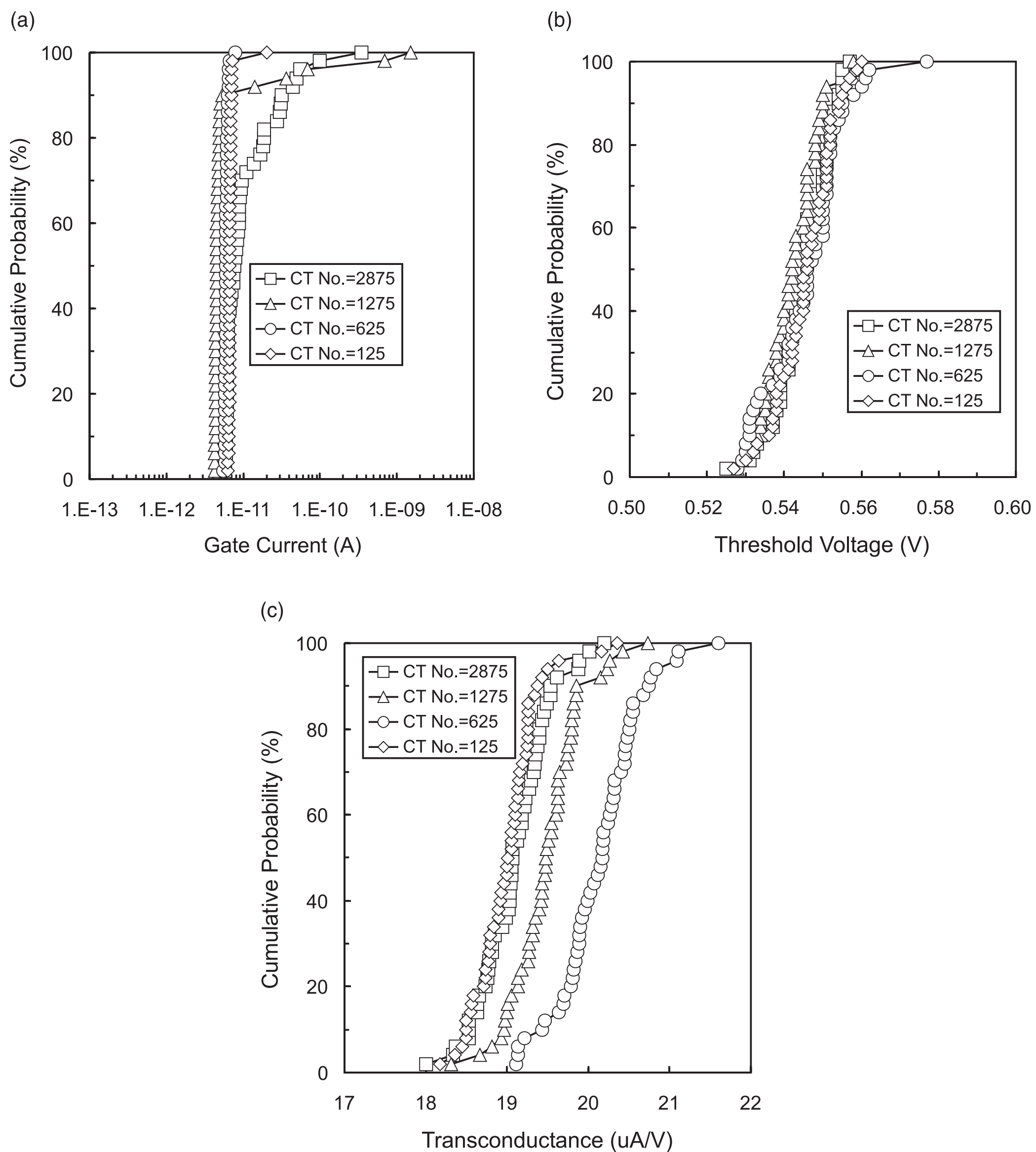



Fig. 3. Cumulative probability plots of (a) gate current $I_g$, (b) threshold voltage $V_{th}$, and (c) transconductance $g_m$ of PMOS devices with various contact number before F–N stress.

polarity of charging during plasma process or due to the difference of poly-Si doping type and is still under investigation.

### 3.2. Latent damages

To determine if any defects were passivated during BEOL processes, another device populations were F–N stressed to 10 mC/cm$^2$, and $I_g$, $V_{th}$, $g_m$, and $S$ were measured. Fig. 4(a) is the cumulative probability plot of $I_g$ of PMOS devices with various contact numbers after stress. It shows that devices with more contact holes have much wider $I_g$ distribution after stress than those with less contact holes. The $V_{th}$ shift after stress, defined as $V_{th}$ (after stress) $-$ $V_{th}$ (before stress), is larger for devices with more contact holes as shown in Fig. 4(b). However, no apparent $g_m$ and $S$ shift difference was observed on PMOS devices with different antenna ratio after stress (not shown). These phenomena indicate that most of the plasma process induced defects were passivated during BEOL processes. Since these defects only results in $V_{th}$ shift but not $g_m$ and $S$ shift after stress, these passivated defects were located in gate oxide but not at oxide/silicon interface.

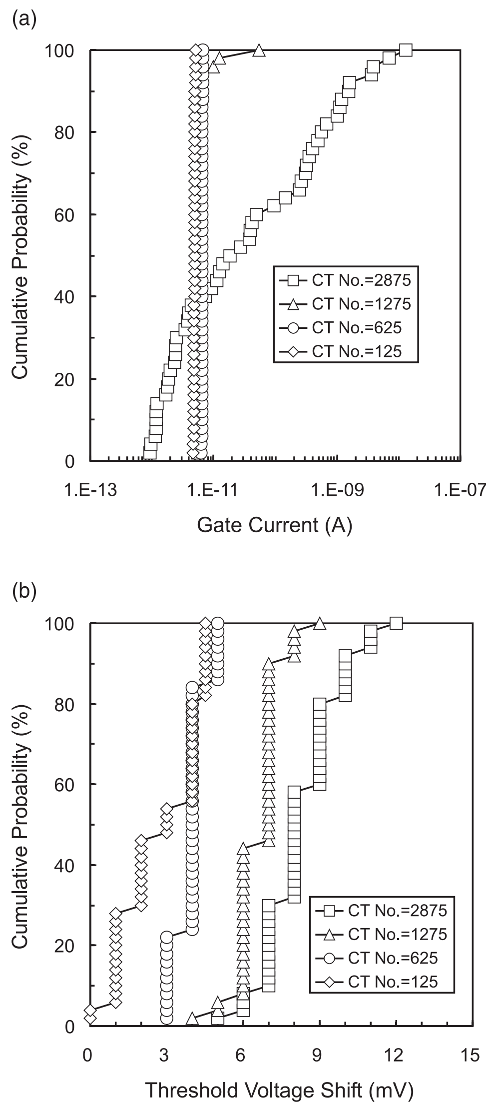



Fig. 4. Cumulative probability plots of (a) gate current and (b) threshold voltage shift of PMOS devices with various contact number after F–N stress at inversion polarity at 1 mA/cm$^2$ for 10 s.

NMOS devices were also F–N stressed to reveal latent damages. However, except the mean value of NMOS devices with 2875 contact holes (AAR = 170) increased from 2 to 10 pA, the other parameters did not show contact number dependence. The latent damages in NMOS devices are much less than that in PMOS devices. This confirms that NMOS device shows less PPID than PMOS device in this experiment.

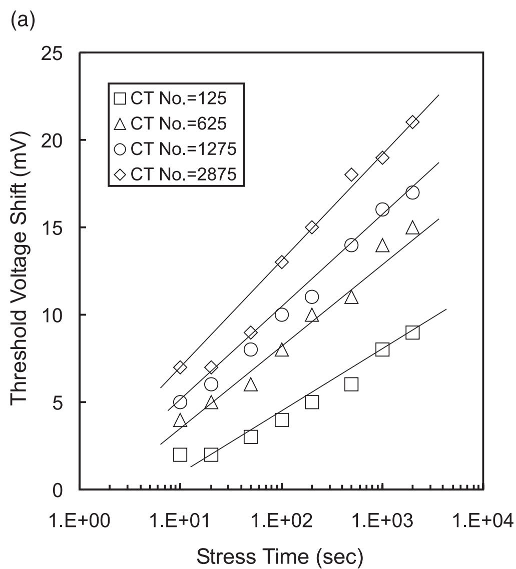
It should be noted that the F–N stress used is not strong. The only purpose is to re-generate the hidden damages. So, if device was not damaged by PPID, $I_g$ will not increase after F–N stress. The results indicate that the device with largest AAR is damaged seriously during contact etch. Since the sensitivity of F–N test is lower than hot carrier test, hot carrier stress was performed in the next step. It was shown that hot carrier stress could resolve latent damages even if the contact number is only several hundreds.

### 3.3. Impact on hot carrier resistance

Fig. 5(a) shows the $V_{th}$ shift of PMOS devices with various contact numbers after hot carrier stress at $V_{ds} = -5$ V and $V_{gs} = -0.8$ V. Higher contact number structure shows higher $V_{th}$ degradation rate. The other parameters such as $g_m$ and $S$ do not show contact number dependence. There are two possible explanations. First, no significant interface states were generated during hot carrier stress. It is reasonable because it is well accepted that the major degradation mechanism of PMOS devices under hot carrier stress is oxide trap but not interface state [34–36]. Secondly, the injected electrons were trapped at those trap sites generated during plasma process. Since the plasma process induced defects are uniformly distributed in channel region, the trapped electrons are distributed broader. The $V_{th}$ shift of NMOS devices stressed at $V_{ds} = 4.5$ V and $V_{gs} = 1.6$ V also show contact number dependence similar to that of PMOS devices as shown in Fig. 5(b). These results confirm that defects located in gate oxide were passivated during BEOL processes and can be re-generated during electrical stress. Although the amount of $V_{th}$ degradation of NMOS devices is higher than that of PMOS devices, the difference between various contact numbers of NMOS devices is less apparent than that of PMOS devices. This is consistent with the conclusion in previous sections that NMOS device shows less PPID than PMOS device. Furthermore, the major degradation mechanism of NMOS and PMOS devices under hot carrier stress are the interface traps and oxide traps, respectively. The observed phenomenon also supports the argument that the latent damages are in the form of oxide traps.

### 3.4. Effect of contact hole size and contact hole density

At first, cumulative probability of $I_g$ of NMOS and PMOS devices with various contact hole size of 0.2, 0.25 and 0.3 μm (aspect ratio of 3.75, 3.0, and 2.5) and various contact hole space of 0.3, 0.6, and 1.2 μm are measured. Since the contact number is 600 and 625 for devices with various contact hole size and various contact hole space, respectively. No difference of $I_g$ distribution was observed. This is not surprising according to the results shown in Section 3.1. To improve the resolution, hot carrier stress was performed on PMOS



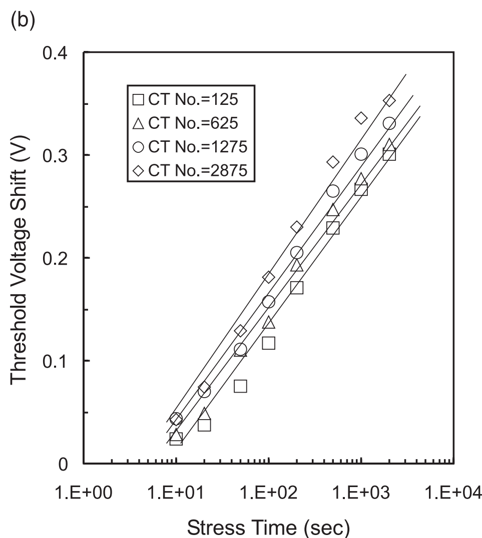




Fig. 5. Threshold voltage shift of (a) PMOS devices and (b) NMOS devices with various contact numbers after hot carrier stress. The PMOS devices is stressed at $V_{ds} = -5$ V and $V_{gs} = -0.8$ V. The NMOS devices is stressed at $V_{ds} = 4.5$ V and $V_{gs} = 1.6$ V.

devices. The stress condition is the same as that used in Section 3.3.

Fig. 6 shows the $V_{th}$ shift of PMOS devices with various contact hole sizes after hot carrier stress. It seems that smaller contact hole results in smaller $V_{th}$ shift. This may be due to the reduction of antenna ratio by a factor of 2.25 as contact hole size is reduced from 0.3 μm to 0.2 μm. No electron shading enhanced effect was observed.

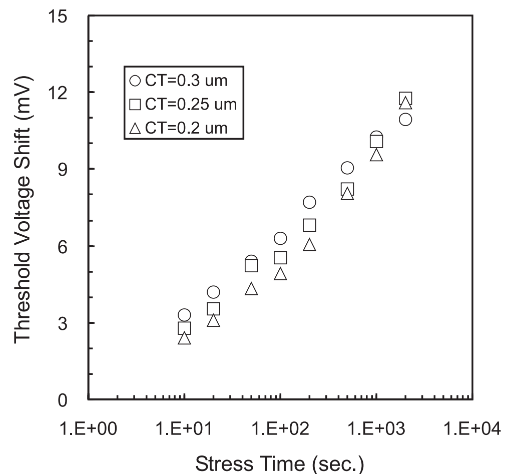



Fig. 6. Threshold voltage shift of PMOS devices with various contact hole size of 0.2, 0.25 and 0.3 μm. The contact space is 0.3 μm and the number is 600.

Fig. 7 shows the $V_{th}$ shift of PMOS devices with various contact hole spaces after hot carrier stress. It is surprising that the larger the contact hole space, the larger the $V_{th}$ shift. This may be due to the local field disturbing effect [37]. To deeply understand the mechanism, additional work on the local field distribution which is beyond the scope of this paper is required. Fortunately, the contact hole space will be pushed to technology limitation to improve the circuit density. This wide space layout does not occur at real circuit.

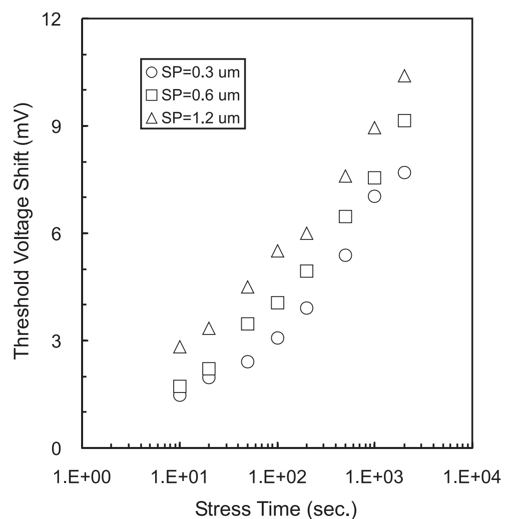



Fig. 7. Threshold voltage shift of PMOS devices with various contact hole space of 0.3, 0.6, and 1.2 μm. The contact size is 0.3 μm and the contact number is 625.

## 4. Conclusions

In this work, the PPID during contact hole etch in a HDP system was investigated comprehensively. Among the devices DC parameters, $I_g$ is the most sensitive parameter to reveal the permanent defects. Some permanent defects were hidden during the BEOL process. These latent damages in the form of oxide trap exist in gate oxide. They can be re-generated after F–N stress or hot carrier stress. NMOS devices show less PPID than NMOS devices in this work.

The PPID shows good correlation with the number of contact, i.e. the total area of contact holes. The hot carrier degradation decreases with the decrease of contact hole size due to the reduction of antenna ratio. The PPID is enhanced by the wide contact hole space. Fortunately, it will not be issues in real circuit. It is also observed that the safe antenna ratio of contact hole etch is much less than that of conductor. Therefore, PPID during contact hole or via hole etch must be considered carefully.

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## References

[1] Fonash SJ. Photons, charging current, hydrogen, and particle bombardment – the four horsemen of plasma etching. Proceedings of International Symposium on Plasma Process Induced Damage, P2ID-96, Santa Clara, 1996. p. 195.

[2] Watanabe T, Yoshida Y. Dielectric breakdown of gate insulator due to reactive ion etching. Solid State Tech 1984;27(4):263.

[3] Ryden KH, Norstrom H, Nender C, Berg S. Oxide breakdown due to charge accumulation during plasma etching. J Electrochem Soc 1987;134(12):3113.

[4] Shone F, Wu K, Shaw J, Hokelet E, Mittal S, Haranahalli A. Gate oxide charging and its elimination for metal antenna capacitor and transistor in VLSI CMOS double layer metal technology. Proceedings International Symposium of VLSI Technology, VLSI-89, Kyoto, 1989. p. 73.

[5] Greene WM, Kruger JB, Kooi G. Magnetron etching of polysilicon: electrical damage. J Vac Sci Technol 1991; B9:366.

[6] Gabriel CT. Gate oxide damage from polysilicon etching. J Vac Sci Technol 1991;B9:370.

[7] Shin H, King CC, Horiuchi T, Hu C. Thin oxide charging current during plasma etching of aluminum. IEEE Electron Dev Lett 1991;12(8):404.

[8] Fang S, McVittie JP. A model and experiments for thin oxide damage from wafer charging in magnetron plasma. IEEE Electron Dev Lett 1992;13(6):347.

[9] Shin H, Hu C. Monitoring plasma-process induced damage in thin oxide. IEEE Trans Semi Manu 1993;6(1):96.

[10] Lin MR, Fang P, Heiler H, Lee R, Rakkhit R, Shen L. Characterization and optimization of metal etch processes to minimize charging damage to submicron transistor gate oxide. IEEE Electron Dev Lett 1994;15(1):25.

[11] Mistry KR, Fishbein BJ, Doyle BS. Effect of plasma-induced charging damage on n-channel and p-channel MOSFET hot carrier reliability. In: 32nd Proceedings International Reliability Physics Symposium, IRPS 94, San Hose, 1994. p. 42.

[12] Noguchi K, Okumura K. The effect of plasma-induced oxide and interface degradation on hot carrier reliability. In: 32nd Proceedings International Reliability Physics Symposium, IRPS 94, San Hose, 1994. p. 232.

[13] Li X, Divakaruni R, Hsu JT, Prabhakar V, Aum P, Chan D, Viswanathan CR. Effect of plasma poly etch on effect channel length and hot carrier reliability in submicron transistor. IEEE Electron Dev Lett 1994;15(4):140.

[14] Hashimoto K. Charging damage caused by electron shading effect. Jpn J Appl Phys 1994;33:6013.

[15] Tsui BY, Liu SH, Lin GL, Ho JH, Chang CH, Lu CY. Recovery phenomenon and local field sensitivity of wafer charge-up effect of magnetically enhanced reactive ion etch system. IEEE Electron Dev Lett 1995;16(2):64.

[16] Joshi AB, Chung L, Min BW, Kwong DL. Gate oxide thickness dependence of RIE-induced damages on N-channel MOSFET reliability. In: 34th Proceedings International Reliability Physics Symposium, IRPS 96, Las Vegas, 1996. p. 300.

[17] Cheung KP, Chang CP. Plasma-charging damage: a physical model. J Appl Phys 1994;75(9):4415.

[18] Krishnan S, Rangan S, Hattangady S, Xing G, Brennan K, Rodder M, Ashok S. Assessment of charge-induced damage to ultra-thin gate MOSFETs. International Electron Device Meeting Tech, Dig IEDM-97, Washington DC, 1997. p. 445.

[19] Krishnan S, Dostalik WW, Brennan K, Aur S. Inductively coupled plasma (ICP) metal etch damage to 30–60 Å gate oxide. International Electron Device Meeting Tech, Dig IEDM-96, San Francisco, 1996. p. 731.

[20] Ma S, McVittie JP. Prediction of plasma charging induced gate oxide tunneling current and antenna dependence by plasma charging probe. In: Proceedings of International Symposium on Plasma Process Induced Damage, P2ID-96, Santa Clara, 1996. p. 20.

[21] Aum PK, Brandshaft R, Brandshaft D, Dao TB. Controlling plasma charge damage in advanced semiconductor manufacturing – challenge of small feature size device, large chip size, and large wafer size. IEEE Trans Electron Dev 1998;45(3):722.

[22] Lukaszek W. Quantifying wafer charging during via etch. Proceedings of International Symposium on Plasma Process Induced Damage, P2ID-96, Santa Clara, 1996. p. 30.

[23] Cheng HC, Lin W, Kang TK, Peng YC, Dai BT. A novel two-step etching to suppress the charging damages during metal etching employing helicon wave plasma. IEEE Electron Dev Lett 1998;19(6):183.

[24] Krishnan S, Amerasekera A. Antenna protection strategy for ultra-thin gate MOSFETs. In: 36th Proceedings International Reliability Physics Symposium, IRPS 98, Reno, 1998. p. 302.
[25] Makabe T, Atsui J, Shibata M, Nakano N. Toward charging free plasma processes: phase space modeling between pulsed plasma and microtrench. In: Proceedings of International Symposium on Plasma Process Induced Damage, P2ID-98, Honolulu, 1998. p. 156.
[26] Noguchi K, Ohtake H, Samukawa S, Horiuchi T. Suppression of topography-dependent charging damage to MOS devices using pulse-time-modulated plasma. In: Proceedings of International Symposium on Plasma Process Induced Damage, P2ID-98, Honolulu, 1998. p. 176.
[27] The National Technology Roadmap for Semiconductors. Semiconductor Industry Association, 1997. p. 101.
[28] Okandan M, Fonash SJ, Awadelkarim OO, Chan YD, Preuninger F. Soft-breakdown damage in MOSFETs due to high-density plasma etching exposure. IEEE Electron Dev Lett 1996;17(8):388.
[29] Park D, Hu C. Plasma charging damage on ultra-thin gate oxide. In: Proceedings of International Symposium on Plasma Process Induced Damage, P2ID-97, San Francisco, 1997. p. 15.
[30] Park D, Kennard M, Melaku Y, Benjamin N, King TJ, Hu C. Stress-induced leakage current due to charging damage: gate oxide thickness and gate poly-Si etching condition dependence. In: Proceedings of International Symposium on Plasma Process Induced Damage, P2ID-98, Honolulu, 1998. p. 56.
[31] Park D, Hu C. The prospect of process-induced charging damage in future thin gate oxides. Microelectron Reliab 1999;39:567.
[32] Matsunaga N, Yoshinari H, Tomioka K, Shibata H. Damascene process induced charging damage phenomenon. In: Proceedings of the International Interconnect Technology Conference, IITC-99, San Francisco, 1999. p. 276.
[33] Chen CC, Lin HC, Chang CY, Liang MS, Chien CH, Hsien SK, Huang TY. Plasma-induced charging damage in ultrathin (3nm) nitrided oxide. In: Proceedings of International Symposium on Plasma Process Induced Damage, P2ID-99, Monterey, 1999. p. 141.
[34] Hu C, Tam SC, Hsu FC, Ko PK, Chan TY, Terrill KW. Hot electron-induced MOSFET degradation – model, monitor, and improvement. IEEE Trans Electron Dev 1985;32(3):375.
[35] Chang WS, Davari B, Wordeman MR, Taur Y, Hsu CCC, Rodriguez MD. A high-performance 0.25-μm CMOS technology: I-design and characterization. IEEE Trans Electron Dev 1992;39(4):959.
[36] Hsu CCH, Wen DS, Wordeman MR, Taur Y, Ning TH. A comprehensive study of hot-carrier instability in P- and N-type poly-Si gated MOSFETs. IEEE Trans Electron Dev 1994;41(5):675.
[37] Tsui BY, Her SH, Lin GL, Ho JH, Chang CH, Lu CY. Recovery phenomenon and local field sensitivity on wafer charge-up effect of magnetically enhanced reactive ion etch system. IEEE Electron Dev Lett 1994; 16(2):64.