# Plasma-Induced Charging Damage in Ultrathin (3-nm) Gate Oxides

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***Abstract*—Plasma-induced damage in various 3-nm-thick gate oxides (i.e., pure oxides and $N_2O$-nitrided oxides) was investigated by subjecting both nMOS and pMOS antenna devices to a photoresist ashing step after metal pad definition. Both charge-to-breakdown and gate leakage current measurements indicated that large leakage current occurs at the wafer center as well as the wafer edge for pMOS devices, while only at the wafer center for nMOS devices. These interesting observations could be explained by the strong polarity dependence of ultra-thin oxides in charge-to-breakdown measurements of nMOS devices. In addition, pMOS devices were found to be more susceptible to charging damage, which can be attributed to the intrinsic polarity dependence in tunneling current between n- and p-MOSFET,s. More importantly, our experimental results demonstrated that stress-induced leakage current (SILC) caused by plasma damage can be significantly suppressed in $N_2O$-nitrided oxides, compared to pure oxides, especially for pMOS devices. Finally, nitrided oxides were also found to be more robust when subjected to high temperature stressing. Therefore, nitrided oxides appear to be very promising for reducing plasma charging damage in future ULSI technologies employing ultrathin gate oxides.**

***Index Terms*—Dielectric breakdown, leakage current, nitrogen, plasma applications, semiconductor device reliability.**

## I. Introduction

ULTRATHIN gate oxides are indispensable for continued scaling of advanced CMOS ULSI technologies into deep sub-half-micron regime. The integrity and reliability of ultrathin gate oxide are therefore of major concern for ULSI devices. Concurrently, it is well known that plasma charging effects can severely degrade the breakdown characteristics of thin gate dielectric. A glow discharge can cause device degradation due to charge imbalance on the wafer surface induced by plasma nonuniformity, or by photons from high energy levels to low energy states. When the voltage due to charge built-up is sufficiently large, Fowler–Nordheim (FN) tunneling current collected by the antenna structure is channeled through the thin gate oxide, causing degradation in gate oxide integrity. Recently, it has been reported in numerous studies that the incorporation of nitrogen in the gate dielectric through $N_2O$-oxidation can suppress process-induced damage [1]–[3]. Besides, nitrogen incorporation also increases the robustness to boron diffusion, an important feature for pMOS devices [4]–[6]. Nitrided oxide is thus highly regarded as a promising alternative gate dielectric to replace thermal oxide in future ULSI technologies. In this work, we investigated and compared the charging damage characteristics of nMOS and pMOS devices. The effectiveness of employing ultrathin nitrided oxide in suppressing plasma damage was then studied. Our experimental results showed that pMOS devices are more sensitive to plasma charging and more susceptible to positive charging damage. More important, $N_2O$-nitrided oxide was found to be very effective in suppressing charging damage, especially for pMOS devices, as evidenced by the lower gate leakage current after plasma damage as well as after high temperature stressing.

Manuscript received November 1, 1999. This work was supported by the National Science Council of the Republic of China under Contract NSC-87-2721-2317-200. The review of this paper was arranged by Editor M. Hirose.

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Publisher Item Identifier S 0018-9383(00)04254-4.

## II. Experimental

Dual-gate (i.e., $n^+$- and $p^+$-poly for n- and p-channel devices, respectively) CMOS test transistors used in this study were fabricated on 6-in wafers. After a conventional LOCOS isolation processing, gate oxides were thermally grown at 850 °C in either $O_2/N_2$ or $N_2O/N_2$ ambient for pure-$O_2$ control samples and nitrided-oxide samples, respectively. All samples have a final oxide thickness of 3 nm. The oxide thickness was verified by ellipsometry on the monitor wafer, and was also confirmed by fitting the FN tunneling current [7] on the completed devices. Metal antenna structures attached to the gates were used to study the charging damage. After metal pattern definition, photoresist was stripped off in a down-stream plasma asher. The ashing process temperature was 200 °C. Previously, we have demonstrated that severe charging damage could occur at the wafer center for nMOS devices, which is attributed to the nonuniform plasma generation caused by the gas injection mode of the asher [8]–[10]. Charging damage was analyzed by antenna devices and was further confirmed by the CHARM-2 monitor wafers [11]. As shown in the inset of Fig. 1, CHARM-2 sensors recorded highly negative and highly positive potential values at the wafer center and wafer edge, respectively. The antenna area ratio (AAR) was defined as the area ratio between the metal pad and the active thin oxide region. Finally, a forming gas annealing at 400 °C was applied to all samples before testing.

## III. Results and Discussion

### A. Plasma Charging Damage in nMOS and pMOS Devices

*1) Indicators for Detecting Charging Damage in Ultrathin Oxides:* Fig. 1 shows the cumulative probability distributions of the absolute threshold voltages ($V_{\rm th}$) for n- and p-channel

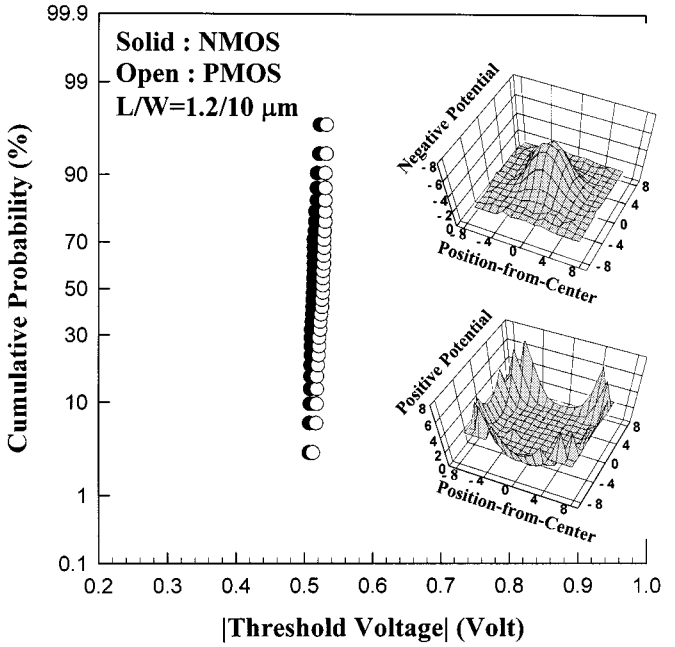


Fig. 1. Cumulative probabilities of the absolute threshold voltage values ($|V_{\rm th}|$) for n- and p-channel devices with pure oxide as the gate dielectric on both antenna and non-antenna structures. Deviation of all the devices is within 20 mV. Inset shows wafer maps of negative and positive potential values recorded by CHARM-2 sensors. Highly negative and highly positive potentials are induced at the wafer center and the wafer edge, respectively.

devices with pure oxide as the gate dielectric for both antenna and non-antenna (i.e., control) structures. First, it can be seen that the threshold voltages are right on the target, i.e., both nMOS devices with $n^+$-gate and pMOS devices with $p^+$-gate depict essentially the same absolute $V_{\rm th}$ value. It is worthy to note that pMOS transistors in this study were carefully processed with a very low thermal budget (i.e., 900 °C, 20 s in $N_2$ ambient) to ensure that no noticeable boron penetration effect was induced in these devices. This is indeed confirmed by the minimal $V_{\rm th}$ shift (i.e., less than 20 mV) for pMOS transistors with pure oxide as the gate dielectric. Thus this study offers a unique opportunity to compare the plasma charging damage in various oxides (i.e., pure oxide and nitrided oxide) without implications due to boron penetration in pure oxide. From Fig. 1, it can be seen that $V_{\rm th}$ shift is minimal for both antenna and nonantenna devices. However, one should not jump to the conclusion that plasma charging damage in these antenna devices is negligible. Rather, these results only indicate that $V_{\rm th}$ is no longer a sensitive charging damage detector for ultrathin gate oxides as thin as 3 nm. Similar results were also observed in subthreshold swing and transconductance characteristics (data not shown). Thanks to the large tolerance of tunneling current, the insensitivity of device parameters to charging damage could be ascribed to insignificant surface state generation and bulk oxide trapping after plasma charging, a property known to be intrinsic to ultrathin oxides.

*2) Charge-to-Breakdown Measurements:* Since traditional charging damage monitors are no longer sensitive for ultrathin gate oxides, other indicators such as charge-to-breakdown ($Q_{bd}$) and gate leakage current ($I_g$) have recently been proposed as viable indicators for detecting antenna effect in ultrathin oxides [12]–[14]. Charge-to-breakdown measurements measured at a stressing current density of 0.2 A/cm$^2$ under accumulation polarity were performed on both nMOS and pMOS transistors with different AAR's. As shown in Fig. 2(a) and (b), severe charging damage was observed at the wafer center as well as the wafer edge for pMOS antenna devices, whereas charging damage occurs only at the wafer center for nMOS devices. Similar results were also obtained when stressed under inversion polarity (not shown). These interesting observations could be explained by the strong polarity dependence of ultrathin oxides in charge-to-breakdown ($Q_{bd}$) characteristics of $n$MOS devices. As shown in Fig. 3, $Q_{bd}$ values of nMOS devices under substrate injection polarity (i.e., $J = +1$ A/cm$^2$) are much higher than those under the gate injection polarity. While $Q_{bd}$ values of pMOS devices under both injection polarities are almost at the same level. Therefore for pMOS devices, charging damage was observed both at the wafer edge and the wafer center, corresponding to the recorded highly positive potential (at the wafer edge) and highly negative potential (at the wafer center), respectively. While for nMOS devices, apparently the superior oxide robustness under substrate injection polarity (i.e., highly positive potential) protects the devices from charging damage at the wafer edge. The strong polarity dependence of $Q_{bd}$ was believed to be due to the weakness of structure transition layer (STL) located in the $SiO_2$/Si interface [15], [16]. The injected energetic electrons may release energy at the STL interface and cause bond breaking, a precursor of dielectric breakdown, under gate injection.

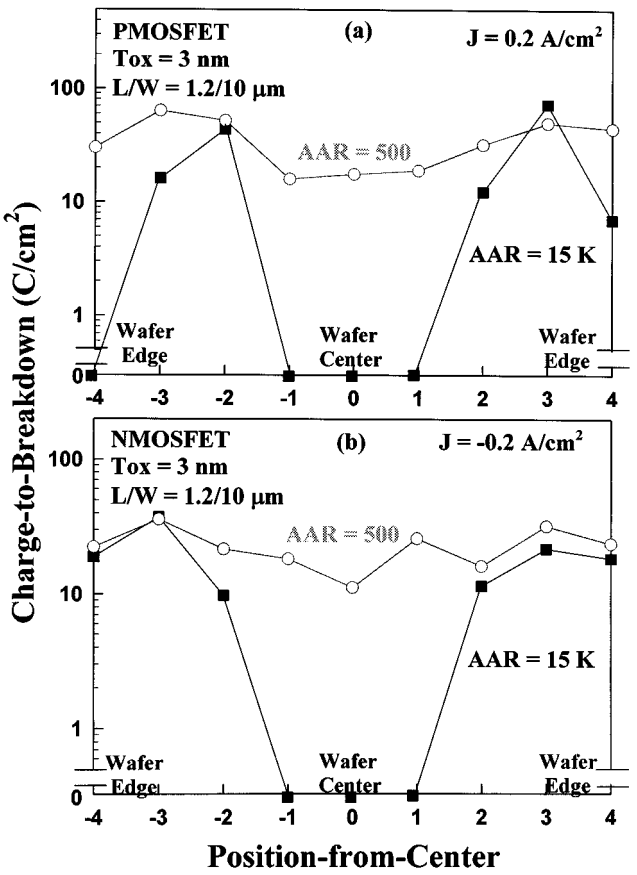


Fig. 2. Charge-to-breakdown values as a function of cell position-from-center for (a) p-channel, and (b) n-channel devices with small (AAR= 500) and large (AAR =15 K) antenna area ratios.

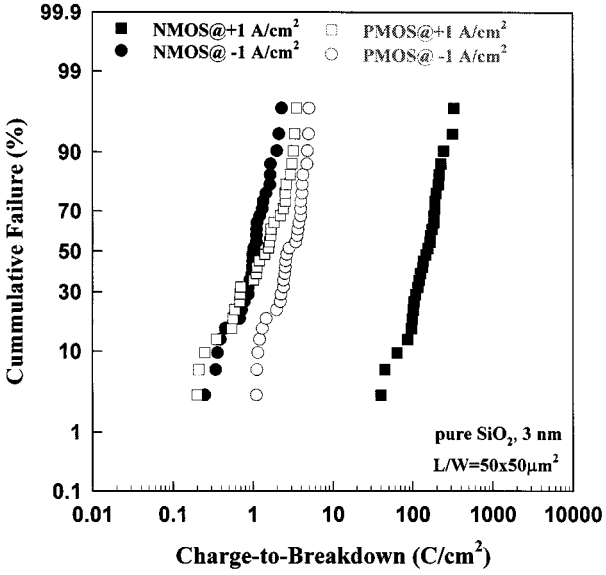


Fig. 3. Cumulative failure of charge-to-breakdown tests for n- and p-channel devices under both gate and substrate injection polarities with constant current density of 1 A/cm$^2$.

It is interesting to note that the 50% $Q_{bd}$ value for pMOS devices under substrate injection is slightly lower than that under gate injection, which is inconsistent with previous literatures [17], [18]. The cause for this phenomenon is probably related to the gate area of the test devices and the stressing current level. In addition, boron segregation at the grain boundary of polysilicon gate is also known to degrade $Q_{bd}$ under substrate injection [18].

*3) Gate Leakage Current Measurements:* Since charge-to-breakdown $(Q_{bd})$ measurement is known to be tedious and time consuming, gate leakage current measurement is used instead as a fast method to study charging damage [12]. Gate leakage current measured at a gate voltage $V_g = 2$ V under inversion polarity (i.e., $+2$ V for nMOS and $-2$ V for pMOS) and with a low drain bias (e.g., $|0.1|$ V) were performed on transistors with different AAR's. As shown in Figs. 4 and 5, large leakage current is observed at the wafer center as well as the wafer edge for pMOS devices [Figs. 4(a) and 5(a)], while charging damage occurs only at the wafer center for nMOS devices [Figs. 4(b) and 5(b)]. These results are consistent with $Q_{bd}$ measurements. Moreover, pMOS devices are shown to be more vulnerable to charging damage since the leakage current of pMOS antenna devices are much larger than that of nMOS devices. This is also consistent with literature reports that charging impacts are more significant on pMOS than on nMOS devices [13], [19]–[21]. Although electron shading effect [22] is a well-known cause for the plasma damage susceptibility of pMOS antenna devices, because the shaded electrons lead to positive stressing of the gate dielectric, which corresponds to carrier accumulation of pMOS devices [20], [21]. However, in this work, electron shading effect is ruled out, since our antenna devices are with low aspect ratio and no dense-line antenna is used (i.e., area-intensive antenna only). Instead, the intrinsic polarity dependence in tunneling current between n- and pMOS devices is believed to be responsible for this discrepancy since pMOS devices show substantially lower tunneling current than nMOS counterparts in both polarities (i.e., $+V_g$ and $-V_g$), as shown in Fig. 6. Note that

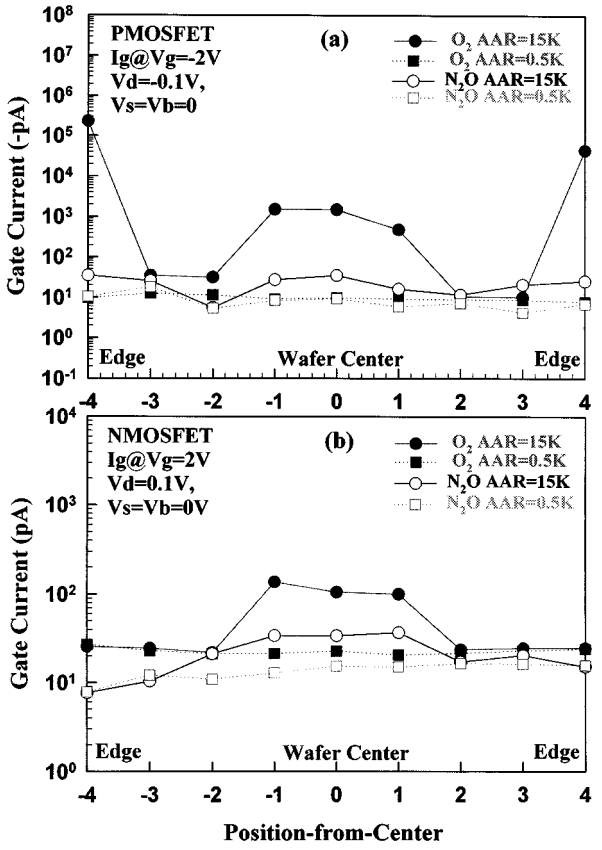


Fig. 4. Gate leakage current as a function of cell position-from-center for both pure $O_2$ and $N_2O$-nitrided oxides. Gate leakage currents were measured at a gate voltage $V_g = 2$ V under inversion polarity for (a) nMOS, and (b) pMOS. Both with a low drain bias ($V_d = 0.1$ V) performed on transistors with small (AAR = 500) and large (AAR = 15 K) antenna area ratios.

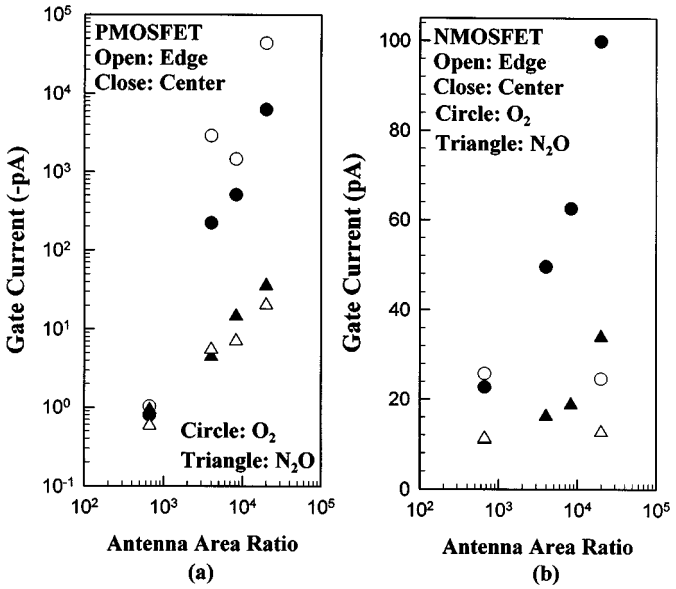


Fig. 5. Gate leakage current as a function of antenna area ratio (AAR) for both pure oxides and $N_2O$-nitrided oxides measured at the wafer center and the wafer edge, respectively. Gate leakage currents were measured at a gate voltage $V_g = 2$ V under inversion polarity for (a) nMOS, and (b) pMOS. A low drain bias ($V_d = 0.1$ V) was applied.

the oxide voltage $(V_{ox})$ in Fig. 6 is extracted by taking polysilicon depletion (when biased in inversion) and flat-band voltage (when biased in accumulation) into account. The discrepancy

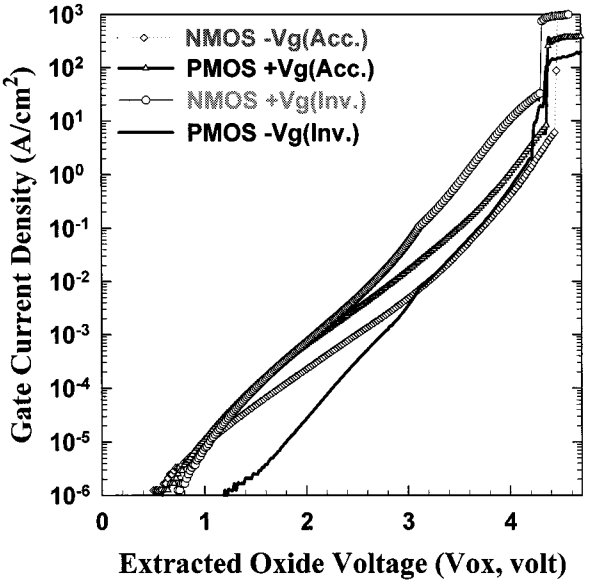


Fig. 6. Gate tunneling currents as a function of oxide voltage ($V_{ox}$) in n- and p-channel transistors measured under both inversion (Inv.) and accumulation (Acc.) polarities. Source/drain are grounded with the substrate during measurement. Oxide voltages are extracted from gate voltages by considering flat-band voltage (accumulation) and polysilicon depletion effect (inversion).

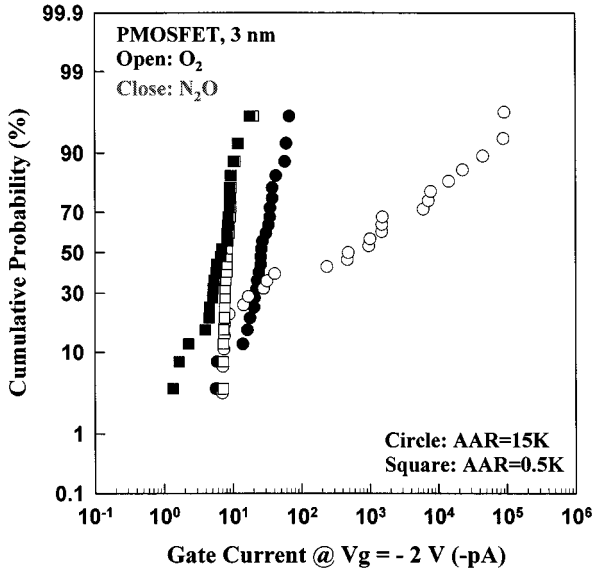


Fig. 7. Cumulative probabilities of gate leakage current for p-channel devices with pure (open symbol) and $N_2O$-nitrided oxides (close symbol), with small (AAR = 500) and large (AAR = 15 K) antenna area ratios.

between n- and p-MOS devices in tunneling can be ascribed to the fact that when biased in inversion, the number of conduction band electrons available for tunneling is substantially lower in pMOS (i.e., $-V_g$) than in nMOS devices (i.e., $+V_g$) [17]. Since it is hypothesized that plasma charging acts more like a current source [23], the corresponding voltage drop in pMOS devices is thus larger than that in nMOS devices. Consequently, pMOS devices are more vulnerable to charging damage. So despite the fact that pMOS devices are reported to depict better TDDB characteristics under normal operating condition [17], a situation resembling constant-voltage stressing, pMOS devices are actually more prone to plasma process-induced charging damage.

### *B. Improved Immunity to Charging Damage in Nitrided Oxides*

*1) Suppression of Gate Leakage Current due to Charging Damage in Nitrided Oxides:* Since charging damage has such significant impacts on ultrathin oxide reliability, $N_2O$-nitrided oxides, which were known to improve gate oxide reliability, were explored in this study as a possible technique to alleviate plasma charging damage. As shown in Figs. 4 and 5, charging damage can indeed be substantially suppressed with $N_2O$-nitrided oxide. In contrast with pure oxide, leakage current of antenna devices is significantly improved with nitrided oxide. In fact, only slight increase in gate leakage current is observed on antenna devices with nitrided oxide. The cumulative plot of gate leakage currents shown in Fig. 7 further confirms that more than two orders of magnitude in gate leakage reduction are achieved on pMOS antenna devices with $N_2O$-nitrided gate dielectric. These phenomena can be ascribed to the nitrogen incorporation in the oxide. The formation of strong Si-N bonds in place of strained Si-O bonds and weak Si-H bonds enhances the interface hardness, resulting in improved gate oxide integrity [3]. Since it has been speculated that trap creation mechanism responsible for SILC is hydrogen-related, the incorporation of nitrogen by $N_2O$-nitridation is expected to terminate Si dangling bonds at the $SiO_2$/Si interface as well as to reduce the stress/strain in the structure transition layer (STL) [15], [24]. As a result, gate leakage current after plasma charging can be reduced. Our results shown in Figs. 4, 5 and 7 indeed confirm that $N_2O$-nitrided oxide is extremely effective in improving the immunity to plasma damage for ultrathin oxides.

*2) Improved Temperature-Accelerated Oxide Degradation in Nitrided Oxides:* It is generally agreed that high temperature degrades oxide reliability, and gate oxide is more susceptible to charging damage at elevated temperature [10], [25], [26]. Since in real plasma processing, the gate oxide is subjected to elevated temperature, the superior SILC characteristics of $N_2O$-nitrided oxides were then further analyzed by high temperature stressing. In this study, test devices including pure oxide and nitrided oxide samples were subjected to a 0.1 Coulomb/cm$^2$ prestress at 180 °C before room-temperature gate leakage current measurement. As shown in Fig. 8, dramatic reduction in SILC caused by high temperature prestressing is observed on $N_2O$-nitrided samples for both n- and p-channel devices, compared to pure oxide counterparts. As the temperature-accelerated oxide degradation is believed to be related to the diffusion of hydrogen-related species caused by breaking strained Si-H and Si-O bonds in the STL [25], [27], so SILC after high temperature prestress and plasma-induced charging damage can thus be improved in nitrided oxides where nitrogen incorporation serves to repair the stressed/strain bonds.

## IV. Conclusion

In summary, plasma damage on CMOS transistors with various 3 nm-thick gate oxides was investigated. Our results showed that pMOS antenna devices are more sensitive to positive plasma charging, thus depicting large gate leakage current both at the wafer center and the wafer edge. In contrast, nMOS antenna devices depict large gate leakage current only at the wafer center. These observations can be explained by

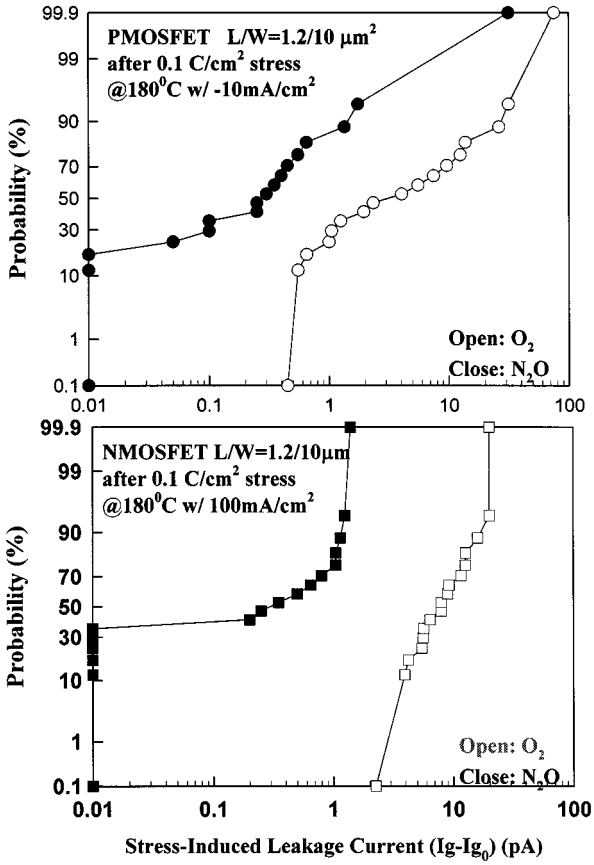


Fig. 8. Cumulative probabilities of stress-induced leakage currents of p-channel (top) and n-channel devices (bottom) for pure oxides (open symbol) and $N_2O$-nitrided oxides (close symbol), after subjecting to a high temperature prestress.

the excellent charge-to-breakdown characteristics for ultrathin gate oxide under positive gate stressing for nMOS devices. More importantly, our results also show that $N_2O$-nitrided oxide depicts significant improvement to charging damage, especially for pMOS devices. Three orders of magnitude in gate leakage current reduction are observed on pMOS devices with nitrided oxide. The nitrided oxide devices are also found to be more robust when subjected to high temperature stressing. All these results indicate that nitrided oxide is very promising for reducing plasma damage in future ULSI technologies employing ultrathin gate oxides.

## ACKNOWLEDGMENT

The authors would like to thank the staff of National Nano Device Laboratories for their technical assistance during the course.

## REFERENCES

[1] D. Crook, M. Domnitei, M. Webb, and J. Bonini, "Evaluation of modern gate oxide technologies to process charging," in *Proc. IEEE/IRPS*, 1993, p. 255.

[2] A. B. Joshi *et al.*, "Suppressed process-induced damage in $N_2O$-annealed $SiO_2$ gate dielectrics," in *Proc. IEEE/IRPS*, 1995, p. 156.

[3] B. W. Min *et al.*, "Impact of process-induced damage on MOSFET reliability and suppression of damage by the user of NO-based oxynitride gate dielectrics," in *Proc. Int. Symp. VLSI TSA*, 1995, p. 273.

[4] K. S. Krisch *et al.*, "Thickness dependence of boron penetration through $O_2$– and $N_2O$-grown gate oxides and its impact on threshold voltage variation," *IEEE Trans. Electron Devices*, vol. 43, p. 982, June 1996.

[5] H. Fang *et al.*, "Low-temperature furnace-grown reoxidized nitrided oxide gate dielectric as a barrier to boron penetration," *IEEE Electron Device Lett.*, vol. 13, p. 217, Apr. 1992.

[6] Z. J. Ma *et al.*, "Suppression of boron penetration in $p^+$ polysilicon gate p-MOSFET's using low-temperature gate-oxide $N_2O$ anneal," *IEEE Electron Device Lett.*, vol. 15, p. 109, Mar. 1994.

[7] K. F. Schuegraf, C. C. King, and C. Hu, "Ultra-thin silicon dioxide leakage current and scaling limit," in *Proc. Symp. VLSI Technology Tech. Dig.*, 1992, p. 18.

[8] C. H. Chien *et al.*, "Resist-related damage on ultra-thin gate oxide during ashing," *IEEE Electron Device Lett.*, vol. 18, p. 33, Jan. 1997.

[9] H. C. Lin *et al.*, "Evaluation of plasma charging damage in ultrathin gate oxides," *IEEE Electron Device Lett.*, vol. 19, p. 68, Mar. 1998.

[10] H. C. Lin *et al.*, "Characterization of plasma charging damage in ultra-thin gate oxides," in *Proc. IEEE/IRPS*, 1998, p. 312.

[11] J. Shideler *et al.*, "A new technique for solving wafer charging problems," *Semiconductor Int.*, p. 153, July 1995.

[12] H. C. Lin, C. H. Chien, and T. Y. Huang, "Characterization of antenna effect by nondestructive gate current measurement," *Jpn. J. Appl. Phys.*, vol. 35, p. L1044, 1996.

[13] Y.-H. Lee *et al.*, "Reliability characterization of process charging impact on thin gate oxide," in *Proc. 3rd Int. Symp. P2ID*, 1998, p. 38.

[14] C.-C. Chen *et al.*, "Plasma-induced charging damage in ultrathin (3 nm) nitrided oxides," in *Proc. 4th Int. Symp. P2ID*, 1999, p. 141.

[15] E. Hasegawa *et al.*, "$SiO_2$/Si interface structures and reliability characteristics," *J. Electronchem. Soc.*, vol. 142, no. 1, p. 273, 1995.

[16] L. K. Han *et al.*, "Polarity dependence of dielectric breakdown in scaled $SiO_2$," in *IEDM Tech. Dig.*, 1994, p. 617.

[17] Y. Shi, T. P. Ma, S. Prasad, and S. Dhanda, "Polarity-dependent tunneling current and oxide breakdown in dual-gate CMOSFET's," *IEEE Electron Device Lett.*, vol. 19, p. 391, 1998.

[18] E. Hasegawa *et al.*, "The impact of nitrogen profile engineering on ultra-thin nitrided oxide films for dual-gate CMOS ULSI," in *IEDM Tech. Dig.*, 1995, p. 327.

[19] M. Alavi *et al.*, "Effect of MOS device scaling on process induced gate charging," in *Proc. 2nd Int. Symp. P2ID*, 1997, p. 7.

[20] M. Creusen, J. Ackaert, E. D. Backer, and G. Groesenken, "Impact of reactor- and transistor-type on electron shading effects," in *Proc. 4th Int. Symp. P2ID*, 1999, p. 8.

[21] J.-P. Carrere and D. R. Heslinga, "Charging protection and degradation by antenna environment on NMOS and PMOS transistors," in *Proc. 4th Int. Symp. P2ID*, 1999, p. 184.

[22] K. Hashimoto, "New phenomena of charge damage in plasma etching: Heavy damage only through dense-line antenna," *Jpn. J. Appl. Phys.*, vol. 32, p. 6109, 1993.

[23] H. Shin, K. Noguchi, and C. Hu, "Thickness and other effects on oxide and interface damage by plasma processing," in *Proc. IEEE/IRPS*, 1993, p. 272.

[24] L. K. Han, H. H. Wang, J. Yan, and D. L. Kwong, "High quality oxynitride gate dielectrics prepared by reoxidation of $NH_3$-nitrided $SiO_2$ in $N_2O$ ambient," *Electron. Lett.*, vol. 31, p. 1196, 1995.

[25] K. Eriguchi and M. Niwa, "Temperature and stress polarity-dependent dielectric breakdown in ultrathin gate oxides," *Appl. Phys. Lett.*, vol. 73, p. 1985, 1998.

[26] C.-C. Chen *et al.*, "Temperature-accelerated dielectric breakdown in ultrathin gate oxides," *Appl. Phys. Lett.*, vol. 74, p. 3708, 1999.

[27] H. Satake, N. Yasuda, S. Takagi, and A. Toriumi, "Correlation between two dielectric breakdown mechanisms in ultra-thin gate oxides," *Appl. Phys. Lett.*, vol. 69, p. 1128, 1996.

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He is currently National Chair, Professor, and the President of National Chiao Tung University (NCTU), Hsinchu. He has devoted himself to education and academic research more than 40 years. During 1962 through 1963, he was in the military service at NCTU, establishing the first Taiwanese experimental TV transmitter, which is the founding part of today's CTS. In 1963, he joined to NCTU to serve as an Instructor establishing the high vacuum laboratory. In 1964, he and his colleague established the semiconductor research center (SRC) at NCTU in April 1965, and the first IC in August 1966. In 1968, he published the first Taiwanese semiconductor paper in an international journal, *Solid State Electronics*. In the same year, he was invited by Prof. L. J. Chu, a Webster Chair Professor, Massachusetts Institute of Technology, to join the NCTU Ph.D. program. In 1969, he became a Full Professor, teaching solid state physics, quantum mechanics, semiconductor devices and technologies. In 1987, he became Dean of Research (1987–1990), Dean of Engineering (1990–1994), and Dean of Electrical Engineering and Computer Science (1994–1995). Simultaneously, he was the founding President of National Nano Device Laboratories (NDL) from 1990 through 1997. Then he became Director of Microelectronics and Information System Research Center (MIRC) of NCTU (1997–1998). He has supervised more than 300 MS and 50 Ph.D. students. They are now founders of most high technology enterprises in Taiwan, namely UMC, TSMC, Winbond, MOSEL, Acer, and Leo, among others. From 1977 through 1987, a strong EECS program at NCKU was established where the GaAs, $\alpha$-Si, poly-Si research projects were established. In 1998, he was appointed President of NCTU. His vision is to lead the university for excellence in engineering, humanity, art, science, management and biotechnology. To strive forward to world class multideciplinery university is the main goal which President Chang and his colleagues have committed.

Dr. Chang has been a Member of Academica Sinica since 1996.

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