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A micromachined silicon-submount package for vertical emission of edge emitting laser diodes

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Abstract

A silicon-submount package structured with vertical emission of edge emitting laser diodes (LDs) is addressed. Utilizing the micromachining technique, a (100) silicon wafer can be engraved into a batch of submount structures having 45°-slant mirrors for light deflection, and mesas for precise die dwelling. The mirrors are fabricated by deep V-groove etching with the etching window aligned to ⟨100⟩ crystal direction, and by multiple cycles of oxidation-and-isotropic etching processes. The initial ridged surface can thus be polished to a final roughness below 30 nm, with 100-μm depth, sufficient to accommodate the vertically extended angle of a laser beam. Gold plating on the surface is patterned to form reflective mirrors on the slopes individually, and to provide the bases, which are connected to common electrode, for electroplating of thick indium pads selectively on the mesa areas. Self-alignment of LD bars or dice soldered right on the mesas can be achieved by the surface-tension mechanism that existed between the LD gold electrodes and the indium pads during melting. With simple TO-5 package, a vertically emitted beam has been observed on a stacked LD-submount device, as expected. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: Laser diode package; Vertical emission; Micromachining; Self-align soldering

1. Introduction

At present, most of laser diodes (LDs) are fabricated with edge emitting structure, in which the horizontal resonant cavity restricts a laser light emitted along the LD substrate plane. Because of its inability to observe the fine light spot from the top, packaging of edge emitting laser (EEL) dice always involves precision mechanics in order to ensure that the laser beams are coupled accurately with their external optical components, as shown in Fig. 1. This complex package structure is different from that of the commercial chip packages, therefore, higher price is expected. In addition to the cost factor, there are other technological motivations demanding simpler LD package such as simpler in-process testing, smaller package size, LD array package, etc.

Because of these reasons, vertical cavity surface emitting lasers (VCSELs) have been actively studied since Iga et al. [1,2] first fabricated the device. However, the wavelength and power generated by state-of-the-art VCSELs are still limited. In addition, an external photodiode is generally required for feedback control of a VCSEL optical power, but to view the VCSEL beam directly by the photodiode is difficult in a conventional TO package. A grating reflector is required to mount on the top optical window, so that a part of light can be reflected back and focused onto the photodiode. Vertically emitting laser (VEL) structured with a 45° mirror and a LD integrated monolithically on a GaAs substrate has also been reported [3]. However, the emission spectrum of this device is also limited by that of GaAs material can provide for.

In view of these shortages, a new VEL package is developed, which provides a micromachined silicon submount capable of allowing vertical emission of EEL diodes, while the disadvantages mentioned above can be totally overcome.

2. The vertical emission package

Fig. 2 shows the cross-section of the proposed vertical emission package. An EEL die is mounted by self-solder-

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ing, which will be described later, onto a micromachined silicon submount at the middle mesa where a pair of V-grooves is formed beside. By crystallographic reason, the V-grooves own a 45° slope if the groove edges are aligned accurately to ⟨100⟩ direction on (100) silicon wafers [4,5]. These slanted surfaces are coated with gold to form mirrors so that the emitted EEL beams can be reflected into vertical direction as shown in the figure.

In order to cover most of the beam field, the submount dimension must obey the following equations:

$$h_1 \geq \left[l\tan\theta_{1/2} - j \right] / 2\left[1 - \tan\theta_{1/2} \right]; \quad (1)$$

$$h_2 \geq \left[h_1\left(1 + \tan\theta_{1/2}\right) + j \right] / \left[1 - \tan\theta_{1/2} \right]. \quad (2)$$

Here h_1 is the altitude difference between the mesa surface and the V-groove tip, h_2 is that between the upper substrate surface and the tip, l is the LD thickness, j is the distance of the LD resonant cavity above the submount surface, and $\theta_{1/2}$ is the half-extended angle of the laser beam. One should note that h_1 must be large enough to avoid the ray impeded by the LD on the upper right corner, and h_2 must be sufficient to allow the mirror covering most of the laser beam field.

To EEL diodes, since their rectangular cavities are shallower in vertical dimension, the far field patterns are elliptical with the longer axis in vertical direction, which generally extends an angle of $\sim 30°$, or $\theta_{1/2} \sim 15°$. While in horizontal direction, the angle is only $\sim 6°$. If a LD has $l = 150$ μm and $j = 6$ μm, the longitudinal extended angle will require a submount dimension of $h_1 \geq 22$ μm and $h_2 \geq 50$ μm, according to Eqs. (1) and (2). Therefore, it is necessary to make the mesa and V-groove to be deep enough so that most of the LD beam can be covered.

In practice, however, perfect matching between the emitting surface, namely the facet, and the edge of the micromachined mesa cannot always be achieved. As shown in Fig. 2, over-shifting to the left of the edge will hinder the lower part of a laser beam by the mesa. According to the geometry, the maximum shifting allowed is $j\cot\theta_{1/2}$ which is ~ 22.4 μm based on the conditions of $j = 6$ μm and $\theta_{1/2} = 15°$. This restriction is very relaxing and can be easily met in reference to current die-bonding accuracy. On the other hand, shifting to the right over the mesa edge causes more concern. It could hinder the lower part of a beam by the upper right corner of a LD, and it might also cause insufficient coverage of the upper-part beam by the upper mirror due to missed reflection. In addition, an over-shifting will result in a suspension facet, which could reduce the LD damage threshold due to insufficient heat conduction at the facet area. Accordingly, the appropriate LD location is to have the facet plane on the left of the mesa edge with a half distance of the maximum tolerable shifting, which is 0.5 $j\cot\theta_{1/2}$ and is counted to be 11.2 μm, with the condition before. This distance constraint is still comfortable referring to the present die-bonding precision (~ 1 μm).

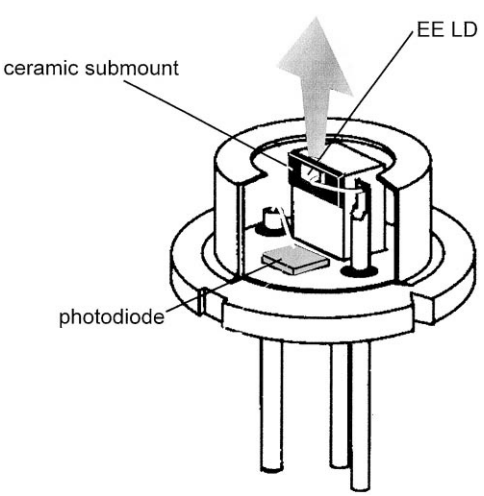

Fig. 1. The conventional package structure of an EEL diode with a collimation cover lens.

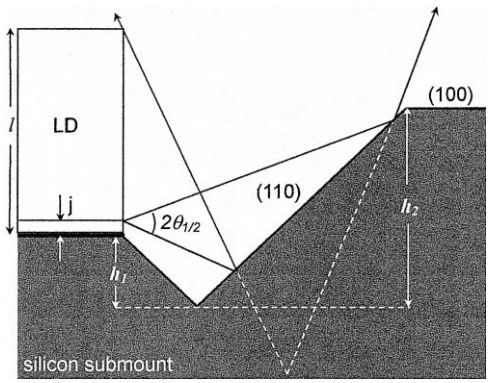

Fig. 2. The proposed structure for vertical emission of EEL diodes, in this study.

3. The fabrication process

A process recipe has been developed to fabricate the VEL package of Fig. 2. As shown in Fig. 3, firstly, an n-type (100) silicon wafer is cleaned and thermally oxidized. Then a window of 450 μm wide is opened on the oxide by photolithographicetching with the edges aligned to ⟨100⟩ directions. The method developed by Ensell [6] is adopted to obtain the alignment within 0.1° accuracy. Anisotropic etching solution of mixed KOH and IPA at 80°C is used to etch through the window a 60 μm deep U-groove with 45° slope (Fig. 3a). This process was previously reported in details by Weng and Shie [4,5]. Afterwards, a second oxidation is performed and a pair of etching window is opened besides the mesa location (Fig. 3b). A second anisotropic etching is proceeded to form another pair of deeper V-grooves and a lower LD mesa for LD dwelling (Fig. 3c). The wafer was then undergone in a series of oxidation-and-isotropic-etching cycles in order to

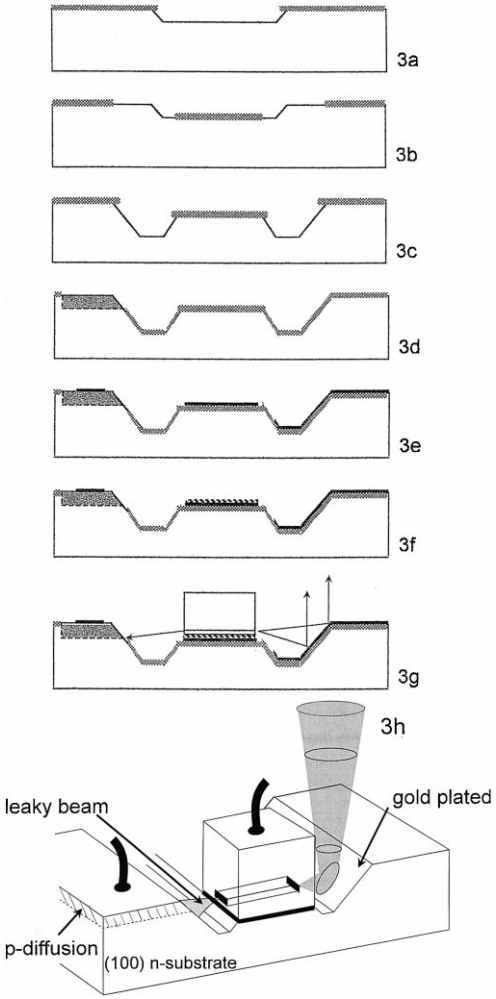

Fig. 3. The fabrication processes designed for the integrated LD-submount device.

polish chemically the slope surfaces, which are rich in ridges [5] initially, into mirror-like (Fig. 3d). We call this the sacrificial-oxide technique. The smoothing mechanism is owing to higher outface energy, thus chemical activity, or oxidation rate, at high-curvature ridge tips. Later, a gold-on-titanium coating, either vacuum-plated or electrochemically plated, is applied on the final oxidized surface, which is then lithographically patterned and etched in KI solution to preserve the demanded areas (Fig. 3e). These areas include the mesas, mirror-like slopes and future bonding pads on submounts. All of these are separated and electrically isolated except the mesas, which are all wired together to a common electrode to allow the subsequent electroplating of thick indium pads ($\sim 5\ \mu m$) selectively on the areas (Fig. 3f). Afterwards, sliced LD bars or dice are individually handled to face downwards on the mesas for soldering at $\sim 200°C$. Because of the highly wetting property between a molten indium and the LD gold electrode, a self-aligned effect appears during the soldering process. This results in highly parallel of a LD facet with a mesa edge, because the electroplated indium pads match completely to the underlaid gold patterns that are accurately aligned to the mesas. The self-aligned soldering step thus ensures that the future laser beams will precisely be perpendicular to the substrate surface precisely, as depicted in Fig. 3h.

During the fabrication, a photodiode could also be built simultaneously in the silicon substrate (Fig. 3h) to detect the optical output power leaking from the other side of the cavity, as also shown in Fig. 3. In addition, after LD bars are integrated on wafer, the whole piece of wafer can be handled for further probing test of good dice, electrically and optically. This simple procedure is very similar to testing a monolithic LED wafer, which is impossible for the conventional EEL package. On-wafer wire bonding

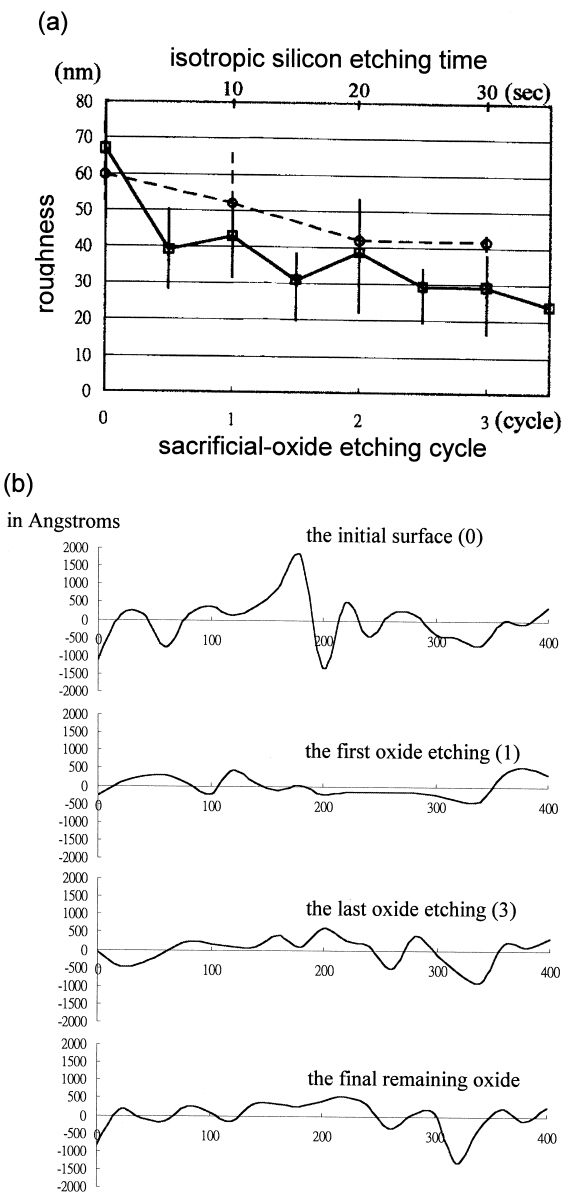

Fig. 4. Progressive measurements of surface roughness on the slopes of the silicon submounts processed by the sacrificial-oxide technique (blank squares), and by an isotropic silicon etching (blank circles).

between the LD dice and corresponding electrodes on individual submounts can also be performed before dicing, if necessary.

At the final stage, the whole processed wafer can be handled for dicing into separated LD-submount hybrid chips, which are then ready for final assembly in the form of the conventional TO package, or even smaller SMT package, without the complex structure shown in Fig. 1.

According to the above description, it is realizable that the stacked LD-submount package is very beneficial to production efficiency, and to that the conventional package of edge emitting LD is difficult to provide for.

4. Results and discussion

Fig. 4 shows the effect of the sacrificial-oxide technique. At the beginning, the surface roughness was measured to be ~80 nm across 300-μm distance, but after few oxidation-and-sacrifice-etching cycles, the toughness is reduced to below ~30 nm. Notice that the surface is smoother if the final oxide is preserved instead of leaving a naked silicon surface. The final ~30-nm flatness is smaller than the 0.1λ flatness requirement of general optical components above the visible wavelength.

It is also possible to replace the oxidation-and-etching cycle by a single isotropic silicon etching step with HF + HNO_3 + CH_3COOH etching solution, noting that the solu-

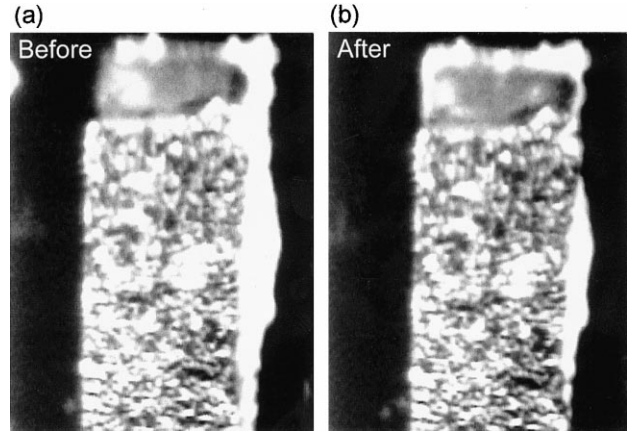

Fig. 6. Observation of self-align soldering of a LD bar on the silicon submount before and after the soldering.

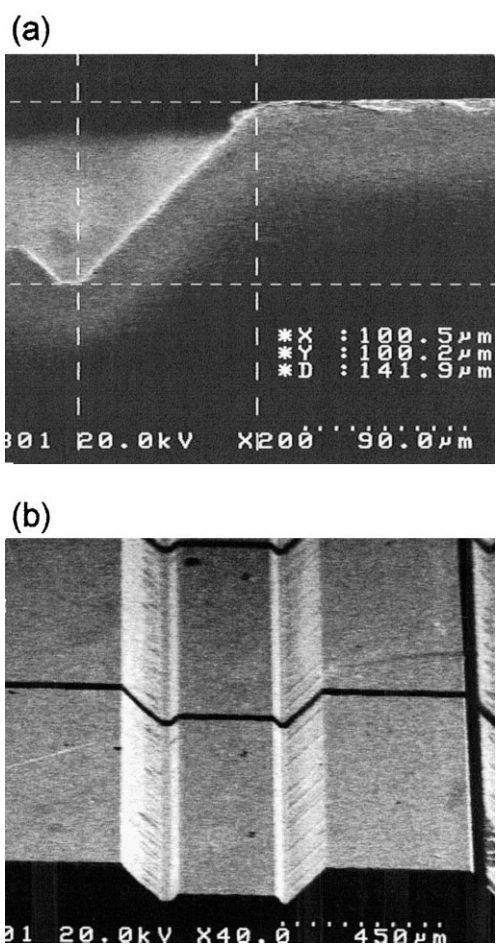

Fig. 5. SEM pictures of a micromachined silicon submount in cross-sectional view (a) and in bird's-eye view (b).

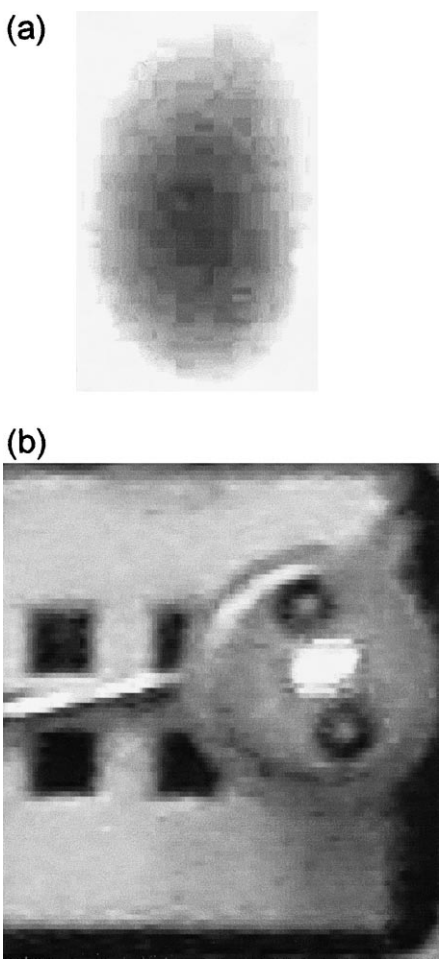

Fig. 7. An observed vertical emission spot on a distant screen (b) projected from the LD-submount package (a).

tion performs the simultaneous oxidation and etching of the Si material. However, as also shown in Fig. 4, this etching process terminates at a rougher surface around 40 nm after 20-s etching.

Fig. 5 shows the SEM pictures of a micromachined silicon submount. A precise 45° slope is observable.

The effect of self-align soldering also has been observed. A LD bar is placed on a mesa location and heated to above 175°C, whence the indium pad melting a spontaneous alignment of the LD bar to the indium pattern also starts. This effect is caused by the surface-energy reduction between the molten indium and the LD gold electrode during alloying wetting. Fig. 6 shows the experimental result by comparing the relative positions of a LD bar before (Fig. 6a) and after (Fig. 6b) soldering. Notice the better LD posture after soldering.

Fig. 7 shows the expected vertical emission spot (Fig. 7b) of an integrated LD-submount chip packaged on a TO-5 head (Fig. 7a).

5. Conclusion

A vertical emission package for EEL diodes has been developed. By the micromachining technique, silicon submounts with 45° mirrors can be fabricated on (100) Si wafers for the purpose of vertical reflection. Furthermore, by the self-aligned soldering between an indium pad and a LD gold electrode, an accurate optical alignment can be accomplished naturally by wetting effect.

The structure and fabricated processes allow efficient package and test of various kinds of EEL diode similar to that of a monolithic LED wafer. It is also possible to have a photodiode built in the silicon submount for optical power sensing without additional cost and the effort for accurate assembly of the external photodiode.

At present, quality of the wavefront of the vertically emitted laser beam is under study.

Acknowledgements

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Biographies

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