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Electrical and material characterization of atomic-layer-deposited Al₂O₃ gate dielectric on ammonium sulfide treated GaAs substrates

Chao-Ching Cheng,¹ Chao-Hsin Chien,^{1,2,*} Guang-Li Luo,² Ching-Chih Chang,¹ Chi-Chung Kei,^{3,4} Chun-Hui Yang,² Chien-Nan Hsiao,³ Tsong-Pyng Perng,⁴ and Chun-Yen Chang¹

¹ Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, R.O.C.

² National Nano Device Laboratory, Hsinchu, Taiwan 300, R.O.C.

³ Instrument Technology Research Center, National Applied Research Laboratories, Hsinchu, Taiwan 300, R.O.C.

⁴ Department of Material Science and Engineering, National Tsing-Hua University, Hsinchu, Taiwan 300, R.O.C.

*E-mail: chchien@faculty.nctu.edu.tw

Abstract. This paper has studied the electrical and interfacial properties of atomic-layer-deposited Al₂O₃ thin film on ammonium-sulfide passivated GaAs. It was found that the Al₂O₃ deposited at 300°C relative to that at 100°C showed the nearly four orders of magnitude reduction in gate leakage current at the capacitance-equivalent-thickness of 40 Å. The capacitance–voltage (*C–V*) characteristics displayed the higher oxide capacitance, reduced frequency dispersion and less charge trapping when GaAs receiving (NH₄)₂S sulfide immersion; these improvements can be reasonably explained by the suppression of both native oxides and the resultant improved interface quality. Annealing as-deposited Al₂O₃/GaAs structures at high temperatures further reduces the Fermi level pinning effect on accumulation capacitance, however, causes an increase in *C–V* frequency dispersion and gate leakage current. We suggested that these phenomena are strongly associated to the amount of As-related defects resided at the dielectric/substrate interface during thermal desorption.

1. Introduction

Novel device structures, channel materials, and gate dielectrics are required to further extend Si-based complementary-metal-oxide-semiconductor (CMOS) front-end fabrication beyond the 22 nm node. One oncoming strategy is to heterogeneous integration of III-V compound materials as transport channels with high-*k* dielectrics on traditional Si or silicon on insulator. However, the absence of thermodynamically stable insulators on III-V compound semiconductors, e.g., (In)GaAs and InSb, etc, have become the foremost bottleneck to III-V technology rivaling or exceeding the properties of Si MOSFETs. For more than four decades, numerous efforts have been devoted in intensively questing the competitive, high interface quality insulators and efficient passivation methods, respectively. Except for SiO₂ and Si₃N₄, (Gd,Ga)₂O₃ and atomic-layer-deposited (ALD) Al₂O₃ [1], HfO₂ [2] high-*k*

dielectrics are of particular interest; meanwhile, the sulfur chemical treatment [3], and Si and Ge [4] as the interfacial passivation layers (IPLs) are currently active approaches to protect the III-V surface prior to the dielectric deposition. This study presented the impact of the surface preparation processes, especially for ammonium sulfide $(\text{NH}_4)_2\text{S}$ immersion, and post-deposition annealing (PDA) on the improvement of interface quality of Pt/ALD- Al_2O_3 /GaAs MOS structures.

2. Experimental

Highly-doped n-type GaAs wafers with the doping concentration of ca. $1 \times 10^{18} \text{ cm}^{-3}$ were used. All samples were precleaned by the acetone (ACE) and rinsed by deionized water. Subsequently, HCl-based acid-solutions with various diluted concentration were tested in GaAs cleaning and ammonium sulfide $(\text{NH}_4)_2\text{S}$ aqua solution was used for surface passivation. We employed x-ray photoelectron spectroscopy (XPS) with an Al $K\alpha$ radiation source to examine the surface chemical bonding prior to high- k layer deposition. The Al_2O_3 thin films were deposited by ALD system at substrate temperatures of 100 and 300°C; Trimethylaluminum, $\text{Al}(\text{CH}_3)_3$, and H_2O were chosen as the metal source and oxidant pulsed alternatively into the reactor for 1 s per pulse separated by N_2 purge of 10 s to remove redundant reactants. Subsequent PDA in an O_2 ambient performed at 600°C was used for film densification. The top Pt capacitance electrode was formed via a shadow mask with the area of ca. $4 \times 10^{-4} \text{ cm}^2$ and Al metal was deposited as the backside contact. The capacitance–voltage (C – V) and gate leakage current (I – V) curves were measured using an HP4284 and Keithley 4200, respectively.

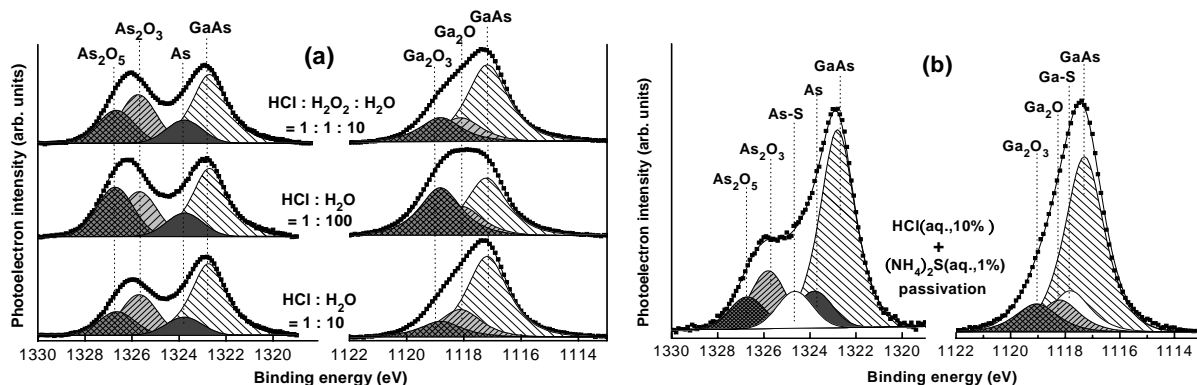


Figure 1. $\text{As}2p3$ and $\text{Ga}2p3$ XPS spectra of GaAs surfaces after (a) different acid-solution cleanings and (b) $(\text{NH}_4)_2\text{S}(\text{aq.})$ sulfide passivation.

3. Results and Discussion

Figure 1(a) displays the $\text{As}2p3$ and $\text{Ga}2p3$ core level spectra of GaAs surface after three different acid cleaning solutions; the peak position and contribution of all chemical components are identified. Clearly, an increase in the concentration of HCl solution assisted to reduce the As-rich layer and both kinds of the native oxides, As_2O_x and Ga_2O_x . Adding H_2O_2 in HCl solution, like the standard clean-2 (SC-2) in RCA, however, seems to further oxidize the GaAs surface with the increased As layer formation. The immersion in $(\text{NH}_4)_2\text{S}$ solution further reduced the As metal and most of native oxides, especially for the As_2O_x , as photoemission spectra shown in Fig. 1(b). The sulfur-based chemical treatment effectively passivated GaAs dangling bonding, by forming As-S and Ga-S chemical bonds at GaAs surface.

We calculated the composition ratios of all contributed components through XPS fitting and summarized the results in Table I. It was found that the higher HCl concentration can diminish the amount of Ga_2O_x with respect to the As_2O_x , leading to thin As-oxide rich surface, which is consistent with the previous report that the acid-etched GaAs wafer revealed both As-oxide and As rich surfaces [5]. During sulfide passivation, Ga atoms have a higher probability than As atoms in bonding to sulfur atoms; this can be attributed to lower bonding strength of As-S chemical bonds.

Wet Clean	As-As/As _{Total}	As-S/As _{Total}	Ga-S/Ga _{Total}	As ₂ O _x /As _{Total}	Ga ₂ O _x /Ga _{Total}
HCl : H ₂ O ₂ : H ₂ O = 1:1:10	12.7 %	--	--	44.9 %	37.9 %
HCl : H ₂ O = 1:100	12.0 %	--	--	48.6 %	56.9 %
HCl : H ₂ O = 1:10	11.1 %	--	--	39.6 %	34.2 %
HCl (aq.,10%) + Sulf.(80°C)	9.7 %	9.8 %	14.8 %	23.7 %	22.1 %

Table I. Chemical bonding ratios calculated by XPS fitting results in Fig. 1 and Fig. 2.

The frequency-dependent and bidirectional $C-V$ curves of Pt/Al₂O₃/n-GaAs MOS capacitors are shown in Figs. 3(a) and 3(b), respectively. As can be seen, the as-deposited sample apparently showed $C-V$ stretch-out behavior accompanying with the lower oxide capacitance; the clockwise hysteresis width was also presented. Even though annealing the sample at 600°C in an O₂ ambient exhibited the higher accumulation capacitance, it also caused a large flat-band voltage (V_{FB}) shift with respect to the measured frequency, implying the generation of slow states at and/or close to the interface. As the (NH₄)₂S treatment was further employed, the highest accumulation capacitance with steep $C-V$ slope presented; meanwhile, the smaller hysteresis behavior was also found. We suggested that the sulfide passivation can improve the interface quality between Al₂O₃ high- k dielectric and GaAs substrate due to the native oxide suppression and enhanced thermal stability.

Figure 4 shows the corresponding $I-V$ characteristics. It was noticed that high-temperature PDA obviously increased the gate leakage current J_g by more than two orders, at gate bias V_g above 2 V. From XPS analysis (not shown here), we found that a small amount of As metal and both native oxides have been incorporated into bulk Al₂O₃ during annealing; the resultant contamination are believed to be responsible for a huge increase in J_g .

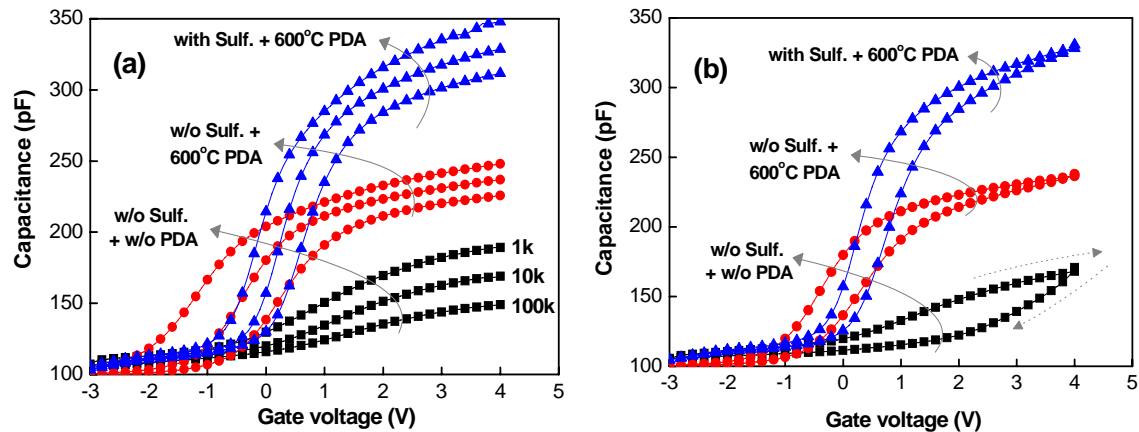


Figure 3. (a) Multi-frequency $C-V$ and (b) bidirectional $C-V$ (10 kHz) curves of Pt/ALD-Al₂O₃/n⁺-GaAs capacitors with different cleaning preparation and annealing processes. The Al₂O₃ thin films were deposited at 100°C for 60 cycles.

The quality of Al₂O₃ deposited at 300°C on GaAs are examined in Fig. 5(a); the inset shows the Weibull plot of J_g distribution at $V_g = 2$ V. The (NH₄)₂S-treated sample relative to the HCl-last sample exhibited the higher oxide capacitance and smaller $C-V$ frequency dispersion, which is similar to the examination in ALD-Al₂O₃ at 100°C. The corresponding J_g seemed to be slightly lower than that in the sample without sulfide process, but, with the broad distribution in the Weibull plot, reflecting the fact that the distribution of sulfur bonding is an important role in gate leakage performance. Besides, as illustrated in Fig. 5(b), all 300°C-Al₂O₃ samples were found to show the better gate leakage

performance, where the nearly four orders of magnitude reduction in J_g at the capacitance-equivalent-thickness (CET) of 40 Å, with respect to the 100°C-Al₂O₃ samples.

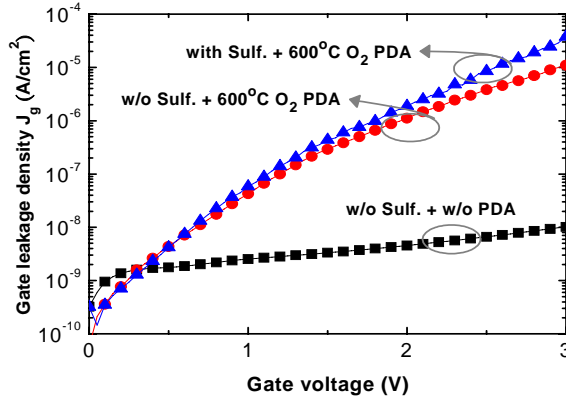


Figure 4. Gate leakage current J_g characteristics of Pt/Al₂O₃/n-GaAs capacitors. The Al₂O₃ thin films were deposited at 100°C for 60 cycles.

4. Conclusions

We investigated the interfacial chemistry of (NH₄)₂S-passivated GaAs and the electrical properties with ALD-Al₂O₃ as gate dielectric. The improvements in $C-V$ characteristics after sulfur surface treatment, including the higher oxide capacitance, reduced frequency dispersion, and less charge trapping, can be reasonably attributed to the reduction of the native oxide formation and improved interface quality. Further, the Al₂O₃/GaAs structure undergoing high-temperature annealing possessed higher accumulation capacitance, however, caused an obvious V_{FB} shift in frequency-dependent $C-V$ curves and increased gate leakage J_g . We suggested that these phenomena depended on the amount of As-related defects remained at the dielectric/substrate interface during thermal processing. In addition, the Al₂O₃ deposited at 300°C relative to that at 100°C showed the nearly four orders of magnitude reduction in J_g at the CET of 40 Å.

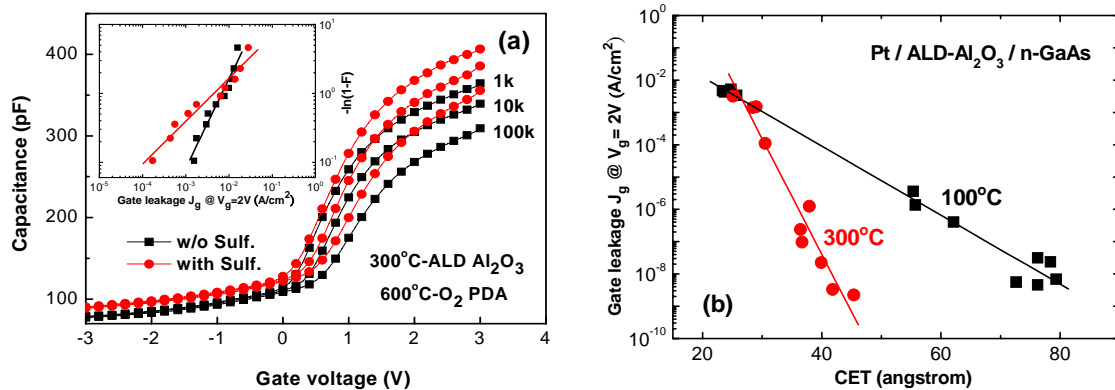


Figure 5. (a) $C-V$ curves of GaAs MOS capacitors with ALD-Al₂O₃ deposited at 300°C for 60 cycles and (b) Comparison of J_g versus CET characteristics of ALD-Al₂O₃/GaAs capacitors deposited at 100 and 300°C with different surface preparation and annealing processes.

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