A New Approach for Characterizing Structure-Dependent Hot-Carrier Effects in Drain-Engineered MOSFET's

Steve S. Chung, *Senior Member, IEEE*, and Jiuun-Jer Yang

***Abstract*— In this paper, we have demonstrated successfully a new approach for evaluating the hot-carrier reliability in submicron LDD MOSFET with various drain engineering. It was developed based on an efficient charge pumping measurement technique along with a new criterion. This new criterion is *based on an understanding of the interface state* $(N_{\rm it})$ *distribution, instead of substrate current or impact ionization rate,* for evaluating the hot-carrier reliability of drain-engineered devices. The position of the peak $N_{\rm it}$ distribution as well as the electric field distribution is critical to the device hot-carrier reliability. From the characterized $N_{\rm it}$ spatial distribution, we found that the shape of the interface state distribution is similar to that of the electric field. Also, to suppress the spacer-induced degradation, we should keep the peak values of interface state away from the spacer region. In our studied example, for conventional LDD device, sidewall spacer is the dominant damaged region since the interface state in this region causes an additional series resistance which leads to drain current degradation. LATID device can effectively reduce hot-carrier effect since most of the interface states are generated away from the gate edge toward the channel region such that the spacer-induced resistance effect is weaker than that of LDD devices.**

I. Introduction

THE spacer-induced degradation resulting from hot-carrier injection is believed to be intrinsic to the conventional LDD structure with n^+-to-gate offset [1], [2]. In recent years, several improved drain-engineered MOSFET's, such as MLDD [3], ITLDD [4], GOLD [5], and LATID [6], have received much attention because of their abilities to enhance current drivability and alleviate spacer-induced degradation [2]. However, there is no unified solution for analyzing the hot-carrier reliability in various drain-engineered devices.

In the past, normally we use drain current degradation $(\Delta I_D/I_D)$, threshold voltage shift voltage shift (ΔV_T), transconductance degradation $(\Delta g_m/g_m)$, or substrate current (I_B) for comparing the hot-carrier reliability of MOS devices [7]. However, to compare the hot-carrier effect in drain-engineered MOSFET's, the commonly used substrate current or total amount of generated interface states is not a sufficient criterion. On the other hand, since interface state generation is the dominant mechanism responsible for the variation of the above characteristics, determination of the interface states, in particular its spatial distributions, becomes critical to a device engineering work. For example, the drain current degradations $(\Delta I_D/I_D)$ are closely related to the distribution of hot-carrier induced interface states and device parameters such as n^- doping profile and gate oxide thickness [1], [8]. Therefore, to get insight into the degradation process of drain-engineered device in more detail, it is essential to first physically characterize the interface state $(N_{\rm it})$ profile.

To deal with the aforementioned problems, in this paper, we will propose an efficient profiling technique to characterize the lateral distribution of $N_{\rm it}$ and to show its applications for a drain engineering work. Section II describes the device parameters and hot-carrier stress conditions used in this study. Section III presents an improved charge pumping profiling technique and the characterization results of $N_{\rm it}$ distributions. Section IV demonstrates an application of this new method to study the structure-dependent hot-carrier degradation in various drain-engineered MOSFET's. A summary and conclusion are given in Section V.

TABLE I
MAJOR DEVICE PARAMETERS FOR DEVICES USED IN THIS STUDY

Device / Device type / Parameters	LDD	LATID	MLDD
T_{ox} (Å)	140	140	140
n^- Dose (cm^{-2})	2.0×10^{13}	4.0×10^{13}	4.0×10^{13}
Energy (keV)	80	80	80
Angle	0°	45°	0°
L_{mask}/L_{eff}	0.7/0.64	0.7/0.43	0.7/0.51
V_T (V)@V_{BS}=0V	0.7845	0.7773	0.7545
I_{D}@V_{DS}=V_{GS}=5V (mA)	7.87	9.62	9.02

II. Device Preparation and Experimental Conditions

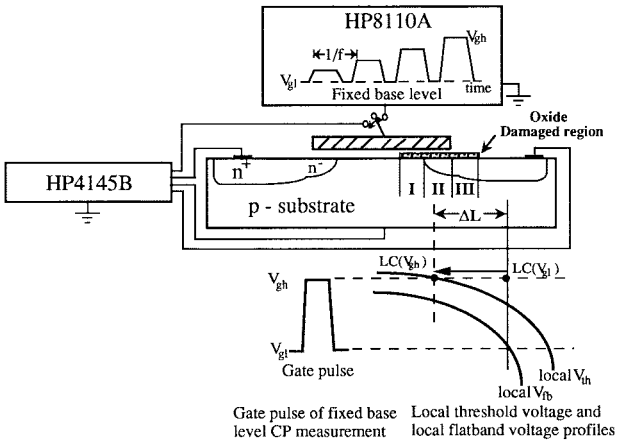
Various submicron n-channel LDD devices with different drain-engineering were fabricated using standard polysilicon gate CMOS process. Table I lists the device process conditions. Threshold voltage adjustment was performed by 70 KeV BF_2 ions at a dose of 3.2×10^{12} cm^{-2}. For 45° LATID device, the phosphorus implanted n^- region was performed by a 45° tilt angle implantation from the source and drain

Manuscript received December 3, 1998. This work was supported by the National Science Council, Taiwan, R.O.C., under Contract NSC82-0404-E009-377. The review of this paper was arranged by Editor M. Fukuma.

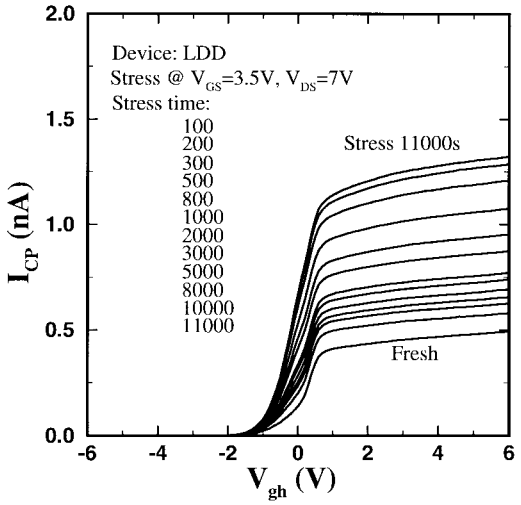
S. S. Chung is with the Department of Electronic Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: schung@cc.nctu.edu.tw).

J.-J. Yang was with the Department of Electronic Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. He. is now with WSMC, Hsinchu 300, Taiwan, R.O.C.

Publisher Item Identifier S 0018-9383(99)05067-4.



(a)



(b)

Fig. 1. (a) Experimental setup and principles of the interface state profiling technique. (b) Time evolution of measured $I_{\rm CP}$-$V_{\rm gh}$ relationship during hot-carrier stress using fixed based level CP measurement.

sides by rotating the wafer automatically. Sidewall spacer were processed by CVD SiO_2 deposition followed by reactive ion etching, the resultant width $(X_{\rm sp})$ is 0.15 μm for all device. N^+ source and drain were formed by 80 KeV arsenic implantation at a dose of 3×10^{15} cm^{-2}. The masked gate width of all devices are 20 μm. Several important device parameters such as drawn channel length $(L_{\rm mask})$, extracted geometrical effective channel length $(L_{\rm eff})$, threshold voltage (V_T), and current drivability (evaluated at $V_{\rm DS} = V_{\rm GS} = 5$ V) are also listed in Table I. All devices were stressed at $V_{\rm GS} = 3.5$ V and $V_{\rm DS} = 7$ V for hot-carrier reliability evaluation.

III. The Interface State Profiling Technique

A. Experimental Setup of CP Measurement

The experimental setup for CP measurement is shown in Fig. 1. The source, drain and bulk electrodes of tested device were grounded. A 1 MHz square pulse waveform provided by HP8110A with fixed base level $(V_{\rm gl})$ and varying high level $(V_{\rm gh})$ was applied to the gate. We keep $V_{\rm gl}$ at -6 V and increase $V_{\rm gh}$ from -6 V to 6 V with 0.1 V step. The voltage step will affect the profiling resolution. Parameter analyzer HP4145B was used to measure the charge pumping current $(I_{\rm CP})$.

B. Derivation of $\Delta N_{\rm it}(x)$ from $I_{\rm CP}$-$V_{\rm gh}$ Relationship

The local threshold voltage $(V_{\rm th})$ and local flatband voltage $(V_{\rm fb})$ along the surface of a device is not laterally uniform due to the variation of doping profile. As illustrated in Fig. 1(a), for a certain $V_{\rm gh}$ value, only interface states in the region ΔL can be detected and contribute to $I_{\rm CP}$, where ΔL is the difference between $LC(V_{\rm gl})$ and $LC(V_{\rm gh})$, $LC(V_{\rm gl})$ and $LC(V_{\rm gh})$ are the positions where local $V_{\rm fb}$ equals $V_{\rm gl}$ and local $V_{\rm th}$ equals $V_{\rm gh}$, respectively. $V_{\rm gl} = -6$ V is believed to be much lower than local $V_{\rm fb}$ at the most right end of damaged region along the SiO_2/Si interface. The measured $I_{\rm CP}$ versus $V_{\rm gh}$ characteristics for fresh and stressed devices are shown in Fig. 1(b). $I_{\rm CP}$ increases with stress time, which means that $N_{\rm it}$ is generated continuously.

In a fixed base level CP measurement [9], the $\Delta I_{\rm CP}$ ($I_{\rm CP}$(stressed)-$I_{\rm CP}$(fresh)) as a function of the $V_{\rm gh}$ can be analytically expressed as

$$\Delta I_{\rm CP} = f \cdot q \cdot W \cdot \int_{V_{\rm gl}}^{V_{\rm gh}} D_{\rm it}(V)\, dV \tag{1a}$$

$$= K \cdot \int_{V_{\rm gl}}^{V_{\rm gh}} D_{\rm it}(V)\, dV \tag{1b}$$

in which, $D_{\rm it}(V_{\rm gh})$ (in unit cm$^{-1} \cdot$V^{-1}) is the density of hot-carrier induced interface states at a position where the local threshold voltage is $V_{\rm gh}$, f is the gate pulses frequency, W is the channel width and $K = f \cdot q \cdot W$. Taking the first derivative of $\Delta I_{\rm CP}$ with respect to $V_{\rm gh}$ gives

$$D_{\rm it}(V_{\rm gh}) = \frac{1}{K} \cdot \frac{d\Delta I_{\rm CP}(V_{\rm gh})}{dV_{\rm gh}}. \tag{2}$$

Since increasing $V_{\rm gh}$ widens the detectable damaged region toward the channel direction, indeed, the $V_{\rm gh}$ versus detected length relationship implies the spectroscopy of local threshold voltage. In other words, $V_{\rm gh} - x$ (x is position coordinate, the origin is set at the point where $V_{\rm fb} = V_{\rm gl}$) relationship is identical to that of $V_{\rm th} - x$. By changing the integral variable from voltage to position, (1b) becomes

$$\Delta I_{\rm CP} = K \cdot \int_0^{x_1} D_{\rm it}(V) \frac{dV}{dx}\, dx \tag{3}$$

in which x_1 is the position where $V_{\rm gh}$ equals $V_{\rm th}$. Let

$$\Delta N_{\rm it}(x) = D_{\rm it}(V_{\rm gh}) \frac{dV_{\rm gh}}{dx} \tag{4}$$

(3) can be rewritten as

$$\Delta I_{\rm CP} = K \cdot \int_0^{x_1} \Delta N_{\rm it}(x)\, dx \tag{5}$$

where $\Delta N_{\rm it}(x)$ (in unit cm^{-2}) is the lateral distribution of generated $N_{\rm it}$. Substituting (2) into (4), $\Delta N_{\rm it}(x)$ is rearranged as

$$\Delta N_{\rm it}(x) = \frac{1}{K} \cdot \frac{d\Delta I_{\rm CP}(V_{\rm gh})}{dV_{\rm gh}} \cdot \frac{dV_{\rm gh}}{dx} \tag{6a}$$

$$= \frac{1}{K} \cdot \frac{d\Delta I_{\rm CP}(V_{\rm gh})}{dV_{\rm gh}} \cdot \frac{dV_{\rm th}}{dx}. \tag{6b}$$

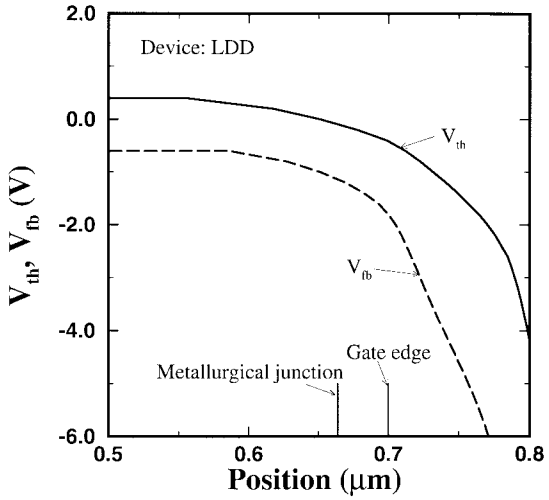


Fig. 2. Simulated local threshold voltage ($V_{\rm th}$) and local flat-band voltage ($V_{\rm fb}$) of LDD device.

Assuming no fixed oxide charges are generated during stress at $I_{B,\rm MAX}$ bias, local threshold voltage will not be altered. By calculating local threshold voltage from two-dimensional (2-D) device simulation and $d\Delta I_{\rm CP}(V_{\rm gh})/dV_{\rm gh}$ from measured $\Delta I_{\rm CP}$-$V_{\rm gh}$ curves, (6b) provides us a simple and accurate way to a simple and accurate way to characterize $\Delta N_{\rm it}(x)$ directly from CP measurement.

C. Simulation of the Local Threshold Voltage

For an n-MOSFET in CP measurement, the local threshold voltage (or flat-band voltage) of a point at the interface is defined as the gate voltage at which the free electron (or hole) concentration (n_e for electron, n_h for hole) at the surface is sufficiently large so that the fast interface states can capture electrons (or holes) during the time the gate pulse is applied [10]. The minimum required surface concentration $n_e(n_h)$ for electrons (holes) with time constant $\tau_e(\tau_h)$ and capture cross section $\sigma_n(\sigma_h)$ is given by

$$n_e = \frac{1}{\upsilon_{\rm th} \cdot \sigma_n \cdot \tau_e}. \tag{7}$$

For a 1 MHz symmetrical square gate pulse, we have τ_e $(= \tau_h = 1/2 \cdot f) = 5 \times 10^{-7}$ s. With $\sigma_n = \sigma_h = 2 \times 10^{-16}$ cm^{-2} and $\upsilon_{\rm th} = 1 \times 10^7$ cm/s, $n_e(n_h) = 1 \times 10^{15}$ cm^{-3}. Thus, for the given gate pulse train, the local threshold (flat-band) voltage of a point at interface is defined as the gate voltage that accumulates 1×10^{15} cm^{-3} electrons (holes) at the surface. The simulated shapes of $V_{\rm th}-x$ and $V_{\rm fb}-x$ relationship using Minimos 4.2 [11] are shown in Fig. 2.

D. Characterization Results and Discussion

Based on (6b), Figs. 1(b) and 2, the calculated $\Delta N_{\rm it}(x)$ distributions for the LDD device are given in Fig. 3. Minimos 4.2 was used to simulate the lateral surface electric field and normalized hot-carrier injection current density are also shown together for examining the appropriateness of the $N_{\rm it}$ profile. The hot-carrier injection current density at each position, $J_{x,\rm inj}(x)$, is calculated as

$$J_{x,\rm inj}(x) = C \cdot J_x(x) \cdot \exp\left(-\frac{\phi_{\rm it}}{q\lambda E_x(x)}\right) \tag{8}$$

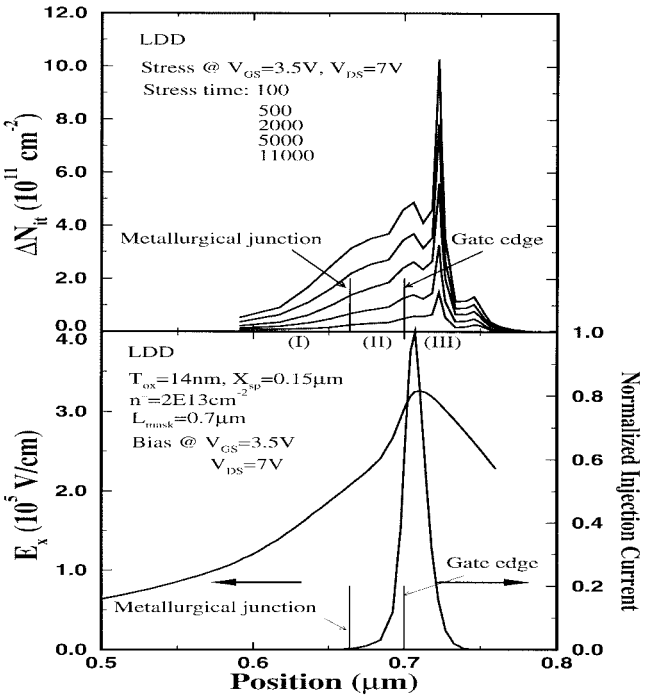


Fig. 3. Time evolution of characterized interface state profiles during hot-carrier stress for LDD device. The distributions of surface electric field and normalized hot-carrier injection current are also shown for comparison.

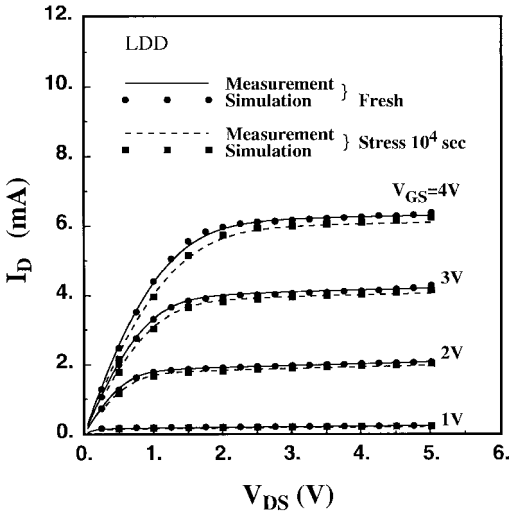


Fig. 4. The comparison of the drain current characteristics between simulation and measurement for both fresh and stressed devices.

where $J_x(x)$ and $E_x(x)$ are lateral components of local surface current density and electric field, respectively, $\phi_{\rm it} = 3.7$ eV, $\lambda = 67$ Å and $q = 1.6 \times 10^{-19}$ coulomb. $J_{x,\rm inj}$ is normalized to its maximum value. As illustrated in Fig. 1(a), we divide the hot-carrier damaged area into three regions: Region I is the channel region, Region II is the gate-to-n$^-$ overlapped region, and Region III is the sidewall spacer region. The discussion of the above results follows.

1) To show the validity of the characterized results in Fig. 3, the distributions of $\Delta N_{\rm it}(x)$ was incorporated into Minimos 4.2 [11] to simulate the drain current characteristics of stressed devices. First, by following

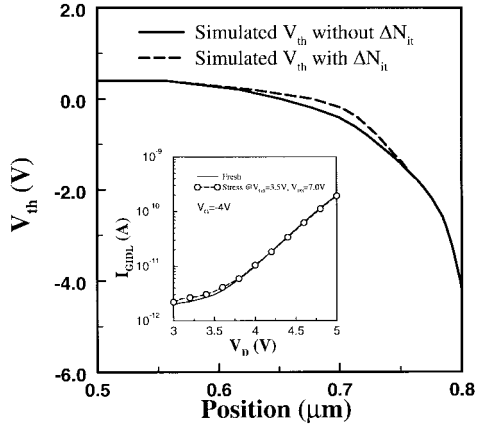


Fig. 5. Simulated local threshold voltage of LDD device without considering $N_{\rm it}$ effect (solid lines) and with considering $N_{\rm it}$ effect (dashed lines). The insert using GIDL current measurement is used to show no fixed oxide charges were generated during the stress.

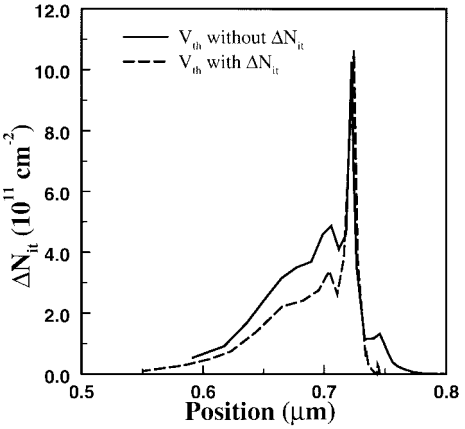


Fig. 6. The calculated interface state distributions of LDD device without considering $N_{\rm it}$ effect (solid lines) and with considering $N_{\rm it}$ effect (dashed lines).

the procedure described in [11] that process flow was set up and the channel profile, source/drain doping profile, and key mobility factors have been calibrated. The solid lines and dotted circles in Fig. 4 are the measured and simulated drain current characteristics respectively for devices before the stress (fresh). Results show pretty good agreements. This is to ensure the accuracy of the $V_{\rm th}-x$ results in this work. Then, to simulate the device drain current by including the $N_{\rm it}$ effect, an empirical mobility degradation formula [12] including Coulomb scattering and surface roughness enhanced scattering was incorporated for the 2-D device simulation. The dashed lines and solid rectangles in Fig. 4 shows the measured and simulated drain current characteristics after the stress at 10^4 s which shows very good match with measurement.

2) The electric field and hot-carrier injection current were simulated using DD (Drift-Diffusion) models. The peak position of $\Delta N_{\rm it}(x)$ after 11 000 s stress is separated from that of E_x and $J_{x,\rm inj}$ by 150 Å. Advanced device simulation [13] proved that this discrepancy is very reasonable due to nonlocal effect in submicron MOSFET's, because carriers need to travel sufficient distance to become energetic.
3) The peak values of generated interface states in LDD device are mostly located in Region III. The negatively charged interface states here are prone to reduce conducting carriers that increases series resistance, thus I_D is degraded. The characterized interface state profile gives direct evidence for the degradation mechanism of spacer-induced degradation in LDD devices.
4) For the $N_{\rm it}$ characterization in Fig. 3, it was assumed that no fixed oxide charge was generated which will make the method more simple. To show that the fixed oxide charge was not generated, we took a measurement of Gate Induced Drain Leakage (GIDL) current as shown in the insert of Fig. 5 ([14]) where we see that no oxide charge was generated in our device stress conditions. This can avoid the complicate determination of fixed oxide charge. On the other hand, the effect of $N_{\rm it}$ on the calculated $V_{\rm th}$ is shown in Fig. 5 (in dashed lines). Again, if these values of $V_{\rm th}$ are used for $N_{\rm it}$ calculation (6b), the $N_{\rm it}$ distribution is given in Fig. 6. The solid lines are the results without considering $N_{\rm it}$ effect, while the dashed lines are the results considering $N_{\rm it}$ effect. Here, we see that although there are much more difference for low values of $N_{\rm it}$, there is not much difference at the near peak $N_{\rm it}$ region. More importantly, the device degradation characteristics are determined mainly by the peak $N_{\rm it}$ values and the position of $N_{\rm it}$ as will be described in the next section. In such a case, it is reasonable to calculate $dV_{\rm th}/dx$ term in (6b) using $V_{\rm th}-x$ curves (Fig. 2) of fresh devices.

IV. Applications to Drain-Engineering Study

In the past, substrate current [7] or impact ionization rate is generally used as a monitor to evaluate MOS device hot-carrier reliability. But, in some cases, a device with larger substrate current may not have poorer drain current degradation. We will show in this section how to evaluate the drain current degradation correctly using the interface state profiling results. The application of the present method to the hot-carrier effect evaluation of MLDD, 45° LATID and LDD devices will be demonstrated. These include the substrate current (I_B), effective impact ionization rate (I_B/I_D), the spacer-induced degradation, and the drain current degradation of these devices.

A. The Comparison of Hot-Carrier Related Static Characteristics

Fig. 7 compares the I_B and I_B/I_D characteristics for three devices. MLDD device has the maximum I_B and I_B/I_D values. LDD device has minimum I_B values over the whole $V_{\rm GS}$ range, while its I_B/I_D at low $V_{\rm GS}$ is larger than 45° LATID due too its lower current drivability. Also, by comparing Figs. 7 and 8, we see that $\Delta I_{\rm CP}$ is proportional to I_B. If we use I_B as a monitor of the generated interface states, the induced total amount of $N_{\rm it}$ is proportional to the I_B value at stressed biases. Under this argument, the MLDD device is expected to suffer the most severe I_D drgradation, 45° LATID device is medium, and LDD device is the minimum. However,

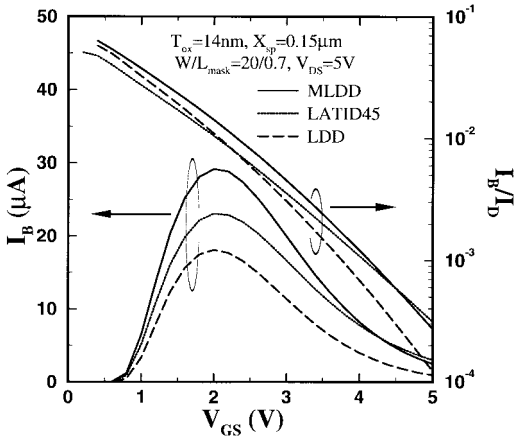


Fig. 7. Comparison of I_B and I_B/I_D characteristics for the MLDD, 45° LATID and LDD devices.

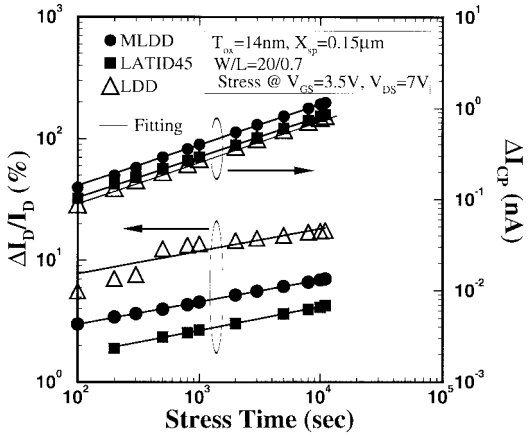


Fig. 8. Time evolution of $\Delta I_D/I_D$ and $\Delta I_{\rm CP}$ during hot-carrier stress for the devices MLDD1, LATID45 and LDD.

the results are just the opposite. From the comparison shown in Fig. 8, the drain current degradation for three devices, we see that LDD device suffers the most severe I_D degradation than the others at the same stress time, 45° LATID has the minimum I_D degradation. Obviously, the above indicator using I_B (Fig. 7) can not explain the results shown in Fig. 8.

B. Structure-Dependent Hot-Carrier Effect

In order to solve the discrepency between Figs. 7 and 8, our results of $N_{\rm it}$ distributions in Fig. 9 can be used to explain the drain current degradation correctly. As a consequence, we can draw a criterion by using $N_{\rm it}$ profiles as a good monitor of device hot-carrier reliability. Fig. 9 compares the $N_{\rm it}$ profile for the MLDD, 45° LATID and LDD devices after 11 000 s stress. Channel electric field is also plotted together for comparing its correlation with $N_{\rm it}$ profile. More details are described as follows.

1) The peaks of interface state profiles are all located outside gate edge, therefore, all three devices suffer spacer-induced degradation. The spacer-induced degradation [2] is driven by the increase of drain region series resistance. Fig. 10 shows that the trend of variation of the series resistance increment (extracted using a method in [15]) is the same as that of $\Delta I_D/I_D$. LDD device suffers the most severe spacer-induced degradation since it has the largest $N_{\rm it}$ peak values underneath the spacer. While, in MLDD, spacer-induced degradation is smaller and is less significant in 45° LATID device. This reveals that the spacer-induced degradation dominates the drain current degradations for LDD devices with spacer structure.
2) From the calculated total amount of interface states in each damaged region, we found that the dominant damaged region for MLDD device is Region II, for 45° LATID device is Region II, and for LDD device

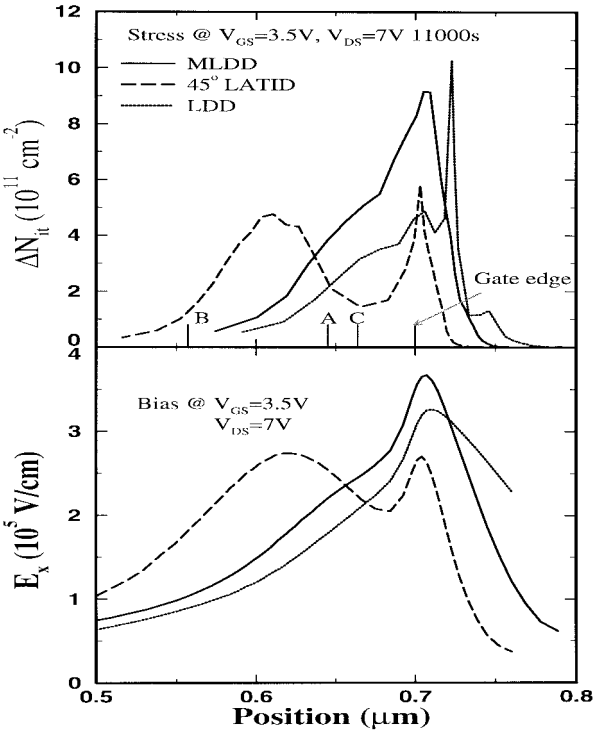


Fig. 9. Comparison of interface state profile for MLDD, 45° LATID and LDD devices after 11 000 s stress. The surface electric field profiles are also shown for examining their relations with interface state profiles. Positions A, B, and C are the drain/bulk junctions for MLDD, 45° LATID and LDD devices, respectively.

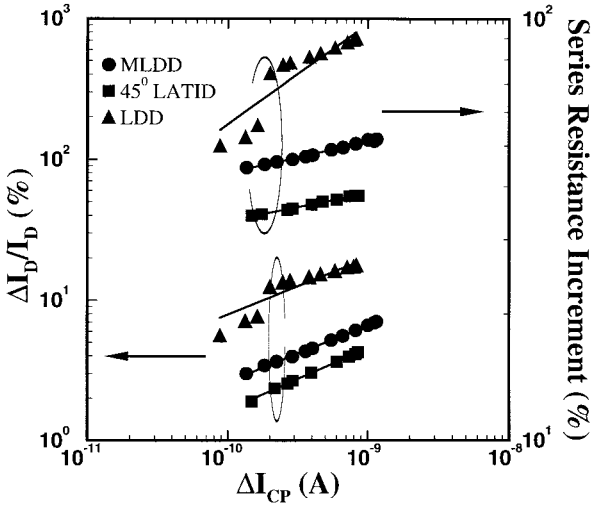


Fig. 10. Linear region drain current degradation and series resistance increment versus the amount of generated interface states. $\Delta I_D/I_D$ is evaluated at $V_{\rm DS} = 0.1$ V and $V_{\rm GS} = 5$ V.

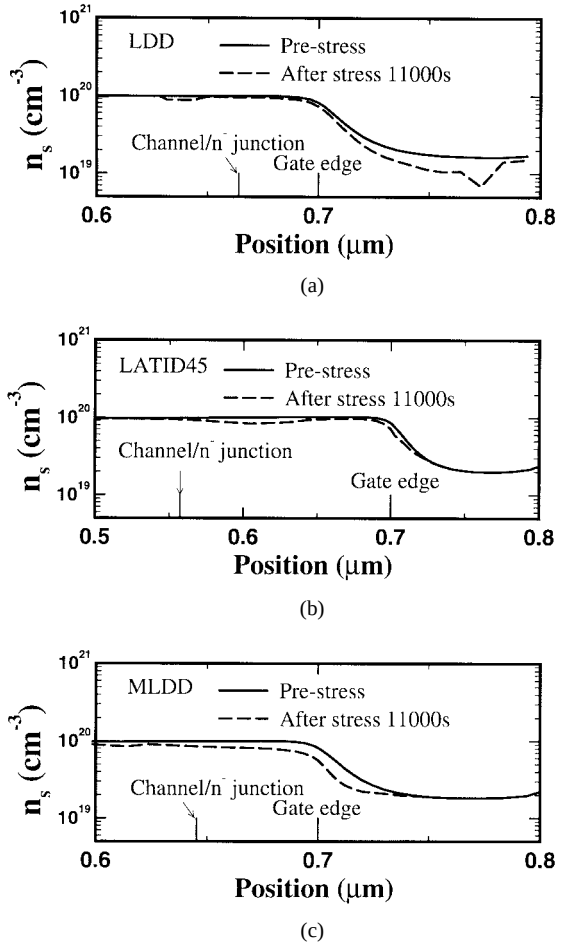


Fig. 11. Reduction of surface electron concentration after 11 000 s stress for the devices (a) LDD, (b) LATID45, and (c) MLDD.

is Region III. Fig. 11 shows the simulated variation of device surface electron concentration before stress and after stress 11 000 s for LDD and LATID45 respectively. For LDD, it has the largest N_{it} peak and the position of peak is located far from gate edge as compared with the others such that the reduction of electron concentration [Fig. 11(a)] is very significant owing to its lighter n^- region doping concentration, which increase the series resistance in the spacer region. It is this serious series resistance effect that causes LDD having the largest I_D degradation.

3) In contrast to LDD device, MLDD device has a little higher n^- concentration than that of LDD device such that the resistance effect is weaker as shown in Fig. 11. By examining N_{it} profils of MLDD and LDD, increasing n^- dosage can move the dominant damaged region toward channel direction as illustrated in Fig. 12, which increases gate controllability over damaged region. This fact helps alleviating the series resistance effect in MLDD.
4) The n^- tilt angle implantation makes the LATID45 having the peak N_{it} values inside the gate edge. The electric field is distributed widely with smallest peak value among all three devices. In addition, LATID45 has smaller reduction of electron concentration in the gate/n^- overlapped region as given in Fig. 11(b) and hence much less resistance increment effect in Fig. 10. These show that LATID45 has the smallest I_D degradation and why LATID45 device can alleviate the hot-carrier effect.

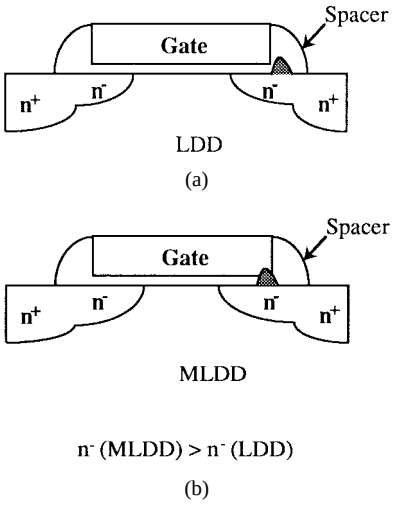


Fig. 12. Schematic diagrams for (a) the conventional LDD devce and (b) the MLDD device. The bell-shape regions indicate the location of maximum hot-carrier injection regions. The n^- dosage of the MLDD device is larger than that of conventional LDD device.

C. Discussion

The present method is superior to those in [16]–[18]. First, in [16] and [18], the depletion width is calculated by analytical formula [16] (based on the depletion approximation formula between V_{db} and depletion layer width) or determined experimentally [18] which may limit profiling accuracy. Secondly, the measurement causes unintentional re-stress effect repeatedly in [16], [17] since a large drain bias is applied during the experiments. Thirdly, the method in [18] can not be applied to LDD device structures since it used the gate length as a reference point where N_{it} is determined inside the gate length (Figs. 6 and 8 in [18]). For the devices being studied, the region under the spacer region will also contribute to the charge pumping current such that most of the N_{it} distribution will cover both the gate-drain overlap region and the spacer region. The present method can achieve this purpose based on the I_{cp}-V_{gh} plot and the simulated $V_{th}-x$ curves. While, the method in [18] based on the experimentally determined $V_{th}-x$ profile is not adequate for application in LDD device structures. Finally, both papers only dealt with the spatial distribution of N_{it}, no criterion was provided to correlate the device degradation with N_{it} distributions for a device drain engineering study.

In short, the conventional criterion using I_B for monitoring the device reliability is not a sufficient criterion for device drain engineering study. The I_D degradation of a drain-engineered MOSFET should be compared based on the extent of the peak position of N_{it} and its peak values. In other words, the more the interface statesare generated inside the spacer region, the larger the drain current degradation becomes. With a tradeoff between the use of n^- implantation dosage and angle, the design optimization of a hot-carrier

resistant MOS device can be better understood through the use of the newly proposed method.

V. Conclusion

In this paper, an efficient interface state profiling technique is proposed to study the hot-carrier reliability of drain-engineered submiron LDD n-MOSFET's. Interface state profiling was first developed based on the charge pumping measurement technique. The developed profiling technique is then applied to study the structure-dependent hot-carrier effects in various drain structure LDD devices. In particular, *a new criterion based on the observation of the $N_{\rm it}$ distribution is a good and correct monitor for hot-carrier reliability evaluation*. We should keep the peak values of $N_{\rm it}$ far away from the spacer region in order to obtain better device reliability. For LDD structure devices in our studies, spacer-induced degradation is inevitable. The series resistance effect induced by the interface state is the origin of device drain current degradation. The larger the generated interface states in the spacer region, the worse the device drain current degradation. LATID device or increasing n^- doping of an LDD device provides a way to reduce hot-carrier effect since most of generated interface states are located away from the spacer region such that the above series resitance effect becomes weak. With a tradeoff between the use of n^- implantation dosage and angle, we conclude that the design optimization of a hot-carrier resistant MOS device can be better understood through the use of the newly proposed method.

References

[1] Y. Toyoshima, H. Nihira, M. Wada, and K. Kanzaki, "Mechanism of hot electron induced degradation in LDD NMOS-FET," in *IEDM Tech. Dig.*, 1984, pp. 786–789.

[2] F.-C. Hsu and H. R. Grinolds, "Structure-enhanced MOSFET degradation due to hot-electron injection," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 71–74, Mar. 1984.

[3] M. Kinugawa, M. Kakuma, S. Yokogawa, and K. Hashimoto, "Submicron MLDD NMOSFET for 5 V operation," in *Symp. VLSI Technol., Tech. Dig.*, 1985, pp. 116–117.

[4] T.-Y. Huang, W. W. Yao, R. A. Martin, A. G. Lewis, M. Koyanagi, and J. Y. Chen, "A novel submicron LDD transistor with inverse-T gate structure," in *IEDM Tech. Dig.*, 1986, pp. 742–745.

[5] R. Izawa, T. Kure, S. Iijima, and E. Takeda, "The impact of gate-drain overlapped LDD (GOLD) for deep submicron VLSI's," in *IEDM Tech. Dig.*, 1987, pp. 38–41.

[6] T. Hori, K. Kurimoto, T. Yabu, and G. Fuse, "A new submicron MOSFET with LATID (large-tilt-angle implanted drain) structure," in *Symp. VLSI Technol., Tech. Dig.*, 1988, pp. 15–16.

[7] C. Hu, S. Tam, F.-C. Hsu, P. K. Ko, and K. W. Terril, "Hot-electron induced MOSFET degradation-model, monitor and improvement," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 375–385, 1985.

[8] Y. Toyoshima, H. Iwai, F. Matsuoka, H. Hayashida, K. Maeguchi, and K. Kanzaki, "Analysis on gate-oxide thickness dependence of hot-carrier-induced degradation in thin-oxide nMOSFET's," *IEEE Trans. Electron Devices*, vol. ED-37, pp. 1496–1503, 1990.

[9] R. G.-H. Lee, J. P. Wu, and S. S. Chung, "An efficient method for characterizing time-evolutional interface state and its correlation with the device degradation in LDD n-MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-43, pp. 898–903, 1996.

[8] T. Poorter and P. Zoestbergen, "Hot carrier effects in MOS transistors," in *IEDM Tech. Dig.*, 1984, pp. 100–103.

[10] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE Trans. Electron Devices*, vol. 36, pp. 1318–1335, 1989.

[11] J.-J. Yang, S. S. Chung, C.-H. Chang, and G.-H. Lee, "A unified 3-D mobility model for simulation of submicron MOS device," *Jpn. J. Appl. Phys.*, vol. 32, pp. 1583–1589, 1993.

[12] S. C. Sun and J. D. Plummer, "Electron mobility and accumulation layers on thermally oxidized silicon surface," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1497–1508, 1980.

[13] T. Wang, C. Huang, P.-C. Chou, S. S. Chung, and T.-E. Chang, "Effects of hot-carrier induced interface state generation in submicron LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, pp. 1618–1622, 1994.

[14] K. T. San and T. P. Ma, "Determination of trapped oxide charge in flash EPROM's and MOSFET's with thin oxides," *IEEE Electron Device Lett.*, vol. 13, pp. 439–441, 1992.

[15] Y. Pan, K. K. Ng, and C. C. Wei, "Hot-carrier induced electron mobility and series resistance degradation in LDD NMOSFET's," *IEEE Electron Device Lett.*, vol. 15, pp. 499–501, 1994.

[16] M. G. Ancona, N. S. Saks, and D. McCarthy, "Lateral distribution of hot-carrier-induced interface traps in MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, pp. 2221–2228, 1988.

[17] W.-L. Chen, A. Balasinski, and T.-P. Ma, "Lateral profiling of oxide charge and interface traps near MOSFET junctions," *IEEE Trans. Electron Devices*, vol. 40, pp. 187–195, 1993.

[18] C. Chen and T.-P. Ma, "Direct lateral profiling of hot-carrier-induced oxide charge and interface traps in thin gate MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, pp. 512–520, 1998.

Steve S. Chung (S'83–M'85–SM'95) received the B.S. degree (highest honors) from the National Cheng-Kung University, Taiwan, R.O.C., in 1973, the M.Sc. degree from the National Taiwan University in 1975, and the Ph.D. degree from the University of Illinois, Urbana-Champaign, in 1985, all in electrical engineering.

From 1976 to 1978, he was with an electronic instrument company as Director of the R&D Division and subsequently, as Manager of the Engineering Division. From 1978 to 1983, he was with the Department of Electronic Engineering and Technology at the National Taiwan Institute of Technology (NTIT) as a Lecturer. He was also in charge of an Instrument Calibration Center at NTIT. From 1983 to 1985, he held a research assistantship in the Solid State Electronics Laboratory and the Department of Electrical and Computer Engineering at the University of Illinois. In September 1985, he served at NTIT again as an Associate Professor in the Department of Electronic Engineering. Since August 1987, he has been with the Department of Electronic Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, and has been a Full Professor since the Fall of 1989. His current teaching and research interests are in the areas of device physics, deep-submicron CMOS VLSI technology; SPICE device modeling; numerical simulation and modeling of submicron and deep-submicron MOS devices, SOI devices, nonvolatile memories and TFT's; characterization and reliability study of VLSI devices and circuits; and computational algorithms for VLSI circuits. He is a co-holder of ten US and ROC patents.

Dr. Chung has served on various technical program committees of IEEE ASIC Conference (U.S.), International Electron Devices and Materials Symposium (IEDMS, Taiwan), and HPC (High Performance Computing)-ASIA'95. He is the recipient of the 1996–1998 Distinguished Research Award from the National Science Council, Taiwan.

Jiuun-Jer Yang received the B.S. degree from Nation Cheng-Kung University, Tainan, Taiwan, R.O.C., and the M.S. and Ph.D. degrees from National Chiao-Tung University, Hsinchu, Taiwan, all in electrical engineering, in 1989, 1991, and 1995, respectively.

Currently, he is a Deputy Manager at the Technology Development Center, Worldwide Semiconductor Manufacturing Corporation, Hsinchu Science-Based Industrial Park, Taiwan, where he is engaged in TCAD and reliability evaluation for advanced processes. His research interests include process/device reliability, process/device modeling, device design, and TCAD.