A 10-Gb/s OEIC with Meshed Spatially-Modulated Photo Detector in 0.18-μm CMOS Technology

Shih-Hao Huang, Wei-Zen Chen, Yu-Wei Chang, and Yang-Tung Huang

***Abstract*—This paper describes the design of a 10-Gb/s fully integrated CMOS optical receiver, which consists of a novel spatially-modulated photo detector (SMPD), a low-noise trans-impedance amplifier (TIA), and a post-limiting amplifier on a single chip. The bandwidth of proposed meshed SMPD can be boosted up to 6.9 GHz under a reverse-biased voltage of 14.2 V. The measured responsivity of the meshed SMPD is 29 mA/W as illuminated by 850-nm light source. To compensate the relatively low responsivity of on-chip CMOS photo detector (PD), a high-gain TIA with nested feedback and shunt peaking is proposed to achieve low-noise operation. The optical receiver is capable of delivering 25-kΩ conversion gain when driving 50-Ω output loads. For a PRBS test pattern of 2^7-1, the 10-Gb/s optoelectronic integrated circuit (OEIC) has optical sensitivity of -6 dBm at a bit-error rate (BER) of 10^{-11}. Implemented in a generic 0.18-μm CMOS technology, the chip area is 0.95 mm by 0.8 mm. The trans-impedance amplifier, post amplifier, and output buffer respectively drain 38 mW, 80 mW, and 27 mW from the 1.8-V supply.**

***Index Terms*—Optical receiver, optoelectronic integrated circuit (OEIC), spatially-modulated photo detector (SMPD), trans-impedance amplifier (TIA), limiting amplifier (LA).**

I. Introduction

DATA communication over optical links benefits from wider bandwidth and lower channel loss compared to electrical counterparts. They are widely deployed for long-haul telecommunications as network backbone. Nowadays, with the increasing speed of backplane interconnects and electronics devices interfaces for short reach data link, such as HDMI [1], [2], USB [2], and light peak [3] technologies, optical links are drawing more and more attentions in these applications for their superiorities in less cross-talk, lower EMI, and fewer equalizer needed for data rate up to 10 Gb/s. Conventionally, an optical receiver is composed of multi-chips in different technologies [4]–[7]. For example, the PD is implemented in more expensive InGaAs or GaAs technology, while the TIA and post-limiting amplifier are fabricated using Bipolar/CMOS or BiCMOS process, as is shown in Fig. 1(a). To realize a cost effective optical receiver front-end for pervasive adaptation, monolithically integrated optoelectronic integrated circuits (OEICs) have drawn tremendous research efforts [8]–[17] recently. As shown in Fig. 1(b), an on-chip PD, a TIA, and a post-limiting amplifier are integrated on a single chip. It benefits from less cross-talk and interference by eliminating bonding wire inductor ($L_{\rm wire}$) for system chips integration. Besides, its signal bandwidth can be increased by eliminating the bonding pad and ESD parasitic capacitance ($C_{\rm pad1}$ and $C_{\rm pad2}$) at the input node of TIA. They provide potential solutions to sustain high-speed and data-intensive platform in the future [3].

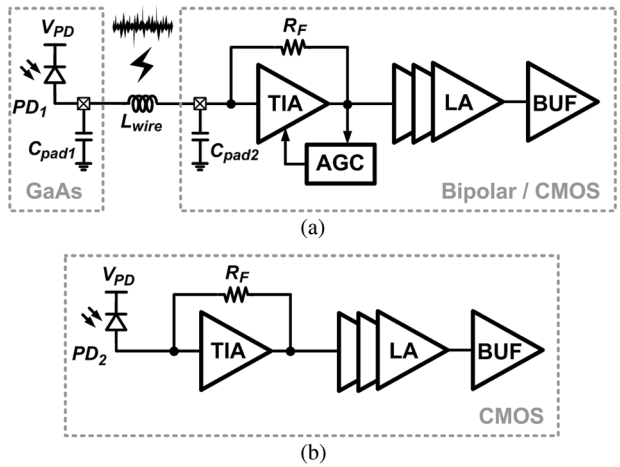

Fig. 1. (a) Hybrid and (b) monolithic optical receiver front-end.

Light detection in CMOS technology is performed by a reverse-biased P/N junction diode, which is mainly comprised of the substrate to well junction and diffusion to well junction. As the penetration depth (16.7 μm) of the 850-nm light into silicon is much deeper than the shallow well or diffusion region, a large portion of carriers are generated in the substrate and lead to slowly diffusive currents, which limit the operating speed of photo detector to tens of MHz range.

Typically, the bandwidth of OEIC can be enhanced to achieve high-speed operation by getting rid of the slowly diffusive carriers in the photo detector [8]–[17]. From technology aspect, this approach can be achieved by using SOI [9] or BiCMOS [10] process, but it requires non-standard CMOS technology and additional cost. [11] proposes a CMOS photo detector comprising of diffusion/well junctions and employing deep $\rm N_{well}$ for $\rm P_{substrate}$ diffusive carrier isolation. However, the photo detector exhibits an 8X larger parasitic capacitance that impedes high-speed operation. To reduce the parasitic capacitance of the CMOS photo diodes, [12] employs a $\rm P_{diffusion}/N_{well}$ PD with the active region of 16.54 μm by 16.54 μm, which is only 1/9 the cross-sectional area of a multi-mode fiber. But it also suffers from the degradation of responsivity.

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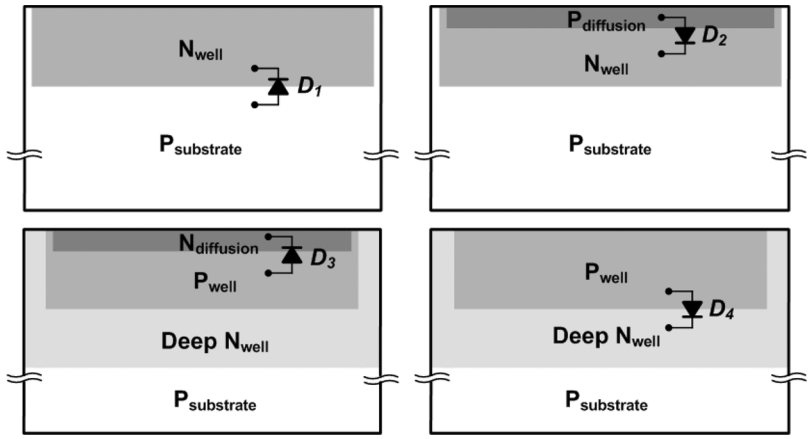


Fig. 2. P/N photo diodes in generic triple-well CMOS technology.

On the other hand, the PD bandwidth can also be compensated with an equalizer from circuit prospective [10], [15]–[17]. However, due to the slowly roll-off characteristic of the CMOS-PD frequency response [17], a high-order and sophisticated equalizer is required for practical usage under PVT variations.

To realize a high-speed CMOS optical receiver, a meshed spatially-modulated photo detector (SMPD) is proposed in this design. Compared to conventional strip SMPD [8], [13]–[16], it increases the effectiveness of slow-carrier cancellation by equalizing the diffusive distance. A common shortage of SMPD is its relatively lower responsivity, it demands more stringent noise performance for the succeeding amplification stage. In this paper, a low-noise TIA with nested feedback is also proposed to achieve the design goal.

This paper is organized as follows. Section II describes the photo detectors in CMOS technology, including conventional P/N photo diodes, the strip SMPD, and the proposed meshed SMPD. Section III describes the detail circuit implementation of this 10-Gb/s OEIC. Section IV summarizes the measurement results, and Section V gives a conclusion.

II. CMOS Photo Detectors

A. Conventional P/N Junction Photo Diodes

Fig. 2 shows the conventional P/N junction PDs in CMOS technology. The depletion regions for photo sensing in D_1, D_2, D_3, and D_4 are composed of $\mathrm{P_{substrate}/N_{well}}$, $\mathrm{P_{diffusion}/N_{well}}$, $\mathrm{P_{well}/N_{diffusion}}$, and $\mathrm{P_{well}/deep\ N_{well}}$ junctions respectively.

As D_1 is illuminated, the depletion region generates fast drift current whereas the neutral P-region and N-region generate slow diffusion current. Because the depth for the $\mathrm{N_{well}}$ region is shallow ($< 3\ \mu$m) from the silicon surface and the absorption length of silicon is about 16.7 μm at 850-nm wavelength, there is approximately only 16% of the photon absorption in the well region, and a large portion of photocurrent is generated in the $\mathrm{P_{substrate}}$ region, which leads to slow diffusion current. It severely limits the bandwidth of D_1. To eliminate the diffusive current generated in the $\mathrm{P_{substrate}}$ region, D_2, D_3, and D_4 are surrounded by $\mathrm{N_{well}}$ or deep $\mathrm{N_{well}}$ to achieve wider bandwidth.

Under the reversed biased-voltage of 1.2 V, the octagon PDs (from D_1 to D_4) with the span of 55 μm have capacitances of 299 fF, 1952 fF, 1773 fF, and 1233 fF respectively by simulation. In spite of bandwidth improvement of D_2, D_3, and D_4, their shallower P-region and N-region with heavier doping concentration result in lower responsivity, and introduce larger junction capacitance to the TIA. On the contrary, D_1 has a better responsivity [17] and smallest intrinsic parasitic capacitance. To circumvent its bandwidth limitation, spatially-modulated layout topology with $\mathrm{P_{substrate}}$ to $\mathrm{N_{well}}$ junction PD is proposed.

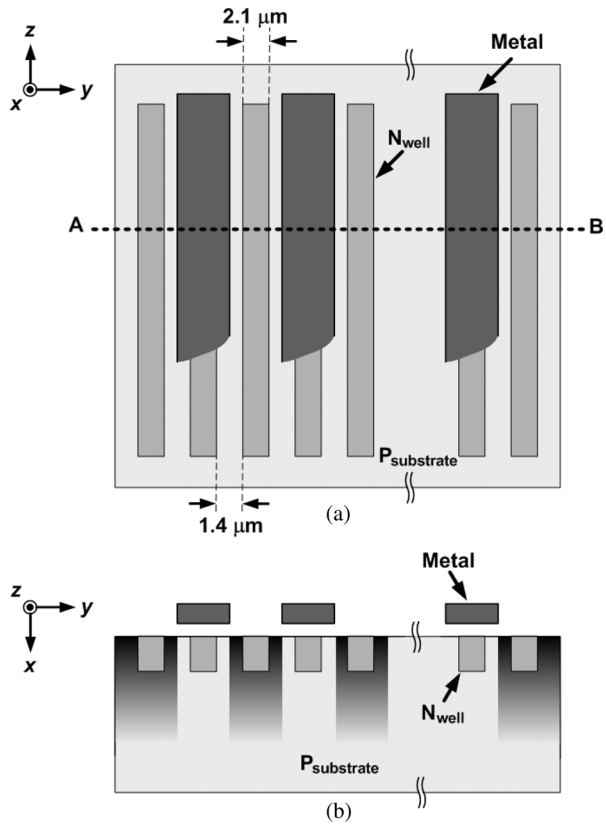


Fig. 3. (a) Top view and (b) cross-sectional view of a strip SMPD.

B. Strip SMPD

Fig. 3 shows the layout view and cross-sectional view of strip SMPD, which is composed of a row of $\mathrm{P_{substrate}}$ to $\mathrm{N_{well}}$ junction photo detectors alternately covered and uncovered with

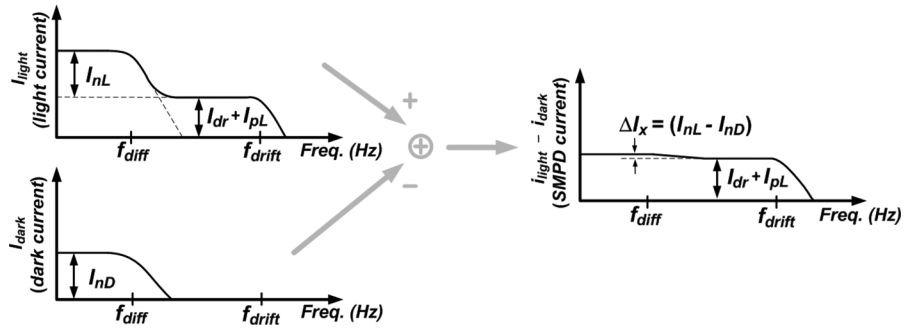


Fig. 4. Frequency response of a spatially-modulated PD.

light-blocking materials, such as metal layers. The covered detectors are named dark detectors, while the uncovered detectors are named light detectors. As the slow diffusive carriers from $\mathrm{P}_{\mathrm{substrate}}$ diffuse in all directions, the light detectors capture the fast drift carriers and slow diffusive carriers, while the dark detectors capture only the slow diffusive carriers. Fig. 4 depicts the photo current components of the light detectors and dark detectors. By applying the outputs of dark and light detectors to a differential TIA, the slowly diffusive carriers can be partially removed. Let I_{nL} and I_{nD} respectively represent the electron diffusion current of the light and dark detectors in the $\mathrm{P}_{\mathrm{substrate}}$ neutral region, I_{pL} be the hole diffusion current in the $\mathrm{N}_{\mathrm{well}}$ neutral region, and I_{dr} be the drift current in the depletion region. The differential photo current of SMPD can be expressed as $(I_{\mathrm{light}} - I_{\mathrm{dark}})$

$$\begin{aligned} I_{\mathrm{light}} - I_{\mathrm{dark}} &= (I_{nL} + I_{dr} + I_{pL}) - I_{nD} \\ &= (I_{nL} - I_{nD}) + I_{dr} + I_{pL} \end{aligned} \tag{1}$$

Since I_{dr} is a high-speed component and I_{pL} also has wide-bandwidth response thanks to shallow diffusion depth, the remaining differential current component $(I_{nL} - I_{nD})$ would determine the overall PD bandwidth according to (1). By applying this spatially-modulated layout topology, the -3-dB bandwidth of strip SMPD can be increased from about 10 MHz to 850 MHz [15]. However, it is still insufficient for multi-Gb/s operations.

C. Meshed SMPD

In order to more effectively cancel the slowly diffusive carriers, this paper proposes two-dimensionally meshed SMPD architecture. The layout view and cross-sectional view of the meshed SMPD are shown in Fig. 5(a) and Fig. 5(b) respectively. A meshed SMPD consists of a mesh of photo detectors alternatively covered and uncovered by light blocking metal layer. Compared to the prior art using a strip SMPD layout scheme, the slow diffusive carriers generated from $\mathrm{P}_{\mathrm{substrate}}$ can be more equally captured by the neighbored dark detectors. Also, the meshed structure reduces the distance that photo carriers drift. Thus, it benefits from smaller R-C delay and wider intrinsic bandwidth. As a result, high-speed optical detection can be achieved by the proposed meshed SMPD, but at the expense of reduced responsivity because a large portion of carriers are slowly diffusive and removed by using the spatially-modulated layout topology.

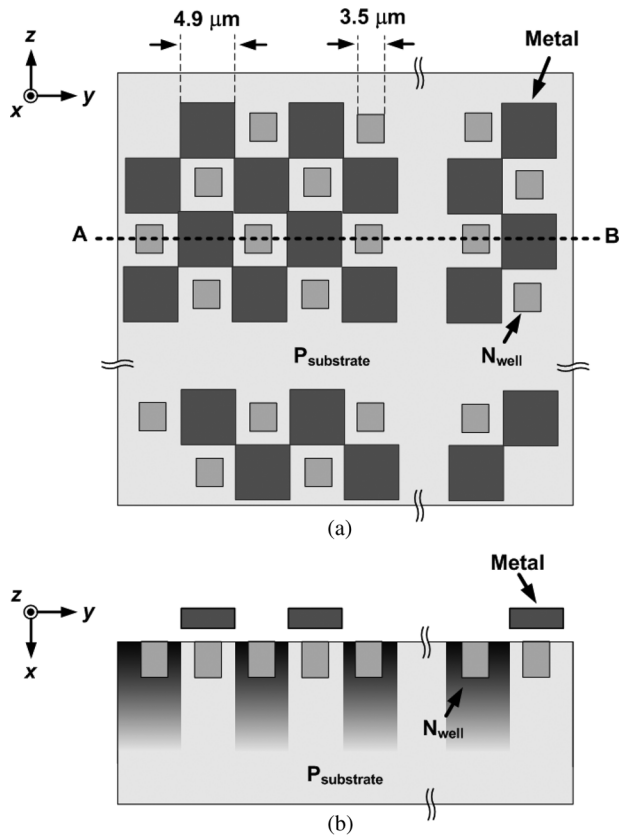


Fig. 5. (a) Top view and (b) cross-sectional view of a meshed SMPD.

On the other hand, to alleviate the reflectivity of optical light incident to the detectors so as to improve its responsivity, passivation layers above the active region of SMPD are removed. By using the impedance-transformation approach [18], the effective impedance (Z) and the reflectance (r) of the photo detector can be derived as

$$Z = \eta_D \frac{\eta_{Si}\cos(kd) + i\eta_D \sin(kd)}{\eta_D \cos(kd) + i\eta_{Si}\sin(kd)} \tag{2}$$

$$r = \left| \left(\frac{Z - \eta_0}{Z + \eta_0} \right)^2 \right| \tag{3}$$

where η_D, η_{Si}, and η_o respectively represent the intrinsic impedance of dielectric layers, silicon substrate, and air; k and d are the wave-number and thickness of the dielectric layers. With 850-nm incident light, theoretical calculations show that

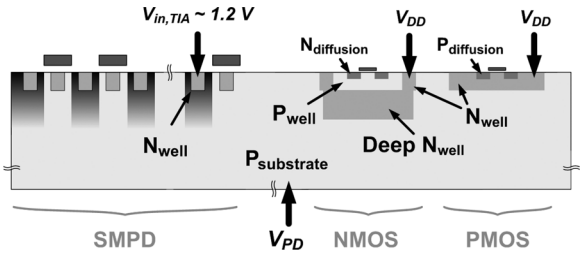


Fig. 6. Integration of the SMPD and transistors in CMOS technology.

the reflectance (r) is around 0.13 and can be reduced to 0.05 by removing the passivation layers.

Besides, the responsivity can also increased by applying a high reverse-biased voltage over the meshed SMPD. It enlarges the depletion region at both the horizontal and vertical junctions, so as to generate more drift carriers. Since the slowly diffusive carriers are generated in the neutral $\mathrm{P_{substrate}}$ region farther away from $\mathrm{N_{well}}$, they can be more equally captured by the light and dark detectors.

However, a high reverse-biased voltage over the SMPD may induce high substrate noise current. To circumvent this issue, all the active circuits are surrounded by voltage islands isolated by deep $\mathrm{N_{well}}$ and $\mathrm{N_{well}}$. Another concern arisen from high reverse-biased voltage is the junction-breakdown issue. As shown in Fig. 6, the cathode of SMPD is connected to the input node of TIA is about 1.2 V. For a PD reverse-biased voltage of 14.2 V, the $\mathrm{P_{substrate}}$ region is biased at -13 V and the maximum reverse-biased voltage happens at the $\mathrm{P_{substrate}}/\mathrm{N_{well}}$ (or deep $\mathrm{N_{well}}$) junction, which is around 14.8 V $(1.8-(-13)$ V). Thus, the applicable PD reverse-biased voltage is limited by the tolerable junction breakdown voltage in CMOS technology.

To investigate the effects of reverse-biased voltage (V_R) on the responsivity and bandwidth of CMOS PD, V_R of 1.2 V and 14.2 V are applied. Their performance is characterized using an optical receiver with chip on board assembly. The in-band gain variation is caused by the series bonding inductor during measurement. The measured frequency responses of the strip and meshed SMPDs are illustrated in Fig. 7. In the strip SMPD, the strips of $\mathrm{P_{substrate}}/\mathrm{N_{well}}$ detectors are all 2.1-μm wide, separated by a 1.4 μm wide $\mathrm{P_{well}}$ region, where the width with minimum design rules is implemented. The light and dark detectors interleave within an octagon of 55 μm $\times$ 55 μm to comply with the diameter of multi-mode optical fiber. On the other hand, the light and dark detectors of the meshed SMPD are composed of 3.5 μm $\times$ 3.5 μm squares with $\mathrm{N_{well}}$ spacing of 1.4 μm. The light and dark junction diodes interleave in both Y and Z directions, as is illustrated in Fig. 5.

To evaluate the PDs' performance, their responsivity-bandwidth product is chosen as a figure of merit. Compared to the conventional strip SMPD, the meshed SMPD has a better responsivity-bandwidth product which can be improved by 2.6X and 2.0X under a reverse-biased voltage of 1.2 V and 14.2 V respectively. For the meshed SMPD, its responsivity is 20 mA/W in the low-voltage mode, and is boosted to 29 mA/W in the high-voltage mode. It demonstrates that the responsivity can be improved by 1.5X by increasing V_R.

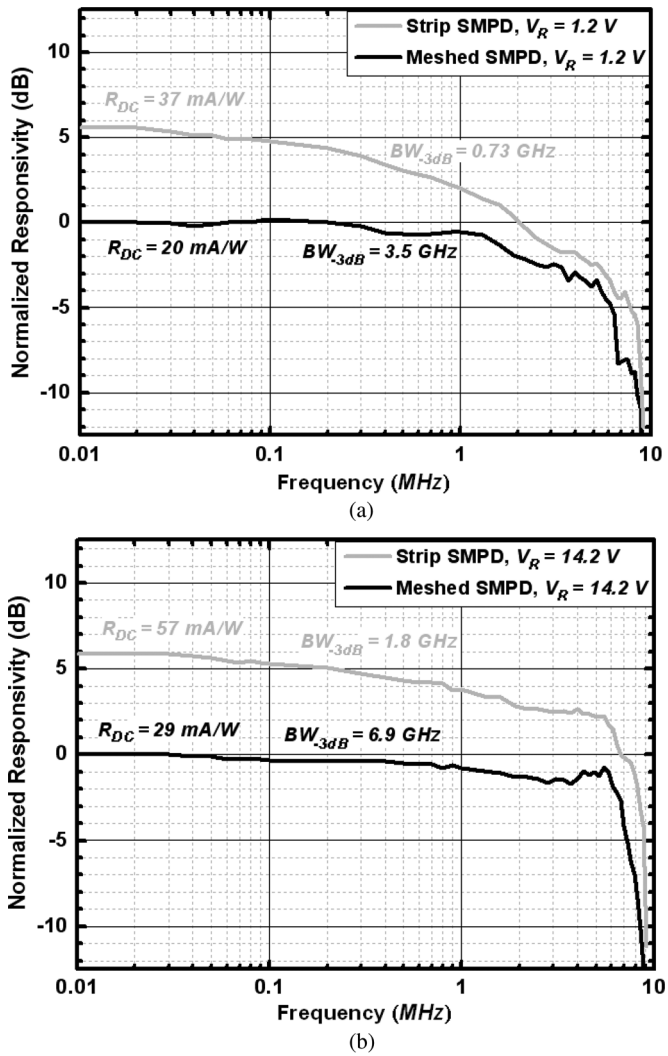


Fig. 7. Measured frequency responses of strip and meshed SMPD under the reverse-biased voltage of (a) 1.2 V and (b) 14.2 V respectively.

Table I summaries the performance of SMPDs and a commercial PD (TPD-8D12-052). For CMOS PDs, the strip SMPD has a larger responsivity though, its -3-dB bandwidth is much lower. On the contrary, the meshed SMPD under a reverse-biased voltage of 14.2 V has $f_{-3\mathrm{dB}}$ of 6.9 GHz, which is suitable for 10-Gb/s operation without an equalizer. Besides, the intrinsic PD capacitance is compatible to that of the commercial PD.

III. Receiver Circuits Design

The architecture of the 10-Gb/s optical receiver is shown in Fig. 8, which integrates an on-chip meshed SMPD, a fully-differential TIA, followed by an input offset compensator (A_{OC}), two stages of voltage gain cells (A_{GC}), and a current-mode output buffer (A_{BUF}). The TIA converts tiny photo current generated from the meshed SMPD to a voltage signal of several millivolts, whose output voltage is further coupled to the post-limiting amplifier to enlarge the signal to a digital level of more than 400 mV. Since the SMPD's responsivity is only 29 mA/W, no automatic gain control circuit is needed. For a

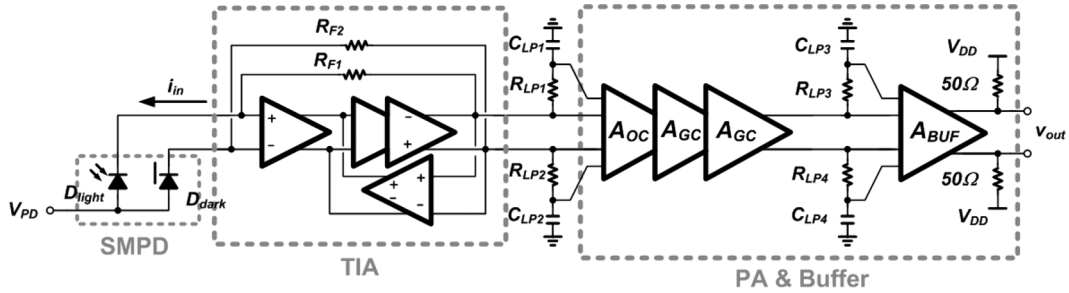


Fig. 8. Proposed CMOS OEIC with the meshed SMPD.

TABLE I
COMPARISON OF SMPDS AND COMMERCIAL PD FOR $\lambda = 850$ nm

Diode Type	Tech.	Responsivity (mA/W)	f_{-3dB} (GHz)	C_{PD} (1) (fF)	V_R (V)
Strip SMPD	0.18-μm CMOS	37	0.73	368	1.2
Strip SMPD	0.18-μm CMOS	57	1.8	213	14.2
Meshed SMPD	0.18-μm CMOS	20	3.5	354	1.2
Meshed SMPD	0.18-μm CMOS	29	6.9	206	14.2
TPD-8D12-052 (2)	GaAs	650	9	220	1.5

(1): CMOS SMPDs' C_{PD} are simulated by HSPICE.
(2): PIN PD, 10-Gb/s photo diode from True-Light Corp.

short-distance interconnect application, the targeted input sensitivity is -6 dBm, and the corresponding input-referred noise current should be less than 1 μA_{rms} for bit-error rate (BER) of less than 10^{-12}. To alleviate the noise contributed from the post amplifier, the TIA is designed to provide as high conversion gain as possible, which is 66 dBΩ in this design. On the other hand, the -3-dB bandwidth of the TIA is designed to be around 7.0 GHz as a compromise between input-referred noise and ISI [19]. Also, the post amplifier provides conversion gain of 22 dB and -3-dB bandwidth of 10 GHz.

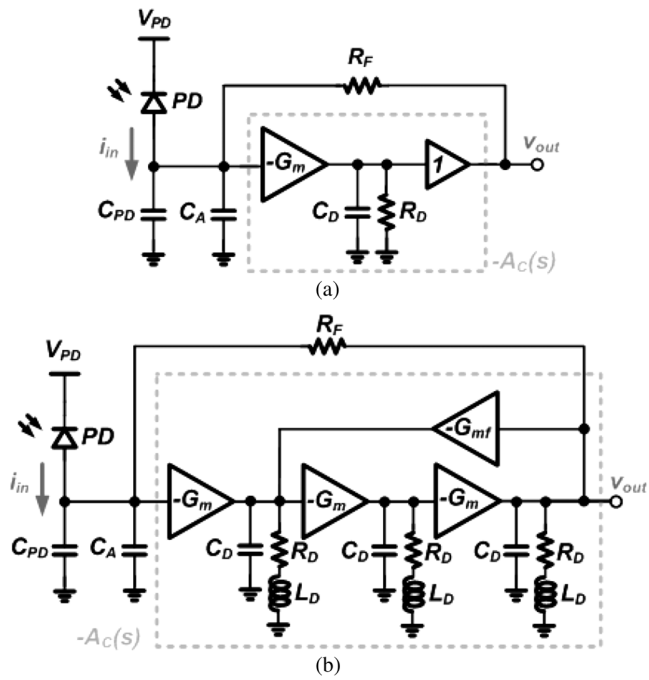


Fig. 9. (a) Shunt-shunt feedback TIA and (b) proposed nested-feedback TIA.

A. Trans-Impedance Amplifier

Typically, a high-sensitivity TIA is based on a common-source amplifier with shunt-shunt feedback. As shown in Fig. 9(a), C_A and C_D denote input and output capacitances of the core amplifier $A_C(s)$, $C_{\rm PD}$ is the PD's parasitic capacitance. Given that $R_F \gg R_D$ and $C_{\rm IN} = C_{\rm PD} + C_A$, the TIA gain (T_z) can be derived as

$$T_Z(s) \approx \frac{R_F}{\frac{R_F C_{\rm IN} C_D}{g_m} s^2 + \frac{R_F C_{\rm IN} + R_D C_D}{g_m R_D} s + 1} \tag{4}$$

The corresponding natural frequency $(\omega_{\rm n})$ and damping factor (δ) can be shown as

$$\omega_n = \sqrt{\frac{g_m}{R_F C_{\rm IN} C_D}} \tag{5}$$

$$\varsigma = \frac{1}{2} \frac{R_F C_{\rm IN} + R_D C_D}{\sqrt{g_m R_D^2 R_F C_{\rm IN} C_D}} \tag{6}$$

For a maximally-flat gain response $(\delta = 0.707)$, the -3-dB bandwidth $(\omega_{-3\rm dB})$ of the TIA can be derived as

$$\omega_{-3\rm dB} = \frac{\sqrt{2} g_m R_D}{R_F C_{\rm IN}} \tag{7}$$

and the dominant pole frequency, $\omega_p = (R_D C_D)^{-1}$, of the core amplifier should be at least $\sqrt{2}\omega_{-3\rm dB}$.

On the other hand, the input-referred noise spectral density $(\overline{I^2_{\rm in,TIA}})$ can be derived as [19]

$$\overline{I^2_{\rm in,TIA}} = \frac{4kT}{R_F} + \frac{1}{R_F^2}\left(\frac{4kT}{g_m} + \frac{4kT}{g_m^2 R_D}\right) \tag{8}$$

According to (8), a low-noise TIA demands a high open-loop gain core amplifier $(g_m R_D)$ and the closed-loop gain (R_F) should be as high as possible. To achieve the targeted bandwidth $(\omega_{-3\rm dB})$, the voltage gain of core amplifier should be increased as well. Both lead to a narrower dominant pole frequency (ω_p), which imposes severe trade-off between high sensitivity, high gain, and wide bandwidth TIA design.

In this design, the $C_{\rm PD}$ and C_A are about 220 fF and 45 fF respectively, a 10-Gb/s, 66-dBΩ TIA demands a core amplifier with -3-dB bandwidth of more than 10 GHz and voltage gain of more than 24 dB. The corresponding gain bandwidth product is about 160 GHz, which is very challenging to be implemented in 0.18-μm CMOS technology with device f_T of only 50 GHz [5].

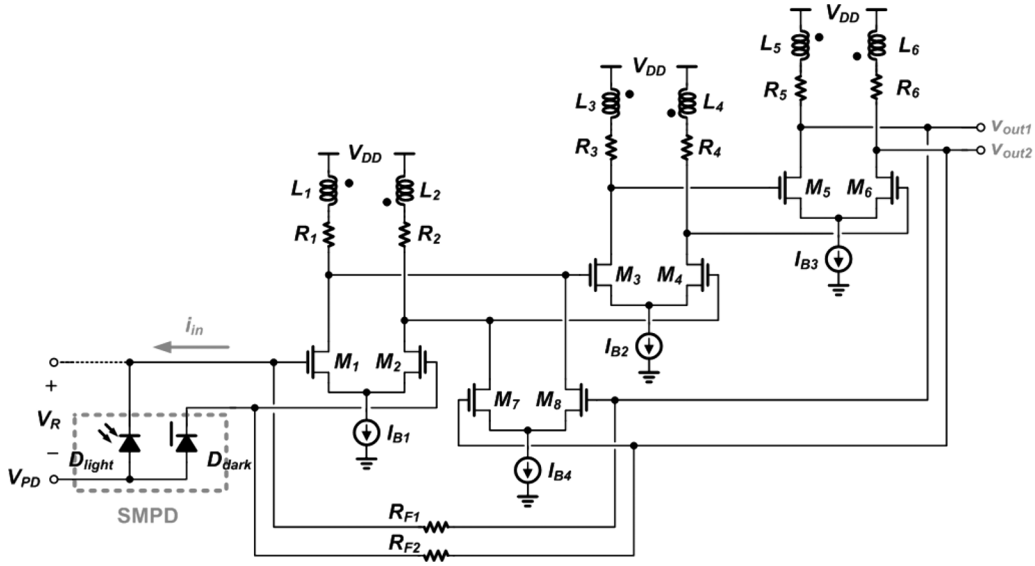


Fig. 10. Circuit schematic of proposed TIA.

To overcome the bottleneck, this paper proposes a TIA incorporating both active and passive nested feedback with transformer shunt peaking. Fig. 9(b) illustrates the circuit architecture. The inner loop is a voltage amplifier composing of another trans-conductance gain stage $(G_{\rm m})$ followed by a trans-impedance amplifier with active feedback (G_{mf}). The outer loop comprising the passive feedback resistor (R_F) performs the current to voltage conversion.

Fig. 10 shows the detailed circuit schematic of the nested-feedback TIA. The photo currents generated from the light and dark detectors are applied to the differential input of the TIA to perform current subtraction. Let g_m denote the trans-conductance of M_1 to M_6, g_{mf} be the trans-conductance of M_7 and M_8, R_D be the resistance of R_1 to R_6, L_D be the inductance of L_1 to L_6, and C_D be the parasitic capacitance at the drain node of M_1 to M_6, the transfer function of the proposed TIA's core amplifier can be derived as

$$A_C(s) = \frac{g_m}{g_{mf}} \left(1 + \frac{1}{g_{mf} g_m^2 Z_D^3(s)}\right)^{-1} \tag{9}$$

where

$$Z_D(s) = \frac{R_D + sL_D}{1 + sC_D R_D + s^2 C_D L_D} \tag{10}$$

and the transfer function of the proposed TIA can be derived as

$$T_Z(s) = \frac{v_{\rm out}(s)}{i_{\rm in}(s)} = \frac{R_F}{1 + (1 + sC_{\rm IN}R_F)A_C^{-1}(s)} \tag{11}$$

By choosing $g_m \gg g_{mf}$, $(A_c)^{-1}$ approaches zero and the TIA conversion gain (T_z) can be approximated as

$$T_Z = \frac{R_F}{1 + A_C^{-1}} \approx R_F \tag{12}$$

According to (10), shunt-peaking technique extends the bandwidth of core amplifier by introducing a zero and an additional pole at higher frequency. For a maximally-flat response, L_D can be chosen as

$$L_D = \frac{R_D^2 C_D}{2.41} \tag{13}$$

and the corresponding bandwidth can be improved by 1.72X compared to that without inductive peaking [20]. Under this criterion, $Z_D(s)$ can be simplified as

$$Z_D(s) \approx \frac{R_D}{1 + 0.58 s C_D R_D} \tag{14}$$

As the -3-dB bandwidth of the $Z_D^3(s)$ is reduced by 0.51X compared to $Z_D(s)$ [5], to simplify the derivation, $Z_D^3(s)$ can be approximated as

$$Z_D^3(s) \approx \frac{R_D^3}{1 + 1.14 s C_D R_D} \tag{15}$$

By substituting (15) into (9) and (11), a high-order TIA frequency response can be approximated as a two pole model without losing much design insight.

$$T_Z(s) = \frac{R_F}{1 + \frac{2}{g_m^3 R_D^3} + \left(\frac{2C_{\rm IN}R_F}{g_m^3 R_D^3} + \frac{1.14 C_D R_D}{g_m^3 R_D^3}\right) s + \frac{1.14 C_D R_D C_{\rm IN} R_F}{g_m^3 R_D^3} s^2} \tag{16}$$

The corresponding natural frequency (ω_n) and damping factor (δ) can be derived as

$$\omega_n \approx g_m R_D \sqrt{\frac{g_m}{1.14 C_D C_{\rm IN} R_F}} \tag{17}$$

$$\varsigma = \frac{C_{\rm IN} R_F + 0.57 C_D R_D}{\sqrt{\left(g_m^3 R_D^3 + 2\right)\left(1.14 C_{\rm IN} R_F C_D R_D\right)}} \tag{18}$$

Compare (17) to (5), ω_n can be improved by a factor of $g_m R_D$, which is about 3.5 (V/V) in this design.

For adequate voltage swing, the output common-mode voltage of the differential pairs in Fig. 10 is about 0.5 V.

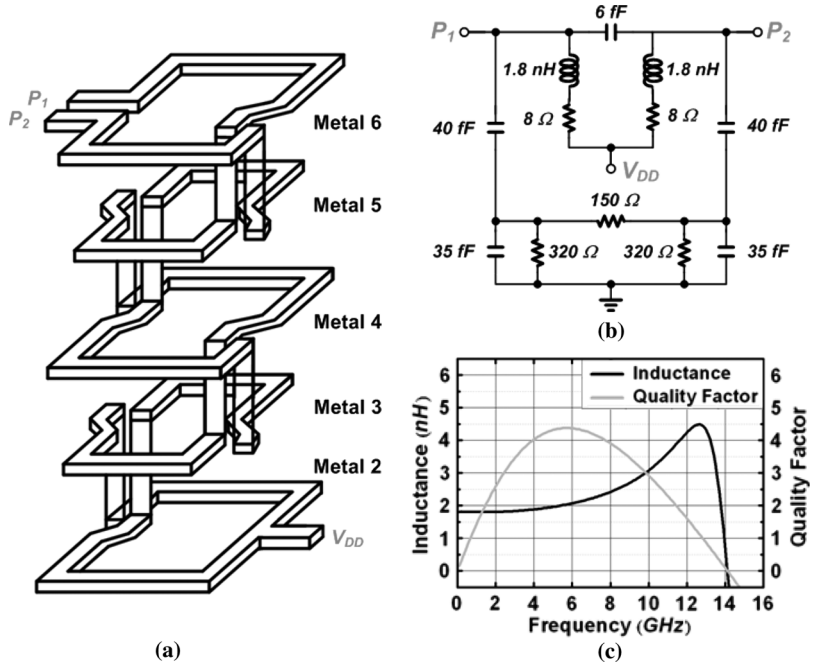


Fig. 11. 3-D symmetric transformer (a) architecture, (b) lumped model, and (c) EM simulation results.

TABLE II
DESIGN VALUES FOR THE NESTED-FEEDBACK TIA

Parameter	Value
$W/L_{1\text{-}6}$	48 μm /0.18 μm
$W/L_{7\text{-}8}$	1.4 μm /0.18 μm
$I_{B1\text{-}3}$	7 mA
I_{B4}	0.2 mA
$R_{1\text{-}6}$	145 Ω
$R_{F1\text{-}2}$	2100 Ω
$L_{1\text{-}6}$	1.8 nH

Table II summarizes the device parameters. In order to minimize chip area occupied by the peaking inductors, all the differential inductors ($L_1 - L_2$, $L_3 - L_4$, and $L_5 - L_6$) are realized as 3-D transformer [7]. Fig. 11 shows the architecture, lumped model, and the parameters of the 3-D transformer by EM simulation. The inductance in each branch is 1.8 nH and the self-resonant frequency is 14.1 GHz. Although its quality factor is relatively low by using lower metal layer, this is not an issue for shunt-peaking application with a maximally-flat gain response.

Fig. 12 illustrates the performance comparisons between the proposed TIA and a conventional TIA. By applying the nested-feedback technique, a core amplifier with 25.5 dB voltage gain and 11 GHz −3-dB bandwidth can be achieved. Thus, the proposed TIA bandwidth can be extended to 7.1 GHz with a high gain of 66 dBΩ. On the contrary, a conventional TIA faces severely direct trade-off between gain and bandwidth performance. Under the same gain requirement, the achievable −3-dB is less than 2 GHz.

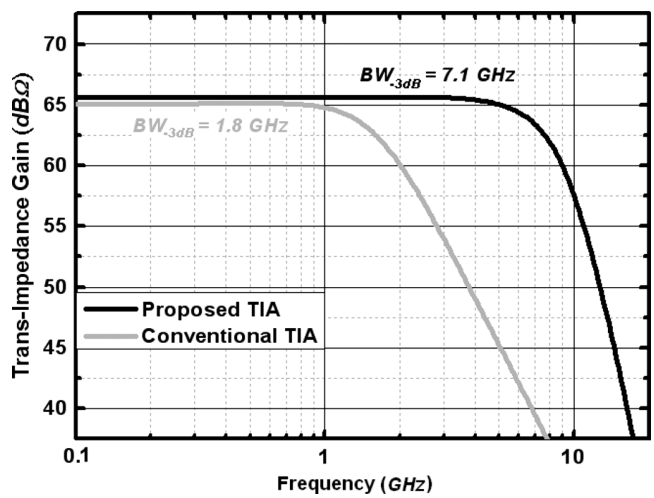


Fig. 12. Simulated magnitude response of proposed and conventional TIA.

Another concern related to multi-path feedback is the gain peaking issue. The phenomena are investigated by changing R_F and the corresponding frequency responses are summarized in Fig. 13. It reveals that a smaller R_F results in a wider bandwidth but a higher gain peaking, which also corresponds with (17) and (18). As a consequence, a feedback resistor R_F of 2.1 kΩ is chosen to maximize its gain and bandwidth performance without severe gain peaking.

The input-referred noise current $\overline{I_{n,TIA}^2}$ of the TIA can be derived as

$$\overline{I_{\text{in,TIA}}^2} = \frac{8kT}{R_F} + \frac{1}{R_F^2}\left[\overline{V_{n,SC}^2} + \frac{1}{g_m^2}\left(g_{mf}^2\overline{V_{n,SC}^2} + g_{mf}^2\frac{\overline{V_{n,SC}^2}}{g_m^2 R_D^2}\right)\right] \quad (19)$$

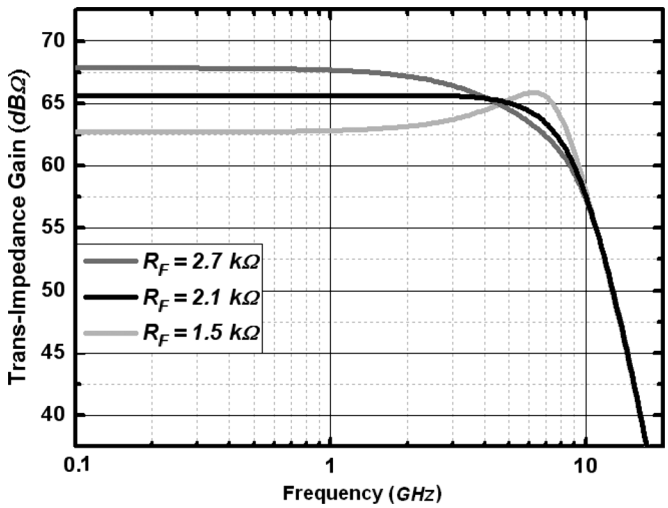


Fig. 13. Simulated magnitude response of TIA with different R_F.

where $\overline{V_{n,SC}^2}$ represents the input-referred noise voltage of a single-stage source coupled pair, and can be expressed as

$$\overline{V_{n,SC}^2} = 2\left(\frac{4kT}{g_m} + \frac{4kT}{g_m^2 R_D}\right) \tag{20}$$

The input-referred noise current of the TIA is about 0.64 $\mu\mathrm{A_{rms}}$ by simulation.

B. Post-Limiting Amplifier

The post amplifier is composed of three stage voltage amplifiers, comprising of a subtractor followed by two voltage gain cells. Fig. 14(a) shows the circuit schematic of gain cell, which is based on Cherry-Hooper architecture with inductive peaking. By shunt-shunt feedback, all the nodes in the circuit become low impedance for wide bandwidth operations. It has been shown in [5] that the active feedback can increase the GBW of the gain cell beyond the technology f_T. Fig. 14(b) shows the input stage of the post amplifier, which functions as an input buffer as well as an offset subtractor. The input offset voltage (V_{in1dc} and V_{in2dc}), which is derived from TIA output and a low pass filter, is converted to a compensation current to be subtracted from the input signal (V_{in1} and V_{in2}) by the source-coupled pair $(M_7 - M_8)$. Besides, to facilitate the characterization of the optical receiver without significantly introducing capacitive load to the preceding stage, an f_T doubler output buffer is adopted [19].

The number of gain stage in post amplifier is chosen as a compromise between gain and bandwidth requirements as well. Assuming each gain cell is identical and approximated by a two-pole amplifier, its conversion gain, $A(s)$, can be described as

$$A(s) = \frac{A_S \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{21}$$

where A_s denotes the small-signal DC gain, ζ is the corresponding damping factor, and ω_n is the natural frequency. Let the targeted -3-dB bandwidth of an N-stage cascaded amplifier

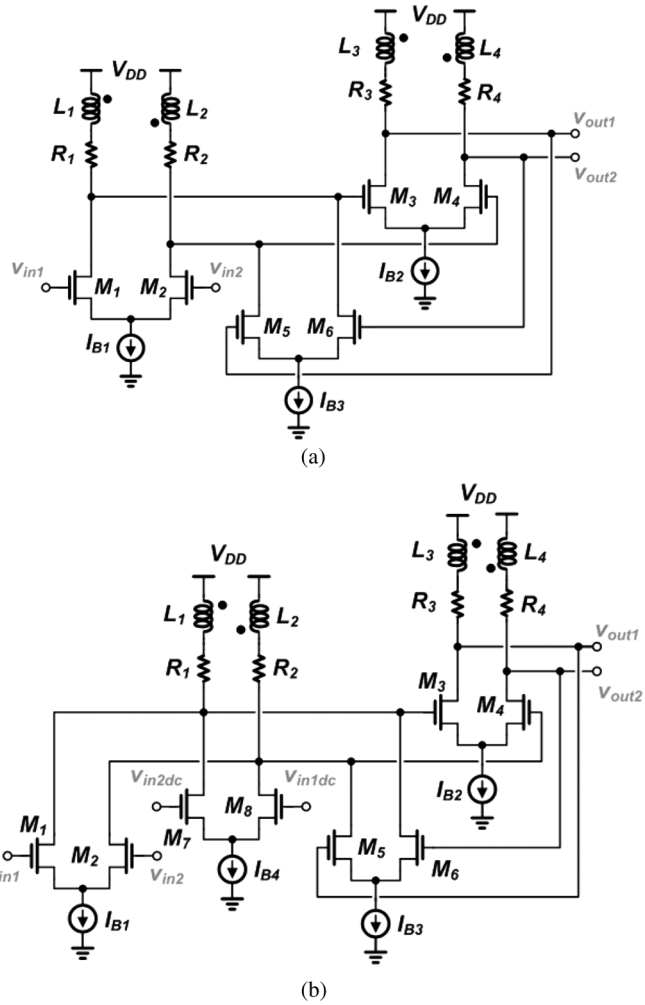


Fig. 14. (a) Gain cell and (b) subtractor of the post amplifier.

be ω_c, and the total conversion gain be A_c. For a flat band response, the required gain-bandwidth product (GBW) per stage can be expressed as [4]

$$\mathrm{GBW} = \omega_c \times \left(\frac{1}{2^{1/N} - 1}\right)^{1/4} \times A_c^{1/N} \tag{22}$$

Assuming the conversion gain of subtractor is less than that of the voltage gain cell by -6 dB, and the insertion loss of the output buffer is about -5 dB, the conversion gain of each gain cell is designed to be 11 dB, so as to enlarge TIA output signal to a logic level of more than 400 mV. The bandwidth of each gain cell is 14 GHz to minimize ISI induced data jitter.

The input-referred noise current of the optical receiver can be expressed as

$$\overline{I_{\mathrm{in,RX}}^2} = \frac{8kT}{R_F} + \frac{1}{R_F^2}\left[\overline{V_{n,Ac}^2}\right] + \frac{1}{R_F^2}\left[\overline{V_{n,PA}^2}\right] \tag{23}$$

where $\overline{V_{n,Ac}^2}$ and $\overline{V_{n,PA}^2}$ respectively represent the input-referred noise voltage of the TIA's core amplifier and the post amplifier. As the input sensitivity of the CMOS OEIC is mainly limited by the responsivity of the photo detector, it can be seen from (23) that R_F should be chosen as large as possible.

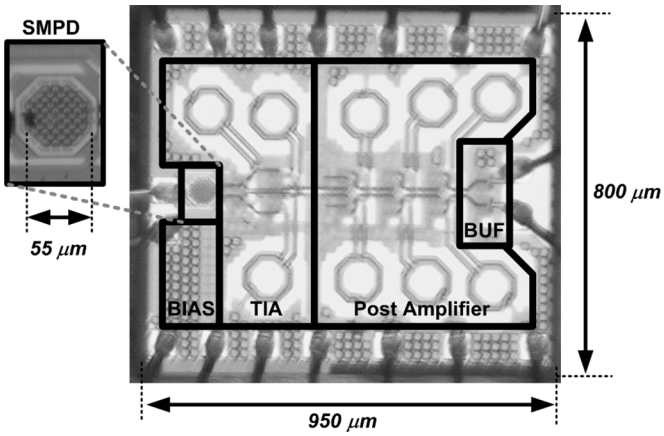


Fig. 15. Die photo of proposed OEIC with meshed SMPD.

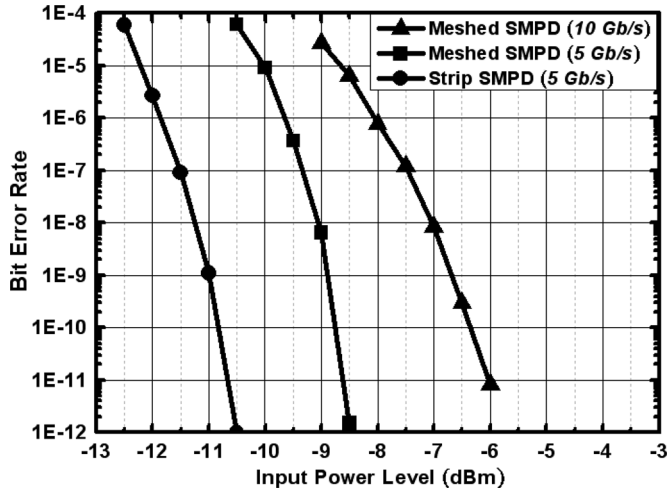


Fig. 16. BER performance of OEIC with the SMPDs under reverse-biased 14.2 V.

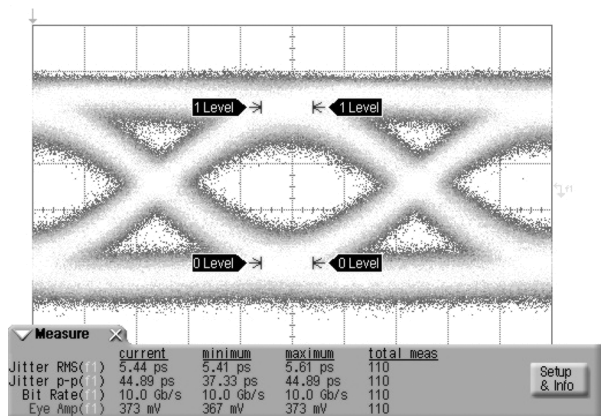


Fig. 17. Measured 10-Gb/s eye diagram of the OEIC with a meshed SMPD under −6-dBm input optical power level.

However, the overall bandwidth becomes severely limited and it burns much more power to sustain the bandwidth. In this design, about 50% input-referred noise current contributed from the feedback resistor R_F, 30% from the TIA's core amplifier, and 20% comes from the post amplifier.

IV. Experimental Results

The receiver IC is mounted on a printed-circuit board (PCB) for measurement. The pulse pattern generator (Anritsu MU181020A) sends a PRBS 2^7-1 test pattern to modulate an 850-nm VCSEL (New Focus) as a light source. The eye diagrams are captured by Agilent 86100C and the BER performance are characterized using Anritsu MU181040A. To measure the input power sensitivity accurately, an optical power attenuator (OZ Optics) is adopted, and the extinction ratio is 7.4 dB.

The chip micrograph is shown in Fig. 15. Fabricated in a generic 0.18-μm CMOS technology, this chip size is 0.95 mm by 0.8 mm. The meshed SMPD is laid out in an octagon, and the area is 55×55 μm^2 to comply with the diameter of the multimode fiber. The SMPDs are powered with a variable supply voltage, $V_{\rm PD}$, (from 0 V to −13 V), while the receiver circuits are operated under the 1.8-V supply. The total power dissipation is 145 mW, among which 27 mW is consumed by the output buffer. By cascading TIA and post-limiting amplifier on a single chip, the optical receiver provides a conversion gain of 88 dBΩ. With an 18-μA$_{\rm pp}$ input current, the optical receiver is capable of delivering 450-mV$_{\rm pp}$ differential voltage swings to 50-Ω output loads directly.

Fig. 16 shows the bit error rate performance of CMOS OEIC with strip and meshed SMPD respectively. Under a reverse-biased voltage of 14.2 V, the input sensitivity of OEIC with meshed SMPD is −6 dBm for the BER of less than 10^{-11}. On the other hand, as the strip SMPD has a better responsivity compared to the meshed SMPD, for a 5-Gb/s operation, the input sensitivity of the OEIC with strip and meshed SMPD are −10.5 and −8.5 dBm respectively. Fig. 17 shows the measured 10-Gb/s eye diagram at the sensitivity level. With −6 dBm incident optical power, the measured data jitter is 5.44 ps$_{\rm rms}$ (44.89 ps$_{\rm pp}$). The data eye becomes fussy with strip SMPD. By a single pole approximation, the −3-dB bandwidth can be estimated based on the rise time $t_{\rm rise}$, (from 10% to 90%), which can be described as

$$f_{H-3\rm dB} = \frac{0.35}{t_{\rm rise}} \tag{24}$$

Based on eye diagram in Fig. 17, it suggests that the overall bandwidth is around 5.8 GHz, which is limited by the rise time of light source (VCSEL), SMPD, and receiver all together.

In order to fully characterize the performance of the receiver circuit itself, an external GaAs PIN PD (TPD-8D12-052) with responsivity of 0.65 A/W for 850-nm optical wavelength is also applied to identical OEIC without on-chip CMOS detector. The chip micrograph is shown in Fig. 18. Fig. 19 summarizes the BER performance. With the external PD, the input sensitivity level of the optical receiver at 10 Gb/s is −18.6 dBm and −19 dBm for BER of less than 10^{-12} and 10^{-10} respectively. Fig. 20 shows the measured eye diagrams at 10 Gb/s with incident optical power at sensitivity (−18.6 dBm) and overloaded (−5 dBm) power level, and the corresponding data jitter are 6.11 ps$_{\rm rms}$ (46.22 ps$_{\rm pp}$) and 3.76 ps$_{\rm rms}$ (21.66 ps$_{\rm pp}$)

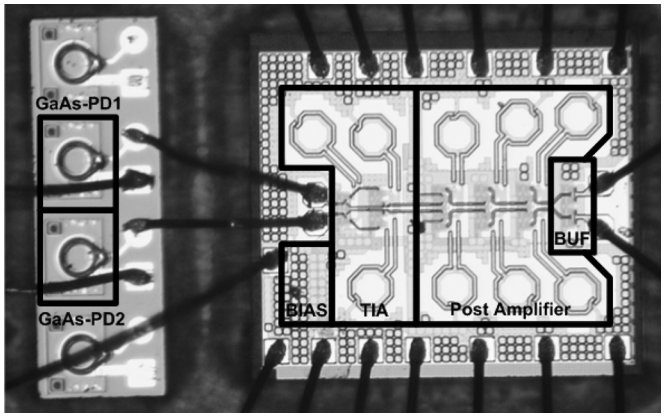


Fig. 18. Dies of commercial PDs and proposed optical receiver.

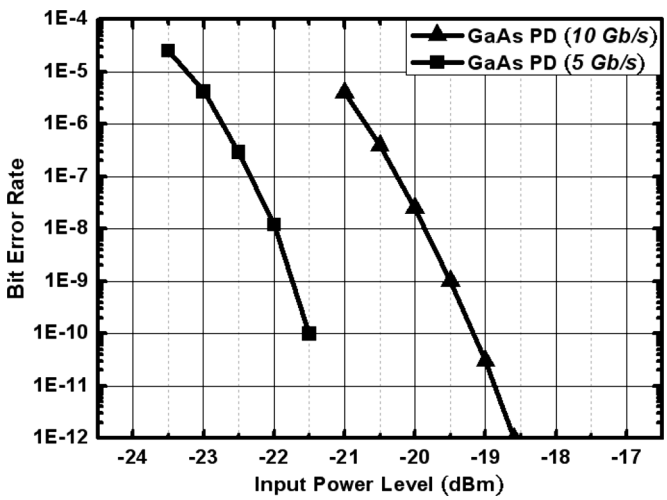


Fig. 19. BER performance of this optical receiver with a commercial PD.

respectively. Thus, the minimum input current $(I_{\mathrm{in,mim}})$ of the optical receiver at BER of less than 10^{-12} can be calculated as

$$I_{\mathrm{in,mim}} = R \times P_{\mathrm{sen}} = 0.65(\mathrm{A/W}) \times 13.8(\mu\mathrm{W}) \approx 9(\mu\mathrm{A}) \tag{25}$$

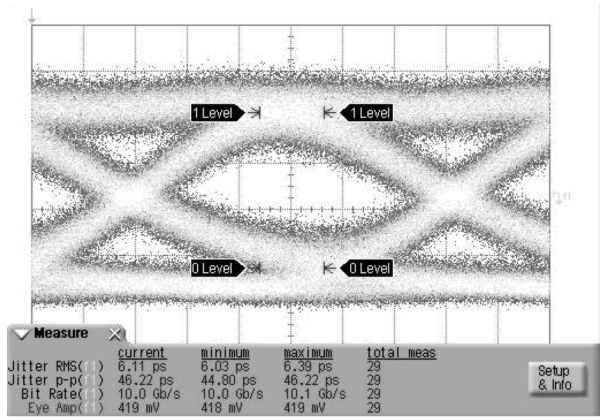
where the PD's responsivity (R) is 0.65 A/W, and the input optical power (P_{sen}) is -18.6 dBm.

Fig. 21 shows the performance benchmark of the prior art at 10-Gb/s operations [7], [10], [21]–[24]. It can be seen that the TIAs with higher conversion gain generally have lower input-referred noise current and thus better input sensitivity. The input-referred noise current $(I_{n,in})$ is calculated by

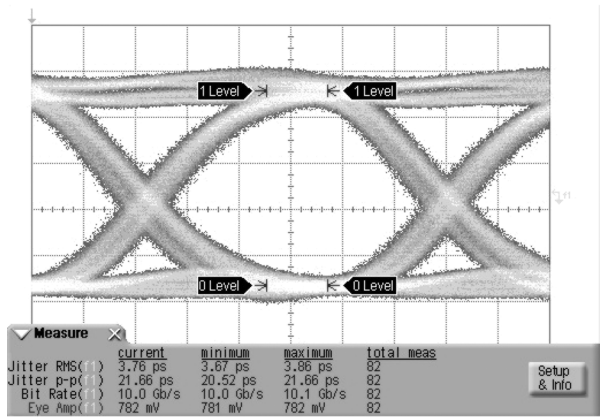
$$I_{n,in} = \frac{I_{\mathrm{in,min}}}{Q} \tag{26}$$

where $I_{\mathrm{in,min}}$ is the minimum input current for a designated BER, and Q is the quality factor which reflects its BER performance [19] ($Q \sim 6$ for $BER = 10^{-9}$ and $Q \sim 7.04$ for $\mathrm{BER} = 10^{-12}$). Our proposed TIA has a conversion gain of 66 dBΩ and input-referred noise of 1.27 μA, which manifests superior performance compared to the prior art.

Table III summarizes the integrated OEIC performance comparisons. For fully integrated CMOS OEICs, this work manifests the highest conversion gain and operating speed, and is the first one capable of operating up to 10 Gb/s in generic CMOS technology without an adopting sophisticated equalizer. That of [10] has a better sensitivity and is also capable of operating up to 10 Gb/s. However, it is fabricated in BiCMOS process and consumes more than twice DC power.



(a)



(b)

Fig. 20. Measured eye diagram with input optical power of (a) -18.6 dBm and (b) -5 dBm.

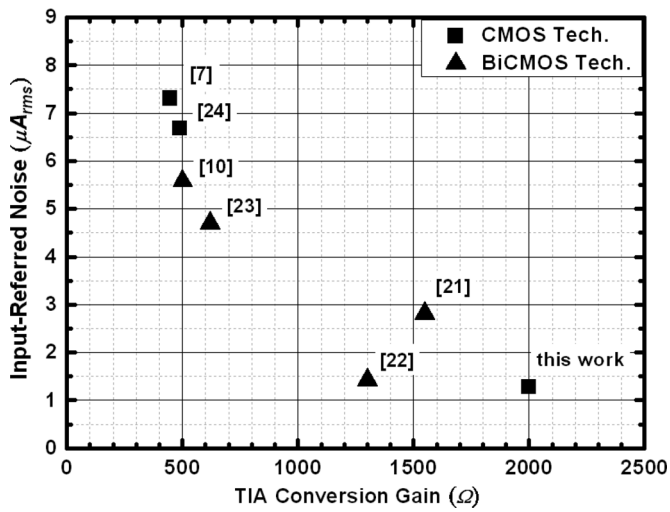


Fig. 21. Performance benchmark of 10-Gb/s OEIC and receiver amplifier in terms of gain and input-referred noise. ([10] and this work are OEICs.)

TABLE III
OEIC PERFORMANCE COMPARISON FOR $\lambda = 850$ nm

Spec.	[11]	[17]	[16]	[10]	This work
PD Type	Lateral PIN (1)	PN	Strip SMPD	PIN(3)	Meshed SMPD(4)
PD Capacitance	1600 fF	280 fF	1000 fF	60 fF	206 fF
PD Bandwidth	1.9 GHz	< 0.01 GHz	0.5 GHz	2.2 GHz	6.9 GHz
PD Responsivity	73 mA/W	560 mA/W	5 mA/W	260 mA/W	29 mA/W
Architecture	TIA + LA	TIA + EQ(2)	TIA + EQ + LA	TIA + EQ + LA	TIA + LA
Data Rate	2.5 Gbps	3 Gbps	4.5 Gbps	11 Gbps	10 Gbps
PRBS Type	2^{31}-1	2^{31}-1	2^{7}-1	2^{31}-1	2^{7}-1
TIA Gain	1 kΩ	0.85 kΩ	4.5 kΩ	0.5 kΩ	2 kΩ
Sensitivity at BER	-4.5 dBm at 10^{-9}	-19 dBm at 10^{-11}	-3.4 dBm at 10^{-12}	-8.9 dBm at 10^{-9}	-6 dBm at 10^{-9}
Power	138 mW	34 mW	74 mW	310 mW	145 mW
Technology	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS	0.5-μm BiCMOS	0.18-μm CMOS

(1): 6-V supply power is needed to bias a lateral PIN.
(2): single-ended.
(3): 17-V supply power is needed to bias a PIN.
(4): −13-V supply power is needed to bias a meshed SMPD.

V. CONCLUSION

This paper presents monolithic CMOS optical receiver, integrating a photo detector, a trans-impedance amplifier, and a post-limiting amplifier on a single chip. A novel meshed SMPD and shunt-peaking techniques are adopted for multi-Gb/s operations. For 5-Gb/s and 10-Gb/s operations, the input sensitivity of the CMOS OEIC is −8.5 dBm and −6 dBm respectively. With external GaAs photo detector, the measured input sensitivity of the optical receiver is −19 dBm at 10 Gb/s. The developed techniques show strong potential to be applied in mutli-lanes intra-chip, inter-chip, and backplane interconnects.

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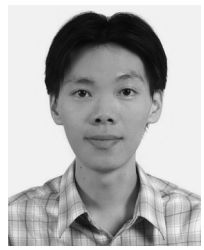

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