Geometric Variability of Nanoscale Interconnects and Its Impact on the Time-Dependent Breakdown of Cu/Low-k Dielectrics

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***Abstract*—Line edge roughness (LER) and via-line misalignment strongly impact the time-dependent breakdown of the low-k dielectrics used in nanometer IC technologies. In this paper, we investigate, theoretically and experimentally, the impact of the variability of geometry on breakdown. By considering the statistical distribution of thickness between adjacent conductors exhibiting LER, we show that the breakdown location is a function of voltage and occurs at the minimum dielectric thickness at high voltage, but moves to the median thickness at the low voltages. Using these concepts, we show that LER modifies the functional form of failure distributions, and leads to a systematic change in the Weibull β with voltage. Accurate reliability analysis requires new reliability extrapolation methodologies to account for these effects. We show that the minimum dielectric thickness present on a test structure or on a circuit is readily determined from routine measurements of dielectric thickness between metal lines. We verify theoretical predictions using measurements of failure distributions of both via and line test structures. Finally, we have shown that LER can significantly modify the apparent field dependence of the failure time, leading to ambiguity in the interpretation of the experimentally determined field dependence.**

***Index Terms*—Cu/low-k interconnect reliability, line edge roughness (LER), porosity, time-dependent dielectric breakdown (TDDB).**

I. Introduction

Low-k materials are widely used for advanced Cu/Low-k interconnects to meet the circuit requirements of lower *RC* delay and power consumption required by technology scaling. However, reliability concerns due to potential early breakdown of these dielectrics have become more serious as k is decreased because of weaker intrinsic material breakdown strength, and smaller interconnect geometries. Fundamental failure mechanisms, lifetime models, and the impact of conductor geometry variability on reliability have been discussed in recent studies [1]–[5]. In particular, there is currently an active debate over which model should be used for TDDB lifetime estimation of low-k dielectrics [6]–[11].

It has become clear, recently, that local conductor geometry variations, or line edge roughness (LER), can have a significant impact on low-k reliability for advanced nanoscale interconnects. This variability leads to local changes in dielectric thickness between the conductor lines and produces enhancements in the local electric field. Similarly, when vias are defined between metal levels, misalignment between vias and the underlying metal level can occur, which reduce the dielectric thickness between the via and the upper-level metal line. Stucchi *et al.* calculated the electric field enhancement associated with vias could be about a factor of two above that expected in the absence of vias [2]. Chen indicated that the Weibull slope (β) of the breakdown failure distribution becomes shallower with decreasing line-to-line dielectric thickness due to LER [1]. Both shallower β and locally high electric fields make reliability projections more pessimistic. On the other hand, Haase *et al.* used failure distribution simulations incorporating dielectric thickness variability to show that the deleterious effects of the thickness variation are diminished at voltages more typical of IC use [3]. However, there is limited understanding of the impact of variability in dielectric thickness on failure distributions as a function of field, particularly for via configurations where field enhancements are largest. This deficiency in understanding makes accurate reliability characterization difficult, and introduce significant ambiguity into assessments of use condition reliability from the measured failure distributions.

While previous studies have focused on determining the magnitude of field enhancements, and their impact on reliability, we instead focus on the observation that there is always a distribution in dielectric thickness due to LER and via-line overlay. The consequences of this statistical distribution in thickness have not yet been explored. In this paper, we study, in detail, the effects of the thickness distribution upon dielectric reliability. We will show that dielectric thickness variability has profound influence on almost all aspects of reliability characterization and prediction, including the functional form of failure distributions, the apparent field dependence of the failure time, and the methodology that is appropriate to calculate use condition reliability.

This paper begins in the Section II by developing a model of dielectric breakdown that determines the most probable thickness for failure as a function of voltage, in the presence of LER. In Section III, we describe experimental details. Section IV presents experimental data for breakdown failure distributions as a function of voltage and provides comparisons with model

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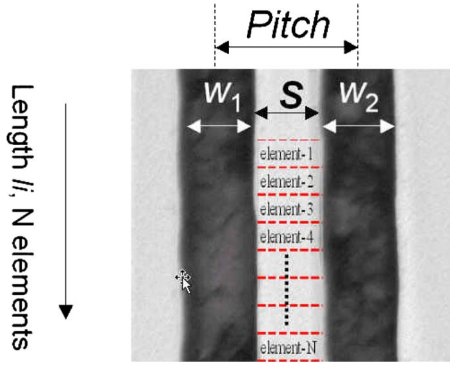


Fig. 1. Example of line edge roughness (LER) of two adjacent Cu conductors.

predictions. In Section V, we discuss the implications of LER for the determination of the field dependence of the failure time.

II. Modeling of Geometric Impact on Cu/Low-k Dielectric Reliability

A. Dielectric Breakdown Statistics

Fig. 1 shows a typical example of the LER associated with two adjacent Cu conductors. To begin, we assume that the dielectric between the conductors can be approximated as a parallel arrangement of N elements, each of length a_0. Percolation theory has been widely used to describe dielectric breakdown statistics in MOS capacitors [16], [17] as well as Cu/porous low-k dielectrics [12], [13]. In percolation theory, the dielectric is divided into a series of small elements of cell size a_0 with failure probability λ. The failure probability of the dielectric can be derived through the assumption of a weak-link process, i.e.,

$$F_{\text{dielectric}} = 1 - \left(1 - \lambda^{\frac{t_{\text{ILD}}}{a_0}}\right)^N \tag{1}$$

where t_{ILD} is dielectric thickness. Here, λ is assumed to follow power law, i.e., $\lambda(t) = (t/t_0)^m$ where m is a constant, which is an approximation that is generally reasonable for times much less than the median time to fail for the cell itself. The use of percolation theory to describe the generation of the breakdown path within the dielectric leads to Weibull failure statistics with distribution parameters given by

$$t_{63\%} = t_0 N(s_0)^{\frac{-1}{\beta}} f(E_{\text{ILD}}) = t_0 N(s_0)^{\frac{-1}{\beta}} f(V/s) \tag{2}$$

$$\beta = \frac{m s_0}{a_0}\left[1 - (1+\alpha)P\right] \tag{3}$$

t_0 is the characteristic failure time of an element; $N(s_0)$ is the number of elements with mean thickness s_0; E_{ILD} is the field in the dielectric; V is the voltage; P is the porosity (or pore density) of the dielectric, s_0 is the mean dielectric thickness, α is a field enhancement factor arising from distortion of the electric field around pores [12]. The function $f(E_{\text{ILD}})$ presents the field dependence of the breakdown process.

The presence of pores (assumed $k = 1$) can be considered to have two effects on breakdown of a dielectric film: 1) pores introduce a local electric field enhancement at the pore and surrounding dielectric, which leads to a current increase so the pore appears to act as a local high-current path; and 2) the pore can be viewed as decreasing the length of the percolation path for breakdown. Both of these effects result in lower TDDB failure time [12]. This local electric field has a stronger impact on dielectric failure time at stress (high-voltage) conditions than in use (low-voltage) conditions. This occurs because the ratio of local maximum field around pores to average field is the same at high-voltage (stress) and low-voltage (use) conditions, but the absolute difference is much higher at stress condition than at use conditions. The field enhancement factor α can be characterized using (2) and experimentally, it has been found that $\alpha \sim 1$ at stress conditions [12]. Theoretically, $\alpha \sim 0$ is expected at use conditions because the local maximum field is close to the average field. Therefore, from (2), β is a function of stress condition, which has been confirmed experimentally [12]. Extrapolation of failure distribution data from accelerated conditions must account for this change β.

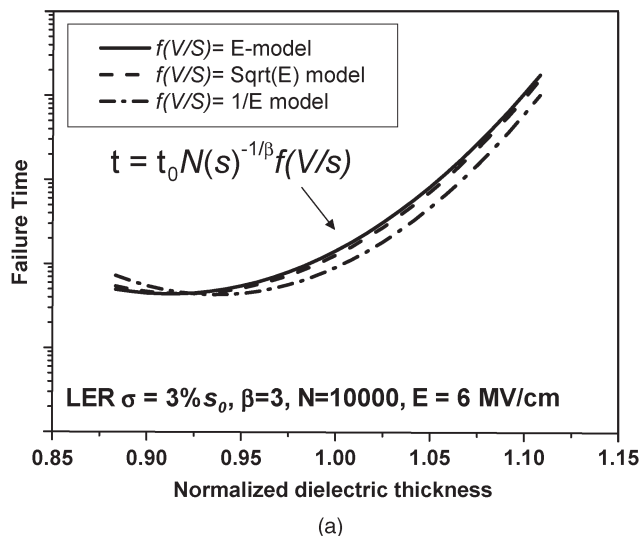
In the presence of LER, for each adjacent cell along the conductor length, the dielectric thickness will differ, which will lead to a variation in the electric field between elements under constant voltage conditions. Equation (2) demonstrates that the location of failure of the dielectric is determined by two factors: 1) the magnitude of the electric field in the dielectric between the conductor units; and 2)the probability of occurrence of the thickness. Failure of the dielectric can be considered as a weak-link problem, with failure occurring where the failure time given by (2) is a minimum. Therefore, the probability of failure of the dielectric is not necessarily highest for the region with highest field, since the probability of the occurrence of the thickness must be considered. In the following, we calculate the most probable thickness for dielectric failure according to (2), where we make the approximation that the electric field is uniform within the unit cell of the dielectric.

B. Modeling of Failure Locations

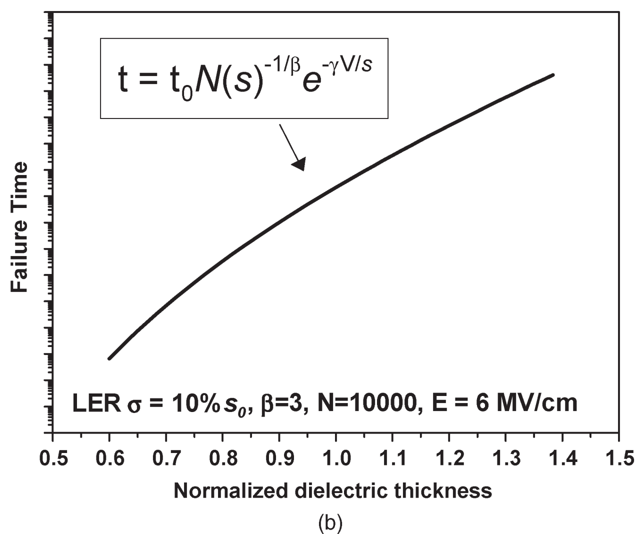
We assume that the thickness distribution can be described by a normal distribution, i.e.,

$$N(s) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{-(S-S_0)^2}{2\sigma^2}}. \tag{4}$$

Fig. 2 shows the results of calculation of the failure time from (2) with dielectric thickness using different field dependence $f(V/s)$ under high-field (accelerated test) conditions with the sample size of 10^4 in conductor elements. In Fig. 2(a) $N(s)$ has $\sigma = 3\% s_0$, while for Fig. 2(b) $\sigma = 10\% s_0$. These two values of σ correspond to typical values anticipated for line structures and via structures, respectively, in nanotechnologies. Via configurations can exhibit larger σ because, in the case of a minimum feature size metal line, which is the worst case practical situation, vias may be larger than the underlying line that they are placed on. Moreover, there is generally a misalignment of vias with the underlying metal layer. These combined effects can lead to a significant reduction of the dielectric thickness between the top surface of vias and lines, and it is this area that is most vulnerable to breakdown [4]. For these calculations, β is linearly scaled with thickness as (3). We start from the assumption of a normal distribution in thickness since this is usually good approximation to the situation that occurs in

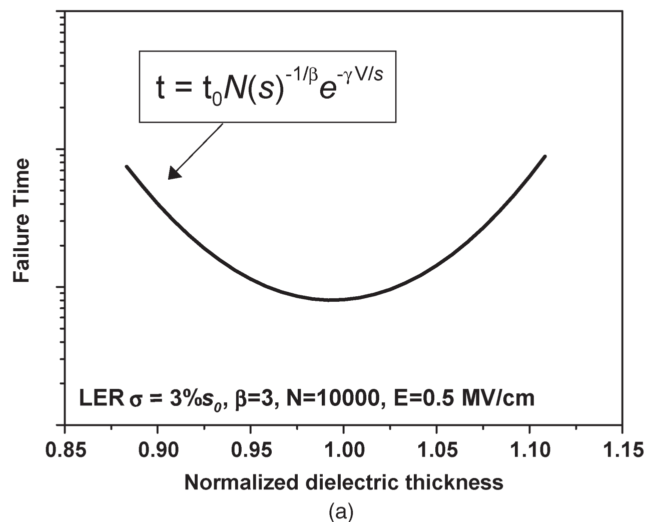


(a)

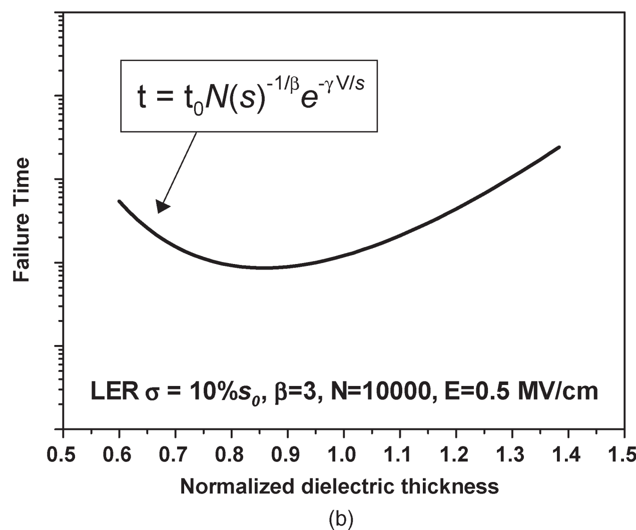


(b)

Fig. 2. (a) LER impact on failure time at acceleration test condition for LER $\sigma = 3\% s_0$ with various field model. (b) LER impact on failure time at acceleration test condition for LER $\sigma = 10\% s_0$.



(a)



(b)

Fig. 3. LER impact on failure time at use condition for (a) LER $\sigma = 3\% s_0$, (b) LER $\sigma = 10\% s_0$.

circuits [19]. For LER $\sigma = 3\% s_0$, the lowest failure time occurs in the range $0.91 \sim 0.93 s_0$ irrespective of the choice of the field model. These values are close to the minimum thickness ($s_{\min}$) anticipated for this situation, which is $0.88 s_0$. Approximating the thickness where failure occurs as $s_{\min}$, introduces an error in failure time of less than a factor of two. $s_{\min}$ will decrease with increasing the total conductor element numbers (or conductor length), but the thickness of lowest failure time will remain the same. However, the error in the failure time introduced by the use of $s_{\min}$ remains relatively little affected by the increase in N; e.g., for $N = 10^7$, $s_{\min} = 0.83 s_0$, and the error for failure time is less than a factor of three with the assumption of using E-model with field acceleration factor of 4.5 cm/MV. The situation is simplified for high LER ($\sigma = 10\% s_0$), where Fig. 2(b) shows that the thickness exhibiting lowest failure time coincides with $s_{\min}$. Therefore, these results suggest that the use of $s_{\min}$ is a good approximation to describe failure under accelerated test conditions for all magnitudes of LER, and, moreover, this is independent of the field dependence of the failure time.

These calculations were repeated for non-symmetric distributions of $N(s)$ such as log-normal. The results obtained (not shown here) were similar to that shown in Fig. 2, i.e., the failing location may be approximated as occurring at $s_{\min}$ and is independent of $N(s)$. This result is to be anticipated, since we are interested in the distribution of the minimum values of samples taken from $N(s)$; and from the well-known extreme value theorem of statistics, this distribution of $s_{\min}$ is independent of the choice of the distribution of $N(s)$. Moreover, $s_{\min}$ itself must follow extreme value statistics.

Fig. 3 plots the variation of the failure time with dielectric thickness using identical procedures to those shown in Fig. 2, but now at the low voltages that are typical of circuit operation. The thickness exhibiting the minimum failure time, s_{fail}, is a function of the voltage stress condition. For both the low and high LER, the lowest failure time occurs at the mean thickness s_0. Note that in Fig. 3(b), the mean thickness of dielectric occurs at a lower value than the line configuration. This occurs because of our assumptions of via size larger than the metal line width, and misalignment between via and underlying metal line.

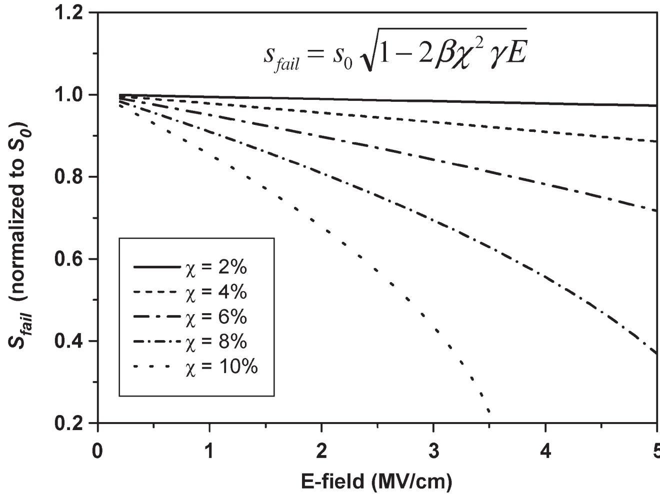


Fig. 4. Failure thickness dependence on LER magnitude with LER $\sigma = 2\% \sim 10\% s_0$.

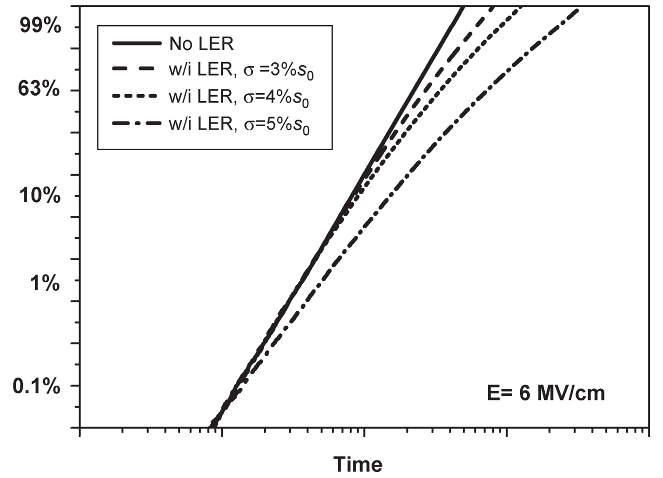


Fig. 5. Simulated failure time distribution of line-line structures with different LER magnitude from $\sigma = 0 \sim 5\% s_0$. Each distribution was normalized to its lowest failure time for the purpose of comparing the failure distribution shape.

In the practical characterization of dielectric reliability, we are interested in experimental data gathered at highly accelerated voltages. It is, therefore, important to be able to characterize $s_{\rm fail}$. The value of $s_{\rm fail}$ at any voltage is readily determined by the condition that the derivative of (2) is zero, since having shown that at high voltage, it is reasonable to assume $s_{\rm fail} = s_{\rm min}$. While a calculation of $s_{\rm min}$ requires a choice of the function form of $f(E_{\rm ILD})$, in Fig. 2, we showed that the choice of $f(E_{\rm ILD})$ does not impact $s_{\rm fail}$. Therefore, for convenience, we choose an E-model, i.e., $f(E_{\rm ILD}) = \exp(-\gamma E_{\rm ILD})$, where γ is the field acceleration factor, and $s_{\rm fail}$ is then given by

$$s_{\rm fail} = \sqrt{s_0^2 - 2\beta\sigma^2\gamma E} = s_0\sqrt{1 - 2\beta\chi^2\gamma E}. \qquad (5)$$

where $\chi \equiv \sigma/s_0$ and is about the LER severity. Fig. 4 shows, for various LER with $\chi = 2\% \sim 10\%$, $s_{\rm fail}$ is dependent on the E. The values of $s_{\rm fail}(= s_{\rm min})$ derived from (5) are in agreement with those derived from the calculations shown in Figs. 2 and 3.

C. Effect of Geometric Variations in Failure Distributions

In the proceeding section, we showed that the dielectric will fail at mean dielectric thickness at low voltage irrespective of the magnitude of LER. Therefore, at low-voltage conditions, failure time exhibits Weibull statistics as given by (2) and (3). However, at high voltages, the failure distribution will be affected by LER, and it is to be expected that for the finite populations of interconnects used for accelerated tests, and circuits, there will be variations in $s_{\rm min}$ between nominally identical samples. In this section, we demonstrate that such variations in $s_{\rm min}$ impact the shape of distribution of failure time.

The impact of $s_{\rm min}$ variation on the failure time is determined using (2). For these calculations, it is necessary to make a choice for $f(E_{\rm ILD}) = f(V/s)$. However, since all models of the field dependence produce similar failure times at accelerated voltages, this choice is not critical to the estimation of the failure time distribution and for convenience, we use an E-model for $f(E_{\rm ILD})$. The failure time, $t_{\rm fail}$, is then given by

$$t_{\rm fail} = t_0 N(s_{\rm min})^{\frac{-1}{\beta}} e^{\frac{-\gamma V}{s_{\rm min}}}. \qquad (6)$$

Fig. 5 shows the simulated failure distributions as a function of the severity of LER, where $s_{\rm min}$ was calculated using a normal distribution for $N(s)$ with a total element number of 10^4 and the β value of the intrinsic distribution of (3) is assumed to be 2.5 for 45-nm technology node, approximately. Each distribution was normalized to its lowest failure time for the purpose of comparing the failure distribution shape. Fig. 5 demonstrates that with increasing LER, failure distributions begin to deviate from Weibull at high percentiles, exhibiting an increasing concave shape. These deviations occur because the variation of $s_{\rm min}$ between devices is negligible at low percentiles, and become significant only at high percentile. This concave shape will become obscure as the intrinsic β value decreased for the same LER magnitude. From this discussion, we can clearly understand that the traditional analysis technique of linear Weibull fitting of experimental data at accelerated voltages can result in pessimistic estimation of reliability estimation. At low percentile, the intrinsic material variation, as given by (3), will dominate the variation in failure time, and so the slope of the failure time distribution in this range should determine failure times and β.

It should be noted from Fig. 5 that there are experimental difficulties to be overcome to accurately characterize failure distributions with LER. The presence of concavity in the measured failure distribution will depend on the length of the test structure, since this will determine the range of $s_{\rm min}$ that is sampled by an experimental population. For the same reason, for any conductor length, a large sample is required to observe changes in distribution shape, and as is evident from Fig. 5, sample size $\sim$100 is required when $\sigma = 3\% s_0$. Therefore, the absence of a concave shape in measured failure distributions cannot be taken to imply the absence of LER in the sample. As we will show later, using length or via-number scaling is an efficient method to increase sample size, and provides a convenient method to assess LER effects on failure distribution shape.

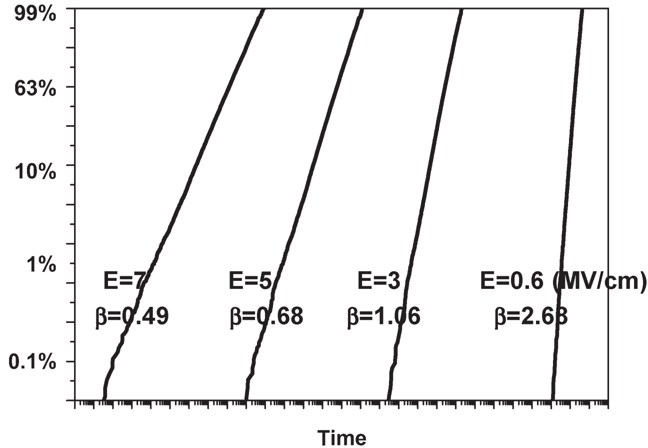


Fig. 6. Voltage dependence on failure distribution for LER $\sigma = 10\% s_0$.

D. Voltage Dependence of Failure Distribution Shape

Fig. 6 shows the simulated failure distribution with large LER $\sigma = 10\% s_0$ over a wide test voltage range, where the $s_{\min}$ distribution is obtained using the same procedure as for Fig. 5, with the assumption that intrinsic $\beta = 3$ of (3). At $E = 7$ MV/cm, the failure distribution will be dominated by variations in $s_{\min}$ between samples, i.e., the $s_{\min}$ distribution. In this case, the Weibull slope, β in the range 0.1%–99% is $\beta = 0.5$, which is much smaller than the intrinsic value of $\beta = 3$ used in the calculation. However, at $E = 0.5$ MV/cm, β is determined to be $\beta = 2.7$, which is close to the intrinsic value of $\beta = 3$. This change in β occurs because the geometry variations are significant only at high voltage (Fig. 2); while at low voltage, the intrinsic variability, from (3) dominates failure distribution. Consequently, β values determined are high voltage are not appropriate for the extrapolation of failure distributions to the low voltages typical of circuit operation. The change of β with voltage must be included to avoid overly pessimistic estimation of dielectric reliability of circuits.

III. Experimental Details

In all cases, SiOCH interlevel dielectric with $k = 2.5$ was used together with damascene Cu interconnects, which were defined by dry etching of the dielectric layer, followed by deposition of a Ta-based trench liner. The Cu conductors were defined by standard electro-plating and CMP planarization techniques and were passivated with a dielectric barrier layer. The nominal dielectric thickness is 70 nm for adjacent metal lines. For via-line structures, because via size is larger than conductor width, so the nominal thickness is smaller and that is ~48 nm for via-to-adjacent-metal lines. The metal length of the comb structures was in the range $10^3 \sim 10^5$ um, while via comb structures contained between one and 10^5 vias.

From inspection of Fig. 9, it may be observed that failure distributions at constant voltage may span several orders of magnitude of time, particularly when large variations of dielectric thickness occur. For example, the spread in via-line failure times over a measurable range of failure probability (1%–99%) can span over three orders of magnitude, which makes complete measurement of failure distributions impossible. For this reason, we use VRDB tests to complement TDDB. To use these measurement techniques interchangeably, we need to understand the relationship between them. In our TDDB testing, we typically use constant voltages that are just 1–2 V lower than the breakdown voltages obtained from VRDB. Under these circumstances, dielectric leakage mechanisms are identical for both tests, and it is, therefore, reasonable to assume that damage mechanisms are identical. The conversion between breakdown voltage and failure time can be accomplished using the field dependence of the failure time. At the high voltages typically used for stressing, it is experimentally difficult to distinguish which field model is the most accurate description to the data, i.e., all recently proposed models such as E, $\mathrm{Sqrt}(E)$, $1/E$ show similar failure times. Therefore, any of these models can be used to covert between VRDB and TDDB. Here, for mathematical simplicity, we choose the E-model for the conversion process so that the failure time and breakdown voltage are related by [13]

$$t = \frac{s}{R\gamma} \exp\left[\frac{\gamma}{s}(V_{\mathrm{BD}} - V_t)\right] \tag{7}$$

where R is voltage ramp rate, V_{BD} is the breakdown voltage and V_t is TDDB stress voltage. We have shown previously that the Weibull shape parameter, β, the field acceleration parameter, γ, and magnitude of failure times are identical for VRDB and TDDB when the conversion is accomplished using (7) [4]. For transistor gate oxides, a similar conversion process gives physical model parameters (β, γ, temperature dependence) that are independent of the measurement procedure used to define oxide breakdown [20], although in this case, the failure time is described by a power law dependence on voltage rather than an exponential relationship. The similarity between the results for low-k dielectric and gate oxides shows the general applicability of this conversion process. For the experiments described in this paper, both measurements were performed at wafer level with a temperature of $T = 125$ °C. For TDDB tests, the stress voltage was typically between 10 and 20 V while measurements of leakage currents were performed at 1 V. VRDB tests were performed with voltage ramp rates in the range of 0.001–10 V/sec, while leakage currents were measured at 1 V between increments in the stress voltage. Failure was defined as the onset of an abrupt current increase.

IV. Results

A. Characterization of Minimum Dielectric Thickness

In Section II, we showed that the minimum thickness will dominate breakdown at high voltage, and hence, the failure time distribution can be calculated using (6), provided, $S_{\min}$ can be determined. However, this presents an impossible difficulty if one assumes this must be done by physical analysis (e.g., TEM). While others have previously experimentally measured thickness variations to describe LER (i.e., $N(s)$ rather than $S_{\min}$) on a few select samples [5], [19], here, we show that it is possible to determine $S_{\min}$ from the readily available measurements of conductor geometries that are made in the

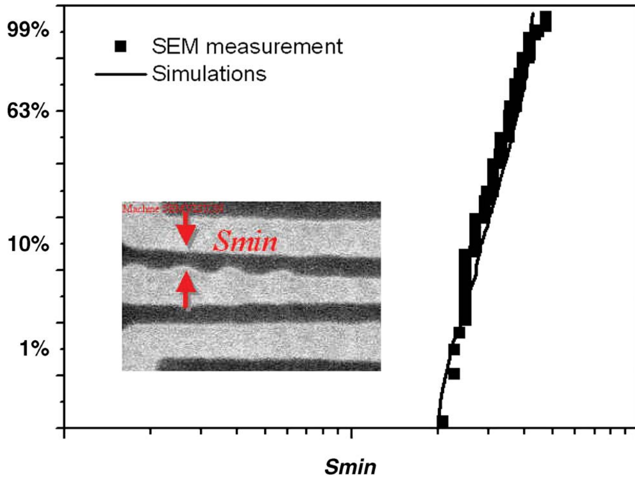


Fig. 7. SEM measurement of minimum thickness between via and adjacent line.

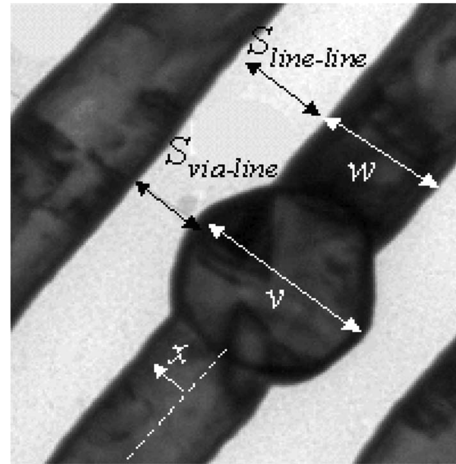


Fig. 8. Configuration of single-via structure.

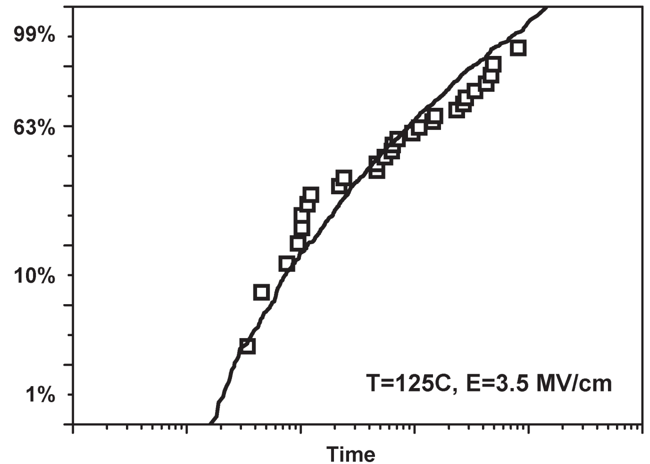


Fig. 9. Failure distributions for single via structure.

manufacturing environment, making the need to determine the thickness distribution on each sample used for testing unnecessary.

To demonstrate this technique, we use via-line test structures, since dielectric thickness variations are relatively large and can be readily measured using SEM techniques. Fig. 7 shows the measured minimum thickness distribution (i.e., the $S_{\min}$ distribution) between vias and an adjacent conductor line of a simple via chain structure consisting of six vias. These $S_{\min}$ values were determined from SEM measurements performed during the fabrication process and before the metal conductors were covered with a dielectric. This experimental distribution is well approximated by a Weibull distribution, as required from the extreme value theorem of statistics. To calculate the $S_{\min}$ distribution, we assume that the thickness of dielectric between vias and adjacent metal lines, s_i, is given by (see Fig. 8)

$$S_i = Pitch - \frac{v_i + w_i}{2} - |x| \tag{8}$$

where v is via diameter, w is conductor line width, and x is the via-to-line overlay. We generate distributions of v, w, and x based on measurements collected from several wafer lots processed with the same technology as used to generate the test structures for Fig. 8. These distributions are all well approximated as normal. Then, for each via in a test structure, we calculate S_i using (8) and determine its minimum dielectric thickness, $S_{i,\min} = \mathrm{Min}(S_1, S_2, S_3, \ldots, S_n)$. This procedure is repeated to generate $S_{\min}$ for each test structure in the experiment. As expected from the extreme value theorem, the simulated $S_{\min}$ distribution is Weibull, and closely matches the experimentally determined $S_{\min}$. We conclude that it is possible to predict $S_{\min}$ from measurements of the components of S, obviating the need for physical measurements to determine $N(s)$ and $S_{\min}$ for every sample in an experiment. Here, we have assumed that the distributions of v, w, and x do not contain defect sub-populations, [18] but the analysis is readily extended provided these distributions are known. Alternatively, this method of analysis provides a means to readily detect the presence of defective populations within experimental data.

B. Failure Distributions of Via-Line Structures

Many recent studies have indicated that breakdown at vias is the most critical issue for dielectric reliability because of lower failure time at accelerated testing conditions [2], [4], [5]. To determine how vias impact dielectric reliability, we first tested a structure containing only a single via in metal comb. Most obviously, the failure distribution shows downward curvature at low percentiles, as shown in Fig. 9, which is consistent with model results of Section II-C. Fig. 10 shows the results of further experiments performed as a function of via number for a fixed total conductor length. Larger via numbers exhibit lower failure times since they contain lower $S_{\min}$. These data show clear via number scaling, assuming Weibull statistics showing that failure times can be described by Weibull statistics despite individual distributions exhibiting significant deviations from Weibull. The lower percentiles of the failure distribution are relatively unaffected by variations in $S_{\min}$ between test structures, and the β value derived from slope of the failure distribution in this region is consistent with that given by (3). Monte-Carlo simulations were performed, assuming a β value given by (3), and $S_{\min}$ determined from (8). The simulations accurately describe the experimental data and confirm that via number scaling follows Weibull statistics. The via number

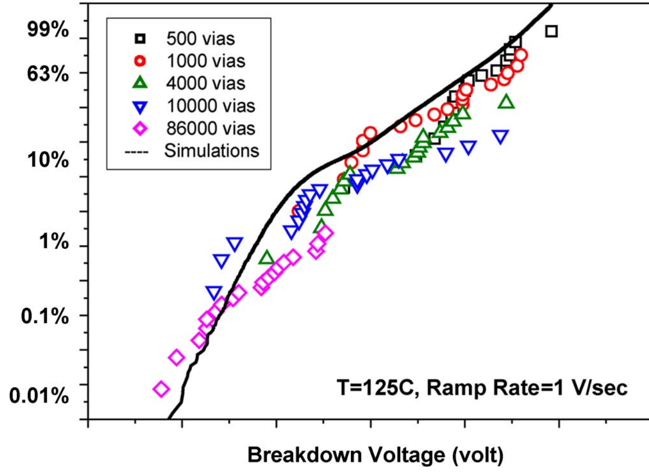


Fig. 10. Failure distributions of via-line structures with via number from 500 vias to 86 000.

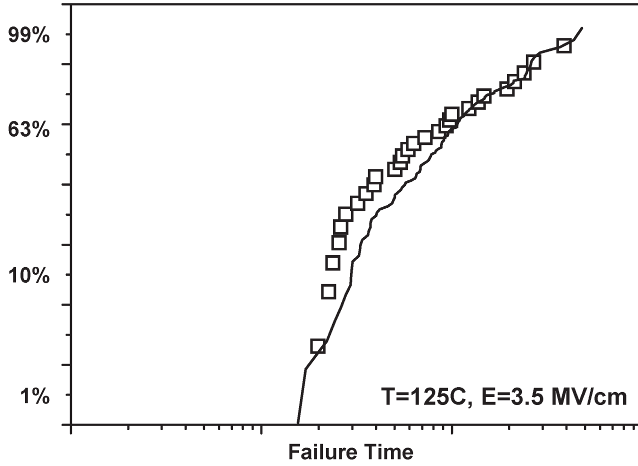


Fig. 11. Failure distributions of line-line structure.

scaling of the failure time occurs because the fundamental processes governing breakdown are described by weak-link (Weibull) statistics, while the apparent deviation from Weibull in the failure time distributions occurs because of the large range of $S_{\min}$ variation between samples.

C. Failure Time Distributions of Line-Line Structures

We also stressed metal line structures to determine the failure time distribution. Fig. 11 shows the experimental data for line-line structures together with a Monte-Carlo simulation, assuming that failure occurred at the minimum dielectric thickness. The simulation was performed, assuming that the β value for breakdown was given by (3). $S_{\min}$ was determined from a thickness distribution (S) by

$$S_i = Pitch - \frac{w_{i,1} + w_{i,2}}{2} \tag{9}$$

where $Pitch$ is the distance between the center line of the adjacent conductors, and is assumed to be constant. In this case only, the distribution of w needs to be determined, and a suitable element unit size chosen ($\sim$1 μm was used here) to generate a Monte-Carlo simulation of the $S_{\min}$ distribution. For these calculations, we used a normal distribution to describe

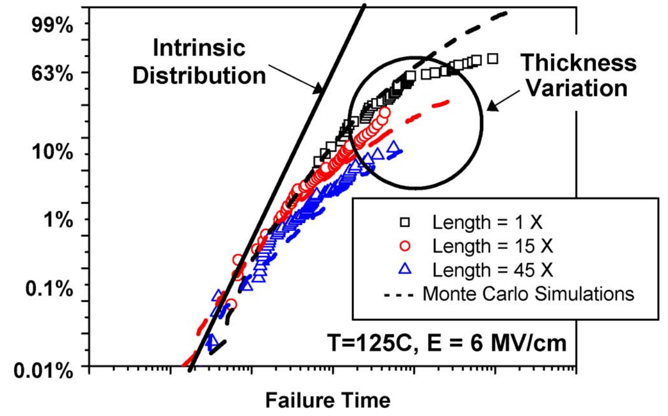


Fig. 12. Failure distribution of line-line structure with different line length.

w with a standard deviation of $\sigma = 3\%$ of the $Pitch/2$; this distribution was chosen to match experimental data for line-line space collected over a large number of wafer lots. The simulations are in excellent agreement with experimental data, indicating the minimum thickness approximation is valid to describe the breakdown of line-line structures. This is particularly significant since it is impossible to directly determine the $S_{\min}$ distribution of these test structures by physical measurements.

In addition, we performed measurements of line-line failure distributions as a function of the line-length. Fig. 12 compares experimental failure distributions with Monte-Carlo simulations, assuming Weibull statistics to describe the length scaling of the failure time. At low percentiles, Weibull scaling occurs, and the β value in this region is in close agreement with (3). The simulations are in good agreement with the experimental data and confirm that the distortion from Weibull can be easily observed by length scaling experiments.

D. Voltage Dependence of Failure Distributions

An important implication of our model of failure is the systematic change of β with deceasing voltage for interconnects exhibiting LER. However, it is difficult to observe this β change under high-voltage stress conditions particularly for typical metal comb structures [8]. This is because the LER magnitude of the metal comb structure is much less than dielectric thickness and, hence, the β change is small. Therefore, the via-line structure was used to characterize the systematic β change with voltage conditions because via-line misalignment can cause much larger thickness variation compared to metal comb structures. In this case, it is important to be able to collect complete failure distributions over a wide range of voltage, and so we use the VRDB technique for this experiment. The precise calculation of β from VRDB depends on the field dependence of failure. However, as we have discussed previously, at high-voltage, failure times are essentially independent of the field model and so we use an E-model for the convenience to convert the breakdown voltage to failure time. The breakdown voltage $(V_{\rm BD})$ is then exponentially related to failure time, and the slope of the Weibull VRDB breakdown distribution is $\beta\gamma/s_0$. As may be seen from (7), varying the voltage ramp rate, R, in a VRDB test is equivalent to changing voltage in a constant voltage test. Therefore, we performed VRDB measurements

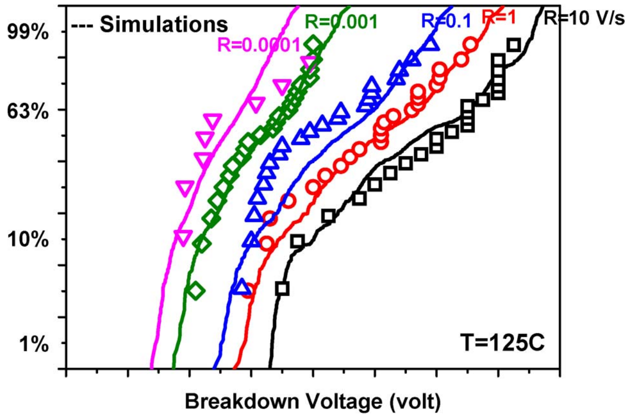


Fig. 13. Failure distribution of via structures for voltage ramp rate in a range of $R = 0.0001 \sim 10$ V/sec.

over a wide range of R to determine how β varies with the equivalent constant voltage. Fig. 13 shows via-line VRDB failure distributions measured as a function of R. The data shows a clear increase in the β of the failure distributions (slope) as R is decreased. Simulations of the breakdown voltage distributions were performed. We first simulate the $S_{\min}$ distribution follow the procedure described in Section IV-A and obtain the failure time distribution from $S_{\min}$ distribution using (6). Then, the breakdown voltage distribution can be converted from the failure time to breakdown voltage conversion using (7). The simulated breakdown voltage distributions in Fig. 13 are all from the identical $S_{\min}$ distribution but with different voltage ramp rate. The simulated distributions are in good accordance with the experimental data.

V. Discussion

Much attention has been paid recently to the precise electric field dependence of breakdown since this has a strong impact on reliability projections. Besides the thermo-mechanical E-field model, which has been adapted from gate oxide studies to metal dielectrics, several current conduction-based models have been suggested which exhibit $\mathrm{Sqrt}(E)$ or $1/E$ characteristics [21], [22]. Kim experimentally investigated low-k dielectric breakdown of line structures with $k = 2.9$ and s_0 of 130 nm, and found that it follows closely an E-model [6]. However, based on observations performed at dielectric thickness of 100 nm and below, both Chen and Suzumura considered breakdown to be associated with a critical copper concentration in the dielectric [7], [8]. Since this concentration depends on the current conduction mechanism, i.e., Schottky or Poole-Frenkel, the failure time exhibits a $\mathrm{Sqrt}(E)$ dependence. Chen have shown that the magnitude of LER depends on dielectric thickness between adjacent metal lines, with smaller thickness exhibiting larger LER. For example, for a nominal thickness of 70 nm, the average LER is $\sim$15%, while for a nominal thickness of 90 nm, the average LER is less than 5% [1]. It is possible that the discrepancy of the experimentally determined field dependence between studies could be related to differing magnitude of LER magnitude in test samples. This is readily understood by examining the calculations of s_{fail} as a function of voltage in Figs. 2 and 3. At high voltage, the most probable

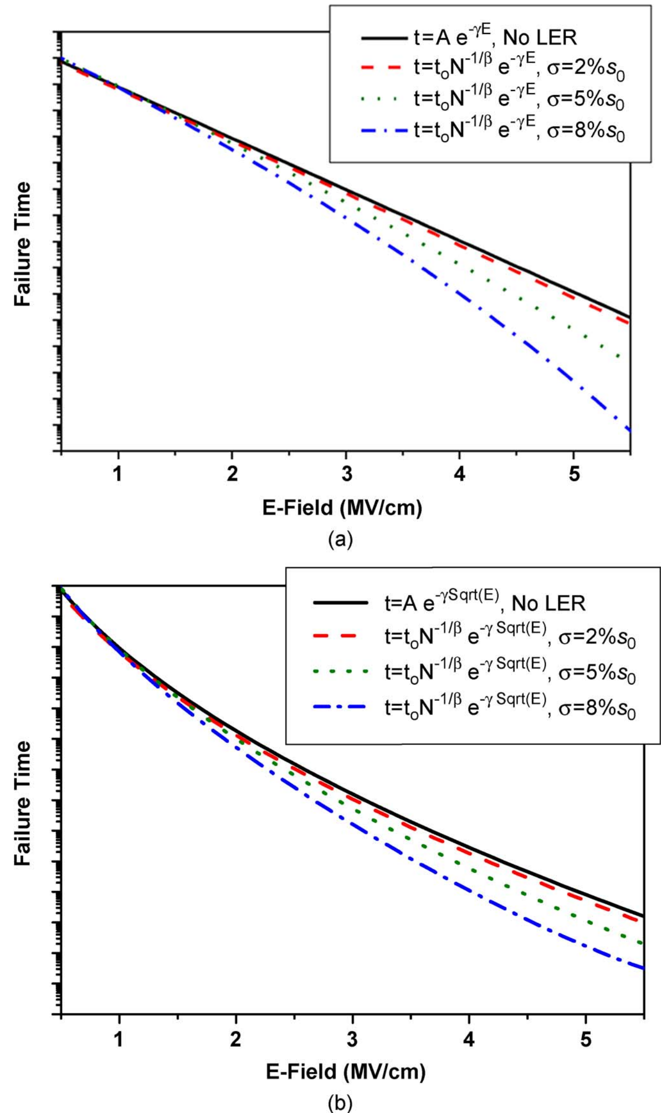


Fig. 14. Simulated field dependence on failure time with LER severity of $\sigma = 0 \sim 8\% s_0$ with field model of (a) E-model and (b) $\mathrm{Sqrt}(E)$ model.

failure location, s_{fail}, will be close to $s_{\min}$, but as the voltage is lowered, s_{fail} transitions toward the mean thickness, s_0. The implication is the relevant field to be used to determine the breakdown time is given by (V/s_{fail}) rather than (V/s_0). Therefore, omitting LER in the consideration of the field magnitude can be viewed as introducing systematic errors in measurements of the field dependence where the assumption is usually made that the dielectric thickness where failure occurs is constant.

Fig. 14 shows the predicted field dependence of the failure time from (2) as a function of LER in the range $\sigma = 0\text{--}8\% s_0$ for linear E and $\mathrm{Sqrt}(E)$ model. It is clear from Fig. 14 that, irrespective of the field dependence, LER lowers the failure time at high voltage due to the high acceleration associated with failure at $S_{\min}$. However, as the voltage is lowered, from (2), failure occurs at $S > S_{\min}$ and failure times increase; thus, measurements of the field dependence, which typically involve sampling a small number of relatively high field values, leads to a deviation from the true field dependence. The observed field dependence now depends strongly on the magnitude of LER,

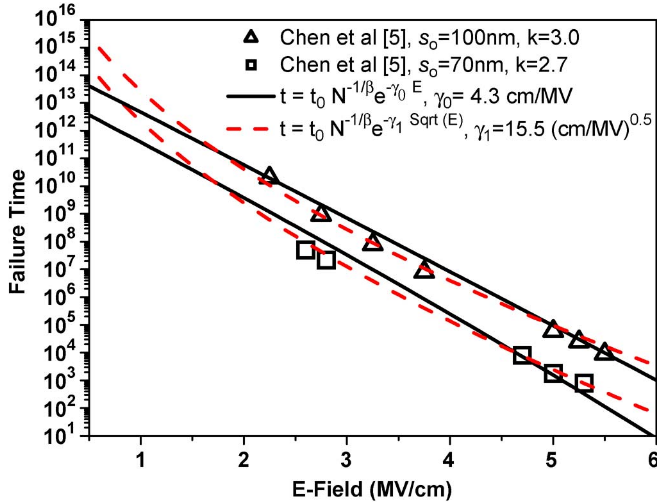


Fig. 15. Modeling of LER impact on electric field dependence of dielectric breakdown on published data from Chen *et al*. [5].

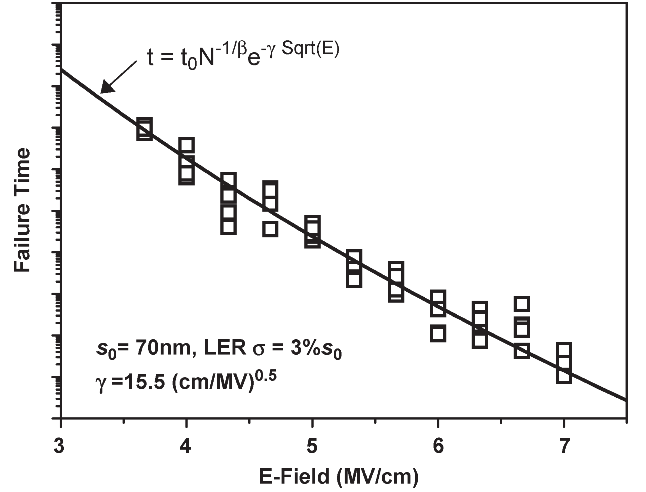


Fig. 16. Modeling of LER impact on electric field dependence of dielectric breakdown on $s_0 = 70$ nm, $k = 2.5$ dielectric.

and shows increasing sensitivity to field as LER increases. The latter observation implies that it will become increasingly difficult with scaling to use measurements of the field dependence to infer the physical mechanism of breakdown. As an example, consider that for a true $\mathrm{Sqrt}(E)$ dependence, with unaccounted for LER, the greater field sensitivity of the measured failure time could be simply interpreted as an indication as a change to a $1/E$—like field dependence. Clearly, LER effects must be considered to consistently interpret experimental data.

Given the ambiguity that LER may introduce into measurements of the field dependence, we have examined published data to attempt to determine if LER has contaminated the interpretation of these results. Fig. 15 compares our model predictions with published experimental data for the 65- and 45-nm technology nodes [1], [5]. For the model fits to the experimental data, we use the reported LER and β; i.e., 65 nm node: LER $\sigma = 2\% s_0$ and $\beta = 4.5$ with 100-nm dielectric thickness; 45-nm node: LER $\sigma = 5\% s_0$ and $\beta = 2$ with 70-nm thickness. We assumed that in both cases, $N(s)$ was normal, although as we showed in Section II, this assumption is not critical to the analysis. The characteristic element failure time (t_0) and field acceleration factor is assumed to be identical in both technology nodes. In Fig. 15, we use both $\mathrm{Sqrt}(E)$ and E-models with the correction of LER effect for the failure time. We obtain good fits to the data for both E-field functionalities, although it is clear that the fit to the experimental data with a $\mathrm{Sqrt}(E)$ function is better over the whole fit range. Our results are consistent with the suggestion that breakdown of low-k dielectrics is governed by a $\mathrm{Sqrt}(E)$ field dependence, but the similarity between models to the experimental data highlight the difficulty in determining the field model unambiguously. To provide convincing evidence of the true field dependence of breakdown, this form of verification of the field functionality requires much more extensive data collected at significantly lower, or higher fields, than is currently available. Instead, models of failure that emphasize a detailed understanding of the microscopic understanding of the nature of the damage should be emphasized, since these models may be tested for validity with data other than from accelerated testing.

The field acceleration factor used in the model fits shown in Fig. 15 is identical for both the 65- and 45-nm technologies, e.g., the $\mathrm{Sqrt}(E)$ fit requires an acceleration factor $\gamma = 15.5$ (cm/MV)$^{0.5}$. Without the consideration of LER, the γ values required for fitting are 17 and 16.2 (cm/MV)$^{0.5}$ for of 65- and 45- nm technologies, respectively. While given the experimental uncertainty, it is not clear if these latter values are statistically different, the field acceleration factor is a material parameter that should be independent of process technology for the same dielectric material (i.e., Si-O based) [12]. We confirmed this contention by investigating the field dependence of a line structure with 70-nm dielectric thickness and $k = 2.5$, as shown in Fig. 16. This data is accurately modeled assuming a $\mathrm{Sqrt}(E)$ dependence with $\gamma = 15.5$ (cm/MV)$^{0.5}$. Our model, therefore, provides a consistent physical picture of the breakdown process as a function of feature size scaling.

VI. Conclusion

We have investigated the impact of geometric variations in Cu conductor geometry (due to line edge roughness and via misalignment) on Cu/Low-k interconnect dielectric reliability. By considering the statistical distribution of thickness between adjacent conductors exhibiting LER, we have developed a model that shows the dielectric breakdown location can be approximated as being at the minimum dielectric thickness present in a test structure or circuit at high voltage. However, the failure location is a function of voltage, and moves to the median thickness at the low-voltage conditions typical of circuit operation. The minimum dielectric thickness present on a test structure or on a circuit is readily determined on a statistical basis from routine measurements of dielectric thickness between metal lines, obviating the need to determine it by physical inspection for each test structure prior to reliability testing. Using these concepts, we show that LER modifies the functional form of failure distributions, necessitating novel analysis for the accurate estimation of circuit failure times. Further, it leads to a systematic change in the failure distribution shape with voltage, as characterized by the Weibull β which requires a new reliability extrapolation methodology to ensure

the accuracy of reliability predictions. We verify these theoretical predictions using measurements of failure distributions of both via and line test structures. Finally, we have shown that LER can significantly modify the apparent field dependence of the failure time, leading to ambiguity in the interpretation of the experimentally determined field dependence.

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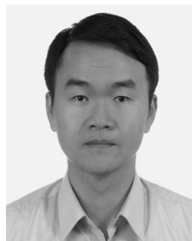

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