Design of Flip-Chip Interconnect Using Epoxy-Based Underfill Up to V-Band Frequencies With Excellent Reliability

Li-Han Hsu, *Student Member, IEEE*, Wei-Cheng Wu, Edward Yi Chang, *Senior Member, IEEE*, Herbert Zirath, *Senior Member, IEEE*, Yin-Chu Hu, Chin-Te Wang, Yun-Chi Wu, and Szu-Ping Tsai

***Abstract*—This study demonstrates a flip-chip interconnect with epoxy-based underfill ($\varepsilon_r = 3.5$ and $\tan\delta = 0.02$ at 10 MHz) for packaging applications up to V-band frequencies. To achieve the best interconnect performance, both the matching designs on GaAs chip and Al_2O_3 substrate were adopted with the underfill effects taken into consideration. The optimized flip-chip interconnect showed excellent performance from dc to 67 GHz with return loss below −20 dB and insertion loss less than 0.6 dB. Furthermore, the dielectric loss induced by the underfill was extracted from measurement and compared with the simulation results. The reliability tests including 85 °C/85% relative humidity test, thermal cycling test, and shear force test were performed. For the first time, the S-parameters measurement was performed to check the flip-chip reliability, and no performance decay was observed after 1000 thermal cycles. Moreover, the mechanical strength was improved about 12 times after the underfill was applied. The results show that the proposed flip-chip architecture has excellent reliability and can be applied for commercial applications.**

***Index Terms*—Design, epoxy resin, flip-chip, interconnect, millimeter wave (MMW), packaging, reliability, underfill, V-band.**

I. INTRODUCTION

IN RECENT years, with the demands for wireless communication systems increases rapidly, the operating frequency for the portable wireless is moving toward millimeter waves (MMWs). To meet the demands for commercial applications, package with low power consumption, low cost, small size, and light weight becomes indispensable. In this respect, the flip-chip interconnect has been regarded as a promising packaging technology for cost-effective module assembly in MMW systems due to its shorter interconnect length, higher throughput for production, and smaller package size [1]–[9]. The flip-chip reliability, however, needs to be carefully considered since it relies only on several metallic connections between chip and carrier. One promising solution is using underfill to improve the reliability by enhancing the joint strength, protecting the interconnect from mechanical shock, and helping the heat dissipation [10]–[13]. However, underfill may result in performance degradation due to its higher dielectric constant (ε_r) and loss tangent ($\tan\delta$) compared to the air [14]–[16], which limits the usage of the flip-chip interconnect for high-frequency applications. This is one of the reasons why bond-wire is still the favorite packaging technology in microwave industry.

The RF characteristics of the flip-chip assembly with epoxy-based underfill have been investigated up to 40 GHz [15], demonstrating an additional insertion loss of 0.5 dB at 30 GHz. Kusamitsu *et al.* reported the RF characteristics of the flip-chip assembled 30-, 60-, and 77-GHz low-noise amplifier (LNA) monolithic microwave integrated circuits (MMICs) [16]. Due to the underfill effect, the frequency response of the MMICs shifted to lower frequency bands. The 30-GHz LNA was shifted by 3 GHz; the 60- and 77-GHz LNAs were shifted by 9 GHz.

In a flip-chip interconnect, the RF degradation due to underfill is induced by three major factors: chip impedance change, parasitic capacitance, and material dielectric loss. The high dielectric constant of the underfill ($\epsilon_r = 3 \sim 4$ typically) tends to reduce the chip line impedance, resulting in impedance mismatch and reflection at the transitions [14]. By using low-k underfill or designing in advance with the underfill effects taken into account can ease this problem. Regarding to the parasitic effect, the flip-chip interconnect generally shows an overall capacitive effects [1], [2], which could degenerate the interconnect performance at MMW frequencies. Due to the underfill injection, the parasitic capacitance at the interconnect increases, indicating that a more inductive counterpart is needed for compensation. Furthermore, a dielectric loss is induced as an epoxy-based underfill ($\tan\delta = 0.007 \sim 0.02$) is applied. The loss can be reduced by introducing low-loss materials such as benzocyclobutene (BCB) or other porous low-k materials.

Moreover, for most commercial applications, reliability investigations are generally required. The adhesion and coefficient

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L.-H. Hsu and W.-C. Wu are with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, MC2, Chalmers University of Technology, Göteborg SE-412 96, Sweden (e-mail: jones2.mse94g@nctu.edu.tw; williamwu.mse90g@nctu.edu.tw; lihan@chalmers.se).

E. Y. Chang, C.-T. Wang, Y.-C. Wu, and S.-P. Tsai are with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: edc@mail.nctu.edu.tw; rinexoper.mse95g@nctu.edu.tw; mai.mse96g@nctu.edu.tw; waterboyz@pchome.com.tw).

H. Zirath is with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, MC2, Chalmers University of Technology, Göteborg SE-412 96, Sweden (e-mail: herbert.zirath@chalmers.se).

Y.-C. Hu was with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan. He is now with Everlight Electronics, Taipei 236, Taiwan.

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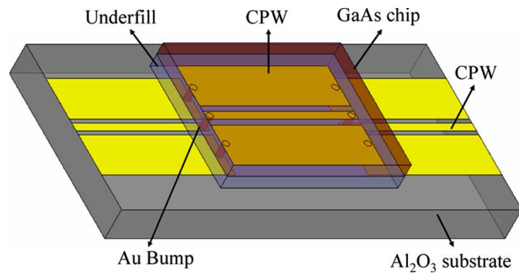


Fig. 1. Schematic of the flip-chip interconnect structure with underfill in this study (without any matching structure adopted).

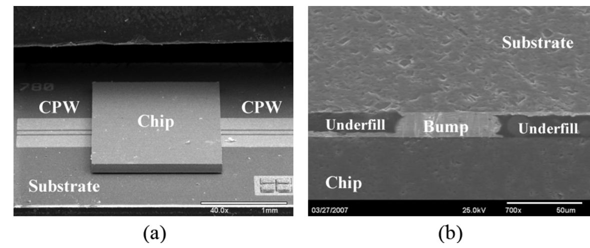


Fig. 2. SEM images of the: (a) fabricated flip-chip interconnect structure and (b) cross-sectional SEM image of the flip-chip interconnect structure at the bump transition region.

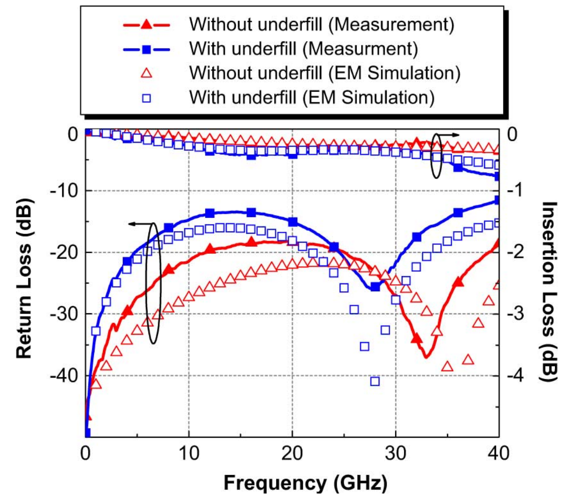


Fig. 3. Measured and simulated S-parameters of the flip-chip interconnect with and without underfill.

of thermal expansion (CTE) mismatch between chip and carrier are very important factors for the flip-chip reliability. For MMW flip-chips, the adhesion relies only on a few bump interconnections, which is deficient and very fragile at mechanical vibration. Besides, the CTE mismatch between chip and carrier could lead to joint fatigue during temperature variation. By using underfill as a buffer layer, the adhesion can be improved and the thermal stress can be reduced significantly. Some investigations about the MMW flip-chip reliability with epoxy underfill have been reported previously [15]–[17]. The fatigue life of the flip-chip assembly with underfill was investigated using finite-element analysis (FEA) simulation [15]. The simulation results indicated that the joint fatigue life improved significantly after underfill was applied. Schmückle *et al.* demonstrated that using an Al_2O_3 carrier $(\mathrm{CTE} = 6.3\ \mathrm{ppm/K})$ for a GaAs $(\mathrm{CTE} = 5.7\ \mathrm{ppm/K})$ flipped-chip has negligible thermal effect due to their small CTE mismatch [17]. However, the adhesion between chip and carrier should be taken into account before commercial applications can be realized.

In this study, the flip-chip assembly with epoxy-based underfill was designed, fabricated, and characterized up to 67 GHz. The reliability tests including a 85 $^\circ$C/85% relative humidity (RH) test, thermal cycling test, and shear force test were performed to evaluate the feasibility of such packages for practical applications.

II. Test Structure and Fabrication

Fig. 1 shows the schematic of the flip-chip interconnect structure with underfill in this study (without any matching structure adopted). The GaAs chip and Al_2O_3 substrate with the thickness of 100 and 254 μm, respectively, were employed. The metallization was 3 μm Au (gold). The characteristic impedances (Z_0) of the coplanar waveguide (CPW) transmission lines on the chip and substrate were both 50 Ω. The total length of the back-to-back flip-chip interconnect structure was 3000 μm, including 1000 μm on the chip and 2000 μm on the substrate. The dimensions of the bump were fixed due to the fabrication concern. The diameter of the bump was 50 μm; the bump height was 20 μm.

The CPW transmission lines were first patterned and electroplated on the GaAs chip. The chip was then upside-down mounted on a sapphire carrier for thinning down to 100 μm. After de-mounting from the sapphire carrier, the chip was diced into individual dies. The substrate with an Au CPW circuit and a bump was fabricated by an in-house bumping process, as reported in [18]. The Au-to-Au thermo-compression process was performed to bond the flip-chip interconnect structure. Fig. 2(a) shows the scanning electron microscope (SEM) image of the fabricated flip-chip interconnect structure.

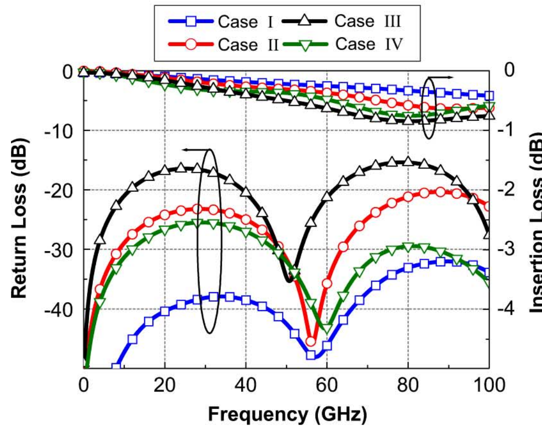
After flip-chip bonding, the epoxy-based underfill ($\varepsilon_r = 3.5$ and $\tan\delta = 0.02$ at 10 MHz) was injected into the gap between the chip and substrate by a capillary underfill process and cured at 150 $^\circ$C for 2 h. Fig. 2(b) shows the cross-sectional SEM image at the Au bump region. As shown in the micrograph, the underfill was successfully filled into the gap without any voids.

III. Design and Optimization

The fabricated flip-chip samples were measured using on-wafer probing measurement with a short-open-load-thru (SOLT) calibration technique. During the measurement, a 10-mm-thick layer of Rohacell 31 ($\epsilon_r = 1.04$ at 26.5 GHz) was placed between the sample and the metal chuck of the probe station to avoid the grounded backside under the substrate. Fig. 3 shows the measured and simulated S-parameters of the flip-chip interconnect with and without underfill from dc to 40 GHz. It is shown that both the return loss ($S11$) and insertion loss ($S21$) became worse after the underfill was applied. The $S11$ was increased about 5 $\sim$ 10 dB from dc to 40 GHz and the resonance frequency with lowest reflection shifted from 33 to 28 GHz. The reason is that the effective dielectric constant $(\varepsilon_{\mathrm{eff}})$ changed due to the insertion of the underfill. This effect will be further discussed in the following Section III-A. Furthermore, the underfill also induced significant dielectric loss

	Cross-Sectional Views of the CPW Structures	Simulated Parameters
Case I	CPW line; G S G; GaAs	—S = 70 μm —G = 44 μm —Z_0 = 50Ω —ε_{eff} = 6.87
Case II	GaAs; G S G; Air (ε_r=1); Al_2O_3	—S = 70 μm —G = 44 μm —Z_0 = 45Ω —ε_{eff} = 7.10
Case III	GaAs; G S G; UF (ε_r=3.5); Al_2O_3	—S = 70 μm —G = 44 μm —Z_0 = 41Ω —ε_{eff} = 8.77
Case IV	GaAs; G S G; UF (ε_r=3.5); Al_2O_3	—S = 70 μm —G = 84 μm —Z_0 = 50Ω —ε_{eff} = 6.52

(a)



(b)

Fig. 4. (a) Simulation structures and CPW parameters for Case I (bare CPW line on GaAs chip), Case II (CPW + Al_2O_3), Case III (CPW + Al_2O_3 + Underfill), and Case IV (CPW + Al_2O_3 + Underfill with Z_0 matching). (b) Simulated S-parameters. (The CPW line length is 1000 μm; the gap between the GaAs chip and Al_2O_3 substrate is 20 μm; the thickness of the GaAs is 100 μm; the thickness of the Al_2O_3 is 254 μm.)

to the overall loss. The $S21$ degraded about 0.2 $\sim$ 0.4 dB from dc to 40 GHz.

In Sections III-A–C, both matching designs on the GaAs chip and Al_2O_3 substrate were performed, targeting on a broadband interconnect performance with low return loss and low insertion loss. Moreover, the dielectric loss induced by underfill was extracted from the measurement and simulation for comparison.

A. Matching Design on GaAs Chip

An underfill with $\varepsilon_r > 1$ acts to lower the Z_0 of the transmission line, leading to the performance deviation of the MMIC chip [14]. To solve this issue, the most effective method is to design in advance by taking the underfill effects into account. Fig. 4 shows the simulated CPW parameters and S-parameters of a 50-Ω CPW transmission line on GaAs chip. As can be seen, a 50-Ω CPW line ($\varepsilon_{eff} = 6.87$) showed a simulated $S11$ of below -30 dB from dc to 100 GHz (Case I). After the flip-chip, an Al_2O_3 substrate is present under the CPW circuit (Case II).

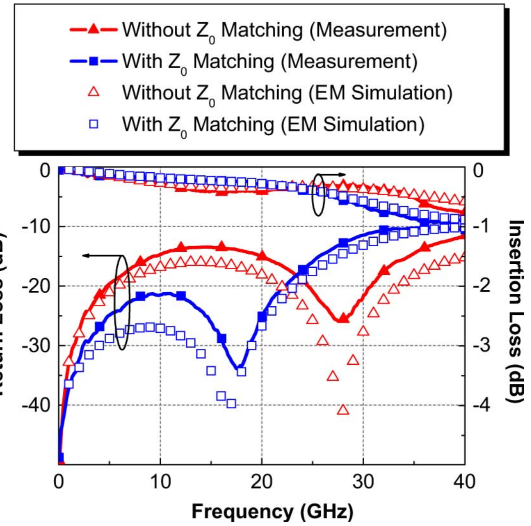


Fig. 5. Measured and simulated S-parameters of the flip-chip assembly with and without Z_0 matching.

ε_{eff} slightly increased to 7.10 and Z_0 became 45 Ω due to the flip-chip detuning effect. The $S11$ degraded about 10 dB in average as compared to Case I. When an epoxy-based underfill with $\varepsilon_r = 3.5$ was applied (Case III), the ε_{eff} increased to 8.77 and the $S11$ minimum shifted to lower frequency (from 57 to 51 GHz). Z_0 was further lowered to 41 Ω and $S11$ decayed up to -16 dB. In Case IV, Z_0 was 50 Ω after modifying G (the gap between the signal and ground conductor) to 84 μm. ε_{eff} was 6.52 and the simulated $S11$ was below -25 dB from dc to 100 GHz.

Based on the simulation, the flip-chip assembly with the impedance matching design on the GaAs chip was fabricated and measured. Fig. 5 shows measurement and simulation results. After the matching design was adopted, $S11$ and $S21$ improved below 25 GHz, but became worse beyond 25 GHz. At higher frequencies, the parasitic capacitance becomes significant, especially when the underfill is injected. The parasitic capacitance can be reduced and compensated with proper matching design on the Al_2O_3 substrate.

B. Matching Design on Al_2O_3 Substrate

Generally speaking, a flip-chip interconnect shows an overall capacitive effect, which would result in impedance mismatch and reflection at MMW frequencies [1], [2]. To improve the interconnect performance, reducing and compensating the parasitic capacitance by employing proper matching design on the packaging carrier is essential. In previous reports, the MMW flip-chip interconnect with a matching design on the packaging carrier has been studied and investigated [1]–[9]. It has been demonstrated that reducing the metal pad overlap, increasing the bump height, and employing the inductive compensations can improve the reflection at the transitions [1]–[9]. Fig. 6 shows the optimized interconnect structure and performance after both matching designs on the GaAs chip and Al_2O_3 substrate were adopted. The matching designs on the Al_2O_3 substrate included a small metal pad overlap ($l_{ob} = 70$ μm), a high impedance line ($C_W = 20$ μm), and a ground pad shrinking ($S_W = 55$ μm). The bump height (B_h) was fixed to 20 μm due to the fabrication

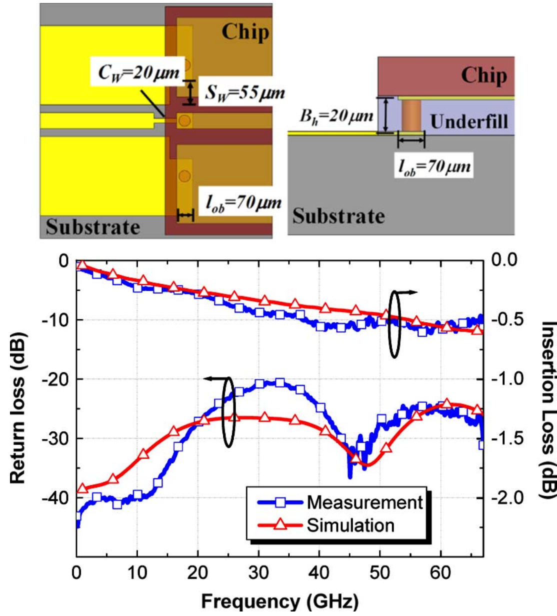


Fig. 6. Optimized interconnect structure and performance.

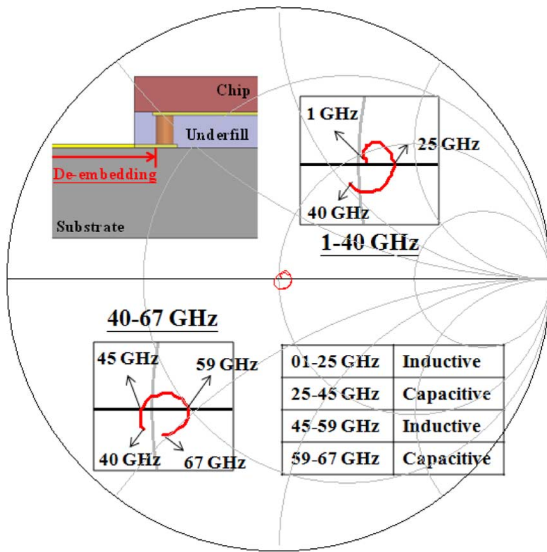


Fig. 7. De-embedded $S11$ of the optimized interconnect structure from 1 to 67 GHz (EM simulation).

concern. As can be seen, the flip-chip interconnect showed good broadband performance up to 67 GHz. From dc to 40 GHz, $S11$ was less than -20 dB; from 40 to 67 GHz, $S11$ was less than -25 dB. $S21$ was within 0.6 dB from dc to 67 GHz, demonstrating excellent performance for flip-chip assembly with underfill material. Fig. 7 shows the de-embedded $S11$ from the electromagnetic (EM) simulation. The inductive and capacitive behaviors versus frequency bands indicate that the matching designs were well adopted with a good counterbalance between the inductance and capacitance at the transition.

C. Dielectric Loss of Underfill Material

The loss induced by the underfill is not only due to the mismatch loss (reflection), but also due to the real loss (attenuation). In general, the real loss consists of three components: metal loss,

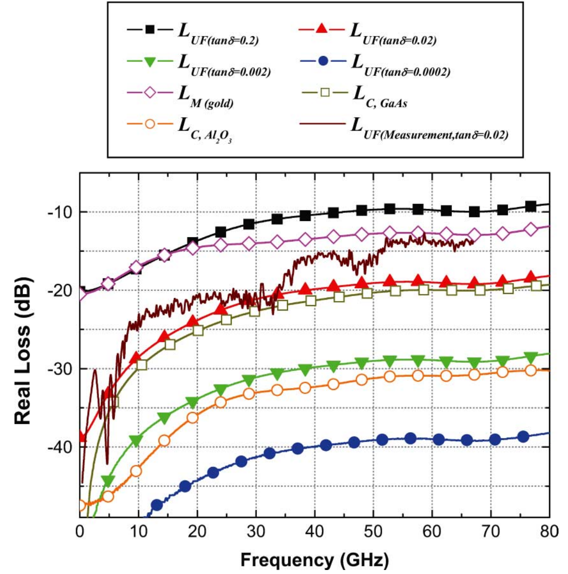


Fig. 8. $L_{\mathrm{UF}(\tan\delta=x)}$, $L_{C,\mathrm{GaAs}}$, $L_{C,\mathrm{Al_2O_3}}$, and $L_{M(gold)}$ of the flip-chip assembly as extracted from the EM simulation; the $L_{\mathrm{UF(Measurement},\tan\delta=0.02)}$ was extracted from the measurement for comparison.

dielectric loss, and radiation loss. For a flip-chip assembly, the radiation loss is very small so that it can be neglected. The dielectric loss means an overall loss in carriers (chip and substrate) and underfill. To specifically identify the carrier loss (L_C), underfill loss (L_{UF}), and metal loss (L_M), the following calculations were employed. Equation (1) is the definition of the loss factor [19], the real loss (L_{Real})

$$L_{\mathrm{Real}} = 1 - |S11|^2 - |S21|^2. \tag{1}$$

To get the real loss induced by underfill with $\tan\delta = x$, one can subtract the real loss of the flip-chip assembly with $\tan\delta = 0$ from the real loss of the flip-chip assembly with $\tan\delta = x$. Equation (2) gives the real loss induced by underfill. A similar approach can be applied for calculating the chip loss $(L_{C,\mathrm{GaAs}})$ and substrate loss $(L_{C,\mathrm{Al_2O_3}})$. Equation (3) gives the real loss induced by carriers. In the simulation, the $\tan\delta$ of GaAs and Al_2O_3 were set to be 0.006 and 0.0002, respectively,

$$L_{\mathrm{UF}(\tan\delta=x)} = L_{\mathrm{Real,UF}(\tan\delta=x)} - L_{\mathrm{Real,UF}(\tan\delta=0)} \tag{2}$$

$$L_{C(\tan\delta=x)} = L_{\mathrm{Real,Carrier}(\tan\delta=x)} - L_{\mathrm{Real,Carrier}(\tan\delta=0)}. \tag{3}$$

On the other hand, to get the real loss induced by metal (gold), one can subtract the real loss of the flip-chip assembly with a perfect electrical conductor (PEC) from the real loss of the flip-chip assembly with a gold conductor. Equation (4) gives the real loss induced by metal as follows:

$$L_{M(\mathrm{gold})} = L_{\mathrm{Real,gold}} - L_{\mathrm{Real,PEC}}. \tag{4}$$

Fig. 8 shows the underfill loss $(L_{\mathrm{UF}(\tan\delta=x)})$, chip loss $(L_{C,\mathrm{GaAs}})$, substrate loss $(L_{C,\mathrm{Al_2O_3}})$, and metal loss $(L_{M(\mathrm{gold})})$ of the flip-chip assembly as extracted from the EM simulation. The underfill loss was also extracted from the measurement $(L_{\mathrm{UF(Measurement},\tan\delta=0.02)})$ for comparison. In this study, $\tan\delta$ of the underfill was 0.02 at 10 MHz. As can

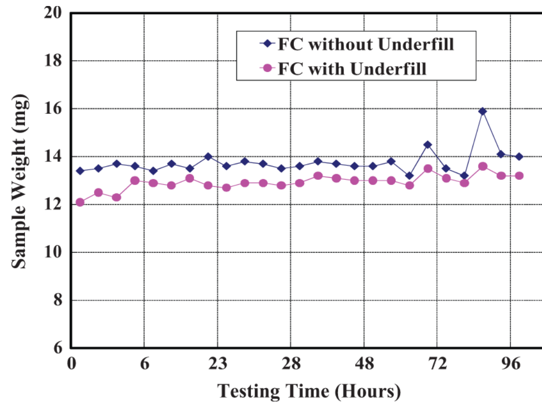


Fig. 9. 85 °C/85% RH test results of the flip-chip assembly.

be seen, at lower frequencies, the measurement and simulation showed fair agreement, below −20 dB from dc to 35 GHz. Beyond 35 GHz, the underfill loss decayed up to −13 dB, which is almost the same level as the metal loss, the dominant loss at MMW frequency. The underfill loss can be minimized by using low-loss underfill material with $\tan\delta < 0.02$. Further reducing $\tan\delta$ to less than 0.0002 is not necessary since the induced loss is too small and can be neglected.

IV. Reliability and Mechanical Strength

Reliability investigation is always essential for commercial applications. In Sections IV-A–C, three types of reliability tests, i.e., 85 °C/85% RH test, thermal cycling test, and shear force test, were performed to test the interconnect reliability of the flip-chip assembly.

A. 85 °C/85% RH Test

The water absorption is an important issue, which would compromise the reliability during a long-term operation, especially for a package with polymer materials. To test the water absorption of the flip-chip assembly, the samples were stored in an testing environment of 85 °C and 85% RH for 96 h. Fig. 9 shows the testing results. The weight increased 4.3% (0.6 mg) for the sample without underfill and 6.8% (0.9 mg) for the sample with underfill after 96-h testing. The underfill contributed the water absorption of around 2.5% weight to the tested samples. Furthermore, no electrical failure was observed after the test.

B. Thermal Cycling Test

During temperature variation, the CTE mismatch between the chip and packaging carrier could lead to joint fatigue and consequent failure. To test the interconnect reliability, the thermal cycling test, i.e., temperature range from −55 °C to 125 °C with 15-min dwell time (specification of the Joint Electron Device Engineering Council (JEDEC) standard) was employed. The contact resistance measurement and S-parameters measurement were used to check the testing results. In Fig. 10, it indicates that no sample failed and the contact resistance showed negligible change during the test no matter with or without underfill. Fig. 11 shows the comparison of the measured S-parameters (with underfill) before and after 1000 thermal cycles. The

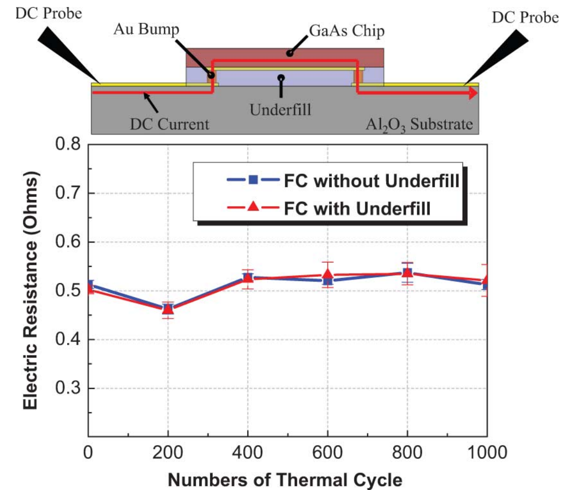


Fig. 10. Thermal cycling test results of the flip-chip assembly.

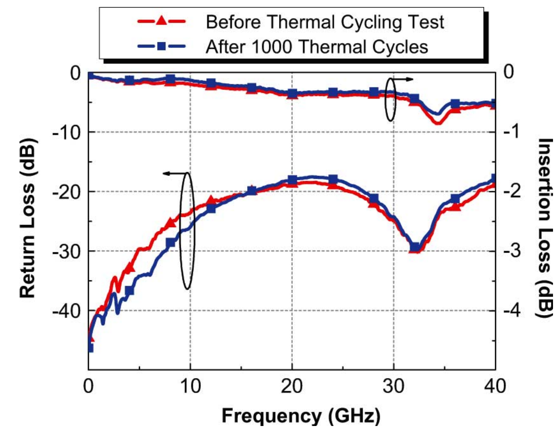


Fig. 11. Measured S-parameters of the flip-chip assembly (with underfill) before and after thermal cycling test.

RF performance did not decay after the test, showing excellent thermal mechanical stability of the flip-chip assembly. To the best of our knowledge, this was the first time the S-parameters measurement was employed to check the flip-chip reliability in open literature.

Table I shows the material properties of some commonly used chip and substrate materials. As can be seen, GaAs, Si, and Al_2O_3 have similar CTE and small CTE mismatch. Hence, using the Al_2O_3 substrate for GaAs or Si flipped-chips has a negligible thermal effect in temperature variation [17]. This point is also supported by the testing results above. However, if one wants to further reduce cost by introducing organic substrates, the CTE mismatch becomes an important issue, and hence, the underfill is essential to improve the reliability.

C. Shear Force Test

Adhesion between the chip and substrate is very critical to the flip-chip reliability since it relies only on a few metallic connections, which is deficient and very fragile at mechanical vibration. The shear force test was performed to investigate the adhesion of the flip-chip assembly. Fig. 12 shows the testing results. Four samples were tested for each condition to obtain the average shear force. The shear force of the samples without

TABLE I
$\text{Tan}\delta$, ε_r, COST AND CTE OF COMMON CHIP AND SUBSTRATE MATERIALS

	GaAs	Si	Al_2O_3	FR-4
Loss Tangent (Tanδ)	0.006	0.004	0.0002	~0.01
Dielectric Constant (ε_r)	12.9	11.9	9.7	4.2
Cost	High	Low	Medium	Very Low
CTE (ppm/K)	5.7	4.6	6.3	15

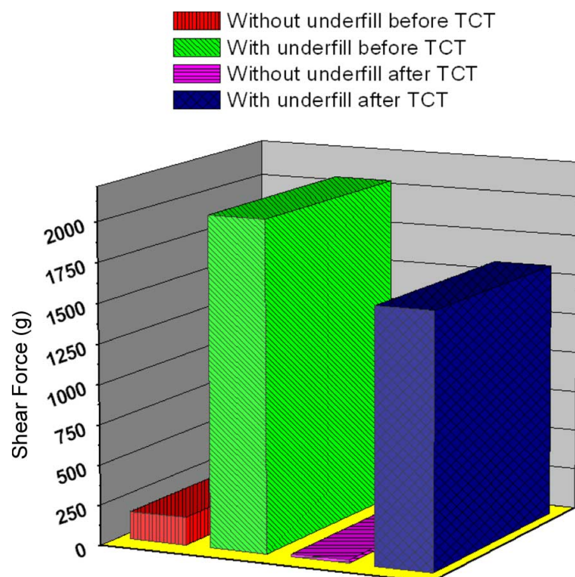


Fig. 12. Shear force test results of the flip-chip assembly.

underfill was 173 g. With the underfill application, the shear force was improved to 2052 g, which is about 12 times improvement, as compared to the samples without underfill. After 1000 thermal cycles, the shear force of the samples were 1584 g (with underfill) and 19 g (without underfill), respectively. The shear strength decayed after the thermal cycling test, especially for the samples without underfill. It is shown from these testing results that the application of the underfill has significantly improved the interconnect reliability of the flip-chip assembly.

V. CONCLUSION

In this study, the use of the epoxy-based underfill in the flip-chip interconnect is evaluated for applications from dc to 67 GHz. The matching designs on both the GaAs chip and Al_2O_3 substrate were employed with the underfill effects taken into account. The optimized structure showed excellent performance of $S11$ below -20 dB and $S21$ less than 0.6 dB from dc to 67 GHz. For the dielectric loss induced by the underfill, the extracted results indicated that the loss can be further improved by using other lower loss underfill materials. The reliability tests including the 85 $^\circ\text{C}/85\%$ RH test, thermal cycling test, and shear force test were performed. The testing results revealed that with underfill, the flip-chip assembly had low water absorption, sustainable joint fatigue life, and robust joint strength, showing its potential for commercial MMW packaging applications.

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REFERENCES

[1] A. Jentzsch and W. Heinrich, "Theory and measurements of flip-chip interconnects for frequencies up to 100 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 5, pp. 871–878, May 2001.

[2] C. L. Wang and R. B. Wu, "Modeling and design for electrical performance of wideband flip-chip transition," *IEEE Trans. Adv. Packag.*, vol. 26, no. 4, pp. 385–391, Nov. 2003.

[3] D. Staiculescu, J. Laskar, and E. M. Tentzeris, "Design rule development for microwave flip-chip applications," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 9, pp. 1476–1481, Sep. 2000.

[4] C. Karnfelt, H. Zirath, J. P. Starski, and J. Rudnicki, "Flip chip assembly of a 40–60 GHz GaAs microstrip amplifier," in *34th Eur. Microw. Conf.*, Amsterdam, The Netherlands, Oct. 11–15, 2004, pp. 89–92.

[5] W.-C. Wu, L.-H. Hsu, E. Y. Chang, C. Karnfelt, H. Zirath, J. P. Starski, and Y.-C. Wu, "60 GHz broadband MS-to-CPW hot-via flip chip interconnects," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 11, pp. 784–786, Nov. 2007.

[6] W. Wu, E. Y. Chang, C. H. Huang, L. H. Hsu, J. P. Starski, and H. Zirath, "Coaxial transitions for CPW-to-CPW flip chip interconnects," *Electron. Lett.*, vol. 43, pp. 929–930, Aug. 2007.

[7] W.-C. Wu, E. Y. Chang, R.-B. Hwang, L.-H. Hsu, C.-H. Huang, C. Karnfelt, and H. Zirath, "Design, fabrication, and characterization of novel vertical coaxial transitions for flip-chip interconnects," *IEEE Trans. Adv. Packag.*, vol. 32, no. 2, pp. 362–371, May 2009.

[8] W. C. Wu, L. H. Hsu, E. Y. Chang, J. P. Starski, and H. Zirath, "60 GHz broadband 0/1-level RF-via interconnect for RF-MEMS packaging," *Electron. Lett.*, vol. 43, no. 22, Oct. 2007.

[9] L.-H. Hsu, W.-C. Wu, E. Y. Chang, H. Zirath, Y.-C. Wu, C.-T. Wang, and C.-T. Lee, "Design and fabrication of 0/1-level RF-via interconnect for RF-MEMS packaging applications," *IEEE Trans. Adv. Packag.*, vol. 33, no. 1, pp. 30–36, Feb. 2009.

[10] K. Chai and L. Wu, "The underfill processing technologies for flip chip packaging," in *1st Int. IEEE Polymers and Adhesives in Microelectron. Photon. Conf.* , Potsdam, Germany, Oct. 2001, pp. 119–123.

[11] L. Nguyen and H. Nguyen, "Effect of underfill fillet configuration on flip chip package reliability," in *27th Annu. IEEE/SEMI Int. Electron. Manuf. Technol. Symp.*, San Jose, CA, Jul. 2002, pp. 291–303.

[12] K. H. Teo, "Reliability assessment of flip chip on board connections," in *Proc. 2nd Electron. Packag. Technol. Conf.*, Singapore, Dec. 1998, pp. 269–273.

[13] J. Sun, H. Fatima, A. Koudymov, A. Chitnis, X. Hu, H.-M. Wang, J. Zhang, G. Simin, J. Yang, and M. A. Khan, "Thermal management of AlGaN–GaN HFETs on sapphire using flip-chip bonding with epoxy underfill," *IEEE Electron Device Lett.*, vol. 24, no. 6, pp. 375–377, Jun. 2003.

[14] G. Baumann, E. Muller, F. Buchali, D. Ferling, H. Richter, and W. Heinrich, "Evaluation of glob top and underfill encapsulated active and passive structures for millimeter wave applications," in *27th Eur. Microw. Conf.*, Jerusalem, Israel, Oct. 1997, vol. 1, pp. 26–31.

[15] Z. Feng, W. Zhang, B. Su, K. C. Gupta, and Y. C. Lee, "RF and mechanical characterization of flip-chip interconnects in CPW circuits with underfill," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 12, pp. 2269–2275, Dec. 1999.

[16] H. Kusamitsu, Y. Morishita, K. Maruhasi, M. Ito, and K. Ohata, "The flip-chip bump interconnection for millimeter-wave GaAs MMIC," *IEEE Trans. Electron. Packag. Manuf.*, vol. 22, no. 1, pp. 23–28, Jan. 1999.

[17] F. J. Schmuckle, F. Lenk, M. Hutter, M. Klein, H. Oppermann, G. Engelmann, M. Topper, K. Riepe, and W. Heinrich, "W-band flip-chip VCO in thin-film environment," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Long Beach, CA, Jun. 12–17, 2005, pp. 1–4.

[18] W. C. Wu, H. T. Hsu, E. Y. Chang, C. S. Lee, C. H. Huang, Y. C. Hu, L. H. Hsu, and Y. C. Lien, "Flip-chip packaged $In_{0.52}Al_{0.48}As/InGaAs$ metamorphic HEMT device for millimeter wave application," in *Proc. CS-MAX, Compound Semiconduct. Manuf. Expo*, Palm Spring, CA, Nov. 2005, pp. 94–97.

[19] J. Capwell, T. W. D. Markell, and L. Dunleavy, "Automation and real-time verification of passive component S-parameter measurements using loss factor calculations," *Microw. J.*, vol. 47, no. 3, pp. 82–90, Mar. 2004.

Li-Han Hsu (S'08) was born in Tainan, Taiwan, in 1981. He received the B.S. and M.S. degrees in materials science and engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 2003 and 2005, respectively, and is currently working toward the dual Ph.D. degrees in materials science and engineering and microtechnology and nanoscience from National Chiao Tung University, Hsinchu, Taiwan and the Chalmers University of Technology, Göteborg, Sweden.

His main research interest is millimeter-wave packaging technology including flip-chip interconnects, hot-via interconnects, and integration of V-/E-band multichip module (MCM) transceiver modules.

Wei-Cheng Wu was born in Hsinchu, Taiwan, in 1979. He received the B.S. degree from in materials science and engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2001, and is currently working toward the dual Ph.D. degrees in materials science and engineering and microtechnology and nanoscience from National Chiao Tung University, Hsinchu, Taiwan and the Chalmers University of Technology, Göteborg, Sweden.

His research interests include fabrication, characterization, and packaging technologies of compound semiconductor devices and integrated circuits (ICs) for high-frequency applications, especially flip-chip interconnects and transition design.

Edward Yi Chang (S'85–M'85–SM'04) received the B.S. degree in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1977, and the Ph.D. degree in materials science and engineering from the University of Minnesota at Minneapolis–St. Paul, in 1985.

From 1985 to 1988, he was with the GaAs Component Group, Unisys Corporation, Eagan, MN. From 1988 to 1992, he was with the Microelectronic Group, Comsat Laboratories. In 1992, he was involved with the GaAs monolithic microwave integrated circuit (MMIC) programs for both groups. In 1992, he was with National Chiao Tung University (NCTU), Hsinchu, Taiwan. In 1994, he helped set up the first GaAs MMIC production line in Taiwan, and in 1995, he became the President of Hexawave Inc., Hsinchu, Taiwan. In 1999, he returned to NCTU, where he is currently a Professor with the Department of Materials Science and Engineering. His research interests include new device and process technologies for compound semiconductor RF integrated circuits (RFICs) for wireless communication.

Dr. Chang is a Senior Member and Distinguished Lecturer of the IEEE Electronic Devices Society.

Herbert Zirath (S'84–M'86) was born in Göteborg, Sweden, on March 20, 1955. He received the M.Sc. and Ph.D. degrees from the Chalmers University, Göteborg, Sweden, in 1980 and 1986, respectively.

He is currently a Professor of high-speed electronics with the Department of Microtechnology and Nanoscience, Chalmers University. In 2001, he became the Head of the Microwave Electronics Laboratory. He currently leads a group of approximately 30 researchers in the area of high-frequency semiconductor devices and circuits. His main research interests include InP-HEMT devices and circuits, SiC- and GaN-based transistors for high-power applications, device modeling including noise and large-signal models for field-effect transistor (FET) and bipolar devices, and foundry-related monolithic microwave ICs for millimeter-wave applications based on both III–V and silicon devices. He also works part-time with Ericsson AB, Mölndal, Sweden, as a Microwave Circuit Expert. He has authored or coauthored over 220 papers in international journals and conference proceedings and one book. He holds four patents.

Yin-Chu Hu was born in Taipei, Taiwan, in 1984. She received the B.S. and M.S. degrees in materials science and engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2005 and 2007, respectively.

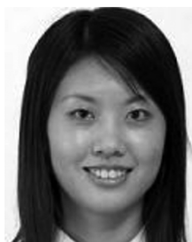
She is currently with Everlight Electronics, Taipei, Taiwan. Her major research interest is using various dielectric materials as underfill in flip-chip interconnect for millimeter-wave applications.

Chin-Te Wang was born in Taipei, Taiwan, on November 6, 1983. He received the B.S. degree in materials science and engineering from National Chung Hsing University (NCHU), Taichung, Taiwan, in 2006, and is currently working toward the M.S. and Ph.D. degrees at National Chiao Tung University (NCTU), Hsinchu, Taiwan.

While with NCHU, he was interested in electric materials. He then joined the Compound Semiconductor Device Laboratory, NCTU.

Yun-Chi Wu was born in Chiayi, Taiwan. He received the B.S. degree in materials science and engineering from Tatung University, Taipei, Taiwan, in 2001, the M.S. degree in materials science and engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 2003, and is currently working toward the Ph.D. degree in materials science and engineering at NCTU.

He is currently with the Compound Semiconductor Device Laboratory, Department of Materials Science and Engineering, NCTU. His research is focused on HEMT device and process technologies for wireless communication applications.



Szu-Ping Tsai was born in Pingtung, Taiwan on February 2, 1985. She received the B.S. degree in materials science and engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 2007, and is currently working toward the M.S. degree at NCTU.

In 2007, she joined the Compound Semiconductor Device Laboratory, NCTU, where she has been involved in the area of the flip-chip technology with a focus on aspects of finite-element thermomechanical modeling and simulation.