A Low-Power K-Band CMOS VCO With Four-Coil Transformer Feedback

Szu-Ling Liu, Kuan-Han Chen, Tsu Chang, and Albert Chin, *Senior Member, IEEE*

***Abstract*—A K-band low-power and low-phase-noise voltage-controlled oscillator (VCO) is presented in this letter. By utilizing four-coil transformer feedback and forward body bias topology, good performances are obtained under a low-power supply with a 5.1% tuning range and a phase noise of −109.8 dBc/Hz at 1 MHz offset from the 21.37-GHz carrier frequency. The core circuit of this VCO only consumes 3.5 mW with a 0.6-V supply voltage and a 0.55-V body bias.**

***Index Terms*—Forward body bias, K-band, low power, transformer feedback.**

I. Introduction

VOLTAGE-CONTROLLED oscillators (VCOs) are one of the critical building blocks in wireless receivers and transmitters. In general, low phase noise and wide tuning range are the most essential requirements; low power dissipation, ease of system integration, and low implementation costs are other important considerations for VCOs. To achieve these goals, fully integrated circuits fabricated in a standard CMOS process have become prevalent in VCO design. However, it is difficult to achieve low VCO phase noise and maintain high output carrier power while lowering the dc power supply voltage. This is due to the high flicker noise of the MOSFET and the significant loss of on-chip passive devices [1]–[4].

To improve the signal-to-noise ratio of CMOS VCOs under a low power supply, a drain-to-source transformer-feedback VCO was proposed by Kwok and Luong [5]. This circuit technique can provide a larger voltage swing under a low supply voltage. Nevertheless, the operating frequency and tunable range are usually restricted by the parasitic capacitance inside the transformer, especially for high-frequency operations.

In this letter, a new four-coil transformer-feedback VCO is presented. It not only has the advantage of drain-to-source transformer-feedback VCO, but also is suitable for 22 GHz operation. This is realized by using a transformer with a low turn-ratio to lower the parasitic capacitance, while a still large drain voltage swing can be obtained by using a buffer source coupling.

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S.-L. Liu, K.-H. Chen, and A. Chin are with the Department of Electronic Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: albert_achin@hotmail.com).

T. Chang is with the Chung-Shan Institute of Science and Technology, Taoyuan 325, Taiwan.

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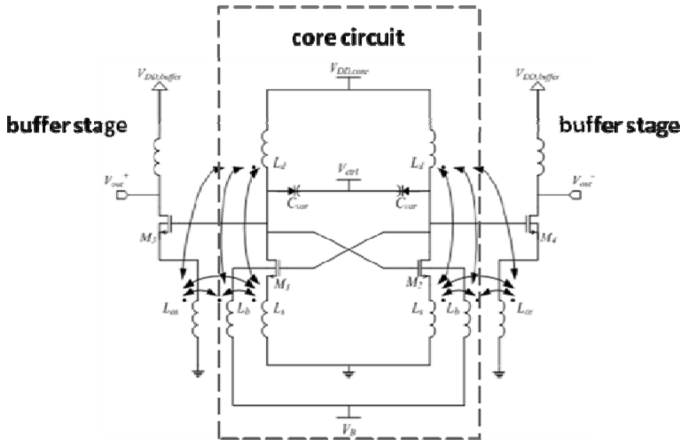

Fig. 1. Circuit schematic of the proposed cross-coupled VCO with a four-coil transformer.

A forward body bias is applied to further reduce the supply voltage, which uses an inductive body coupling to lower the body current and dynamic threshold voltage $(V_{\rm th})$ variation.

II. Circuit Design and Fabrication

The proposed VCO was implemented in standard 1 P6M 0.18 μm CMOS technology with a top metal layer of 2 μm thickness and other metal layers of 0.53 μm thickness. Fig. 1 shows the schematic of the proposed VCO. To avoid increasing the supply voltage and flicker noise, the tail-current transistor in conventional cross-coupled VCOs is not adopted. In this circuit, NMOS transistors are used with the deep n-well process to decrease the substrate noise. M_1 and M_2 transistors form a cross-coupled pair and generate negative conductance for oscillation. M_3 and M_4 are output buffer transistors. $C_{\rm var}$ is a MOS varactor for oscillation frequency tuning. $L_{\rm d}, L_{\rm s}, L_{\rm b}$, and $L_{\rm os}$ are the self-inductances of the coils connected to drain, source, and body terminals and the buffer transistor's source terminals, respectively. Here, only a transformer with a low turn-ratio is used to lower the parasitic capacitance and reach high oscillation frequency. This is in sharp contrast to the previous drain-to-source transformer [5], which required a relatively high turn-ratio between the drain and the source coils to establish a suitable impedance transformation and maintain a high quality factor of the tank. However, the multiturn spiral inductor has significant parasitic capacitance, thus limiting the maximum oscillation frequency.

To satisfy the requirements of both low parasitic capacitance and impedance transformation, a novel four-coil concentric single-turn transformer was designed for the proposed VCO, as shown in Fig. 2. The related model parameters were obtained from full-wave electromagnetic (EM) simulation by using an

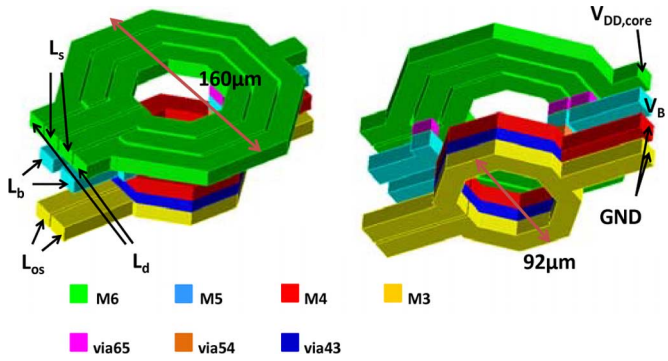

Fig. 2. Cross section of the four-coil transformer.

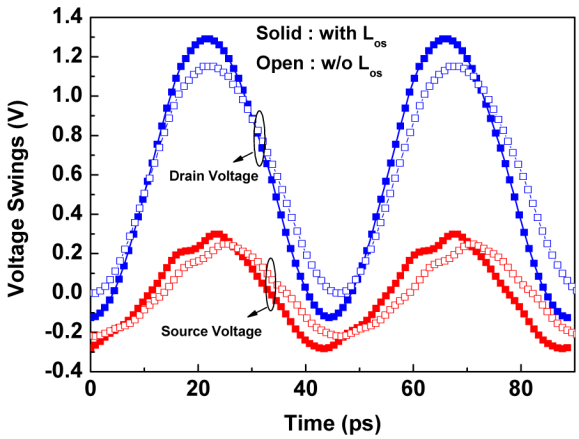

Fig. 3. Simulated waveforms of the drain voltage and the source voltage.

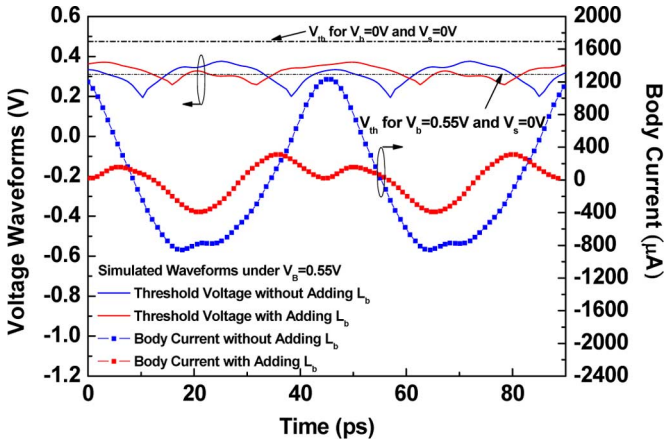

Fig. 4. Simulated waveforms of the threshold voltage and body current.

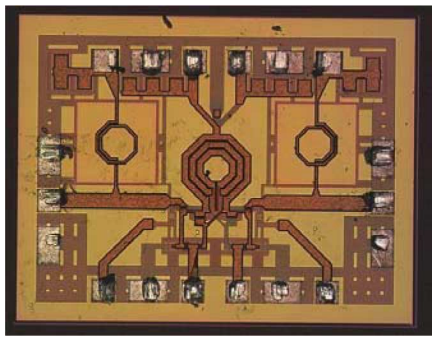

Fig. 5. Microphotograph of the proposed VCO.

Agilent ADS Momentum EM simulator. The top metal layer, metal-6 (M6), was used for $L_{\rm d}, L_{\rm b}$, and $L_{\rm s}$. To decrease the resistive loss, $L_{\rm os}$ was fabricated by stacking metal-4 and metal-3 with via connections. The simulated self-inductances for $L_{\rm d}, L_{\rm s}, L_{\rm os}$, and $L_{\rm b}$ are 0.22, 0.12, 0.13, and 0.16 nH, respectively, at 22 GHz. The quality factors for $L_{\rm d}, L_{\rm s}, L_{\rm os}$, and $L_{\rm b}$ are 13.2, 13.5, 8.5, and 8.8, respectively, at 22 GHz. Each coil in the transformer has 15 μm width and 2 μm spacing between adjacent top metal windings.

In this design, the large radius difference between $L_{\rm d}$ and $L_{\rm s}$ is utilized to replace the high turn-ratio in the drain-to-source transformer. Although this improves the parasitic capacitance issue for high-frequency VCOs, the weak coupling between $L_{\rm d}$ and $L_{\rm s}$ remains as the drawback. To improve the drain voltage swing, $L_{\rm os}$ is used to provide another in-phase voltage feedback from $V_{\rm os}$. A small radius for $L_{\rm os}$ is adopted because the source of buffer transistors is also a low-impedance node. The coupling coefficient between $L_{\rm os}$ and $L_{\rm s}$ is $\sim$0.67. Fig. 3 shows the simulated voltage swings. The voltage amplitudes are increased by the assistance of magnetic coupling from $L_{\rm os}$, which further gives $\sim$3 dB better phase noise improvement from simulation. Such performance improvement is unreachable by using a high-ohmic resistor body biasing, which results in a much degraded phase noise. As the tank is located at the drain terminal, increasing the drain voltage swing is more important to improve the phase noise.

For MOSFET, $V_{\rm th}$ is related to the source–body voltage ($V_{\rm sb}$):

$$V_{\rm th} = V_{\rm th0} + \gamma(\sqrt{|2\Phi_F + V_{\rm sb}|} - \sqrt{|2\Phi_F|}) \qquad (1)$$

where $V_{\rm th0}$ is $V_{\rm th}$ of MOSFET at $V_{\rm sb} = 0$ V. In this circuit, the $V_{\rm th0}$ of NMOS is around 0.475 V; γ and Φ_F are the physical parameters with 0.3–0.4 $V^{1/2}$ [6] and 0.3 V [7], respectively. Therefore, using the body effect can further reduce the required supply voltage of a VCO. However, applying a forward body bias in a drain-to-source transformer-feedback VCO will cause a dynamic $V_{\rm th}$ because of a dynamic $V_{\rm sb}$, which increases the nonlinear component of the output signal and degrades the signal-to-noise ratio [6]. To eliminate this effect, $L_{\rm b}$ is connected to the body with a positive body bias. Fig. 4 compares the time-varying $V_{\rm th}$ by applying a forward body bias with and without $L_{\rm b}$. When $L_{\rm b}$ is added, the time variation of $V_{\rm th}$ is remarkably alleviated, with its average value 150 mV below $V_{\rm th0}$. This is due to the feedback of $V_{\rm d}, V_{\rm s}$, and $V_{\rm os}$ to the body terminal, keeping $V_{\rm sb}$ more stationary. Since the body is at a high-impedance terminal, if the parasitic diode of MOSFETs does not turn on, it is unnecessary to reach a high turn-ratio between $L_{\rm d}$ and $L_{\rm b}$. As a result, $L_{\rm b}$ is chosen to be placed between $L_{\rm d}$ and $L_{\rm s}$. Besides, using $L_{\rm b}$ also effectively decreases the body current due to the lesser varying $V_{\rm sb}$. This is an important concern for low-power VCOs. Fig. 5 shows the micrograph of the

TABLE I
PERFORMANCE COMPARISON OF THE REPORTED K-BAND VCOS AND THIS WORK

Ref.	CMOS Tech. (μm)	Freq. (GHz)	$V_{DD,core}$ (V)	$P_{DC,core}$ (mW)	Tuning (%)	P_{out} (dBm)	Phase Noise 1 MHz Offset (dBc/Hz)	FOM* (dB)
[8]	0.18	21.3	2.4	9.6	3	-3	-105.9	-182.8
[9]	0.18	19.9	1.8	32	2.6	-3	-111	-182
[10]	0.18	24.5	1.7	1.7	16.8	-12	-95.46	-180.2
[11]	0.13	23	1	4	2	-25	-100	-181
				10	1.5	-20	-109.5	-187
This work	**0.18**	**21.37**	**0.6**	**3.5**	**5.1**	**-8.56**	**-109.8**	**-190.9**

* $\text{FOM} = 10\log_{10}[(\frac{f_o}{\Delta f})^2 \cdot \frac{1}{\text{L}\{\Delta f\} \cdot \text{P}_{dc}})]$

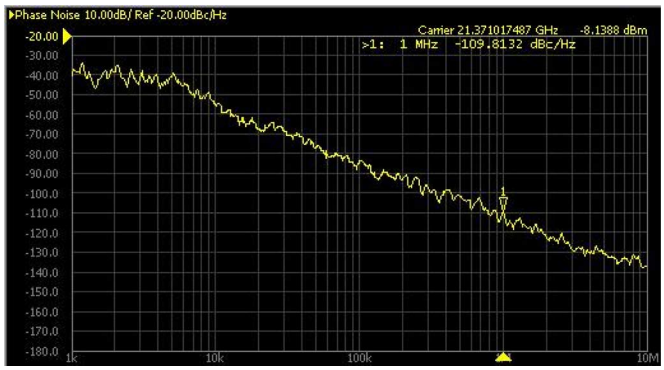

Fig. 6. Measured phase noise of the fabricated VCO at 21.37 GHz with respect to a 1-MHz offset.

fabricated VCO; the chip size is 795×595 μm^2, including the buffer stages and pads. The size of the core VCO circuit is only 260×345 μm^2.

III. MEASUREMENT RESULTS

The characterization of the circuit performance was carried out by on-wafer probing. The output spectrum and phase noise were measured using an Agilent E5052 system and an Agilent N5507A microwave down converter. The circuit is biased at $V_{\text{DD,core}} = 0.6$ V, $V_{\text{B}} = 0.55$ V, and $V_{\text{DD,buffer}} = 1.8$ V, while the core circuit and the buffer stages consume dc power of 3.5 and 3.8 mW, respectively. The oscillation frequency is from 21.33 to 22.44 GHz with a 5.1% tuning range. The average output power is -8.56 dBm in the operating frequency range. The measured phase noise of this VCO as shown in Fig. 6 is -109.8 dBc/Hz at a 1-MHz offset from the 21.37-GHz oscillation frequency. The variation of measured phase noise is comparable with other published data in literature [8]. Table I summarizes the circuit characteristics and compares them to the reported CMOS K-band VCOs [9]–[12]. The figure of merit (FOM) of the fabricated VCO is -190.9 dBc/Hz, which is comparable to the best reported K-band CMOS VCOs.

IV. CONCLUSION

The novel four-coil transformer VCO successfully combines the merits of drain-to-source transformer-feedback VCO and a forward body bias technique. The time variation of V_{th} is also minimized. Under the requirements of both low-power and high-frequency operation ($\sim$22 GHz), the performance of this VCO compares well with the reported state-of-the-art K-band CMOS VCO, with a core VCO area of only 260×345 μm^2.

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REFERENCES

[1] K. T. Chan, C. H. Huang, A. Chin, M. F. Li, D. L. Kwong, S. P. McAlister, D. S. Duh, and W. J. Lin, "Large Q-factor improvement for spiral inductors on silicon using proton implantation," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 11, pp. 460–462, Nov. 2003.

[2] K. T. Chan, A. Chin, M. F. Li, D. L. Kwong, S. P. McAlister, D. S. Duh, W. J. Lin, and C. Y. Chang, "High performance microwave coplanar band-pass and band-stop filters on Si substrates," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 9, pp. 2036–2040, Sep. 2003.

[3] K. T. Chan, A. Chin, Y. D. Lin, C. Y. Chang, C. X. Zhu, M. F. Li, D. L. Kwong, S. McAlister, D. S. Duh, and W. J. Lin, "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," *Microw. Wireless Compon. Lett.*, vol. 13, no. 11, pp. 487–489, Nov. 2003.

[4] A. Chin, K. T. Chan, H. C. Huang, C. Chen, V. Liang, J. K. Chen, S. C. Chien, S. W. Sun, D. S. Duh, W. J. Lin, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "RF passive devices on Si with excellent performance close to ideal devices designed by electro-magnetic simulation," in *IEDM Tech. Dig.*, 2003, pp. 375–378.

[5] K. Kwok and H. C. Luong, "Ultra-low-voltage high-performance CMOS VCOs using transformer-feedback," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 652–660, Mar. 2005.

[6] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

[7] H. H. Hsieh and L. H. Lu, "A high-performance CMOS voltage-controlled oscillator for ultra-low-voltage operations," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 3, pp. 467–473, Mar. 2007.

[8] M. D. Wei, S. F. Chang, and Y. J. Yang, "A CMOS backgate-coupled QVCO based on back-to-back series varactor configuration for minimal AM-to-PM noise conversion," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 5, pp. 320–322, May 2009.

[9] C. C. Li, T. P. Wang, C. C. Kuo, M. C. Chuang, and H. Wang, "A 21 GHz complementary transformer coupled CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 4, pp. 278–280, Apr. 2008.

[10] H. H. Hsieh and L. H. Lu, "A low-phase-noise K-band CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 10, pp. 552–554, Oct. 2006.

[11] Y. H. Kuo, J. H. Tsai, and T. W. Huang, "A 1.7-mW, 16.8% frequency tuning, 24-GHz transformer-based in LC-VCO using 0.18-μ CMOS technology," in *Proc. IEEE RFIC Symp.*, Jun. 2009, pp. 79–82.

[12] C. K. Hsieh, K. Y. Kao, J. R. Tseng, and K. Y. Lin, "A K-band CMOS low power modified colpitts VCO using transformer feedback," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 1293–1296.