A Physical Model for the Correlation Between Holding Voltage and Holding Current in Epitaxial CMOS Latch-Up

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***Abstract*—A new physical model concerning the holding points for latch-up in epitaxial CMOS structures is established by combining the lateral p-i-n high level injection and the vertical BJT base push-out formula. The model matches adequately the correlation between holding voltage and holding current extensively measured from different combinations of temperatures, epitaxial layer thicknesses, and anode-to-cathode spacings. This is also the case for the two-dimensional device simulations. A quantitative analysis based on the model consistently judges the crucial role of the vertical BJT base push-out width in producing the observed correlation. The potential merits of the model in extended applications are outlined.**

I. Introduction

BASED on three different fabrication processes [1]–[3] for the epitaxial CMOS latch-up structures, Sleeter and Enlow [1] reported a new finding of a correlation between holding voltage and holding current. One interested in this correlation may raise the following questions: Does a correlation between holding voltage and holding current exist for other processes and over temperatures? What is the underlying physics? What are the implications? and What additional applications are suggested? On the other hand, a novel physically-based analytical model for the latch-up holding voltage was developed by Seitchik *et al.* [4]. In this letter, we establish a new linking between the work [1] and [4], and attempt to answer the above questions.

II. Physical Model

The lateral p-i-n diode high level injection and the vertical BJT base push-out formula as cited in [4] for epitaxial CMOS latch-up have been separately modified adequately for the holding point case [5]

$$I_H = q(\mu_n + \mu_p)\,\frac{\eta P_0}{2}\,[V_H - 1V]\,\frac{hW}{L} + I_{\rm sub} \tag{1}$$

$$h = \frac{t_{\rm epi}}{1 + \dfrac{N_{\rm epi}(V_H/2)}{\eta P_o(kT/q)}} \tag{2}$$

where V_H and I_H are the holding voltage and holding current, respectively; μ_n and μ_p are the electron and hole mobilities, respectively; $\eta (= 0.7$ throughout the work$)$ is the calibration factor accounting for the nonuniform nature of the vertical carrier density distribution at the mid-point between anode and cathode; P_o is the surface carrier density evaluated at the mid-point; h is the vertical BJT base push-out width at the mid-point; W is the device width; L is the anode-to-cathode spacing; $I_{\rm sub}$ is part of the I_H that does not traverse the whole i-region; $t_{\rm epi}$ is the epitaxial layer thickness; and $N_{\rm epi}$ is the dopant concentration of the low-doped epitaxial layer. By combining both equations with the common factor P_o eliminated, we obtain

$$V_H = \frac{1}{2}\,V + \frac{1}{2}\,\sqrt{1V^2 + 4\alpha^2\beta(I_H - I_{\rm sub})} \tag{3}$$

$$\alpha = \sqrt{\frac{4kT/q}{q(\mu_n + \mu_p)N_{\rm epi}W}} \tag{4}$$

$$\beta = \frac{L}{h}\left(\frac{t_{\rm epi}}{h} - 1\right). \tag{5}$$

Obviously, (3) can serve as a physical model for the correlation between V_H and I_H: for $I_H \gg I_{\rm sub}$ the V_H follows the square root of I_H, as originally observed in [1].

III. Experimental and Simulation Evidence

A large variety of latch-up stripe-type structures formed on a p-type epitaxial layer/p$^+$ substrate, having two different epitaxial layer thicknesses and four different anode-to-cathode spacings, were fabricated by a 0.35-μm CMOS process. Each of the structures had the same device width $W = 30$ μm. The measured doping profiles are given in [5]. By means of the three different measurement methods [5], a large amount of the latch-up $I-V$ characteristics were produced in a wide temperature range of 27–250 °C. The holding points obtained from these $I-V$ characteristics are depicted in Fig. 1 in terms of the scatter plot of holding voltage versus holding current. By fitting (3) to the data points in Fig. 1, the $\alpha^2\beta$ and $I_{\rm sub}$ were simultaneously extracted to be 0.1264 V^2/mA and 10.02 mA, respectively. From Fig. 1 we can observe that almost all the

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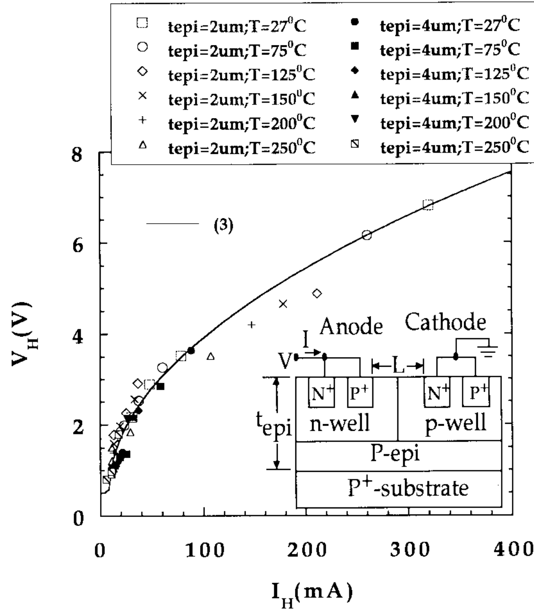

Fig. 1. The scatter plot of the measured holding voltages and currents (symbols) from two different effective epitaxial layer thicknesses of 2 and 4 μm, four different anode-to-cathode spacings of 1.6, 2.0, 2.4, and 5 μm, and six different temperatures of 27, 75, 125, 150, 200, and 250 °C. A curve from (3) is together plotted. The inset schematically shows the cross section of the latch-up stripe-type structures in a 0.35-μm process.

holding points fall on or around the same curve provided by (3).

On the other hand, a two-dimensional device simulation using MEDICI was performed on the latch-up structures with the epitaxial layer thickness, the anode-to-cathode spacing, and the temperature, all as input parameters. The process parameters and the physical models were kept the same for each simulations [5]. The holding voltage and holding current obtained from all the simulated $I-V$ characteristics are together compared in a scatter plot as shown in Fig. 2. Reproduction of the simulation data points in Fig. 2 by (3) leads to $\alpha^2\beta = 18.43$ V^2/mA and $I_{\rm sub} = 0.62$ mA for $W = 1$ μm.

The presence of the above experimental and MEDICI data as well as those from the other processes [5] indeed proves the existence of the correlation between V_H and I_H, and this correlation is essentially independent of temperature, epitaxial layer thickness, and anode-to-cathode spacing. It is specially noteworthy that the extracted $\alpha^2\beta$ in Fig. 2 is different from that in Fig. 1. Such difference can be attributed to the different W and different $N_{\rm epi}$ used in the model. For the latter, as schematically shown in the inset of Figs. 1 and 2, $N_{\rm epi} = 1 \times 10^{15}$ cm^{-3} in simulation structures while in 0.35-μm process the p-well was formed on the p-epi layer, thus effectively increasing the value of $N_{\rm epi}$. Then according to (4) the value of $\alpha^2\beta$ in 0.35 μm process is greatly lowered as compared with the simulation case.

IV. Quantitative Analysis and Discussion

To explain why in the above work the factor $\alpha^2\beta$ can be regarded as a constant, a quantitative analysis was performed

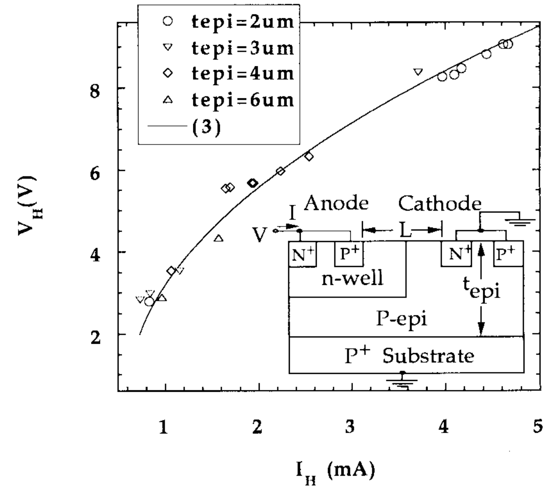

Fig. 2. The scatter plot of the simulated holding voltages and currents (symbols) for four different epitaxial layer thicknesses of 2, 3, 4, and 6 μm, four different anode-to-cathode spacings of 4, 6, 8, and 10 μm, and five different temperatures of 27, 75, 150, 200, and 250 °C. A curve from (3) is together plotted. The inset schematically shows the cross section of the latch-up simulation structures.

TABLE I
The Four Different Structures and the Corresponding Simulated Values of V_H, I_H, P_o, and h

t_{epi}(um)	L(um)	V_H(V)	I_H(mA)	P_o(cm^{-3})	h*(um)	h**(um)
4	10	6.3	2.50	2.0×10^{17}	2.04	2.23
4	8	3.5	1.06	9.7×10^{16}	1.92	2.14
2	6	9.0	4.67	4.0×10^{17}	1.01	1.02
2	4	2.8	0.83	8.4×10^{16}	0.92	0.94

* the location of the carrier density equal to 10 N_{epi}
** the width of the flat portion of the potential profile

on the simulation structures. The results are presented in Table I that lists the simulated h values for $t_{\rm epi} = 4$ μm with two different L of 8 and 10 μm as well as for $t_{\rm epi} = 2$ μm with two different L of 4 and 6 μm. The simulation results show that an increase in $t_{\rm epi}$ is followed by an increase in h. One of the plausible interpretations is that the corresponding decreased holding voltage or equivalently the decreased collector to base voltage for a vertical BJT predominantly gives rise to an increase in the base push-out width [6]. To provide better insights, we rewrite (5) to

$$h = \frac{L(-1 + \sqrt{1 + (4\beta t_{\rm epi}/L)})}{2\beta}. \quad (6)$$

Equation (6) transparently describes the effects of changing $t_{\rm epi}$ or L on h for a given β. The calculated h values using (6) corresponding to Table I are listed in Table II. In Table II, we also list the calculated h from (2) directly using the simulated P_o and V_H listed in Table I both as input parameters. From Table II, we can observe that all the calculated values of h

TABLE II
THE FOUR DIFFERENT STRUCTURES AND THE CORRESPONDING CALCULATED VALUES OF h AND I_H. IN CALCULATION, $\alpha = 2.08$ V/mA$^{1/2}$ AND $\beta = 4.25$ FOR $\mu_n = 1000$ cm^2/V · S, $\mu_p = 500$ cm^2/V · S, $N_{\text{epi}} = 1 \times 10^{15}$ cm^{-3}, $W = 1$ μm, AND $kT/q = 0.02586$ V

t_{epi}(um)	L (um)	h*(um)	h**(um)	I_H***(mA)
4	10	2.11	2.13	2.53
4	8	1.96	2.00	0.78
2	6	1.12	1.24	7.06
2	4	0.98	1.05	0.69

* from (6)

** from (2) with P_o, and V_H from Table I

*** from (1) with P_o, V_H, and h from Table I

from two different sources (2) and (6) are not only close to each other, but also to the simulated values in Table I. The corresponding I_H values are also given in both tables, from which the calculated I_H by (1) using the simulated P_o and V_H as input parameters appears to be comparable with the simulated ones. The above self-consistent analysis thus judges the vertical BJT base push-out width as the cause of the observed correlation.

The potential merits of the model in extended applications have been in part demonstrated elsewhere [5] in terms of a scaling law for the holding voltage [7] as well as a guideline projected for the low voltage CMOS integrated circuits. Another application is creation of a new physically-based analytical model for high-temperature latch-up, which significantly advances the work of [4] and [5] in this area and will be reported in the future.

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