Back-Gate Bias Enhanced Band-to-Band Tunneling Leakage in Scaled MOSFET's

Ming-Jer Chen, *Member, IEEE*, Huan-Tsung Huang, Chin-Shan Hou, *Member, IEEE*, and Kuo-Nan Yang

Abstract— **The drain leakage current in MOSFET's in the present standard process is separated into three distinct components: the subthreshold conduction, the surface band-to-band tunneling (BTBT), and the bulk BTBT. Each of the three shows different dependencies on back-gate bias. As a result, the bulk BTBT, increasing exponentially with increasing the magnitude of back-gate reverse bias, promptly dominates the drain leakage. Additional experiment highlights the effect of the increased bulk dopant concentrations as in next-generation scaled MOSFET's on the bulk BTBT. This sets the bulk BTBT a significant constraint to the low-voltage, low-power, high-density CMOS integrated circuits employing the back-gate reverse bias. In the work, the measured drain leakage of interest is successfully reproduced by two-dimensional (2-D) device simulation.**

I. Introduction

The leakage in the drain is a big problem for scaling the MOSFET's toward the deep submicrometer regime. The reasons are that 1) the subthreshold conduction increases exponentially due to threshold voltage reduction [1], [2]; 2) the surface band-to-band tunneling (BTBT) or gate-induced drain leakage (GIDL), increases exponentially due to reduced gate oxide thickness [3]–[5]; and 3) the bulk BTBT increases exponentially due to increased high doping bulk or pocket concentrations [1], [2]. On the other hand, in the CMOS integrated circuits such as DRAM's, the back-gate reverse bias or substrate bias has been widely utilized with the following advantages created: suppressing subthreshold leakage, lowering parasitic junction capacitances, increasing immunity against latch-up or parasitic bipolar, etc. Without considering the GIDL and the back-gate bias, the other two leakage components for next-generation scaled MOSFET's have been projected by Mead [1], pointing to the dominance by subthreshold leakage in the scaling direction down to 0.01-μm feature size.

In this letter, we demonstrate experimentally that the back-gate reverse bias can significantly enhance the bulk BTBT to the level over the GIDL and the subthreshold conduction, and this situation is more serious in the scaling direction.

Manuscript received September 29, 1997; revised October 20, 1997. This work was supported by the National Science Council under Contract NSC 86-2215-E-009-029.

M.-J. Chen, H.-T. Huang, and K.-N. Yang are with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

C.-S. Hou is with the Logic Technology R&D Department, Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C.

Publisher Item Identifier S 0741-3106(98)02628-7.

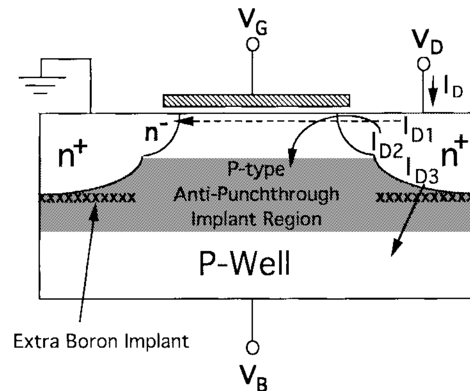

Fig. 1. The schematic cross section of the MOSFET structures under study. The current labeled I_{D1} is the subthreshold conduction, the I_{D2} is the surface BTBT in the gate-to-drain overlap region, and the I_{D3} is the bulk BTBT through the high doping anti-punchthrough region as well as the extra Boron implant region marked by "×".

II. Separation and Analysis

The n-channel LDD MOSFET's under test were fabricated in the present standard CMOS process. In this process, Boron (3.0×10^{12} cm^{-2}, 120 KeV) and then Boron (9.0×10^{12} cm^{-2}, 90 KeV) were implanted to control the punchthrough. The gate width to length ratio was 20 μm/0.35 μm and the gate oxide thickness was 70 Å. Phosphorus (6.0×10^{12} cm^{-2}, 30 KeV) and then Arsenic (4.0×10^{13} cm^{-2}, 45 KeV) were implanted to form the low-doped source/drain and Arsenic (4.4×10^{15} cm^{-2}, 40 KeV) was implanted to form the highly-doped n$^+$ source/drain. The simulated doping profile using SUPREM-IV showed that 1) the peak dopant concentration is 1×10^{18} cm^{-3} in the gate-to-drain overlap region and 2) the anti-punchthrough implant region, having the peak dopant concentrations of 5×10^{17} cm^{-3}, is formed at the bottom junction of the n$^+$ region. The cross section of the structures under study is schematically shown in Fig. 1.

The measured drain current versus gate voltage with back-gate reverse bias as a parameter is shown in Fig. 2 for drain voltage V_D fixed at 3 V and source being grounded. This figure reveals that the drain current for reverse back-gate bias can be separated into two distinct components: one exponentially follows the gate voltage, which is a measure of subthreshold conduction, and another is not affected by gate voltage. The latter component quite matches the measured bulk (p-well) current (not shown here). Thus, the subthreshold component flows from drain to source while the bulk component from

0741–3106/98$10.00 © 1998 IEEE

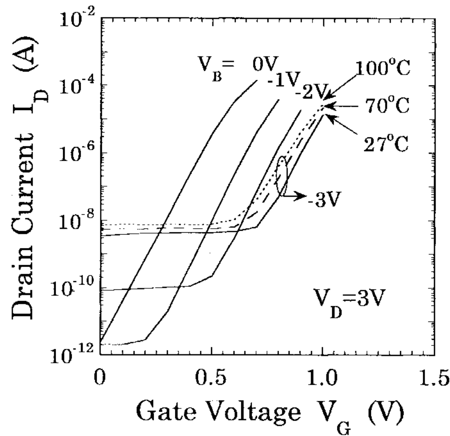

Fig. 2. The measured drain current versus gate voltage with back-gate bias as a parameter for drain voltage fixed at 3 V and source being grounded. The temperature dependent drain current is also shown for back-gate bias of −3 V.

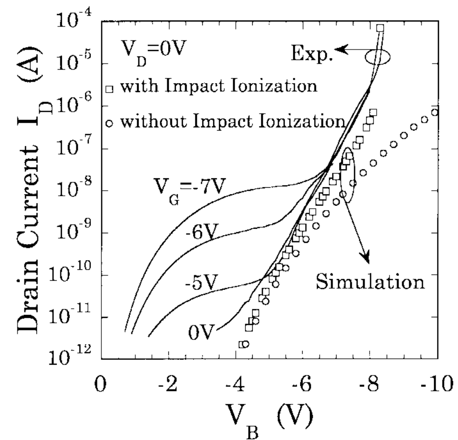

Fig. 3. The measured drain current versus back-gate bias with gate voltage as a parameter for grounded drain and open source. Also plotted are the simulated results. In simulation, the BTBT rate $G = \alpha(E^2/Eg^{0.5})\exp(-\beta Eg^{1.5}/E)$ where $\alpha = 5 \times 10^{20}$ $\mathrm{eV}^{0.5}/\mathrm{cm\ s\ V}^2$; $\beta = 20$ MV/cm $\mathrm{eV}^{1.5}$; Eg is the energy bandgap; and E is the electric field strength. The values of the BTBT and impact ionization physical parameters are close to those in the literature. The n^+ drain area $= 20 \times 20$ $\mu\mathrm{m}^2$. The simulated peak surface electric field strength in the gate-to-drain overlap region and the simulated peak bulk electric field strength at $V_D - V_G = V_D - V_B = 7$ V are 1.0 and 0.92 MV/cm, respectively.

drain to bulk. From Fig. 2 we can observe that increasing the magnitude of back-gate reverse bias V_B can substantially lower the subthreshold conduction, as expected due to the body effect; however, the bulk component is increased exponentially and promptly dominates the drain leakage at $V_G = 0$ V for $V_B < -1$ V. Also plotted in Fig. 2 are the measured temperature dependencies, showing a small, positive temperature coefficient in the bulk component. This suggests the BTBT as the origin of the bulk component. Indeed, Fig. 2 removes the possibilities of the surface BTBT or GIDL that is essentially independent of back-gate bias [3]–[6]. Thus, the bulk BTBT flows through the high doping anti-punchthrough implant region, which is far away from the surface modulation region as schematically shown in Fig. 1. Again, the simultaneously measured gate current is found to be only the measurement noise, and thereby has no contribution to the drain leakage.

The surface and bulk BTBT components were separated in a gated diode configuration with $V_D = 0$ as shown in Fig. 3, where the curve of zero gate voltage stands for the bulk BTBT while the remaining the surface BTBT. From Fig. 3, two observations of concern can be drawn. First, at the critical points $V_D - V_B \cong V_D - V_G$ the bulk BTBT is about equal to the surface BTBT. Second, an increase in the drain to substrate bias over the drain to gate bias can render the bulk BTBT dominate the leakage. Thus, in the conventional CMOS integrated circuits ($V_B = 0$ V) in the same fabrication process, the surface and bulk BTBT components at a given supply V_D contribute almost equally to the standby drain leakage at $V_G = 0$ V. However, for the case of reverse back-gate bias such as DRAM's, the bulk BTBT dominates over the surface BTBT.

A two-dimensional (2-D) device simulation program MEDICI was further performed with the simulated doping profiles as input parameters. First considering only the BTBT generation, the simulation results shown in Fig. 3 exhibit a large discrepancy in the large $|V_B|$ region for $V_G = 0$ V. This deviation is due to an amplification by impact ionization. Second simulation taking into account impact ionization considerably improves the reproduction quality as shown in Fig. 3. The simulated current flowlines (not shown here)

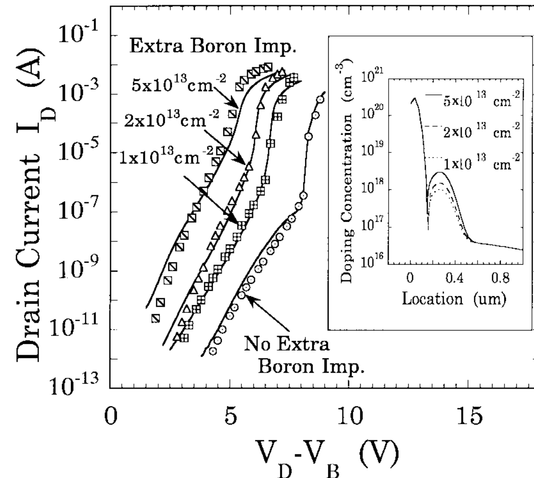

Fig. 4. The measured (lines) and simulated (symbols) bulk BTBT current versus the drain to back-gate voltage with the extra Boron implant dosage as a parameter. The inset shows the corresponding simulated vertical doping profiles from the surface of the n^+ drain. The n^+ drain area $= 100 \times 20$ $\mu\mathrm{m}^2$. The $V_D - V_B$ values needed for 1 nA leakage level are 6.2 V for no extra Boron implant and 4.4, 3.9, and 2.6 V for extra Boron implant dosages of $1 \times 10^{13}, 2 \times 10^{13}$, and 5×10^{13} cm^{-2}, respectively. The corresponding simulated peak electric field strengths are almost equal to 0.8 MV/cm.

have judged that the area component rather than the edge component is responsible for the observed bulk BTBT.

III. Additional Experiment

To reflect the influences of the increased bulk dopant concentrations in next-generation scaled MOSFET's on the bulk BTBT, the other test structures were fabricated by the same process with and without the extra Boron implant. The extra Boron species immediately following the n^+ source/drain implant were through the same window and a local higher doping p^+ region was formed at the bottom junction of the n^+ region as schematically shown in Fig. 1. Three different

dosages of $1 \times 10^{13}, 2 \times 10^{13}$, and 5×10^{13} cm^{-2} were used, all having the same implant energy of 55 KeV. The corresponding peak dopant concentrations from SUPREM-IV were $1 \times 10^{18}, 1.5 \times 10^{18}$, and 3×10^{18} cm^{-3}, respectively. The simulated vertical doping profiles are given in the inset of Fig. 4. The measured bulk BTBT leakage versus drain to back-gate voltage characteristics with the extra Boron implant dosage as a parameter are shown in Fig. 4. Apparently, the increased local bulk dopant concentrations can produce an exponential increase in the bulk BTBT and, overall, push the $I-V$ curves to the low-voltage regime. Thus, in projecting the low-voltage, low-power, high-density CMOS integrated circuits along the MOSFET scaling direction, the impact of the bulk BTBT must be taken into account especially when the back-gate reverse bias is applied. The 2-D device simulation results using MEDICI with the same BTBT and impact ionization physical parameter values as in Fig. 3 are together plotted in Fig. 4 for comparison. The corresponding $V_D - V_B$ values and peak bulk electric field strengths at a specified leakage level of 1 nA are given in the caption to provide relevant tunneling information in the scaling direction.

IV. Conclusion

The back-gate reverse bias has many potential advantages in the CMOS integrated circuits; however, we demonstrate that it can significantly enhance the bulk BTBT leakage to the level over the surface BTBT and the subthreshold conduction, and this situation is more serious in the scaling direction. The large bulk BTBT can deteriorate the circuit performance in terms of decreased retention time in dynamic logic and memory, heavy loading of substrate bias generators, large stand-by power, etc. Thus, to preserve the original merits of the back-gate reverse bias, a trade-off in the device structure parameters and/or a novel circuit technique each must be carefully engineered aiming to control the bulk BTBT.

References

[1] C. A. Mead, “Scaling of MOS technology to submicrometer feature sizes,” *J. VLSI Signal Processing*, vol. 8, pp. 9–25, 1994.

[2] Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S. H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H. J.C. Wann, S. J. Wind, and H. S. Wong, “CMOS scaling into the nanometer regime,” *Proc. IEEE*, vol. 85, pp. 486–504, 1997.

[3] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, “Subbreakdown drain leakage current in MOSFET,” *IEEE Electron Device Lett.*, vol. EDL-8, pp. 515–517, 1987.

[4] C. Chang and J. Lien, “Corner-field induced drain leakage in thin oxide MOSFET’s,” in *IEDM Tech. Dig.*, 1987, pp. 714–717.

[5] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, “The impact of gate-induced drain leakage current on MOSFET scaling,” in *IEDM Tech. Dig.*, 1987, pp. 718–721.

[6] M. J. Chen, “Effect of back-gate bias on tunneling leakage in a gated p^+-n diode,” *IEEE Electron Device Lett.*, vol. 12, pp. 249–251, 1991.