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Nickel silicide nanocrystals embedded in SiO_2 and HfO_2 for nonvolatile memory application

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Abstract

In this study, a nonvolatile memory device with $NiSi_2$ nanocrystals embedded in the SiO_2 and HfO_2 layer has been fabricated. A significant memory effect is observed during the characterization of the electrical properties. When a low operating voltage, 4 V, is applied, a significant threshold voltage shift of 1.3 V, is observed. The processing of this structure is compatible with the current manufacturing technology of semiconductor industry.
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Keywords: Nonvolatile memory; Nanocrystals; HfO_2

1. Introduction

In 1967, D. Kahng and S. M. Sze invented the first floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [1]. Nonvolatile memory devices with a floating-gate (FG) structure are used widely in applications such as mp3 players, digital cameras and IC cards at present. Conventional floating-gate (FG) devices have their limitations even though they are a huge commercial success. The most prominent disadvantage is the limited potential for continued scaling of the device structure. When the tunnel oxide is thinner, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. There is, therefore, a tradeoff between speed and reliability. The thickness of the tunnel oxide is about 8–11 nm, which is a compromise and which has changed little over more than five successive generations of the industry [2]. Recently, memory-cell structure using discrete traps as the charge storage media has received much attention as the promising candidate to replace conventional dynamic random access memory or flash memories for future high speed and low power consuming memory devices [3,4]. Nanocrystals memory devices employing distributed nanodots as storage elements have exhibited great potential in device applications [5–11]. Among the different materials of nanocrystals, the metal nanocrystals memory possesses several advantages, such as stronger coupling with the conduction channel, a wide range of available work functions, higher density of states around the Fermi level, and smaller energy perturbation due to carrier confinement [4]. Besides, using the high-k dielectric as the blocking oxide concentrates and releases the electric fields across the tunnel oxide and the blocking oxide, respectively, under the program/erase mode. Using a high-k dielectric as the blocking oxide leads to lower program and erase voltage [12].

2. Experiment

(100) oriented p-type silicon wafers were chemically cleaned by a standard Radio Corporation of America cleaning, followed

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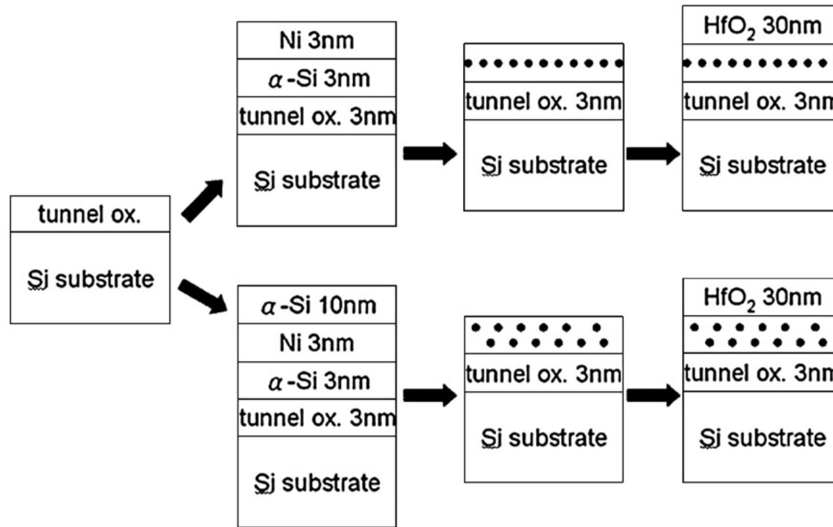

Fig. 1. The process flow of nickel silicide nanocrystals.

by formation of a 3-nm tunnel oxide layer which was thermally grown at 1000 °C in a vertical furnace system. Subsequently, a 3-nm amorphous silicon layer and a 3-nm-thick nickel layer were deposited onto the tunnel oxide by electron beam evaporation, respectively. In addition, a 10-nm amorphous silicon layer was deposited on some of the samples. Oxidation at 800 °C, 700 °C and 600 °C was performed at 5 min, 10 min and 10 min respectively to form nickel silicide nanocrystals. The 30-nm-thickness blocking oxide (HfO_2) layer was deposited by sputtering. Finally, an Al gate electrode was patterned and sintered. Fig. 1 presents the process flow. The structural analyses were performed by transmission electron microscopy (TEM). The capacitance–voltage (*C*–*V*) measurements were performed by a precision LCR meter HP 4284A to study the electron charging and discharging effects of the nickel silicide nanocrystals.

3. Results and discussion

Fig. 2 shows the forward and reverse sweep *C*–*V* characteristics, indicating the electron charging and discharging effects of nickel silicide nanocrystals embedded between the SiO_2 and HfO_2 layers. The bidirectional *C*–*V* sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited an electron charging effect. In Fig. 2, with the voltage swept from 8 to −8 V and back to 8 V, an outstanding threshold voltage shift of 0.7 V was observed. As

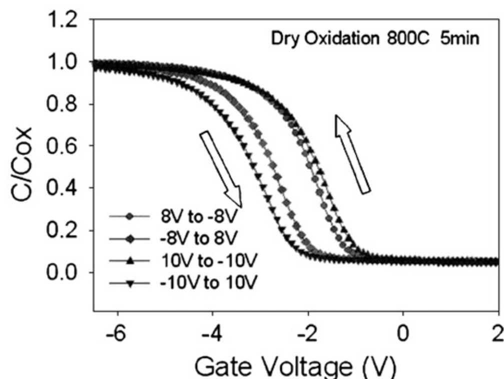

Fig. 2. The capacitance–voltage (*C*–*V*) hysteresis of nickel silicide nanocrystals memory device after bidirectional sweeps between 8 V/(−8 V) and 10 V/(−10 V).

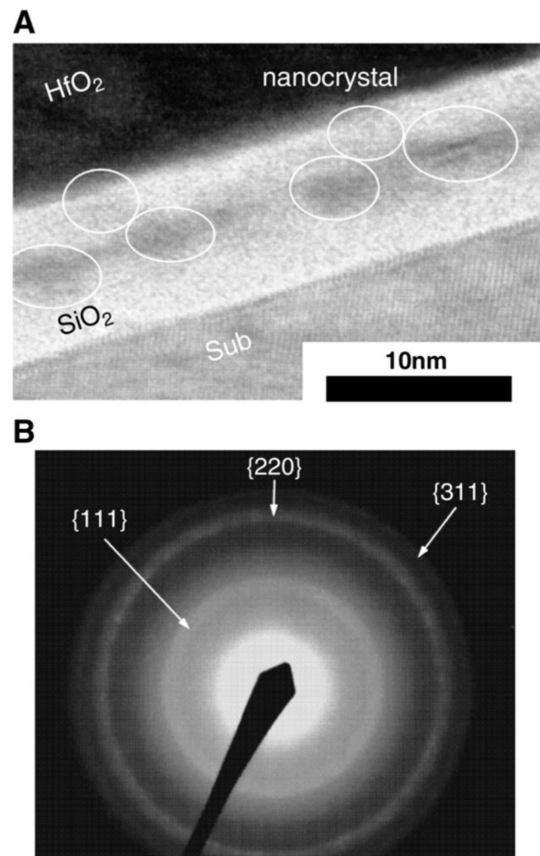

Fig. 3. (A)The cross-section TEM micrographs of an HfO_2/nickel silicide/SiO_2/Si stacked structure, and (B) The electron diffraction pattern corresponding to nickel silicide nanocrystals.

the whisked voltage was increased to 10 V, a more obvious *C–V* shift of 1.3 V was seen. It is perceived that the hysteresis is counterclockwise which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate. The resulting *C–V* shift indicates that the charging effects of nickel silicide nanocrystals are more significant than that seen for semiconductor nanocrystals. The high-k blocking oxide concentrates the electric fields across the tunnel oxide and releases it across the blocking oxide under program and erase mode. This effect leads to lower program and erase voltage. When the device is written or programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the nickel silicide nanocrystals. On the other hand, as the device is erased, the electrons may tunnel back to the deep accumulation layer of the Si substrate. The blocking oxide is utilized to prevent the carriers from the gate electrode from being injected directly into the nickel silicide nanocrystals by Fowler–Nordheim tunneling. In addition, the nickel silicide nanocrystals do not exhibit a voltage drop from the gate voltage, which means all the voltages provided from control gate are dropped to tunnel oxide and control oxide and this provides an advantage over their semiconductor counterparts. Fig. 3(A) presents the cross-section TEM micrographs of an HfO_2/nickel silicide/SiO_2/Si stacked structure with dry oxidation at 600 °C. As illustrated in Fig. 3(A), well-separated and spherical nickel silicide nanocrystals were observed between the SiO_2 layer and HfO_2 layers. The nanocrystals were identified to be a $NiSi_2$ phase through analysis

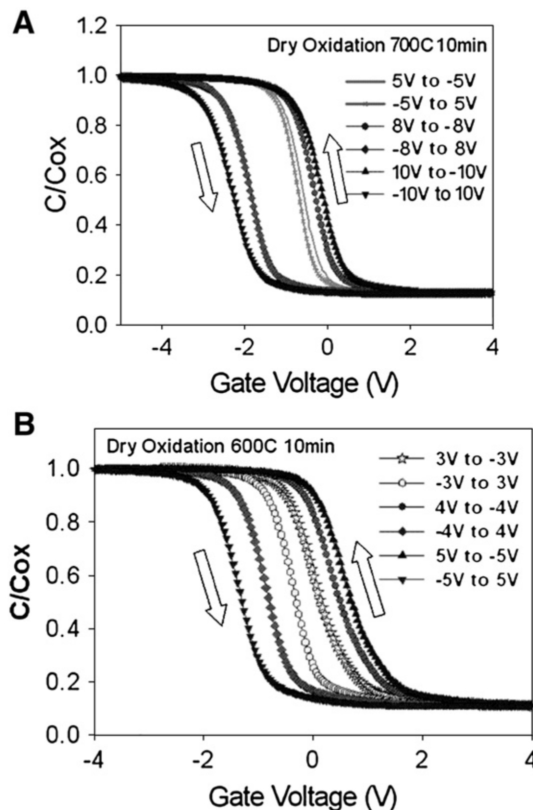

Fig. 4. The capacitance–voltage (*C–V*) hysteresis of sample with α-Si/Ni/α-Si structure after dry oxidation at (A) 700 °C, and (B) 600 °C.

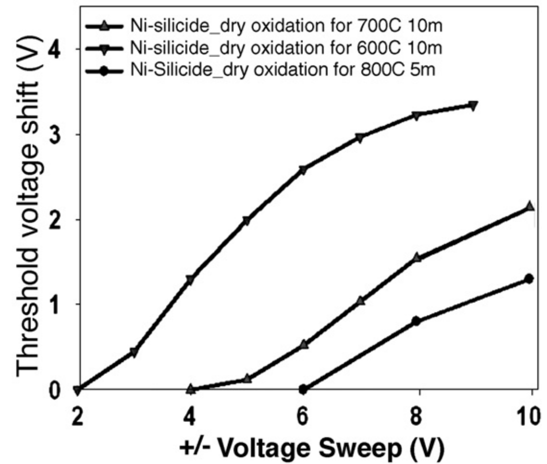

Fig. 5. The memory window vs. (program/erase) voltage of nickel silicide nanocrystal memory.

of the diffraction ring pattern shown in Fig. 3(B). Fig. 4(A) shows the capacitance–voltage (*C–V*) hysteresis of sample with α-Si/Ni/α-Si structure after dry oxidation at 700 °C. It was found that as the voltage swept from 8 to −8 V and back to 8 V, a significant threshold voltage shift of 1.7 V was observed. When the whisked voltage was increased to 10 V, a more obvious *C–V* shift of 2.1 V was seen. For samples oxidized at 600 °C, these voltage shifts were larger. In Fig. 4(B), the voltage swept from 3 to −3 V and back to 3 V, a threshold voltage shift of 0.4 V was observed. When the whisked voltage was increased to 5 V, a more obvious *C–V* shift of 2 V was seen. Fig. 5 presents the threshold voltage vs. operation voltage for samples oxidized at different temperatures. The sample which used α-Si/Ni/α-Si structure had improved memory characteristics. As shown in Fig. 1, the nickel silicide nanocrystals of α-Si/Ni/α-Si structure had random distribution between SiO_2 and HfO_2. It was different from the α-Si/Ni conventional device(distribution of plane) [11,13]. It shows that more charges were injected into deep nickel silicide nanocrystals under programming mode. The charges which were injected into deep nickel silicide nanocrystals resulted in the higher threshold voltage. The operating voltage of the memory devices with a conventional floating-gate or semiconductor nanocrystals embedded in SiO_2 is above 7 V [14,15]. In our approach to fabricate the nickel silicide nanocrystals embedded in SiO_2 and HfO_2, a lower programming voltage of 4 V and erasing voltage of −4 V realizes a significant threshold voltage shift, 1.3 V, which is sufficient to be defined as “1” and “0” by a typical sensing amplifier for a memory device.

4. Conclusions

A nonvolatile memory device with $NiSi_2$ nanocrystals embedded in the SiO_2 and HfO_2 layer has been fabricated. A significant memory effect is observed through the electrical measurements. When a low operating voltage, 4 V, is applied a significant threshold voltage shift, 1.3 V, is observed. The processing of the structure is compatible with the current manufacturing technology of semiconductor industry.

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