

Source–drain barrier height engineering for suppressing the a-Si:H TFTs photo leakage current

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Abstract

For effectively reducing the off-state signal loss resulted from the a-Si:H TFTs photo leakage current, the a-Si:H TFTs with the use of ITO as source–drain metal have been fabricated for this study. Several TFT structures have been fabricated to examine this characteristic. A remarkable reduction in photo leakage current has been observed under the 3300 cd/m² CCFL backlight illumination. The source–drain barrier height engineering has been proposed for these results. According to the energy band diagram, the barrier height for hole is estimated about 3 eV. As a result, the photo-generation holes blocked in the source–drain barrier height could effectively reduce the photo leakage current in off-state.

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1. Introduction

Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) have been widely used as switching devices of AM-LCDs. The a-Si:H TFT is particularly advantageous to the production of large flat panel displays and facilitates mass production [1,2]. Metallic films with low resistivity such as copper (Cu) or aluminum (Al) are needed to reduce the RC propagation line delay for the fabrication of large-area and high-resolution AM-LCD's [3]. Copper metallization has been receiving increasing attention in both microelectronics [4,5] and large-area electronics, because RC time delay can be reduced considerably by employing the low electrical resistivity metallurgy. Moreover, to improve the motion blur of TFT-LCD, the double frequency addressing has been proposed to improve the moving image quality. Unfortunately, the double rate operation also reduces the device charging time and therefore reduces the TFT-LCD brightness [6,7].

In addition to reduce the RC propagation line delay for the fabrication of large-area and high-resolution active-matrix liquid-crystal displays (AM-LCD's), the reduction of the TFT off-state leakage current under back light illumination is also an important issue. Because a-Si:H is a photo-sensitive material, the main objectives for flat panel display application are to enhance the field effect mobility and to reduce the off-state leakage current under back light illumination [8]. The off-state leakage current under light illumination is, in particular, a serious problem in the projection and/or multimedia displays that require high intensity backlight illumination. The design rule strategy of TFT-LCD is to increase the on-state current without increase the parasitic capacitance in the gate/source overlap region. In order to reduce the parasitic capacitance between the gate and source/drain electrodes, a self-aligned a-Si:H TFT structure has been proposed. However, the higher off-state leakage current under light illumination compared to a conventional TFT has been observed [9]. As a result, the reduction of off-state photo leakage current in a-Si:H TFT is very important for a high quality TFT-LCD technology.

The most widely adopted method to lower the off-state photo leakage current is to reduce the thickness of undoped a-Si:H

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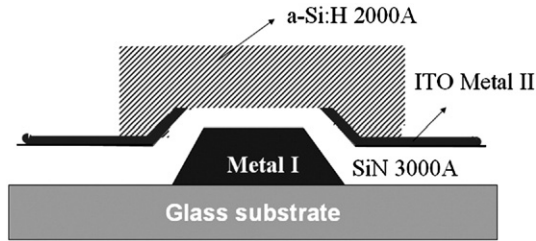


Fig. 1. The structure of the simple TFTs.

layer. However, the reduced undoped a-Si:H thickness would decrease the production yield of large size TFT-LCDs and also decrease the field effect mobility of the TFT devices [10]. Pervious studies have been reported that the off-state dark leakage current of a-Si:H TFT is mainly originated from the hole current [11]. In contrast, electrons are the majority carriers of off-state current for the a-Si:H TFT under light illumination, since electron mobility is much higher than that of hole. Recently, Cl incorporated hydrogenated amorphous silicon a-Si:H (Cl) has been prepared by various deposition methods using SiH_2Cl_2 mixtures to improve film quality [12], stability [13] and deposition rate [14].

Furthermore, the off-state photo leakage current of a-Si:H TFT is also suppressed by the addition of Cl [15,16]. The photo leakage current of a-Si:H(Cl) TFTs is at least two orders of magnitude lower than that of conventional a-Si:H TFTs [17], stemmed from the p-type like behavior of a-Si:H(Cl) channel. In this study, the a-Si:H TFT with ITO as source/drain barrier has been fabricated to transform the device photo leakage current. The off-state leakage current characteristics of a-Si:H TFTs with ITO as source/drain barrier under light illumination was also investigated.

2. Experimental

In order to analyze the electrical characteristic of ITO/a-Si:H, Fig. 1 shows schematically the structure of the simple structure a-Si:H TFTs. After the gate electrode of 300 nm-thick MoW was patterned on the glass substrate, a 300 nm-thick silicon-nitride (SiN_x) were deposited by plasma enhanced chemical vapor deposition (PECVD) method. The 100 nm-thick ITO was continuously deposited by sputtering and patterned as source/drain electrodes. Finally, a 200 nm-thick a-Si:H active layer were deposited by PECVD method, and defined as the island region. Furthermore, the inverted-staggered a-Si:H TFTs with back-channel-etched (BCE) process, were fabricated on glass substrate for the study of electrical characteristics. The device fabrication process was described as followed. After the gate electrode of 300 nm-thick MoW was patterned on the glass substrate, the 300 nm-thick silicon-nitride (SiN_x), a 200 nm-thick a-Si:H active layer and a 50 nm-thick n^+ -a-Si:H were continuously deposited by PECVD method. After defining the island region, the photo resist was not removed and the 100 nm-thick ITO was continuously deposited by sputtering. Afterward the lift-off process was used for the removal of photo resist and ITO in the island region. In general, the sputtering process of the ITO adds the oxygen for good ITO quality. Because the ITO deposition was prior to source/drain metal deposition, the contact resistance of the metal/ITO would be decreased. The capping ability of ITO was also confirmed by the scanning electron microscopy (SEM). The 300 nm-thickness MoW was deposited by sputtering and patterned as source/drain metal. After the electrodes are formed for devices, the n^+ -a-Si:H layer in the TFT channel region would to be etched off using the source/drain pattern as a mask. The detail process flow was illustrated in Fig. 2. The dimension of channel length and width

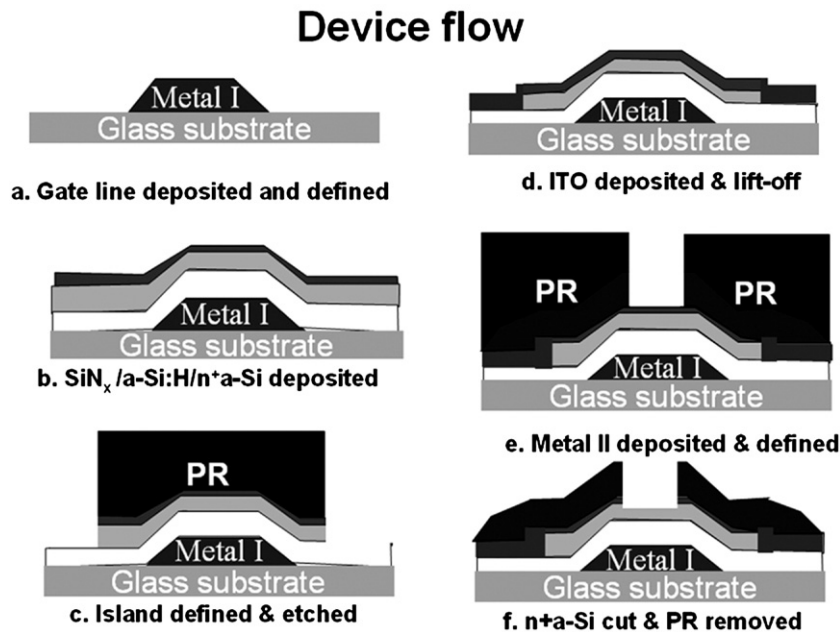


Fig. 2. The detail process flow of the a-Si:H TFT with the ITO as source/drain barrier.

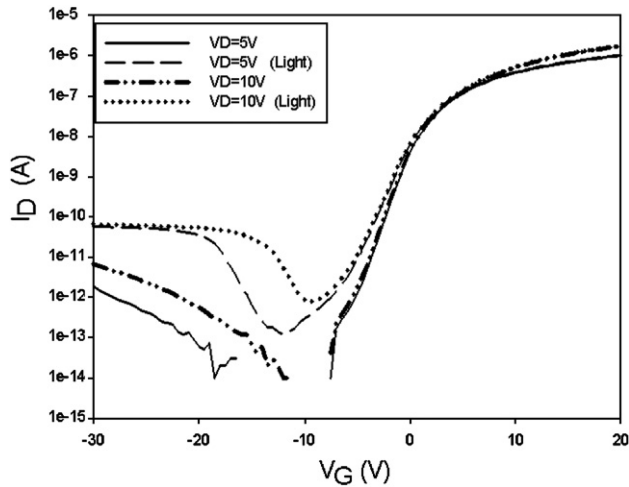


Fig. 3. The photo leakage current characteristic of conventional a-Si:H TFTs.

both was 10 μm for the TFT devices. The electrical measurement was carried out by HP 4156C precision semiconductor parameter analyzer. All TFT structures were measured under the back light illumination. The photo leakage current measurement was carried with the 3300 cd/m^2 CCFL back light to compare the difference in the off-state photo leakage currents between the proposed device and the conventional one.

3. Results and discussion

The photo leakage current of conventional a-Si:H TFTs was shown in Fig. 3. When the a-Si:H TFT was operated in the small negative gate voltage ($V_G > -10$ V) and 5 V drain voltage, the photo leakage current is decreased with the increase of density of states (DOS), serving as recombination centers. However, with the larger negative gate voltage ($V_G < -10$ V), the large photo leakage current was observed. According to previous study [11], the larger off-state photo leakage current is due to the faster hole channel accumulation in the larger negative gate voltage. Fig. 4 shows the electrical characteristic of the simple TFT structure. However, the photo

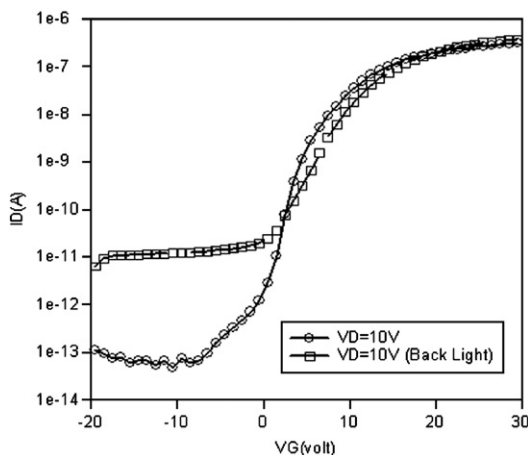


Fig. 4. The photo leakage current characteristic of the simple TFT structure.

leakage current was saturated at about 10^{-11} A in the simple TFT structure. This characteristic was different from the conventional inverted-staggered a-Si:H TFTs. Because the ITO/a-Si:H device is a Schottky diode, the current is carried by majority carriers on both sides of the junction. The photocurrent is primarily due to the photo-excited electron-hole pairs in the a-Si:H, but also due to the photo-excited electrons from the conduction band of the ITO through the interfacial SiO layer into the conduction band of the a-Si:H. The photo-excited electrons in the a-Si:H are accelerated away from the interface and directly contribute to the photocurrent. Also, the photo-excited holes in the a-Si:H can contribute to the photocurrent by recombining via interface states with electrons from the ITO conduction band. However, these holes could also lead to photocurrent suppression via recombining with photo-excited electrons in the a-Si:H conduction band [18]. The work function of the ITO is about 4.1 eV and the band gap of the ITO is about 3.7 eV. Because the off-state current under the back illumination is resulted from the hole generation in the a-Si:H layer, the barrier height for hole is the most important parameter to reduce the photo leakage current. The barrier height for hole is estimated about 3 eV according to the band diagram of ITO/a-Si:H structure. The holes were accumulated near the interface and recombined with photo-excited electrons. If the interfacial SiO layer was thick enough, the photo-excited holes in the a-Si:H can no longer tunnel through the SiO, and recombine with electrons in the ITO conduction band. Instead, they accumulated near the interface and recombined with photo-excited electrons. The photocurrent was, therefore, suppressed in the ITO/a-Si:H structure. Since the recombination rate near the SiO/a-Si:H interface is proportional to the concentration of holes trapped in this region, the simple structure a-Si:H TFT has showed the saturated photo leakage current characteristic. For the application of conventional inverted-staggered BCE a-Si:H TFTs, the ITO source/drain barrier height was introduced by

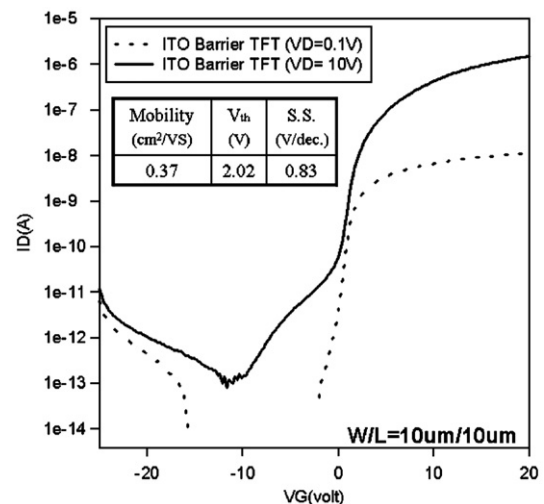


Fig. 5. The characteristics and the device parameter of the a-Si:H TFTs with ITO as source/drain barrier.

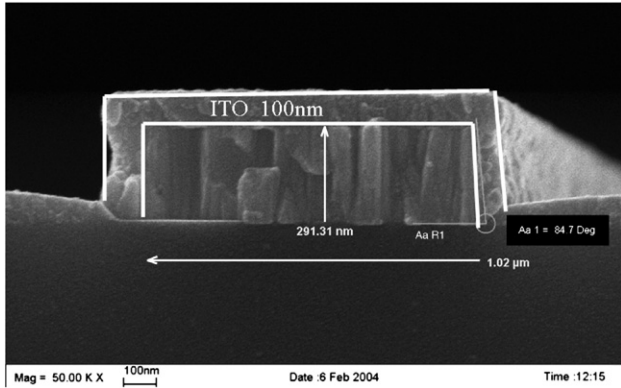


Fig. 6. The SEM picture of the 291 nm-thick thin film capping with 100 nm-thick ITO at the taper angle about 84.7°.

the ITO lift-off process, as shown in Fig. 2. After the device manufacture process, the characteristics of the a-Si:H TFTs with ITO as source/drain barrier demonstrated the field-effect mobility about $0.37 \text{ cm}^2/\text{V}\cdot\text{s}$, the minimum subthreshold swing about $0.83 \text{ V}/\text{dec}$, and the $I_{\text{ON}}/I_{\text{OFF}}$ ratio is 10^6 at $V_{\text{DS}}=10 \text{ V}$. The threshold voltage was about 2.02 V , determined from turn-on current (I_{on}) extrapolation in the linear region of $I_{\text{D}}-V_{\text{G}}$ curve at $V_{\text{DS}}=0.1 \text{ V}$, as shown in Fig. 5. Fig. 6 shows the SEM of the 291 nm-thick thin film capping with 100 nm-thick ITO at the taper angle about 84.7° . The good capping ability of ITO also ensured the existence of the ITO/a-Si:H interface. Fig. 7 shows the transfer characteristics of the a-Si:H TFT with ITO as source/drain barrier under back light illumination. Here the source/drain is illuminated, and different drain voltages were tested. The photo leakage current of the a-Si:H TFT with ITO as source/drain barrier has shown the similar characteristic with the simple structure TFT. Furthermore, the photo leakage current is proportional to the drain voltage, and independent of gate voltage. That's also because the photo-excited holes in the a-Si:H accumulated near the interface and recombined with photo-excited electrons, thereby making the photocurrent characteristic different from the conventional a-Si:H TFT

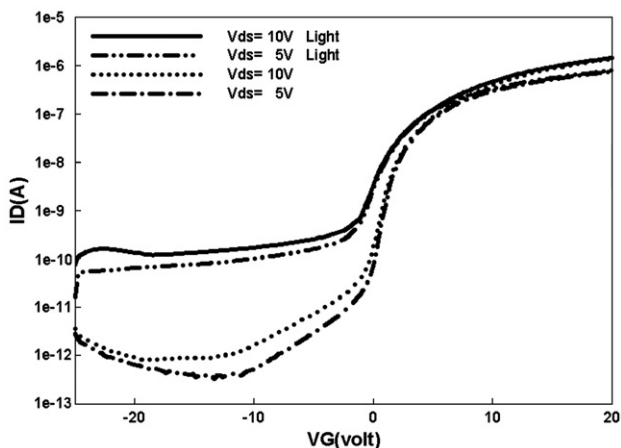


Fig. 7. The transfer characteristics of the a-Si:H TFT with ITO as source/drain barrier under back light illumination.

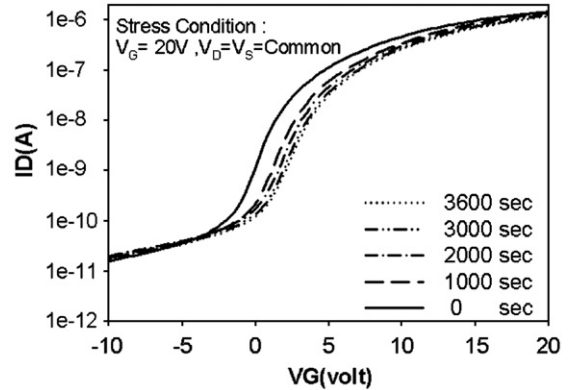


Fig. 8. The transfer characteristics of the proposed device structure after the gate bias stressing for 1000, 2000, 3000, 3600 s.

without ITO as source/drain barrier. Besides, the reliability of the proposed device structure also showed in Fig. 8. The gate bias stress condition was set $V_{\text{G}}=20 \text{ V}$, $V_{\text{D}}=V_{\text{S}}$ is commonly ground for 3600 s. After the gate bias stress, the shift of threshold voltage was only 2.2 V in the proposed structure. This result is also similar to the conventional a-Si:H TFT. Furthermore, the ITO capping process was not an additional step due to the necessity of having ITO as pixel electrode in conventional TFT-LCD manufacture.

4. Conclusion

We have fabricated the simple TFT structure to verify the photo leakage current of the ITO/a-Si:H device. The photo leakage current was different from the conventional inverted-staggered a-Si:H TFT. The suppression of the photocurrent was due to the holes accumulated near the interface and recombined with photo-excited electrons. Furthermore, the a-Si:H TFTs using the ITO as source/drain barrier via the lift-off process was also fabricated without increasing the process steps. The a-Si:H TFT with the ITO as source/drain barrier has shown superior characteristics of photo leakage current compared to conventional a-Si:H TFTs. The photo leakage current is suppressed by the source/drain barrier between the ITO/a-Si:H, and proportional to the drain voltage. The impact of using ITO layer for driving current is to effectively reduce the off-state current under the back illumination. Therefore, the off-state signal loss resulted from the a-Si:H TFTs photo leakage current was reduced. These results indicated that a-Si:H TFT with the ITO as source/drain barrier has the potential for the application of high quality TFT-LCD.

Acknowledgements

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