國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

積體電路之系統層級靜電放電暫態偵測電路設計

Design of On-Chip Transient Detection Circuits for System-Level ESD Protection

研 究 生：廖期聖　　(Chi-Sheng Liao)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國九十七年七月

積體電路之系統層級靜電放電暫態偵測電路設計

Design of On-Chip Transient Detection Circuits for System-Level ESD Protection

研 究 生：廖期聖　　Student: Chi-Sheng Liao

指導教授：柯明道教授　　Advisor: Prof. Ming-Dou Ker

國立交通大學

電子工程學系 電子研究所

碩士論文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao-Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master
in
Electronics Engineering
July 2008
Hsin-Chu, Taiwan, Republic of China

中華民國九十七年七月

積體電路之系統層級靜電放電暫態偵測電路設計

學生：廖期聖　　指導教授：柯明道教授

國立交通大學　電子工程學系電子研究所碩士班

ABSTRACT (CHINESE)

隨者互補式金氧半導體(Complementary Metal-Oxide-Semiconductor, CMOS)積體電路(Integrated Circuits, IC)製程技術的演進，積體電路中的電晶體尺寸逐漸縮小，日益複雜的功能整合在相同積體電路之中，造成積體電路對靜電放電(Electrostatic Discharge, ESD)的耐受度下降，更容易使得在靜電放電的瞬間對積體電路產生破壞，所以靜電放電防護在微電子產品良率及可靠度上扮演相當重要的角色。

由於系統層級靜電放電測試規範(IEC 61000-4-2)之嚴格要求，越來越多的積體電路對系統層級靜電放電更為敏感，即使已經符合元件層級靜電放電(Component-Level ESD)規範之測試，依然無法達到系統層級靜電放電之相關要求。在系統層級靜電放電測試下，一個擁有積體電路的電子設備在接觸放電(Contact-Discharge)及空氣放電(Air-Discharge)測試模式中如欲達到“等級四”的標準需求，則此待測設備(Equipment under Test, EUT)必須通過高達±8kV(接觸放電模式)及±15kV(空氣放電模式)的靜電放電等級(ESD Level)需求。在此測試進行時，待測設備中的積體電路會遭受到由外部耦合(Coupling)至內部的靜電放電能量之影響，一旦此種由靜電放電所造成的暫態電壓耦合至積體電路的電源線(Power Line)上，便有可能引發電子設備不正常工作，甚至損毀。在傳統的防護方法中，多種不同的分離元件被應用於微電子產品之中，但是明顯增加了微電子產品的生產成本。因此，對於系統層級靜電放電防護而言，應用於金氧半導體製程的積體電路設計防護方法具有其重要性。

本論文首先於第二章與第三章提出了採用 0.18-μm 金氧半導體製程之二個系統層級靜電放電暫態偵測電路設計，經由相關模擬以及量測證實，此暫態偵測電路能夠偵測到系統層級靜電放電在電源線上所造成之暫態電壓，並且能夠送出轉態之邏輯訊號。相關的量測方式包括：暫態觸發閂鎖效應測試(Transient-Induced Latchup Test, TLU Test)、系統層級靜電放電測試(System-Level ESD Test)、電性快速脈衝測試(EFT Test)。

其次，暫態偵測電路對於偵測系統層級靜電放電引發之暫態電壓的偵測範圍將在第四章被研究討論，在此採用了多種不同的雜訊濾波器，藉由其對電源線上雜訊抑制的功能，配合暫態偵測電路做量測，證實雜訊濾波器可以改變暫態偵測電路在系統層級靜電放電測試下之偵測範圍。

最後，第五章提出了一個結合雜訊濾波器以及暫態偵測電路的四位元暫態轉數位之轉換器，此種轉換器可以成功的將系統層級靜電放電之電壓轉換為數位訊號輸出，因此能夠確切知道積體電路在系統層級靜電放電測試之下所遭受影響之程度，並期望未來能夠藉由此數位訊號配合軟體以及韌體之設計，對於電子系統做出不同程度的應用，使得具有積體電路的微電子產品能夠通過系統層級靜電放電相關規範之要求。

Design of On-Chip Transient Detection Circuits for System-Level ESD Protection

Student: Chi-Sheng Liao **Advisor: Prof. Ming-Dou Ker**

Department of Electronics Engineering and Institute of Electronics
National Chiao-Tung University

ABSTRACT (ENGLISH)

As the improvement of semiconductor process and technology, the device size of CMOS ICs has been scaled down and more complicated functions are integrated into a single chip. The potential destructive nature of ESD in CMOS ICs becomes serious and the design of ESD protection circuits becomes more challenging in scaled-down CMOS process. Therefore ESD protection has become an important reliability issue in CMOS IC products.

System-level ESD is an increasingly important reliability issue in CMOS IC products. It has been also reported that reliability issues still exist in CMOS ICs under system-level ESD tests, even though they have passed component-level ESD specifications. In order to meet high electromagnetic compatibility (EMC) regulations, the microelectronic products are required to evaluate system performance under reliability test standard of system-level ESD tests. In the system-level ESD test standard of IEC 61000-4-2, the microelectronic products are required to sustain the ESD voltage of ±8kV (±15kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4". The experimental results have confirmed that the power and ground lines of microelectronic products no longer maintain the normal operating voltage under system-level ESD tests, but underdamped sinusoidal waveforms instead. Furthermore, the transient noise under system-level ESD tests can cause system into locked state, system frozed state, transient-induced latch-up, or even hardware damage. In traditional solutions, extra discrete components are added on PCB to

suppress system-level ESD events in microelectronic products. Therefore, the chip-level solutions to meet high system-level ESD specification for microelectronic products are strongly requested by IC industry.

In chapter 2, two transient detection circuits have been designed and investigated to detect the fast electrical transients on the power line (V_{DD}) and ground line (V_{SS}) under system-level ESD tests. In chapter 3, the proposed on-chip transient detection circuits have been fabricated in a 0.18-μm CMOS process with 3.3-V devices. The circuit performance of the circuits has been evaluated by transient induced latchup (TLU) tests, system-level ESD tests, and EFT tests. It has been confirmed that the transient detection circuits can detect and memorize the occurrence of the positive (negative) fast electrical transients on the power and ground lines of CMOS ICs.

Evaluation on the board-level noise filter network to reduce the ESD energy coupling into the DUT under system-level ESD tests is investigated in chapter 4. Different types of board-level noise filters, including capacitor filter, LC-like (2^{nd}-order) filter, π-section (3^{rd}-order) filter, etc., have been evaluated to change the detection range of the proposed on-chip transient detection circuits.

In chapter 5, a novel on-chip transient-to-digital converter composed of four transient detection circuits and four different RC filters has been successfully designed and verified in a 0.18-μm CMOS process with 3.3-V devices. The output thermometer digital codes of the proposed on-chip transient-to-digital converter correspond to different positive/negative ESD voltages under system-level ESD tests. These output digital codes can be used as the firmware index to execute different auto-recovery procedures in microelectronic systems. Therefore, the system with auto-detection function can detect the transient noise and then automatically reset itself to achieve the “Class B” specification defined in the IEC 61000-4-2 standard.

ACKNOWLEDGEMENTS

致謝

在碩士生涯中，首先要感謝我的指導老師柯明道教授所給予的教誨，教導我們做事情必須擁有的嚴謹態度，待人處事必須具備的圓融技巧，尤其老師的『烏龜尾巴』理論，更是我一輩子謹記在心的名言。

在研究過程中，感謝『奇景光電股份有限公司』的蔡志忠副總與陳東暘博士所提供之專業協助和豐富資源，讓我能夠順利的完成研究。

我也要感謝『奈米晶片與系統實驗室』的陳榮昇、許勝福、顏承正、蕭淵文、陳世宏、陳穩義、王資閔、林群祐等學長們，在各方面給予我許多幫助與指導。感謝所有碩班的同學們：感謝縱慾大哥大、豪哥、老木、俊哥與鯉魚學長在研究、學業上給予我的指導。也感謝小州哥一片苦心，讓我在學業上能有多次練習的機會。感謝阿宅、小帆、大仔、宗恩、建名、科科、六號岐陪我一起奮戰，我不會忘記那長達七個小時的戰鬥的。感謝阿邦在我落寞時所給予的微笑。感謝 99 範帶我進入運動健身的世界，讓我有健康的身體。感謝區文在軟、硬體上給予的幫助。感謝歐陽叔叔提供寶貴的人生經驗。再感謝塔哥沒有扭斷張君雅小妹妹的頭，以及國維不時搖晃我的椅子，藉此提振我的精神。此外，謝謝佳琪、筱妊、怡歆、林良、小昀昀、昕爺、天哥、kitty、溫董、a-dair、彥偉、叔叔、小狗達、痴痴等學弟妹們，大家一起打球、唱歌、吃蛋糕，在苦悶的碩士生活中常常帶給我歡笑。

在此，我要特別感謝顏承正學長，承正學長彷彿是我的第二個指導老師，無論在學業、研究、甚至生活上，都給予我相當大的指導與幫助，實驗室的同學們無一不羨慕我有一個這麼好的學長，雖然我經常給學長惹麻煩，但學長從沒來有動怒，總是不厭其煩的替我想辦法解決問題。學長做事非常謹慎細心，處處替人著想，總是燃燒自己照亮別人，無論有多忙，都會抽出時間幫助需要幫助的人。在這二年中，學長所寄給我的信件遠遠超過了三百封以上，貨真價實的三百封指導！即使學長遠在國外，也不忘關心我是否在研究上遇到困難，還特地留了保命錦囊給我。因此，在我的碩士生涯中，我最感謝、最感謝的人就是承正學長。

最後，我要感謝我的家人，父親廖昌植、母親詹淑淑和姊姊廖祐伶，因為有了你們，才能讓我無後顧之憂的完成學業與研究論文，成為了我最強大的後盾，支持者我。

要感謝的人太多了，若有遺漏，在此一併謝過。本論文撰寫時已力求嚴謹，然謬誤之處在所難免，尚祈各位讀者不吝惜賜予寶貴意見，使本論文能更加完善。

廖　期　聖

僅誌於竹塹交大

民國九十七年七月

CONTENTS

Table Captions

Chapter 1

Chapter 5

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 1

Introduction

1.1. Motivation

As the improvement of semiconductor process and technology, the device size of CMOS ICs has been scaled down and more complicated functions are integrated into a single chip. Due to thinner gate oxide and shallower junction depth in advance technologies, microelectronic products with CMOS ICs are susceptible to electrostatic discharge (ESD) damage. The potential destructive nature of ESD in CMOS ICs becomes more serious and the design of ESD protection circuits becomes more challenging in scaled down CMOS process. Therefore, ESD protection has become an important reliability issue in CMOS IC products. In order to verify the robustness of the ESD protections against the ESD-induced energy, many international standards have been established. Component-level ESD and system-level ESD are two kinds of ESD specifications to verify the reliability of the CMOS ICs inside the electronic products. The major difference between component-level ESD and system-level ESD specifications is that whether the equipment under test (EUT) with or without power supply. Component-level ESD test is used to simulated the well-controlled environment, such as factory environment. To characterize component-level ESD susceptibility of CMOS ICs, the test method should follow three ESD test standards: human-body-model (HBM), machine-model (MM), charge-device-model (CDM) [1]-[3].

System-level ESD is an increasingly important reliability issue in CMOS IC products [4], [12]. Under system-level ESD test, the ESD-generated transient electrical voltage with quite large amplitude and fast period can randomly exist on power line (V_{DD}), ground line (V_{SS}), and input/output (I/O) pins to cause malfunction (e.g., loss of data logic state) or hardware destruction (e.g., the chip burns out). In order to meet high electromagnetic compatibility

(EMC) regulations, the microelectronic products are required to evaluate system performance under reliability test standard of system-level ESD tests. In the system-level ESD test standard of IEC 61000-4-2 [5], the microelectronic products are required to sustain the ESD-generated voltage of ±8kV (±15kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4". Recently, more international companies have adopted the system-level ESD standard IEC 61000-4-2 to verify the EMC performance of CMOS IC products. Unfortunately, it has been reported that some CMOS IC products which have passed component-level ESD specifications are susceptible to system-level ESD tests. It has been also reported reliability issues still exist in CMOS ICs under system-level ESD tests, even though they have passed component-level ESD specifications. In the IEC 61000-4-2 standard, contact-discharge and air-discharge test modes are used to verify CMOS IC products under system-level ESD tests. The experimental results have confirmed the power and ground lines of microelectronic products no longer maintain the normal operating voltage under system-level ESD tests, but underdamped sinusoidal waveforms with an amplitude of several tens to hundreds of volts and period of several tens of nanoseconds instead [4]. Furthermore, the transient noise under system-level ESD tests can cause system locked state, system frozed state, transient-induced latch-up, and hardware damage. From the previous studies, it has been reported the super twisted nematic (STN) liquid crystal display (LCD) panel keeps in reset state and shows error display after system-level ESD tests [6]. In traditional solutions, extra discrete components are added to suppress system-level ESD events in microelectronic products [7]. Those discrete components including ferrite bead, magnetic core, and transient voltage suppressor (TVS) are used to decouple, absorb or bypass the electrical transients generating from system-level ESD zapping. In traditional solutions, the total cost of microelectronic products will increase substantially. Additionally, the requirement of ESD level is often depended on customer-defined specifications and ESD protection designs are different for various product applications. It is more challenging to achieve ESD level high

enough than before. System-level ESD protection design plays an important role in many kinds of CMOS IC products. Therefore, the chip-level solutions to meet high system-level ESD specification for microelectronic products are strongly requested by IC industry.

1.2. Introduction of International Standard

ESD is an increasingly important reliability issue on CMOS IC products, especially in the advanced technology. Many international associations, such as ESDA (Electrostatic Discharge Association), AEC (Automotive Electronics Council), EIA (Electronic Industries Alliance), JEDEC (Joint Electron Device Engineering Council), MIL-STD (US Military Standard), etc, draw up the different ESD standards for all kinds of ESD conditions. All of the international standards which have been described above are component-level ESD standards. The component-level ESD standards defined the test environment, test methods, and the corresponding ESD test level. In order to verify the robustness of CMOS ICs under system-level ESD events, many international companies adopt other specifications, such as IEC 61000-4-2 (ESD events) and IEC 61000-4-4 (EFT events). IEC 61000-4 is a part of the IEC 61000 series, and the mainly contents of part4 is about testing and measurement techniques. In this section, the international standards are described below.

1.2.1. IEC 61000-4-2 Specification

The object of the standard, IEC 61000-4-2 is to establish a common and reproducible basis for evaluating the performance of CMOS ICs inside the electrical/electronic microelectronic products. This standard specifies typical waveform of the discharge current, test levels, test equipment, test set-up, and test procedure. In order to verity the disturbance of CMOS ICs under system-level ESD tests, the ESD gun is used to zap the ESD-induced energy into the EUT. Fig. 1.1 (a) shows the equivalent circuit of ESD gun. The energy storage capacitor, the discharge resistor, and the discharge switch shall be placed as close as possible

to the discharge electrode, which is shown in Fig. 1.2. Otherwise, the equivalent circuit of human body model is shown in Fig. 1.1(b). To compare two equivalent circuits, the storage capacitor in Fig. 1.1 (a) is 150pF, and that in Fig. 1.1 (b) is 100pF. Therefore, the ESD-induced energy stored in the system-level ESD condition is lager than that in the component-level ESD condition. The discharge resistors used in the Fig. 1.1 (a) and (b) are 330Ω and 1.5kΩ, respectively. Therefore, the ESD-induced energy generating from ESD gun in system-level ESD tests has faster rise time than that in component-level ESD tests. Fig. 1.3 shows the typical waveforms of the discharge current under system-level ESD test (IEC 61000-4-2) and component-level ESD test (MIL-STD 883). Under 8-kV ESD zapping condition, the peak current in system-level ESD test is about five times larger than that in component-level ESD test. In order to compare the test results obtained from different ESD generators, the characteristics of the waveform of discharge current is listed in Table I and shown in Fig. 1.3. Table II shows the test level (test voltage) of component-level ESD test, such as HBM, MM, and CDM. The system-level ESD test levels with contact discharge and air discharge test modes are shown in Table III. Contact discharge is the preferred test method, and air discharge shall be used where contact discharge can not be applied. It is not intended to imply that the test severity is equivalent between contact discharge and air discharge test modes. To compare Table III with Table II, the test voltage of system-level ESD is lager than component-level ESD, no matter with contact discharge or air discharge. Noteworthiness, the voltage waveforms are different for each method due to the different test methods of test. According to those phenomena, system-level ESD tests are more significant to affect the system operation of the microelectronic products than component-level ESD tests. Table IV shows the evaluation of system-level ESD test results, the test results shall be classified in terms of loss function or degradation of performance of the EUT. In the evaluation table, the microelectronic product should reset itself automatically after system-level ESD test to pass the “Class B” specification at least. The EUT shall be operated within the specified climatic

conditions to avoid unnecessary influence from electromagnetic environment of the laboratory. The measurement setup of system-level ESD test is shown in Fig. 1.4 and the elaboration of this will follow in chapter 3.

1.2.2. IEC 61000-4-4 Specification

IEC 61000-4-4 is an international standard which gives immunity requirements and test procedures related to electrical fast transients (EFT) [8]. EFT disturbances are common in industrial environment where electromechanical switches are used to connect and disconnect. The EFT test is intended to demonstrate the immunity of electronic equipments to transient disturbances such as those originating from switching transients (interruption of inductive loads, relay constant bounce, etc.).

The equivalent circuit diagram of the EFT generator is shown in Fig. 1.5 and the major elements of the EFT test generator are listed in Table V. In particular, the impedance matching resistor R_m (50Ω) and the DC blocking capacitor C_d (10nF) are defined in the standard. The charging capacitor C_c is used to store the charging energy and R_c is the charging resistor. The R_s is used to shape the pulse duration. The effective output impedance of the generator shall be 50Ω.

During EFT tests, the power lines of the CMOS ICs inside the microelectronic products no longer maintain their initial voltage levels. A number of fast transients would couple into power, ground, and I/O pins randomly causing the ICs inside the EUT to be upset or frozen after EFT zapping. The characteristics of such a high-voltage-level EFT-induced disturbance are listed in Table VI and shown in Fig.1.6. The test voltage waveforms of these fast transients are defined in the standard with the repetition frequency of 5kHz and 100kHz. A burst is consisted of seventy-five pulses with repetition period of 0.2ms while the repetition rate is 5kHz under EFT tests. Therefore, the burst duration time is 15ms, and the period between two adjacent bursts is 300ms. Similarly, for the EFT pulse with the repetition frequency of

100kHz, there are seventy-five pulses in each burst and the burst duration time is 0.75ms.

The rise time and duration of a single pulse voltage waveform must accord with the characteristics which are listed in Table VII and shown in Fig. 1.7. A voltage pulse waveform with rise time of 5ns±30% and duration of 50±30% occurs on the pins of EUT under EFT tests. The EFT test levels for testing power supply ports and for testing I/O, data, and control ports of the equipment are listed in Table VIII. The voltage peak for I/O, data, and control ports is half of the voltage peak for testing power supply ports. Level "X" is an open level, and is specified in the dedicated equipment specification.

1.3. Traditional System Design Solutions

In order to improve the immunity of microelectronic products to achieve the strict ESD specifications, there are many approaches that system designers can take to against the ESD damage. One of the system design solution to against system-level ESD events is to add some discrete noise-decoupling components or board–level noise filters on the printed circuit board (PCB), as shown in Fig. 1.8. The discrete components are used to decouple, bypass, or absorb the transient noise generating from system-level ESD events. Therefore, the discrete components can reduce the transient disturbance on microelectronic products. The fast electrical transients will be bypassed or absorbed by the discrete noise-bypassing components. And some noise-decoupling components can even clamp the transient voltage at low level to avoid ESD damage on internal circuits of CMOS ICs. Some discrete noise-bypassing components for ESD protection, such as TVS, or low-pass noise filters have been reported and discussed in the following sections [9].

1.3.1. Transient Voltage Suppressor (TVS)

TVS is commonly used to improve the system-level ESD immunity of microelectronic products. TVS can provide ESD energy discharge path under system-level ESD tests. In the

PCB of microelectronic products, TVS is located near CMOS ICs to provide system-level ESD protection function. The main function of transient voltage suppressor is to absorb high peak power as a surge device under ESD tests. It has been reported that the peak pulse power of TVS can be estimated by

$$P_{peak} = I_{pp} \times V_{clamp} \tag{1}$$

where I_{pp} is the maximum lightning current that TVS can bypass, and V_{clamp} is the voltage when I_{pp} is applied across the device. The device with lower clamping voltage during ESD stress conditions can sustain higher ESD level. Although TVS also can be an ESD protector, the performance is not well enough as other discrete components, which exhibit better system-level ESD immunity. The disadvantage of TVS is high capacitive loading, which can cause distortion on high data rate signals. As a result, TVS is not suitable for high speed applications.

For ESD protections, there are many types of TVS components, such as varistor, metal oxide varitors (MOVs), zener diode, etcs. Varistors are made from ceramic materials. Compare with TVS components, MOVs have lower capacitance. However, for high speed interface applications, the capacitance of MOVs is still not low enough without causing distortion on signals. Other disadvantage of MOVs is that the resistance characteristic of MOVs is nonlinear. The MOVs is high impedance with a low clamping voltage. When voltage is high enough across the MOVs, the resistance value drops to a low level. The voltage drop across the varistor will increase dramatically as the current increases. Varistor is hard to help products to pass the “Class A” level in IEC 61000-4-2 standard owing to the ESD clamping voltage is too high.

1.3.2. Low-Pass Noise Filter

To meet the strict system-level ESD specification, different types of board-level noise filters have been investigated to improve the immunity of CMOS ICs inside the

microelectronic products under system-level ESD tests [10]. Adding board-level noise filter between noise trigger source and CMOS ICs can absorb, bypass, or decoupling ESD-generated energy to avoid ESD damage on EUT. Several types of board-level noise filters, including capacitor filter, LC-like (2^{nd}-order), and π-section (3^{rd}-order) filters, which have been investigated and confirmed the enhancement of system-level ESD immunity. Among different noise filter network, the higher-order noise filters have better system-level ESD immunity. For example, it have been investigated that π-section (3^{rd}-order) filters have better enhancement of system-level ESD immunity.

1.3.3. Design Concept of Printed Circuit Board (PCB)

While discrete ESD components are required to suppress the effect of system-level ESD events, PCB design is another important topic on ESD immunity of EUT. First, the magnetic of the current induced into circuit loop will be proportional to the size of the loop [9]. Therefore, minimizing the loop size on the PCB is a critical issue for ESD reliability enhancement. Second, placing the circuit devices on the PCB as close as possible is important to minimize the lengths of signal and power lines. By using this method, it can avoid receiving too much energy generating from system-level ESD events.

Table I Waveform parameters of discharge current.

Level	Indicated Voltage (kV)	First Peak Current of Discharge ±10% (A)	Rise Time With Discharge Switch (ns)	Current (±30%) at 30ns	Current (±30%) at 60ns
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Table II Component-level ESD specifications.

Model Name	Test Voltage
Human Body Model	> 2000V
Machine Model	> 200V
Charge Device Model	> 1000V

Table III System-level EMC/ESD specifications - test levels.

Contact Discharge		Air Discharge	
Level	Test Voltage	Level	Test Voltage
1	±2kV	1	±2kV
2	±4kV	2	±4kV
3	±6kV	3	±8kV
4	±8kV	4	±15kV
X (1)	Special	X (1)	Special
(1) "X" is an open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment may be needed.			

Table IV Recommended classifications of system-level ESD test results.

Criterion	Recommended Classification
Class A	Normal performance within limits specified by the manufacturer, requestor or purchaser.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention. (Automatic Recovery)
Class C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention. (Manual Recovery)
Class D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

Table V Characteristics of the EFT generator.

Parameter	Definition
R_c	Charge Resistor
C_c	Energy Storage Capacitor
R_s	Impulse Duration Shaping Resistor
R_m	Impedance Matching Resistor (=50Ω)
C_d	DC Blocking Capacitor (=10nF)

Table VI Characteristics of the fast transient/burst.

Repetition Rate	Repetition Period	Pulse Number	Burst Duration	Burst Period
5kHz	0.2ms	75	15ms	300ms
100kHz	0.01ms	75	0.75ms	300ms

Table VII Characteristics of a single pulse in each burst.

Parameter	Value
Frequency	5 or 100kHz
Rise Time	5ns±30%
Duration	50ns±30%

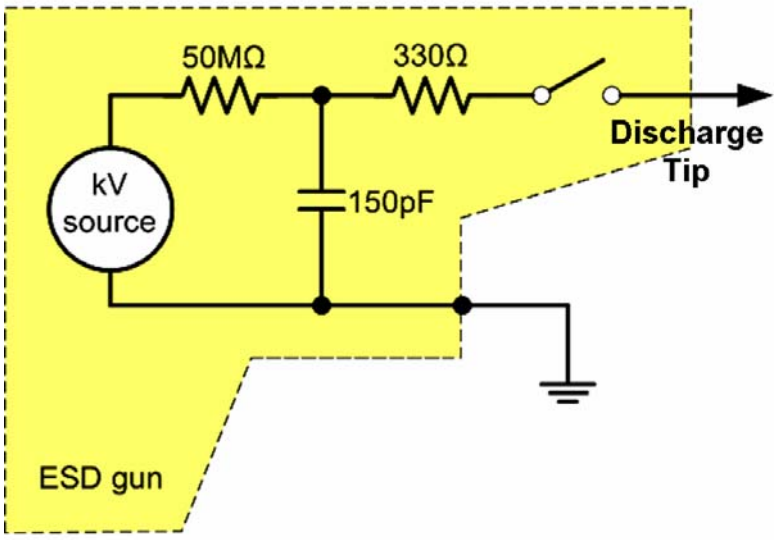
Table VIII EFT specifications - test levels.

Level	Voltage[(a)] (kV)	Voltage[(b)] (kV)
1	±0.5	±0.25
2	±1	±0.5
3	±2	±1
4	±4	±2
X[(c)]	Special	Special

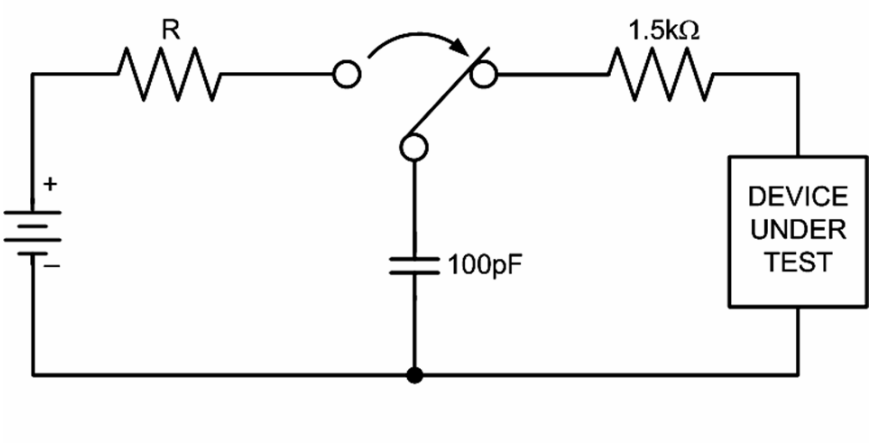
(a) On power ports.

(b) On I/O(input/Output) signal, data, and control ports.

(c) “X” is an open level. The level has to be specified in the dedicated equipment specification.



(a)



(b)

Fig. 1.1 The equivalent circuit of (a) ESD gun which is used to zap the ESD-induced energy under system-level ESD test and of (b) human body model under component-level ESD test.

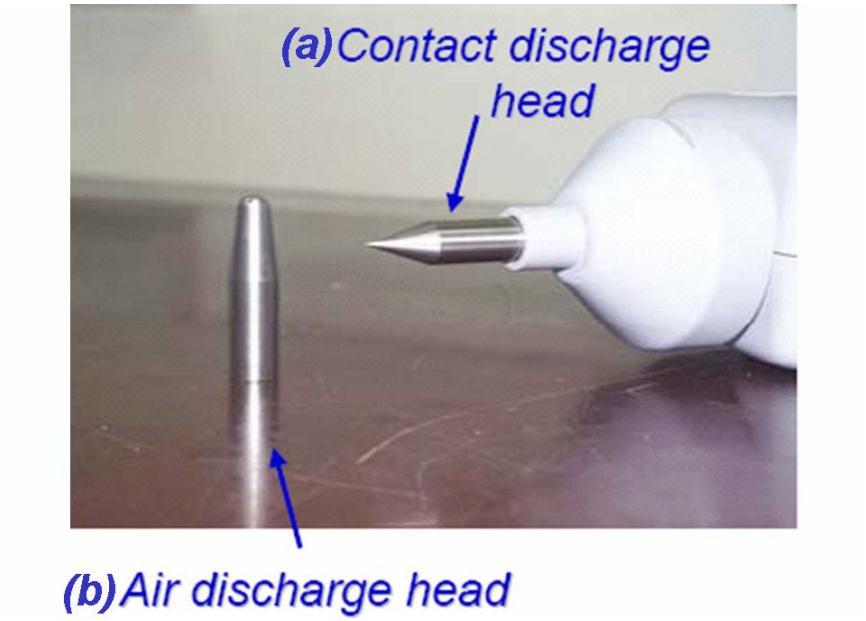


Fig. 1.2 Discharge electrodes of ESD gun which is used under system-level ESD test with (a) contact discharge mode and (b) air discharge mode.

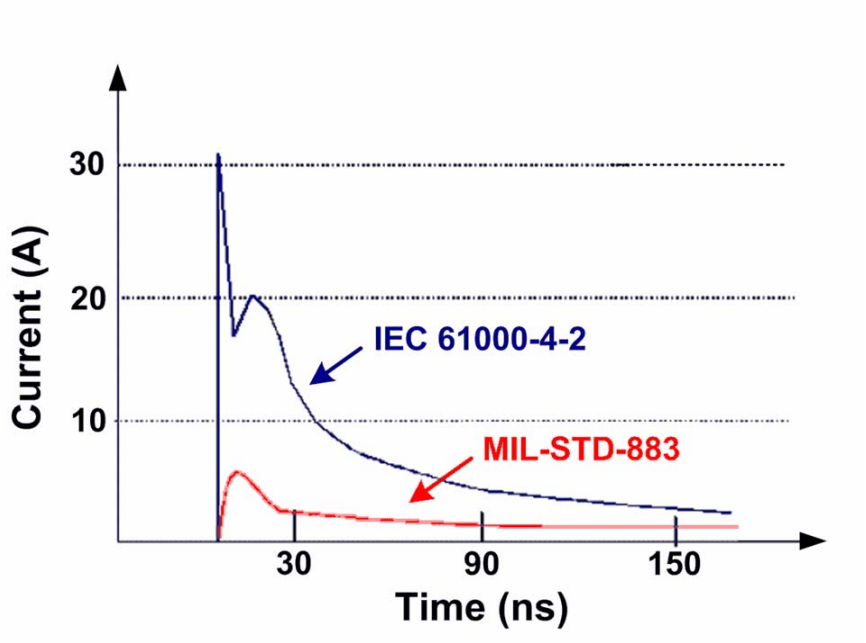


Fig. 1.3 Under 8-kV ESD zapping, the peak current in system-level ESD test is about five times larger than that in component-level ESD test.

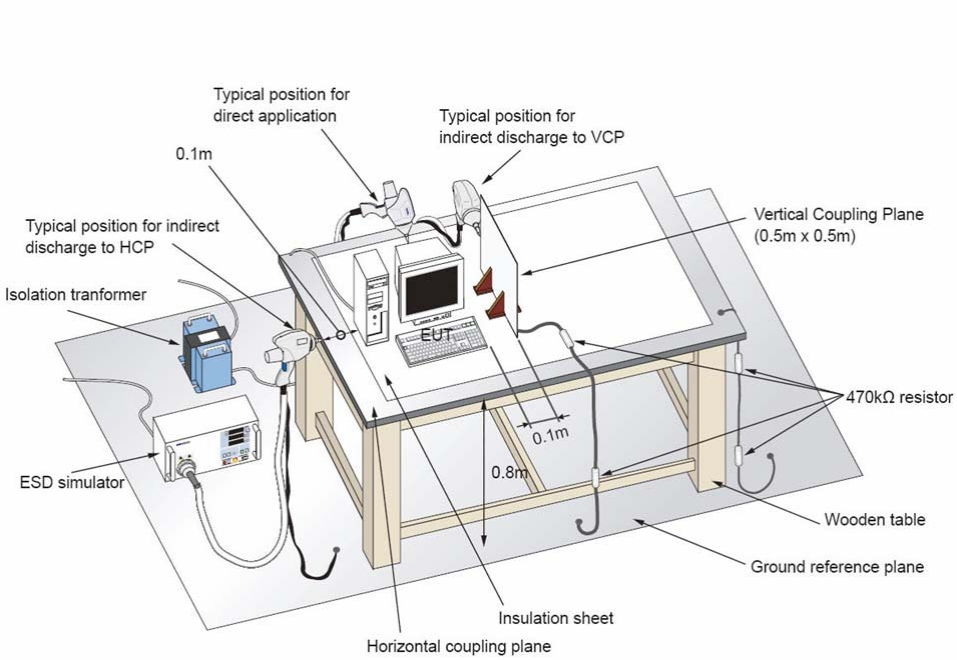


Fig. 1.4 Measurement instruments of system-level ESD test.

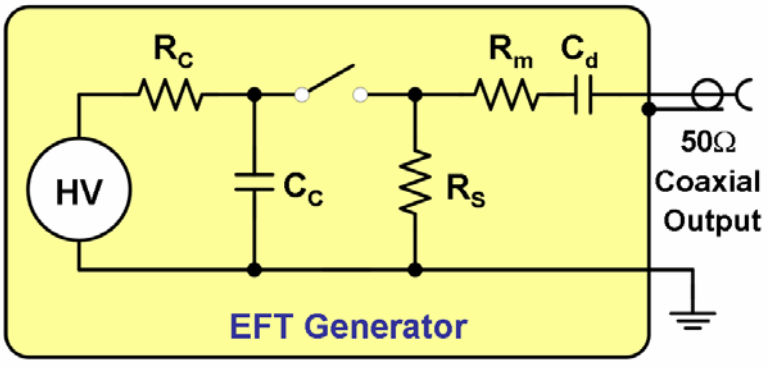


Fig. 1.5 The equivalent circuit of EFT generator.

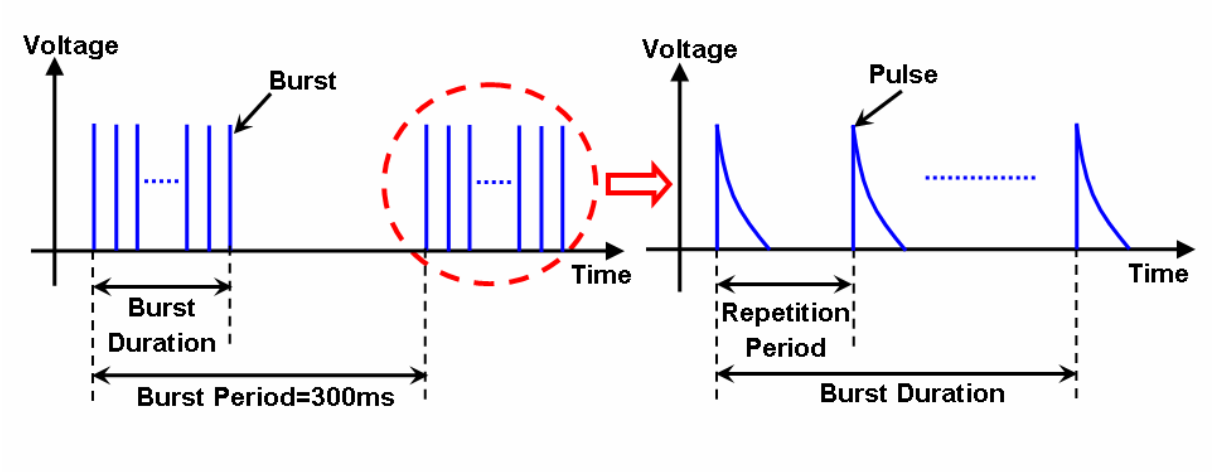


Fig. 1.6 General graph of a fast transient/burst.

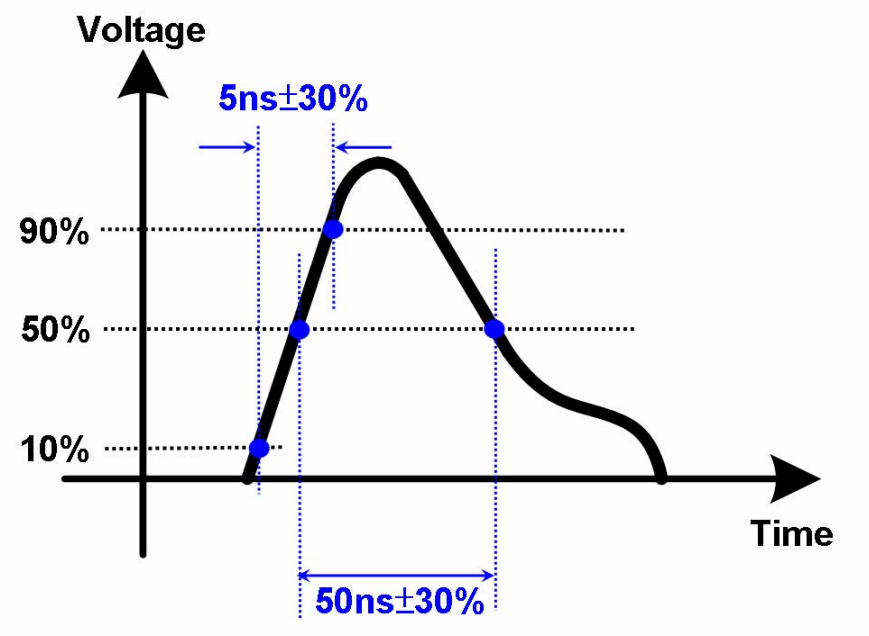


Fig. 1.7 Voltage waveform of a single pulse in each burst.

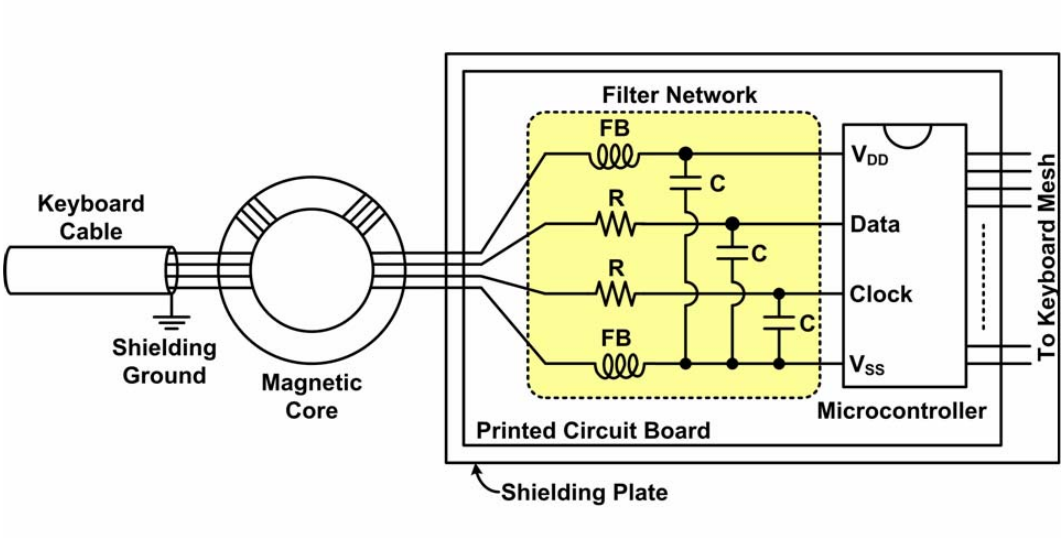


Fig. 1.8 The system solution to overcome the system-level ESD issue in keyboard by adding extra discrete components to absorb or bypass the electrical fast transients.

Chapter 2

Design of On-Chip Transient Detection Circuits

2.1. Background

During system-level ESD tests, the power line (V_{DD}) and ground line (V_{SS}) of CMOS ICs inside EUT will be disturbed with high-energy ESD-induced transient noise. Such high ESD-induced noise on the power line and ground line can lead to data loss, malfunction, or hardware damage of microelectronic products. To avoid the system upset or frozen by the system-level ESD stress, the system should design with auto-detection function to detect the fast transients, then the system can automatically reset itself and restore to stable state. Therefore, the system can achieve the "Class B" specification which is defined in the specification, IEC 61000-4-2 required by most international companies. According to this reason, an effective on-chip circuit to detect the electrical transients under system-level ESD tests is devised by IC industry.

2.1.1. Prior Art

Two transient detection circuits for system-level ESD protections have been proposed [7], [11]. The circuit diagram of the first on-chip transient detection circuit is shown in Fig. 2.1 (a). There are two latch logic gates used as the ESD sensor unit to detect the system-level ESD events on the power and ground lines. Some coupling capacitors can be added to the ESD sensor between the input/output nodes of latch and V_{DD}/V_{SS} lines in order to enhance the sensitivity of the ESD sensor to fast transients on the V_{DD}/V_{SS} line. Therefore the simulation tool HSPICE can be used to fine tune the device size and the capacitance in the ESD sensor to detect the overshooting or undershooting transients. It has been analyzed that the NMOS in the inverter of sensor_1 in Fig.2.1 (a) is designed with a larger W/L ratio than that of the

PMOS to make the latch locking at logic 0 easily. The PMOS in the inverter of sensor_2 is designed with a larger W/L ratio than that of the NMOS to make the latch easily locking at logic 1.

The other transient detection circuit is designed with latch logic gates and capacitors shown in Fig. 2.1 (b). In this transient detection circuit, a latch circuit composed of inv1 and inv2 is used to memorize the logic state after the system-level ESD tests. The capacitors C_{p1} (C_{p2}) are used to detect the positive (negative) fast electronic transients. These device parameters of the circuit such as W/L ratio and capacitance can be designed and simulated by HSPICE. It has been confirmed that the W/L ratio of inverters in the latch and the coupling capacitance will strongly influence the sensitivity of this detection circuit. In order to increase the operation speed to detect the system-level ESD events, the NMOS (M_{n1}) in the inverter (inv1) is designed with a lager W/L than that of PMOS (M_{p1}). On the contrary, the PMOS (M_{p2}) in the inverter (inv2) is designed with a lager W/L than that of NMOS (M_{n2}). The NMOS (M_{nr}) can provide a reset function to pull down node A and then the output of the detection circuit (V_{OUT}) can be set to logic 0. Furthermore, this reset function can be realized with NMOS or PMOS. When the voltage of V_{DD} is below the voltage of V_{SS}, the parasitic diodes of PMOS such as M_{p1} and M_{p2} would be turned on. Therefore, this circuit can detect the positive system-level ESD events. Correspondingly, the parasitic diodes of NMOS such as M_{n1} and M_{n2} would be turned on under the negative system-level ESD stress.

2.1.2. Simulation Parameter in HSPICE Simulator Tool

2.1.2.1. System-Level ESD Tests

It has been reported that the V_{DD}/V_{SS} lines of CMOS ICs will be influenced during system-level ESD zapping conditions [7]. The power and ground lines of microelectronic ICs no longer maintain the normal voltage levels, but an underdamped sinusoidal voltage with amplitude of several hundred volts instead. Fig. 2.2 (a) and (b) show the measured V_{DD}

waveforms on the CMOS ICs inside EUT with the positive and negative ESD zapping, respectively. According to the measured results, the proper parameters of the simulated voltage source such as frequency, damping factor, voltage amplitude, and delay time can be constructed. Therefore, in order to investigate and simulate the transient voltage waveforms occurred on the power line and ground line under system-level ESD events, a specific time-dependent voltage source given by

$$V(t) = V_0 + V_A \times \sin(2\pi D_{Freq}(t - t_d)) \times \exp(-(t - t_d)D_{Factor}) \quad (2)$$

is used to apply an underdamped sinusoidal voltage on the V_{DD}/V_{SS} lines of CMOS ICs, as shown in Fig. 2.3 to investigate the performance of proposed on-chip transient detection circuits.

2.1.2.2. Electrical Fast Transient (EFT) Tests

For EFT pulse with the repetition frequency of 5kHz, the measured voltage waveforms on the 50-Ω resistor with +200V and -200V are shown in Fig. 2.4 (a) and (b). Due to the impedance matching resistors of the EFT generator and EUT, the measured transient peak voltage is +100V and -100V. An exponential time-dependent voltage source with rise/fall time constant parameters is used to simulate the EFT-induced transient disturbance on the power lines of CMOS ICs. The rising edge of the exponential voltage pulse is expressed as

$$V_{P1} = V_1 + (V_2 - V_1) \times [1 - \exp(-\frac{Time - t_{d1}}{\tau_1})] \quad \text{, when } t_{d1} \le t \le t_{d2}. \quad (3)$$

The falling edge of the exponential voltage pulse is expressed as

$$V_{P2} = V_1 + (V_2 - V_1) \times [1 - \exp(-\frac{t_{d2} - t_{d1}}{\tau_1})] \times \exp(-\frac{Time - t_{d2}}{\tau_2}) \quad \text{, when } t \ge t_{d2}. \quad (4)$$

With the proper parameters such as rise (fall) time constant τ_1 (τ_2), rise (fall) delay time t_{d1} (t_{d2}), initial DC voltage value V_1, and exponential pulse voltage V_2, the exponential voltage source can be constructed to simulate the EFT-induced disturbance under EFT tests as shown in Fig. 2.5.

2.2. New Proposed On-Chip Transient Detection Circuits

There are two new transient detection circuits which have been investigated for system-level ESD protection. The proposed circuits are designed to detect the positive and negative fast electronic transients under system-level ESD tests. In this section, the circuit operation and HSPICE simulation of proposed on-chip transient detection circuits have been analyzed.

2.2.1. On-Chip Transient Detection Circuit I

2.2.1.1. Circuit Structure

The schematic diagram of proposed on-chip transient detection circuit I consisted of transient detection block, memory block, and output buffer block is shown in Fig. 2.6. To detect the fast electronic transients on the V_{DD}/V_{SS} lines under system-level ESD tests, the RC delay circuit is used in this work. The detection function is based on the different rise time value between power-on condition (in the order of milliseconds) and system-level ESD event (in the order of nanoseconds). The RC time constant between milliseconds and nanoseconds is designed to distinguish system-level ESD events from normal power-on status. Therefore, the duration of the RC time constant can be significantly longer than the period of the fast transients on the power line. Two inverters (INV_2 and INV_3) comprise the latch structure as a memory block which can provide storage function to memorize the occurrence of system-level ESD events. The NMOS (M_{nr}) is designed to provide the initial reset function while the V_{reset} input signal attains to high logic level, and then NMOS (M_{nr}) can be turned on to cause low logic level at the output node (V_{OUT}). The voltage level at the node V_{RC} is logic high under normal operating condition, and then the NMOS (M_n) can be turned off without changing the logic states memorized in the memory block after reset function. Under system-level ESD tests, voltage response of the node V_{RC} is slower than power line because of the longer RC time constant design. The longer delay at the node V_{RC} causes the PMOS of

INV_1 to conduct. The potential on the gate of NMOS (M_n) is increased toward to V_{DD} rail, and the M_n device can be turned on. Consequently, the output logic state stored at node V_B can be changed from low voltage level to high voltage level. Finally, the output voltage of the transient detection circuit can be changed to high logic level to detect and memorize the occurrence of system-level ESD events.

2.2.1.2. HSPICE Simulation Results under System-Level ESD Test

A time-dependence voltage source with different parameters such as frequency, damping factor, and voltage amplitude has been constructed to simulate the system-level ESD events. Because of the disturbance on the V_{DD}/V_{SS} line under system-level ESD stress occurs randomly, there are many different combinations of voltage source parameters applied on the V_{DD} or V_{SS}. To investigate the performance of the transient detection circuit I under different conditions, the simulated results is shown in Fig. 2.7 ~ Fig. 2.8. The simulated V_{DD}, V_{SS}, V_{RESET}, and V_{OUT} waveforms with positive-going (negative-going) underdamped sinusoidal voltage on both V_{DD} and V_{SS} lines are used to simulate the positive (negative) system-level ESD zapping conditions. In the following HSPICE simulation with underdamped sinusoidal waveforms on V_{DD}/V_{SS} lines, the same parameters of $D_{Facter}=2x10^7s^{-1}$, $D_{Freq}=50MHz$, td=500ns are used in both positive and negative underdamped sinusoidal voltage source, whereas the only different is the value of voltage amplitude. Firstly, the initial DC V_{DD} voltage is kept at 3.3V with a relatively V_{SS} of 0V. Secondly, a logic high voltage pulse is used to trigger the reset function of the transient detection circuit causing the initial output voltage at 0V and the memory block would store this logic state. Fig. 2.7 (a) (Fig. 2.8 (a)) shows the overshooting (undershooting) voltage amplitude coupled on both V_{DD}/V_{SS} lines, and the voltage amplitude on V_{DD} is lager than that on V_{SS}. On the contrary, the overshooting (undershooting) voltage couple on both V_{DD} and V_{SS} shown in Fig. 2.7 (b) (Fig. 2.8 (b)), but that on the V_{SS} is lager. During different system-level ESD conditions, the V_{DD}/V_{SS} begins to

jiggle rapidly from 3.3V/0V and the output node V_{OUT} is disturbed simultaneously. As the results, after V_{DD}/V_{SS} returns to its normal voltage level of 3.3V/0V, the output voltage of the transient detection circuit will be changed from 0V to 3.3V.

The routing traces may be different for power lines and ground lines on the PCB shown in Fig. 2.9. For this reason, coupling path from the ESD zapping source to the V_{DD} and V_{SS} inside ICs may be different. A signal delay of 5ns between V_{DD} and V_{SS} waveforms under system-level ESD zapping has been measured, as shown in Fig. 2.10. In order to simulate this signal delay condition, a 5-ns delay time between the V_{DD} and V_{SS} is applied on the underdamped sinusoidal waveforms with positive-going and negative-going shown in Fig. 2.11 (a) and (b). From the simulated results with a signal delay between V_{DD} and V_{SS}, the on-chip transient detection circuit can still detect the fast electrical transients.

2.2.1.3. HSPICE Simulation Results under EFT Test

In order to achieve the requirement of a single exponential pulse under EFT tests, the parameters of τ_1=3ns, τ_2=25ns, and t_{d1}-t_{d2}=10ns are used to simulate the positive/negative time-dependent voltage waveforms. In addition, the initial DC voltage on the power line (V_{DD}) of the transient detection circuit I is still at 3.3V.

The simulated V_{DD}, V_{RESET}, and V_{OUT} waveforms of the proposed on-chip transient detection circuit I with a positive/negative exponential voltage pulse on the V_{DD} are shown in Fig. 2.12 (a) and (b). To reset the output voltage level of the transient detection circuit I to 0V, a logic high voltage pulse is applied on the reset function. Then, the exponential voltage source with amplitude of +15V is used to simulate the positive EFT-induced transient disturbance on the power lines under EFT tests. V_{DD} begins to increase rapidly from 3.3V to 13V, and the output voltage of transient detection circuit I is influenced at the same time as shown in Fig 2.12 (a). Similarly, the exponential voltage source with amplitude of -15V is used to simulate the negative EFT-induced transient disturbance on the power lines under EFT

tests. V_{DD} begins to decrease rapidly from 3.3V to -13V, and the output voltage of transient detection circuit I is influenced simultaneously as shown in Fig 2.12 (b). After the positive/negative transient disturbance duration, V_{DD} returns to its initial voltage level of 3.3V and the output state of the transient detection circuit I changes from 0V to 3.3V.

2.2.2. On-Chip Transient Detection Circuit II

2.2.2.1. Circuit Structure

The design concept of the proposed transient detection circuit II for system-level ESD test shown in Fig 2.13 is investigated in this section. The RC-based structure is used to detect the fast electrical transients under system-level ESD stress. The time response of power-on condition is in the order of milliseconds and that of the system-level ESD events is in the order of nanoseconds. Therefore, the RC time constant is designed between nanoseconds (ns) and milliseconds (μs) to distinguish the power-on condition and system-level ESD events. The node V_{RC} is originally kept at V_{DD} as logic 1, and the PMOS (M_P) is turned off. The NMOS (M_{nr}) can realize a reset function by using a power-on reset circuit. After power-on reset procedure, the output voltage (V_{OUT}) is set to 0V as logic 0, and the NMOS (M_N) can be simultaneously turned on to maintain the voltage level of node V_{FP} at 0V initially. Under system-level ESD events, the V_{DD} voltage of transient detection circuit II is disturbed with an underdamped sinusoidal waveforms that has a fast rise (fall) time of nanoseconds. The PMOS (M_P) can be turned on due to the longer RC time response. Therefore the PMOS (M_P) can conduct a voltage to V_{FP} causing this node to change the voltage level from logic 0 to logic 1. While the node V_{FP} is set to logic 1, the NMOS (M_N) can be turned off due to the feedback loop. After system-level ESD tests, the PMOS (M_P) and NMOS (M_N) are turned off and no discharge path conducts at node V_{FP}. The logic state at node V_{FP} is memorized to logic 1, and the output of on-chip transient detection circuit II is finally changed from logic 0 to logic 1 to detect and memorize the occurrence of system-level ESD events.

2.2.2.2. HSPICE Simulation Results under System-Level ESD Test

The simulated waveforms of V_{DD}, V_{SS}, V_{RESET}, and V_{OUT} of the proposed on-chip transient detection circuit II with positive-going and negative-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} are shown in Fig. 2.14 (a) and (b). The initial V_{DD} voltage level is kept at 3.3V with a relatively V_{SS} of 0V. In order to simulate the disturbance on the CMOS ICs under positive system-level ESD zapping, a time-dependent overshooting voltage waveform with amplitude of +12V is applied to the power line shown in Fig.2.14 (a). At the same time, an underdamped waveform with the same parameters such as damping factor, frequency and time delay is used on the ground line. The only different parameter applied to the V_{SS} is the smaller amplitude of +5V. After system-level ESD events, the output voltage level V_{OUT} is changed from 0V to 3.3V. Fig. 2.14 (b) shows a similar simulated result of V_{DD}, V_{SS} V_{RESET} and V_{OUT} waveforms, but the underdamped sinusoidal waveforms applied on both V_{DD} and V_{SS} are negative-going voltage source to simulate the negative system-level ESD zapping condition. That is to say, the amplitude of underdamped sinusoidal voltage source applied on the power and ground lines are both negative. As the result, after V_{DD} finally returns to its original voltage level of 3.3V, V_{OUT} is pulled up its voltage level to 3.3V. A simulated condition of signal delay between V_{DD} and V_{SS} waveforms are shown in Fig. 2.15 (a) and (b). This signal delay condition under system-level ESD tests is due to the different coupling path from the ESD zapping source to the V_{DD}/V_{SS} pins of CMOS ICs on the PCB. In order to simulate the signal delay condition under positive and negative system-level ESD zapping, a time-dependent overshooting (undershooting) underdamped sinusoidal voltage source with amplitude of +12V (-12V) is applied to the V_{DD}, as shown in Fig. 2.15 (a) (Fig. 2.15 (b)). At the same time, an underdamped waveform with the same parameters including voltage amplitude is used on the V_{SS}. A signal delay of 5ns between V_{DD} and V_{SS} is also applied to the power and ground lines of the proposed on-chip transient detection circuit. During the period with fast transient stress, V_{OUT} is influenced by the V_{DD}/V_{SS} disturbance.

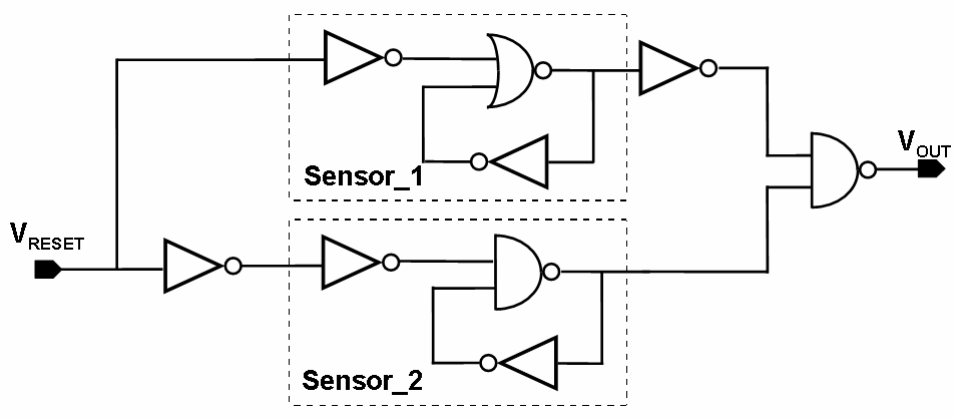
When V_{DD} (V_{SS}) returns to its normal operating voltage of 3.3V (0V), V_{OUT} is finally changed from 0V to 3.3V after system-level ESD tests.

2.2.2.3. HSPICE Simulation Results under EFT Test

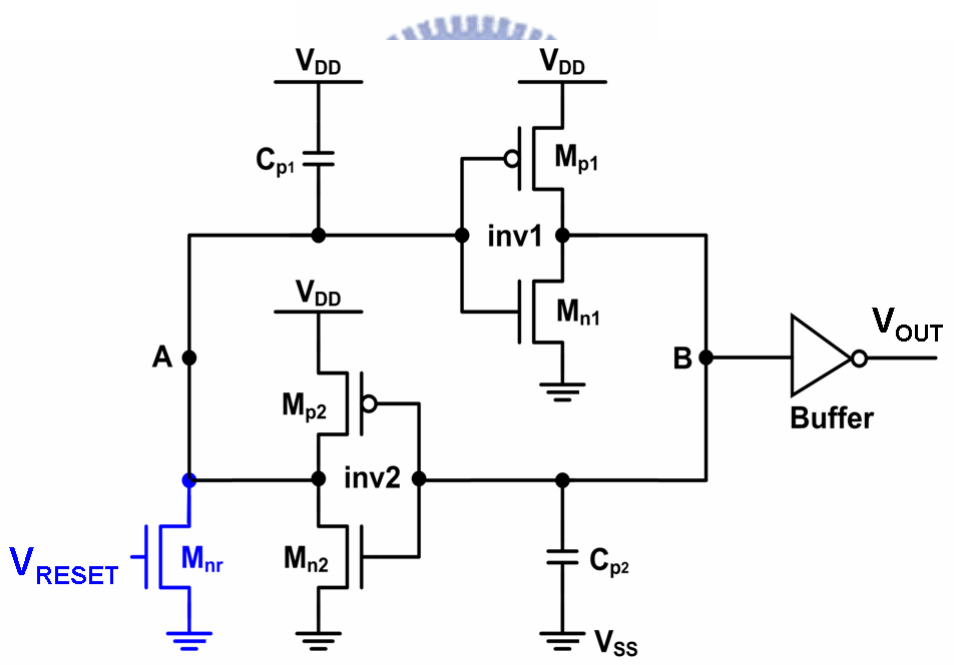
The simulated V_{DD}, V_{RESET}, and V_{OUT} waveforms of the proposed on-chip transient detection circuit II with a positive/negative exponential voltage pulse on the V_{DD} are shown in Fig. 2.16 (a) and (b). A logic high voltage pulse is used to reset the output state to 0V as the initial state. Then, the exponential voltage source with amplitude of +15V (-15V) is used to simulate the positive (negative) EFT-induced transient disturbance on the power lines under EFT tests. The output voltage (V_{OUT}) of transient detection circuit I is influenced by the V_{DD} disturbance simultaneously. After the positive (negative) transient disturbance duration, the output state of the transient detection circuit II transmits from 0V to 3.3V.

2.3. Conclusion

The circuit performance of the two proposed on-chip transient detection circuits has been investigated by the simulation tool HSPICE. The device size of transient detection circuits can be optimized by using HSPICE. From the simulation results, the output voltage level of both new proposed on-chip transient detection circuits can changed from logic 0 to logic 1 after system-level ESD and EFT events. Therefore, these two circuits can detect the positive and negative fast electronic transients disturbed on the V_{DD} or V_{SS} lines. Furthermore, two proposed on-chip transient detection circuits can memorize the occurrence of system-level ESD and EFT events.

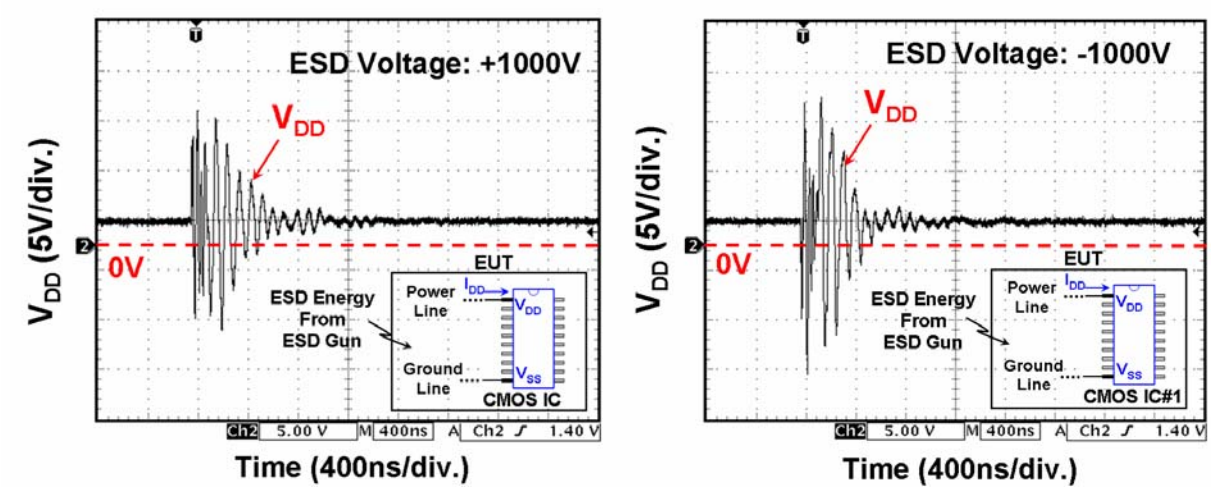


(a)



(b)

Fig. 2.1 The previous on-chip transient detection circuit realized with (a) sensor units and with (b) NMOS-reset function.



(a) (b)

Fig. 2.2 Measured V_{DD} waveforms under system-level ESD tests with ESD voltage of (a) +1000V and (b) -1000V.

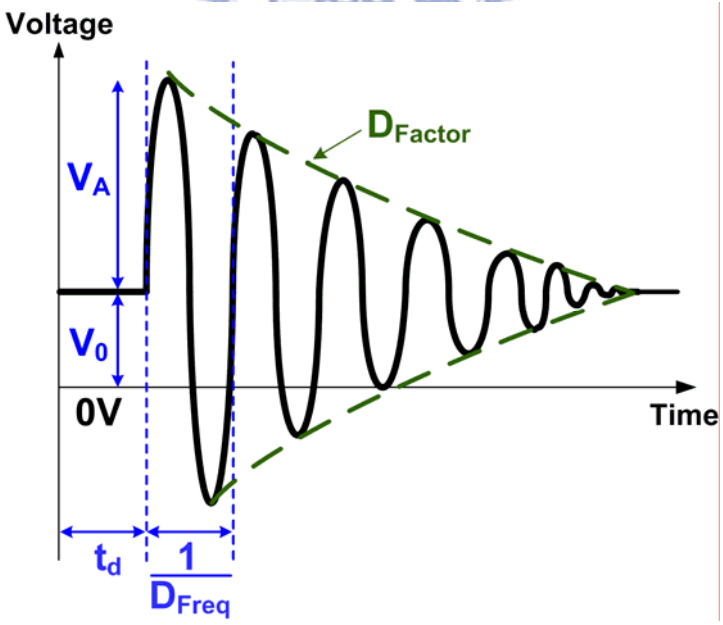
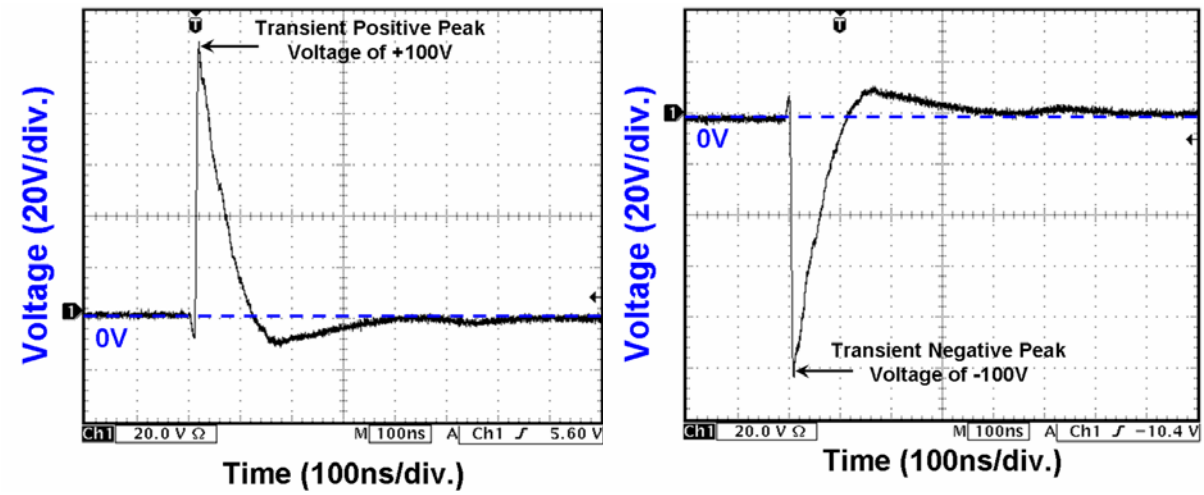


Fig. 2.3 The specific time-dependent underdamped sinusoidal waveforms applied on the power and ground lines to simulate the disturbance under system-level ESD zapping.



(a) (b)

Fig. 2.4 Measured voltage waveforms of a single pulse on 50Ω under EFT tests with EFT voltage of (a) +200V and (b) -200V.

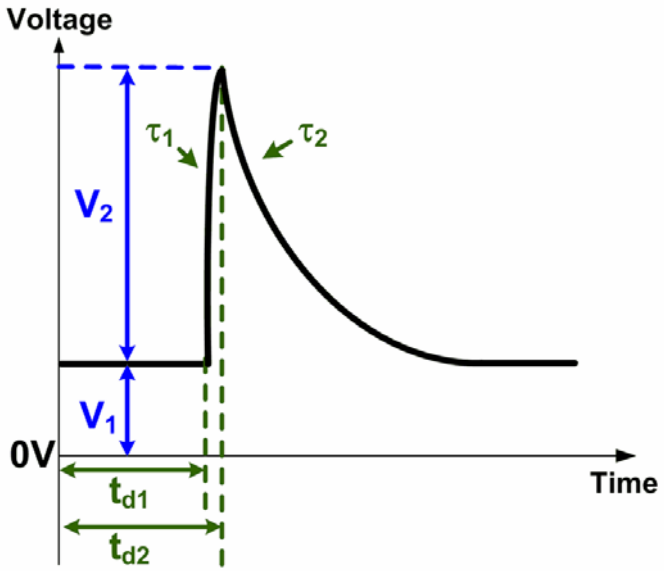


Fig. 2.5 The specific time-dependent exponential pulse waveform applied on the power lines to simulate the disturbance under EFT zapping.

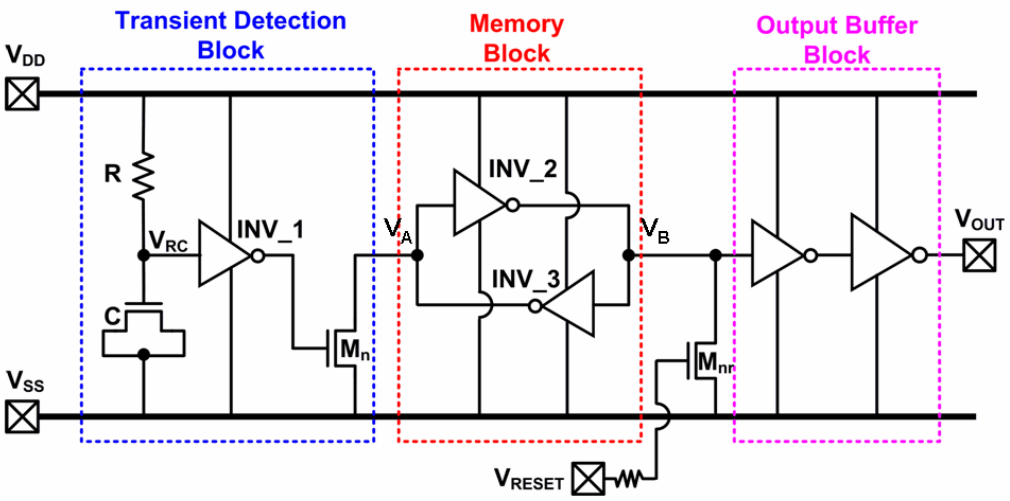
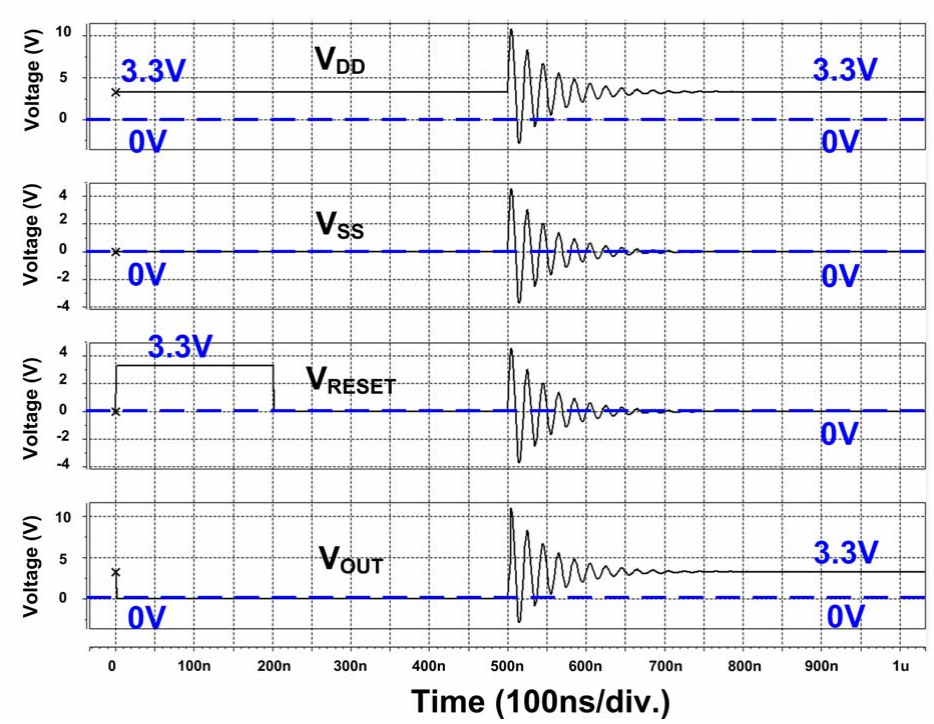
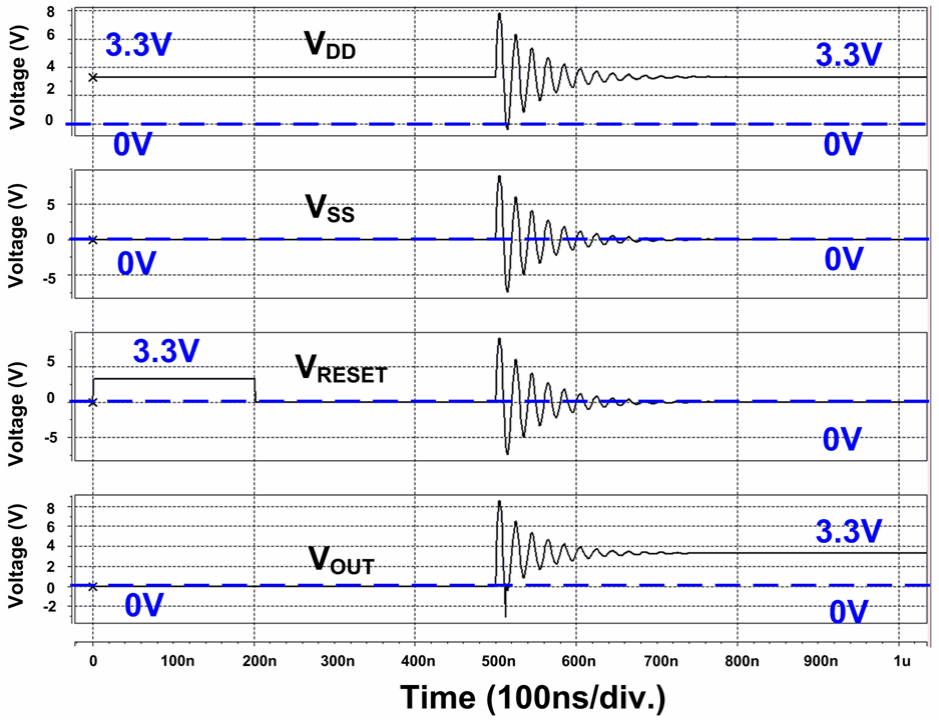


Fig. 2.6 Schematic diagram of the proposed new transient detection circuit I.

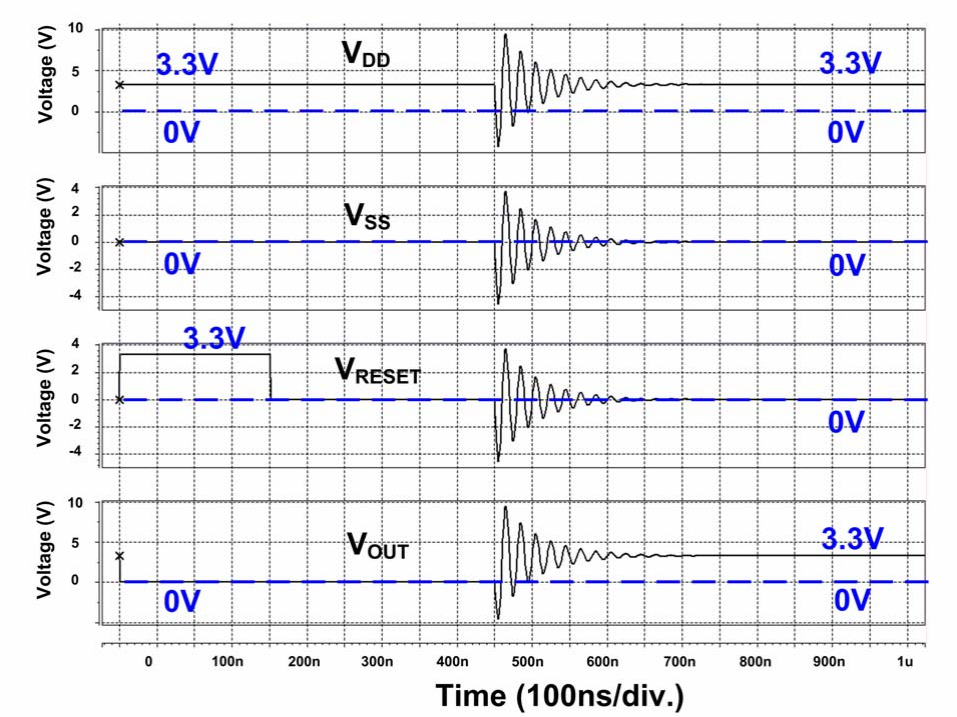


(a)

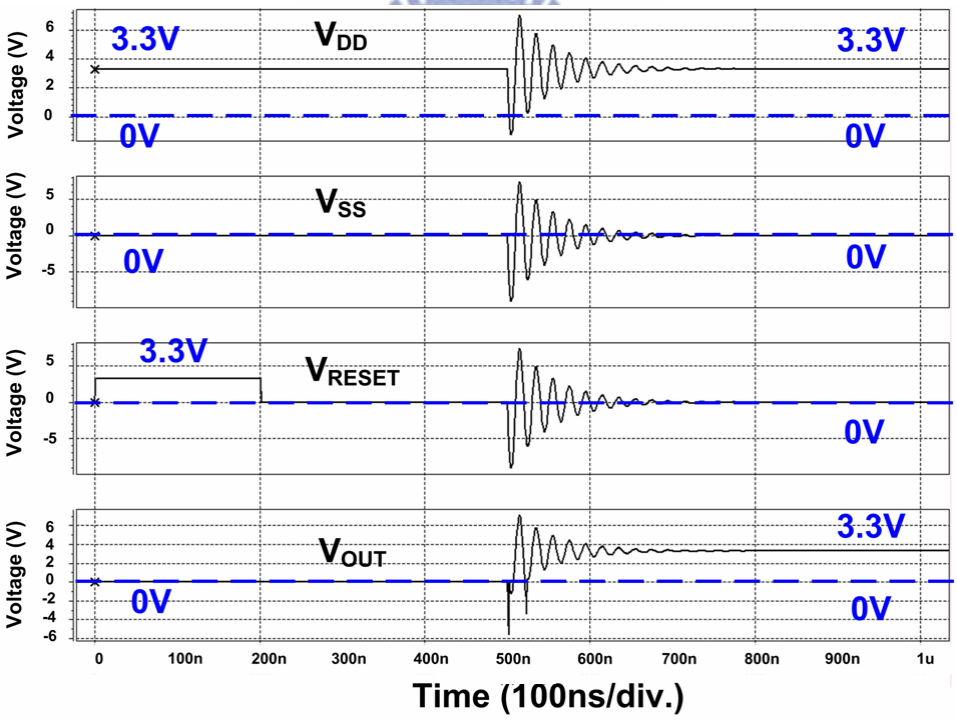


(b)

Fig. 2.7 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit I with positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS}. (a) The overshooting amplitude on V_{DD} is larger than that on V_{SS} (b) The overshooting amplitude on V_{SS} is larger than that on V_{DD}.



(a)



(b)

Fig. 2.8 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit I with negative-going underdamped sinusoidal voltage on both V_{DD} and V_{SS}. (a) The undershooting amplitude on V_{DD} is larger than that on V_{SS} (b) The undershooting amplitude on V_{SS} is larger than that on V_{DD}.

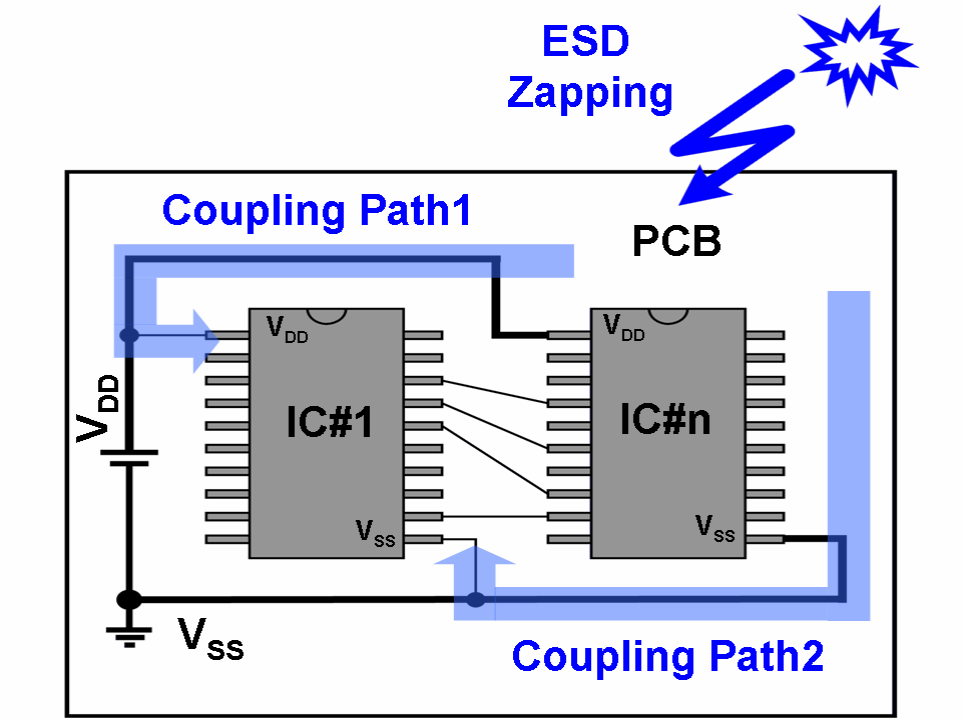


Fig. 2.9 Different coupling path from the ESD zapping source to V_{DD} and V_{SS} pins of CMOS IC on the PCB.

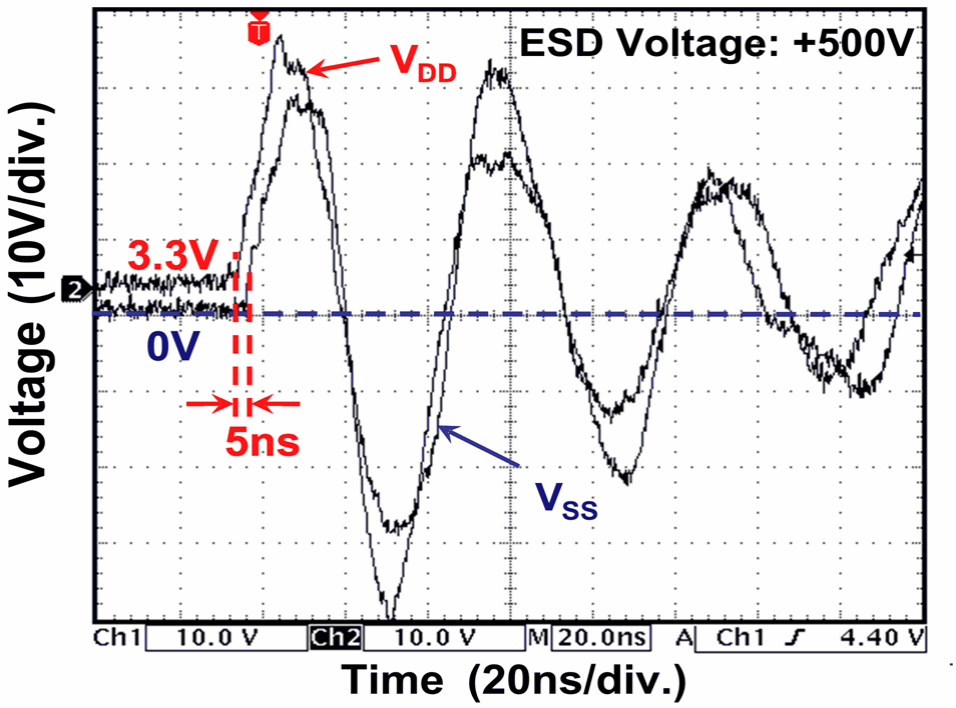
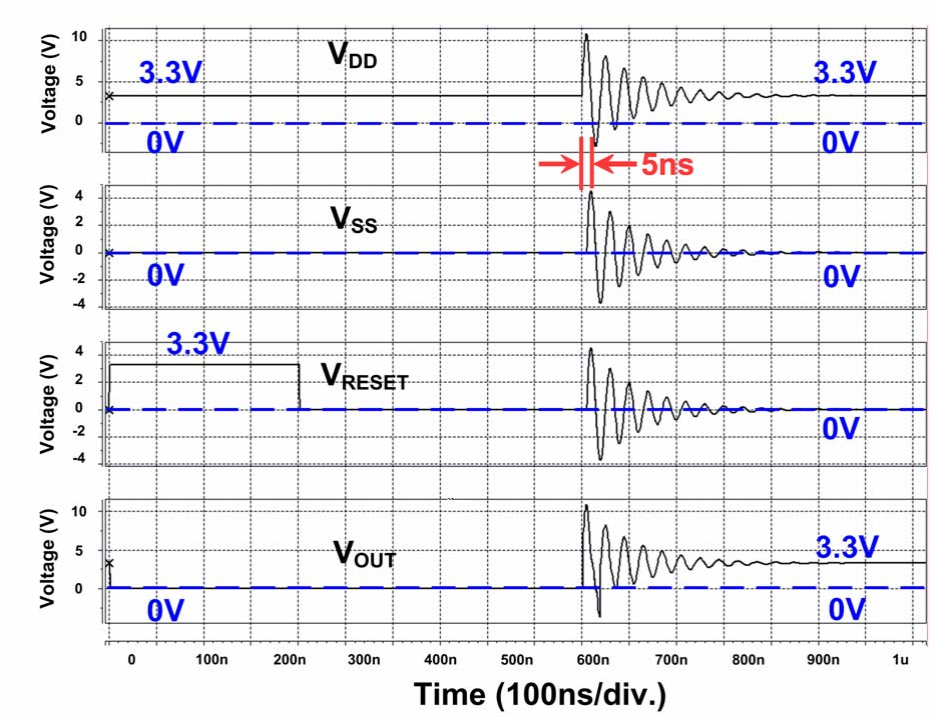
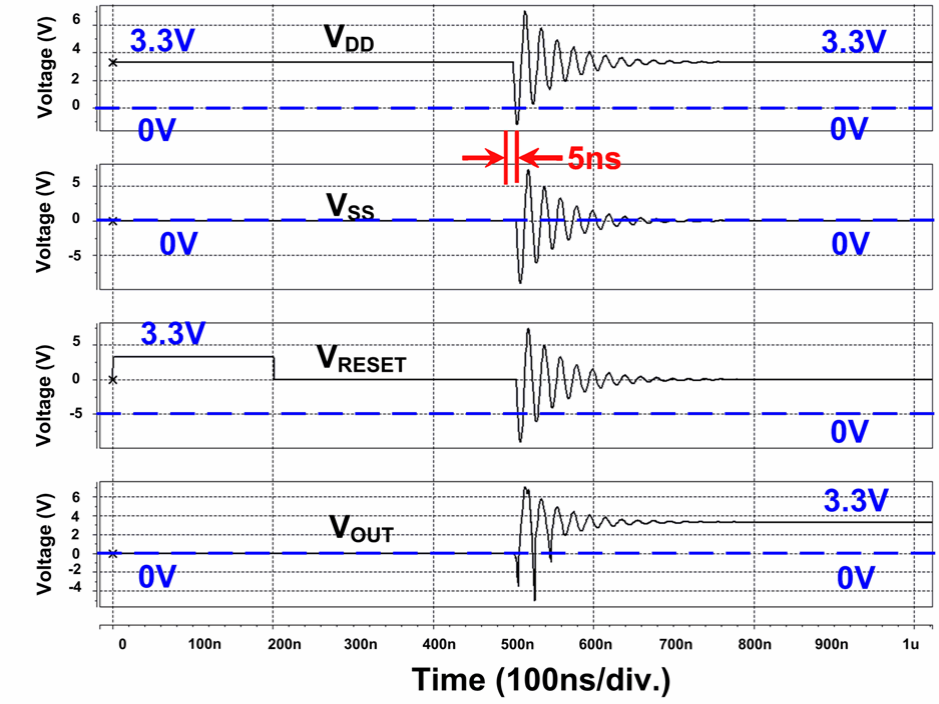


Fig. 2.10 Time delay between the measured V_{DD} and V_{SS} waveforms is due to the different coupling path.

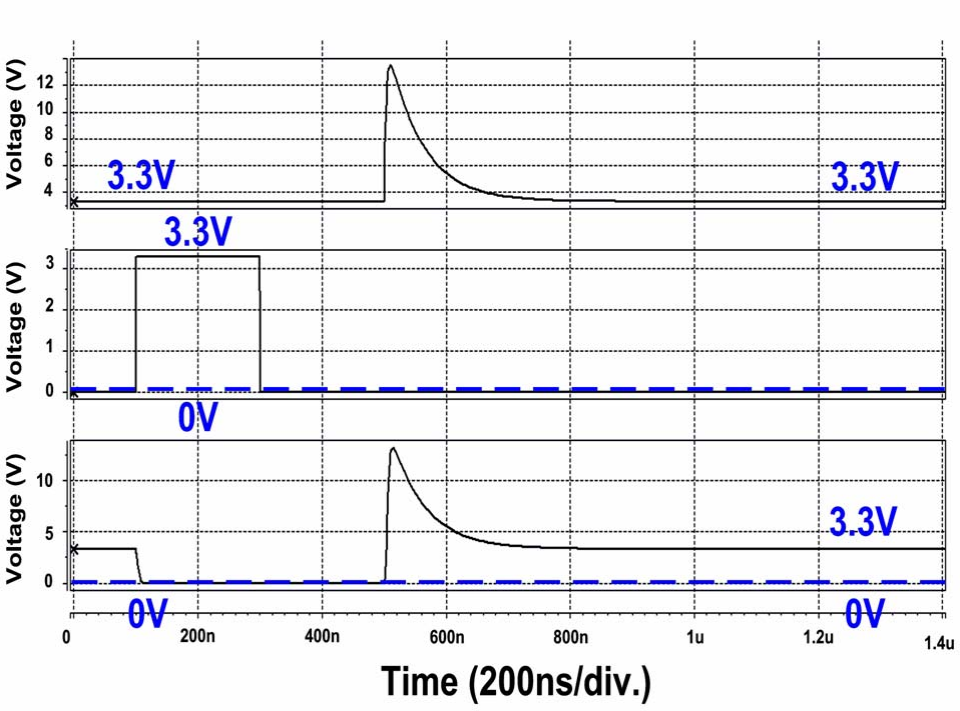


(a)

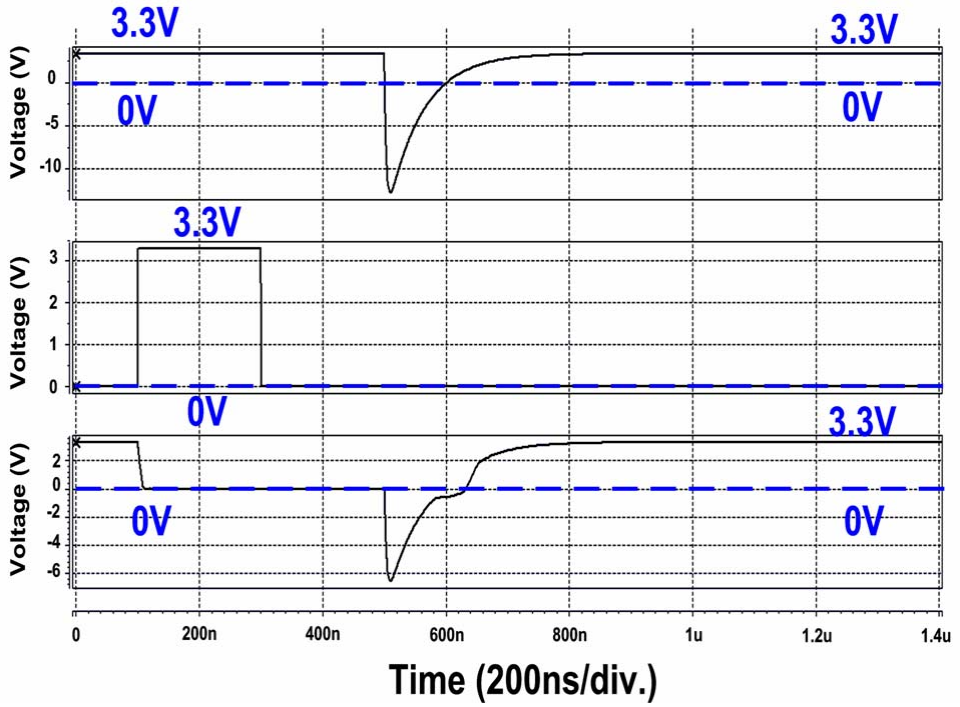


(b)

Fig. 2.11 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit I under (a) positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} with 5ns delay time and under (b) negative-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} with 5ns delay time.



(a)



(b)

Fig. 2.12 Simulated V_{DD}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit I under (a) positive exponential pulse on V_{DD} with amplitude of +15V and under (b) negative exponential pulse on V_{DD} with amplitude of -15V.

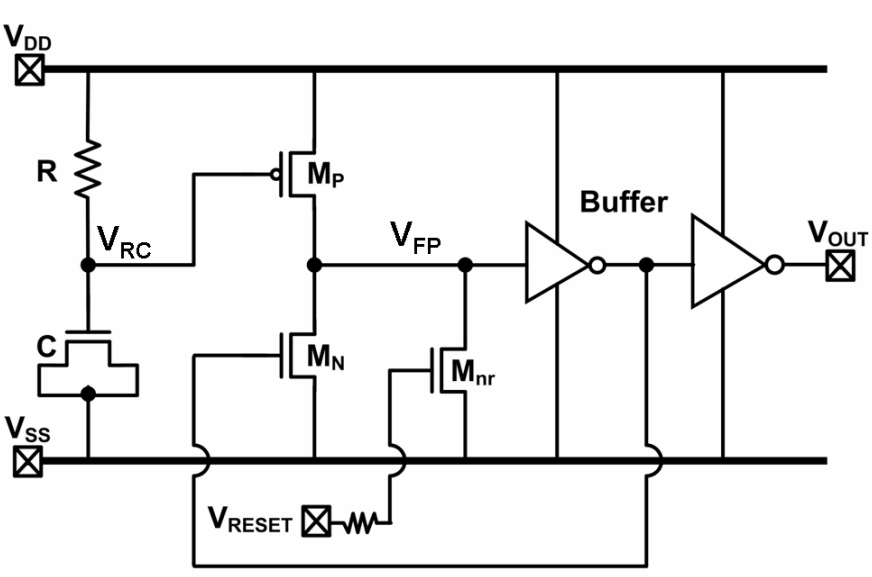
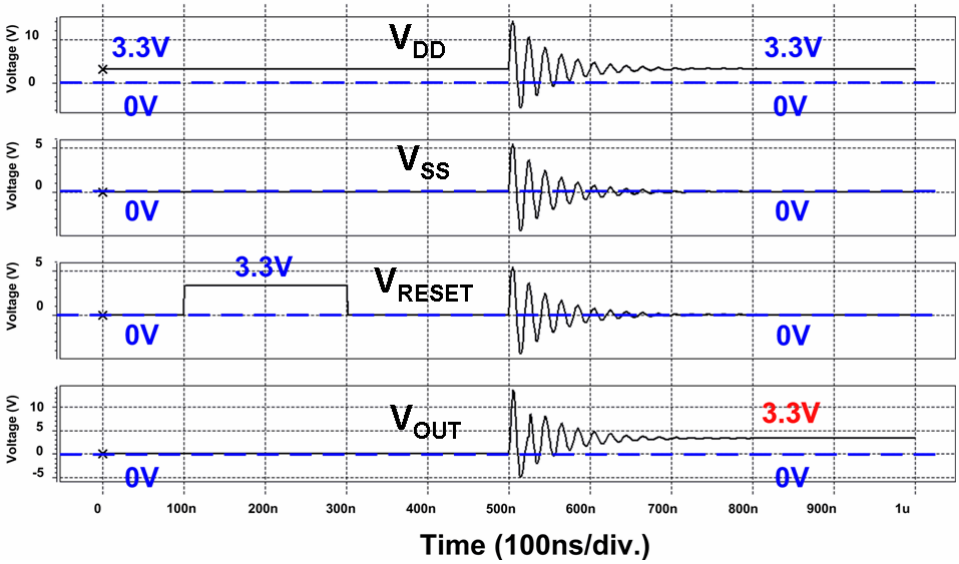
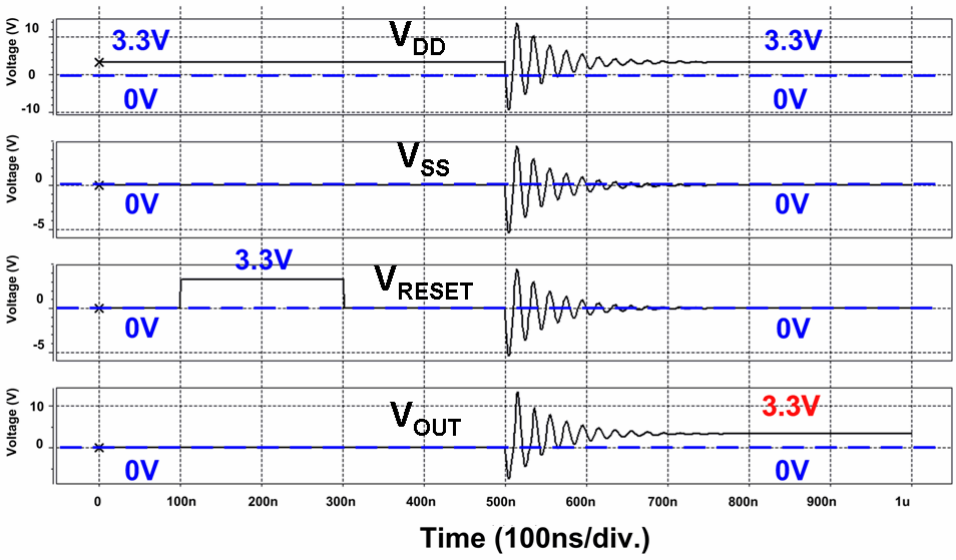


Fig. 2.13 Schematic diagram of the new transient detection circuit II realized with a feedback loop.

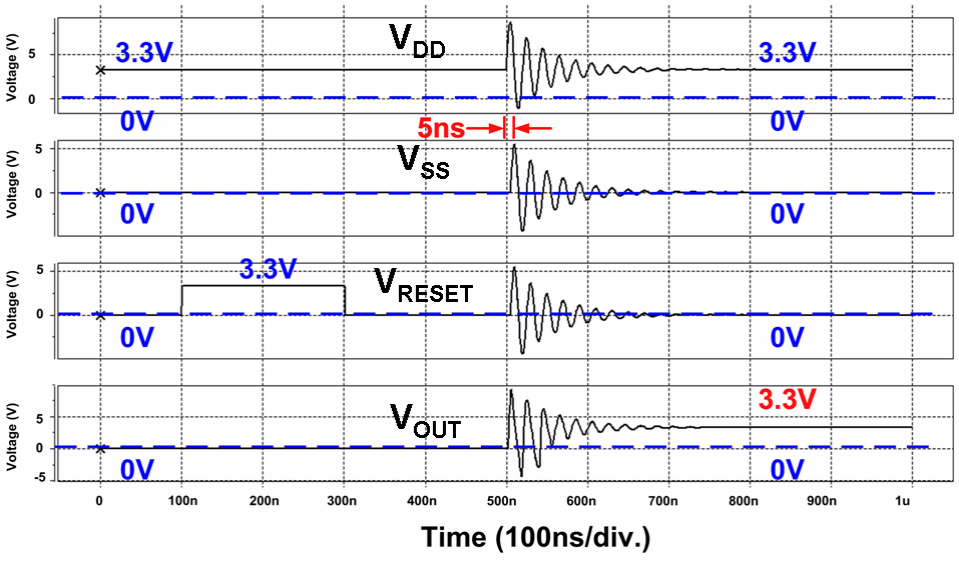


(a)

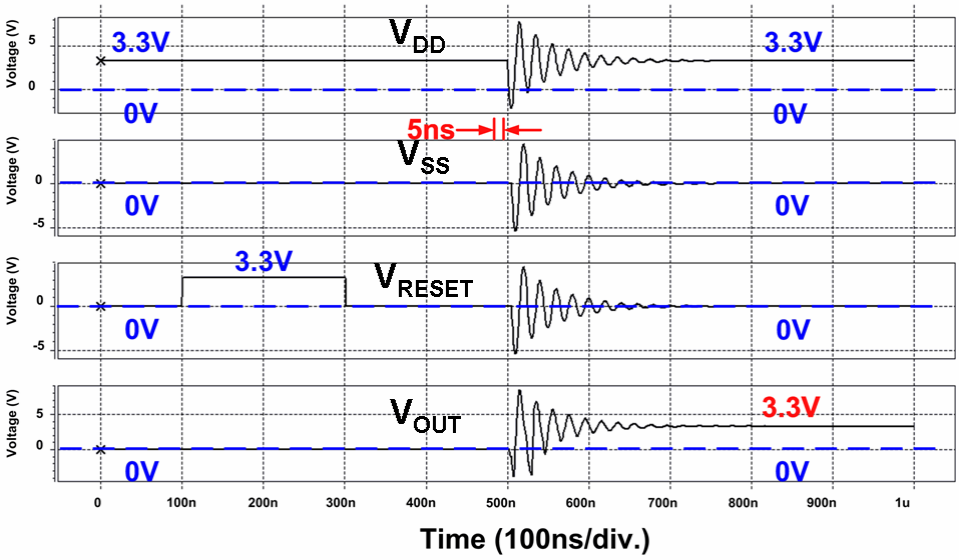


(b)

Fig. 2.14 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit II with (a) positive-going underdamped sinusoidal voltage and with (b) negative-going underdamped sinusoidal voltage on both V_{DD}/V_{SS}, and both the overshooting amplitudes on V_{DD} are larger than that on V_{SS}.

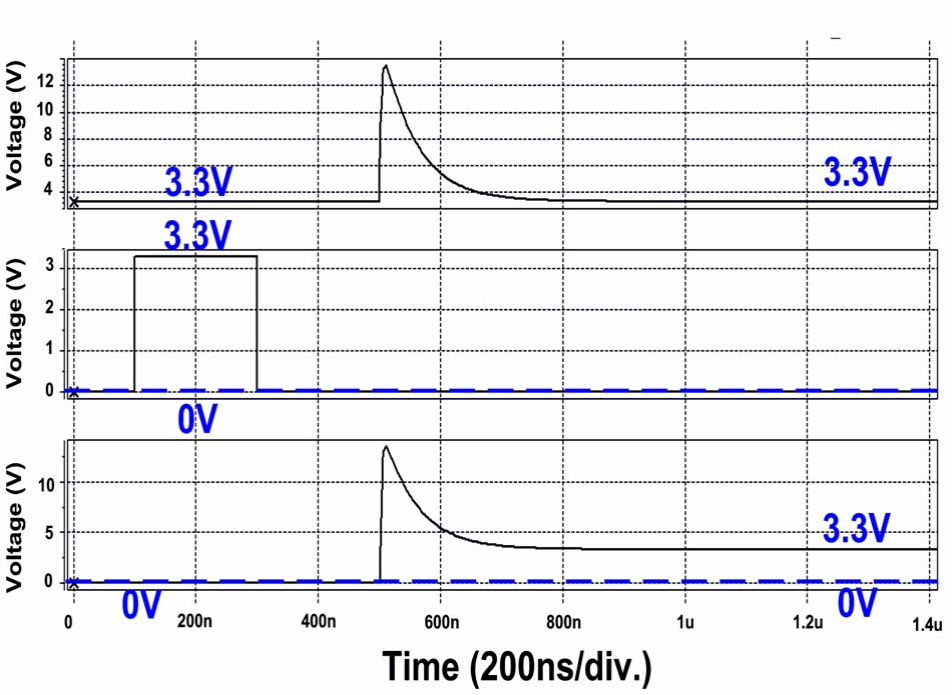


(a)

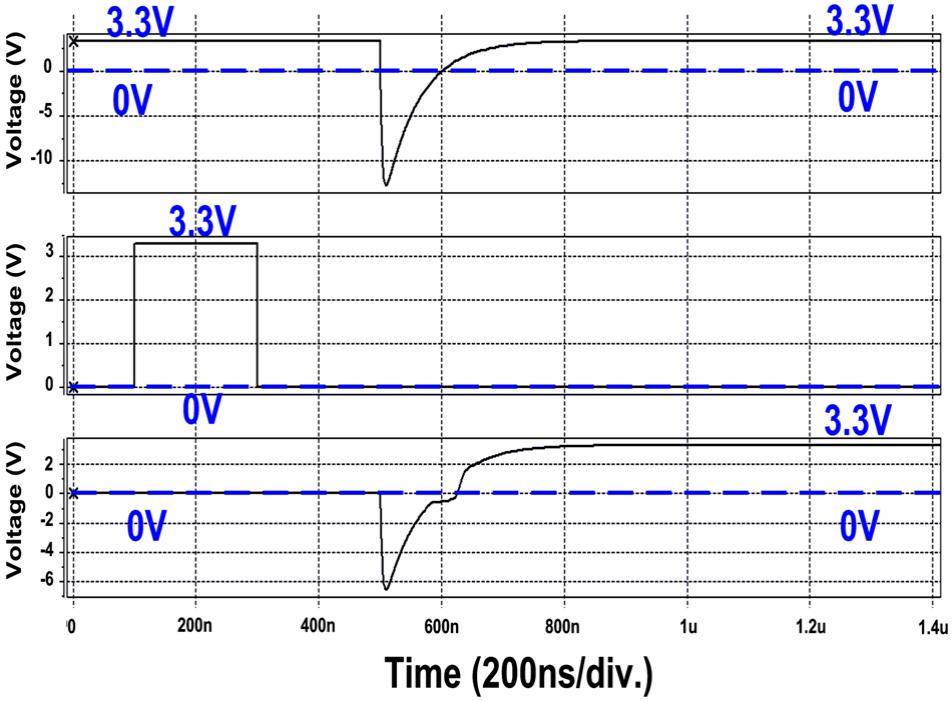


(b)

Fig. 2.15 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit II under (a) positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} with 5ns delay time and under (b) negative-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} with 5ns delay time.



(a)



(b)

Fig. 2.16 Simulated V_{DD}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit II under (a) positive exponential pulse on V_{DD} with amplitude of +15V and under (b) negative exponential pulse on V_{DD} with amplitude of -15V.

Chapter 3

Measurement Setup and Measurement Results of Transient Detection Circuits

3.1. Background

During system-level ESD tests, the high-energy ESD-induced noise on the power (V_{DD}) and ground (V_{SS}) lines often leads to frozen states or malfunction of the EUT. In the standard of IEC 61000-4-2, there are two kinds of test modes have been specified: contact-discharge test mode and air-discharge test mode. It is difficult to evaluate the immunity of "single" CMOS IC inside the EUT by using ESD gun under the system-level ESD tests, even though the IEC 61000-4-2 standard has been adopted as reliability test method of microelectronic products by most international companies. The quantity of energy induced by system-level ESD zapping is hard to evaluate in the experiments because of different box shielding and PCB layout designs applied on the microelectronic products. To solve this problem, a component-level transient induced latchup (TLU) test for system-level ESD consideration has been investigated [13]-[16]. In the measurement setup of TLU tests, the ESD trigger source can only apply the ESD-induced energy on the V_{DD} power line. Nevertheless, the measurement setup still can be used as an efficient method to investigate the system-level ESD immunity of CMOS IC. In this chapter, the new proposed on-chip transient detection circuits are fabricated in a 0.18-μm CMOS process with 3.3-V devices. The die photos of two proposed on-chip transient detection circuits are shown in Fig. 3.1 (a) and (b), respectively. The circuit performance of the circuits has been evaluated by TLU tests, system-level ESD tests, and EFT tests, respectively.

3.2. Transient Induced Latchup (TLU) Test

There are several advantages of the TLU tests. First, it can easily evaluate the immunity of "single" CMOS IC by the measured voltage/current waveforms through oscilloscope. Secondly, it can provide accurate simulation and high accuracy without over estimation for ESD-generated voltage disturbed on the CMOS ICs under system-level ESD tests. Through the TLU measurement setup, positive-going or negative-going underdamped sinusoidal voltages similar with the waveforms generated from ESD gun under system-level ESD tests can be provide by setting positive or negative charged voltage levels.

3.2.1. Measurement Setup

The measurement setup of TLU test is shown in Fig. 3.2 and 3.3. An electrostatic discharge simulator is used as a trigger source and it can generate the ESD-like energy to apply the underdamped sinusoidal voltage which is similar to the waveforms generated by ESD gun. A capacitor of 200pF is employed as the charging capacitor, as the same value used in machine model (MM) ESD test. This capacitor can store the energy (V_{charge}) generated from the electrostatic discharge simulator and then the stored charge can be discharged to the DUT through the relay. Therefore, by setting positive (negative) V_{charge} value, a positive-going (negative-going) underdamped sinusoidal voltage can be generated to simulate the transient disturbance on the power pins of CMOS ICs under system-level ESD test. Finally, the transient V_{DD} or I_{DD} waveforms can be measured through the digital oscilloscope with voltage and current probes. Noteworthiness, a 5Ω resistor is located between the DUT and power supply to avoid electrical-over-stress (EOS) damage on the DUT under a high current latchup state. In previous studies, the usage of a small current-limiting resistance, instead of a current-blocking diode is suggested in the TLU measurement setup in order to evaluate system-level ESD immunity of CMOS ICs [16].

3.2.2. Measurement Results of Transient Detection Circuit I

Fig. 3.4 (a) and (b) show the measured V_{DD} and V_{OUT} waveforms of the on-chip transient detection circuit I under TLU tests, respectively. The V_{DD} power line of the on-chip transient detection circuit I is disturbed with ESD-induced noise under TLU test. Therefore, the V_{DD} power line would not maintain its normal voltage level of 3.3V, but rapidly increase (decrease) from 3.3V under TLU test with positive (negative) V_{charge}. The V_{OUT} voltage level is simultaneously affected by the ESD-generated transient noise. Under TLU test with V_{charge} of +9V, a positive-going underdamped sinusoidal waveform can be generated on V_{DD} power line, as shown in Fig. 3.4 (a) Under TLU test with V_{charge} of -1V, a negative-going waveform can be generated on V_{DD} power line likewise, as shown in Fig 3.4 (b). After TLU tests with positive and negative V_{charge}, the output voltage level of on-chip transient detection circuit I can be changed from 0V to 3.3V.

3.2.3. Measurement Results of Transient Detection Circuit II

The measured V_{DD} and V_{OUT} waveforms of the on-chip transient detection circuit II under TLU tests with positive and negative V_{charge} are shown in Fig. 3.5 (a) and (b), respectively. Under TLU tests, the power line would not maintain its normal voltage, but an underdamped sinusoidal voltage instead. As shown in Fig. 3.5 (a), under positive ESD stress with V_{chage} of +11V, V_{DD} rapidly increases from 3.3V to a high peak voltage and the output is disturbed with the positive-going underdamped sinusoidal voltage waveform at the same time. After TLU test with positive V_{charge}, the output voltage level is changed from 0V to 3.3V. As shown in Fig. 3.5 (b), under negative ESD stress with V_{chage} of -3V, V_{DD} rapidly reduces from 3.3V to a low peak voltage and the output is disturbed with the negative-going underdamped sinusoidal voltage waveform simultaneously. After TLU tests with negative V_{charge}, the output voltage level is changed from 0V to 3.3V.

3.3. System-Level ESD Test

To evaluate the performance of electrical/electronic equipments when subjected to EMC regulations, performing the system-level ESD test for the electrical/electronic equipment is necessary. System-level ESD tests can judge whether the microelectronic products meet the immunity requirement in IEC 61000-4-2 standard. The immunity of microelectronic products against ESD-induced energy can be evaluated by system-level ESD tests. For example, to achieve the requirement of "level 4" defined in the IEC 61000-4-2 standard, a contact-discharge (air-discharge) test mode with ESD zapping voltage of ±8kV (±15kV) is the required voltage level. There are several test modes in the standard, such as direct contact-discharge, indirect contact-discharge, and air-discharge test mode. In the following measurement, the ESD gun is zapped on the edge of horizontal coupling plane (HCP) under system-level ESD tests with indirect contact-discharge mode, as shown in Fig. 3.6. Electromagnetic interference (EMI) energy coming from the ESD zapping is coupled to the CMOS ICs inside the DUT. The performance of the proposed on-chip transient detection circuits can be evaluated under system-level ESD tests with indirect contact discharge mode.

3.3.1. Measurement Setup

The measurement setup of system-level ESD tests clarified in the IEC 61000-4-2 international standard is shown in Fig. 3.6. The test environment consists of a wooden table standing on the ground reference plane (GRP). The connection from the earth cables to the GRP shall be low impedance path. The horizontal and vertical coupling planes for indirect discharge test mode are both connected to the GRP with two 470kΩ resistors in series. These resistors are used to avoid the ESD-induced energy conducts to the GRP without coupling to the DUT in indirect contact-discharge condition. In addition, an insulation sheet between the EUT and the HCP is placed on the table to separate the EUT from HCP. The ESD gun acts as the trigger source and the discharge return cable of the ESD gun shall be connected to the

GRP when the ESD energy is zapped to the DUT. The ESD gun should be able to generate at a repetition rate of twenty discharges per second at least for exploratory purposes only. The discharge return cable shall be sufficiently insulated to prevent the flow of the discharge current to conduct surfaces other than via its termination during system-level ESD tests. For conformance testing, the EUT shall be continually operated in its most sensitive mode. The transient response of the proposed on-chip transient detection circuits can be recorded and evaluated by using digital oscilloscope under system-level ESD tests. After system-level ESD zapping, the output voltage level of the proposed on-chip transient detection circuits can be recorded to verity the detection function.

3.3.2. Measurement Results of Transient Detection Circuit I

Under system-level ESD test with positive ESD voltage of +0.2kV, the measured V_{DD} and V_{OUT} waveforms of the proposed on-chip transient detection circuit I are shown in Fig. 3.7 (a). The power and ground lines of the on-chip transient detection circuit I are disturbed with ESD stress under system-level ESD tests. Therefore, V_{DD} (V_{SS}) line would not maintain its normal voltage level of 3.3V (0V), but rapidly increase from 3.3V (0V) under system-level ESD zapping with positive ESD voltage. Meanwhile, V_{OUT} is disturbed by such a high-energy ESD stress. The V_{DD}, V_{SS} and V_{OUT} voltage levels are simultaneously influenced by the ESD-induced transient noise. After system-level ESD tests with positive ESD voltage, V_{DD} and V_{SS} return to the original operation voltage level of 3.3V and 0V. Finally, the output voltage level of the on-chip transient detection circuit I can transit from 0V to 3.3V to memorize the occurrence of system-level ESD events.

Under system-level ESD test with negative ESD voltage of -0.2kV, the measured V_{DD} and V_{OUT} waveforms of the proposed on-chip transient detection circuit I are shown in Fig. 3.7 (b). The power and ground lines of the on-chip transient detection circuit I are disturbed with ESD stress under system-level ESD tests. During the negative-going fast electrical

transients on the V_{DD}/V_{SS} lines, V_{DD} and V_{OUT} are disturbed simultaneously by such a high-energy ESD stress. After system-level ESD tests with negative ESD voltage, V_{DD} and V_{SS} return to the normal operation voltage level of 3.3V and 0V. The output voltage level of transient detection circuit I can transit from 0V to 3.3V to memorize the occurrence of system-level ESD events.

3.3.3. Measurement Results of Transient Detection Circuit II

The measurement setup shown in Fig. 3.6 is used to verify the performance of the proposed on-chip transient detection circuit II. Fig. 3.8 (a) shows the measured V_{DD} and V_{OUT} waveforms of the transient detection circuit II under system-level ESD test with positive ESD voltage of +0.2kV. The V_{DD} voltage rapidly increases from 3.3V to a high peak voltage owing to the disturbance of system-level ESD zapping. During the positive-going underdamped sinusoidal transient disturbance on the V_{DD} power lines, V_{DD} and V_{OUT} are influenced at the same time. Finally, while V_{DD} returns to 3.3V, the output of on-chip transient detection circuit II can be changed from 0V to 3.3V.

Fig. 3.8 (b) shows the measured V_{DD} and V_{OUT} waveforms of the transient detection circuit II under system-level ESD test with negative ESD voltage of -0.2kV. The V_{DD} voltage rapidly decreases from 3.3V to a low peak voltage owing to the disturbance of system-level ESD zapping. During the negative-going underdamped sinusoidal transient disturbance on the V_{DD} power lines, V_{DD} and V_{OUT} are influenced at the same time. Finally, while V_{DD} returns to 3.3V, the output of on-chip transient detection circuit II can be changed from 0V to 3.3V.

3.4. EFT Test

3.4.1. Measurement Setup

In order to simulate the EFT-induced transient disturbance on the CMOS ICs inside the microelectronic products, the attenuation network with 200dB degradation is used in this

work. The measurement setup for EFT tests combined with attenuation network is shown in Fig. 3.9. The EFT generator is connected to the EUT through the attenuation network. The V_{DD} and V_{OUT} transient responses of the on-chip transient detection circuits can be monitored by the digital oscilloscope. Thus, the influences on power lines and the transient detection function under EFT tests can be directly evaluated with the measurement setup of EFT test with attenuation network.

3.4.2. Measurement Results of Transient Detection Circuit I

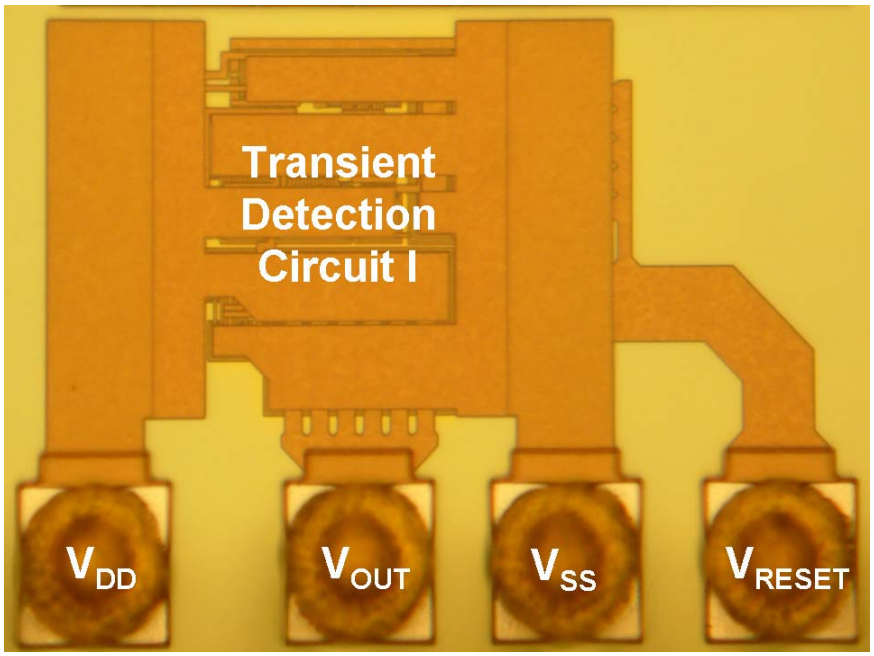
Fig. 3.10 (a) and (b) show the measured transient waveforms of V_{DD} and V_{OUT} of transient detection circuit I under positive and negative EFT tests, respectively. Before each EFT voltage zapping, the initial output voltage (V_{OUT}) of the proposed on-chip transient detection circuit I is reset to 0V. During the EFT tests with positive and negative EFT voltage, V_{DD} and V_{OUT} of the transient detection circuit I are disturbed simultaneously with the exponential voltage waveforms. Thus, V_{DD} increases (decreases) rapidly from its initial value of 3.3V under positive (negative) EFT tests. After EFT tests with attenuation network, the output voltage of the transient detection circuit I transits from 0V to 3.3V.

3.4.3. Measurement Results of Transient Detection Circuit II

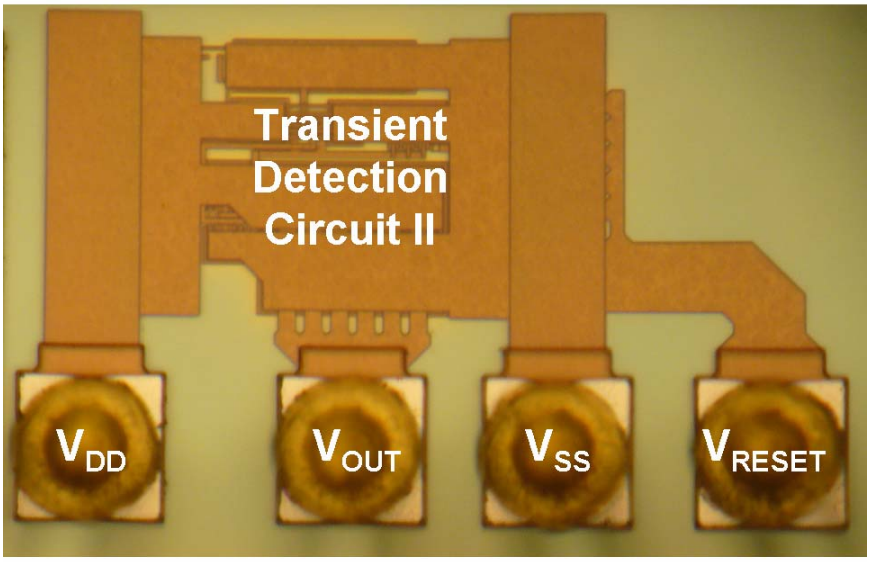
Fig. 3.11 (a) and (b) show the measured transient waveforms of V_{DD} and V_{OUT} of transient detection circuit II under positive and negative EFT tests, respectively. Before each EFT voltage zapping, the initial output voltage (V_{OUT}) of the proposed on-chip transient detection circuit II is reset to 0V. During the EFT tests with positive and negative EFT voltage, V_{DD} and V_{OUT} of the transient detection circuit II are disturbed simultaneously with the exponential voltage waveforms. Thus, V_{DD} increases (decreases) rapidly from its initial value of 3.3V under positive (negative) EFT tests. After EFT tests combined with attenuation network, the output voltage of the transient detection circuit II transits from 0V to 3.3V.

3.5. Conclusion

The two new proposed on-chip transient detection circuits have been fabricated in a 0.18-μm CMOS process with 3.3-V devices. These circuits have been investigated and designed with the HSPICE simulator tool. Three test methods including TLU test, system-level ESD test, and EFT test are adopted to verify the circuit performance of proposed on-chip transient detection circuits. From the experimental results, the outputs of two transient detection circuits can transit from 0V to 3.3V after voltage zapping. Therefore, it has been confirmed that the transient detection circuits can detect and memory the occurrence of the positive (negative) fast electrical transients on the power and ground lines of CMOS ICs.



(a).



(b)

Fig. 3.1 Die photos of (a) transient detection circuit I and (b) transient detection circuit II.

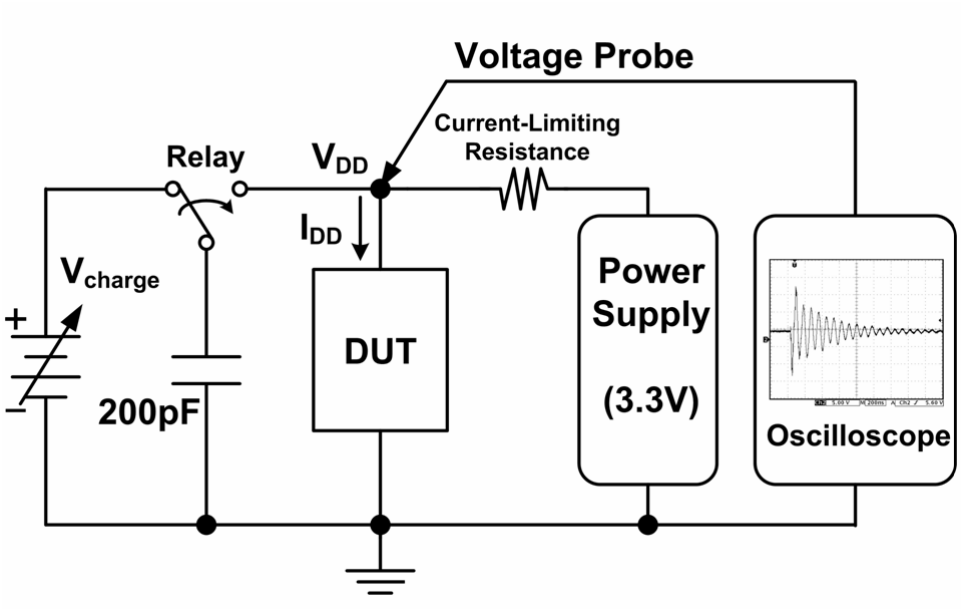


Fig. 3.2 Measurement setup of component-level transient induced latchup (TLU) test.

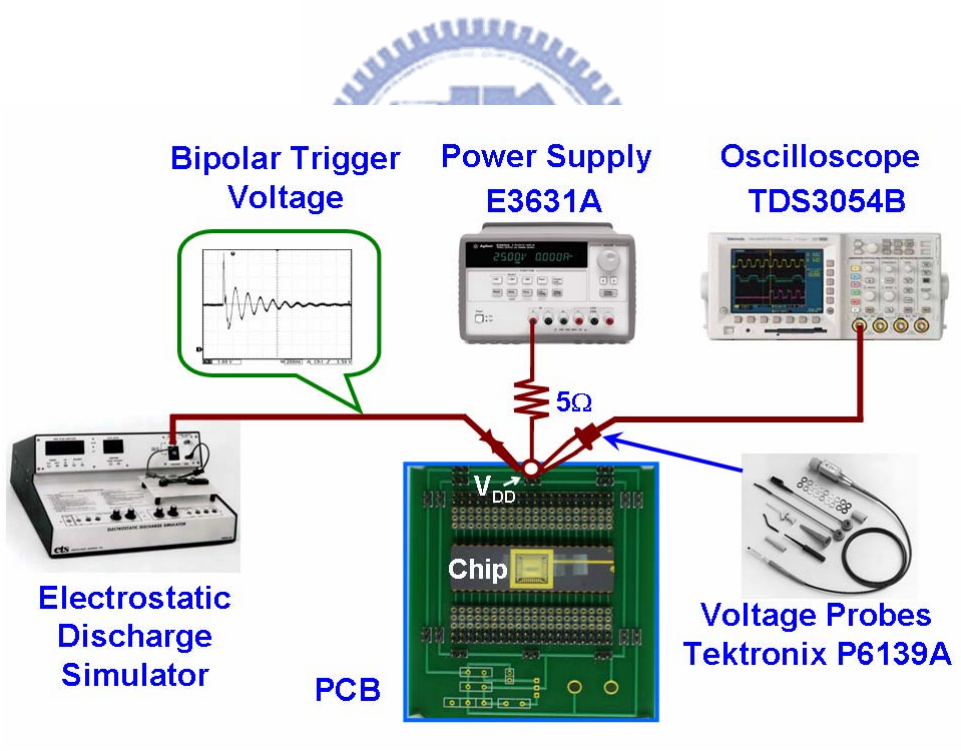
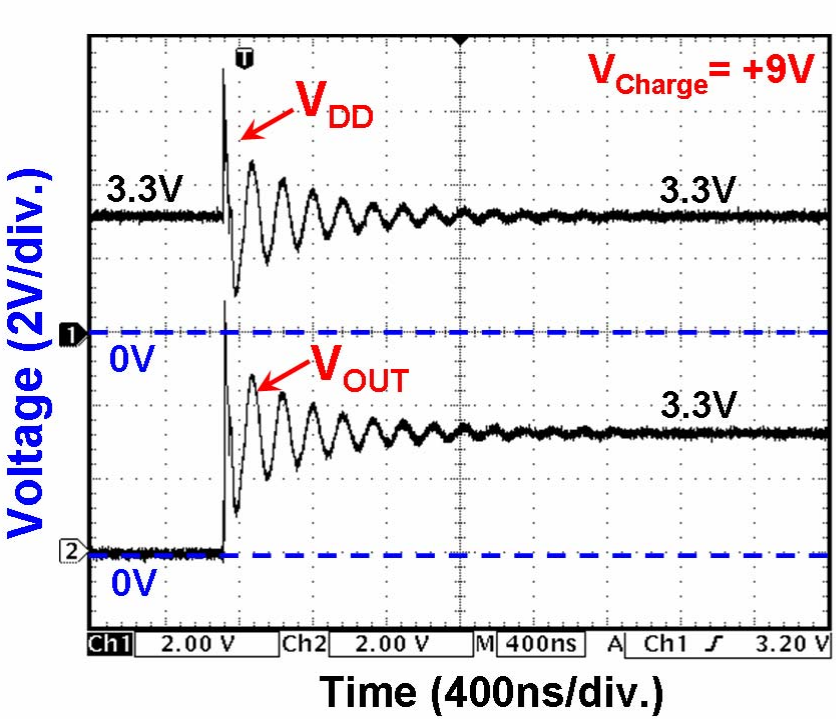
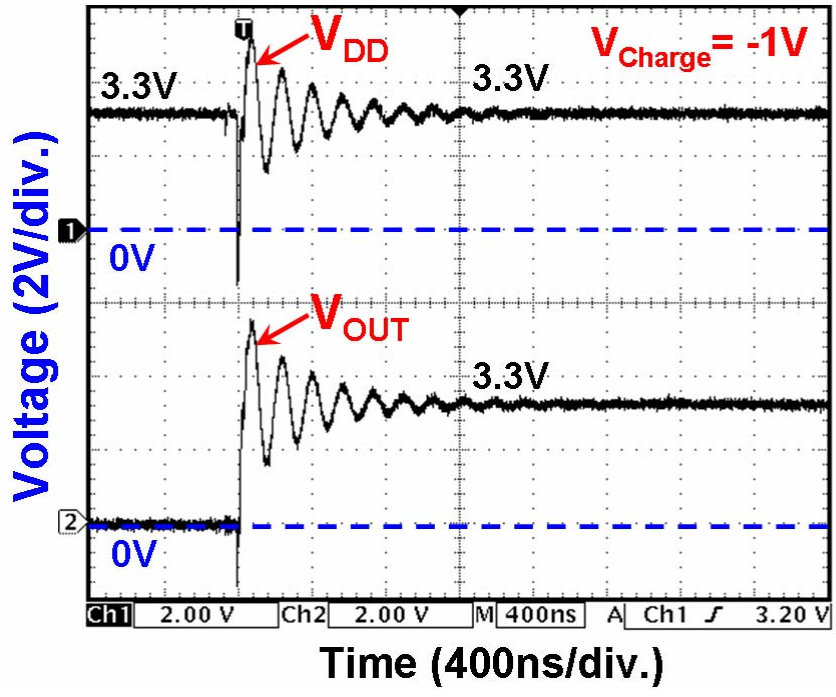


Fig. 3.3 Measurement instruments of component-level transient induced latchup (TLU) test.

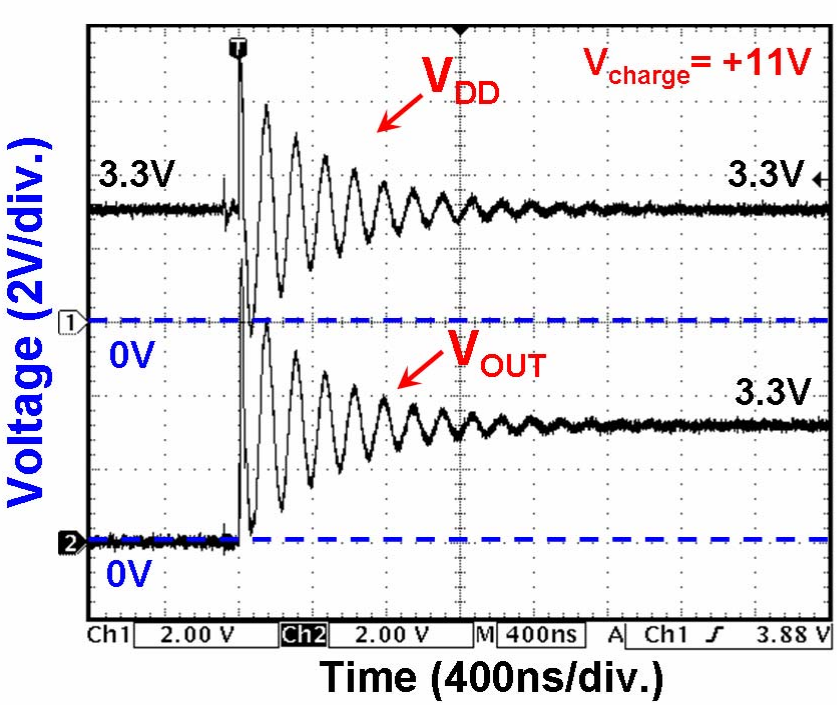


(a)

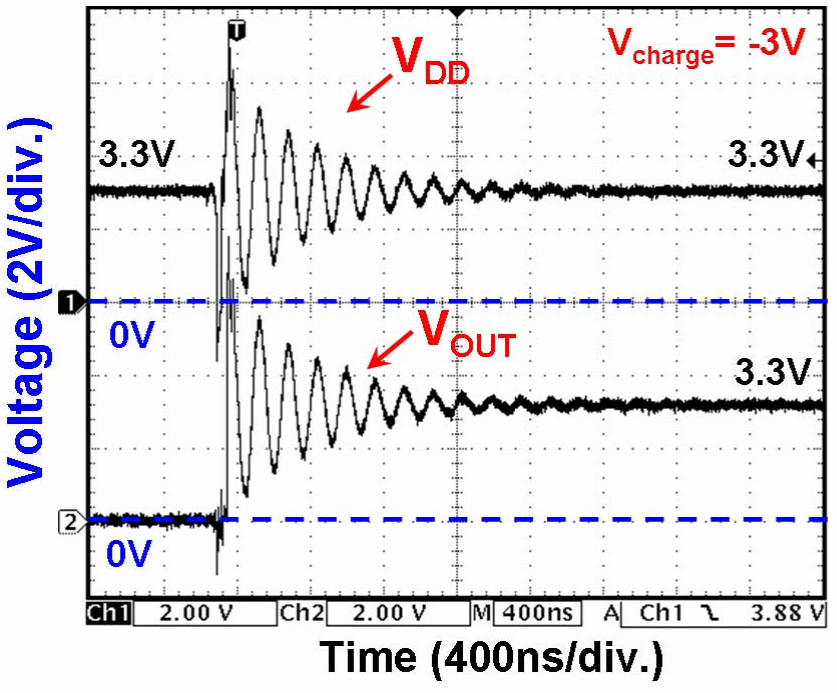


(b)

Fig. 3.4 Measured V_{DD} and V_{OUT} transient responses on the proposed on-chip transient detection circuit I under TLU test with (a) V_{charge} of +9V and (b) with V_{charge} of -1V.



(a)



(b)

Fig. 3.5 Measured V_{DD} and V_{OUT} transient responses on the proposed on-chip transient detection circuit II under TLU test with (a) V_{charge} of +11V and with (b) V_{charge} of -3V.

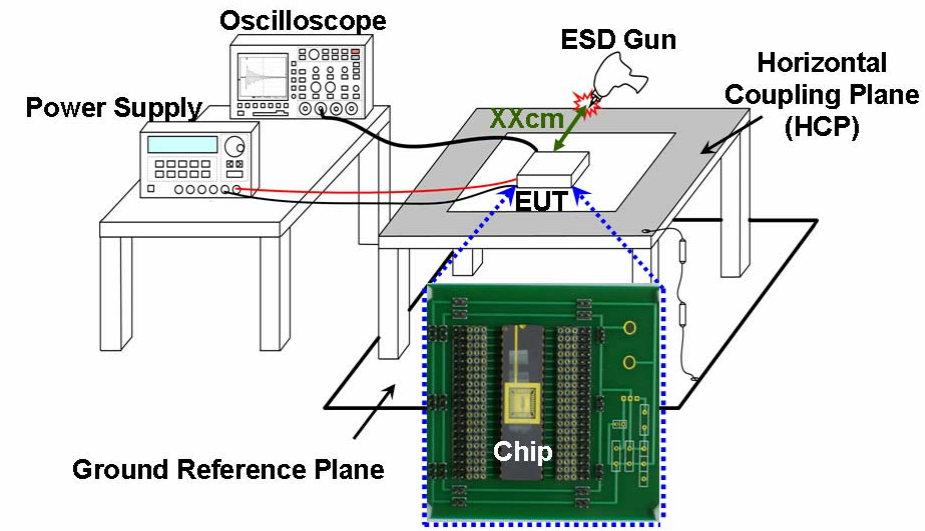
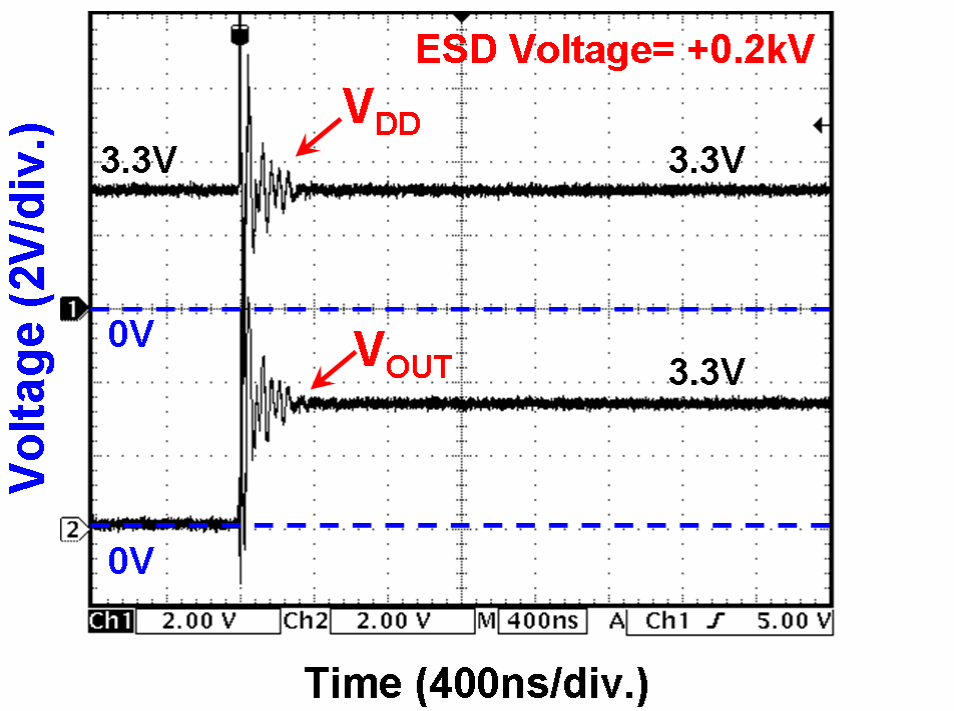
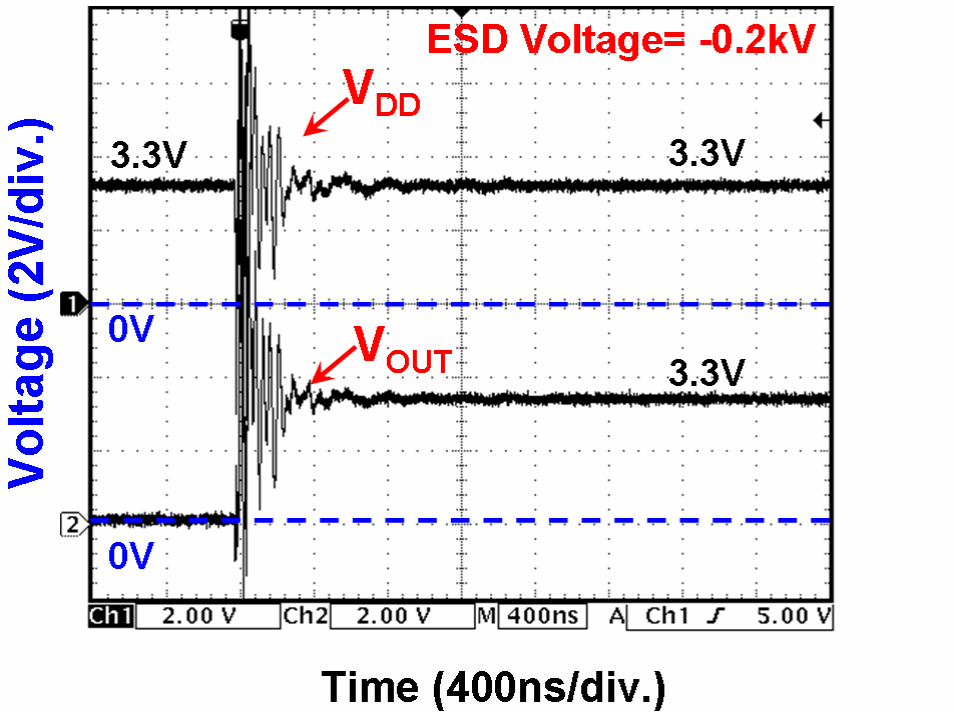


Fig. 3.6 Measurement setup of system-level ESD test with indirect contact discharge mode.

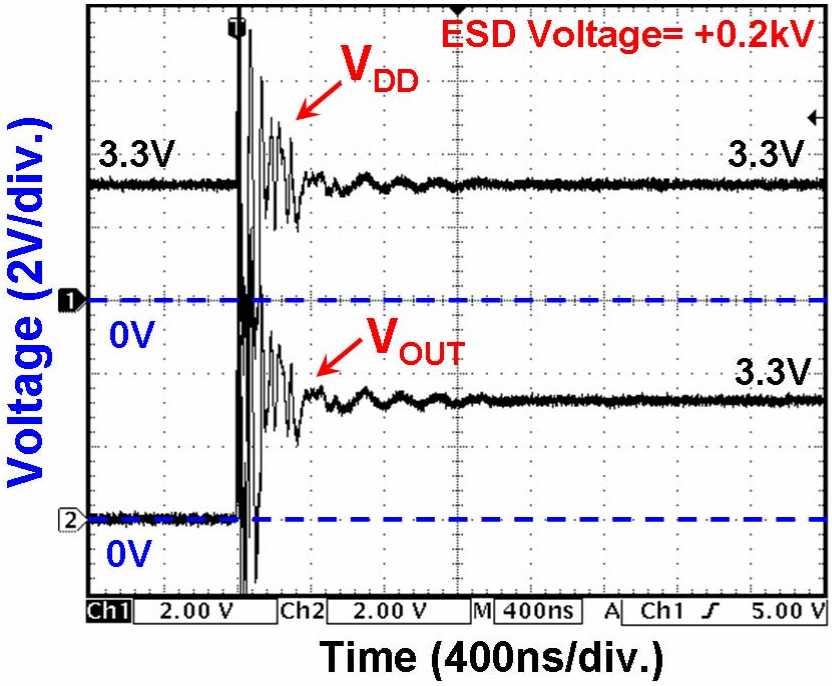


(a)

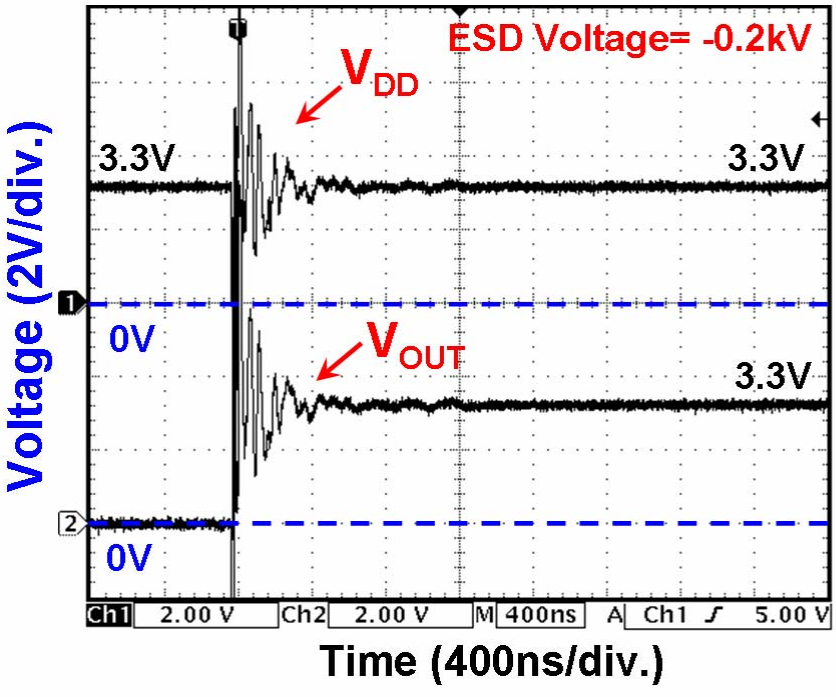


(b)

Fig. 3.7 Measured V_{DD} and V_{OUT} transient responses on the proposed on-chip transient detection circuit I under system-level ESD test with (a) ESD voltage of +0.2kV and with (b) ESD voltage of -0.2kV.



(a)



(b)

Fig. 3.8 Measured V_{DD} and V_{OUT} transient responses on the proposed on-chip transient detection circuit II under system-level ESD test with (a) ESD voltage of +0.2kV and with (b) ESD voltage of -0.2kV.

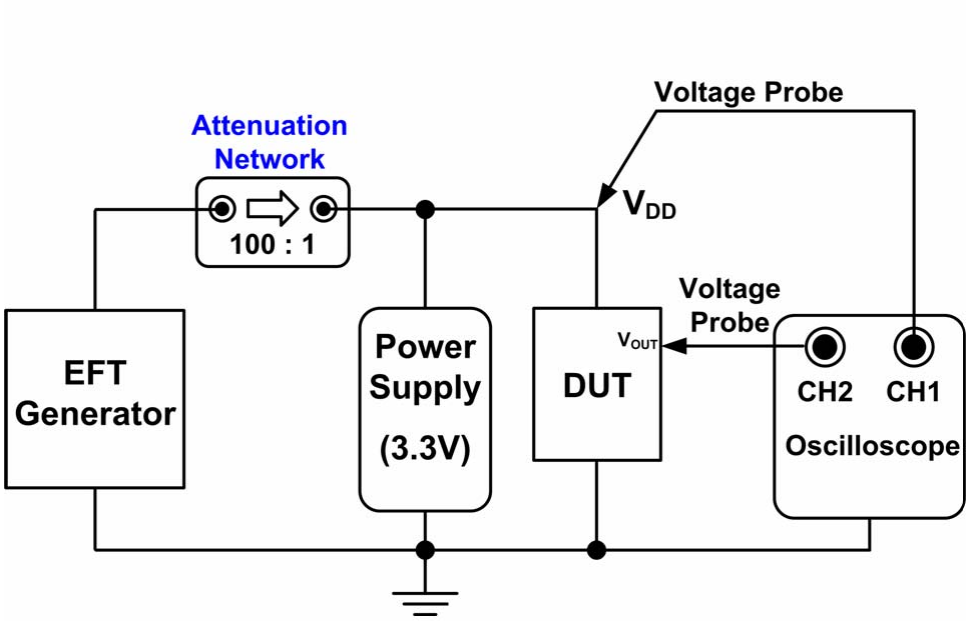
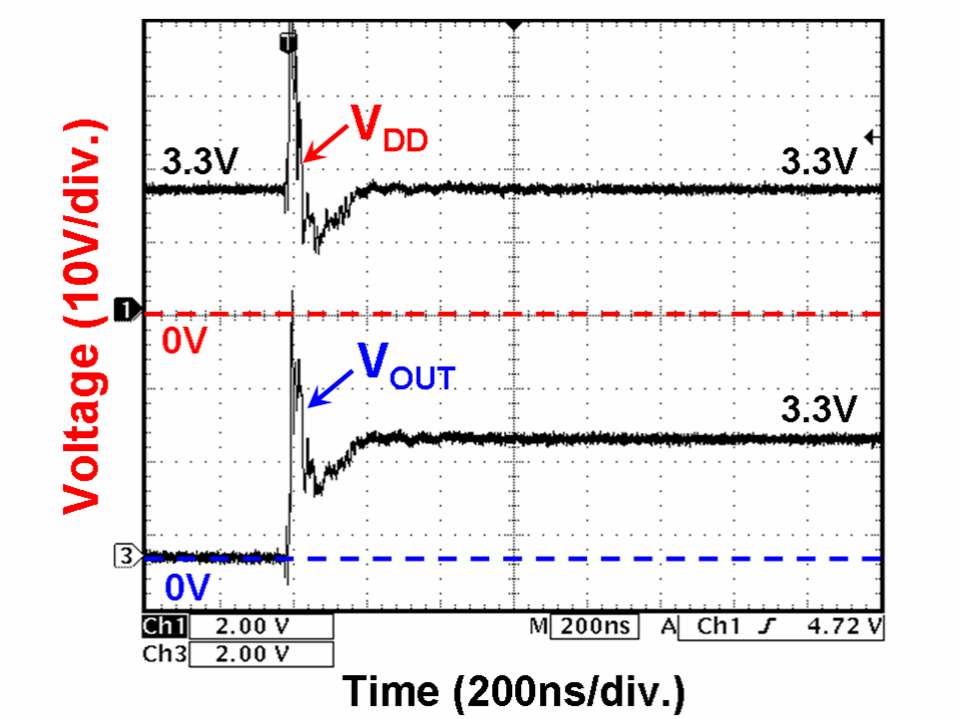
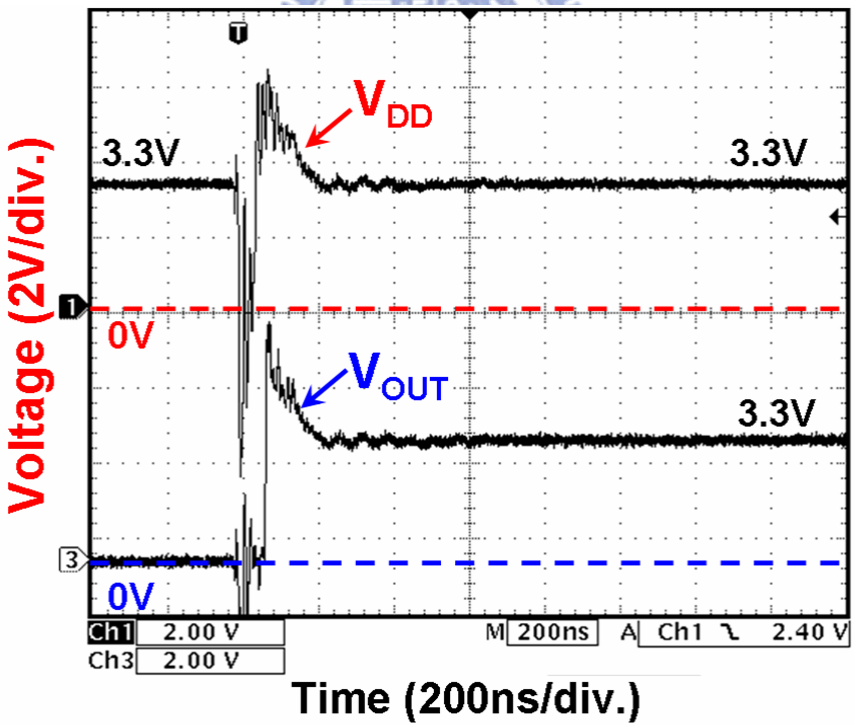


Fig. 3.9 Measurement setup of EFT test combined with attenuation network.

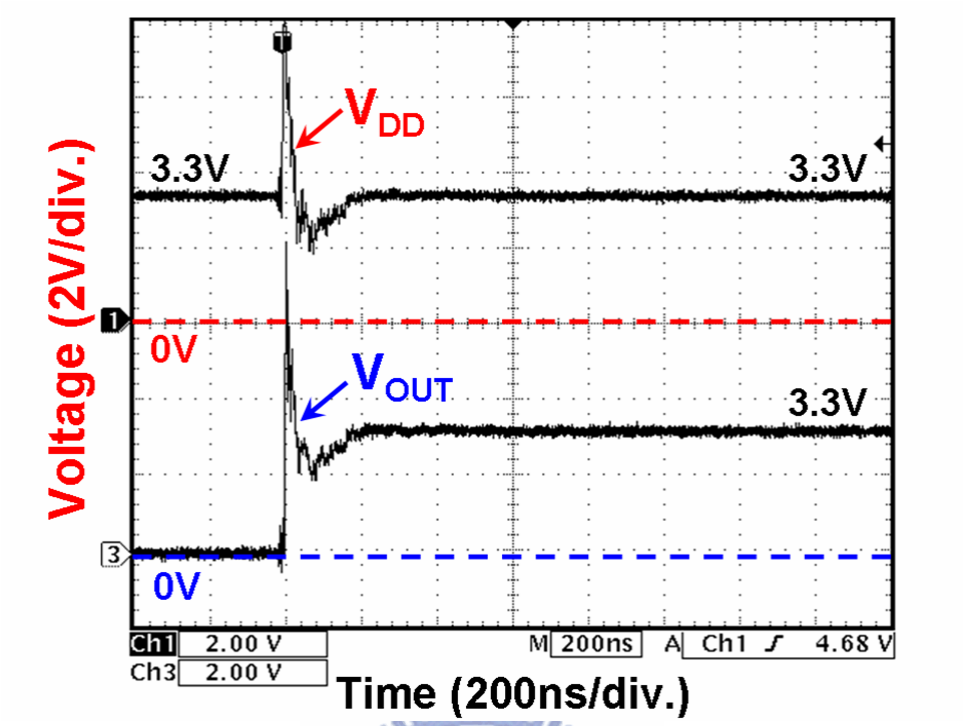


(a)

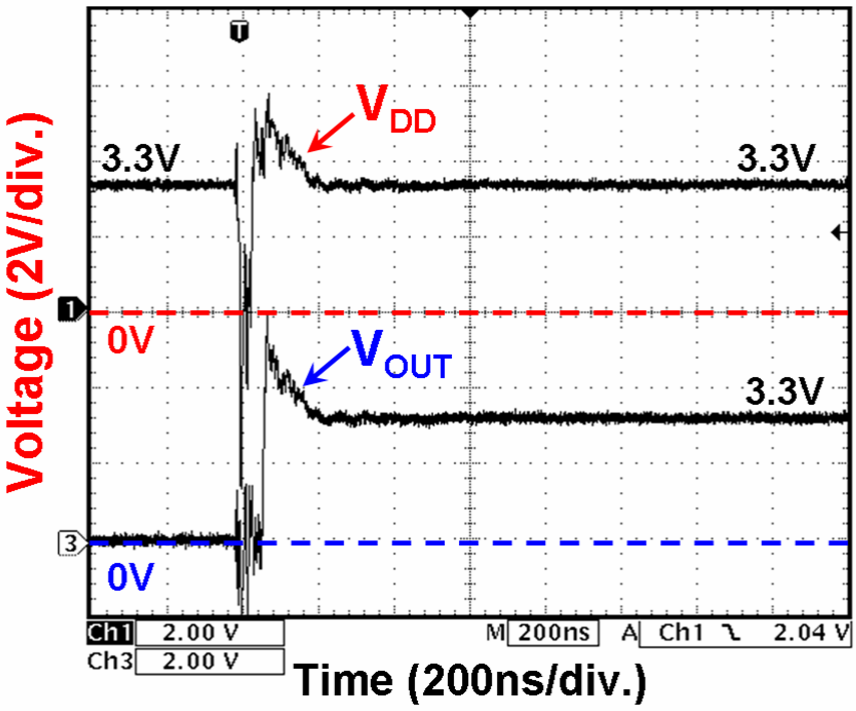


(b)

Fig. 3.10 Measured V_{DD} and V_{OUT} transient responses on the proposed on-chip transient detection circuit I under EFT test with (a) positive EFT voltage and with (b) negative EFT voltage.



(a)



(b)

Fig. 3.11 Measured V_{DD} and V_{OUT} transient responses on the proposed on-chip transient detection circuit I under EFT test with (a) positive EFT voltage and with (b) negative EFT voltage.

Chapter 4

Evaluation on Transient Detection Circuit with Board-Level Noise Filter Networks

4.1. Background

It has been reported that, by choosing proper components in the board-level noise filters, the ESD immunity of CMOS ICs can be significantly enhanced under system-level ESD tests [10]. The usage of board-level noise filters between the noise source and CMOS ICs can decouple, bypass, or absorb noise voltage (energy) such as bi-polar transient waveform. "Bi-polar" waveform means that the polarity of the voltage waveform can be varied between positive and negative with time repeatedly. The bi-polar transient waveforms are similar with the underdamped sinusoidal waveforms disturbed on the power and ground lines under system-level ESD tests. The domain parameters of the bi-polar transient waveform disturbed on the power and ground lines of CMOS ICs under system-level ESD tests include frequency, damping factor, and transient peak voltage. According to the previous investigations on board-level noise filters, the purpose of this chapter is to develop an effective board-level noise filter network to reduce the ESD energy zapped into the DUT under system-level ESD tests. Different types of board-level noise filters have been evaluated to find their improvement on reducing ESD-induced energy, including capacitor filter, LC-like (2^{nd}-order) filter, π-section (3^{rd}-order) filter, etc. These noise filters can be used to appropriately improve the ESD immunity of DUT under system-level ESD tests. Some board-level noise filters can be even integrated into the chip design to further achieve the system-on-chip (SOC) design and reduce the cost of microelectronic products. Furthermore, the proposed on-chip transient detection circuits have been verified in a 0.18-μm technology with 3.3-V devices successfully. Under system-level ESD tests, the proposed on-chip transient detection circuits can detect and

memorize the occurrence of the fast electrical transients disturbance on the power and ground lines of CMOS ICs. Therefore, board-level (chip-level) noise filters with proper components can reduce high ESD energy zapped into the proposed on-chip transient detection circuits.

4.2. Different Types of Board-Level Noise Filters to Suppress Bi-Polar Trigger Waveform under System-Level ESD Test

During system-level ESD tests, the bi-polar transient voltages (underdamped sinusoidal waveforms) disturbed on the V_{DD}/V_{SS} lines of CMOS ICs inside the EUT often cause malfunction or hardware damage of microelectronic products. It has been reported that the different types of board-level noise filter network can impact the dominant parameters of bi-polar transient voltage, such as transient peak voltage, frequency and damping factor, by suppress the ESD-induced voltage efficiently [10], [17]. Therefore, four types of board-level noise filters have been investigated in this section and the experimental measurement results are shown below. The measurement setup combined noise filter network with TLU test measurement instruments is shown in Fig. 4.1.

Four types of noise filter networks: capacitor filter, π-section filter, type-I RC filter, and type-II RC filter are depicted in Fig. 4.2(a), Fig. 4.2(b), Fig. 4.2(c), and Fig. 4.2(d), respectively. The TLU test is adopted to evaluate the ESD immunity enhancement of different board-level noise filter networks. The TLU tests have advantage of providing similar ESD-induced disturbed voltage waveforms on V_{DD}/V_{SS} lines of CMOS ICs under system-level ESD tests. The TLU test method can avoid overestimation for ESD-induced disturbance during system-level ESD tests. In this work, different board-level noise filter networks are located between ESD trigger source and DUT in order to investigate the ESD immunity against ESD-induced energy.

4.3. Evaluate the Effectiveness of On-Chip Transient Detection Circuit with Board-Level Noise Filter Networks

In Fig. 4.3, decoupling capacitances widely ranging from 1pF to 0.1μF are investigated the system-level ESD detection level of the on-chip transient detection circuit with different board-level noise filters. The definition of system-level ESD detection level is that minimum ESD voltage can cause transition at the output of on-chip transient detection circuit from 0V to 3.3V. Due to TLU test is the adopted measured method in this work, the system-level ESD detection level is expressed as V_{Charge}. Furthermore, the system-level ESD detection level is dependent on the voltage level zapped into the CMOS ICs inside the DUT. For proposed on-chip transient detection circuits, the combined different noise filter networks can provide different abilities to reduce ESD-induced disturbance on V_{DD}/V_{SS} lines and cause the detection function triggered under different ESD zapping voltages. In the following analyses, different types of board-level noise filters combined with the new proposed on-chip transient detection circuit I shown in Fig. 2.6 have been investigated. Fig. 4.3 shows the relations between the decoupling capacitance of the capacitor and system-level ESD detection level of the proposed on-chip transient detection circuit I under TLU tests. As shown in Fig. 4.3, larger capacitance of decoupling capacitor responses to higher system-level ESD detection level. By using larger decoupling capacitor in noise filter networks, the higher ESD-induced energy must be zapped into the DUT to trigger on the detection function of proposed on-chip transient detection circuit. Therefore, for the on-chip transient detection circuit, the system-level ESD detection level can be adjusted by combining different noise filter networks.

Fig. 4.4 shows the measurement results of proposed on-chip transient detection circuit I combined with 3rd-order π-section noise filter network shown in Fig. 4.2 (b) under TLU tests. There are two different resistances of 5Ω and 100Ω used in the 3rd-order noise filter network, and both the board-level noise filters are measured and analyzed under TLU tests. From the

measured results shown in Fig. 4.4, larger decoupling capacitance responses to higher system-level ESD detection level (V_{charge}). For example, by using π-section noise filter consisting of a 100Ω resistor and two 0.1μF capacitors, the positive system-level ESD detection level (V_{charge}) can be enhanced more than +400V. Furthermore, in this work, a 5Ω resistor and a 100Ω resistor are used in the 3rd-order π-section noise filters with the same capacitance of capacitor, respectively. The π-section noise filter with the 100Ω resistance can provide higher system-level ESD detection level than that with 5Ω resistance.

For the proposed on-chip transient detection circuit I combined with the board-level 2nd-order RC noise filter network, Fig. 4.5 shows the measurement results of the system-level ESD detection level. Two kinds of RC noise filters are used to verify the performance of suppressing the ESD-generated voltage under TLU tests. For two RC noise filters, one consists of a 5Ω resistor, and the other consists of a 100Ω resistor. The decoupling capacitances are the same in both RC noise filters. The capacitances widely ranging from 1pF to 0.1μF are used to investigate the system-level ESD detection level of the on-chip transient detection circuit combined with RC noise filters. From the measured results shown in Fig. 4.5, the efficiency of RC noise filter with 100Ω resistor to against the ESD-induced noise is better than that with 5Ω resistor. If the resistance is fixed, the larger capacitance of the capacitor used in the RC noise filter network will response to the higher system-level ESD detection level (V_{charge}), as shown in Fig. 4.5.

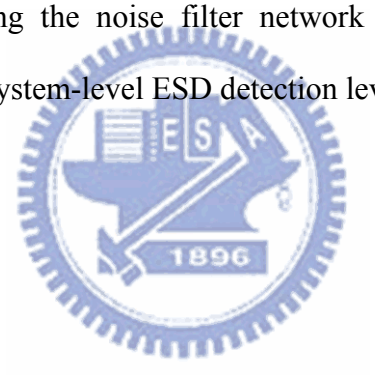
In order to reduce the capacitance used in the RC noise filter networks, a modified noise filter network shown in Fig.4.2 (d) is proposed. The original RC noise filter shown in Fig. 4.2(c) is named as type-I RC noise filter, and the modified noise filter is named as type-II RC noise filter. For the same RC time constant, the capacitance of the capacitor in the type-II RC noise filter can be reduced due to two resistors used in the type-II RC noise filter. That is, the capacitance of type-I RC noise filter would be larger than that in type-II RC noise filter for the same RC time constant. Furthermore, V_{DD}/V_{SS} lines of CMOS ICs would be disturbed

simultaneously under system-level ESD tests. The resistor located between V_{SS} line and ESD trigger source is needed to against the ESD-induced energy coupled on V_{SS} line. Fig. 4.6 shows the system-level ESD detection level characteristics of the on-chip transient detection circuit combined with type-II RC noise filter under TLU tests. Two capacitances (10pF and 100pF) are used in the type-II RC noise filter network, separately. The system-level ESD detection level is strongly dependent on the capacitance of the capacitor used in the type-II RC noise filter while the resistance is fixed. In addition, the larger resistance used in type-II filter can cause higher system-level ESD detection level. Compared with the measured results in Fig. 4.5 and Fig. 4.6, the type-I RC noise filter consisted with 5Ω resistance and 600pF capacitance response to 15-V system-level ESD detection level (V_{charge}), but the type-II RC noise filter consisted with 150Ω resistance and only 10pF capacitance can achieve approximate level. Therefore, type-II RC noise filter can reduce the capacitance on the RC noise filters, no matter for positive and negative V_{charge} under TLU tests. Such board-level type-II RC noise filter can be further integrated into chip design to effectively enhance the system-level ESD detection level of CMOS ICs.

4.4. Conclusion

By choosing proper noise filter networks, the ESD-induce energy (voltage) zapped into the CMOS ICs inside the EUT can be suppressed effectively. The performance of different type noise filters against the ESD-induced transient noise have been measured and analyzed under TLU tests. The 3rd-order π-section noise filter networks can enhance the system-level ESD detection level of on-chip transient detection circuit better than the 2nd-order type-I RC noise filter under TLU tests. Otherwise, the type-I RC noise filter can enhance the detection level more efficiently than the 1st-order noise filter. The compared measurement results among different type noise filter networks are shown in Fig. 4.7. For different noise filter networks, capacitances widely ranging from 1pF to 0.1μF are investigated the system-level

ESD detection range of the on-chip transient detection circuit. The higher order of noise filters can more effectively enhance system-level ESD detection level, no matter for positive or negative ESD events. Therefore, the board-level noise filters can be combined with the proposed on-chip transient detection circuit to adjust the system-level ESD detection range. Fig. 4.8 (a) and (b) show the measured V_{DD} and V_{OUT} waveforms under positive and negative TLU tests with V_{Charge} of +9V and -1V, respectively. In the TLU tests, the on-chip transient detection circuit I is combined with noise filter network. The measured results shown in Fig. 4.8 (a) and (b) can be compared with transient waveforms shown in Fig. 3.4 (a) and (b). Because noise filter network can effectively suppress the ESD-generated energy, the output voltage of transient detection circuit still maintains at 0V under TLU tests with the same V_{charge}. Therefore, by combining the noise filter network properly, the on-chip transient detection circuit can adjust the system-level ESD detection level.



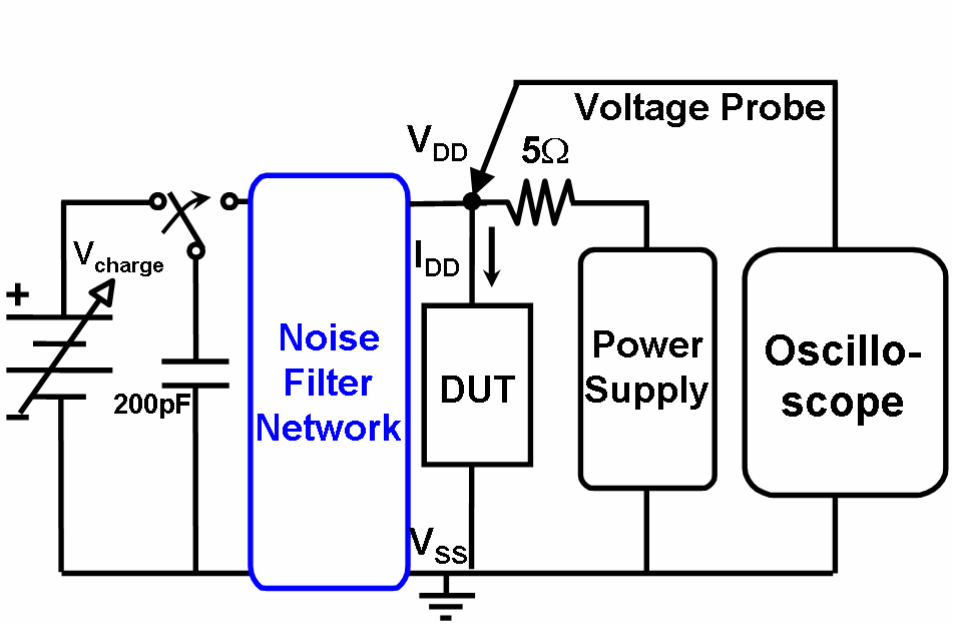


Fig. 4.1 Modified measurement setup of component-level transient induced latchup (TLU) test.

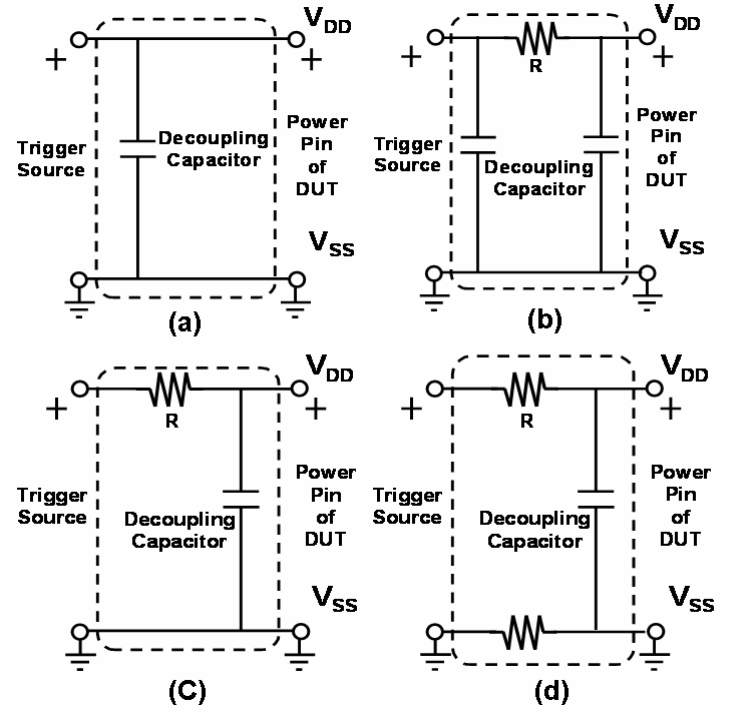


Fig. 4.2 Four types of noise filter networks investigated for their improvement on system-level ESD detection level: (a) capacitor filter, (b) π-section filter, (c) type-I RC filter, and (d) type-II RC filter.

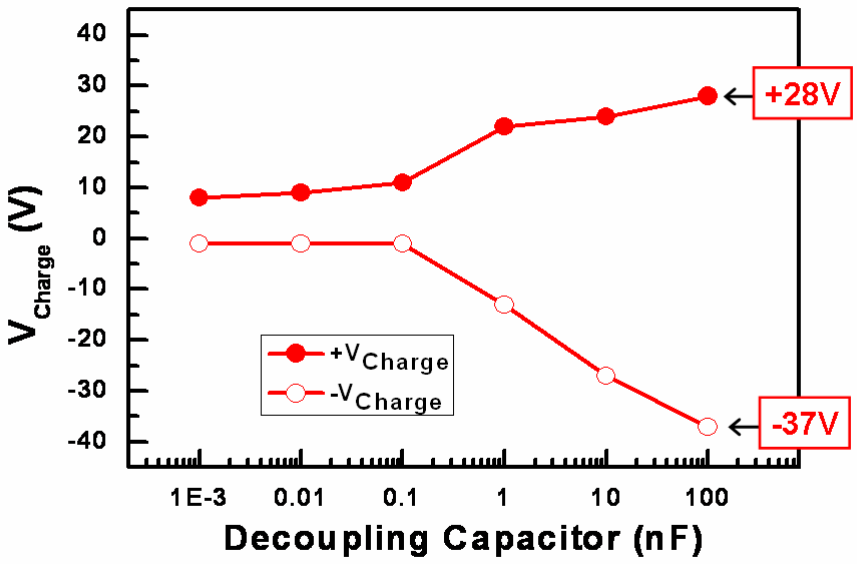


Fig. 4.3 Relations between the decoupling capacitance of the capacitor filter and system-level ESD detection level (V_{charge}) of the proposed transient detection circuit under both positive and negative TLU test.

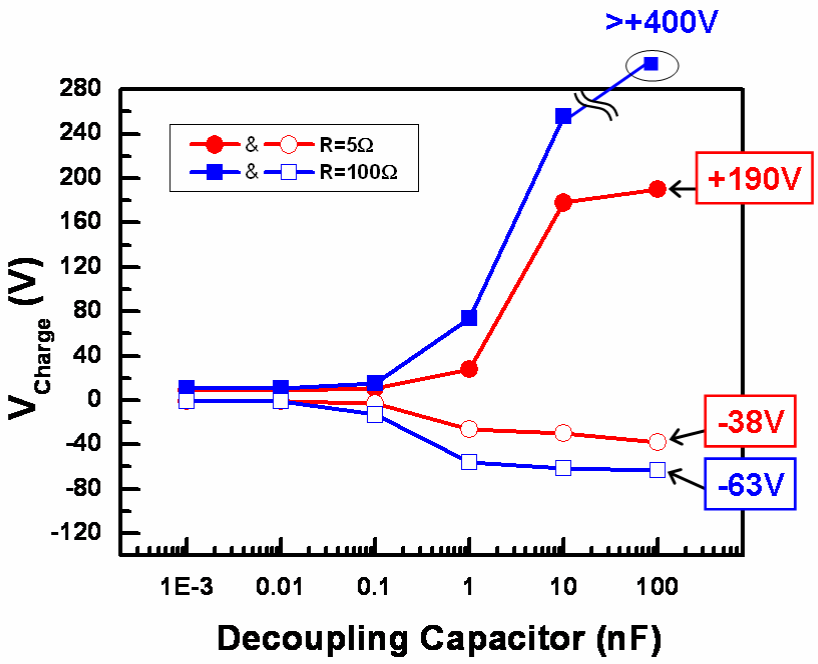


Fig. 4.4 Relations between the decoupling capacitance of the π-section filter and system-level ESD detection level (Vcharge) of the proposed transient detection circuit under both positive and negative TLU test.

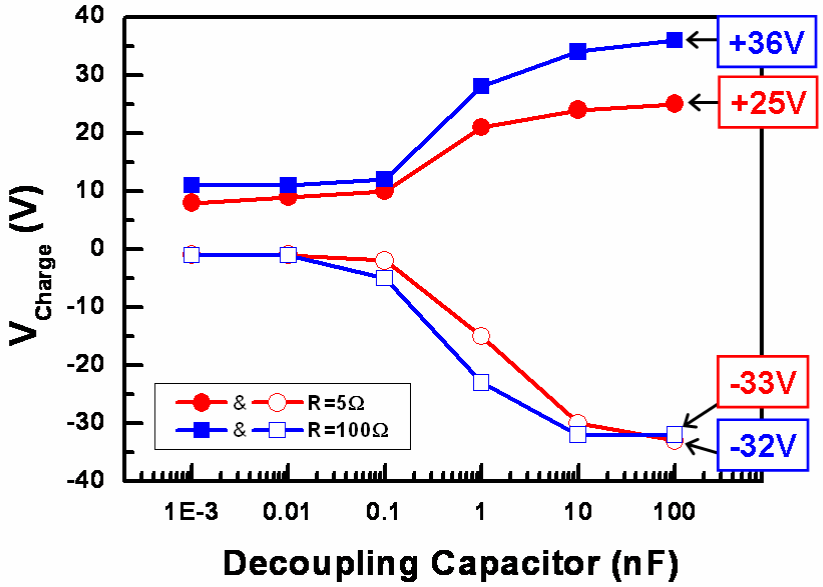


Fig. 4.5 Relations between the decoupling capacitance of the type-I RC filter and system-level ESD detection level (V_{charge}) of the proposed transient detection circuit under both positive and negative TLU test.

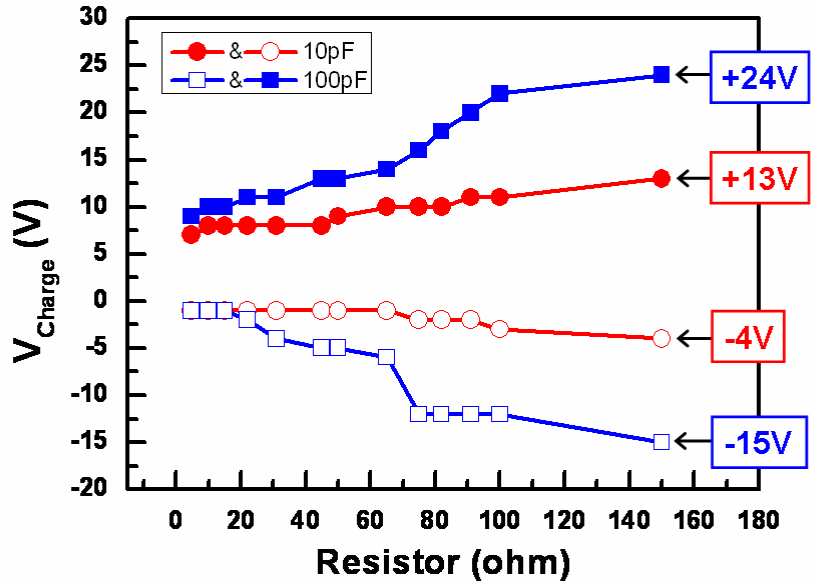


Fig. 4.6 Relations between the resistance of the type-II RC filter and system-level ESD detection level (V_{charge}) of the proposed transient detection circuit under both positive and negative TLU test.

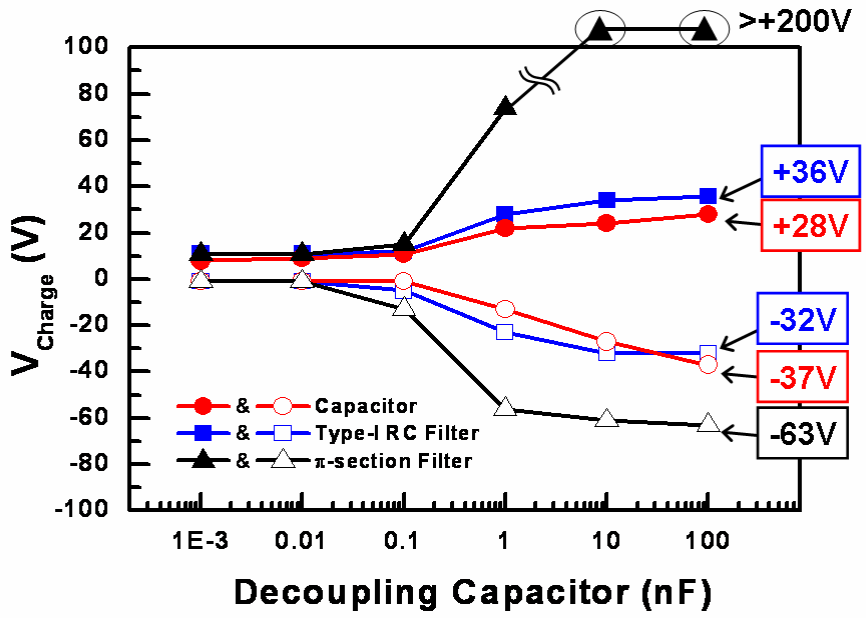
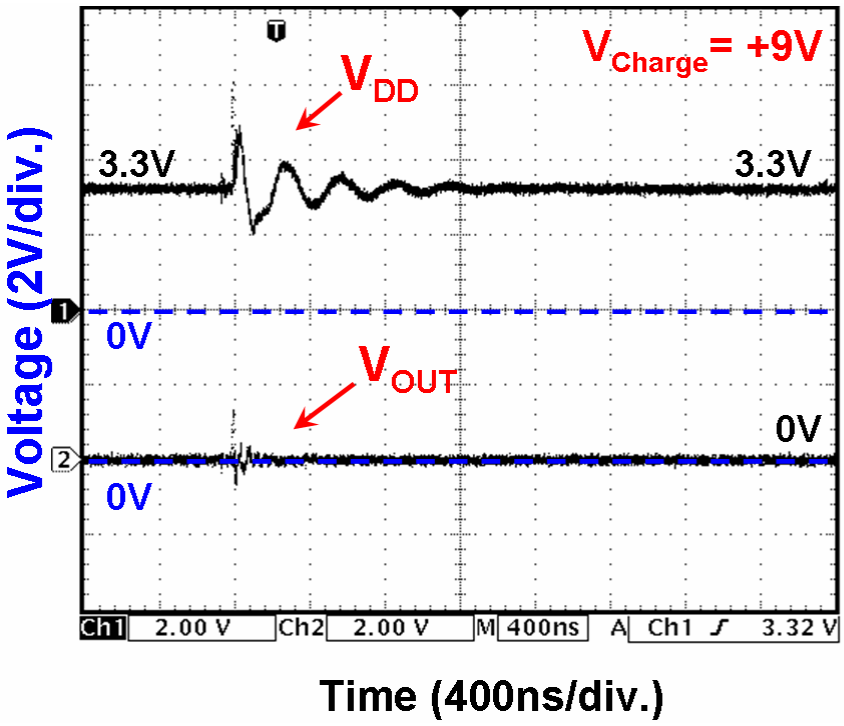
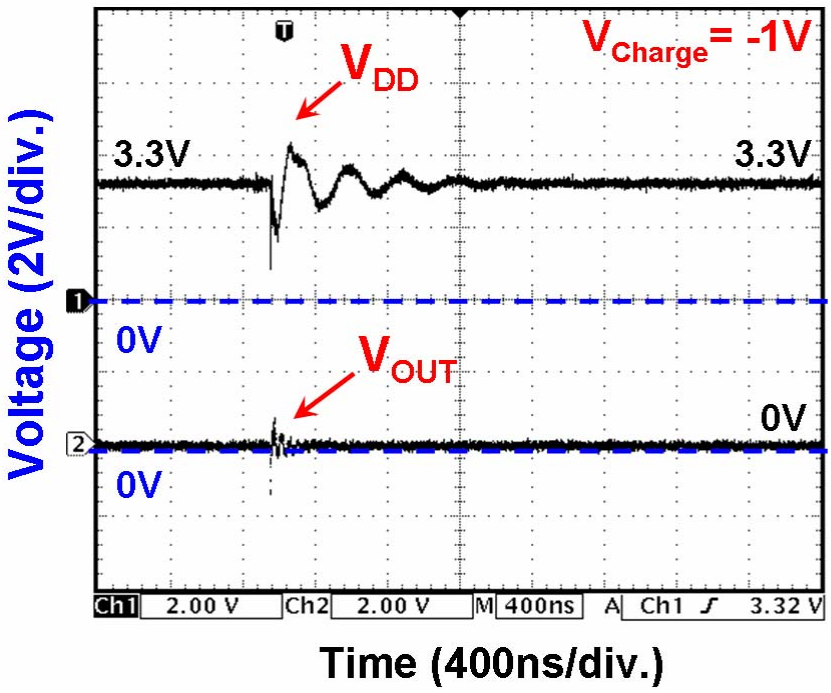


Fig. 4.7 Relations between the decoupling capacitance and system-level ESD detection level (V_{charge}) of the proposed transient detection circuit under three types of noise filter networks: capacitor filter, type-IRC filter, π-section filter.



(a)



(b)

Fig. 4.8 Measured V_{DD} and V_{OUT} transient responses on the proposed on-chip transient detection circuit I with noise filter under (a) positive and (b)negative TLU test with Vcharge of +9V and -1V, respectively.

Chapter 5

Design of On-Chip Transient-to-Digital Converter

5.1. Background

In chapter 2 and chapter 3, the proposed on-chip transient detection circuits have been designed and fabricated in a 0.18-μm technology with 3.3-V devices. From the simulation and measurement results, the proposed transient detection circuits can successfully detect positive/negative fast electrical transients on the power and ground lines under system-level ESD tests. In chapter 4, different types of board-level noise filter networks have been evaluated the ability to suppress the system-level ESD-induced energy on the power and ground lines. The higher order noise filter applied between the power and ground lines can provide better suppressed ability to reduce the ESD-induced energy zapping into the CMOS ICs. By choosing adaptable noise filter networks to combine with the transient detection circuits, the quantity of the ESD-induced energy zapping into the transient detection circuits on the power or ground lines can be further controlled. In this chapter, different noise filters combined with the proposed transient detection circuit has been designed and investigated under system-level ESD tests. Even with the same ESD zapping voltage, the different noise filters between the ESD trigger source and the transient detection circuit would provide different suppression on the ESD-induced energy. Under system-level ESD tests with smaller ESD voltages, the proposed on-chip transient detection circuit combined with higher-order noise filter network would not easily change the stored logic state, but that with lower-order noise filter network can easily change the logic state from logic 0 to logic 1. Therefore, the positive/negative fast electrical transient voltages under system-level ESD tests can be converted to digital thermometer codes. By using the proposed on-chip transient-to-digital converter, the quantity of the ESD voltage zapped into the CMOS ICs inside the

microelectronic products under system-level ESD tests can be quantified as digital thermometer codes.

5.2. Proposed On-Chip Transient-to-Digital Converter

The design concept of proposed on-chip transient-to-digital converter is shown in Fig. 5.1. The detection block could be on-chip transient detection circuit I (or transient detection circuit II) to detect the positive/negative fast transients under system-level ESD tests. Otherwise, different types of noise filter networks have different ability to bypass, absorb, or decouple ESD-induced energy. Therefore, by combing different noise filter networks with several detection blocks, the ESD-induced voltage zapping into the power and ground lines of each proposed on-chip transient detection circuits would be different. By using this design idea, the system-level ESD-induced energy can be converted into digital thermometer codes which can estimate the noise quantity under system-level ESD tests.

5.2.1. Circuit Structure

The evaluation of an on-chip transient detection circuit with board-level noise filter networks has been investigated in the previous chapter. In order to combine the noise filter network with on-chip transient detection circuit in chip-level, type-II RC filter shown in Fig. 4.2 (d) is adopted to design the proposed on-chip transient-to-digital converter. Fig. 5.2 shows the proposed 4-bits on-chip transient-to-digital converter consisted of on-chip transient detection circuit II and type-II RC filter, realized with one decoupling capacitor and two resistors with equal value. The four different type-II RC filters with the same capacitance and different resistance ranging from 10Ω to 150Ω provide noise filter function under system-level ESD stress. Therefore, the different type-II RC filters provide different ability to suppress the ESD-induced noise zapping into the on-chip transient detection circuit. The outputs of four on-chip transient detection circuits would be influenced simultaneously, but

the noise quantity affected on the V_{DD}/V_{SS} lines of each on-chip transient detection circuits is different owing to the different on-chip noise filters. Each transient detection circuit combined with different noise filter networks needs different ESD-induced zapping voltage to trigger the detect function under system-level ESD stress. By combing with noise filter network to suppress transient noise on power and ground lines, the proposed on-chip transient detection circuit needs higher ESD voltages to trigger on detection function than that without using noise filter network. Therefore, to properly combine the on-chip transient detection circuit with on-chip type-II RC filter as a transient-to-digital converter shown in Fig. 5.2, the system-level ESD-induced energy can be further converted into digital thermometer codes to estimate the quantity of ESD-induced energy zapped into the CMOS ICs under system-level ESD tests. Fig. 5.3 shows the chip photograph of the proposed on-chip transient-to-digital converter.

5.2.2. Measurement Results of System-Level ESD Tests

5.2.2.1. Positive System-Level ESD Zapping Conditions

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD tests with positive ESD voltage of +0.7kV are shown in Fig. 5.4 (a). When the power and ground lines of transient-to-digital converter are affected by ESD stress under system-level ESD tests, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are influenced simultaneously. Due to the different ability of on-chip type-II RC filters to suppress ESD-induced energy, V_{OUT1} is changed from 0V to 3.3V and V_{OUT2}, V_{OUT3}, and V_{OUT4} are still kept its initial voltage at 0V. Therefore, the ESD-induced voltage under system-level ESD tests can be successfully converted into digital thermometer code "0001."

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD tests with positive ESD voltage of +0.9kV are shown in Fig. 5.4 (b). When the power and ground lines are affected by ESD stress under system-level

ESD tests, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are influenced simultaneously. Finally, V_{OUT1} and V_{OUT2} are changed from 0V to 3.3V, and V_{OUT3}, and V_{OUT4} are still kept its initial voltage at 0V. Therefore, the ESD-induced energy under system-level ESD tests can be converted into digital thermometer code "0011."

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD tests with positive ESD voltage of +1.1kV are shown in Fig. 5.4 (c). Under system-level ESD tests, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are influenced simultaneously. Finally, V_{OUT1}, V_{OUT2}, and V_{OUT3} are changed from 0V to 3.3V and V_{OUT4} is still kept its initial voltage at 0V. Therefore, the ESD-induced energy under system-level ESD tests can be converted into digital thermometer code "0111."

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD tests with positive ESD voltage of +1.3kV are shown in Fig. 5.4 (d). Under system-level ESD tests, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are influenced simultaneously. Finally, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are all changed from 0V to 3.3V. Therefore, the ESD-induced energy under system-level ESD tests can be converted into digital thermometer code "1111."

5.2.2.2. Negative System-Level ESD Zapping Conditions

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD tests with negative ESD voltage of -1.1kV are shown in Fig. 5.5 (a). During the ESD stress zapping on the HCP under system-level ESD tests, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are influenced simultaneously. Due to the different ability of on-chip type-II RC filters to suppress ESD-induced energy, V_{OUT1} is changed from 0V to 3.3V and the other outputs of transient-to-digital converter, V_{OUT2}, V_{OUT3}, and V_{OUT4}, still keep its initial voltage at 0V, finally. Therefore, the ESD-induced energy under system-level ESD tests can be converted into digital thermometer code "0001."

Similarly, Figs. 5.5 (b), 5.5(c), and 5.5(d) show the measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of on-chip transient-to-digital converter under system-level ESD tests with negative ESD voltages of -1.6kV, -2.0kV, and -2.2kV, respectively. After system-level ESD tests, the ESD voltages zapping on HCP can be transferred into digital thermometer codes of "0011," "0111," and "1111."

Fig. 5.6 depicts the relationship between ESD voltage and the digital code of proposed transient-to-digital converter under system-level ESD tests with positive and negative ESD voltage. The x-axis represents the ESD-induced energy (ESD voltage) and the y-axis represents the digital thermometer codes. With larger ESD-induced energy (ESD voltage) under system-level ESD tests, the transferred digital thermometer code goes higher. Thus, the positive (negative) ESD voltages of +0.7kV (-1.1kV), +0.9kV (-1.6kV), +1.1kV (-2.0kV), and +1.3kV (-2.2kV) can be converted into digital thermometer codes, "0001," "0011," "0111," and "1111," respectively.

Similarly, the proposed on-chip transient-to-digital converter can be measured under TLU tests to accurately evaluate the system-Level ESD detection level of each output bit. Fig. 5.7 (a) and (b) shows the measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} voltage waveforms under TLU tests with two different positive V_{Charge}. Two output bits and four output bits of transient-to-digital converter change their logic states after different TLU tests. The completed measured results of transient-to-digital converter under TLU tests are listed in Table 5.1. From the measured results, each output bit of transient-to-digital converter can change its voltage level from 0V to 3.3V sequentially with different positive/negative V_{Charge}.

5.3. Conclusion

The new proposed on-chip transient-to-digital converter composed of noise filter networks and transient detection circuits have been fabricated in a 0.18-μm process with 3.3-V devices. By using on-chip noise filter network to reduce the transient disturbance

voltage on the power and ground lines, the minimum system-level ESD voltage to cause transition at outputs of transient detection circuit can be adjusted. From the measurement results, the proposed on-chip transient-to-digital converter can successfully detect and transfer output voltages into thermometer digital codes under system-level ESD tests with different ESD voltages. Therefore, a novel on-chip transient-to-digital converter can be designed by using the proposed on-chip transient detection circuits combined with different RC filter networks. The digital thermometer codes of transient-to-digital converter with corresponding positive/negative V_{Charge} (ESD voltage) under TLU tests (system-level ESD tests) are listed in Table 5.1.

Table IX Different positive/negative V_{charge} and ESD voltage corresponds to digital thermometer codes under TLU and system-level ESD tests.

Test	TLU test		System-Level ESD test	
Digital Codes	Positive V_{Charge} (V)	Negative V_{Charge} (V)	Positive ESD Voltage (kV)	Negative ESD Voltage (kV)
0000	0 ~ 15	0 ~ -3	0 ~ 0.7	0 ~ -1.1
0001	15 ~ 18	-3 ~ -5	0.7 ~ 0.9	-1.1 ~ -1.6
0011	18 ~ 22	-5 ~ -7	0.9 ~ 1.1	-1.6 ~ -2.0
0111	22 ~ 28	-7 ~ -11	1.1 ~ 1.3	-2.0 ~ -2.2
1111	>28	<-11	> 1.3	< -2.2

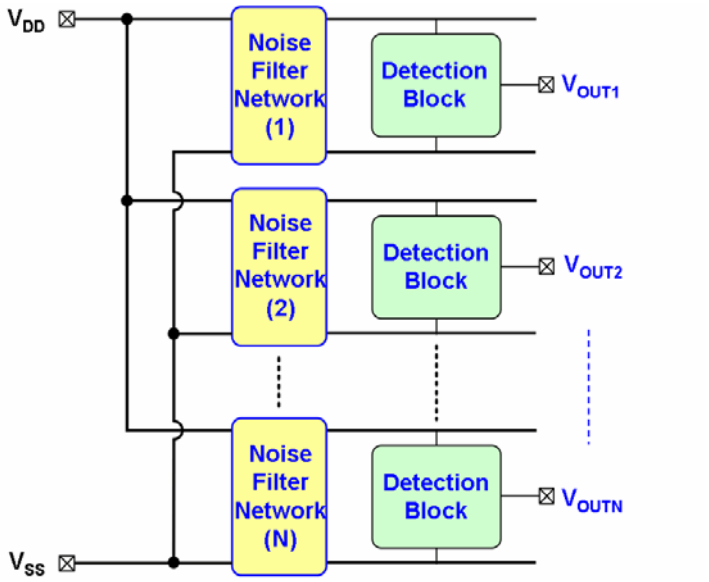


Fig. 5.1 The circuit structure of transient-to-digital converter composed of noise filter networks and detection blocks.

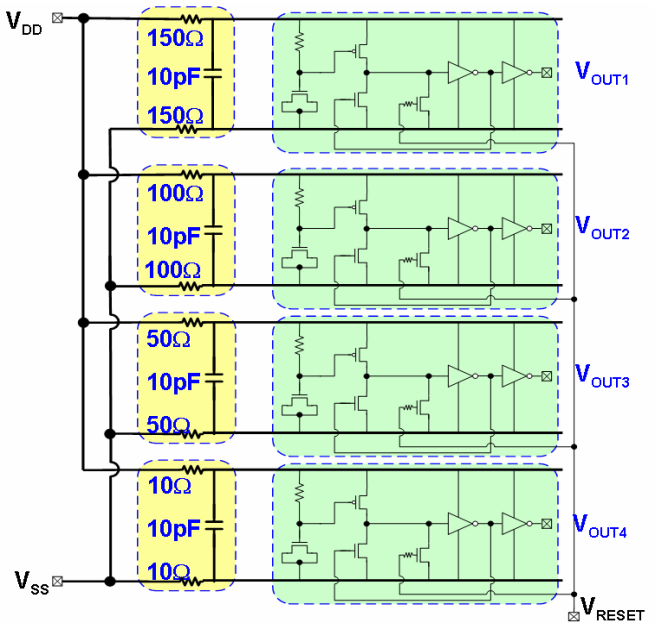


Fig. 5.2 The circuit schematic of proposed on-chip transient-to-digital converter.

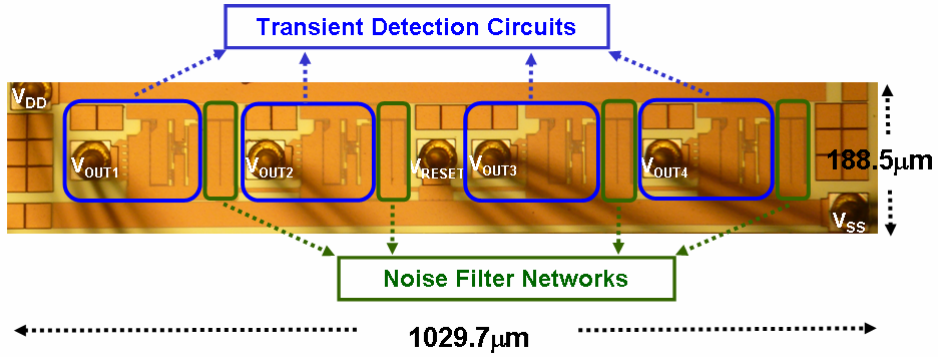


Fig. 5.3 Die photos of proposed on-chip transient-to-digital converter.

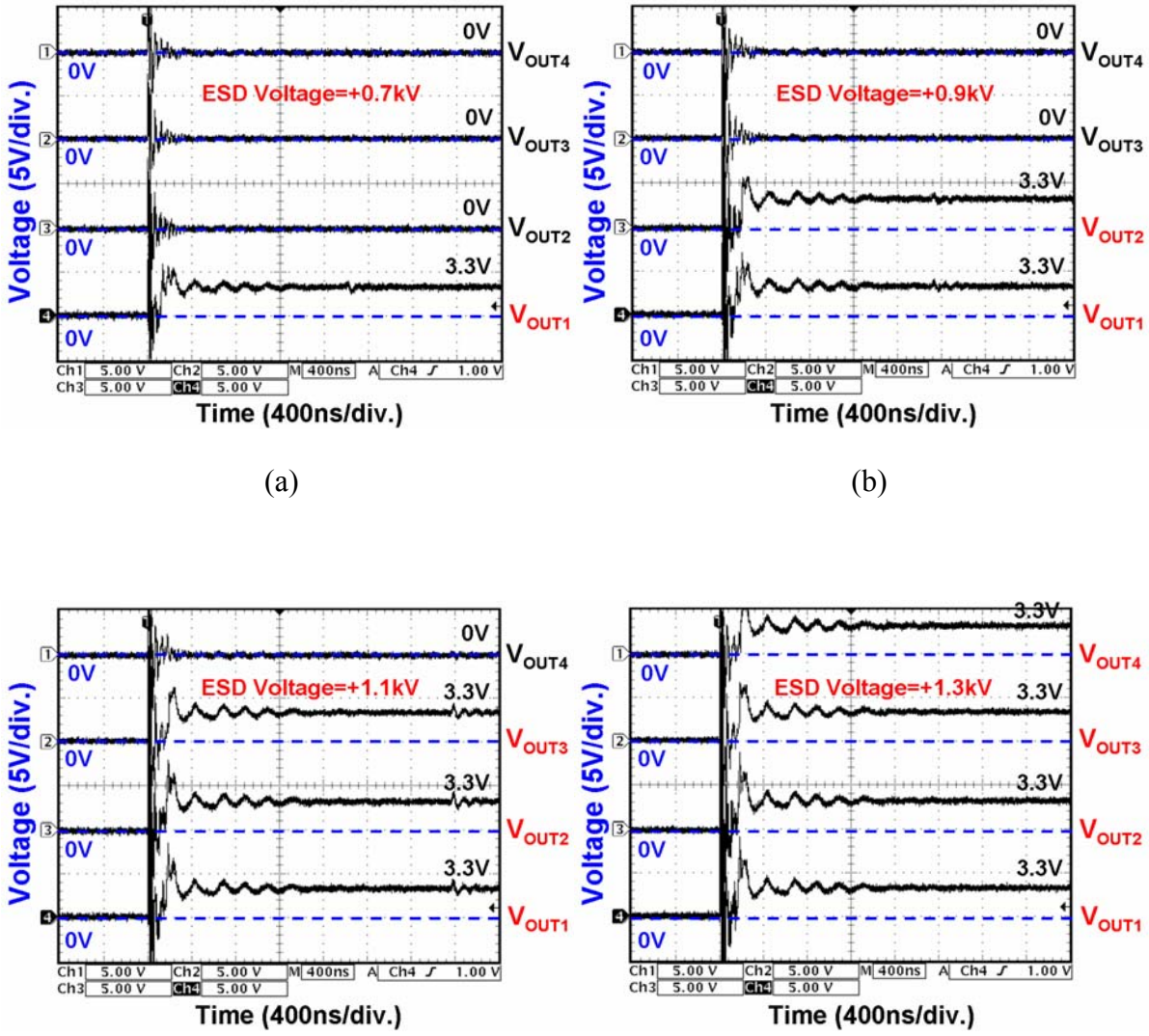


Fig. 5.4 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under positive system-level ESD tests with ESD voltage of (a) +0.7kV, (b) +0.9kV, (c) +1.1kV, and (d) +1.3kV.

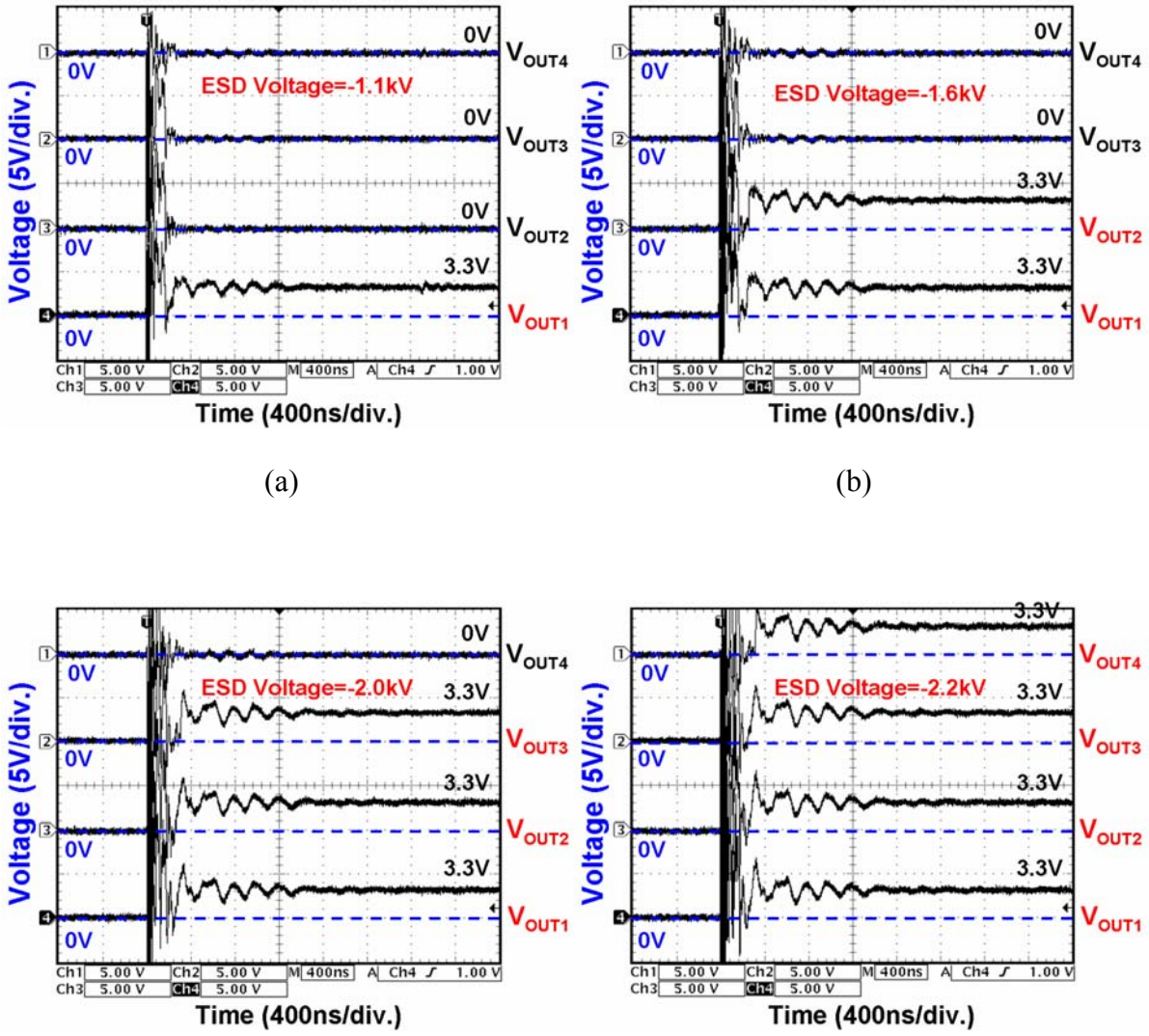


Fig. 5.5 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under negative system-level ESD tests with ESD voltage of (a) -1.1kV, (b) -1.6kV, (c) -2.0kV, and (d) -2.2kV.

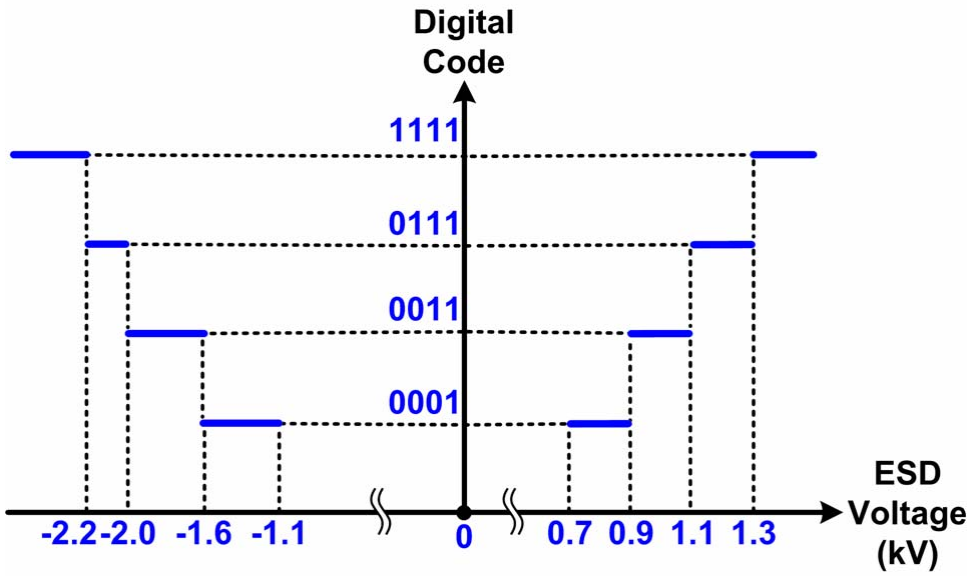
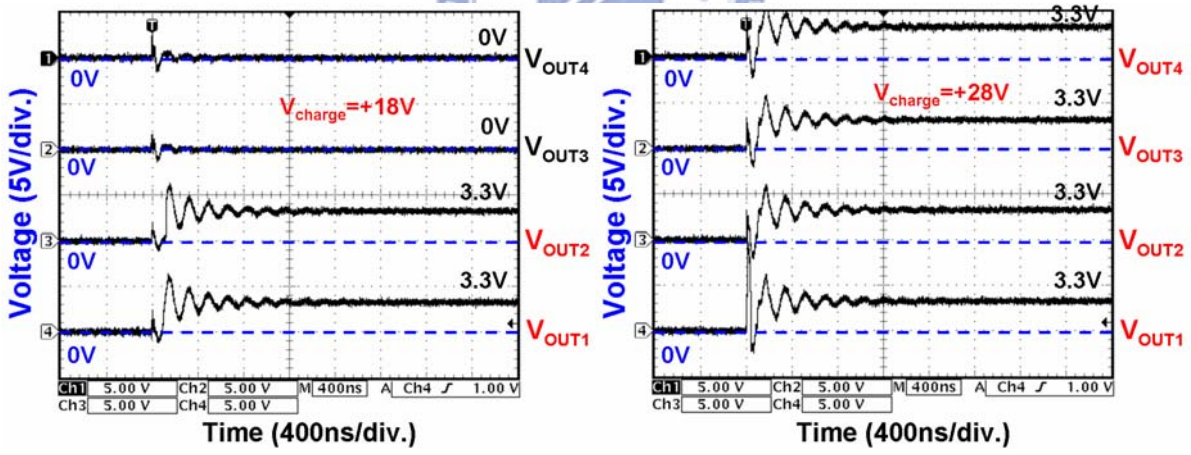


Fig. 5.6 The relationship between ESD voltage and the digital code of the proposed transient-to-digital converter.



(a) (b)

Fig. 5.7 Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient waveforms under positive TLU tests with V_{Charge} of (a) +18V, (b) +28V.

Chapter 6

Conclusions and Future Works

6.1. Conclusions

Two novel on-chip transient detection circuits have been proposed in chapter 2. The circuit performance has been investigated by the simulation tool HSPICE. From the simulation results, the output voltage level of both on-chip transient detection circuits can be changed from logic 0 to logic 1 after system-level ESD and EFT events.

These transient detection circuits have been fabricated in a 0.18-μm CMOS process with 3.3-V devices. From the experimental results in chapter 3, the outputs of transient detection circuits can transit from 0V to 3.3V after TLU, system-level ESD, and EFT zapping. Therefore, it has been confirmed that the transient detection circuits can successfully detect and memorize the occurrence of positive and negative fast electrical transient disturbance on the power and ground lines of CMOS ICs.

The performances of different noise filter networks on the transient detection circuit have been evaluated under TLU tests in chapter 4. The higher order of noise filters can more effectively change the detection level of the proposed on-chip transient detection circuits.

A novel proposed on-chip transient-to-digital converter composed of four different noise filter networks and four transient detection circuits have been designed and fabricated in a 0.18-μm CMOS process with 3.3-V devices. By using on-chip noise filter network to reduce the transient disturbance on the power and ground lines, the minimum system-level ESD voltage to cause transition at outputs of each transient detection circuit can be adjusted. From the measurement results, the proposed on-chip transient-to-digital converter can successfully detect and transfer different ESD voltages into digital thermometer codes under TLU and system-level ESD tests.

6.2. Future Works

The detection level of two proposed on-chip transient detection circuits can be adjusted by the noise filter networks. Therefore, a novel transient-to-digital converter composed different noise filters and transient detection circuits can successfully transit different ESD voltages into digital thermometer codes under system-level ESD tests. In advance, the linear relation between ESD zapping voltages and digital thermometer codes should be improved by optimizing the combined on-chip noise filter networks and designing new circuit structure.

By using the RC-delay design concept, the proposed on-chip transient detection circuits and transient-to-digital converter can detect the transient voltage disturbance on the power and ground lines. However, for the experimental results, the system-level ESD voltage detection range is under ±2kV. The voltage disturbance detection is also dependent on the impedance of the EUT. In advance, the further on-chip transient detection circuits and transient-to-digital converter can be designed to detect current transition of power and ground lines under system-level ESD zapping condition.

In system application, the on-chip transient-to-digital converter can be cooperated with power-on reset circuits and operating firmware to provide a hardware/firmware co-design solution for system-level ESD protection. After firmware receives different digital thermometer codes as ESD flag, different recover procedure can be executed and then reset the output voltage levels of on-chip transient-to-digital converter for detecting next system-level ESD events. Therefore, the IC products can achieve the “Class B” system-level ESD specification at least. Besides, in order to meet the “Class A” specification, the on-chip transient-to-digital converter should be designed without reset function to automatically recover all system function.

Reference

[1] *EOS/ESD Standard for ESD Sensitivity Testing – Human Body Model – Component Level*, STM 5.1, EOS/ESD Association, NY., 2001.

[2] *EOS/ESD Standard for ESD Sensitivity Testing – Machine Model – Component Level*, STM 5.2, EOS/ESD Association, NY., 1999.

[3] *EOS/ESD Standard for ESD Sensitivity Testing – Charge Device Model – Component Level*, STM 5.3.1, EOS/ESD Association, NY., 1999.

[4] M.-D. Ker and S.-F. Hsu, "Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821-1831, Aug. 2005.

[5] IEC 61000-4-2 Standard, "*EMC – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test*," IEC, 2001.

[6] T.-H. Wang, W.-H. Ho, and L.-C. Chen, "On-chip system ESD protection design for STN LCD drivers" in *Proc. EOS/ESD Symp.*, 2002, pp. 316-322.

[7] M.-D. Ker and Y.-Y. Sung, "Hardware/firmware co-design in a 8-bits microcontroller to solve the system-level ESD issue on keyboard" in *Proc. EOS/ESD Symp.*, 1999, pp. 352-360.

[8] IEC 61000-4-4 Standard, "*EMC – Part 4-4: Testing and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test*," IEC, 2004.

[9] M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, IEEE Press, 2000.

[10] M.-D. Ker and S.-F. Hsu, "Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electromagn. Compat.* vol. 48, no. 1, pp. 161-171, Feb. 2006.

[11] M.-D. Ker, C.-C. Yen, and P.-C. Shin, "On-chip transient detection circuit for system-level ESD protection in CMOS integrated circuits to meet electromagnetic compatibility regulation," *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 1, pp. 13-21, Feb. 2008.

[12] D. Smith and A. Wallash, "Electromagnetic interference (EMI) inside a hard disk driver due to external ESD," in *Proc. EOS/ESD Symp.*, 2002, pp. 32-36.

[13] M. Kelly, L. Henry, J. Barth, G. Weiss, M. Chaine, H. Gieser, D. Bonfert, T. Meuse, V. Gross, C. Hatchard, and I. Morgan, "Developing a transient induced latch-up standard for testing integrated circuits," in *Proc. EOS/ESD Symp.*, 1999, pp. 178-189.

[14] I. Morgan, C. Hatchard, and M. Mahanpour, "Transient latch-up using an improved bi-polar trigger," in *Proc. EOS/ESD Symp.*, 1999, pp. 190-202.

[15] M.-D. Ker and S.-F. Hsu, "Evaluation on efficient measurement setup for transient-induced latchup with bi-polar trigger," in *Proc. IEEE Int. Rel. Phys Symp.*, 2005, pp.121-128.

[16] M.-D. Ker and S.-F. Hsu, "Component-level measurement for transient-induced latchup in CMOS ICs under system-level ESD considerations," *IEEE Trans. Device Mater. Reliab.*, vol. 6, no. 3, pp. 461-472, Sep. 2006.

[17] S.-F. Hsu and M. D. Ker, "Dependences of damping frequency and damping factor of bi-polar trigger waveforms on transient-induced latchup," in *Proc. EOS/ESD Symp.*, 2005, pp. 118-125.

簡歷 (Vita)

姓　　名：廖期聖

學　　歷：

國立師範大學附屬高級中學　　(88 年 9 月~91 年 6 月)

國立中興大學電機工程學系　　(91 年 9 月~95 年 6 月)

國立交通大學電子研究所碩士班　　(95 年 9 月~97 年 7 月)

研究所修習課程：

類比積體電路	吳介琮教授
數位積體電路	周世傑教授
計算機輔助設計特論	周景揚教授
資料轉換積體電路	吳介琮教授
計算機結構	劉志尉教授
積體電路之靜電放電防護設計特論	柯明道教授
穩健設計之品質工程	黎正中教授
鎖相迴路設計與應用	陳巍仁教授
顯示電子電路	戴亞翔教授

Email：gosh.ee95g@nctu.edu.tw

m9511653@alab.ee.nctu.edu.tw