中文摘要

隨光儲系統發展過程中，微光點量測越來越重要。傳統上微光點可由 CCD 攝影機量測，但其解析度受限於像素的大小，也無法使用於近場光學量測。光點的近場分佈可以利用近場光學顯微鏡進行，但探針易於量測中損壞、架設困難及高成本為其缺點。

為改善以上的缺點，我們以刀緣掃描法做量測，量測系統整合平整的刀緣掃瞄板、梳狀致動器、光感測器及電路於同一晶片上以直接對微光點作量測。利用標準 CMOS 製程，可以將上述元件整合於同一晶片，再以額外的後製程將結構懸浮。成功懸浮微結構後，將以此晶片對微光點做量測，利用吸收式元件完成微光機電系統之整合。

於此論文中已成功將光學、機械及電路元件整合於同一晶片內，光學量測方面將於此論文呈現以下結果：一、D35-95D 梯次之吸收式微結構結合 off-chip 轉阻放大器及於 D35-97C 梯次晶片中轉阻放大器；二、D35-97C 晶片上之微結構與其晶片內之轉阻放大器的量測。

Abstract

As the developing of data storage systems, micro spot size measurement becomes more important. Micro spot size can be traditionally measured by CCD camera. However, the resolution is limited by the pixel size and can not apply to near-field measurement. For near-field measurement, near-field scanning optical microscopes (NSOM) can be used to measure micro spot size with high resolution. However, the NSOM tip easily wears out under measurement. The setup of this system is complex and cost is high.

To improve these disadvantages, a microelectromachanical system (MEMS) optical spot profile measurement system based on the scanning knife-edge technique is proposed. In the fabricated device, a knife-edge plate, a micro actuator, a photo detector and circuit are integrated on the micro actuator to scan across the optical distribution. The standard CMOS process is used to integrate above component together. Extra post process is used to suspend the microstructure in this chip. After fabricating the device successfully, this chip is used to measured micro spot size. The absorption type device successfully integrates optical, mechanical and electrical component in the same chip.

致謝

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Chapter 1 Introduction

Optical spot measurement is important in data storage systems. The spot profile is traditionally measurement by a charge-coupled device (CCD) beam profiling system. The setup of the system is shown in Fig. 1-1. The image processing unit is used to acquire the spot profile from the camera. However, the measurement result in this kind of system is easily affected by aberration. Additionally, by the system can not measure the near-field optical distribution. For near-field measurement, near-field scanning optical microscopy (Fig. 1-2) can be used to measure the optical distributions with very high resolution [1]. However, the NSOM tip easily wears out under repeated operation.

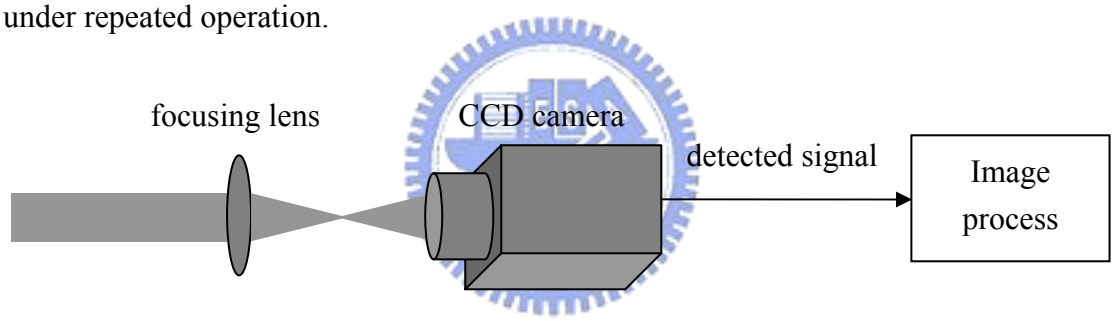


Fig. 1-1 Setup of CCD beam profiling systems

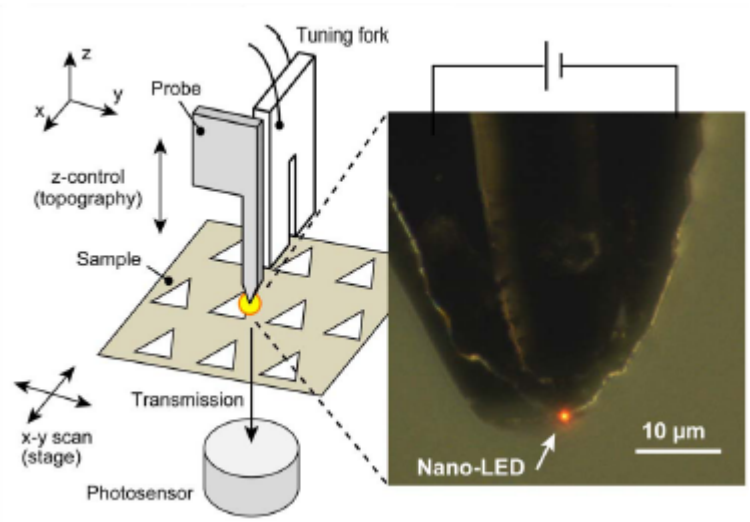


Fig. 1-2 NSOM setup [1]

To overcome the disadvantages described above, a knife-edge method is used to measure the spot profile with sub-micro resolution. MEMS-based technology is used to fabricate the device which contains a moving photo detector as a knife edge plane. The photo detector is actuated by a micro actuator to scan across the spot. A circuit is also integrated in the chip to process the photocurrent produced from the photo detector. The spatial resolution is limited by the actuator control and signal analysis.

The proposed micro optical spot profile measurement system is also a demonstration of an integrated optical MEMS system. The actuator, photo detector, and signal processing circuits can be integrated monolithically to form a photonic system on chip.

1.1 MEMS-based optical spot profile measurement system

The knife edge method is applied to the spot profiling system (Fig. 1-3). A sharp knife edge plate scans across an optical field distribution. A photo detector behind the edge detects the transmitted light energy of the spot and produces a photocurrent. The photocurrent is:

$$I(x) = k\int_{x}^{\infty} P(x')dx', \tag{1}$$

where x is the position of edge, $P(x)$ is the optical field distribution, and k is the sensitivity of the photo detector. Therefore, the optical field distribution can be obtained by taking the derivative of $I(x)$ and is given by:

$$P(x) = -\frac{1}{k}\frac{dI(x)}{dx} \tag{2}$$

If the spot has a Gaussian profile, the full width at half maximum (FWHM) of the spot can be taken the distance between 12% and 88% of the full scale of the measured photo current $I(x)$, as shown in Fig. 1-4.

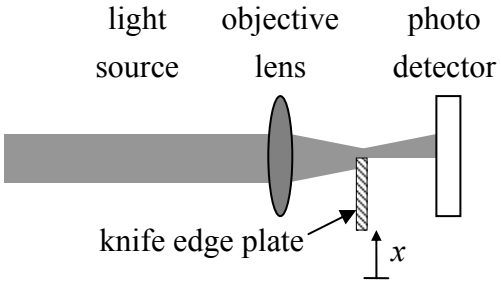


Fig. 1-3 Schematic of knife edge method

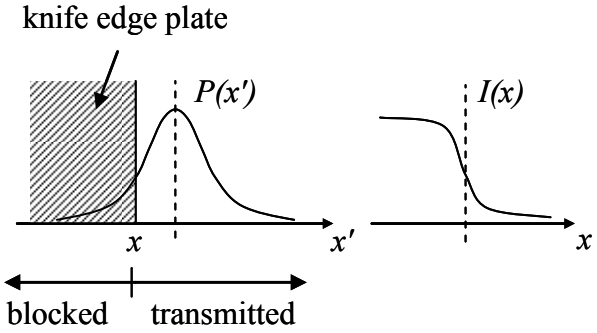


Fig. 1-4 Relationship between spot profile and detected photocurrent

This kind of system can be realized as three configurations, namely the transmission type (Fig. 1-5(a)), reflection type (Fig. 1-5(b)), and absorption type (Fig. 1-5(c)). In the reflection type system, a reflective area scans across the spot. The reflected light is detected by an external photo detector. In the absorption type system, a photo detector scans across the spot and detects the energy of the light directly. To implant the micro optical spot profile measurement system shown in (Fig. 1-5(d)), the photo detector is integrated in the movable structure and actuated by a comb actuator. The photo detector is designed to be a right angled triangle for two-axis spot profiling. The actuator is actuated at the resonant frequency to obtain large scanning range. Among different configurations, the absorption type device is more attractive than the others by its higher integration level. Therefore, our efforts are focused on the design of the absorption type.

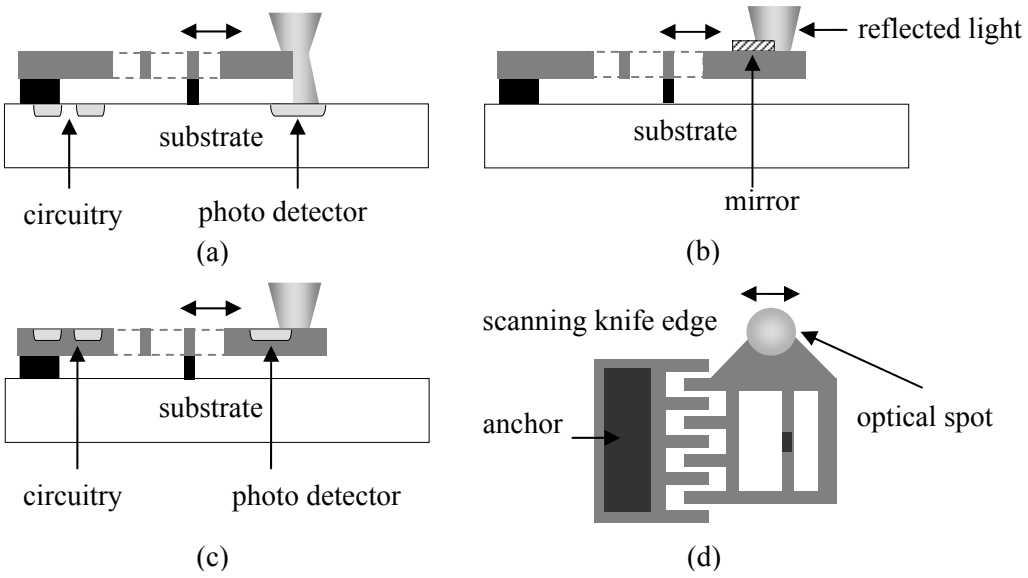


Fig. 1-5 Micro spot profiling system (a) transmission type (b) reflection type (c) absorption type (d) system top view

1.2 Microstructure fabrication

To fabricate the absorption type device, a photo detector is fabricated in movable part. The photo detector has better performance by using single crystalline silicon (SCS). Therefore, the movable part must have a SCS region where the photo detector of the absorption type device is fabricated. To suspend a microstructure with movable SCS part, SOI process and CMOS-MEMS process can be used. These processes will be discussed in the following sections.

1.2.1 SOI process

A SOI wafer contains a device layer, a buried oxide layer, and a handle layer. In the SOI process, deep reactive ion etching (DRIE) is used to create high-aspect-ratio microstructures (Fig. 1-6(a)). The buried oxide serves as a sacrificial layer. The microstructures are released by using HF to etch the buried oxide (Fig. 1-6(b)). They are popular due to the process simplicity and the ability to make SCS microstructures

with 100 μm-ranged thicknesses. Electrical signals of the sensors and actuators can be isolated by the remaining buried oxide.

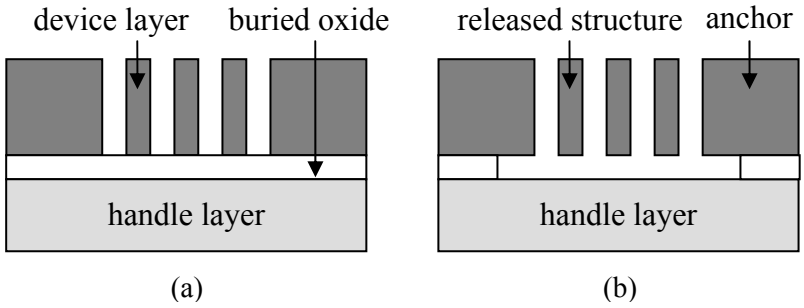


Fig. 1-6 SOI MEMS process (a) DRIE (b) release by HF

1.2.2 CMOS process and post-CMOS fabrication

Although the SOI process for releasing microstructures is simple and provides good signal isolation, the integration level is less then the CMOS process for circuit integration. The signals from MEMS sensors need to be processed before readout. Compatibility of MEMS fabrication with mainstream integrated circuit (IC) technology provides not only these advantages but also fast economical accessibility and short design cycles. For a high-performance, reliable, and low cost product, it is necessary to integrate the MEMS sensor with circuit components.

To release a microstructure fabricated by standard IC processes, a post process is needed. Usually, MEMS structures in the CMOS process is composed of the metal (aluminum), via (tungsten), and dielectric (SiO_2) layers [2]. Wet etching and photolithography are not necessary to release a structure. The cross section view of a typical post CMOS process for structure releasing is shown in Fig. 1-7(a). First, the dielectric layer is etched by CHF_3:O_2 reactive ion etching (RIE) (Fig. 1-7(b)). The top metal layer serves as a highly selective mask thus defines the structure. After the dielectric etching, silicon DRIE then sets the spacing from the suspended structure to substrate (Fig. 1-7 (c)). The structure is finally released by isotropic silicon etching

(Fig. 1-7(d)). The post process uses only dry etching to prevent stiction. Various thin-film CMOS-MEMS devices such as accelerometers [3] and infrared imagers [4] have been demonstrated. However, silicon substrate is not attached to the movable structure by using this kind of post CMOS process. Therefore, it is not an appropriate process for the absorption type device.

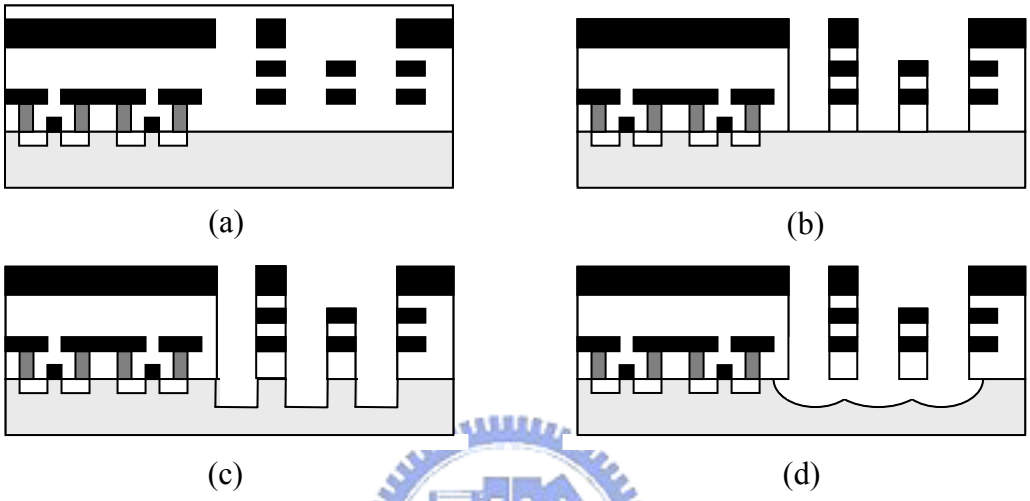


Fig. 1-7 Thin film CMOS MEMS (a) original chip (b) dielectric etching (c) frontside DRIE (d) isotropic silicon etching

The backside of the CMOS chip can also be micromachined. The backside silicon is first etched by DRIE (Fig. 1-8 (a)). After the frontside dielectric etching (Fig. 1-8(b)), the frontside silicon is etched by DRIE (Fig. 1-8(c)). The structure is finally released by isotropic silicon etching (Fig. 1-8(d)). Different kinds of DRIE CMOS-MEMS device such as micromirrors [5], gyroscopes [6], and comb drive resonators [7] have been demonstrated. To leave the silicon substrate for the photo detector, this method is used to fabricate the absorption type device.

1.3 Transimpedance circuit

To convert the current signal of the photodiode to a voltage signal, a

transimpedance circuit is needed. As shown in Fig. 1-9(a), a common gate configuration is used to implement this function [8]. However, part of the photocurrent flows into bias resistors of M1. The photocurrent can not completely flow into the transimpedance circuit.

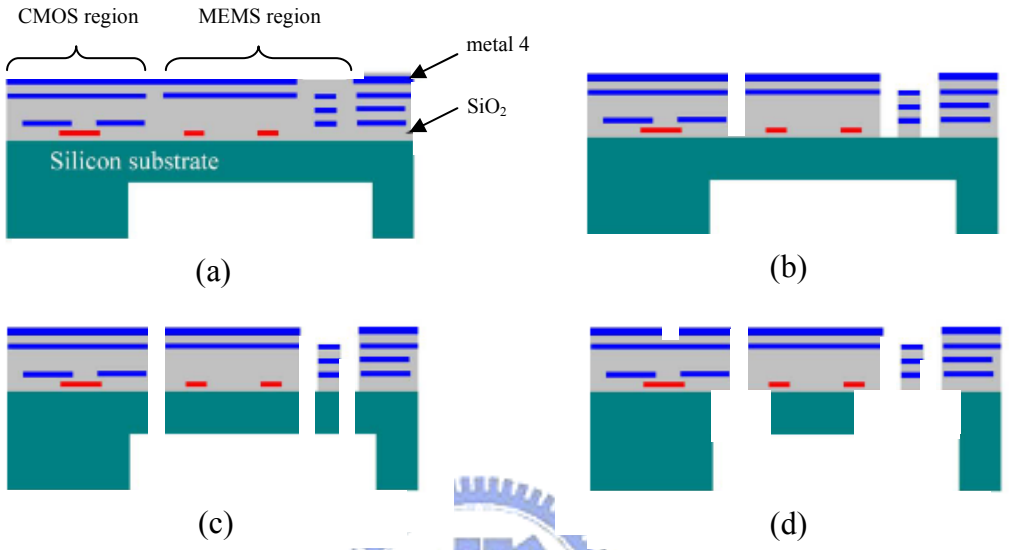


Fig. 1-8 DRIE CMOS MEMS (a) backside DRIE (b) dielectric etching (c) frontside DRIE (d) isotropic silicon etching [6]

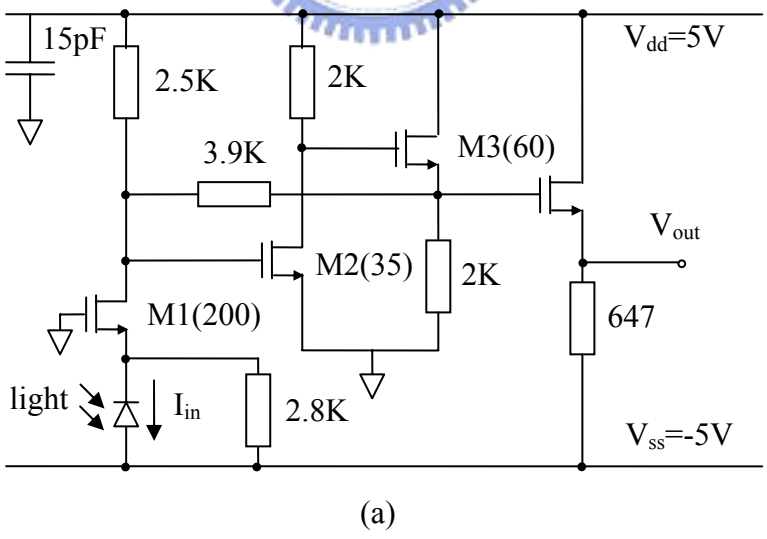
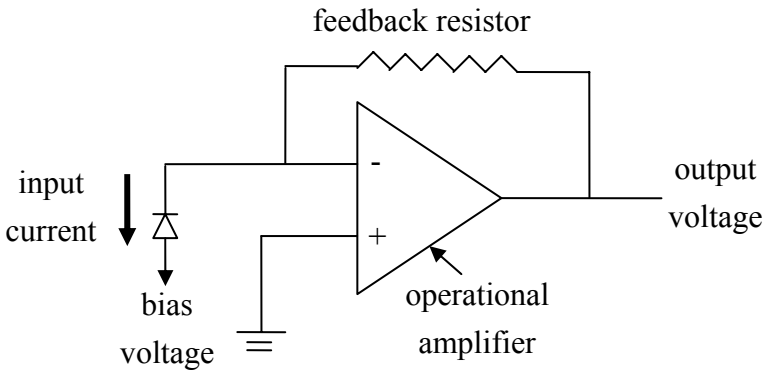


Fig. 1-9 Transimpedance circuit (a) common gate [8] (b) constructed by an operational amplifier



(b)

Fig. 1-9 Transimpedance circuit (a) common gate [8] (b) constructed by an operational amplifier (continued)

An operational amplifier and a feedback resistor can used to form a transimpedance circuit (Fig. 1-9(b)). The photo diode is connected to the inverting input of the operational amplifier. The current flowing into operational amplifier is almost zero. Therefore, the percentage of photocurrent which flows into the transimpedance circuit is higher then common gate configuration. Therefore, the configuration described in Fig. 1-9(b) is more suitable in our design.

1.4 Literature survey

1.4.1 Method of spot profile measurement

A dithering probe can measure the focused spot profile as shown in Fig. 1-10. The beam transmitted through the z-axis is focused by a focusing lens. The probe vibrates in x-axis and dither across the spot. The bicell detector can detect the sum or difference of the signal produced by detectors A and B [9].

The knife edge method is also used to measure the spot size. Ref. [10] uses this method to measure the spot size focused by a lens. The electric signal is produced by an optical head or photo diode when detecting the partial light energy of the spot. The

spot profile can be obtained by taking the derivative of the knife edge signal. In this research, the resolution is better than $\lambda/8$ (λ=820 nm). Therefore, a sub-micro resolution can be achieve by using the knife edge method.

From the above discussion, the scanning knife edge provides a sub-micro resolution. The knife edge and photo detector can be fabricated by MEMS technology.

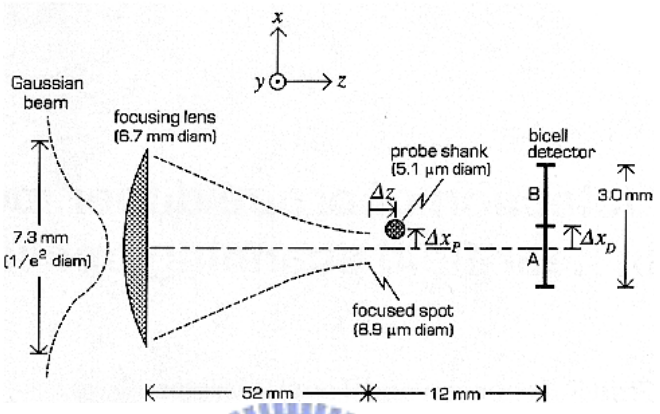


Fig. 1-10 Dithering probe to measure a focused spot [9]

1.4.2 Optical MEMS system

The DMD array is used to simulate the knife edge measurement of a spot [11]. By rotating a row or a column of micromirrors sequentially, the partial reflected light is detected by an external photo detector (Fig. 1-11). This system integrates electrical and mechanical components but not optical elements in MEMS.

A NSOM probe was presented by Sasaki, et al., as shown in Fig. 1-12 [12]. The waveguide and photo detector are integrated on a cantilever beam. The integration of micro optical components, optoelectric components and micromechanical structure is demonstrated.

The optical bench (Fig. 1-13(a)) proposed by Wu, et al. is used to form a three dimensional micro stage [13]. By the scratch drive actuators (SDA), the position of lower 45° mirror, upper 45° mirror, and microlens can be actuated laterally. The lateral optical path can be adjusted by actuating the lower 45° mirror. The upper 45°

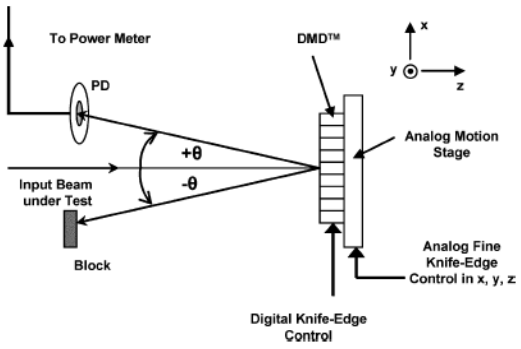


Fig. 1-11 Setup for knife-edge method simulation [11]

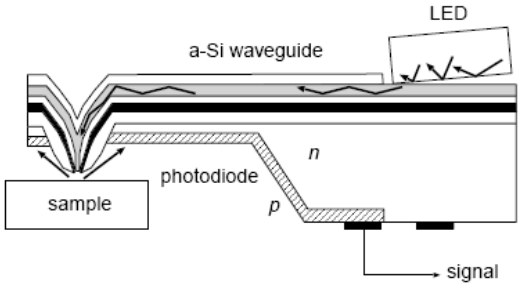
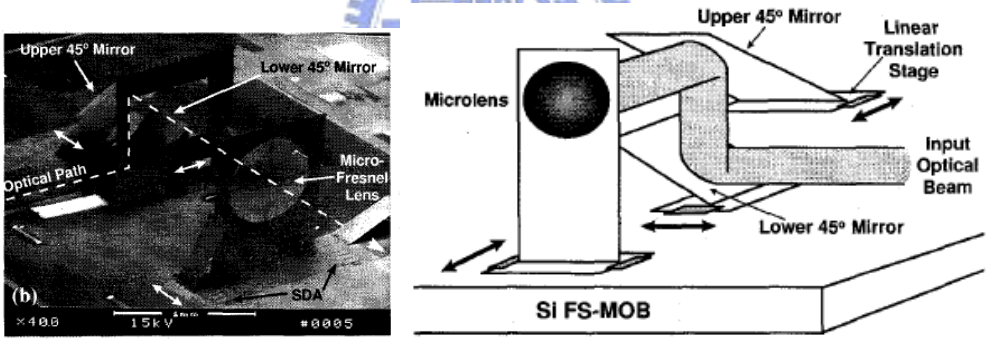
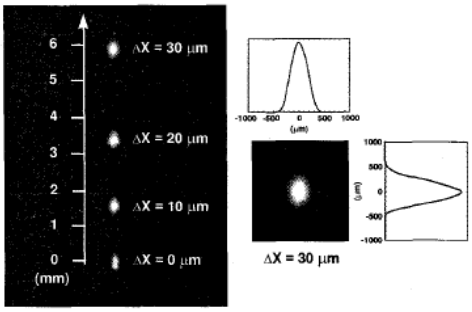


Fig. 1-12 NSOM probe in a cantilever beam [12]



(a) (b)



(c)

Fig. 1-13 Micro optical bench (a) SEM picture (b) schematic of optical path adjusting (c) measured changing of optical path [13]

mirror is used to vertically adjust optical path (Fig. 1-13(b)). The vertical adjustment can be achieved by only in-plane microactuators. The change of the optical path is captured by an external CCD camera (Fig. 1-13(c)). Reflective mirrors, lens, and scratch drive actuator are integrated in a single chip. However, the optical sensing component does not integrated in this chip.

In the above systems, few of them integrate actuators and optical sensors in a single chip. In the proposed spot profile measurement system, we will demonstrate micro actuator, photo sensor, and circuit on the same chip.

1.4.3 Devices in CMOS MEMS

MEMS structures can be integrated with circuit components by standard CMOS process. For the absorption type knife edge scanning device, a fully integrated system including circuits is an important target to handle complex signal processing in real-time.

Comb structures are widely used for actuation, capacitive position sensing and frequency tuning. Accelerometers [14], gyroscopes [15], and variable capacitors [16] contain comb structures as part of the MEMS structure. A released z-axis accelerometer fabricated by thin-film CMOS-MEMS process is shown in Fig. 1-14. The z-axis comb is used to capacitive sensing out-of-plane acceleration. The stator and the rotor which form a Wheatstone bridge can convert the capacitive change into voltage signal.

The comb finger structure with ring shape is shown in Fig. 1-15. The capacitance of this structure is changed by applying a voltage between the stator and rotor. This variable capacitance can be applied in radio frequency (RF) system.

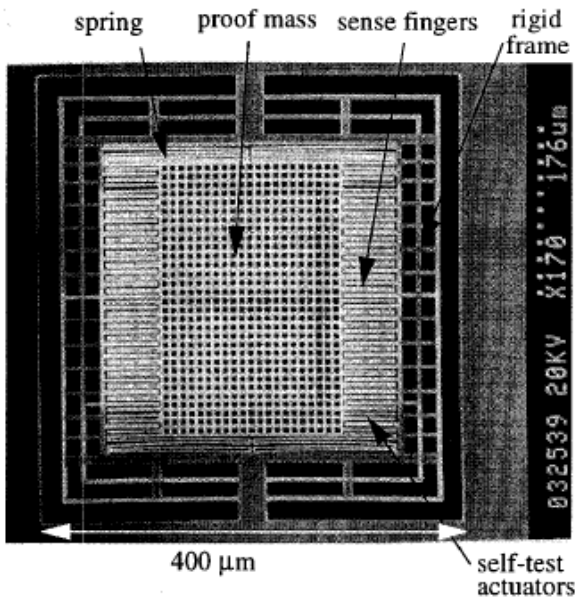


Fig. 1-14 Sensing comb fingers in microstructure [14]

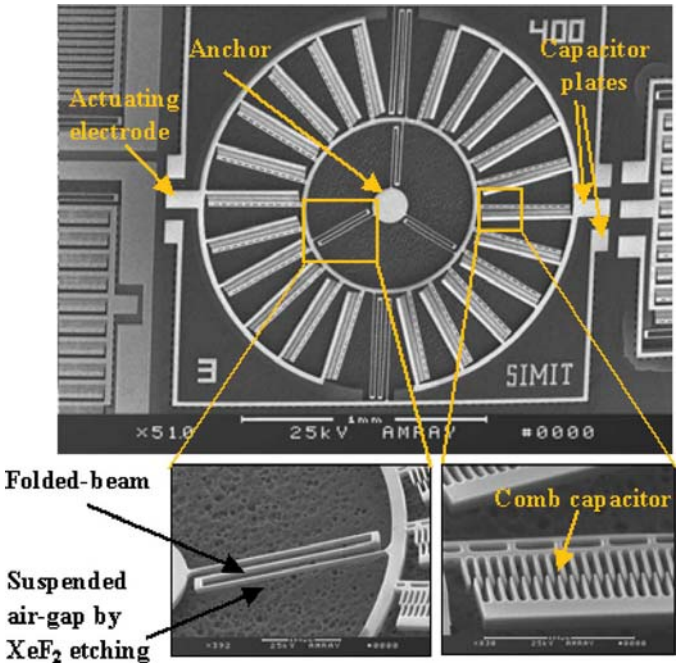
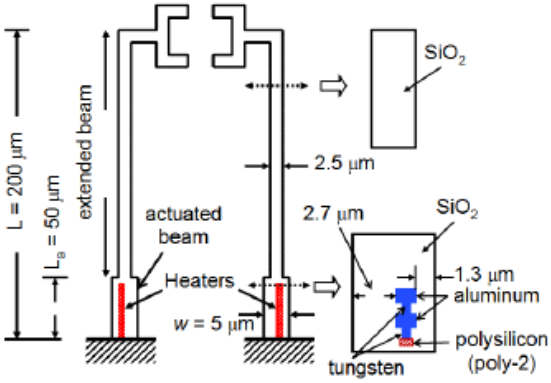


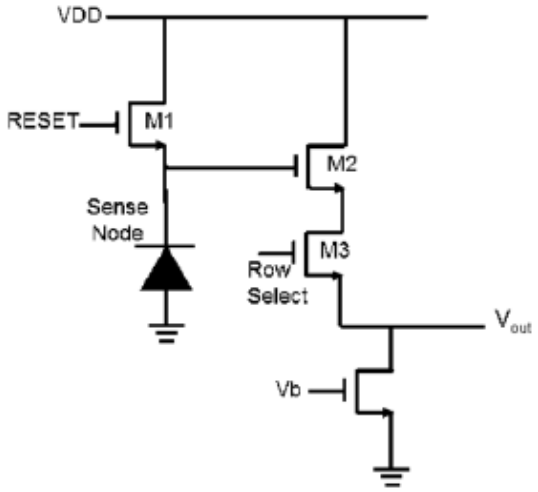
Fig. 1-15 Ring-shaped tunable capacitance [16]

CMOS active pixel sensors (APS) can be integrated with a micro gripper to judge whether the gripper is grabbing an object [17]. The gripper is composed by poly2, aluminum, tungsten, and silicon dioxide layers. The poly2 is used to be a heater. The thermal of aluminum and silicon dioxide rises up when energy is applying to heater. The gripper is actuated laterally due to different thermal expansion coefficient

between aluminum and silicon dioxide (Fig. 1-16(a)). Therefore, the micro gripper can grab an object. The photo detector behind the micro gripper is connected with an active pixel circuit (Fig. 1-16(b)). Transistor M2 is used to be a source follower. The output voltage of this active pixel circuit changes when the gripper is laterally actuated to grab an object and photo detector detects partial energy of the incident light.



(a)



(b)

Fig. 1-16 (a) Micro gripper with photo detector (b) an active pixel circuit [17]

From the above literature, the comb structure and optical sensing element can be fabricated by post CMOS-MEMS process. In the absorption type system, the knife edge must be driven laterally. Therefore, the configuration similar to [14] is used as the comb drive actuator. The optical sensing element is integrated with the comb structure.

1.5 Objectives and thesis organization

From the above survey, both the comb actuator and optical sensor can be fabricated by CMOS and its post process. Therefore, the CMOS MEMS device is suitable for integrating the electro-optical components and signal processing circuits in a single chip. The objective is to develop a CMOS MEMS-based optical spot measurement system based on the knife edge method. The fabrication and measurement results of the absorption type device will be demonstrated.

The design and simulation results will be given in Chapter 2. The fabrication process and issues are discussed in Chapter 3. The measurement results will be presented in Chapter 4. In Chapter 5, the conclusion and future work will be given.

Chapter 2 Design of spot profiler system

The system contains a photo detector which is actuated by a comb drive actuator and scans across the focused spot to measure its profile. A transimpedance circuit converts the current signal to a voltage signal. Additionally a position sensor is used to sense the displacement of the comb drive actuator. In this chapter, the design of the comb drive actuator, photo detector, circuit, and position sensor will be discussed.

2.1 Actuator design

The comb actuator with folded springs operates at resonant frequency to scan across the spot by applying a voltage between the rotor and the stator. The comb will be analyzed by both theory and simulation by finite element method (FEM).

2.1.1 Spring design

The folded spring is used in the design to minimize the area of the device and apply large linear deflection range (Fig. 2-1). In this structure, the spring constant can be calculated from [18]:

$$k_x = \frac{2Etw^3}{L^3}\frac{L_t^2 + 14\alpha L_t L + 36\alpha^2 L^2}{4L_t^2 + 41\alpha L_t L + 36\alpha^2 L^2}, \quad (1)$$

where E is the Young's modulus, t is the thickness of the spring, w is the width of the spring, L is the spring length, w_t is the width of the truss beam, L_t is the length of the truss beam and $\alpha = (w_t / w)^3$.

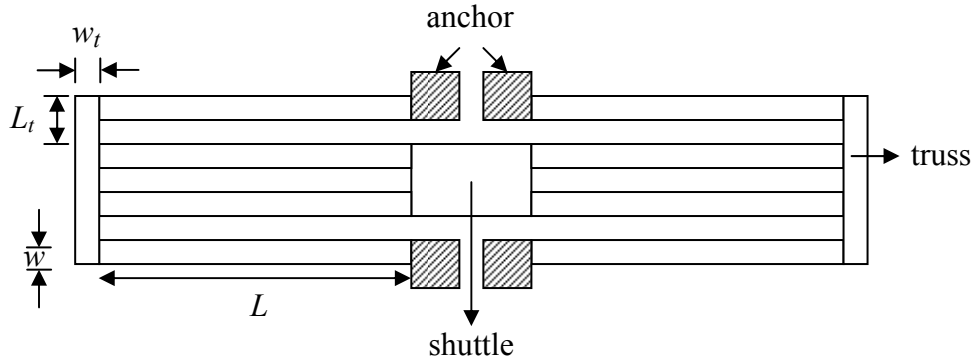


Fig. 2-1 Folded flexure structure

For the composite material layers in the device, the equivalent Young's modulus E_{eq} is calculated by the following equation [19]:

$$E_{eq}I_{eq} = \sum_j E_j I_j, \tag{2}$$

where I_{eq} is the moment of inertia of the composite beam and I_j is the moment of inertia of the jth layer. According the parallel theorem, I_{eq} and I_j can be calculated by the following equation:

$$I_j = \frac{wt_j^3}{12} + wt_j d_j^2, \tag{3}$$

where w is the width of the structure, t_j is thickness of the jth layer, d_j is the distance between the centurial axis of the composite beam and the neutral axis of the jth film.

2.1.2 Comb fingers design

In this system, the comb actuator moves laterally. A finger pair is shown in Fig. 2-2. To simplify the analysis, the fingers are modeled as a parallel plate capacitor and can be expressed as:

$$C = \frac{2N\varepsilon_0 t(x + x_0)}{g}, \tag{4}$$

where N is the number of fingers in one side, ε_0 is the dielectric constant of air, t is the thickness of the fingers, x_0 is the overlap of the fingers, x is the displacement of the comb, and g is the finger gap.

The electrostatic force of the comb F_x when a voltage V is applied between the

stator and the rotor is:

$$F_x = \frac{1}{2}\frac{\partial C}{\partial x}V^2 = \frac{N\varepsilon_0 t}{g}V^2. \tag{5}$$

The spring also applies a force to pull the rotor fingers back. The force of spring F_s can be expressed as:

$$F_s = k_x x. \tag{6}$$

When the electrostatic force of the comb is equal to the force of spring to pull back the rotor fingers, the displacement x can be determined and expressed in Eq. (7):

$$\frac{N\varepsilon_0 t}{g}V^2 = k_x x \Rightarrow x = \frac{N\varepsilon_0 t}{gk_x}V^2. \tag{7}$$

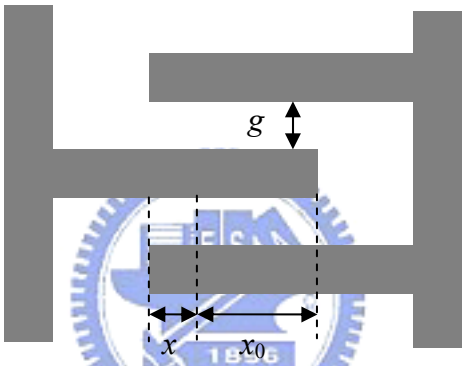


Fig. 2-2 Schematic of a comb finger pair

The actuator is operated in the lateral resonant mode to obtain the largest displacement. The resonant frequency can be obtained from Rayleigh's quotient [20] and expressed as:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_x}{M_{shuttle} + \frac{1}{2}M_{truss} + \frac{96}{35}M_{spring}}}, \tag{8}$$

where $M_{shuttle}$ is the mass of the shuttle, M_{truss} is the mass of the single truss and M_{spring} is the mass of a single spring.

2.1.3 CMOS MEMS device in D35-95D

The device is to be fabricated by the TSMC 2P4M 0.35μm process and post CMOS process. Chips taped out in D35-95D are post processed by dry etching only. The cross section view of the chip is shown in Fig. 2-3. The finger gaps are designed to be 2 μm due to the limitation of the post process capability. The thickness of comb fingers composed of three oxide layers and three metal layers is 5.045 μm (Fig. 2-4). A mesh structure is used to release structure.

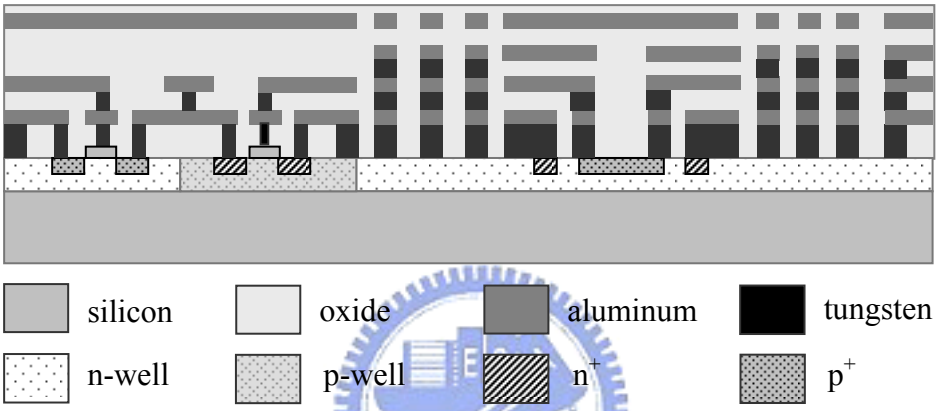


Fig. 2-3 Cross section view of chip in D35-95D group

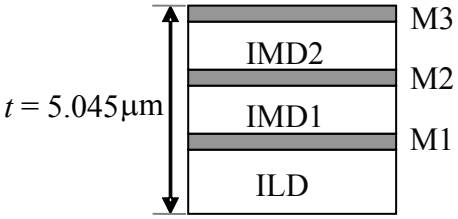


Fig. 2-4 Structure cross section view of fingers in Fig. 2-3

Table 2-1 Thickness of each layer in D35-95D

layer	material	thickness
M3	aluminum	0.64 μm
IMD2	oxide	1 μm
M2	aluminum	0.64 μm
IMD1	oxide	1 μm
M1	aluminum	0.665 μm
ILD	oxide	1.1 μm

The quality factor is assumed to be 10 for the uncertainty of the quality factor. For a ±10 μm amplitude in the resonant frequency, a static displacement of 1 μm is needed. The length of longer spring is designed to be 280 μm and the finger number is 40 to satisfy the limitation of the tape out area (2500×2500 μm^2). The proof mass can be calculated from the equivalent density and the volume. The equivalent density ρ_{eq}

can be expressed as:

$$\rho_{eq} = \frac{\rho_{Al} t_{Al} + \rho_{oxide} t_{oxide}}{t_{total}}, \tag{9}$$

where t_{total} is the thickness of the structure, t_{Al} is the total thickness of the metal layers in the structure, t_{oxide} is the total thickness of the dielectric layers in the structure, ρ_{Al} is the density of the aluminum and ρ_{oxide} is the density of the oxide layers. From the above discussion, the calculation results of the spring constant k_x and the proof mass M are 1.65 N/m and 3.4×10^{-10} kg. Therefore, the resonant frequency is calculated to be 12.1 kHz. To release the structure, opening holes sized from 4×4 μm^2 to 8×8 μm^2 are distributed on the device to help undercut the substrate. The detail parameters are shown in Table. 2-2 and the layout of the comb actuator is shown in Fig. 2-5. The full layout of D35-95D device is shown in Fig. 2-6.

Table 2-2 Design parameters of the D35-95D device

Parameter	Dimension	Unit	Parameter	Dimension	Unit
spring length L_1	280	μm	triangle base l	20	μm
spring length L_2	150	μm	triangle height h	10	μm
spring width w	4	μm	thick finger w_{fl}	6	μm
finger length L_f	60	μm	width r	4	μm
finger width w_f	2	μm	width t_1	4	μm
overlap x	15	μm	thickness t	5.045	μm
gap spacing g	2	μm	density ρ	2.33	g/cm^3
truss length L_t	110	μm	proof mass M	3.4×10^{-10}	kg
truss width w_t	4	μm	Young's modulus E	70	GPa
shuttle length a	74	μm	spring constant k_x	1.65	N/m
shuttle width b	64	μm	finger number n	40	
release hole h_1	4	μm	applied voltage V	100	volts
release hole h_2	6	μm	device area	800×450	μm^2
release hole h_3	8	μm	resonance freq. f_0	12.1	kHz
release hole h_4	6	μm	Quality factor	10	
release hole h_5	5.5	μm	static displacement amplitude @ 100V	1	μm
release hole h_6	2.5	μm			
length C_1	322	μm	total displacement	±10	μm

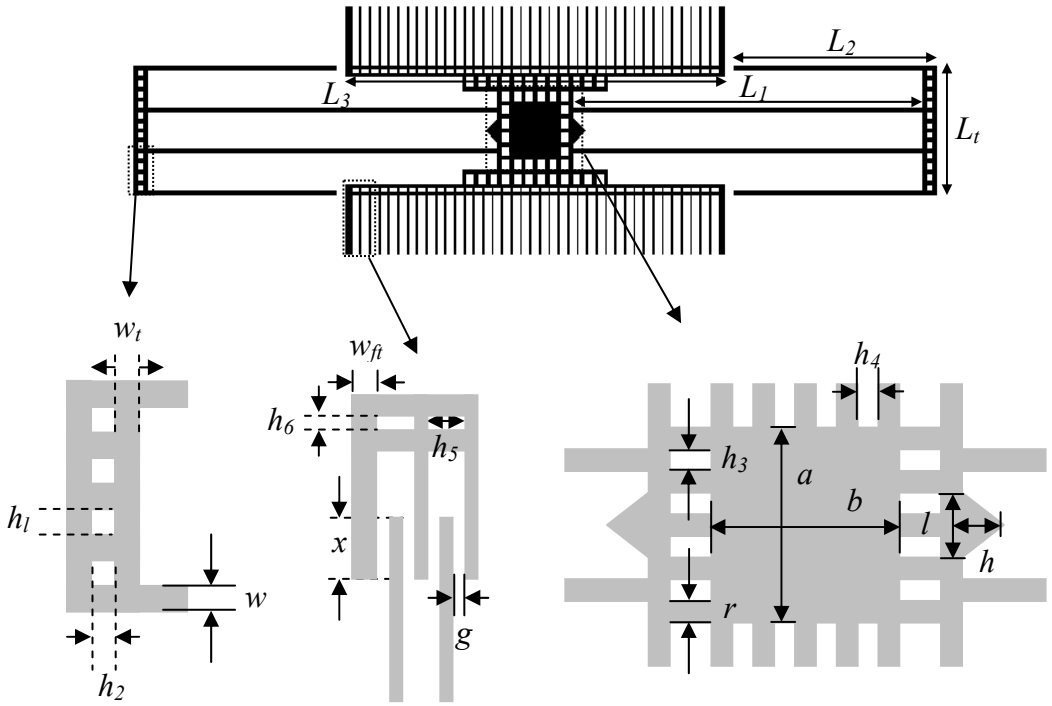


Fig. 2-5 Layout of absorption type comb actuator

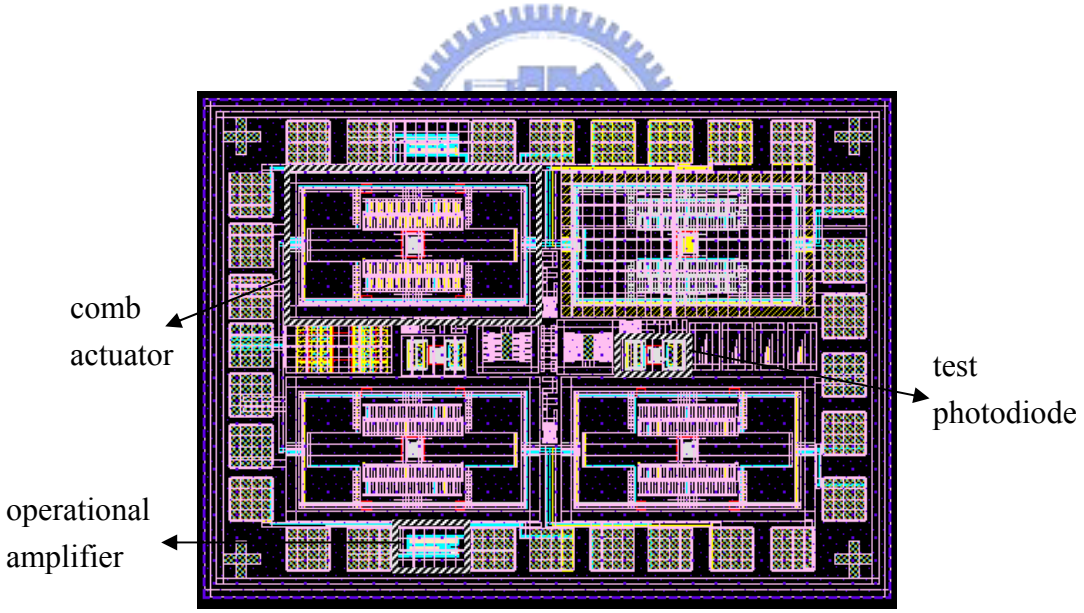


Fig. 2-6 Full layout of D35-95D chip

This device is simulated by CoventerWare. The simulation result of the D35-95D device is shown in Fig. 2-7. The silicon substrate thickness of the movable part is 20 μm. The first mode (lateral mode) is 13.7 KHz. The device is operated in this mode. The second mode is 14.7 KHz (vertical mode) and the third mode is 22.7 KHz

(torsional mode).

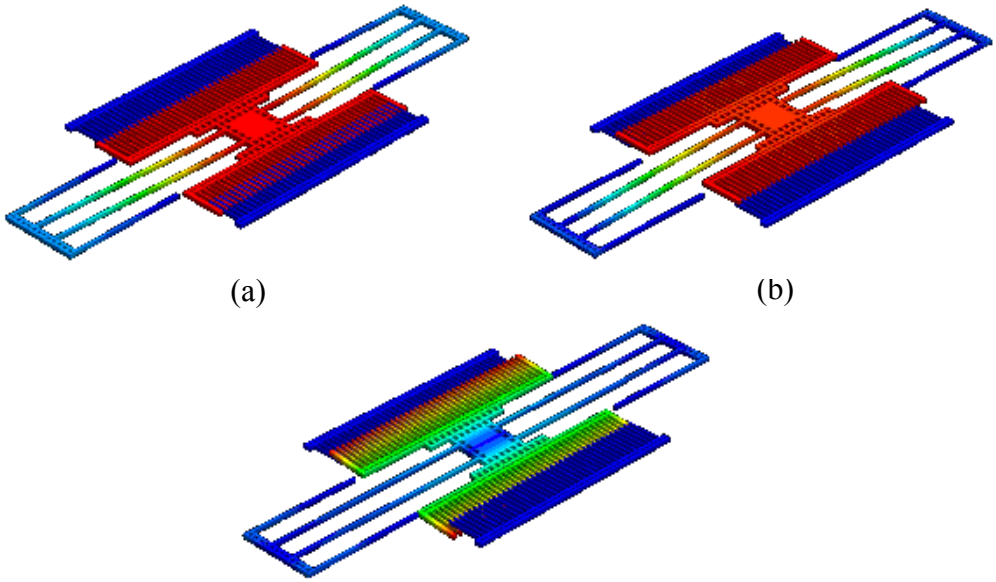


Fig. 2-7 Simulation results of D35-95D device (a) lateral mode, (b) vertical mode, and (c) torsional mode

2.1.4 CMOS MEMS device in D35-96A

In this device, poly1 layer is used as a piezoresistor material to form position sensor. The cross section view of D35-96A is shown in Fig. 2-8. The piezoresistors are covered by oxide. Therefore, piezoresistors can be protected during release process. After post process, the structure contains three metal and three oxide layers.

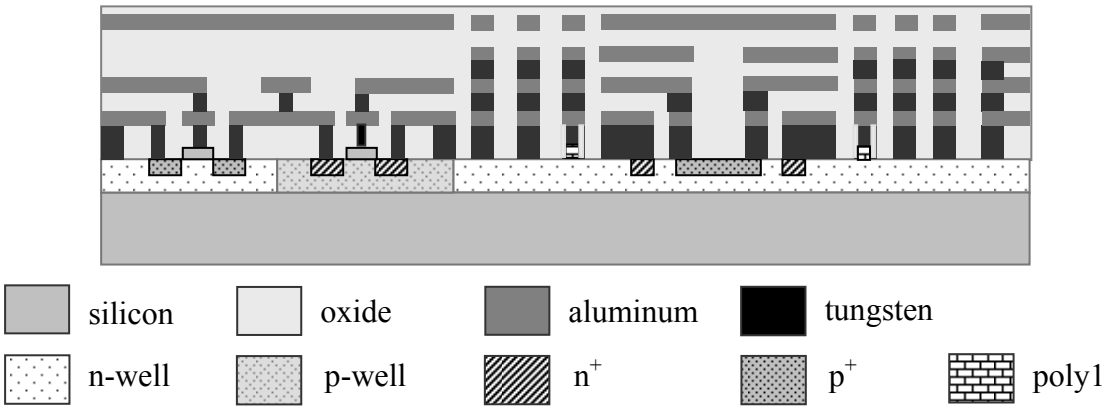


Fig. 2-8 Cross section view of chip in D35-96A group

The other design parameters are the same as D35-95D device as listed in Table 2-2. The spring constant k_x and proof mass M are 1.65 N/m and 3.4×10^{-10} kg. Therefore, the calculated resonant frequency is 12.1 kHz. The mode shapes and corresponding resonant frequency is the same as Fig. 2-7. The full layout view is shown in Fig. 2-9.

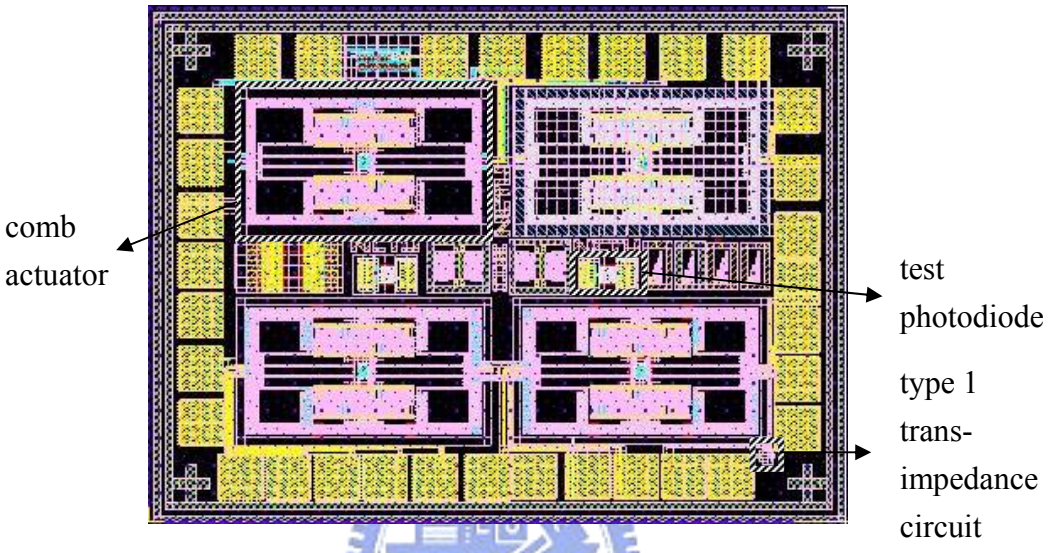


Fig. 2-9 Full layout of D35-96A chip

2.1.5 CMOS MEMS device in D35-97C

In chips taped out in D35-97C, the dielectrics between comb fingers, springs, and mesh structure are replaced by stacked metal layers. The metal layer is etched by H_2SO_4 and H_2O_2. The cross section view of the chip is shown in Fig. 2-10. After the post process, the structure contains four metal and four oxide layers. The thickness of comb fingers composed of four oxide layers and four metal layers is 6.97 μm (Fig. 2-11).

The design parameters are the same as the D35-95D device except for the fingers and spring (Table 2-4). The comb finger is covered by silicon oxide due to the limitation of the design rules. A 0.8 μm space must exist between the metal to be etched and the metal in comb fingers and spring. The width of spring changes from 4

μm to 5 μm.

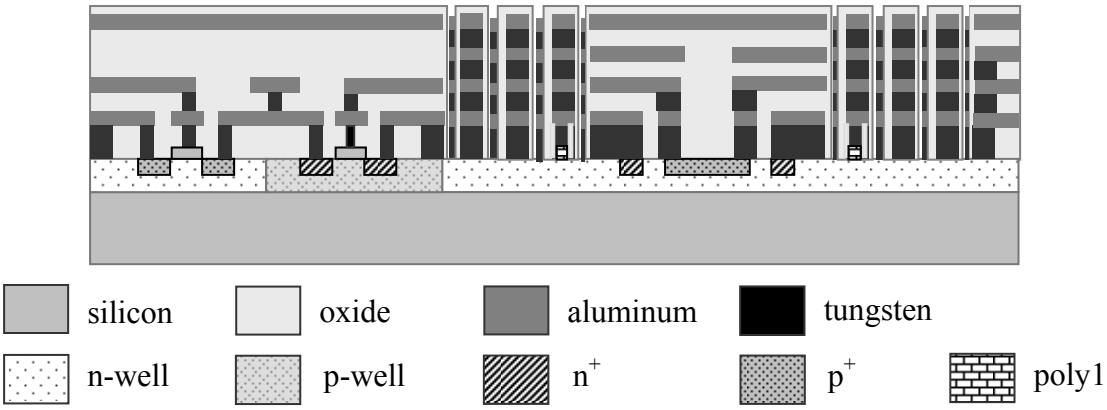


Fig. 2-10 Cross section view of chip in D35-97C group

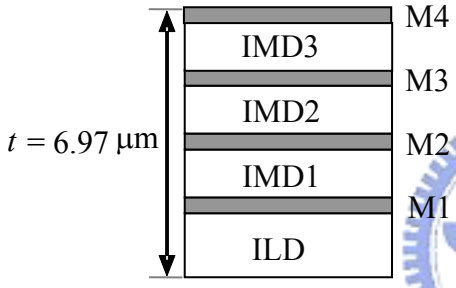


Fig. 2-11 Structure cross section view of fingers in Fig. 2-10

Table 2-3 Thickness of layers in D35-97C

layer	material	thickness
M4	aluminum	0.925 μm
IMD3	oxide	1 μm
M3	aluminum	0.64 μm
IMD2	oxide	1 μm
M2	aluminum	0.64 μm
IMD1	oxide	1 μm
M1	aluminum	0.665 μm
ILD	oxide	1.1 μm

The thickness of the structure is 6.97 μm. Therefore, the spring constant k_x in this device is 3.78 N/m and the proof mass M is 4.7×10^{-10} kg. The resonant frequency is calculated to be 14.3 kHz.

The model is simulated by CoventerWare. The silicon substrate of the movable part is 20 μm. For the D35-97C design, the first mode (lateral mode) is 24.2 kHz. The device is operated in this mode. The second mode is 35.9 kHz (vertical mode) and the third mode is 44.1 kHz (torsional mode). The simulation result is shown in Fig. 2-12. The full layout view is shown in Fig. 2-13.

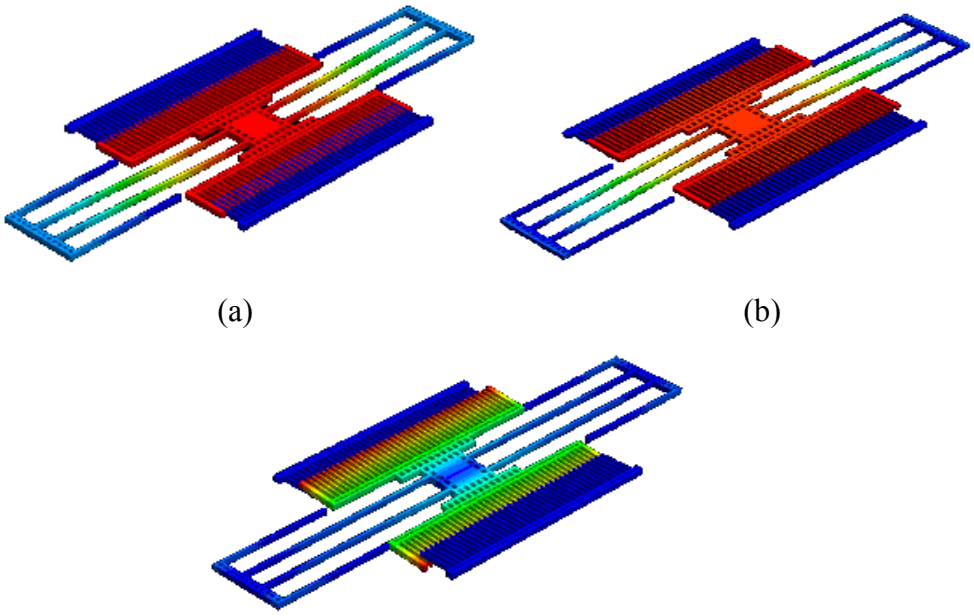


Fig. 2-12 Simulation results (a) lateral mode, (b) vertical mode, and (c) torsional mode

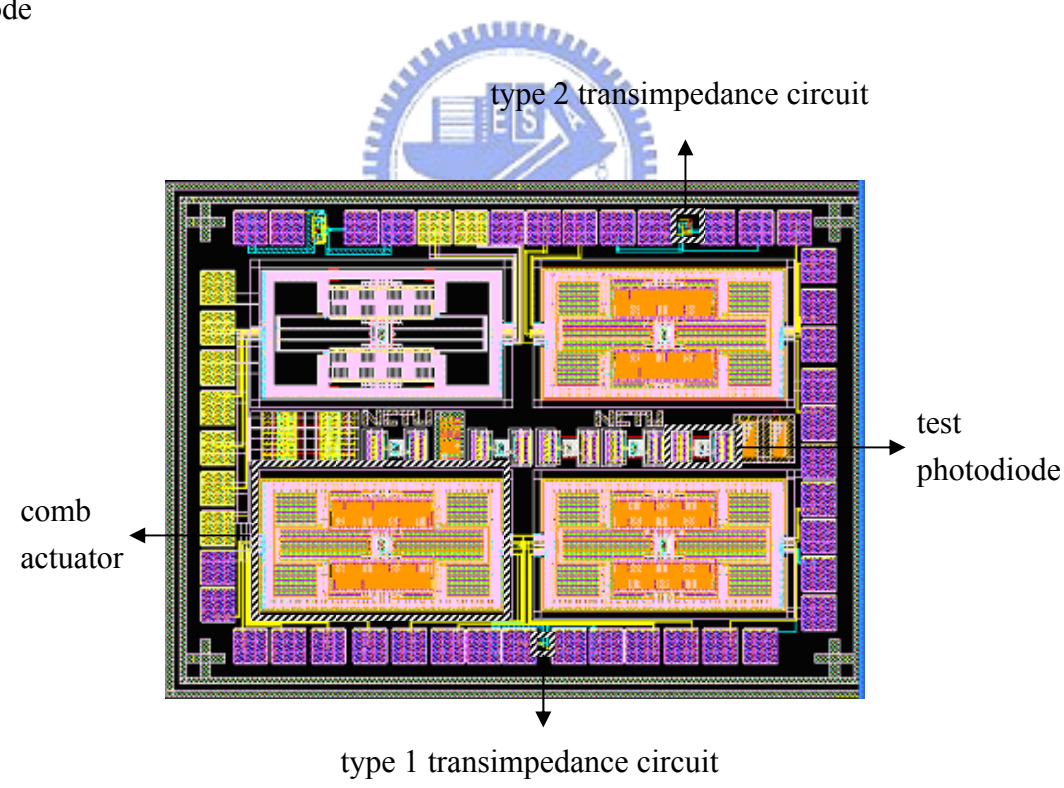


Fig. 2-13 Full layout of D35-97C chip

Table 2-4 CMOS comb actuator layout parameters for D35-97C

Parameter	Dimension	Unit	Parameter	Dimension	Unit
spring length L_1	280	μm	triangle base l	20	μm
spring length L_2	150	μm	triangle height h	10	μm
spring width w	5.6	μm	thick finger w_{fl}	6	μm
finger length L_f	60	μm	width r	4	μm
finger width w_f	2	μm	width t_1	4	μm
overlap x	15	μm	thickness t	5	μm
gap spacing g	2	μm	density ρ	2.33	g/cm^3
truss length L_t	110	μm	proof mass M	4.7×10^{-10}	kg
truss width w_t	4	μm	Young's modulus E	70	GPa
shuttle length a	74	μm	spring constant k_x	3.78	N/m
shuttle width b	64	μm	finger number n	40	
release hole h_1	4	μm	applied voltage V	60	volts
release hole h_2	6	μm	device area	800×450	μm^2
release hole h_3	8	μm	resonance freq. f_0	14.3	kHz
release hole h_4	6	μm	Quality factor	10	
release hole h_5	5.5	μm	static displacement	1	μm
release hole h_6	2.5	μm	amplitude @ 60V		
length C_1	322	μm	total displacement	±10	μm

2.2 Photo detector and circuit design

In the absorption type system, silicon photodiode is used to detect light with wavelength ranging from 100 nm to 1100 nm. The photo detector is formed by the N-well and p^+ layers in the TSMC 2P4M 0.35 μm process. A transimpedance circuit is integrated with the photo diode to convert the photocurrent to a voltage signal.

2.2.1 Design of the photo detector

In a silicon photodiode, the incident light generates the electron-hole pairs in the depletion region. The applied electric field separates the electron-hole pairs and produces photo current.

The top view of the photodiode is shown in Fig. 2-14. The N-well is used to be a signal isolation between photocurrent and actuating signal of comb actuator. The p^+ region is used to form the p-n junction between the N-well and p^+. The n^+ can apply an ohmic contact to the N-well. The conduction layer is designed to be a right-triangular region to form the knife-edge detection area. The bottom is 30 μm and the height of the right-triangular region is 15 μm. The photocurrent is transferred by aluminum layer for further signal processing.

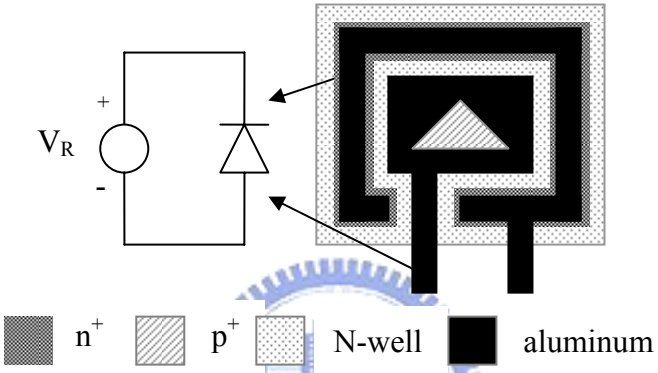


Fig. 2-14 Top view of the photo diode

2.2.2 Circuit design

Trans-impedance circuit can transfer the photocurrent to a voltage signal. From the seniors work, the photocurrent produced from photodiode is about 1 μA. Therefore, the trans-impedance of the circuit should design to be 1 MΩ to obtain 1V output signal.

Two kinds of transimpedance circuit are designed. The type 1 circuit is a two stage transimpedance circuit (Fig. 2-15). The first stage composed of transistors M_{p1}, M_{n1}, and M_f is used to convert photocurrent to voltage signal. Transistor M_f is operated in triode region to serve as a resistor. The second stage composed of transistors M_{p2} and M_{n2} is used to amplify the voltage signal from output signal of the first stage.

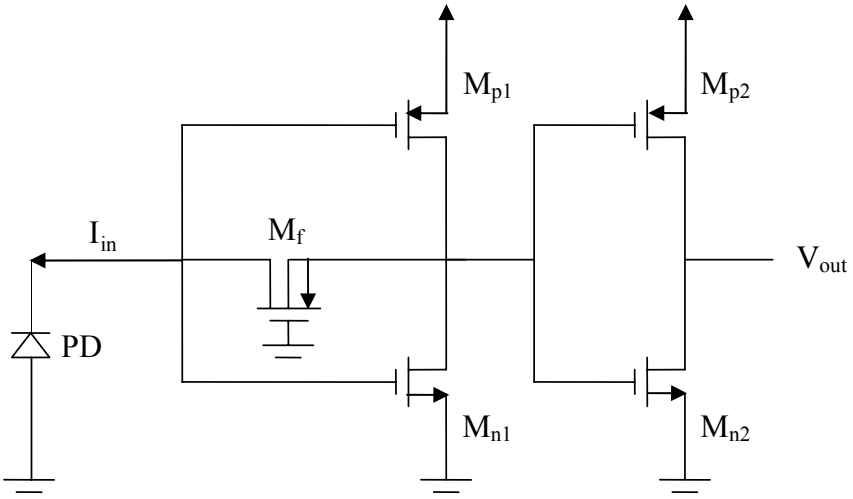


Fig. 2-15 Type 1 transimpedance circuit

The transimpedance of the first stage is express as:

$$A_1 = \frac{(r_{o_{n1}} \| r_{o_{p1}})[1-(g_{m_{n1}} + g_{m_{p1}})R]}{1+(r_{o_{n1}} \| r_{o_{p1}})(g_{m_{n1}} + g_{m_{p1}})} \tag{10}$$

where A_1 is the transimpedance gain, R is the equivalent resistance of M_f. The voltage gain of the second stage A_2 is express as:

$$A_2 = (g_{m_{n2}} + g_{m_{p2}})(r_{o_{n2}} \| r_{o_{p2}}) \tag{11}$$

Therefore, the overall transimpedance of this circuit is

$$A_1 \times A_2 = \frac{(r_{o_{n1}} \| r_{o_{p1}})[1-(g_{m_{n1}} + g_{m_{p1}})R]}{1+(r_{o_{n1}} \| r_{o_{p1}})(g_{m_{n1}} + g_{m_{p1}})}(g_{m_{n2}} + g_{m_{p2}})(r_{o_{n2}} \| r_{o_{p2}}), \tag{12}$$

where $g_m = \frac{2I_D}{V_{gs} - V_t}$ and $r_o = \frac{1}{\lambda I_D}$.

The product of carrier mobility and gate capacitance per unit area k', threshold voltage V_t, and channel length modulation parameter λ of NMOS and PMOS are listed in Table 2-4.

Table 2-4 Process parameters of NMOS and PMOS

parameter	k' (μA/V×S)	V_t (V)	λ (V^{-1})
NMOS	153.7	0.54	0.04
PMOS	57.3	-0.747	0.035

The power of the circuit is limited below 0.4 mW. For a circuit with 3.3V power supply, 60 μA is limited to flow through M_{p1}, M_{n1}, M_{p2}, and M_{n2}. The DC level of the gate voltage in all transistors except M_f is assumed to 1.65V to obtain the maximum output voltage swing. Therefore, g_m is calculated to be 0.108 mA/V in NMOS and 0.133 mA/V in PMOS. $(\frac{W}{L})_{n2}$ and $(\frac{W}{L})_{p2}$ are calculated to be 1 and 5. r_o is calculated to be 416.67 KΩ and 476.16 KΩ. From the above calculation, the voltage gain of the second stage is 53.56 V/V.

The g_m and r_o of M_{n1} and M_{p1} are assumed to equal to M_{n2} and M_{p2}. Therefore, $(\frac{W}{L})_{n1}$ and $(\frac{W}{L})_{p1}$ are also 1 and 5. The transimpedance gain can be obtained from the following equation:

$$A_1 = 18670.65 = \frac{222.26\times10^3\times[1-R\times0.241\times10^{-3}]}{1+53.56}. \qquad (13)$$

Table 2-5 Size of each transistor

MOS	Type	W(μm)	L(μm)
M_{n1}	n	0.4	0.4
M_{p1}	p	2	0.4
M_f	p	0.4	0.4
M_{n2}	n	0.4	0.4
M_{p2}	p	2	0.4

Therefore, R can be calculated to be 14.85 KΩ. The equivalent resistance in triode region of a transistor can be expressed as:

$$R = \frac{1}{k_p'(\frac{W}{L})_{M_f}[|(V_{gs} - V_t)| - |V_{ds}|]}. \quad (14)$$

From the above discussion, $(\frac{W}{L})_{M_f}$ is calculated to be 1. The sizes of the transistors of this circuit are listed in Table 2-5.

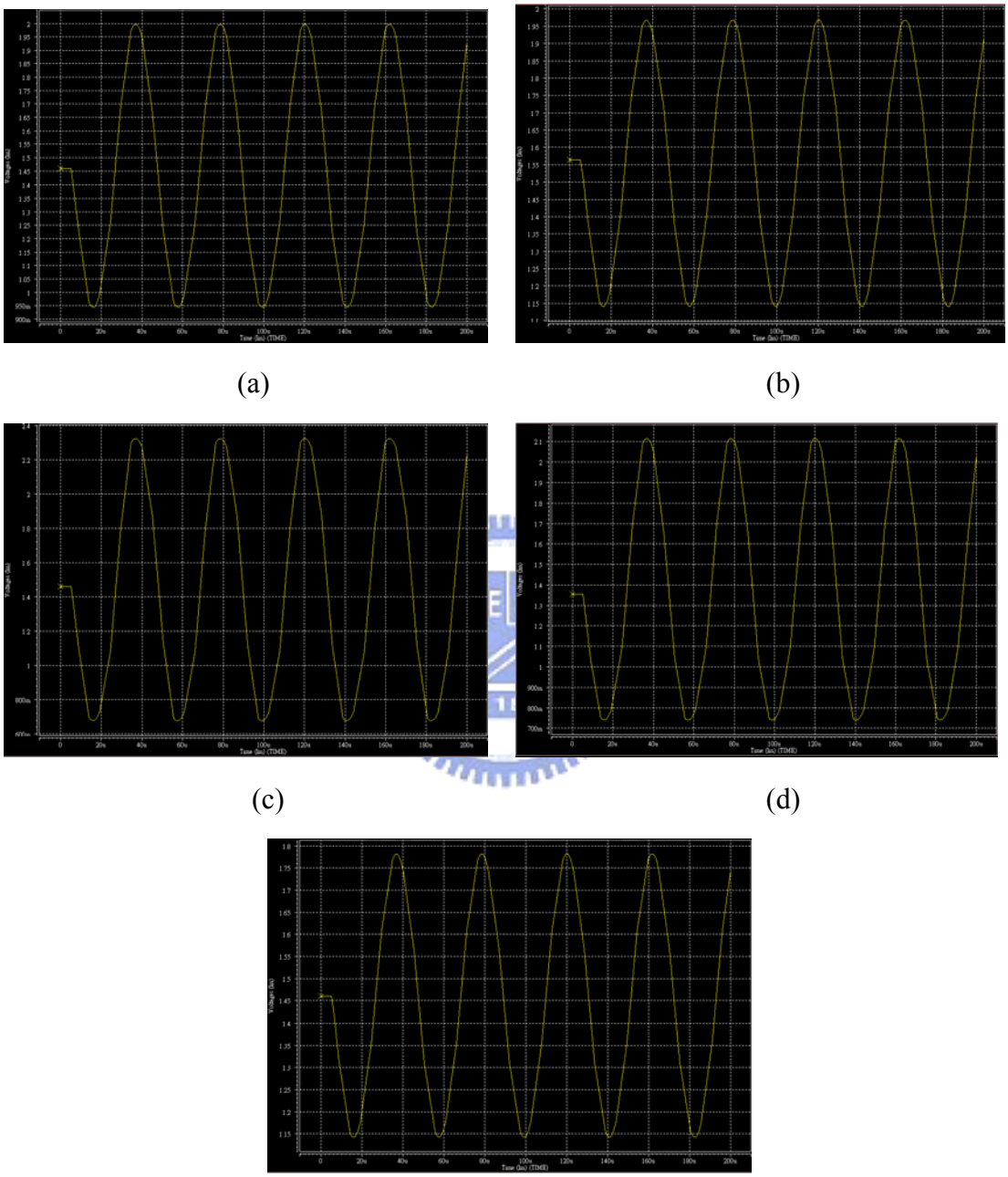
Table 2-6 Simulation result of each corner

Corner	TT	SF	SS	FS	FF
Transimpedance (Ω)	588.59K	443.35K	1.09M	842.83K	336.05K
3dB bandwidth (Hz)	206K	188K	116K	168K	256K
DC level (V)	1.45	1.55	1.45	1.35	1.45

The circuit is simulated by Hspice. The power supply is set as 3.3V and the impedance of output node is set as the input impedance of frequency response analyzer (FRA-5087). The value of this input impedance is 1MΩ//10pF. The transimpedance of this circuit in the five corners is listed in Table 2-6. The transient responses of five corners are also simulated. The simulation results are shown in Fig. 2-16. The input current is 1 μA and the frequency is 13.7 KHz. The DC levels of the five corners are also listed in Table 2-6.

Type 2 transimpedance circuit is also designed. An operational amplifier and a feedback resistor form this circuit (Fig. 2-17). To minimize the layout area, the feedback resistor is replaced by a NMOS transistor which is operated in the triode region. The operational amplifier contains of differential amplifier, bias circuit and an output stage (Fig. 2-18). The bias circuit applies the bias voltage at half of the power

supply voltage so that the upper and lower voltage swing ranges are the same. The output stage applies the larger power to drive the loads in the output node.



(a) (b)

(c) (d)

(e)

Fig. 2-16 Transient response of type 1 circuit in (a) TT (b) SF (c) SS (d) FS (e) FF corner

Transistors M1 to M5 are used to form a differential amplifier and work in the saturation region. The limitation of the current flowing through M5 is 15 μA. The gain of the differential amplifier is equal to the following equation:

$$A_d = g_{m2}\left(r_{o2} \| r_{o4}\right). \tag{15}$$

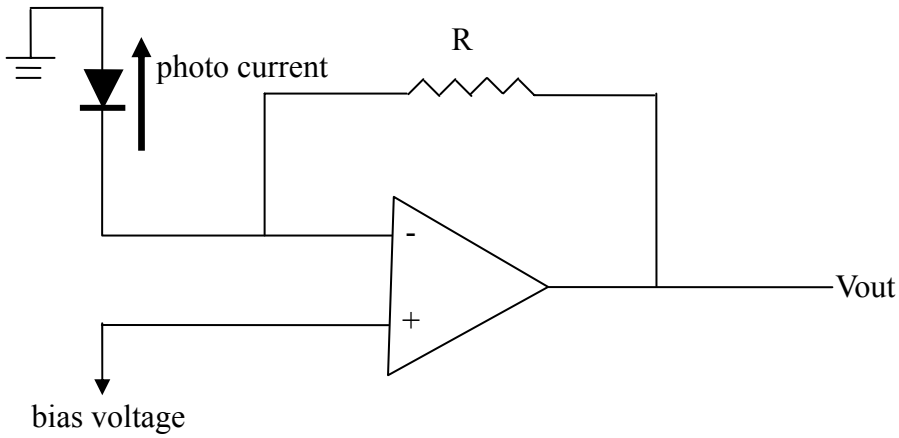


Fig. 2-17 Type 2 transimpedance circuit

Assume the current flowing M_1 is equal to the current flowing through M_2, r_{o2} and r_{o4} are calculated to be 3.33 MΩ and 3.81 MΩ. g_{m2} can be calculated to be 214.56 μA/V. Therefore, the gain of the differential amplifier is calculated to be 381.46 V/V. The size of the transistor M_2 can be calculated by the following equation:

$$g_{m2} = \sqrt{2k_n'\left(\frac{W}{L}\right)_2 I_D} \tag{16}$$

Therefore, $\left(\frac{W}{L}\right)_2$ is calculated to be 20. The current flowing through M_4 is equal to current flowing through M_2. The value of $\left(\frac{W}{L}\right)_4$ can be obtained as 3.33. The size of M_1 is equal to M_2 and the size of M_3 is equal to M_4. The transistor size of M_5 can be calculated by the following equation:

$$I_D = \frac{1}{2}k_n'(\frac{W}{L})_5(V_{gs} - V_t)^2 \tag{17}$$

The gate voltage of M_5 is designed to be 0.6 volts to ensure the transistor can be turned on. Therefore, the value of $(\frac{W}{L})_5$ is calculated to be 28. Transistor M_r is operated in triode region to be a resistor. From equation (13), the value of $(\frac{W}{L})_{M_r}$ is calculated to be 0.12.

The output stage is used to be a buffer to apply low output resistance. The output resistance is limited to 100 KΩ to reduce the effect of the input resistance of oscilloscope. The output resistance can be expressed by:

$$R_o = \frac{1}{(\lambda_n + \lambda_p) I_D}. \tag{18}$$

From Table 2-4, the value of I_D is designed to be 133.33 μA. Therefore, $(\frac{W}{L})_7$ and $(\frac{W}{L})_6$ are calculated to be 1.14 and 6.

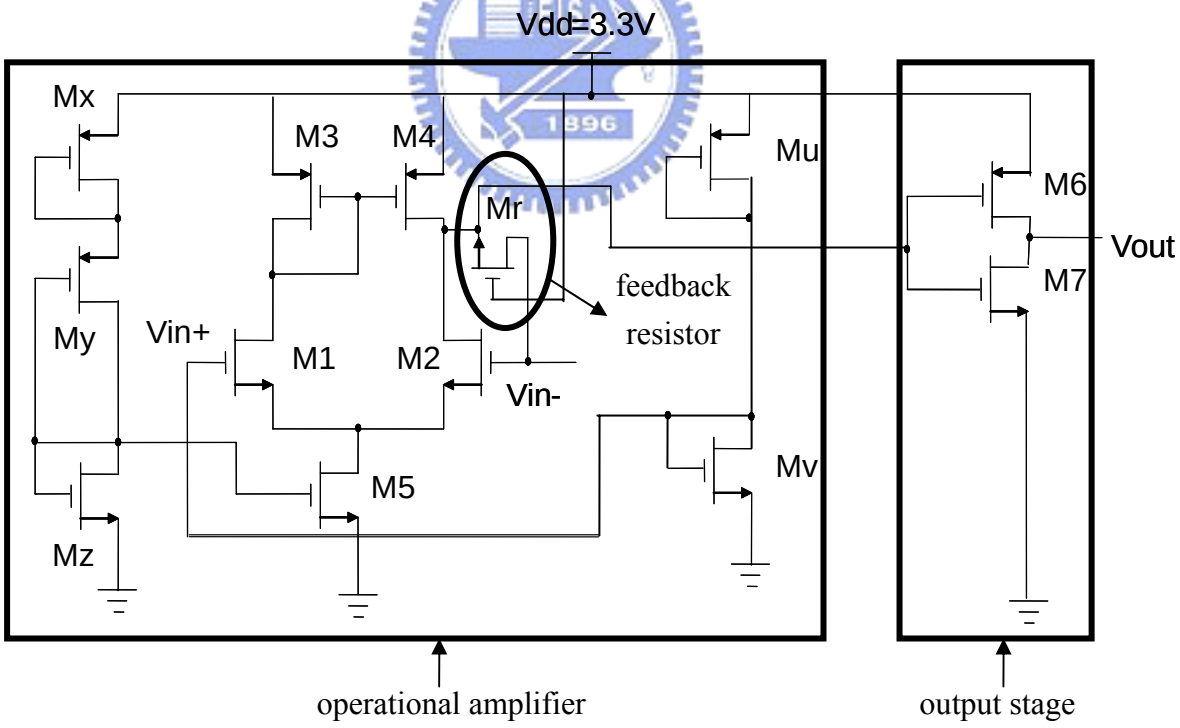
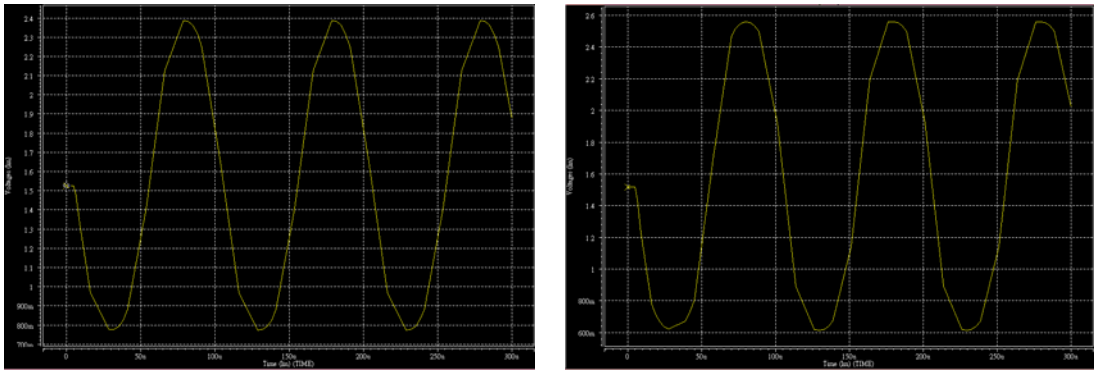
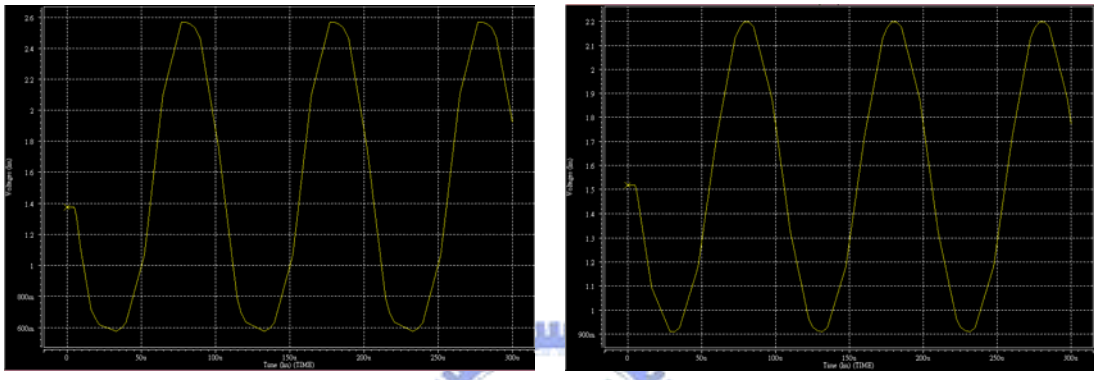


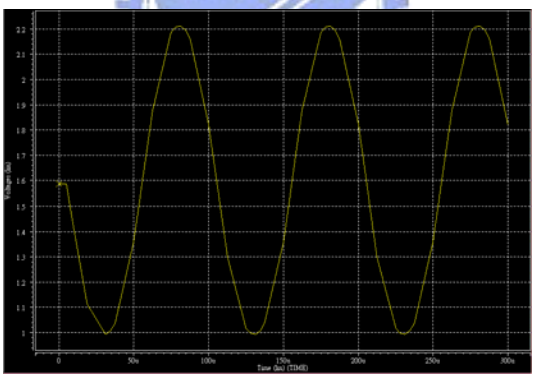
Fig. 2-18 Detail circuit schematic of type 2 circuit



(a) (b)



(c) (d)



(e)

Fig. 2-19 Transient response of type 2 circuit in (a) TT (b) SF (c) SS (d) FS (e) FF corner

The bias of the gate of M_1 is composed by M_u and M_v and the bias circuit for the gate of M_5 is composed by M_x, M_y, and M_z. The current flowing through M_u and M_y is equal to 10 μA and the current flowing through M_x, M_y, and M_z is 5 μA. By equation (17), the size of these transistors can be obtained. The size of each transistor in this tansimpedance circuit is listed in Table 2-7. The circuit is also simulated. The

conditions for simulation are the same as type 1 circuit except frequency of input current. The frequency of input current is 24.2 KHz. The simulation result is listed in Table 2-8. The waveforms of transient response are shown in Fig. 2-19.

Table 2-7 Size of each transistor

MOS	Type	W(μm)	L(μm)
Mx	p	1	1
My	p	1	1
Mz	n	9.47	1
M1	n	8	0.4
M2	n	8	0.4
M3	p	2.5	0.75
M4	p	2.5	0.75
M5	n	10	0.35
Mr	n	0.4	3.3
Mu	p	1.7	3.5
Mv	n	0.4	4
M6	p	2.12	0.35
M7	n	0.4	0.35

Table 2-8 Simulation result of each corner

Corner	TT	SF	SS	FS	FF
Transimpedance (Ω)	1.02M	1.55M	1.49M	739.74K	695.48K
3dB bandwidth (Hz)	300K	276K	232K	305K	368K
DC level (V)	1.53	1.50	1.40	1.51	1.60

2.2.3 Piezoresistive position sensor

The position sensor is a Wheatstone bridge circuit formed by four piezoresistors. In TSMC 0.35 μm process, poly1 layer is used for the piezoresistors. When the piezoresistors are under pressure, the resistivity of the piezoresistors is changed. The

piezoresistors are placed near the anchor to obtain maximum stress when the actuator is actuating.

The arrangement of the piezoresistors is shown in Fig. 2-20, the size of each piezoresistor is also described in Fig. 2-20. The thickness of each piezoresistors is 0.275 μm. The change of the resistivity can be calculated by the following equation:

$$\frac{\Delta R}{R} = \pi_l \sigma_l + \pi_t \sigma_t \tag{19}$$

where π_l is the coefficient of longitudinal piezoresistivity, σ_l is the longitudinal stress, π_t is coefficient of the transverse piezoresistivity, σ_t is the transverse stress. Because the direction of the current is parallel to the strain of the actuator, only the longitudinal stress needs to be considered.

The longitudinal stress can be obtained from the following equation:

$$\sigma_l = \frac{3Ebd_{\max}(L-x)}{2L^3} \tag{20}$$

where E is the Young's modulus of the spring, b is the spring width, $d_{\max}$ is the maximum displacement of the actuator, L is the spring length, and x is the distance between anchor and the piezoresistor. The length of piezoresistor is much shorter than the spring length. Therefore, the distribution of the stress on piezoresistor is almost linear distribution. In this case, E = 70 GPa, H = 4 μm, $d_{\max}$ =20 μm, L =280 μm and x =10 μm. The longitudinal stress σ_l can be calculated to be 90 MPa. The coefficient of the longitudinal piezoresistivity π_l is 3.15×10^{-10} Pa^{-1}. Therefore, the change of resistance $\frac{\Delta R}{R}$ can be calculated to be 2.98%. R is 160Ω in this design.

The four piezoresistors form a Wheatstone bridge (Fig. 2-21). In this circuit, if R_1 and R_3 are compressed, R_2 and R_4 are extended. Because the motion of the actuator is harmonic, the output of the circuit is expected to be a sinusoidal signal. The amplitude of the output signal can be obtained from the following equation:

$$V_o = \left(\frac{(\frac{\Delta R}{R})_1 + (\frac{\Delta R}{R})_2}{2(1 + (\frac{\Delta R}{R})_1 - (\frac{\Delta R}{R})_2)}\right) \times V_s \qquad (21)$$

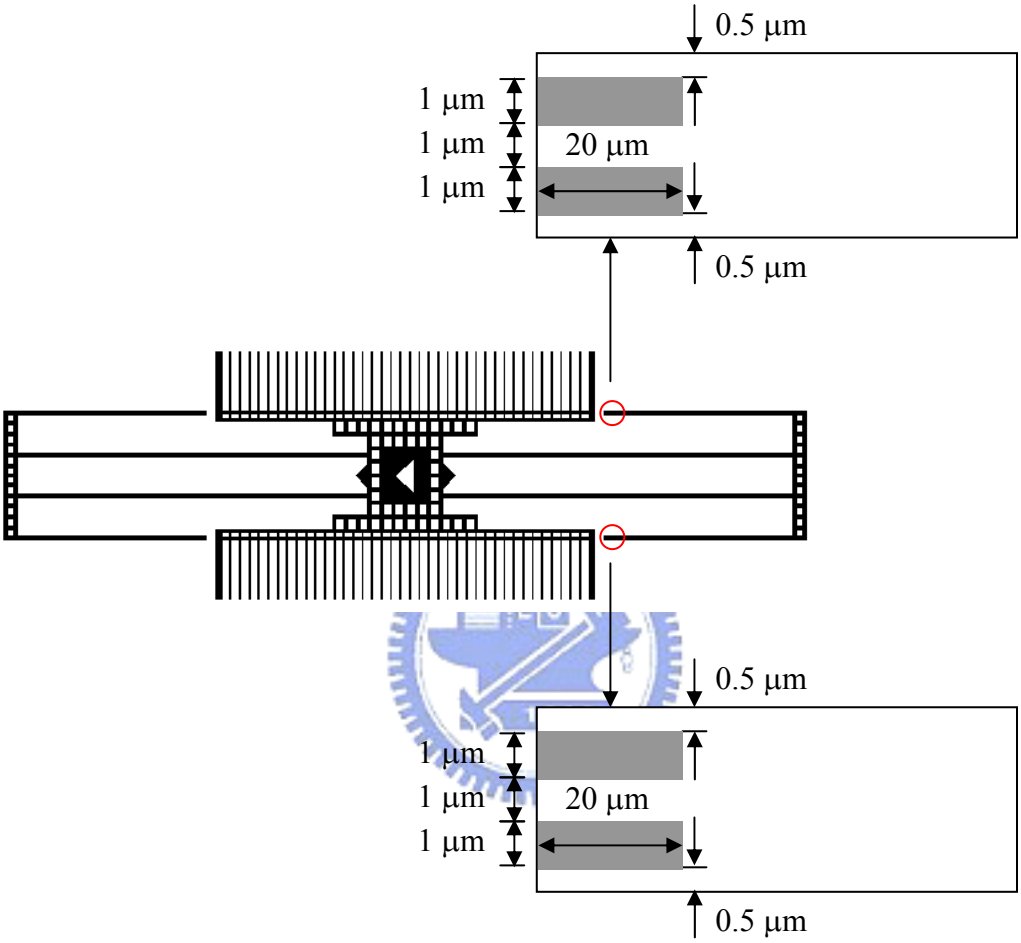


Fig. 2-20 Arrangement of piezoresistors

From the above discussion, $\frac{\Delta R}{R}$ is 2.98%. Therefore, the peak to peak amplitude of the output signal is 0.0298V_s. The change of the resistance of the piezoresistors can be simulated by CoventorWare. The change of the current flowing through the piezoresistor is 2.79%. Assume the voltage across a piezoresistor is V and the current flowing through non-compressed piezoresistor is I. The changing of the

piezoresistivity $\frac{\Delta R}{R}$ is $\frac{(\frac{V}{I-0.0279I})-(\frac{V}{I})}{\frac{V}{I}}=\frac{1}{0.9721}-1=2.87\%$. The simulation result is close to the calculation.

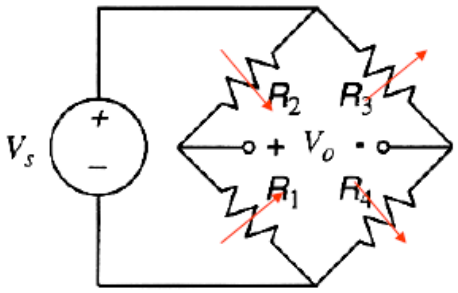


Fig. 2-21 Position sensor formed by a Wheatstone bridge

2.3 Conclusion

In this chapter, the comb drive actuator, photodiode, transimpedance circuit, and position sensor are designed. The characteristics of two kinds of CMOS devices are simulated. The measurement results of these devices will be discussed in chapter 4.

Chapter 3 Fabrication

The CMOS device taping out in D35-95D and D35-97C were fabricated with a post-CMOS MEMS process. After solving the fabrication problems, the device was successfully fabricated. These problems are discussed in this chapter and the fabrication results are presented.

3.1 Post CMOS in D35-95D device

3.1.1 Fabrication process

The CMOS process is the TSMC 2P4M 0.35 μm process (Fig. 3-1). After the standard CMOS process, post processing steps are used to suspend the movable structures.

To avoid hurting the frontside structure in the fabrication process, the post process begins with backside etching. Silicon oxide is first deposited and patterned on the backside to be a hard mask in backside silicon etching. In order to leave silicon substrate in the movable structures to be the photodiode, the backside silicon is etched

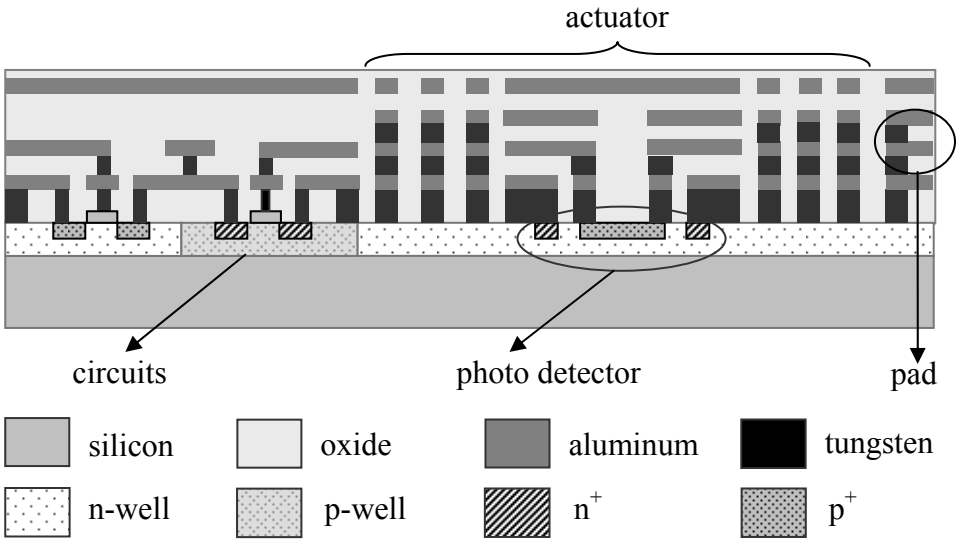


Fig. 3-1 Cross section view of CMOS device of D35-95D device

by inductively coupled plasma (ICP). The thickness of silicon is left between backside silicon etching, the frontside silicon oxide layer is etched by high density plasma reactive ion etching (HDP-RIE) to define the structure (Fig. 3-2(b)). The top metal layer (M4) is used to protect photo detector in frontside oxide etching process. Then the metal-4 layer is etched by HDP-RIE to open a window of the photodiode (Fig. 3-2(c)). After metal etching, the frontside silicon is etched isotropicly to release the structures. As shown in Fig. 3-2 (d), the exposed oxide is used to be the hard mask for

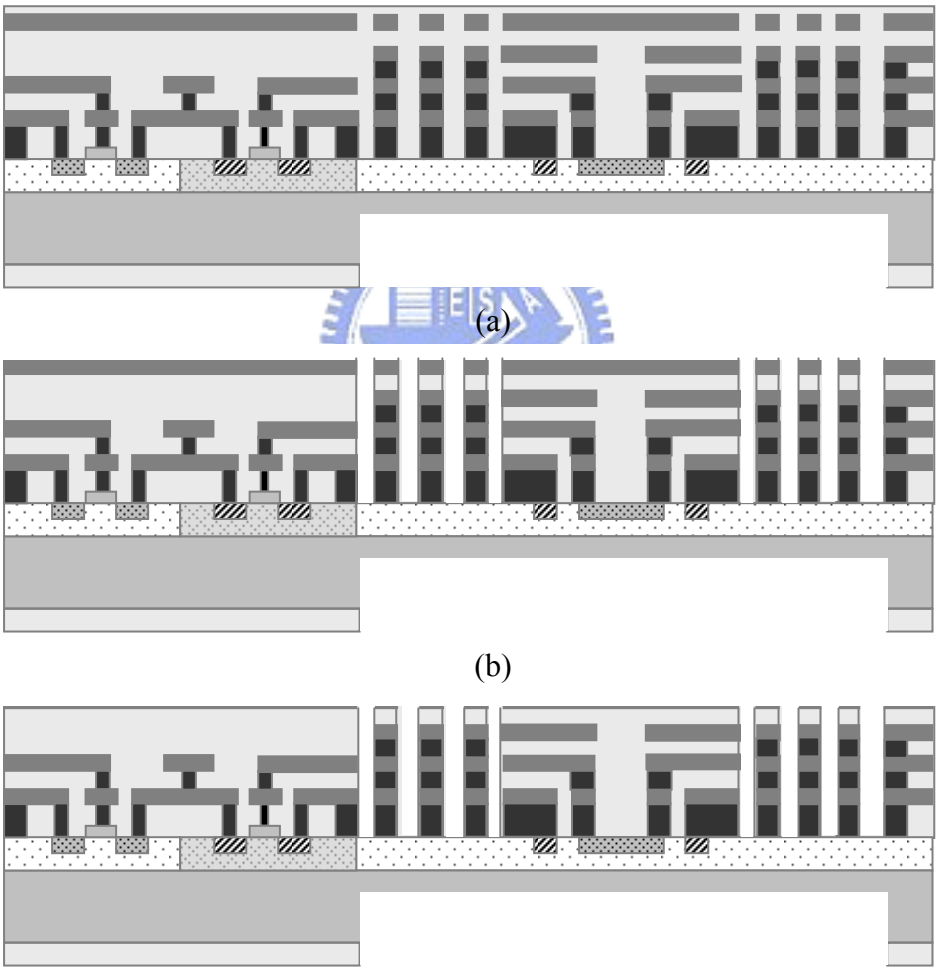
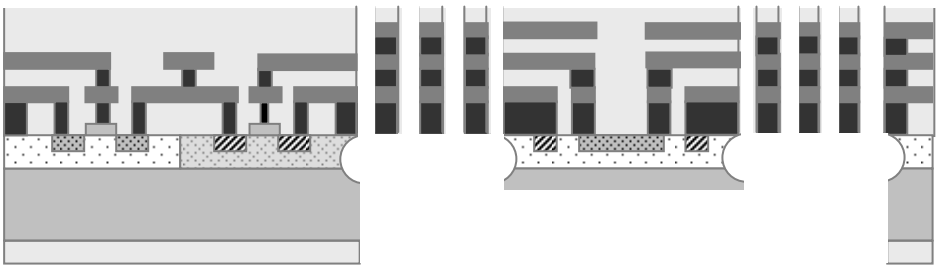
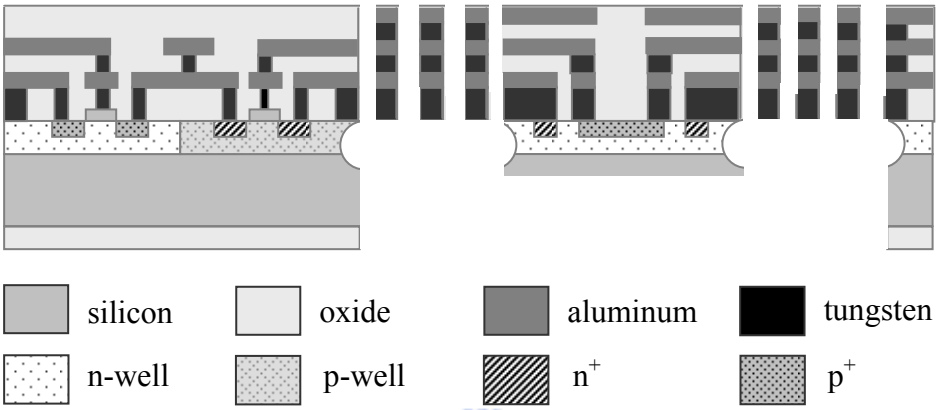


Fig. 3-2 Post CMOS process of D35-95D, (a) backside silicon etching, (b) frontside oxide etching, (c) frontside aluminum etching, (d) release structure, (e) top oxide layer etching



(d)



(e)

Fig. 3-2 Post CMOS process of D35-95D, (a) backside silicon etching, (b) frontside oxide etching, (c) frontside aluminum etching, (d) release structure, (e) top oxide layer etching (continued)

the following isotropic etching of silicon. By the high selectivity of SF_6 between oxide and silicon, the silicon substrate is undercut and suspended without sticksion. Additionally, the isolation of electrical signals is achieved when the silicon is removed. Finally, the top oxide layer is etched to expose the metal-3 layer for measuring (Fig. 3-2 (e)). The detail of the fabrication process is listed in Table 3-1.

Table 3-1 Detailed post CMOS process and recipe of D35-95D device

step	process	recipe	thickness/depth
1	grind backside Si	grind=3min, burnish=10min	300 μm
2	initial clean	H_2SO_4:H_2O_2=3:1	
3	PECVD SiO_2	N_2O=90sccm, SiH_4=5sccm,	3 μm

		RF power=10W, pressure=400mT	
4	backside photolithography	AZ4620 1st spin 1000rpm 2nd spin 3000rpm exposure time with filter=10min	8 μm
5	wet etching SiO_2	BOE 7min	3 μm
6	DRIE backside Si	passivate=7sec, etch=11.5sec C_4F_8=85sccm when passivating SF_6=130sccm, O_2=13sccm when etching coil power=600W when passivating and etching platen power=0W when passivating platen power=11.5W when etching	330 μm
7	RIE frontside SiO_2	CHF_3=40sccm, Ar=40sccm ICP power=750W, RF power=120W etching time=3500sec	7 μm
8	RIE frontside Al	BCl_3=35sccm, Cl_2=35sccm ICP power=750W, RF power=120W etching time=100sec	1 μm
9	DI water rising	10 min	
10	isotropic etching frontside Si	SF_6=50sccm ICP power=100W, RF power=120W etching time=60 min	10 μm
11	RIE frontside SiO_2	CHF_3=40sccm, Ar=40sccm ICP power=750W, RF power=120W etching time=3500sec	1 μm

3.1.2 Residue produced after aluminum etching

After aluminum etching, there is residue produced in the finger gaps (Fig. 3-3). The test chip after aluminum etching is used to analysis the composition of the residue by energy dispersive spectrometer (EDS). The result is observed by scanning electron microscope (SEM) and shown in Fig. 3-4 (a). The analysis result is shown in Fig. 3-4 (b). Except the elements contain in the CMOS structure, the chlorine is found in the

EDS analysis result. The residue is caused by reaction of remaining chlorine gas and the moisture in the air. The chemical formula [21] of this phenomenon is shown as:

$$AlCl_3+H_2O \rightarrow Al_2O_3+HCl$$

$$HCl+Al \rightarrow AlCl_3+H_2$$

The reaction produces the hydrogen chlorine and causes the corrosion of the aluminum.

This problem is solved by rinsing the chip by deionized water. After rinsing the chip by deionized water, the chip is observed by SEM (Fig. 3-6 (a)) and analyzed by EDS (Fig. 3-6 (b)). The chlorine disappears in the EDS analysis result. Thus, the problem is solved.

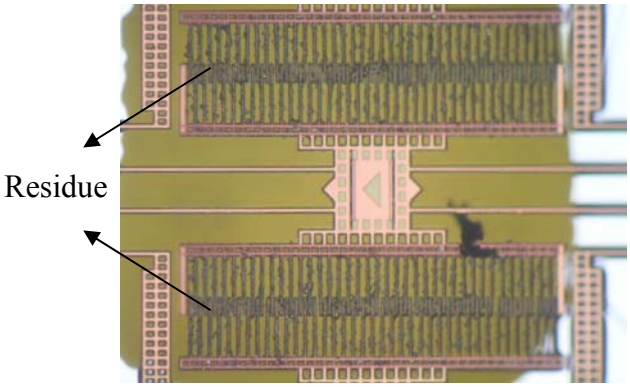
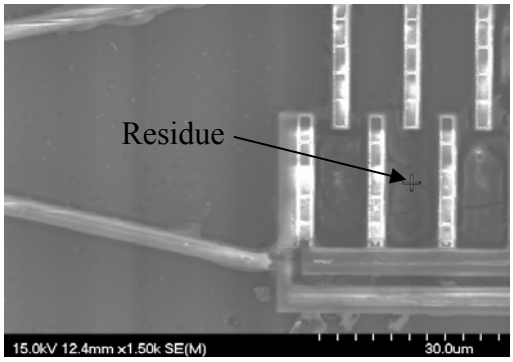
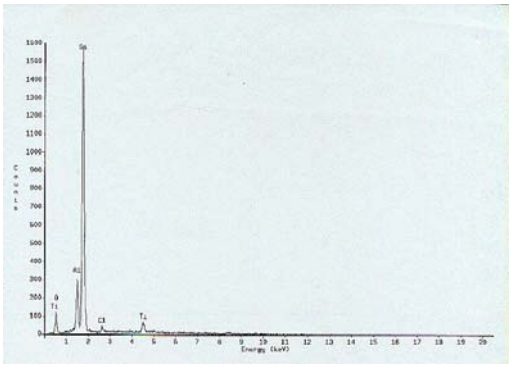


Fig. 3-3 After aluminum etching, residue is produced in the fingers gaps



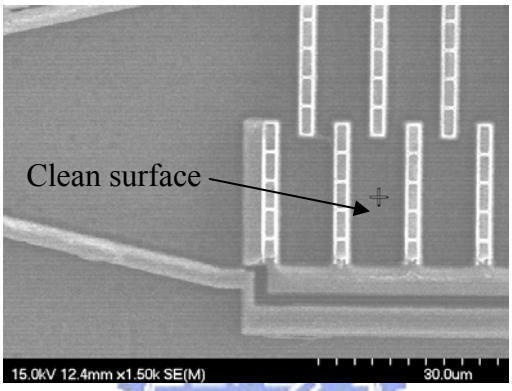
(a)

Fig. 3-4 The results analyzed after aluminum etching (a) SEM (b) EDS

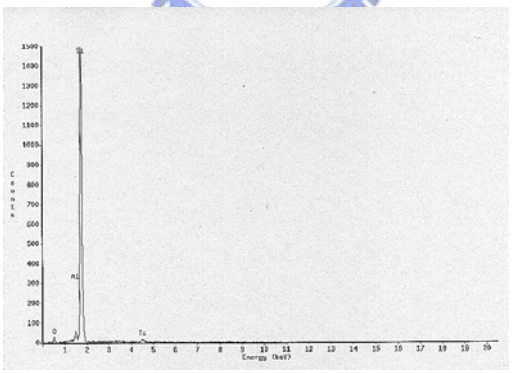


(b)

Fig. 3-4 The results analyzed after aluminum etching (a) SEM (b) EDS (continued)



(a)



(b)

Fig. 3-5 The results analyzed after DI water rising (a) SEM (b) EDS

3.2 Post CMOS in D35-97C device

The original chip of D35-97C device is shown in Fig. 3-6. To solve the problem mentioned in 3.1.2, the metal wet etching is used to define the structure. Use the post

process supported by TSMC, the passivation of metal etching area is pre-etched to open the etching window for this wet etching process.

The fabrication process begins from backside DRIE (Fig. 3-7(a)) for the purpose mentioned in 3.1.1. The oxide is deposited and patterned to be a hard mask of this etching process. After backside DRIE, frontside metal wet etching is used to define the structure. The dielectric layer can protect the structure in this metal etching (Fig. 3-7(b)). The structure is released by isotropic etching (Fig. 3-7(c)). Finally, the top passivation layer is removed by HDP-RIE to expose the M4 layer for electrical connection (Fig. 3-7(d)). The detail recipes are listed in Table 3-2.

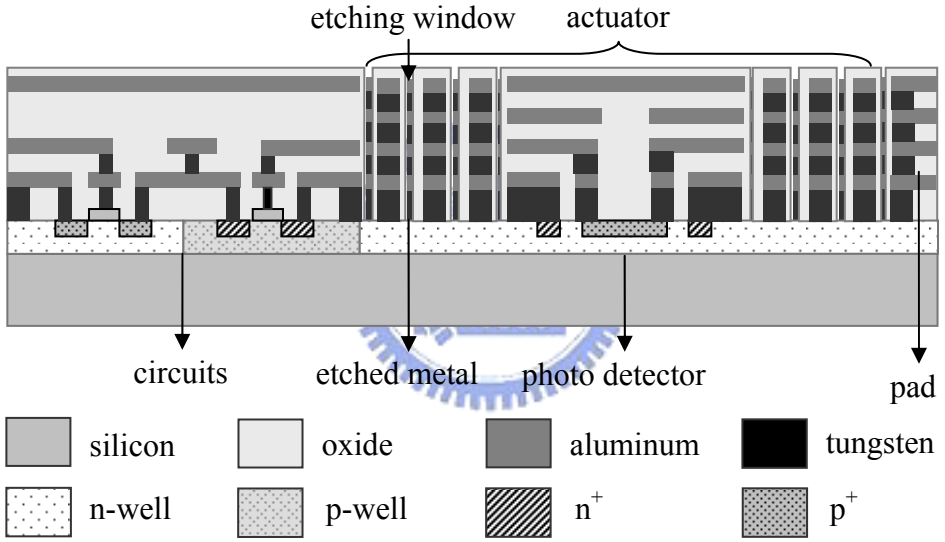
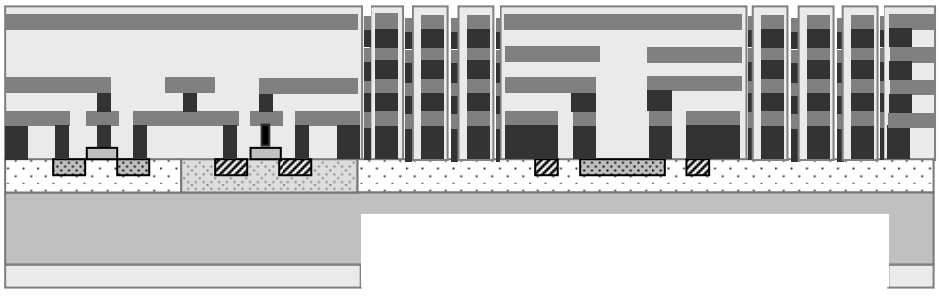


Fig. 3-6 Cross section view of CMOS device of D35-97C device



(a)

Fig. 3-7 Post CMOS process of D35-97C, (a) backside silicon etching, (b) frontside metal wet etching, (c) release structure, (d) top oxide layer etching

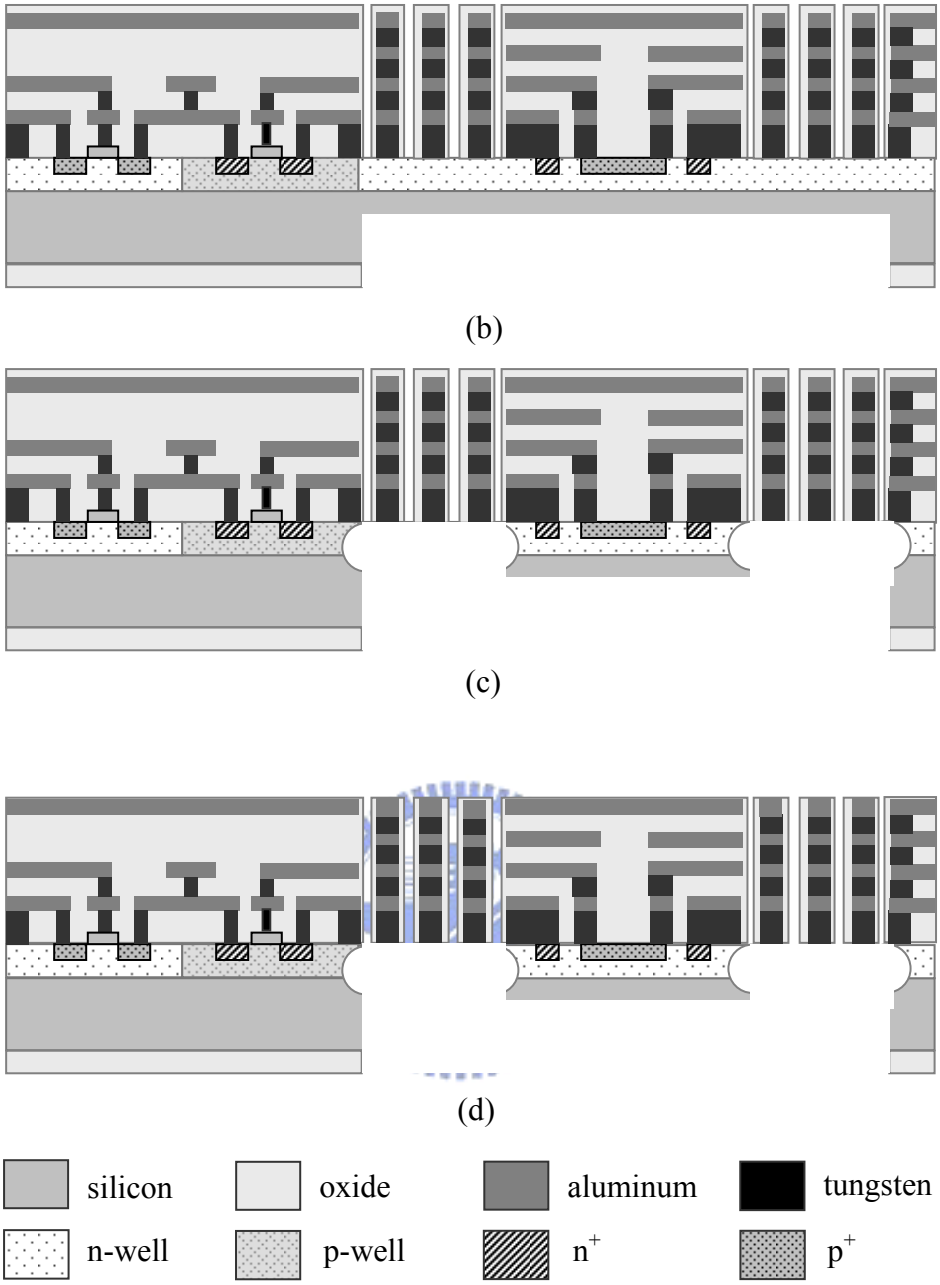


Fig. 3-7 Post CMOS process of D35-97C, (a) backside silicon etching, (b) frontside metal wet etching, (c) release structure, (d) top oxide layer etching (continued)

Table 3-2 Detailed post CMOS process and recipe of D35-97C device

step	process	recipe	thickness/depth
1	grind backside Si	grind=3min, burnish=10min	300 μm
2	initial clean	ultrasonic with ACE	
3	PECVD SiO_2	N_2O=90sccm, SiH_4=5sccm, RF power=10W, pressure=400mT	3 μm

4	backside photolithography	AZ4620, 1st spin 1000rpm 2nd spin 3000rpm exposure time with filter=10min	8 μm
5	wet etching SiO_2	BOE 7min	3 μm
6	DRIE backside Si	passivate=7sec, etch=11.5sec C_4F_8=85sccm when passivating SF_6=130sccm, O_2=13sccm when etching coil power=600W when passivating and etching platen power=0W when passivating platen power=11.5W when etching	330 μm
7	Metal wet etching	H_2SO_4:H_2O_2=3:1, 2hr etching	7 μm
9	isotropic etching frontside Si	SF_6=50sccm ICP power=100W, RF power=120W etching time=60 min	10 μm
10	RIE frontside SiO_2	CHF_3=40sccm, Ar=40sccm ICP power=750W, RF power=120W etching time=3500sec	1 μm

3.3 Fabricated device

After completing the post CMOS process listed in Table 3-1, D35-95D device is fabricated. The top view of the device is shown in Fig. 3-8 (a) and the photo detector in the central mass is shown in Fig. 3-8 (b). Light can be focused on the triangular region and absorbed by the photo detector to measure the spot profile. The spring and comb fingers are shown in Fig. 3-8 (c) and Fig. 3-8 (d).

From WYKO interferometer measurement, the curling of spring (Fig. 3-9) can be seen. The upward deflections of the free end in the longer spring and shorter spring are 8.6 μm and 4.7 μm. The level of deflections is not too large to let the device failure working. The radius of curvature ρ of longer spring and shorter spring can be calculated by equation (1):

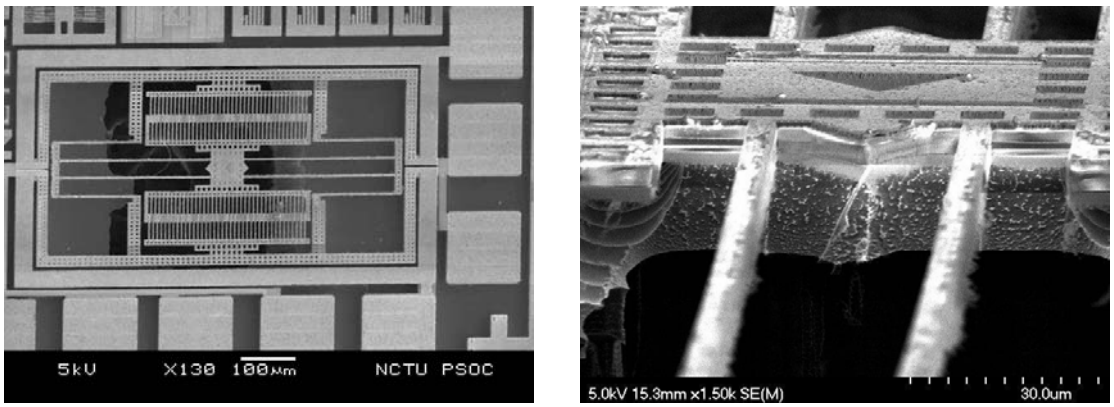
$$\rho = \frac{L^2}{2\delta}, \tag{1}$$

where L is the length of spring and δ is the deflections of the free end in spring. The radius of curvature can be calculated to be 4.56 mm in longer spring and 2.39 mm in shorter spring. After obtaining radius of curvature, the residue stress σ can be calculated by equation (2):

$$\sigma = \frac{Et}{2\rho}, \tag{2}$$

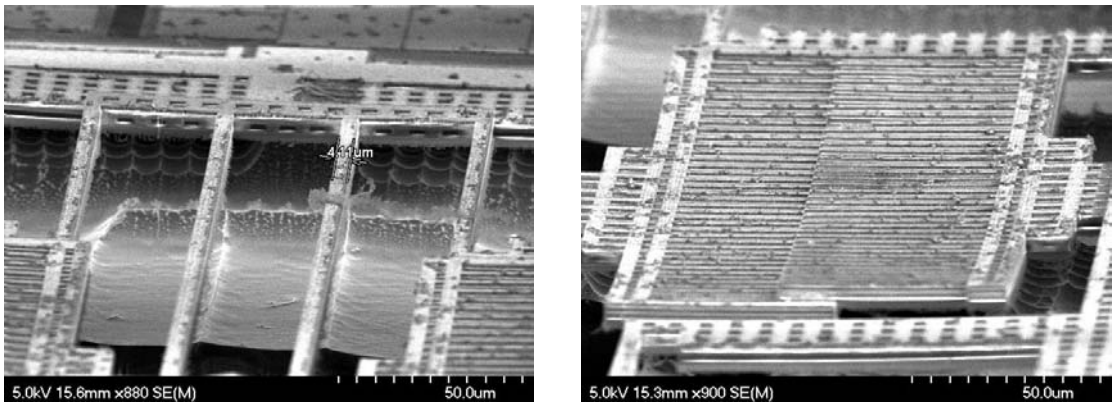
where E is the equivalent Young's modulus of spring, t is thickness of spring, and ρ is radius of curvature of spring. From above calculation, the residue stress can be calculated to be 38.38 MPa in longer spring and 73.22 MPa in shorter spring. The device is used to measure the spot size and the measurement results will be discussed in chapter 4.

D35-96A device is also processed. The top view of fabricated device is shown in Fig. 3-10 (a). From this figure, unclean surface can be seen in the device. The comb fingers are also observed (Fig. 3-10(b)). Residue can be seen in comb fingers. Therefore, this device can not be released successfully.



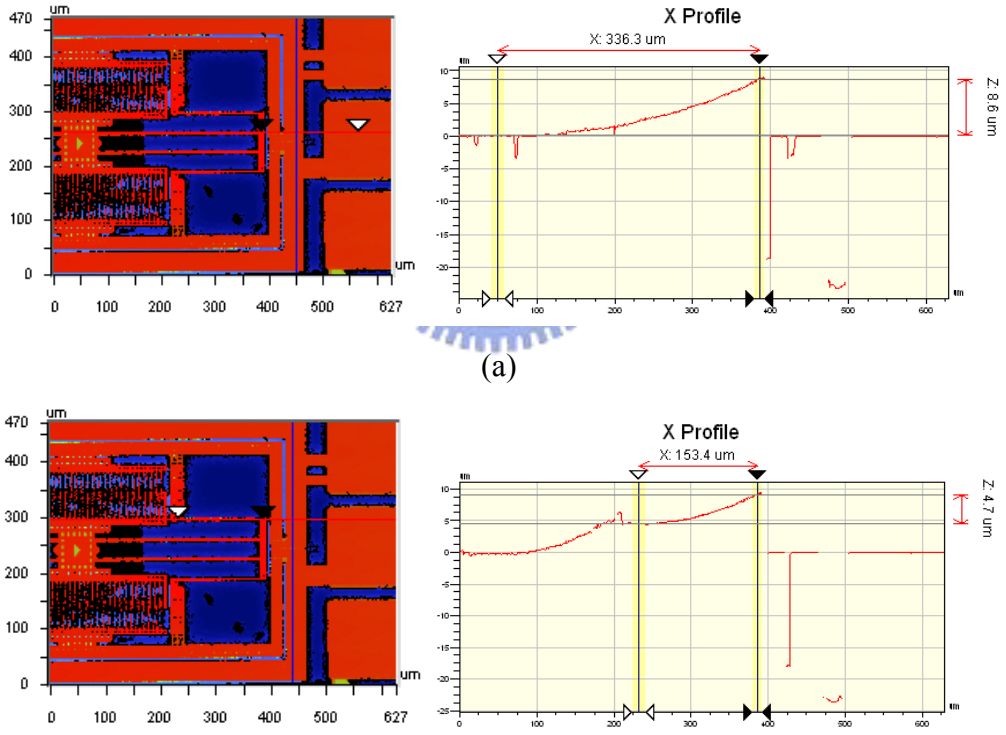
(a) (b)

Fig. 3-8 SEM picture of fabricated D35-95D device (a) top view, (b) photodiode in central mass, (c) spring, and (d) comb fingers



(c) (d)

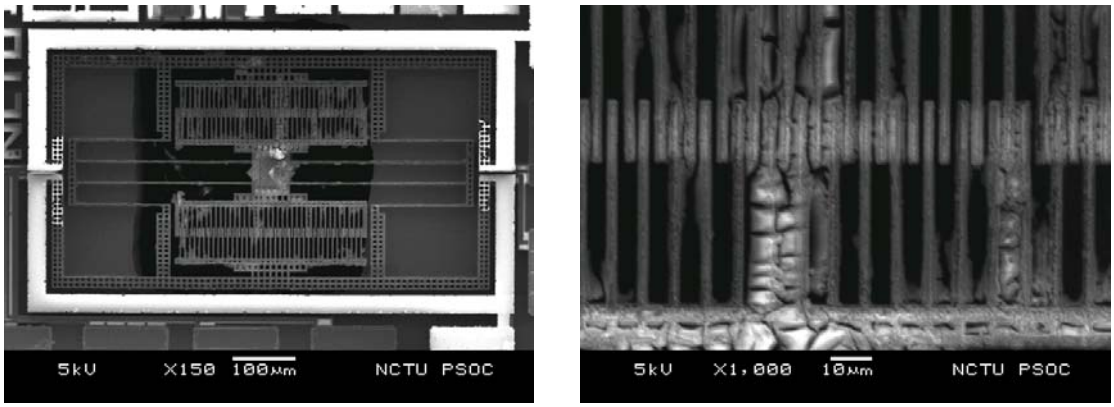
Fig. 3-8 SEM picture of fabricated D35-95D device (a) top view, (b) photodiode in central mass, (c) spring, and (d) comb fingers (continue)



(a)

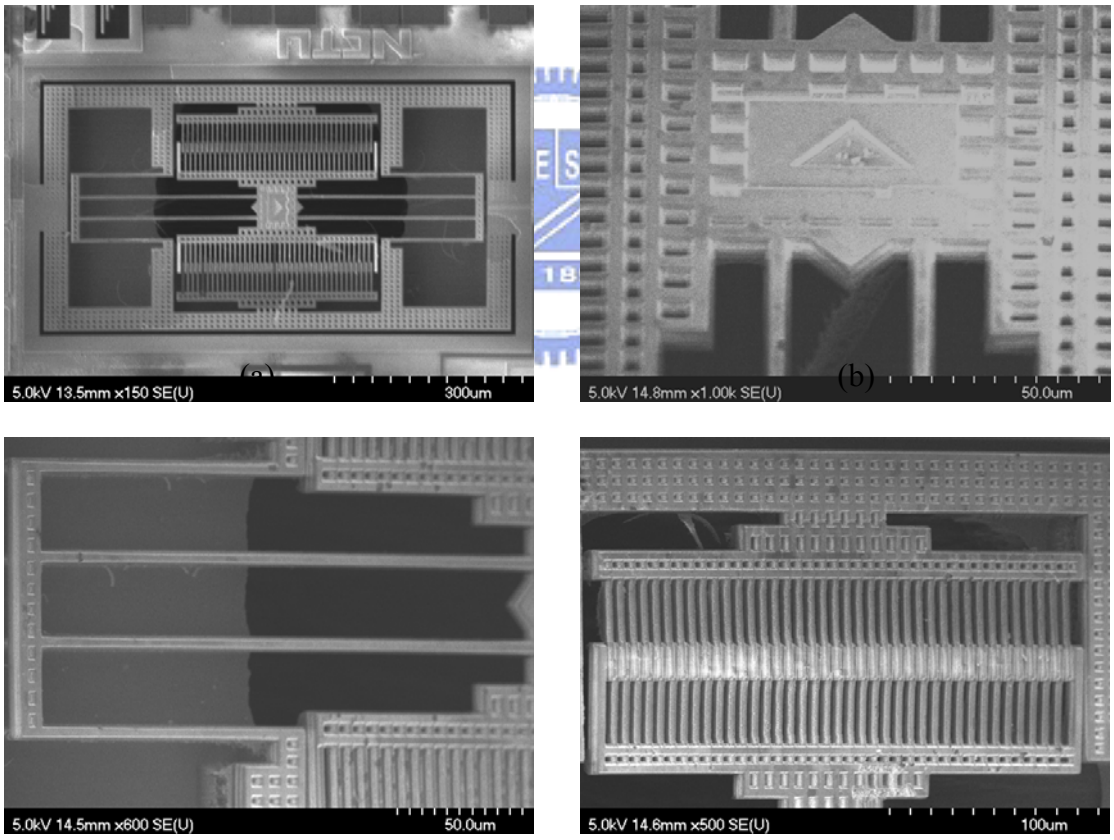
(b)

Fig. 3-9 Deflection of spring structure in D35-95D device (a) longer spring (b) shorter spring



(a) (b)

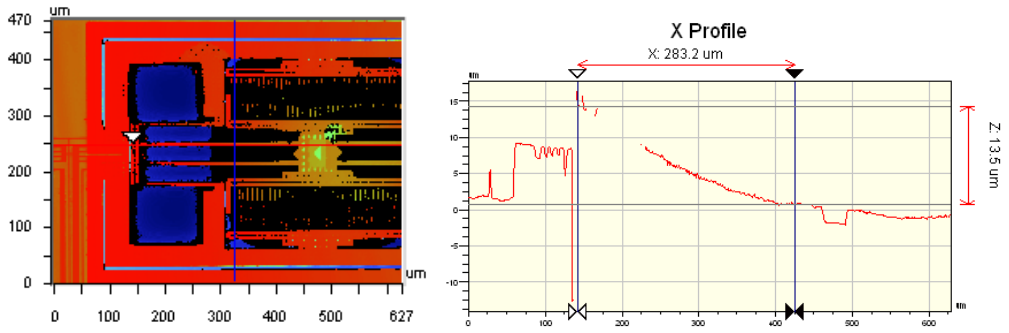
Fig. 3-10 SEM picture of fabricated D35-96A device (a) top view, (b) residue in comb fingers



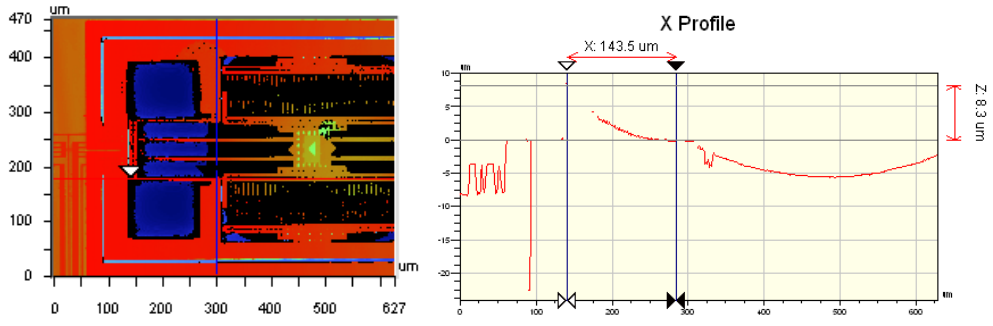
(c) (d)

Fig. 3-11 SEM picture of fabricated D35-97C device (a) top view, (b) photodiode in central mass, (c) spring, and (d) comb fingers

After completing the post CMOS process listed in Table 3-2, D35-97C device is also fabricated. The device is shown in Fig. 3-11 (a) and the photo detector is shown in Fig. 3-11 (b). Fig 3-11 (c) and Fig 3-11 (d) are spring and comb fingers. From WYKO interferometer measurement, the curling of spring (Fig. 3-12) can be seen. The upward deflections of the free end in the longer spring and shorter spring are 13.5 μm and 8.3 μm. Under the level of deflection, the actuator can still be actuated without sticking in the substrate. The radius of curvature can be calculated to be 2.90 mm in longer spring and 2.39 mm in shorter spring. After calculation of radius of curvature, the residue stress can be calculated to be 84.48 MPa and 102.51 MPa.



(a)



(b)

Fig. 3-12 Deflection of spring structure in D35-97C device (a) longer spring (b) shorter spring

3.4 Summary

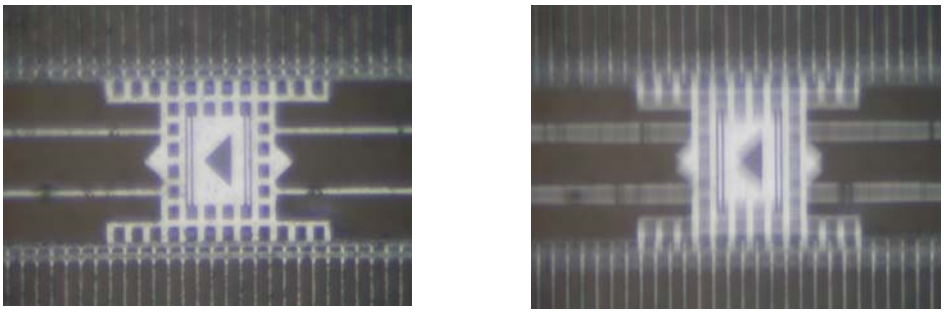
In this chapter, the process of CMOS absorption type device is presented. The encountered problems are solved and the device is successfully fabricated. The curling can be seen in the structure. However, the device is still suspended.

Chapter 4 Experiment and Measurement Results

In this chapter, characteristics of the microstructures and photodiodes in D35-95D and D35-97C are measured. The transimpedance circuits in D35-96A and D35-97C are also measured. The absorption type measurement data is also presented in this chapter.

4.1 Mechanical characteristics

The mechanical characteristic of D35-95D device is measured by the MEMS motion analyzer. For the D35-95D device, the comb drive actuator is actuated by applying a DC (V_{DC}) and an AC (V_{AC}) voltage in serious across the fixed and the movable electrodes. The resonant frequency can be found to be 10.0 kHz under V_{DC} of 30 V and V_{AC} amplitude of 30V. The vibration of the microstructure is shown in Fig. 4-1. The frequency response of amplitude and phase are plotted in Fig. 4-2. The applied voltage across the fixed and the movable fingers are V_{DC}=30 V and V_{AC}= *30* V (Fig. 4-2(a), (b)), V_{DC}=40 V and V_{AC}=40 V (Fig. 4-2(c), (d)), and V_{DC}=50 V and V_{AC}=50 V (Fig. 4-2(e), (f)).



(a) (b)

Fig. 4-1 Optical microscope image for D35-95D device (a) fabricated device (b) operation at resonant

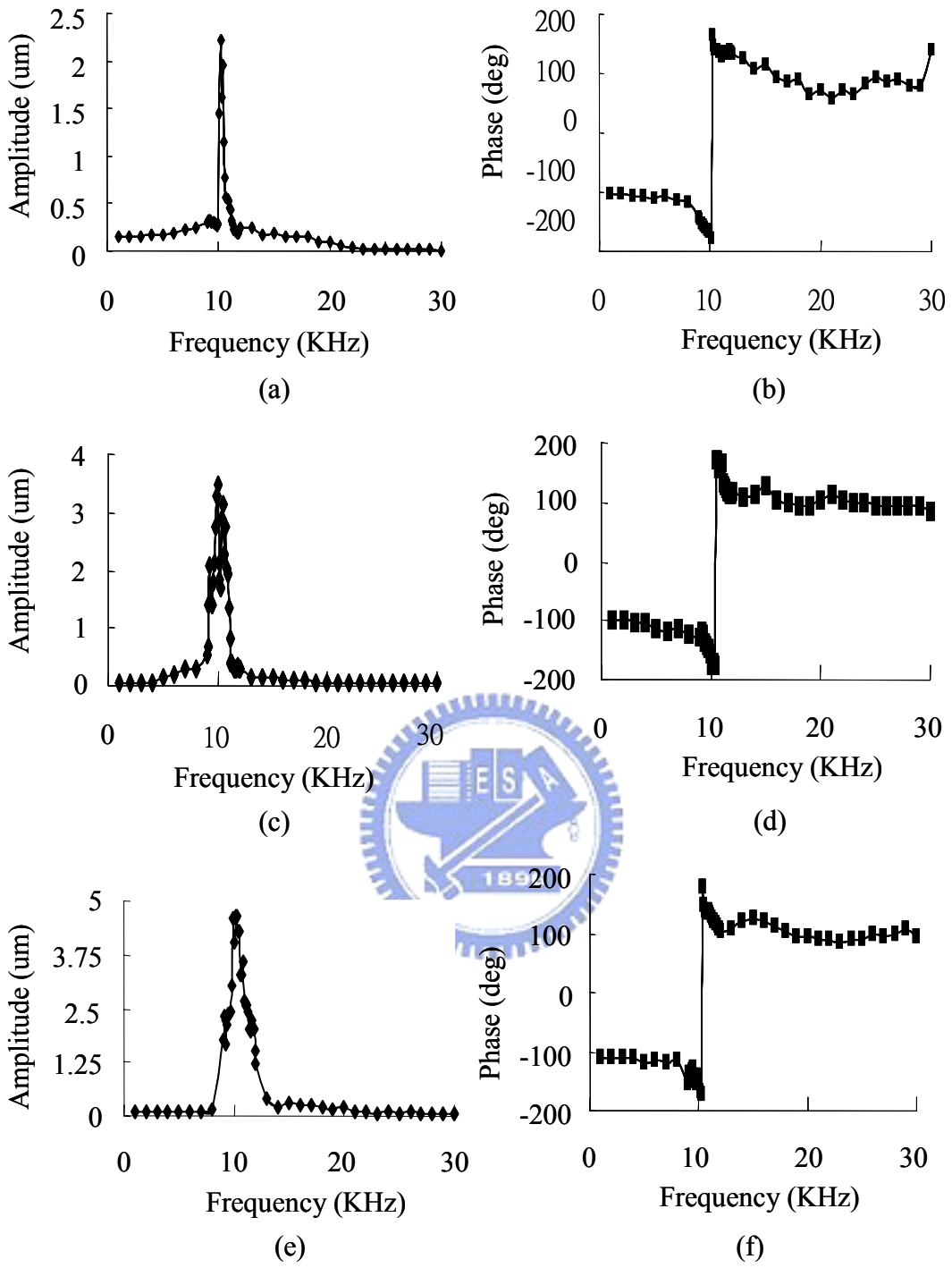


Fig. 4-2 Frequency response of the D35-95D device under V_{DC} = 30 V and V_{AC} = 30 V (a) amplitude (b) phase, under V_{DC} = 40 V and V_{AC} = 40 V (c) amplitude (d) phase, and under V_{DC} = 50 V and V_{AC} = 50 V (e) amplitude (f) phase

The maximum amplitude in each applied voltage is 2.22 μm, 3.48 μm, and 4.65 μm at resonant frequency. A phase shift of 180° was also observed across the

resonance frequency. The measured resonant frequency is less then simulation result due to thicker silicon substrate left in the movable structure. From WYKO interferometer measurement, the measured backside thickness is 30 μm (Fig. 4-3). The total thickness of frontside layers is 6.97 μm before frontside processing. Therefore, the thickness of backside silicon is 23.03 μm. The backside silicon is thicker than the expected thickness (20 μm). Additional mass in the movable part causes lower resonant frequency than the simulated value (12.1 kHz).

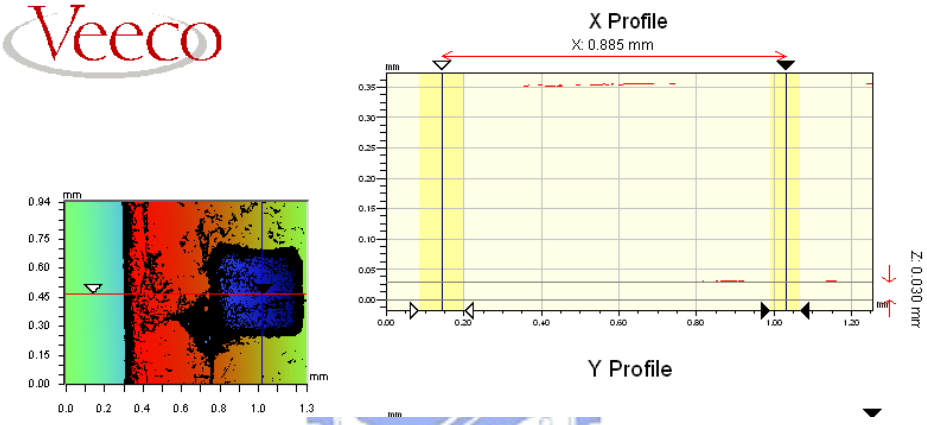
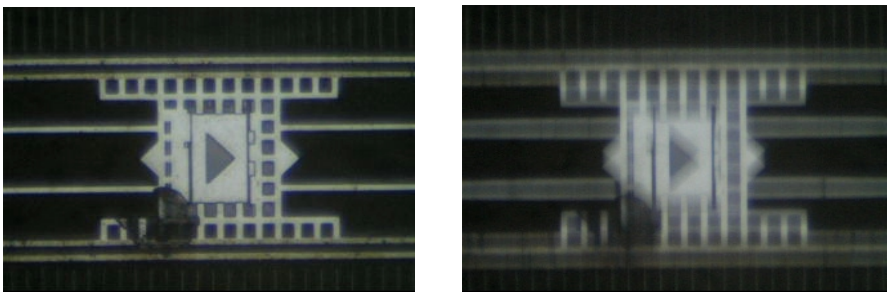


Fig. 4-3 Thickness of backside silicon measured by WYKO interferometer

For the D35-97C device, voltage is applied across rotor and stator with V_{DC}=30 V and V_{AC}= *30* V. The vibration of this device is shown in Fig. 4-4. The mechanical characteristic of this device is shown in Fig. 4-5. The measured resonant frequency is 24.0 KHz. The amplitude at resonant frequency is 4.55 μm.



(a) (b)

Fig. 4-4 Optical microscope image for D35-97C device (a) fabricated device (b) operation at resonant

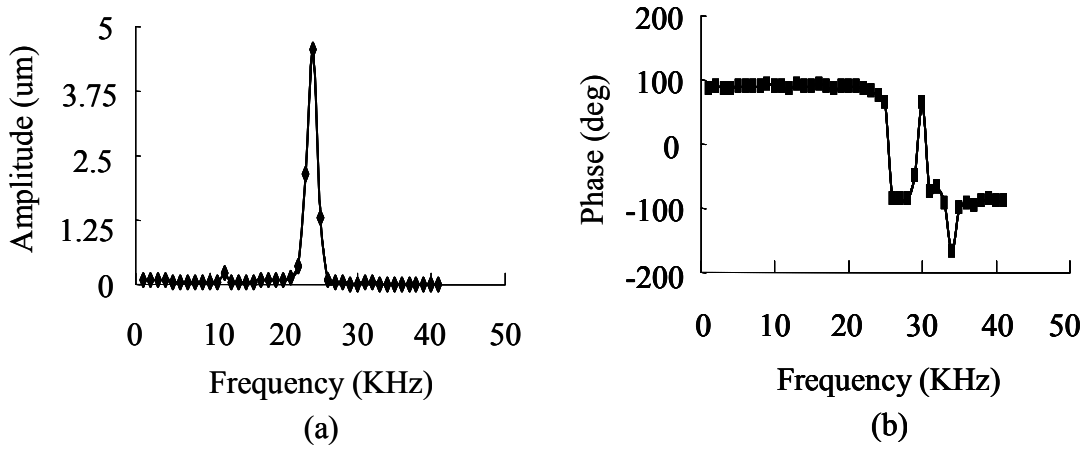
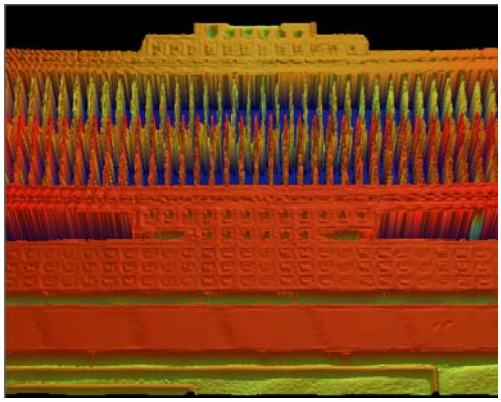


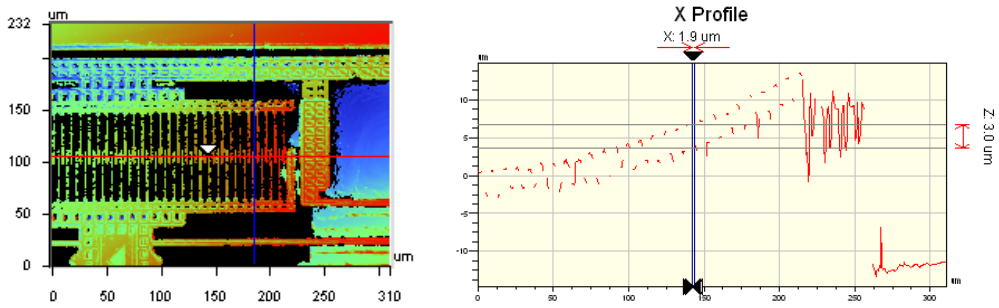
Fig. 4-5 Frequency response of the D35-97C device under V_{DC} = 30 V and V_{AC} = 30 V (a) amplitude (b) phase

In the above measurement, the measured amplitude is less than expected value due to the sidewall of the fixed and movable fingers are not completely overlap. The capacitance between the fixed and movable fingers is less than ideal case (complete overlapping). This phenomenon is measured by a WYKO interferometer (Fig. 4-6). The 3D measurement shows a height different between fixed and movable fingers. The height different between fixed and movable fingers are 3 μm in D35-95D device and 3.9 μm in D35-97C device.

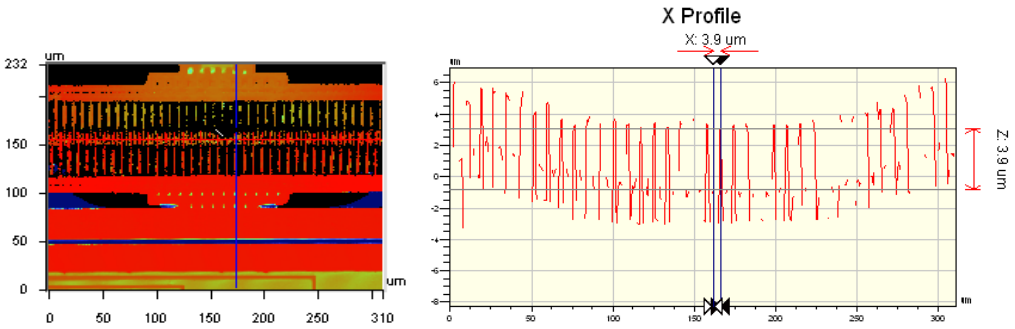


(a)

Fig. 4-6 Partial overlapping of comb fingers (a) 3D view (b) D35-95D device (c) D35-97C device



(b)



(c)

Fig. 4-6 Partial overlapping of comb fingers (a) 3D view (b) D35-95D device (c) D35-97C device (continued)

4.2 Photodiode and transimpedance circuit

The I-V curves of the photodiodes in the test structure and the fabricated device are measured by a Keithley 4200 semiconductor analyzer system. The light source is produced from optical microscope. The optical power in the 9.08 mm^2 illuminated area under the microscope is 3.34 mW with the power meter set for 575 nm wavelength.

The I-V curves of the test photodiode and the photodiode in fabricated device are shown in Fig. 4-7. The absorption area of photodiodes is 225 μm^2. After comparing the illuminated area and absorption area of photodiodes, the light power absorbed by photodiodes is 82.8 nW. The photocurrent at 5 volts reverse bias are 13.06 nA of the photodiode in the test structure and 5.20 nA of the photodiode in the fabricated

device .Therefore, the responsivity of each photodiode is 0.158 A/W and 0.063 A/W under 5 volts reverse bias. It can be seen that the responsivity of the faricated device is lower than the responsivity of test structure. The backside DRIE is performed only for fabricated device. The silicon is etched by F^+ ions and this chemical reaction is exothermic [22]. The high temperature causes the lower responsivity after DRIE.

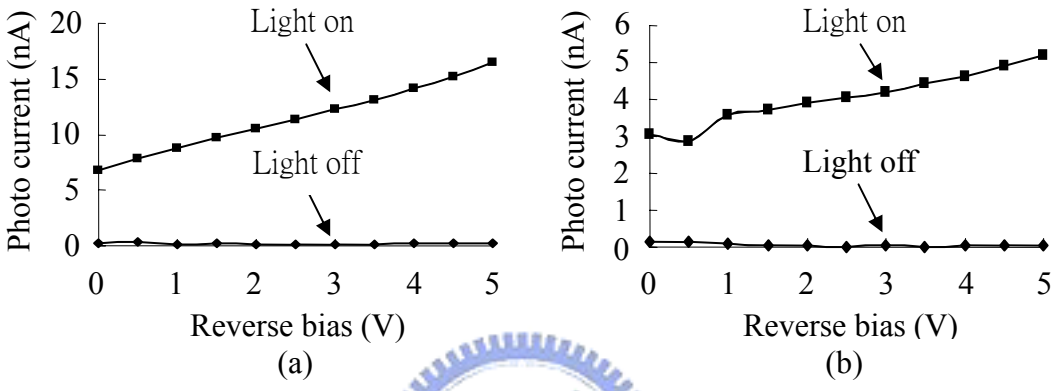


Fig. 4-7 Responsivity of photodiode (a) test photodiode and (b) fabricated device

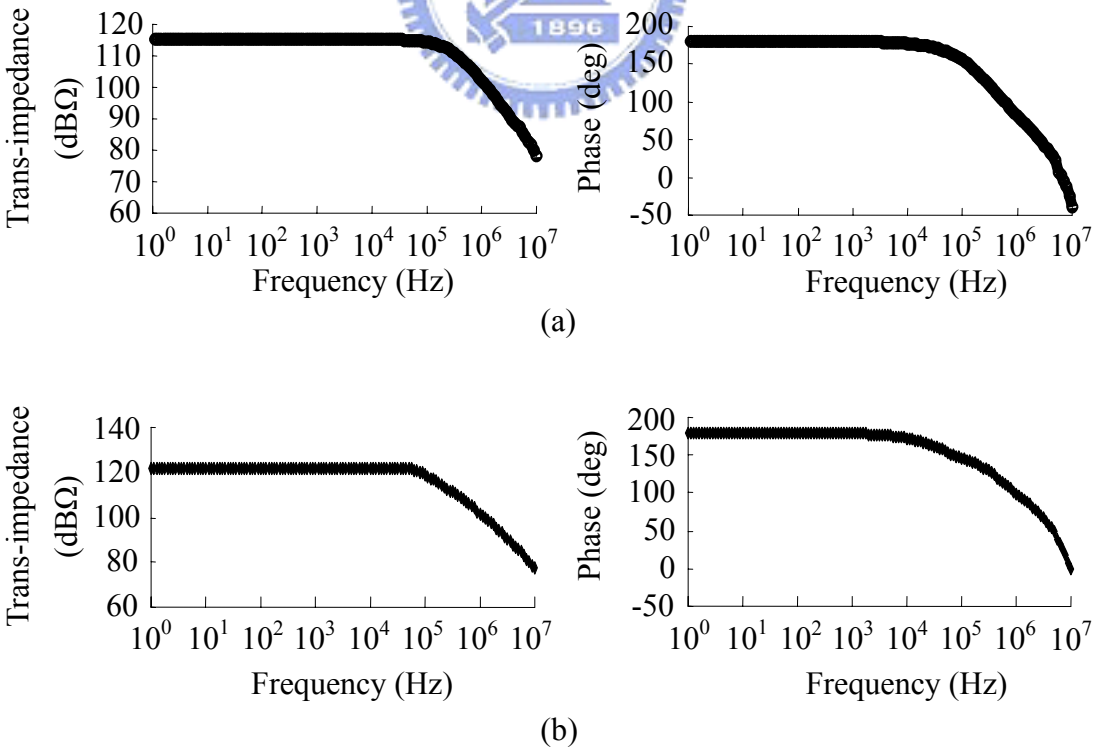


Fig. 4-8 Frequency response (a) type 1 and (b) type 2

The frequency response of the transimpedance circuits are also measured by frequency response analyzer (FRA-5087) [23]. The measurement results are shown in Fig. 4-8. The transimpedance of type1 in D35-96A design and type2 circuit in D35-97C design are 582 KΩ and 1.25 MΩ. The bandwidth of type1 and type2 circuit is 251 kHz and 126 kHz. Due to the process variation, the measurement results are different from the expected transimpedance. The measurement result of type 1 circuit is near the simulation result in TT corner. The measurement result of type 2 circuit is between the values of TT and SS corner.

4.3 Piezoresistive position sensor

The V_s = 10 V DC voltage is applied to the Wheatstone bridge shown in Fig. 2-11. The device is driven harmonically. Therefore, a sinusoidal output signal V_o is expected.

The driving signal and the output signal are shown in Fig. 4-9. The peak to peak amplitude of output signal is 100 mV which is smaller than expected value (298 mV) due to the smaller AC displacement (4.55 μm) than expected value (10 μm). The output signal is suffered from electrical interference. However, the phase difference between the driving signal and the output signal is 90°. The phase difference matches the theoretical when this actuator is driven in resonant frequency.

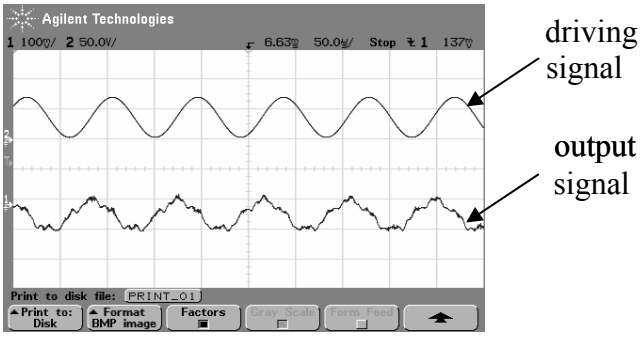


Fig. 4-9 Observed driving signal and output signal

4.4 Spot profile measurement

4.4.1 D35-95D device measurement with off-chip TIA

The D35-95D device is first measured with an off-chip tansimpedance circuit. The setup for experiment is shown in Fig. 4-10. The light sources are 10 mW red light (633 nm) and 0.8 mW green light (543 nm). The beam expander expanded the laser beam before entering the objective lens to enhance the focus ability of the objective lens. The 20X and 40X objectives are used to focus the incident light in this experiment. The off-chip operational amplifier with a feedback resistor is used to convert the photocurrent to a voltage signal. The feedback resistor is 500Ω for red light measurement and 5 KΩ for green light measurement. A V_{DC} = 40 V and V_{AC}= 40 V is applied across fingers in the fixed and movable fingers to actuate the photodiode in the actuator. Part of light is absorbed by the actuated photodiode during scanning across the measured spot. If the amplitude of the actuator is larger than twice the diameter of focused optical spot, the spot can be scanned in two orthogonal directions in half of the scan cycles. Therefore, four scans of the focused spot distribution can be recorded in one full scan cycle.

The original signals of each combination of light source and objective lens are shown in Fig. 4-11. To minimize electric noise, the measured signals were averaged by the oscilloscope (Agilent 54622A). The average number is 8 for this experiment. The signals after averaging are shown in Fig. 4-12. A 0.3 volts signal scale can be seen in the waveform for red light and green light experiments. The averaged signal is used to calculate the focused spot size. The folded knife edge signal plotted with respect to position is shown in Fig. 4-13. The average photocurrent of positive and negative scan is used to calculate the spot size. The power distribution can be obtained from the differentiation of current output. Fig. 4-14 shows the derived power

distribution derived from Fig. 4-13. The full width at half maximum (FWHM) spot size can be obtained from taking the width between the positions which the normalized power in the positions is 0.5.

The measurement results are summarized in Table 4-1. The theoretical diffraction limit [24] is expressed as:

$$s \cong \frac{0.5\lambda}{NA} \tag{1}$$

where λ is the wavelength of incident light source and NA is the numerical aperture of objectives. For the 20X and 40X objectives, the NA values are 0.4 and 0.65, respectively. Imperfect optical setup causes the measured spot sizes are all larger than theoretical diffraction limit. There are irregular peaks in the divided power distribution due to the electrical noise from photodiode. However, the function of this absorption type device is demonstrated.

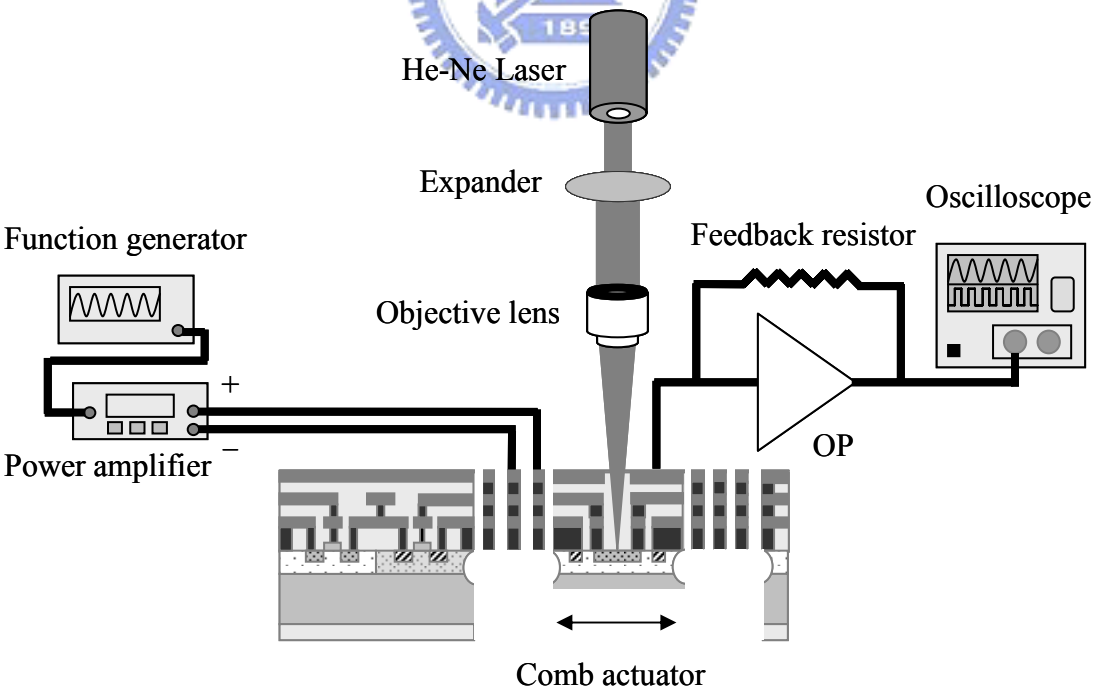
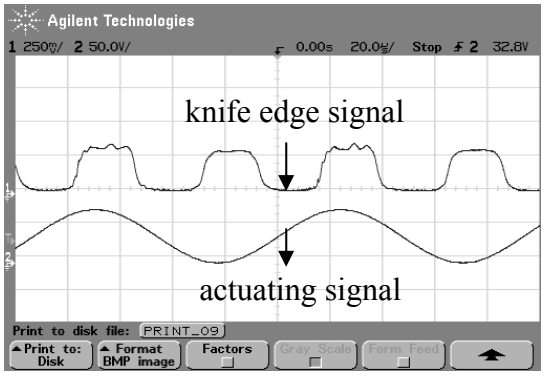
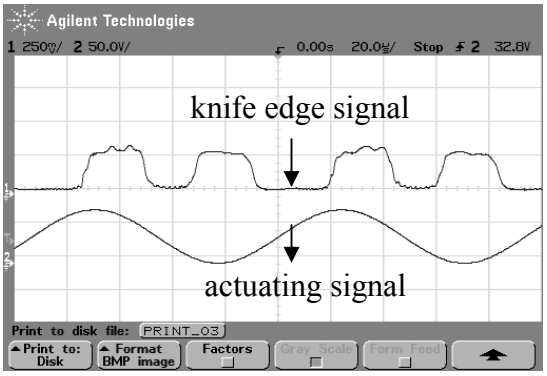


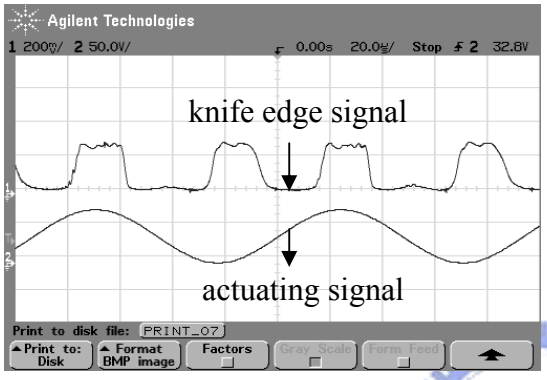
Fig. 4-10 Optical setup of spot profile experiment with off-chip TIA



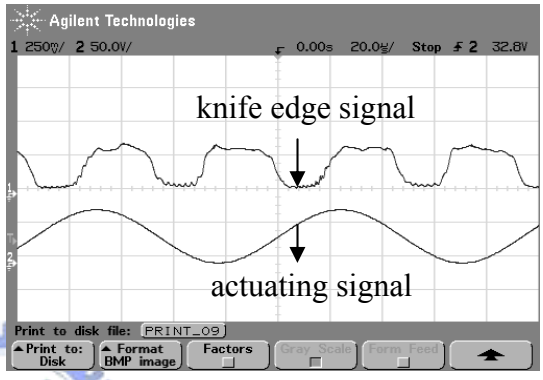
(a)



(b)

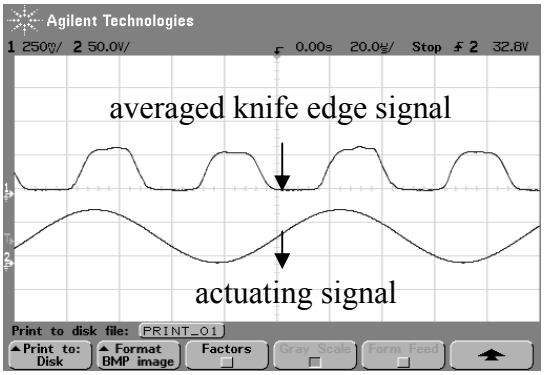


(c)

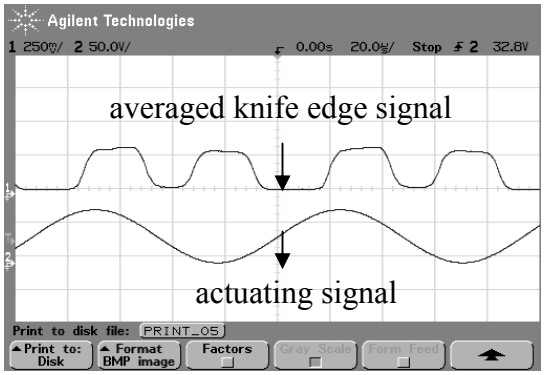


(d)

Fig. 4-11 Observed signal without averaging of red light with (a) 20X (b) 40X objective lens and green light with (a) 20X (d) 40X objective lens for D35-95D device

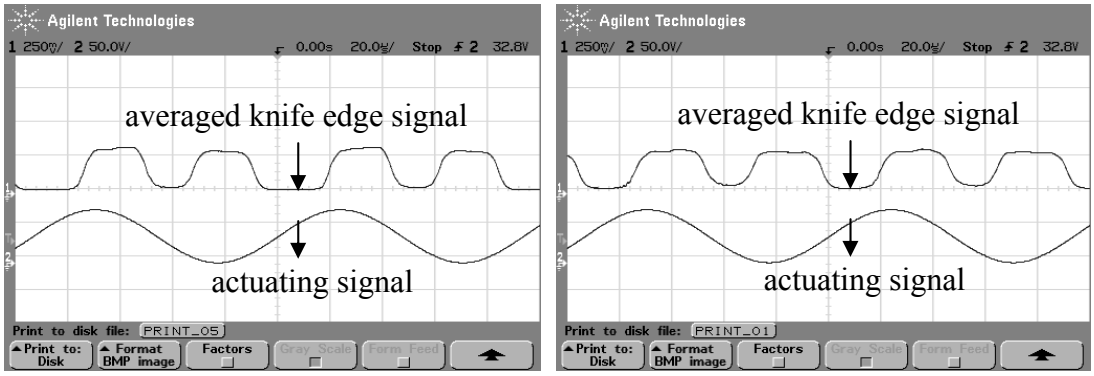


(a)



(b)

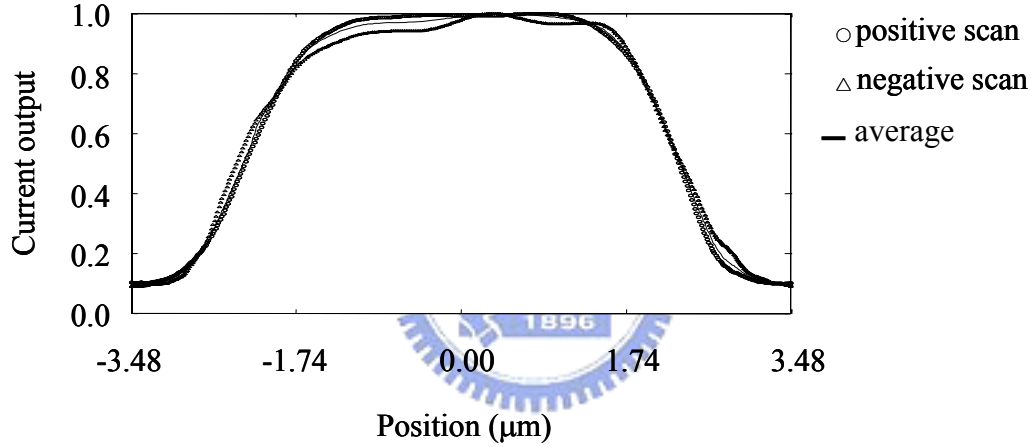
Fig. 4-12 Observed signal averaged by oscilloscope of red light with (a) 20X (b) 40X objective lens and green light with (a) 20X (d) 40X objective lens for D35-95D device



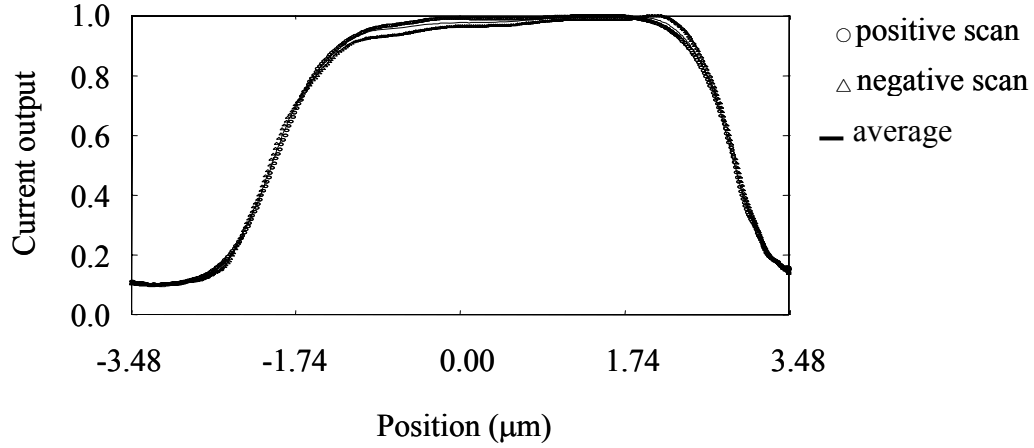
(c) (d)

Fig. 4-12 Observed signal averaged by oscilloscope of red light with (a) 20X (b) 40X objective lens and green light with (a) 20X (d) 40X objective lens for D35-95D device

(continued)

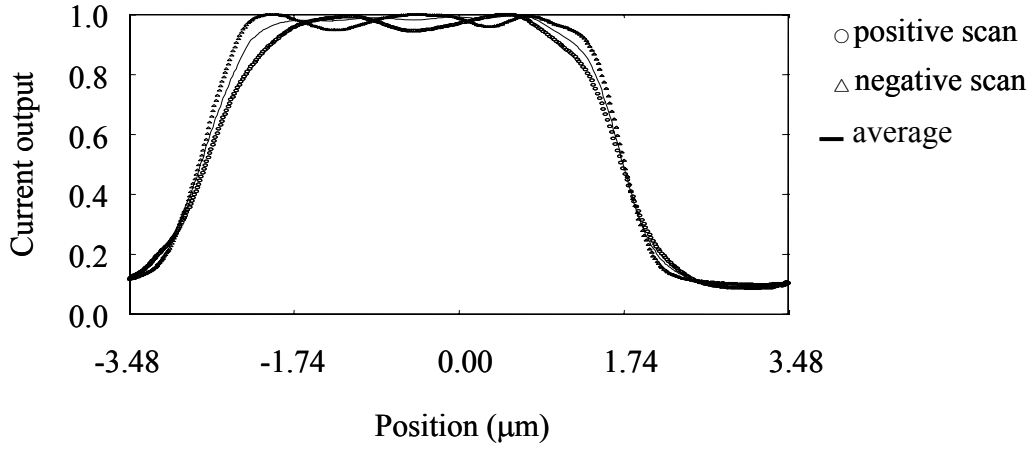


(a)

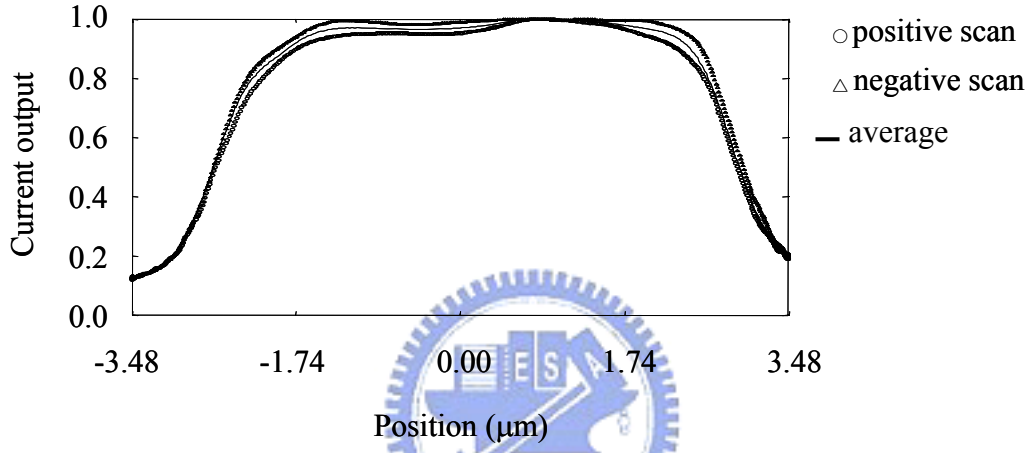


(b)

Fig. 4-13 Folded knife edge signal plot to position of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device

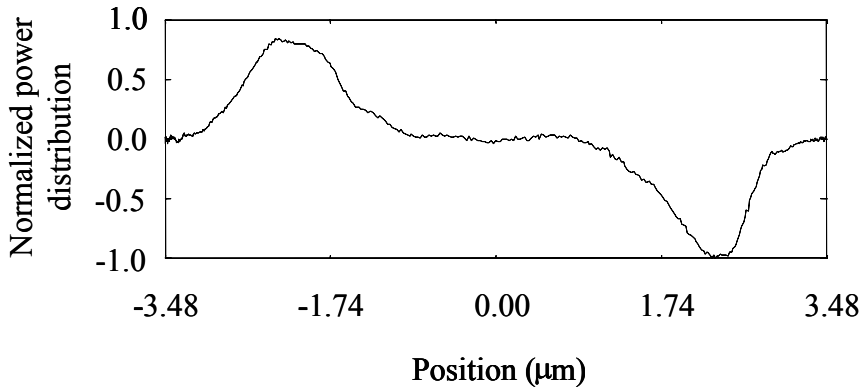


(c)



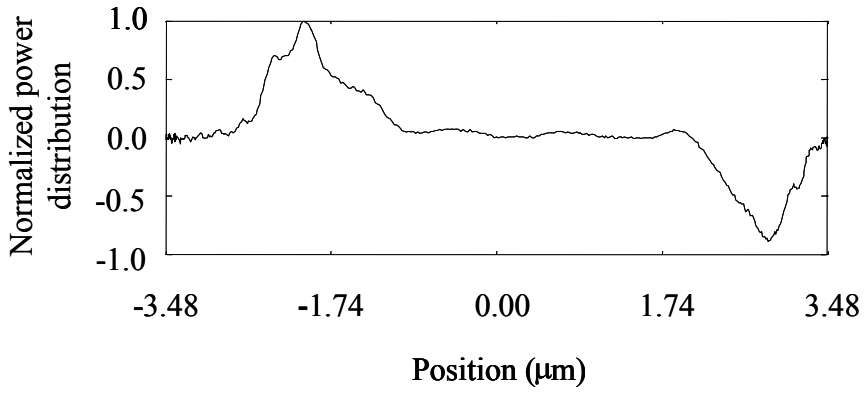
(d)

Fig. 4-13 Folded knife edge signal plot to position of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device (continued)

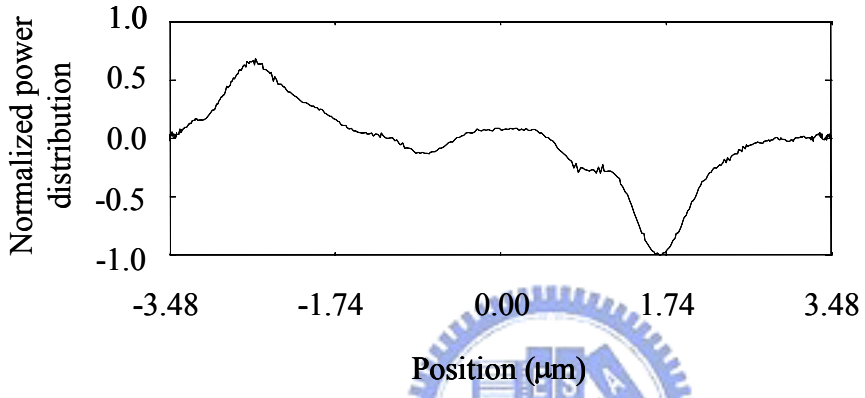


(a)

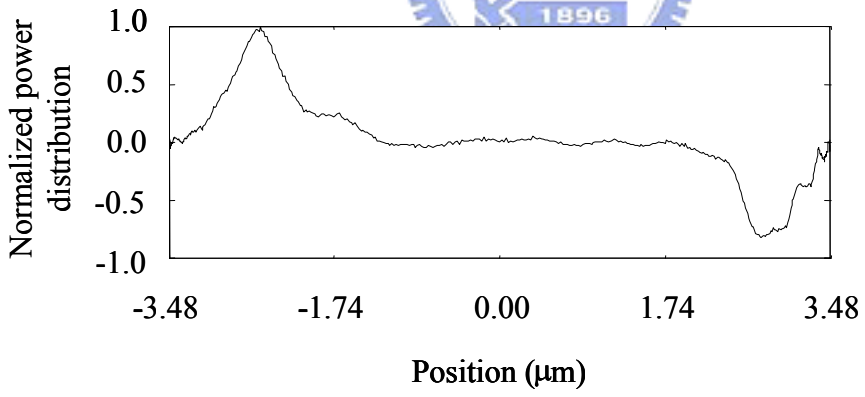
Fig. 4-14 Derived power distribution of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device



(b)



(c)



(d)

Fig. 4-14 Derived power distribution of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device (continued)

Table 4-1 Measured and theoretical focused spot size of measurement in Fig. 4-10

	wavelength	laser power	objectives	NA	$S_{theoretical}$	$S_{measured}$
1	633 nm	10mW	20X	0.4	0.79 μm	0.93 μm
2	633 nm	10mW	40X	0.65	0.53 μm	0.62 μm
3	543 nm	0.8mW	20X	0.4	0.68 μm	0.80 μm
4	543 nm	0.8mW	40X	0.65	0.44 μm	0.58 μm

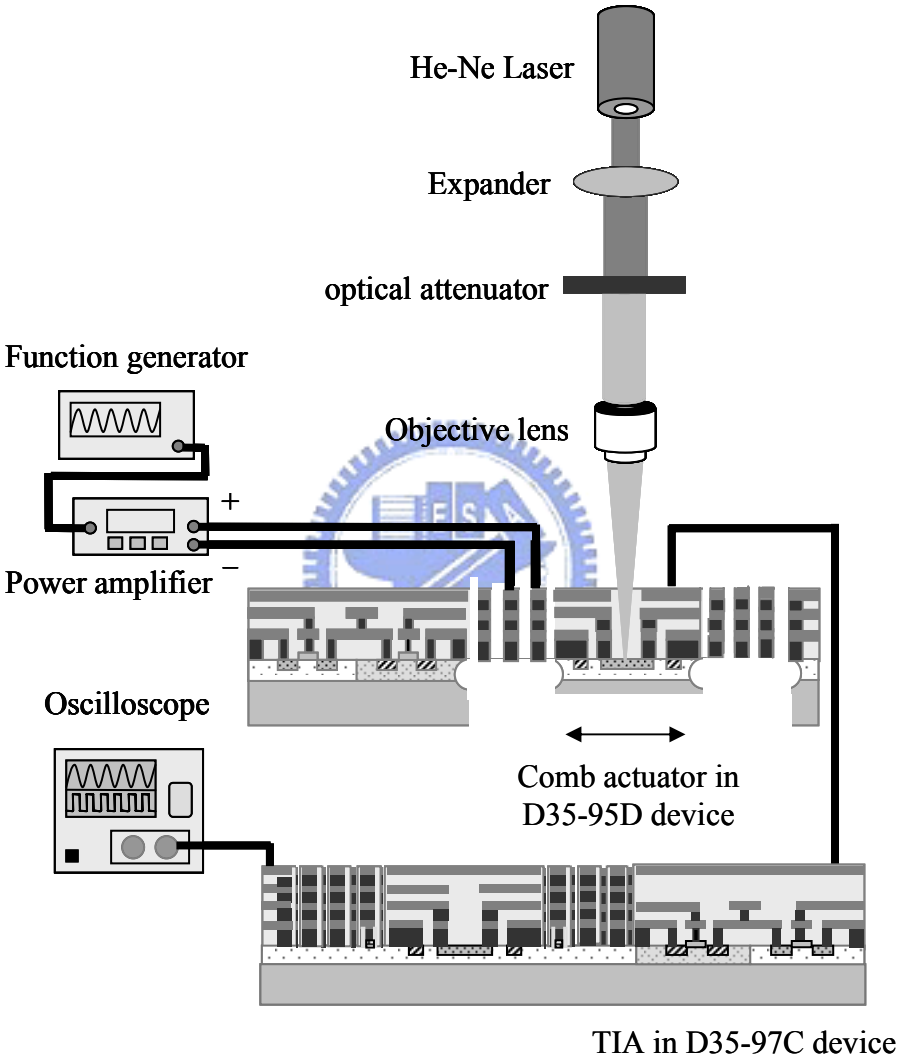


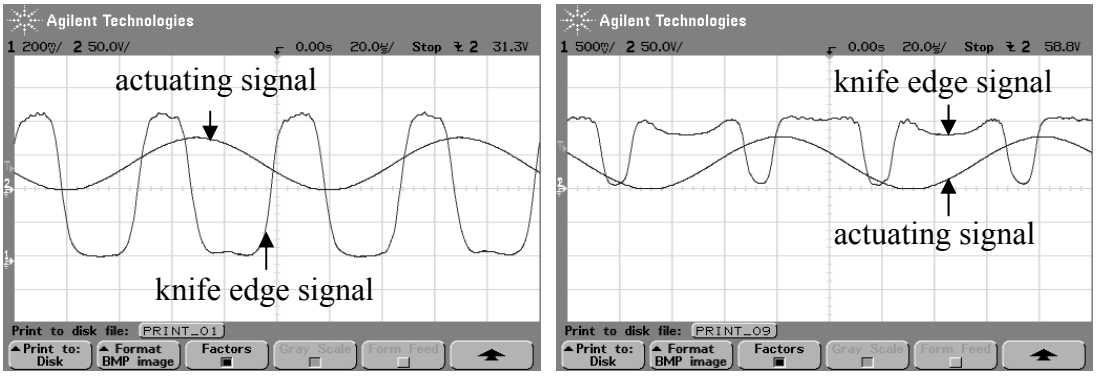
Fig. 4-15 Optical setup of spot profile experiment of D35-95D device with on-chip TIA in D35-97C device

4.4.2 D35-95D device measurement with on-chip TIA in D35-97C

The D35-95D device was also used to measure the focused spot size with on chip

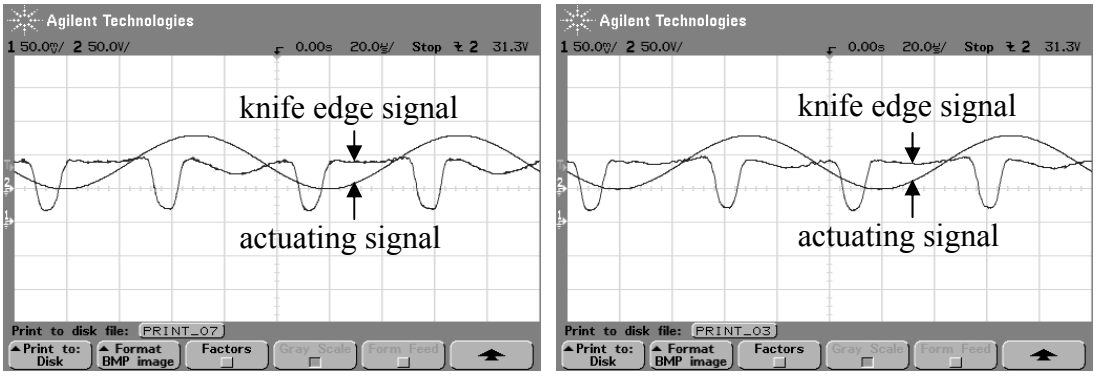
TIA (type2) in D35-97C device. The setup of this experiment is shown in Fig. 4-15. The optical attenuator is used to prevent saturation of the output signal. The power of red laser and green laser are 9.5 μW and 1.5 μW. The pad of D35-97C device is exposed by oxide dry etching. A V_{DC} = 40 V and V_{AC}= 40 V is applied across fingers in the rotor and the stator to actuate the photodiode in the actuator. The signals in D35-95D device and D35-97C device are connected on bread board.

The captured signals without averaged by oscilloscope are shown in Fig. 4-16. A 0.85 volts signal scale for red light measurement and a 0.1 volts signal scale for green light can be seen. The folded knife edge signals are plotted with respect to position of the photodiode (Fig. 4-17). The average photocurrent of positive and negative scan is used to calculate the spot size. The derived power distributions by taking differentiation of the knife edge signal are shown in Fig. 4-18. The measurement results are summarized in Table 4-2. The full width at half maximum (FWHM) spot size can be obtained from taking the width between the positions which the normalized power in the positions is 0.5. The measured spot sizes are larger than theoretical results due to imperfect optical setup.



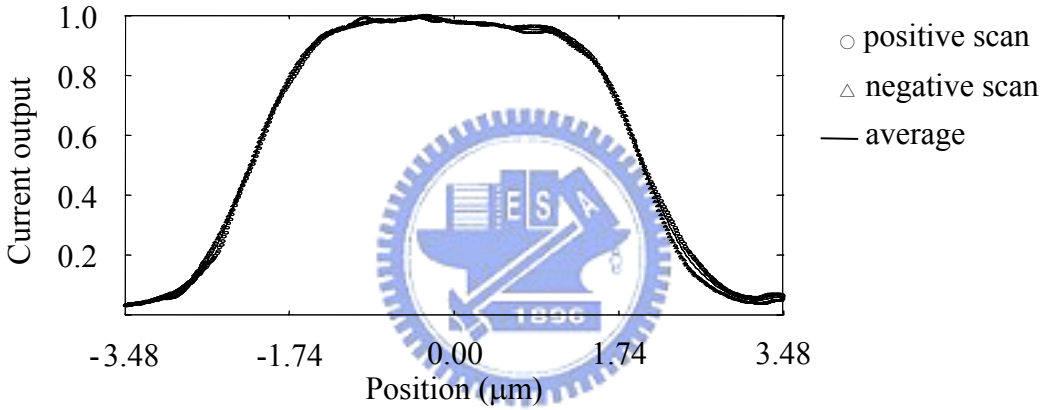
(a) (b)

Fig. 4-16 Observed signal by oscilloscope of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device with on-chip TIA in D35-97C deevice

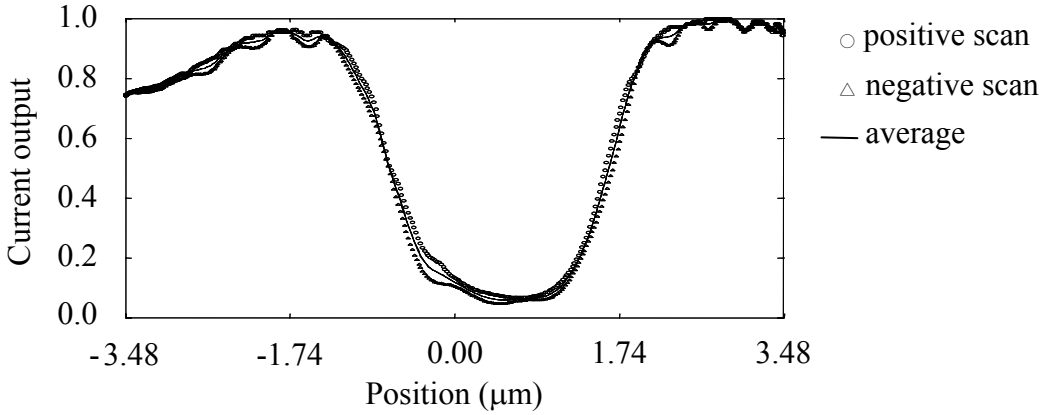


(c) (d)

Fig. 4-16 Observed signal by oscilloscope of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device with on-chip TIA in D35-97C deevice (continued)

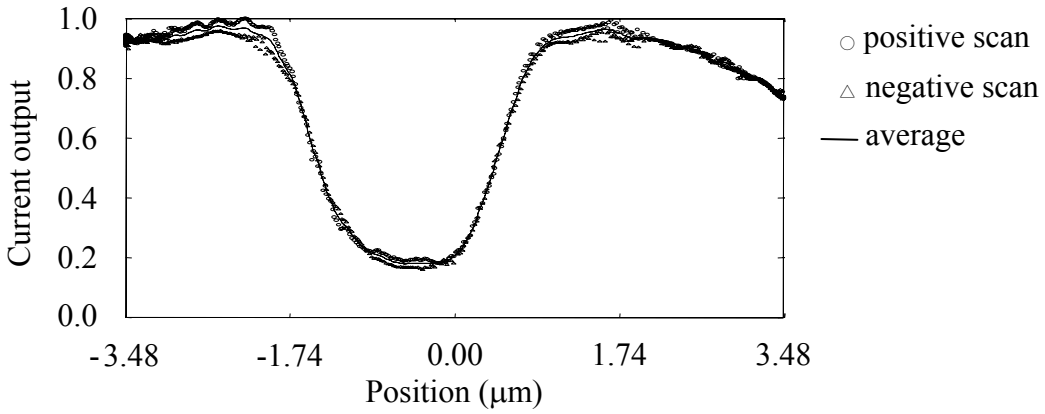


(a)

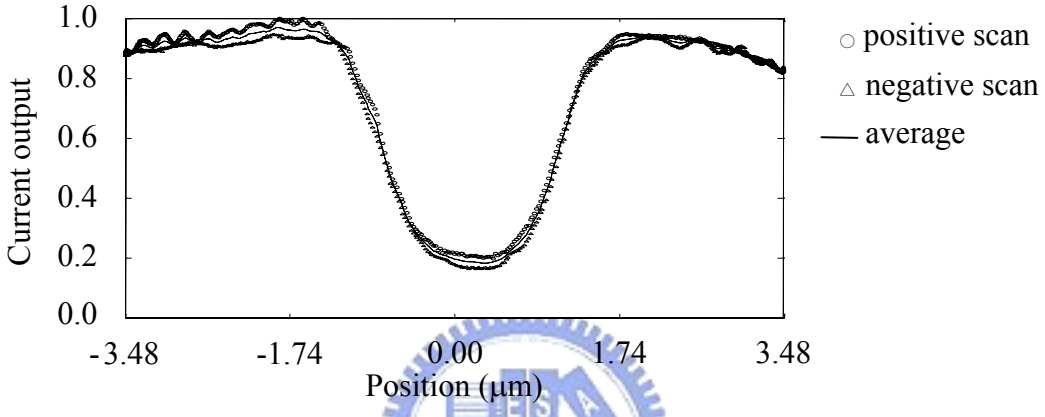


(b)

Fig. 4-17 Folded knife edge signal red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device with on-chip TIA in D35-97C deevice

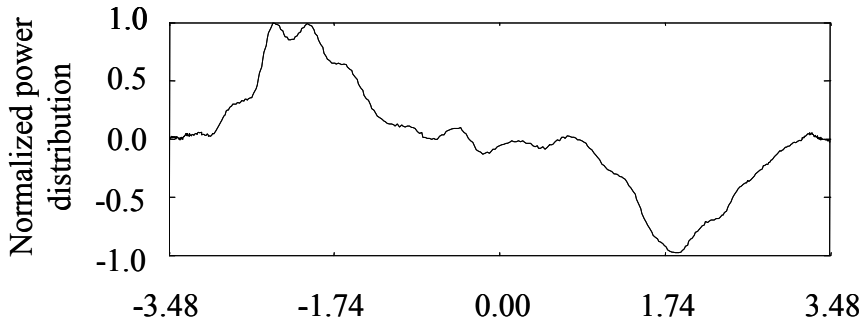


(c)



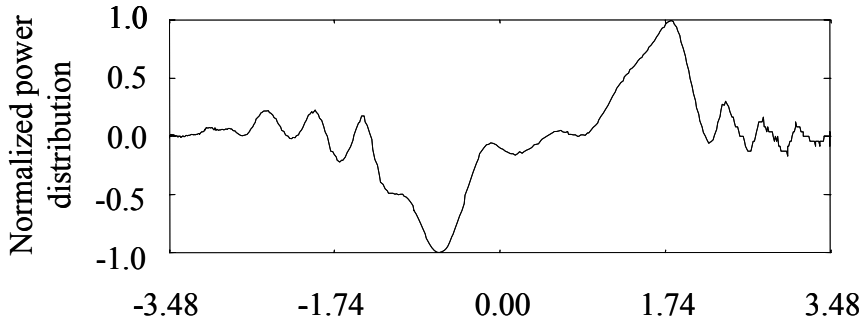
(d)

Fig. 4-17 Folded knife edge signal red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device with on-chip TIA in D35-97C deevice (continued)

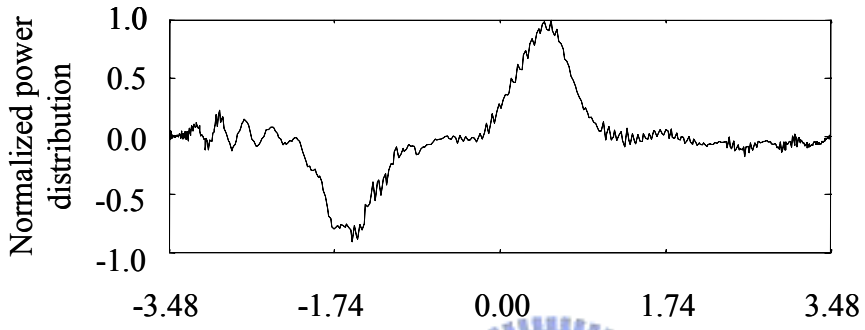


(a)

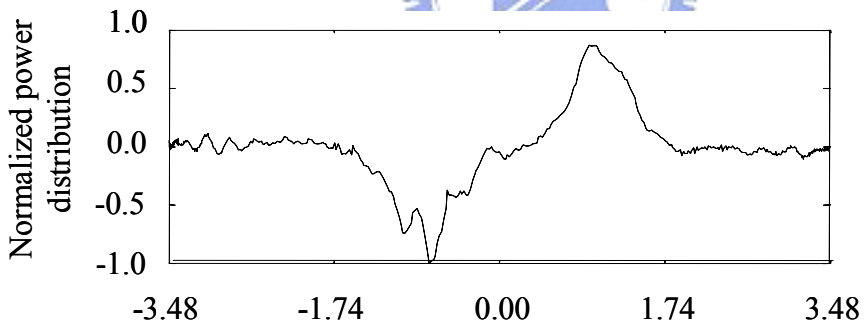
Fig. 4-18 Derived power distribution of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device with on-chip TIA in D35-97C deevice



(b)



(c)



(d)

Fig. 4-18 Derived power distribution of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-95D device with on-chip TIA in D35-97C deevice (continued)

Table 4-2 Measured and theoretical focused spot size of measurement in Fig. 4-15

	wavelength	laser power	objectives	NA	$S_{theoretical}$	$S_{measured}$
1	633 nm	10mW	20X	0.4	0.79 μm	1.00 μm
2	633 nm	10mW	40X	0.65	0.53 μm	0.66 μm
3	543 nm	0.8mW	20X	0.4	0.68 μm	0.68 μm
4	543 nm	0.8mW	40X	0.65	0.44 μm	0.53 μm

4.4.3 D35-97C device measurement with on-chip TIA

Optical spot profile measurement also applied to this device. The optical setup is shown as Fig. 4-19. Type 1 circuit is integrated with the photodiode in the same chip. A V_{DC} = 30 V and V_{AC}= 30 V is applied across fingers in the rotor and the stator to actuate the photodiode in the actuator.

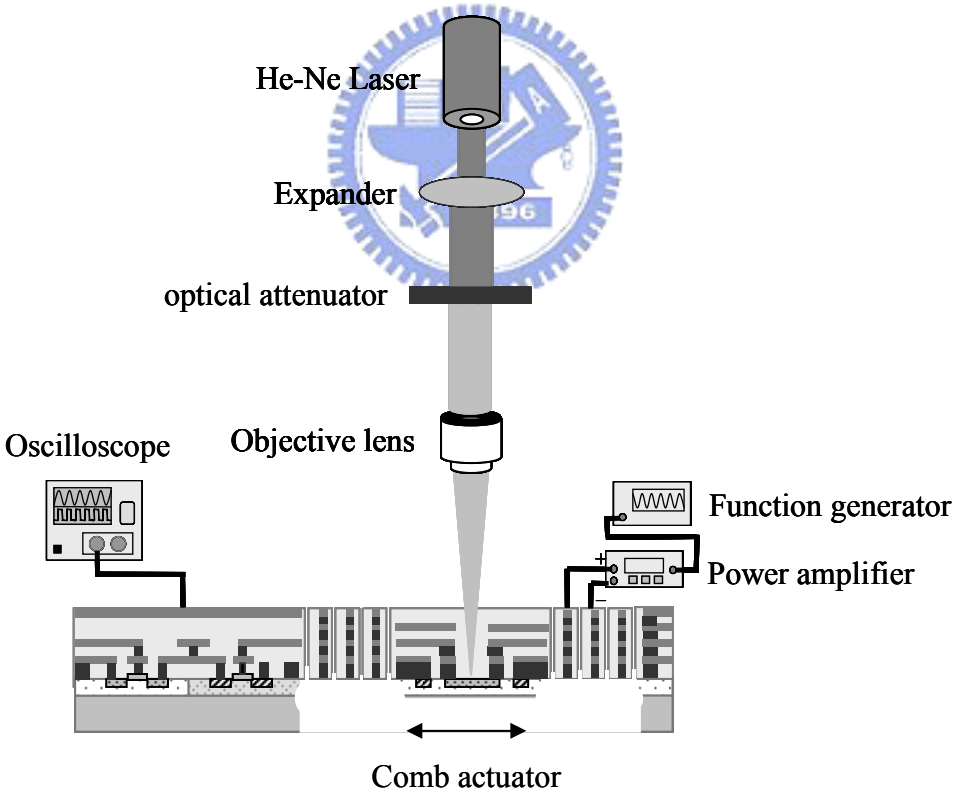


Fig. 4-19 Optical setup of spot profile experiment for D35-97C device with on-chip TIA

The captured signals are shown in Fig. 4-20.After scanning cross the measured spot, a 0.8 volts signal scale for red light measurement and a 0.2 volts signal scale for green light can be seen. The folded knife edge signals are plotted with respect to position of the photodiode (Fig. 4-21). The average photocurrent of positive and negative scan is used to calculate the spot size. The divided power distributions are shown in Fig. 4-22. The full width at half maximum (FWHM) spot size can be obtained from taking the width between the positions which the normalized power in the positions is 0.5. The measurement results are summarized in Table 4-3.

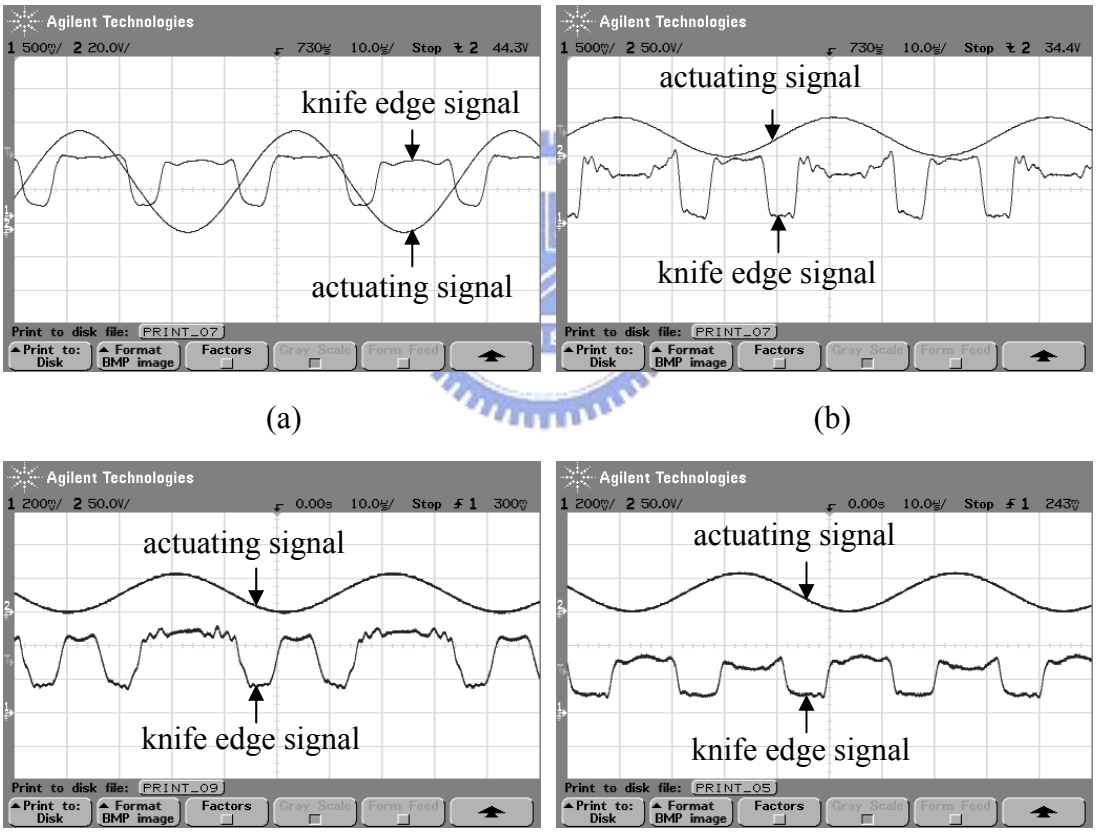
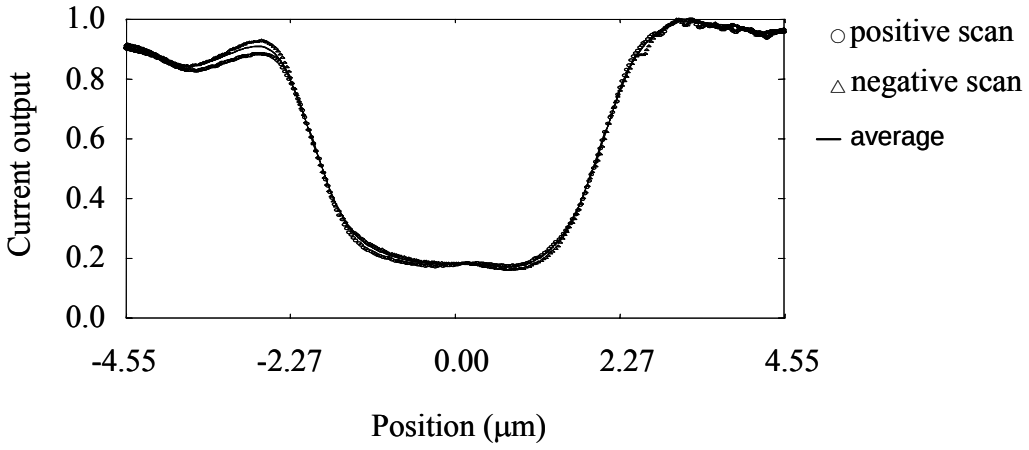
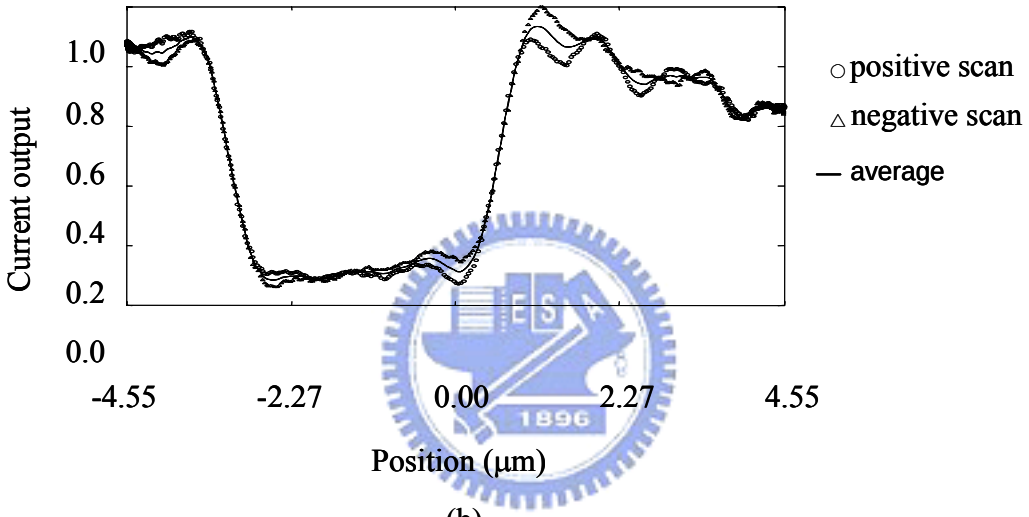


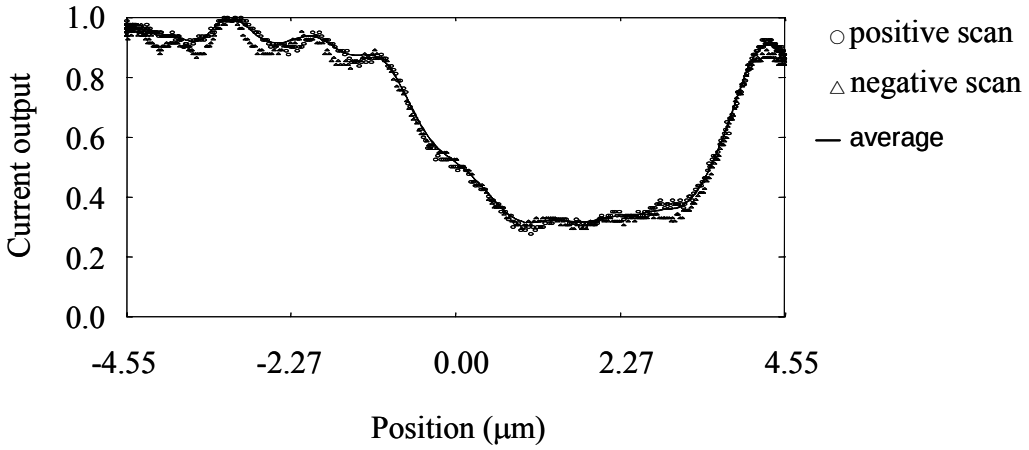
Fig. 4-20 Observed signal by oscilloscope of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-97C device



(a)

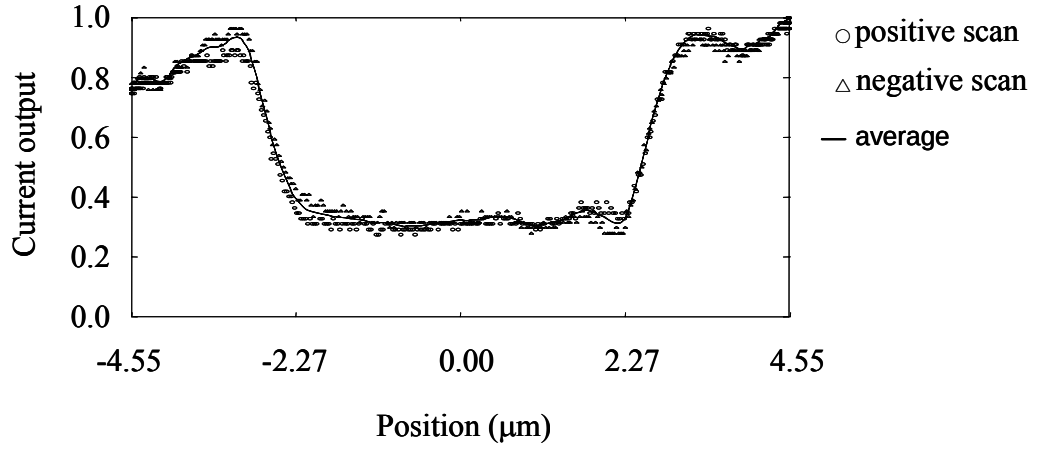


(b)



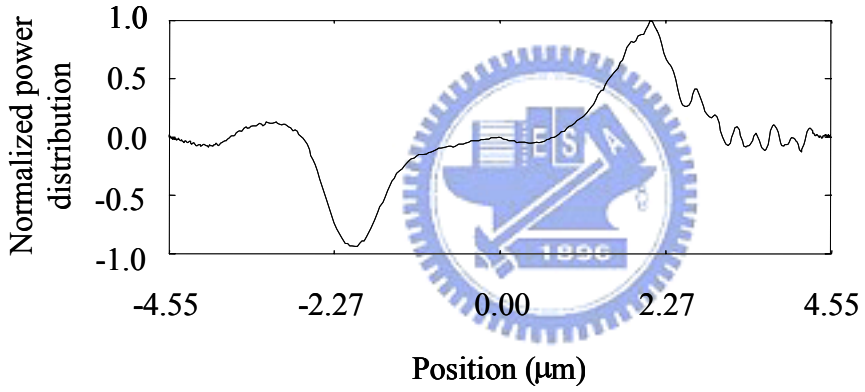
(c)

Fig. 4-21 Folded knife edge signal red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-97C device

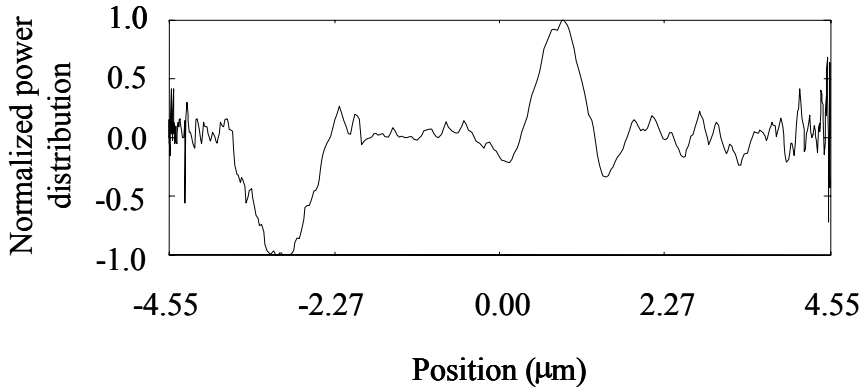


(d)

Fig. 4-21 Folded knife edge signal red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-97C device (continued)

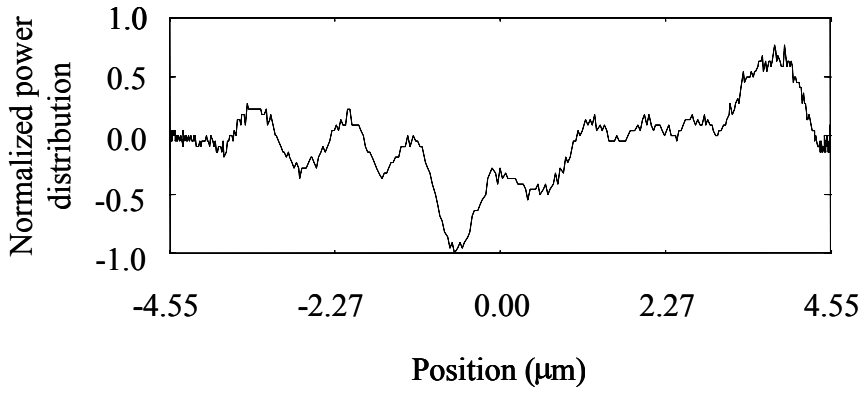


(a)

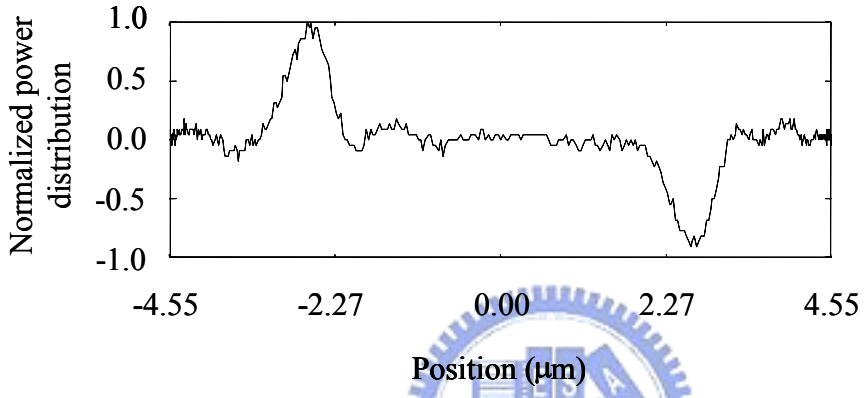


(b)

Fig. 4-22 Derived power distribution of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-97C device



(c)



(d)

Fig. 4-22 Derived power distribution of red light with (a) 20X (b) 40X objective lens and green light with (c) 20X (d) 40X objective lens for D35-97C device (continued)

Table 4-3 Measured and theoretical focused spot size of measurement in Fig. 4-19

	wavelength	laser power	objectives	NA	$S_{theoretical}$	$S_{measured}$
1	633 nm	10mW	20X	0.4	0.79 μm	0.89 μm
2	633 nm	10mW	40X	0.65	0.53 μm	0.62 μm
3	543 nm	0.8mW	20X	0.4	0.68 μm	0.76 μm
4	543 nm	0.8mW	40X	0.65	0.44 μm	0.60 μm

4.5 Discussion

In the measured knife edge signals in Fig. 4-20, the DC levels of these signals are 0.1V. The DC levels drift seriously. Therefore, some samples are used to measure the DC level under attenuated red light (9.5 μW), attenuated green light (1.5 μW), and without light incident. The measured DC levels of these samples at the attenuated power are listed in Table 4-4.

Table 4-4 Measured DC level under attenuated red light, attenuated green light, and without light incident

Sample	Power of light source	Attenuated power	DC level
1	dark	0	2.92
	10 mW	9.5 μW	3.28 V
	0.8 mW	1.5 μW	3.03 V
2	dark	0	4.46 mV
	10 mW	9.5 μW	186.38 mV
	0.8 mW	1.5 μW	47.05 mV
3	dark	0	12.43 mV
	10 mW	9.5 μW	175.56 mV
	0.8 mW	1.5 μW	22.11 mV
4	dark	0	4.21 mV
	10 mW	9.5 μW	155.78 mV
	0.8 mW	1.5 μW	58.51 mV

A transfer curve of the second stage in type 1 circuit is simulated in TT corner (Fig. 4-23). The derivative of the transfer curve is obtained from the curve. When the

input voltages of the second stage are 1.38V to 1.95V, the value of derivative curve is -1. The second stage in type 1 circuit can be served as a signal amplifier when the input voltage is ranging from 1.38V to 1.95V. The corresponding output voltage of type 1 circuit is ranging from 0.27V to 2.96V. The others corners are also simulated. The ranges of corresponding output voltage level of circuit which can be served as a signal amplifier are listed in Table 4-5.

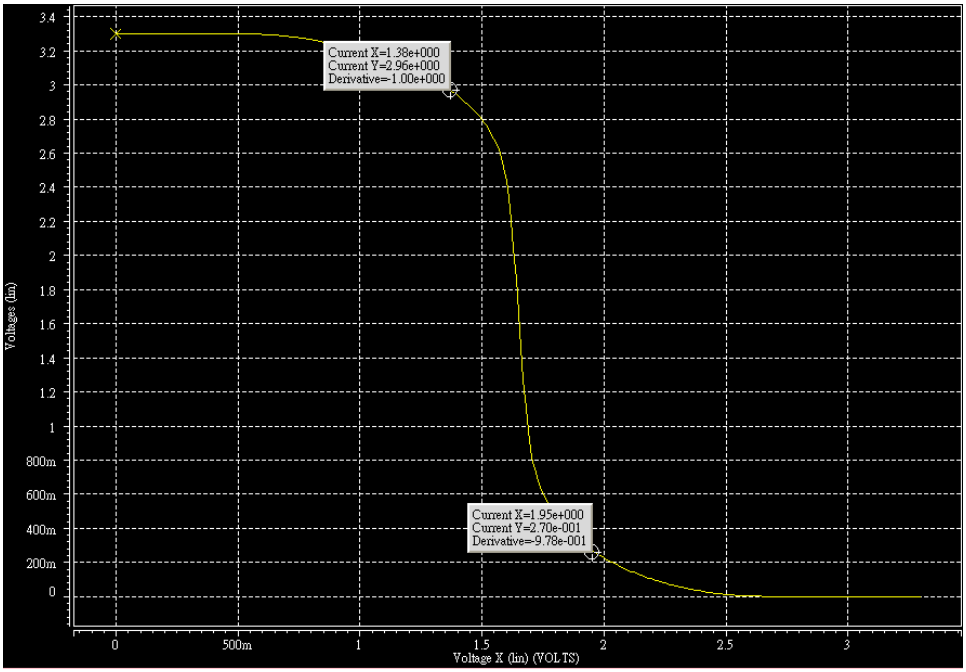


Fig. 4-23 Simulated transfer curve

Table 4-5 Corresponding output voltage level

Corner	Range of output level
TT	0.27V to 2.96V
SF	0.27V to 2.96V
FS	0.28V to 2.97V
FF	0.32V to 2.91V
SS	0.24V to 3.01V

From red light measurement, the voltage with focused light absorbed by photodiode is 0.9V and the voltage without light absorbed is 0.1V. From simulated voltage transfer curve, knife edge signals of red light are reasonable except the voltage below 0.32V. From green light measurement, the voltage with focused light absorbed is 0.3V. From simulation result, the circuit is not operated as a signal amplifier when green light incident.

4.6 Conclusion

In this chapter, the mechanical characteristics of the microstructures are measured. The measured amplitudes are less than the expected values due to partial overlapping of the comb fingers.

The responsivity of the photodiode, frequency response of the TIA and position sensor are measured. The responsivity of photodiode etched and not etched by DRIE are compared and discussed. The measurement of TIA shows the TIA can normally work. The output signal is suffered from electrical interference.

The absorption type device is used to measure the focused spot size. The measured spot sizes are all larger than the theoretical values due to imperfect optical setup. However, the function of the absorption type system is demonstrated.

Chapter 5 Conclusion and Future Work

5.1 Conclusion

In this thesis, the absorption type optical spot profiling system is designed and fabricated by post CMOS-MEMS process. The amplitude at resonant frequency is less than the expected value due to partial overlapping of the comb fingers caused by curling. The transimpedance circuit and position sensor are measured and discussed.

The spot profile in each condition is measured by the absorption type device. The measured spot sizes are larger than theoretical diffraction limits due to imperfect optical setup. However, the function of the absorption type device and the concept of the knife edge method are demonstrated.

5.2 Future work

The actuating voltage of comb drive actuator is higher than 30 volts. To reduce the actuating voltage, silicon substrate can be left in comb fingers to increase the capacitance between the rotor and the stator. The DRIE CMOS-MEMS technology can used to leave the silicon substrate in structures [25]. Additionally, the curling in fingers can be decreased by the left silicon substrate in fingers.

To obtain the optical profile, some signal processing by computer is needed. The differentiator can be integrated on chip to take differentiation of the photocurrent. Thus, the optical profile of measured spot can be obtained directly from single chip without signal processing by computer.

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