國立交通大學

電機學院　電機與控制學程

碩士論文

以MathCAD為基礎之邊界模式功率因數修正轉換器與EMI濾波器設計

MathCAD Design of Critical Conduction Mode PFC Converters with EMI Filter

研究生：洪袈瀚

指導教授：鄒應嶼 博士

中華民國九十八年十一月

以 MathCAD 為基礎之邊界模式功率因數修正轉換器與 EMI 濾波器設計

MathCAD Design of Critical Conduction Mode PFC Converters with EMI Filter

研 究 生：洪袈瀚　　Student：Chia-Han Hung

指導教授：鄒應嶼　　Advisor：Ying-Yu Tzou

國 立 交 通 大 學

電機學院 電機與控制學程

碩 士 論 文

A Thesis

Submitted to College of Electrical and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electrical and Control Engineering

November 2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年十一月

以 MathCAD 為基礎之邊界模式功率因數修正轉換器與 EMI 濾波器設計

研究生：洪袈瀚　　指導教授：鄒應嶼 博士

國 立 交 通 大 學　　電 機 與 控 制 學 程　　碩 士 班

摘要

本文主要探討用於 100W 電源級 AC-DC 功率因數改善電路，具功率因數修正之臨界導通模式升壓式功率因數修正轉換器及 EMI 濾波器之設計與功率損失分析。文中將針對採用臨界導通模式控制之升壓式功率因數修正轉換器說明電壓控制模式的原理及電路控制架構、電路設計與差模 EMI 濾波器設計並透過 MathCAD 軟體作完整連貫性的計算與設計程序，藉以探討在不同負載工作點與輸入電壓下，各個主要零件的功率損失與切換頻率的變化。再探討輸入電壓,電流,電感電流,導通時間,關閉時間與開關切換頻率對不同輸入電壓相位角度的分析比較。而設計加入一個差模 EMI 濾波器以提升系統電路的功率因數並降低總電流諧波量以符合相關的規範。再用 PSIM 軟體模擬開關控制、輸出入電壓及電流的波形與加入 EMI 濾波器後的整體功率因數校正結果，最後再由 MathCAD 整合基本計算、理論分析、模擬資料與量測資料。將計算、模擬、與實驗結果互相比對驗證。

MathCAD Design of Critical Conduction Mode PFC Converters with EMI Filter

Student: Chia-Han Hung Advisor: Dr. Ying-Yu Tzou

Degree Program of Electrical and Computer Engineering
National Chiao Tung University

Abstract

This paper presents a practical design method for the critical-conduction-mode (CRM) power-factor-correction (PFC) converter with EMI filter design by using an interactive mathematical computation and documentation software, the MathCAD. The design of CRM PFC converter is an involved process and there is a need for practical design engineers to follow an interactive and intuitive design procedure. The selection of major power components with loss analysis of the CRM PFC converter has been described. The design of input differential-mode (DM) EMI filter for the reduction of total-harmonic-distortion (THD) for line current has been developed in considerations of practical design limitations. Computer simulations have been carried out by using power electronic system simulation software, the PSIM, to verify the design results such as power factor and THD. An illustrated design procedure and analysis are presented with given design example by using the MathCAD to combine and analyze the results of design, simulation .and experiment.

誌　謝

首先我要特別感謝我的老師鄒應嶼教授這三年多來的悉心指導，增加我的專業知識能力，也讓我參與國內外的研討會投稿，使我在過程中學習到更多的知識並堆砌更好的研究架構。

感謝諸位口試委員：李迪章教授、與蔡明發教授、在口試時所給予的寶貴建議。

感謝育宗學長不吝傳授知識與經驗，讓我獲益良多。也感謝實驗室的同學夥伴哲瑋、茗皓、煒超、宗豪與國光的相互鼓勵，期勉大家未來發展順利。

感謝我任職中的美商台灣艾儀公司的同事們：競平經理及宗堅、嘉偉、宗緯、志鵬、重毅與智然在工作上的幫忙與協助，讓我得以抽空完成學業研究。

特別感謝親愛的老婆能夠體諒我忙碌的研究生活與工作，一路陪伴在我左右，不時地給予我鼓勵，讓我能夠持續堅持我的理想。也感謝今年八月中出生的兒子睿廷，能夠即時與我一同分享喜悅。

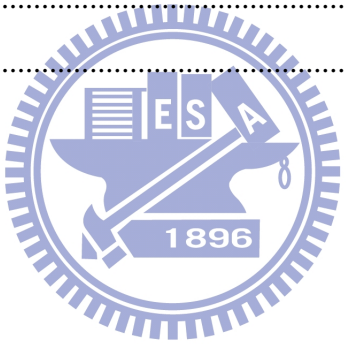
最後，要特別感謝我慈愛的雙親，是你們的栽培，才有今日的我，願將此榮耀和喜悅與你們一同分享。

僅以此論文獻給所有關心我的長輩、師長與朋友們…

洪袈瀚

2009 秋天 於新竹交大

TABLE OF CONTENTS



LIST OF TABLES

LIST OF FIGURES

Chapter 1

Introduction

1.1 Research Background and Recent Development

Power-factor-correction (PFC) is necessary for off-line switch mode power supplies (SMPS) required output powers above 75 W. Active PFC techniques gets its fast development due to the requirement in EU to meet the compliance of EN 61000-03-2 for the regulation of current harmonics [1]. Table Ⅰ shows the EN-61000-3-2 standard for the regulation of harmonics for utility interface of class D equipments, which includes specifically PCs, their monitors, and LCD TV.

Critical-conduction-mode (CRM) PFC converters provides its advantages such as zero-voltage-switching (ZVS) for the turn-on of MOSFET and zero-current-switching (ZCS) for the turn-off of the diode. Therefore, the CRM PFC converter can reduce its switching loss significantly for low power applications. The CRM PFC converter has two major disadvantages. The first disadvantage is its high input current harmonics. The peak inductor current is two times higher than CCM at the same power level. The larger of inductor and the differential-mode EMI filter are necessary and increase the circuit cost and size. Interleaving techniques for the CRM PFC can reduce the input current and EMI filter size. The second disadvantage of CRM PFC is the wide switching frequency range increase the design complexity of differential-mode (DM) EMI filter and the switching loss.

In view of the wide applications of CRM PFC control scheme in low-power off-line power converters. Few investigations have been done on the overall design and analysis of

CRM PFC [1]-[4]. This research uses the systematic method with illustrated design example for the design of CRM PFC converter includes power loss, DM EMI filter and hardware design by using MathCAD [5]. The MathCAD provides a user friendly equation-like interactive technical document interface for input and computing of the symbolic mathematical equations. The illustrated design equations with their computation results can be directly output to a user defined graph with text form documentation [6]-[7]. The developed MathCAD design method has been verified by computer simulation using the PSIM software.

1.2 Objectives and Contributions

The research objectives of this thesis is thus in three-folds. The first one is to develop an effective and practical method using MathCAD for the hardware design, EMI filter and characteristic analysis such as power losses, power factor and current harmonics of CRM PFC to improve the consistency and correction of design by showing the calculated result with unit and graph. It also reduces the design period. It also assists the studying of students. Students can easy to completely imitate the MathCAD model to modify the parameters for different conditions and design [8]-[9]. The present result is useful in this simplicity and easy to apply to the study.

The second objective is to develop a program to calculate the power losses for major component and comparing the total losses with the simulations of PSIM.

The third objective of this study is to develop a sample method for EMI filter design and verify the results with the simulations of PSIM.

1.3 Thesis Organizations

The dissertation is organized as follows. In Chapter 2, the fundamentals of power factor, the mathematical modeling of Boost PFC, and the control methods are presented. The

inductor current modes are reviewed. At least, an introduction of input EMI filters for ac line-powered equipment will be presented based on the analysis of conducted EMI problems and the use of an EMI Filter.

In Chapter 3, a control architecture analysis and operation of critical conduction mode PFC IC MC33260 is presented, and verifying the behavior by PSIM. The design procedures for each component and analysis are designed by MathCAD. The power loss of each component and the effect of phase vs. different loads are analyzed by MathCAD. Four simple designs for EMI filter are presented and verified by the simulation of PSIM. Simulation comparison and analyses are also given in this chapter.

In Chapter 4, the simulations of PSIM and the experiment results are combined to a MathCAD program to analyze the input current harmonics distortion (THD) and power factor then an estimation of the effect of DM-EMI filter and the improved current harmonic and waveform are calculated by MathCAD and simulated by PSIM in this chapter.

Some concluding remarks and suggested future works related to this research are summarized and discussed in Chapter 5 for the design performance review. And the design program of MathCAD is given in appendix.

Chapter 2

Review of Critical Conduction Mode Power Factor Correction

2.1 Definition of Power Factor

Power factor (PF) is simply defined as the ratio of real power to apparent power [10]. And the PF is given by following equation:

$$\mathrm{PF} = \frac{P}{S} = \frac{\text{Real Power}}{\text{Apparent Power}} = \frac{\frac{1}{T}\int_0^T v(t)\cdot i(t)dt}{V_{rms}\cdot I_{rms}}. \tag{2-1}$$

Fig. 2.1 show the input current $i(t)$ drawn from the utility by the power electronic equipment becomes a non-sinusoidal waveform, $i_1(t)$ is the fundamental of $i(t)$ and its RMS value is represented as $I_{1,rms}$. θ is the phase angle between the sinusoidal $i_1(t)$ and the input voltage $v(t)$.

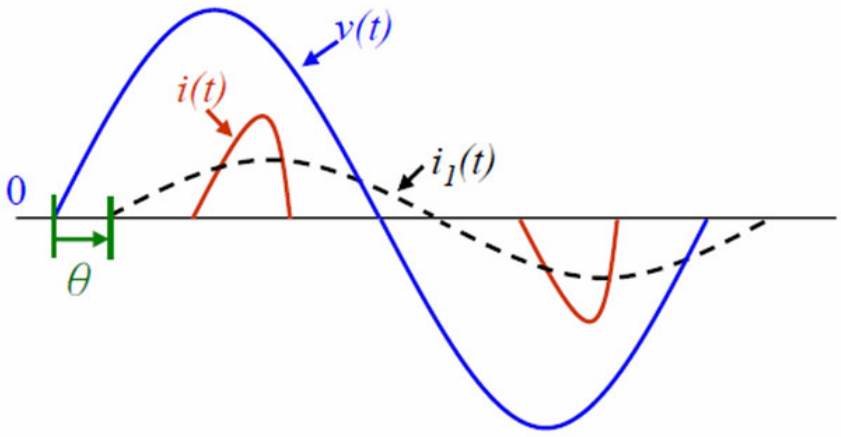


Fig. 2.1. Input current distortion.

The real power is equal to average power and can be represented as

$$\begin{aligned} P &= \frac{1}{T}\int_0^T p(t)dt = \frac{1}{T}\int_0^T v(t)\cdot i(t)dt \\ &= \frac{1}{T}\int_0^T \sqrt{2}V_{rms}\sin(\omega t)\cdot\sqrt{2}I_{1,rms}\sin(\omega\omega-\theta)dt \\ &= V_{rms}\cdot I_{1,rms}\cdot\cos\theta \end{aligned} \tag{2-2}$$

Substituting (2-2) into (2-1)

$$\mathrm{PF} = \frac{P}{S} = \frac{V_{rms}\cdot I_{1,rms}\cdot\cos\theta}{V_{rms}\cdot I_{rms}} = \frac{I_{1,rms}}{I_{rms}}\cos\theta \tag{2-3}$$

The displacement power factor (DPF) is defined as $\cos\theta$.

$$\mathrm{DPF} = \cos\theta \tag{2-4}$$

The DPF is equal with PF in linear circuit with sinusoidal current and voltage.

The power factor with a non-sinusoidal current then become

$$\mathrm{PF} = \frac{P}{S} = \frac{V_{rms}\cdot I_{1,rms}\cdot\cos\theta}{V_{rms}\cdot I_{rms}} = \frac{I_{1,rms}}{I_{rms}}\cdot\mathrm{DPF} \tag{2-5}$$

The RMS value of input current, I_{rms} can be defined as

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i^2(t)dt} = \sqrt{{I_{1,rms}}^2 + \sum_{n\neq 1}{I_{n,rms}}^2} \tag{2-6}$$

The distortion component is defined as

$$I_{dis} = \sqrt{{I_{rms}}^2 - {I_{1,rms}}^2} = \sqrt{\sum_{n\neq 1}{I_{n,rms}}^2} \tag{2-7}$$

Then the total harmonics distortion (THD) of current is defined as

$$\mathrm{THD} = \sqrt{\sum_{n\neq 1}\left(\frac{I_{n,rms}}{I_{1,rms}}\right)^2} = \sqrt{\left(\frac{I_{rms}}{I_{1,rms}}\right)^2 - 1} = \frac{I_{dis}}{I_{1rms}} \tag{2-8}$$

The distortion factor k_d is defined as

$$k_d = \left(\frac{I_{1,rms}}{I_{rms}}\right) \tag{2-9}$$

Substituting (2-9) into (2-8)

$$\mathrm{THD} = \sqrt{\frac{1}{{k_d}^2} - 1} \tag{2-10}$$

k_d is redefined as

$$k_d = \frac{1}{\sqrt{1+(\text{THD})^2}} \tag{2-11}$$

k_θ is defined as DPF

$$k_\theta = \text{DPF} = \cos\theta \tag{2-12}$$

In terms of (2-5) and (2-8), the power factor can be expressed as

$$\text{PF} = \frac{1}{\sqrt{1+(\text{THD})^2}} \cdot \text{DPF} \tag{2-13}$$

In case where both the fundamentals of input voltage and input current are in phase, the DPF =1, the power factor definition simplifies to follow equation.

$$\text{PF} = \frac{1}{\sqrt{1+(\text{THD})^2}} \tag{2-14}$$

The relationship between power factor and total harmonics distortion is shown in Fig. 2.2 [11].

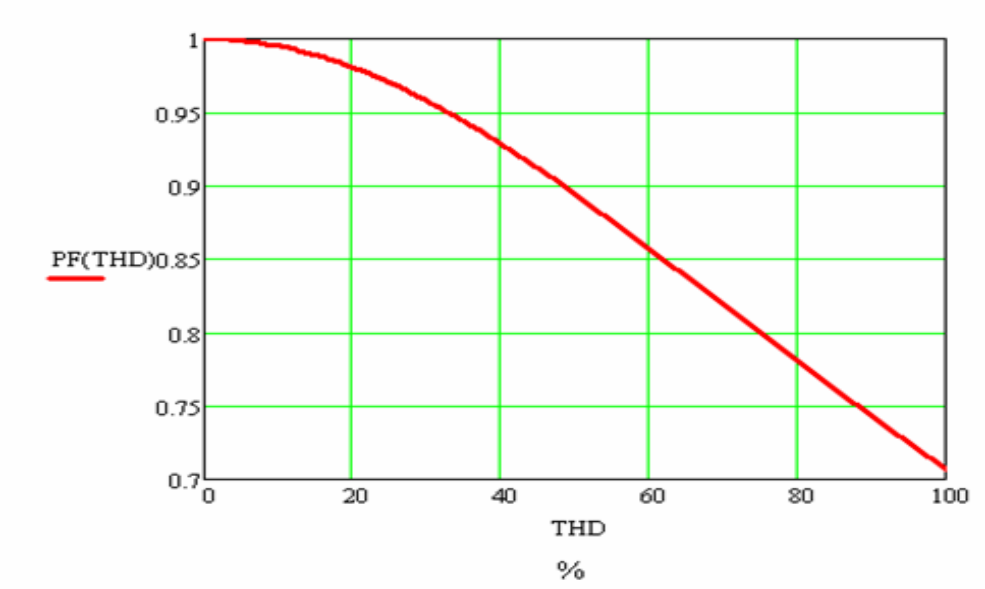


Fig. 2.2. Relationship between PF and THD

Substituting (2-11), (2-12) into (2-13)

$$\text{PF} = k_d \cdot k_\theta \tag{2-15}$$

2.2 Power Factor Correction Theorem

2.2.1 Harmonic Limits

The present, electrical equipment must comply with the European Standard EN61000−3−2 in Europe [12]. This requirement applies to most electrical equipment beyond 75 W and under 600W, and it specifies the maximum amplitude of line frequency harmonics up to the 39th harmonic as shown in Table 2-1 [5].

Table 2-1
Limits For EN61000-3-2 Class D Equipments

Harmonic order n	Maximum permissible harmonic current per watt,mA/W	Maximum permissible harmonic current,A
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13≦n≦39 (odd harmonics only)	3.85/n	2.25/n

2.1.2 Passive PFC vs. Active PFC

Fig. 2.3 shows the input circuitry of the PC power supply with passive PFC. One switch is designed to change the setting of input voltage between 115 Vac and 230 Vac. In the 230 Vac condition both halves of the inductor winding are used with the rectifier function of full-wave. In the 115 Vac condition only the left half of the inductor is used with the rectifier function of half-wave [13]. The typical power factor value for passive PFC circuit is around 0.7 only. It may able to increase to 0.9 in special case [11].

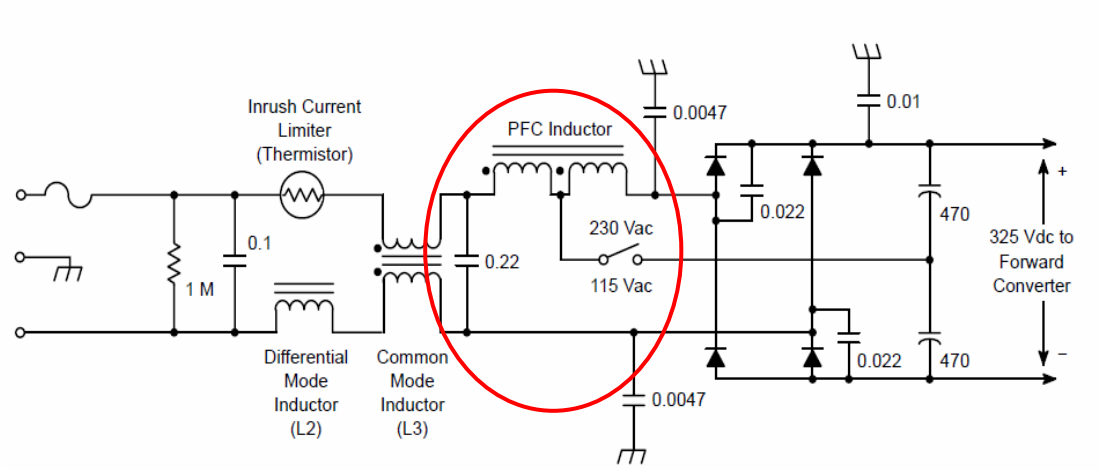


Fig. 2.3. Passive PFC in a 250 W PC Power Supply.

Active PFC converter has better performance than the passive PFC. It also designed to work in widely input voltage range (85 Vac~265 Vac) without any switch to select the input voltage range. Active PFC can be classified as buck converter, boost converter, and buck-boost converter [14].

Because of the boost converter represents the better performances than buck converter and buck-boost converter such as system design simplicity, low part count, and better efficiency. The boost converter is easy to implement and works well [15]. So the boost converter topology becomes the common used to realize the active PFC. The simple circuit in Figure 2.4 is a circuit of boost PFC and it is easy to improve the power factor close to unity.

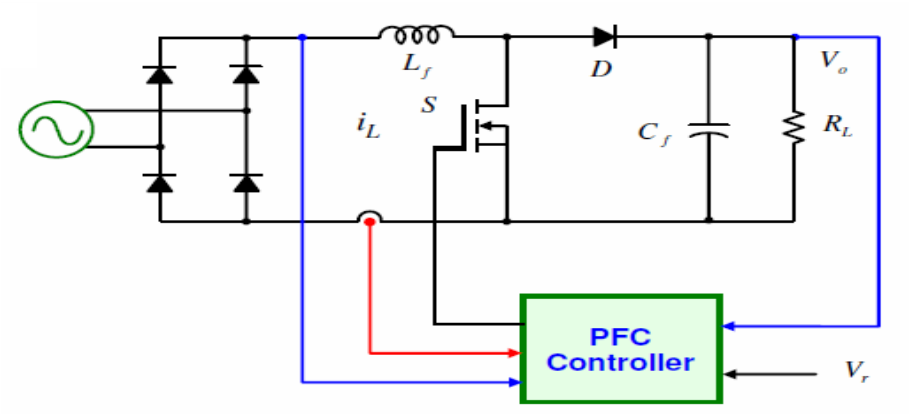


Fig. 2.4 Active boost PFC circuit.

Fig. 2.5 shows the input current waveforms between no PFC, passive PFC and active PFC. Basically, the power factor of passive PFC be limited by operation voltage.

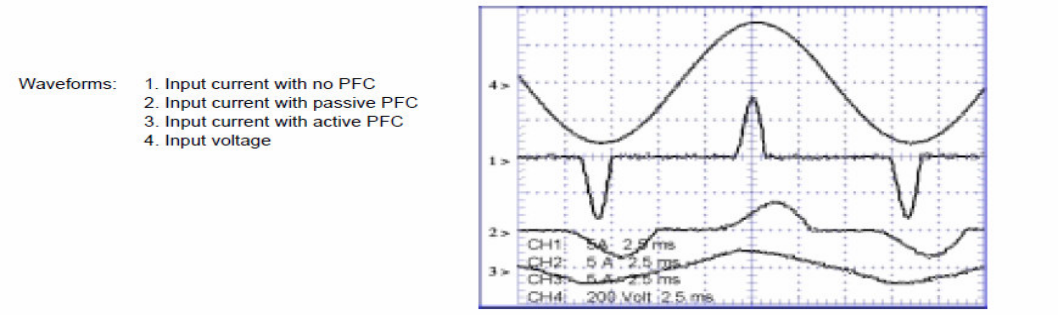


Fig. 2.5. Input characteristics of power supplies with different PFC types [13].

2.3 BOOST MODE PFC OPERATING

Depending upon how much power is drawn by the unit, three kinds of different common control modes can be chosen. All of the schematics are the same, but the value of the PFC inductor and the control method are different. A discontinuous–conduction-mode (DCM) control scheme is typically used for input power of less than 75 W, in which the PFC inductor is completely emptied prior to the next power switch conduction cycle. For powers between 75 and 300 W, the critical-conduction-mode (CRM) is recommended. This is a method of that the control IC senses when the PFC inductor is emptied of its energy then the next power switch conduction cycle is immediately begun. The continuous–conduction-mode (CCM) control is recommended for the power level greater than 300 watts. All of waveforms of inductor current are shown in Figure 2.6 [5].

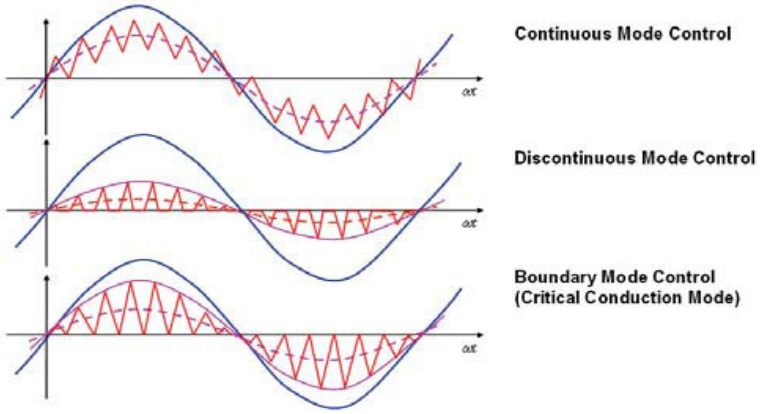


Fig. 2.6. PFC inductor current profiles.

2.3.1 *Discontinuous Conduction Mode*

In the DCM of operation, the inductor current falls to zero prior to the end of the switching period as shown in Fig. 2.7.The peak inductor current is much higher than others mode, such as CRM and CCM mode.

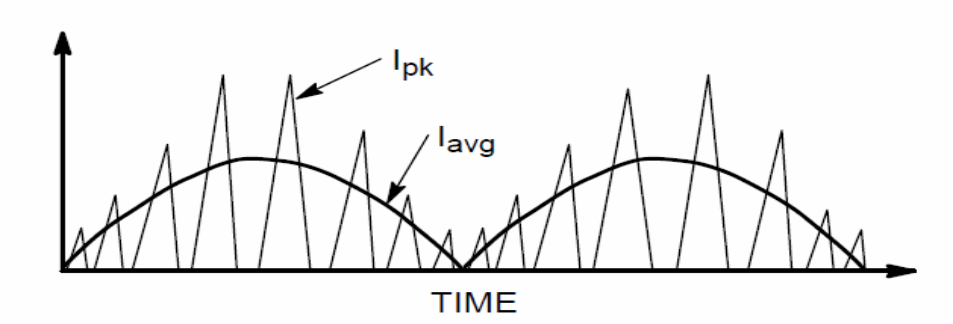


Fig. 2.7. Inductor current waveform in DCM.

2.3.2 *Critical Conduction Mode*

The CRM operation of the boost PFC converter provides its advantages for zero voltage switching (ZVS) for the turn-on of the MOSFET and zero current switching (ZCS) for the turn-off of the diode. Therefore, the CRM PFC converter can reduce its switching loss significantly for low power applications. But its high peak current puts some limitations for the higher power applications. Fig. 2.8 shows the waveforms of inductor current, diode current with fixed on time operation.

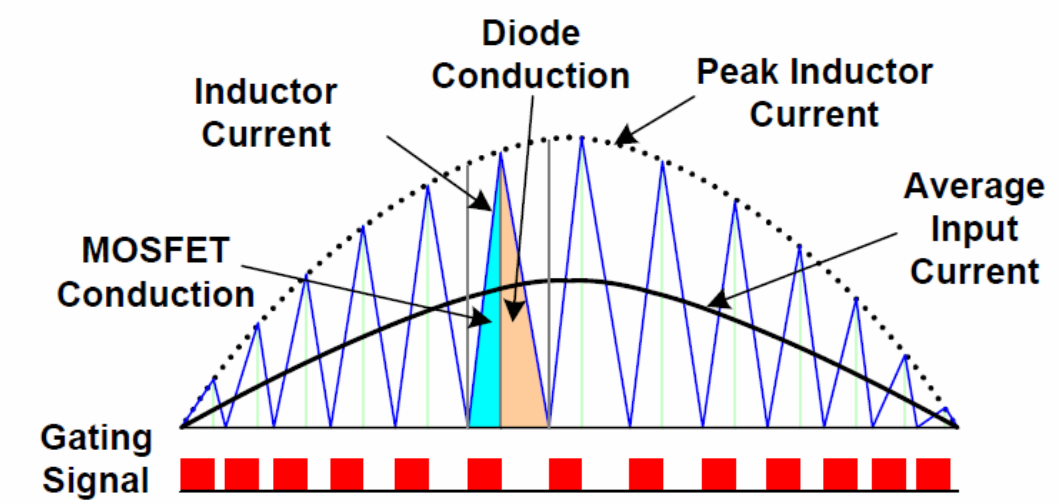


Fig. 2.8. CRM boost PFC inductor current and diode current waveforms [18].

2.3.3 *Continuous Conduction Mode*

In CCM circuit the peak currents can be lowered by using the larger inductor, but it also increase the cost of inductor and the size of PCB. Another one trouble is the reverse recovery characteristic of the output rectifier encountered, and it adds an additional 20~40 % losses into the PFC circuit. Fig. 2.9 shows the waveform of inductor in CCM mode as detail. It shows the advantage of lower inductor current decreases lower current distortion.

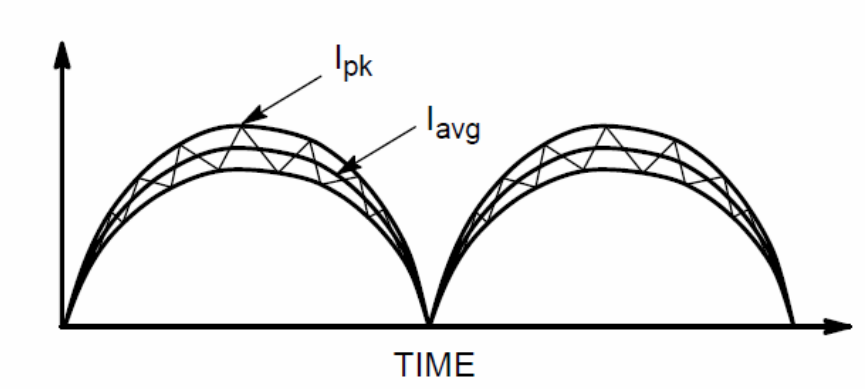


Fig. 2.9. CCM Inductor current waveform.

2.3.4 *Comparison of DCM, CRM and CCM*

A comparison of power losses between CCM and CRM based on 100 KHz switching frequency, widely input voltage (85V~265V), and 400VDC output voltage is shown in Fig 2.10 and Fig 2.11 and it is easy to find out the CCM PFC is suitable in the power range

greater than 300W due to better efficiency [16].

Fig. 2.10. CRM vs. CCM power losses analysis.

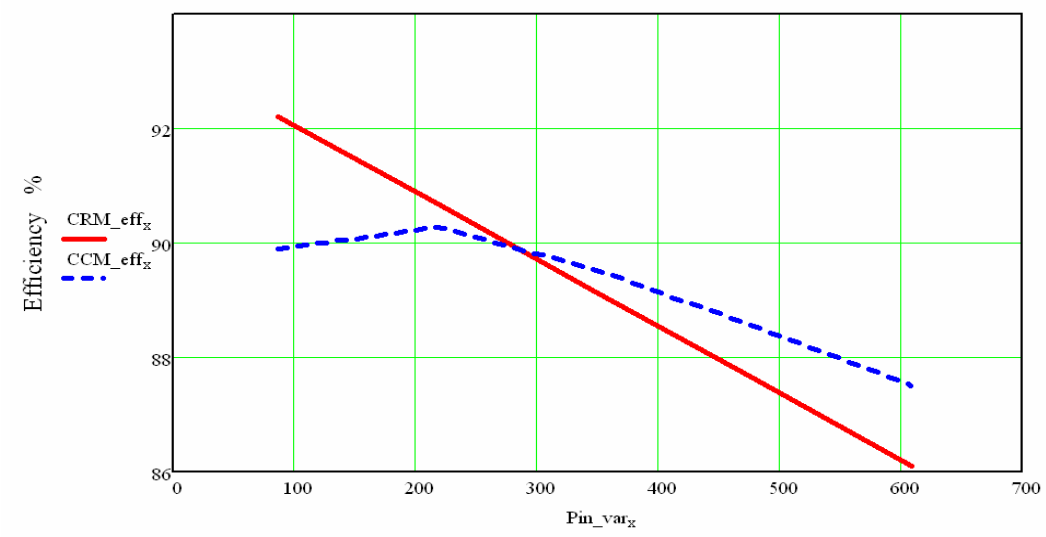


Fig. 2.11. CRM vs. CCM efficiency analysis.

TABLE 2-2

COMPARISON OF DCM, CRM AND CCM

Mode	Power level	Advantages	Disadvantages
DCM	<75W	MOSFET ZVS switching Suitable for low power applications	Highest peak current High current harmonics distortion Difficult to design the EMI filter due to widely switching frequency range
CRM	75~300W	Diode ZCS switching MOSFET ZVS switching	High peak current High current harmonics distortion Difficult to design the EMI filter due to widely switching frequency range
CCM	>300W	Low peak current Low harmonics distortion	High power losses in low power applications Big component size

2.4 CONTROL ARCHITECTURE OF CRM PFC IC

2.4.1 Voltage control without a Multiplier

There are two schemes to realize the CRM PFC IC. One control strategy can be generated without using a multiplier to fix the switch on-time as constant according to the output signal of the voltage error amplifier and a saw tooth generator and the switch current sensing can be eliminated as shown in Fig. 2.12, and its main waveforms are shown in Fig. 2.13. The PFC IC's are: MC33260 (ON Semiconductor) [17] and FAN7529 (Fairchild) [18].

In voltage control mode, only the output voltage is monitored. The voltage error signal is calculated by forming the difference between actual the output voltage and desired out voltage. This error signal fed into a comparator to compare it with the ramp voltage generated by the internal oscillator section of the control IC. The comparator converts the voltage error signal into the PWM drive signal to the MOSFET. The output voltage is the key control parameter, with an internal delay through the circuit, so the voltage control mode tends to respond slowly to the input.

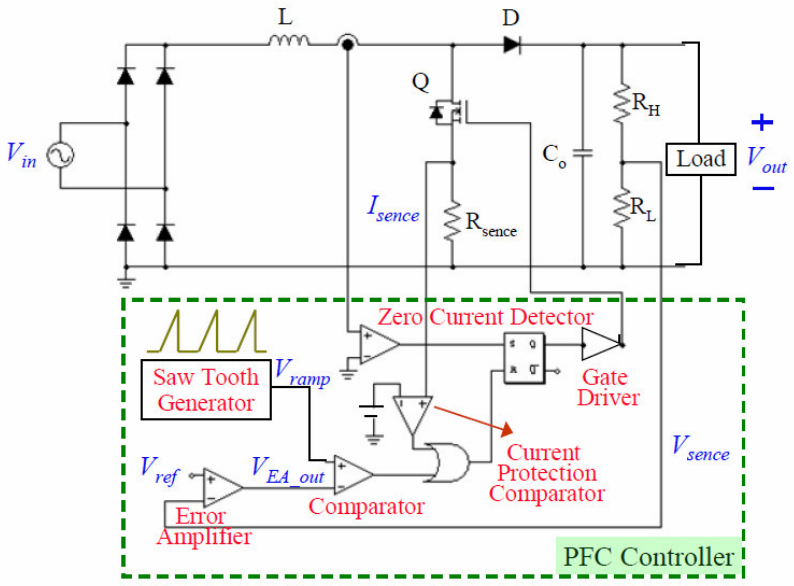


Fig. 2.12. The architecture of boundary mode PFC controls the constant turn on time.

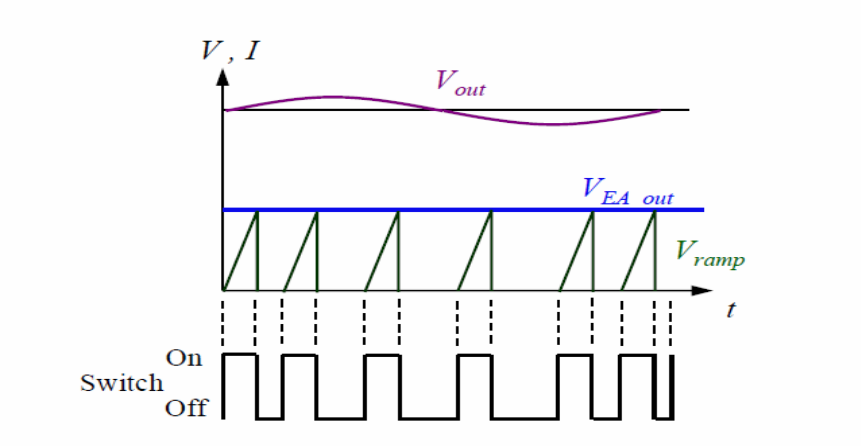


Fig. 2.13. Main waveforms of the boundary mode PFC with constant turn on time.

2.4.2 *Current control with a Multiplier*

Another control strategy is use a multiplier for generating a current command proportional to the input voltage, as shown in Fig. 2.14, and the switch is turned off when the switch current is sensed achieving the borderline of the multiplier output, as shown in Fig. 2.15. The Type of IC's: MC33262 (ON Semiconductor) [19], L6561 (STMicroelectronics) [20] and UCC38050 (Texas Instruments) [21]. Current Control mode is typically used with boost–type converters. It monitors not only the output voltage, but also the input voltage. The voltage error signal is used to control the peak current during each power switch on–time. Current control mode provides a very rapid input and output response time with an internal over current protection.

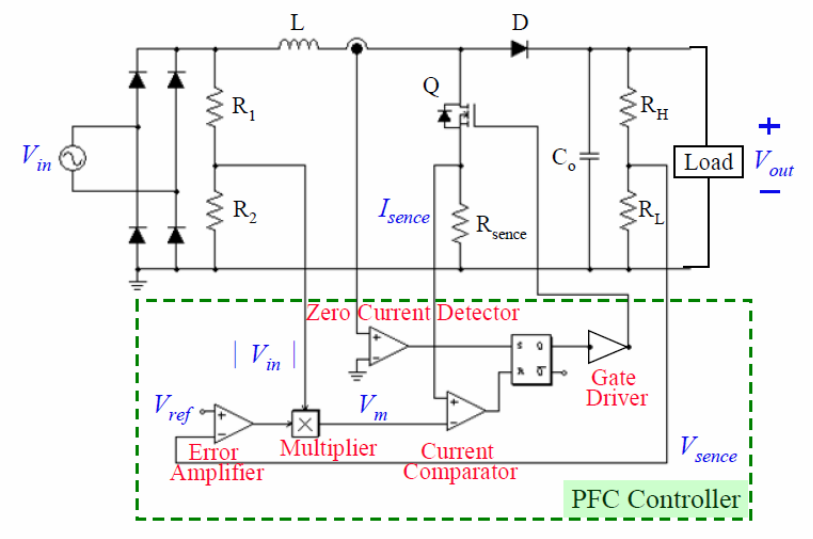


Fig. 2.14. The circuit architecture of boundary mode PFC uses the multiplier.

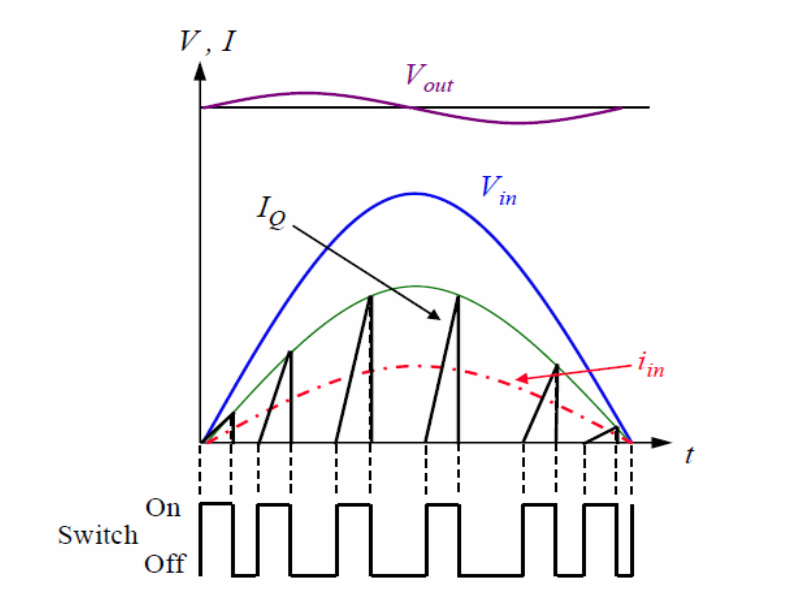


Fig. 2.15. Main waveforms of the boundary mode PFC with a multiplier.

2.5 INPUT EMI FILTERS

The design of conducted electromagnetic interference (EMI) filters for PFC circuits is more and more important for the fast development of power electronic product and the accompanied EMI reduction standards. The design procedure is not an exact science. It usually likes a try-error process for a designer to come up with a proper filter design. So, designing an EMI filter is a time-consuming process not only for junior engineers but also for experienced engineers when they meet new design.

The following three major requirements are important for the EMI filter design:

1. Requirement for switching noise attenuation,
2. Low input displacement angle (IDF) between input voltage and input current,
3. Overall system is stability.

The first requirement is defined by the EMI control standards, such as the frequency range from 10 kHz to 30MHz for VDE 0871/B limits and 450 kHz to 30MHz for FCC limits by definition the conducted EMI.

The second requirement exists only for the PFC circuit input EMI filter design. Fig. 2.16 [25] shows a simplified diagram of a PFC converter with a standard L-C input EMI filter. The voltage V_a causes the reactive current, i_c. The I_A has the phase shifted relative to the input voltage, V_A by the angle θ are given by following equations (2-12)~(2-15).

$$V_a \cong V_A = V_m \cos \omega t \tag{2-12}$$

$$I_a = I_m \cos \omega t \tag{2-13}$$

$$I_A = I_a + i_c = I_m \cos \omega t - \omega \cdot C \cdot V_m \sin \omega t \tag{2-14}$$

$$\theta = \tan^{-1} \frac{\omega C V_m}{I_m} \tag{2-15}$$

where V_m is the voltage amplitude

I_m is the current amplitude

The capacitor size has to be minimized and the limit value is given in equation (2-16) [25]-[26]

$$C_{max} = \frac{I_m}{\omega V_m} \tan(\cos^{-1} IDF) \tag{2-16}$$

$$L = \frac{1}{\omega^2 C_{max}} \tag{2-17}$$

where C_{max} is the sum of all capacitance in the filter

ω is the value of $2\pi \times$ line frequency

Fig. 2.17 shows the phasor diagram of the input currents and voltages. It is important to design a minimum displacement angle between the input current and voltage and keep low phase shift after the input EMI filter is added.

The third requirement amounts to controlling the impedance interaction between the input filter and the PFC converter. The filter output impedance should be small than the converter input impedance to keep the stability of system [22]-[24]. The impedance interaction constraint will practically determine the lower bound on the filter capacitor value. Additionally, proper filter pole damping is very important to achieve low filter output impedance for all frequencies and keep the overall system stability.

In order to keep the filter component values and size small, the filter corner frequency has

to close to the switching frequency. So, the high-order filters can have a reasonable size and meet all the requirements in the PFC circuit.

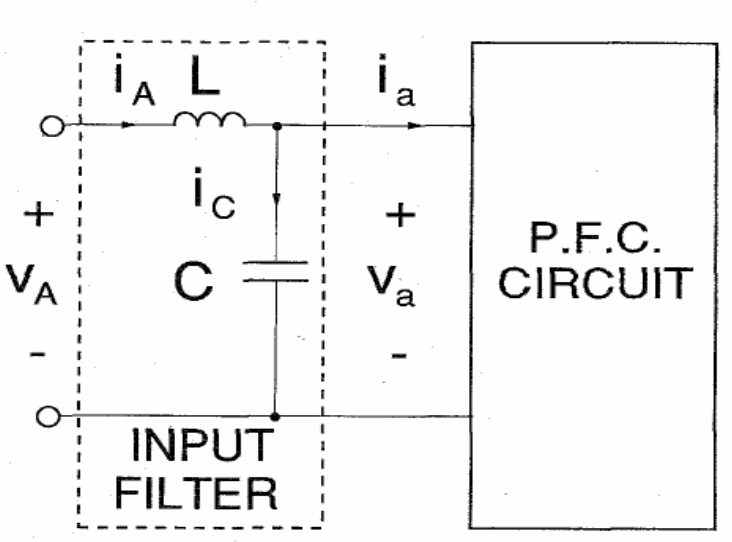


Fig. 2.16. PFC Circuit with simply input EMI filter diagram [25].

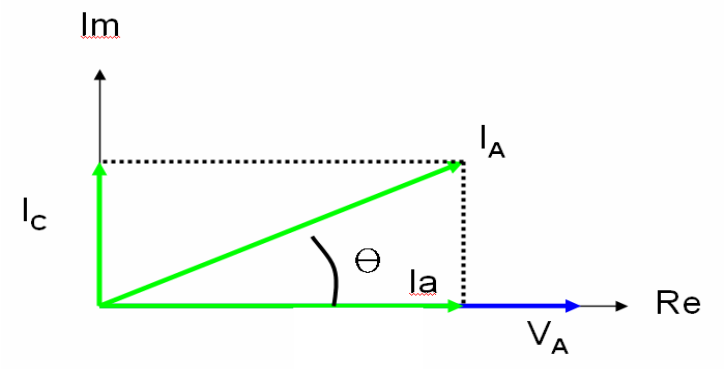


Fig. 2.17. Input voltage and current phasor diagram [25].

Usually, the total conducted EMI noise is caused by two parts, the common-mode (CM) noise and the differential-mode (DM). Normally the DM noise is related to switching current the source is a switch component such as MOSFET, and the CM noise is related to capacitive coupling of switching voltage into the input. Fig.2.18 shows the typical setup for conducted EMI measurement [27]. The LISN contains the components: inductors, capacitors and 50 W resistors. The inductors are shorted; the capacitors are open for a 60 Hz line

frequency. For EMI noise frequency, the inductors are essentially open, the capacitors are shorted and the noise sees 50 W resistors.

The noise voltage measured across the 50 W input impedance of a spectrum analyzer is defined as the conducted EMI emission.

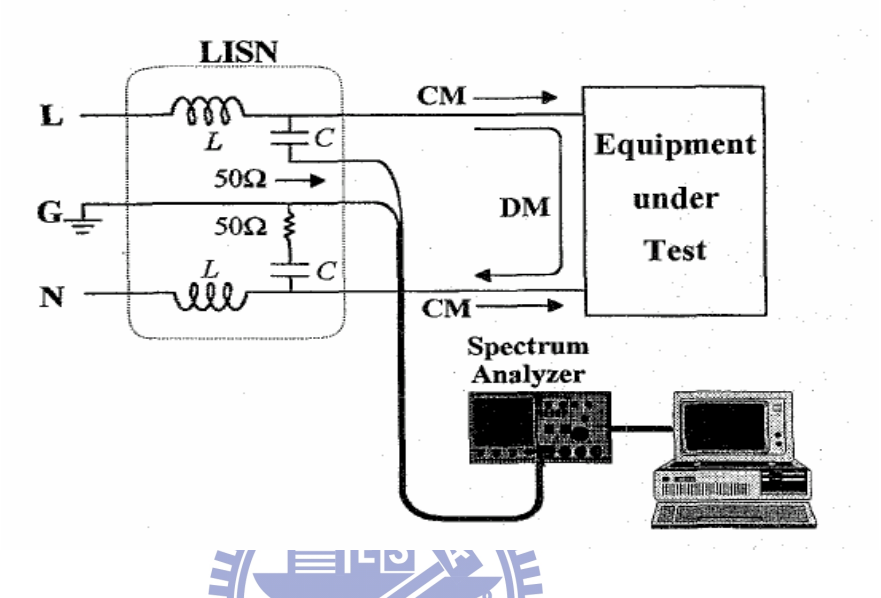


Fig. 2.18. Test setup for conducted EM1 measurement.

Fig. 2.19 shown a typical EMI filter topology, and the Fig. 2.20 (a) and (b) shows the equivalent circuit of CM section and the DM section. It also indicates that some components of filter affect the CM or DM noise only and some components of filter affect both of CM and DM noise [27].

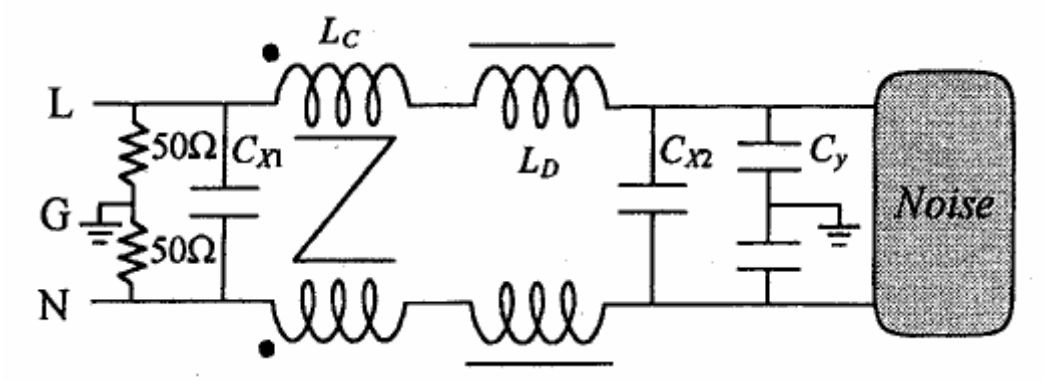


Fig. 2.19. A typical EMI filter topology.

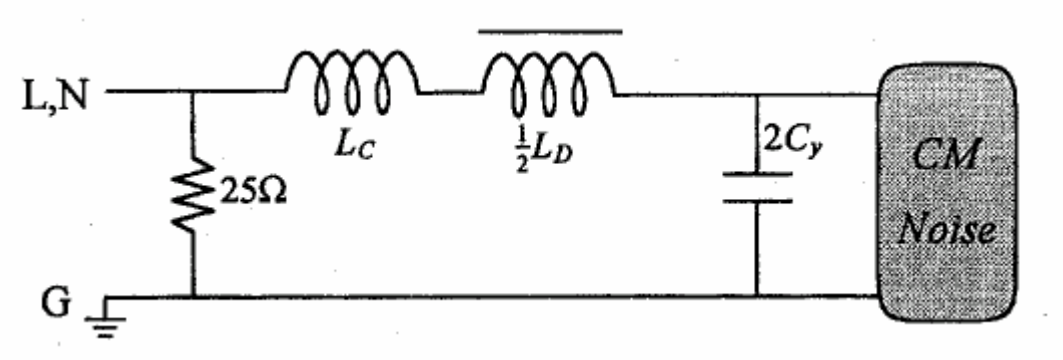


Fig. 2.20. CM noise equivalent circuit.

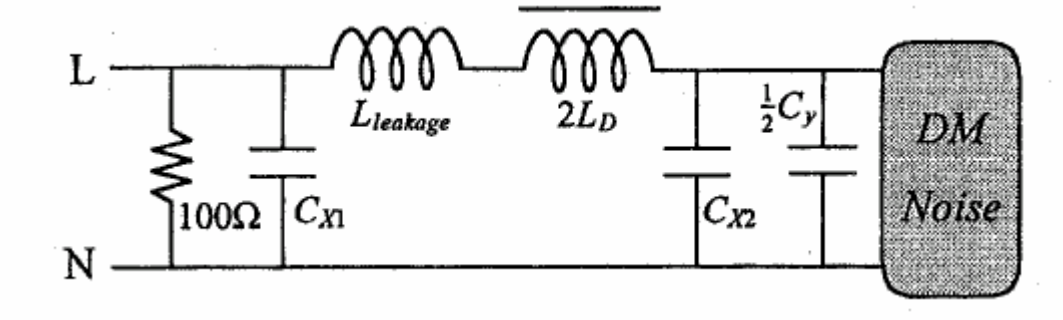


Fig. 2.21. DM noise equivalent circuit.

Chapter 3

Operation of MC33260 and Hardware Design

3.1 Introduction of MC33260

MC33260 is a power factor correction control IC of ON Semiconductor to meet the international standard requirements in electronic equipments. Fig. 3.1 shows the typical boost PFC converter using a CRM PFC controller MC33260. The CRM control scheme features a constant ON time and has a variable switching frequency. The MC33260 is optimized to just as well drive a free running as a synchronized discontinuous voltage control mode. It also provides features protections such as under-voltage, over-voltage protection, over-current limitation to make the PFC pre-regulator works in a safe condition. It is also able to safely face any uncontrolled direct charges of the output capacitor from the mains which occur when the output voltage is lower than the input voltage [28].

The MC33260 can also work in an innovative mode named “Follower Boost” that offers to significantly reduce the size of the inductor and power MOSFET and improving the efficiency [28] [29]. When MC33260 works in Follower mode, the output voltage is not forced to a constant value, it can be changed according to the AC input voltage. The gap between the output voltage and the AC input voltage becomes lower and causing the inductor and power MOSFET of PFC size reduction. Finally, this method brings a significant cost reduction.

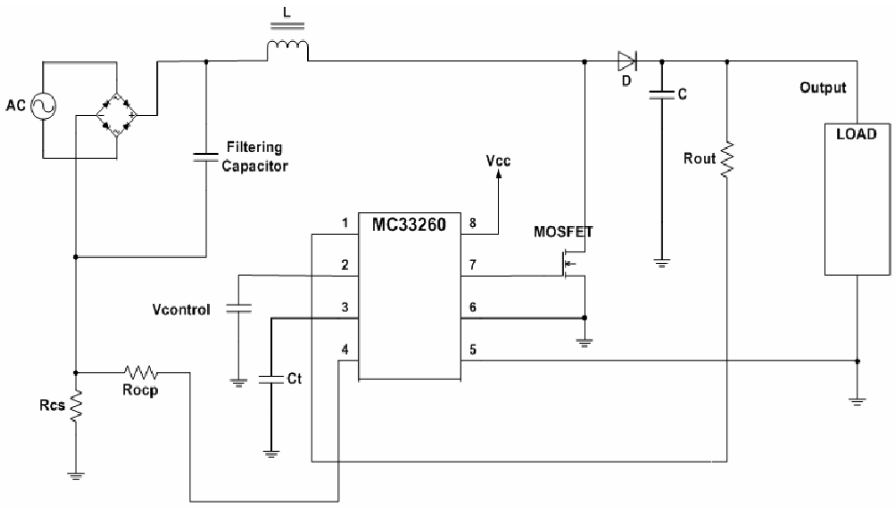


Fig. 3.1. CRM PFC circuit with MC33260.

Fig. 3.2 shows a typical schematic of a CRM PFC controller without multiplier [13]. The comparator generates a constant on-tome PWM signal by comparing the output of a programmable on-shot timer with a constant voltage reference. The zero current detector turn on the power MOSFET again when the inductor current drops to zero. The inductor current with a constant rising slope and is switched up and down between a sinusoidal reference in proportional to line voltage and a zero current.

A novel approach to the CRM PFC controller is available in an ON Semiconductor chip, MC33260. This chip provides the same function as the controllers described above. And it accomplishes this without the use of a multiplier.

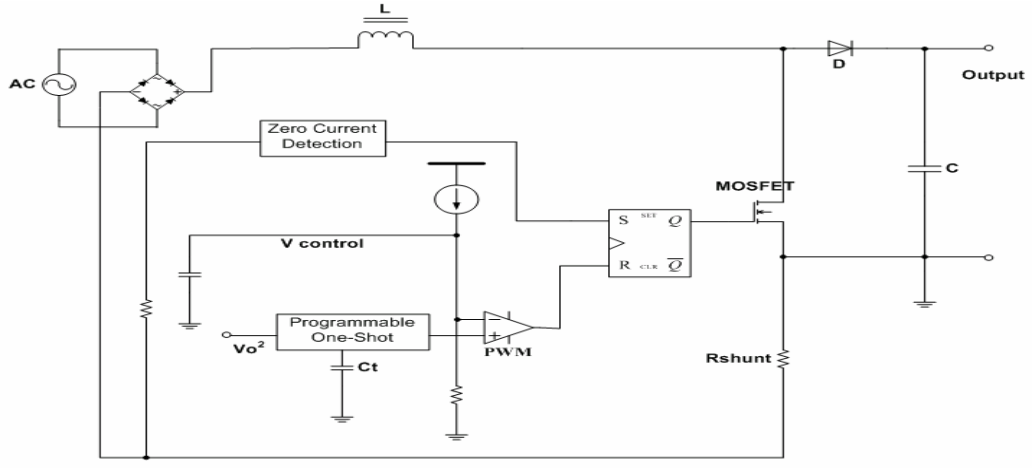


Fig. 3.2. Basic schematic for a CRM PFC controller without multiplier [5].

Fig. 3.3 is the waveform as explained in the previous section, the current waveform for a CRM controller ramps from zero to the reference signal and then slopes back down to zero. The reference signal is a scaled version of the rectified input voltage, and be referred to as k × V_{in}, where k is a scaling constant from the ac voltage divider and multiplier in a classic circuit. The turn-on time is equal to k × L.

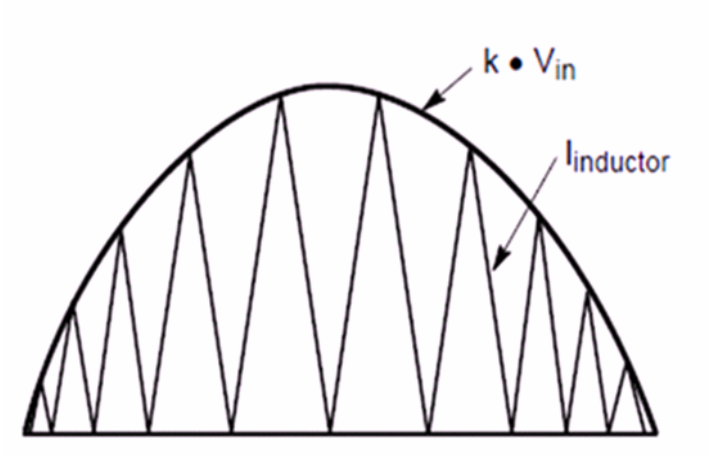


Fig. 3.3. Inductor current waveform [13].

Above equation shows that t_{on} is a constant with a given reference signal (k × V_{in}). T_{off} vary throughout the cycle, which is the cause of the variable frequency. The on time is constant for a given line and load condition is the basis for this control circuit.

3.2 Operation of MC33260

3.2.1 Oscillator Section

The oscillator consists of three states: 1.Charge State: The oscillator capacitor voltage grows up from ground until it exceeds $V_{control}$ (regulation block output voltage) linearly. At that moment, the PWM latch output is low and the oscillator discharge sequence is set. 2. Discharge State: The oscillator capacitor discharged down to its valley value (0 V) shortly. 3.Waiting State: The oscillator voltage is kept in a low until the PWM latch is set again during the end of the discharge sequence.

The charge current of oscillator is dependent on the feedback current where I_{charge} is the oscillator charge current, I_o is the feedback current from output, I_{ref} is the internal reference current and it is defended as 200 μA. The V_o is the output voltage, R_o is the feedback resistor, V_{pin1} is the pin 1 clamp voltage.

$$I_{\text{charge}} = 2 \cdot \frac{I^2{}_o}{I_{ref}} = \frac{2 \cdot (V_0 - V_{pin1})^2}{R_o{}^2 \cdot I_{ref}} \tag{3-1}$$

Pin 3 is the oscillator terminal includes an internal capacitance (C_{int}) that varies versus the pin 3 voltage. The average value is 15 pF.

3.2.2 *Regulation Section*

The feedback current is obtained by connecting a resistor between the output and pin 1. The value is given by following equation:

$$V_{pin1} = \frac{V_o - V_{pin1}}{R_o} \tag{3-2}$$

The feedback current is compared to the reference current and the regulation block outputs a signal following the future as Fig. 3.4

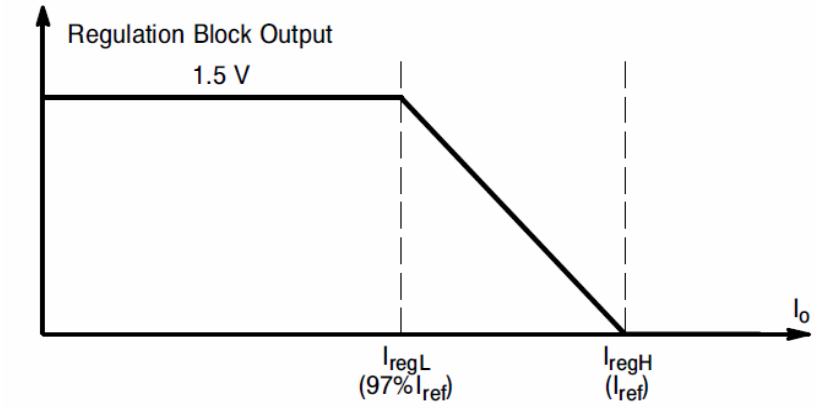


Fig. 3.4. Regulation characteristic [17].

3.2.3 *Current Sense and Zero current detection Section*

A ground reference resistor (R_{cs}) inserts in series with the input rectifier and input filtering capacitor to convert the inductor current into a negative voltage as following equation:

$$V_{cs} = -(R_{cs} \cdot I_L) \tag{3-3}$$

The I_L is the inductor current, R_{cs} is the current of sense resistor, V_{cs} is the voltage on R_{cs} and a negative voltage to the inductor current proportionally.

The zero current detection function controls the power MOSFET off as long as the inductor current does not reach zero during the off time. The pin 4 voltage compared to the threshold (-60 mV) to kept the gate drive signal in low state when V_{cs} is small than the threshold. The MOSFET turn on until the V_{cs} is smaller than 60 mv when the inductor current is close to zero. The pin 4 signal is used for the over-current limitation during on time, and it serves the zero current detection during the off time. The Fig. 3.4 shows the current sense block includes the main components, PWM Latch, R_{cs}, and comparator for the operation of zero current detection. The Fig. 3.5 shows the waveforms of power switch drive, inductor current, and pin 4 voltage where simulated with PSIM and the results are the same with the application notes.

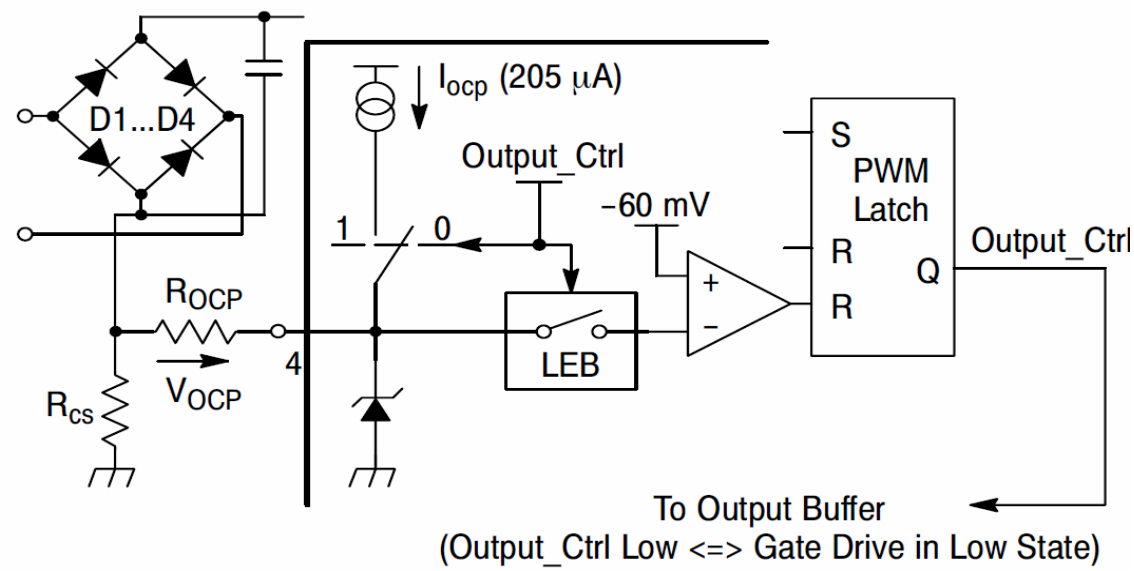


Fig. 3.5. Current sense block [17].

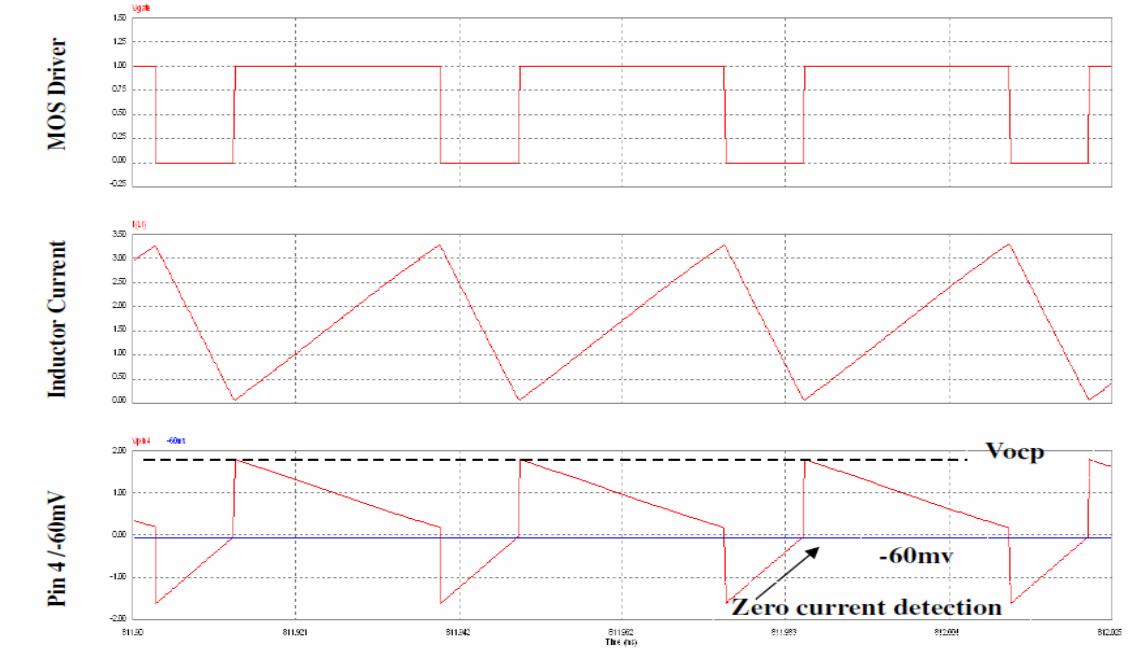


Fig. 3.6. Zero current sensing circuit.

3.3 CRM PFC HARDWARE SELECTION AND ANALYSIS

A basic design specification concerns the following for the hardware selection and analysis:

Design Variables	**Definition**
$fline := 60\,Hz$	Line Frequency
$Vinmin := 85V$	Minimum Input Voltage
$Vinmax := 265V$	Maximum Input Voltage
$Pout := 100W$	Maximum Output Power
$Vout := 400V$	Output Voltage
$fs := 25 \cdot 10^{3} Hz$	Minimum Switching Frequency
$t\_hold := 40 \cdot 10^{-3} s$	Output Hold up time
$tholdup := 16.7 \cdot 10^{-3} s$	Period of one Line Cycle
$Vdrop := 120V$	Amount of holdup voltage
$\eta := 0.92$	Efficiency
$Pin := \frac{Pout}{\eta}$	$Pin = 108.696\,W$

Based on above specifications, the input peak current can be calculated as following equation:

$$I_{in,pk} = \frac{\sqrt{2} \cdot P_{out}}{\eta \cdot V_{in,min}} \tag{3-4}$$

3.3.1 *Input Filtering Capacitors Design*

The high frequency input filtering capacitor works to filter the high frequency noise from switch off and diode on periods and keeping the voltage reference for the control circuit is sinusoid. However, a dc component will into the voltage reference signal dependent on the design of filtering capacitor. Fig. 3.7 shows the effect of a dc component where I_{Lpk} is the sum of I_k and I_p. I_k is a dc element, and $I_{psin\omega t}$ is a sinusoidal element of inductor current as shown in following equation:

$$I_{LPK} = I_p + I_k \tag{3-5}$$

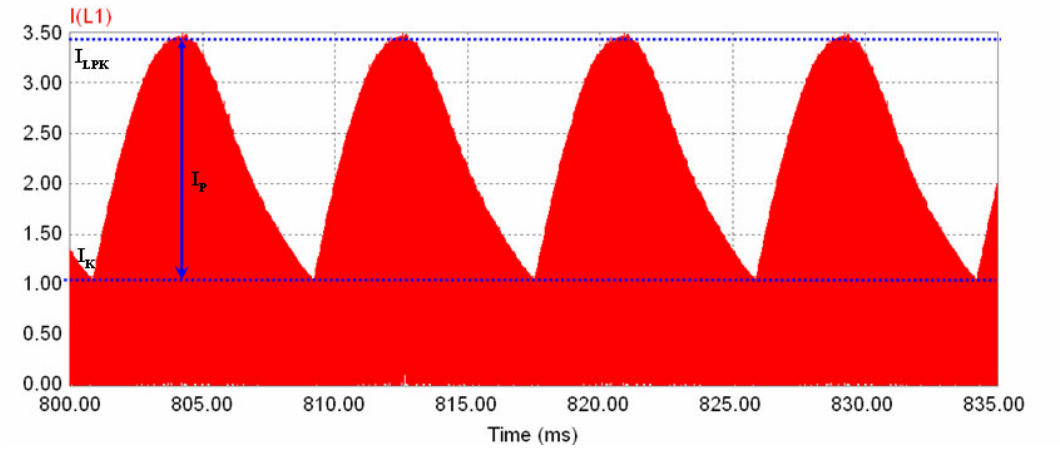


Fig. 3.7. Inductor current waveform after adding a filtering capacitor [5].

K factor is defined as following :

$$\mathrm{K} = \frac{I_p}{I_k} \tag{3-6}$$

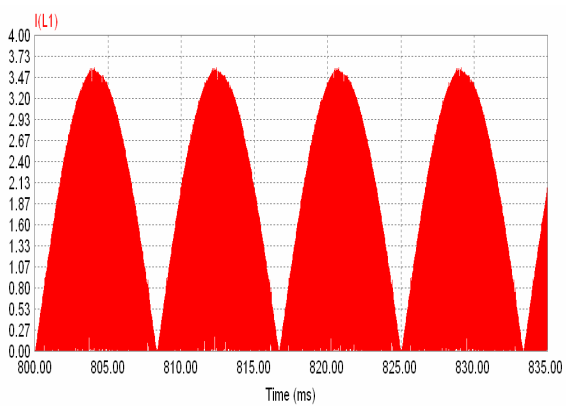


Fig. 3.8. Inductor current with a 0.5μF cap.

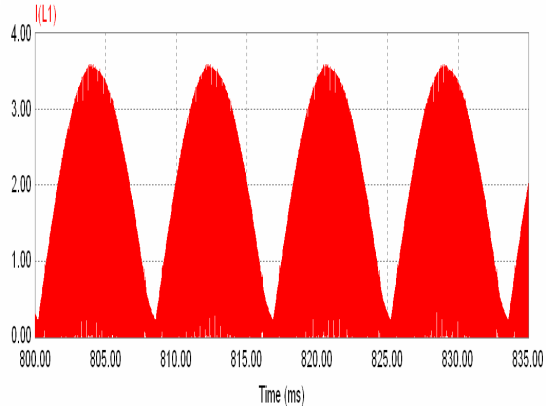


Fig. 3.9. Inductor current with a 10μF cap.

TABLE 3.1
COMPARISON OF DIFFERENT INPUT CAPACITORS

Input Capacitor	K	Power Factor (Calculated)	Power Factor (PSIM simulated)
0.5 μF	36.1	0.861	0.865
10 μF	13.48	0.853	0.851

The power factor value without an EMI filter can be calculated as equation (3-7) as a function of K [5] [30].

$$PF = \frac{\sqrt{2} \cdot I_{LPK} \cdot (\frac{\pi}{4} + K)}{4 \cdot (1+K) \cdot I_L} \tag{3-7}$$

Fig. 3.10 shows the power factor is close to 0.867 when the K value is approaches infinity.

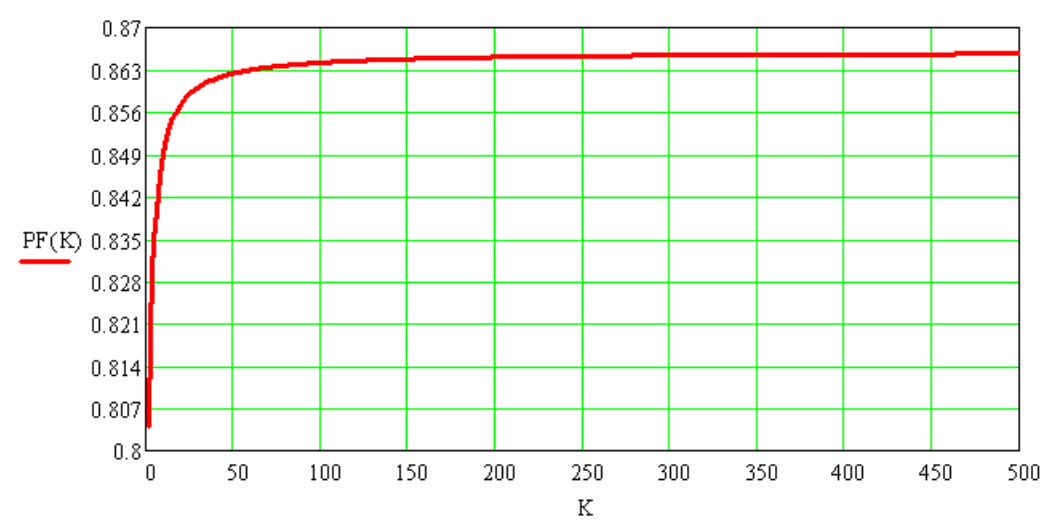


Fig. 3.10. Power factor as a function of K.

3.3.2 Inductor Selection

The value of inductor needs to be calculated based on four conditions, minimum AC input voltage, minimum switching frequency, output voltage and output power as shown in following equation:

$$L_p = \frac{\left(V_{out} - \sqrt{2}\cdot V_{in,min}\right)\cdot \eta \cdot {V_{in,min}}^2}{2\cdot f_s \cdot V_{out}\cdot P_{out}} \tag{3-8}$$

Based on the equation (3-8) and the specifications of design, the value of incuctor is calculated. Refer others discussion [31]-[33], a 0.93 mH inductor of EPCOS E 30/15/7 is selected. After the inductor value is found, the turn on time can be calculated as following equation:

$$T_{on} = 2\cdot L_p \cdot \frac{P_{in}}{{V_{in,min}}^2} \tag{3-9}$$

The turn off time is given by following equation: and drawing in Fig. 3.11.

$$T_{off} = 2\cdot\sqrt{2}\cdot L_p \cdot \frac{P_{in}}{V_{in,min}\cdot(V_{out} - \sqrt{2}\cdot V_{in,min}\cdot \sin(\omega t))}\cdot \sin(\omega t) \tag{3-10}$$

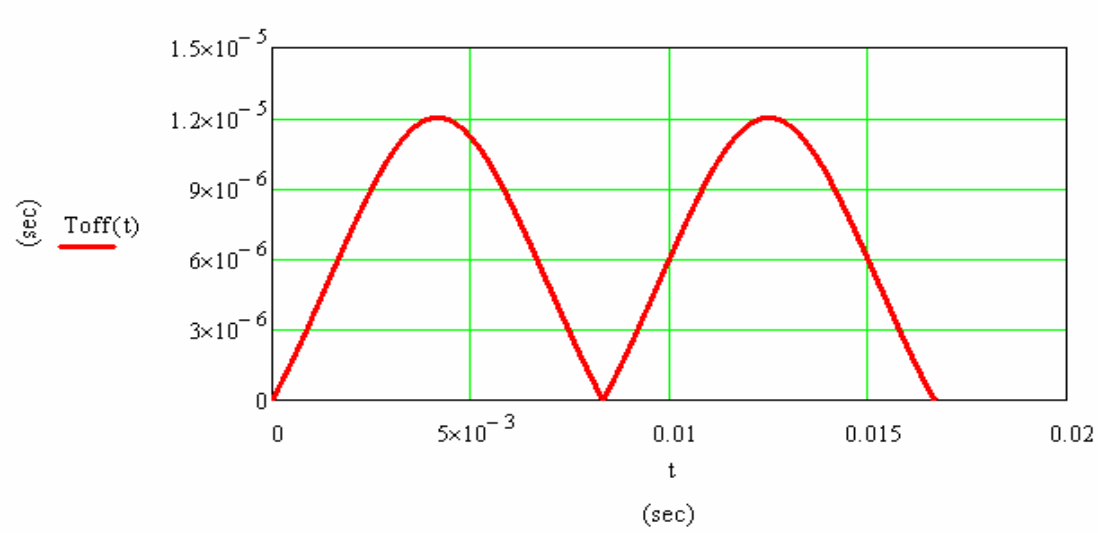


Fig. 3.11. Inductor turn off time.

The inductor current is given by following equation: the waveform is shown in Fig. 3.12.

$$I_{Lp}(t) = \frac{\left| \frac{V_{in,min}}{L_p} \cdot T_{on,max} \cdot \sin(\omega t) \right|}{\sqrt{2}} \tag{3-11}$$

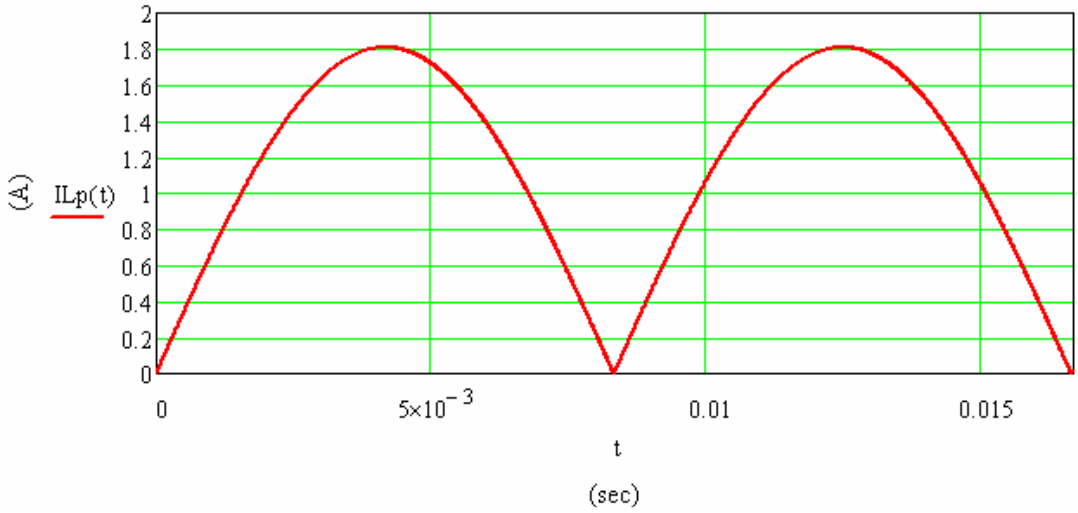


Fig. 3.12. Inductor current waveform.

3.3.3 MOSFET Selection

The selection of MOSFET is driven by the amount of power dissipation allowable. It is important to select the MOSFET as minimizes gate charge and capacitance and minimizes of power loss for switching and conduction. The turn on losses of MOSFET for Critical conduction mode is minimized due to the current is zero during switch turn on. It is more

important for the conduction losses reduction.

3.3.4 DIODE Selection

Normally, the reverse recovery current in the diode is important. However, the reverse recovery time and current is not important in the critical conduction mode due to the diode operate in zero current mode when diode off. The reverse voltage, forward current and switching speed becomes main selections.

3.3.5 Output Capacitors Selection

The value of output capacitor is important to be calculated to meet the specification of hold-up time as following equations:

$$C_{out} = \frac{(2 \cdot P_{out} \cdot T_{hold})}{(V_{out})^2 - (V_{out,min})^2} \tag{3-12}$$

Besides, the value of output capacitor the ESR of capacitor and maximum RMS ripple current are also important [34]. A simple method to reduce the ESR is parallel connecting of output capacitor. The RMS of output capacitor is given by following equation [35]:

$$I_{cout,rms} = \sqrt{\left[\frac{32 \cdot \sqrt{2} \cdot P_{in}^{2})}{9 \cdot \pi \cdot V_{in} \cdot V_{out}}\right] - \left(\frac{V_{out}}{R_{out}}\right)^2} \tag{3-13}$$

The output ripple voltage is given by following equation:

$$V_{out,p-p} = \frac{\eta \cdot P_{in}}{C_{out} \cdot \omega \cdot V_{out}} \tag{3-14}$$

And the output voltage is given by equation (3-15) and drawing the waveform in Fig. 3.13

$$V_{out}(t) = V_{out} - V_{out,p-p} \tag{3-15}$$

where $V_{out} = 400\text{V}$

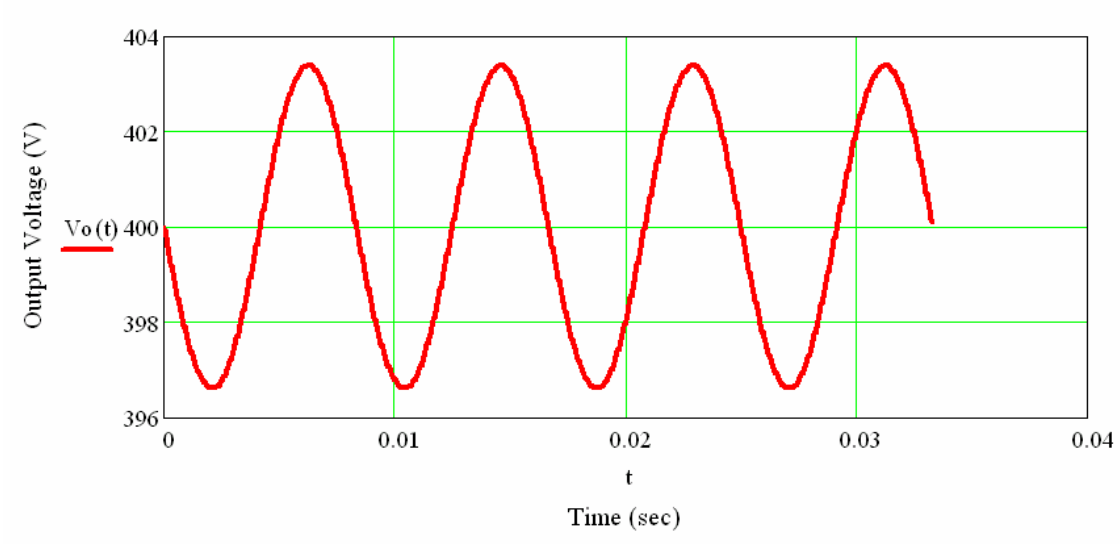


Fig. 3.13. Calculated output voltage with ripple voltage.

3.4 EMI FILTER DESIGN

The critical conduction mode PFC has main advantage such as zero-voltage-switching (ZVS) to improve the circuit efficiency. However, it also has two major disadvantages, higher input current ripple and wide switching-frequency range. The higher input current ripple increases the inductor size and cost both PFC converter and EMI filter. The wide switching-frequency range increases the switching losses and the complexity of DM EMI filter design. Because of the high inductor current ripple, The DM EMI filter for CRM PFC is more important than CCM PFC and only described in this analysis. In order to evaluate the EMI filters the spectrum of inductor current has to be derived. Many discussions about the EMI filter design need to review before the start of filter design [36]-[47].

3.4.1 Differential Mode EMI Filter Design

The requirement of a DM EMI filter is given as following list

1. Power Factor $\geqq 0.98$
2. Power losses $\leqq 2\%$ of DC output
3. Small size as possible

Four kinds of EMI filter are presented and simulated by PSIM in follows, for the waveforms of output voltage, input current, the phase angle between input current and input voltage, power factor and power losses.

Standard L-C Filter:

Referring the equation (2-16) and (2-17) the value of capacitor and inductor can be calculated. The inductor value is 0.125 mH and the capacitor is 8μF based on the selection of a 5 kHz cut-off frequency as the circuit in Fig. 3.14.

Fig. 3.15 shows the bode plots of attenuation and the gain near the cutoff frequency could be very large and causes the system instability, then amplify the noise at that frequency. It is necessary to analyze the transfer function of the filter to have a better understanding for the nature of the problem [48].

Fig. 3.16 shows the waveforms of input current with input voltage and the output voltage. It is easy to find out a phase shift between the input current and input voltage and resulting in the lower IDF value and power factor. The power factor is 0.975 be simulated by PSIM.

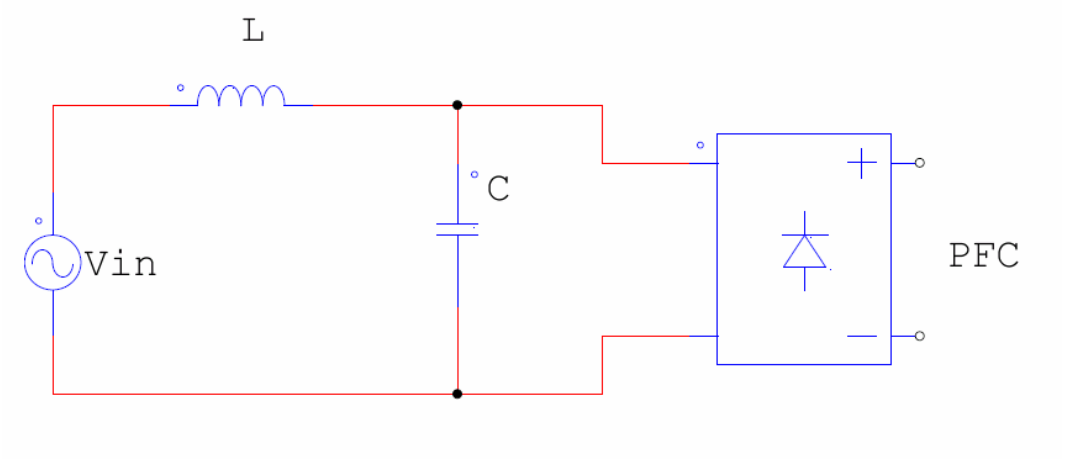


Fig. 3.14. Standard L-C filter circuit.

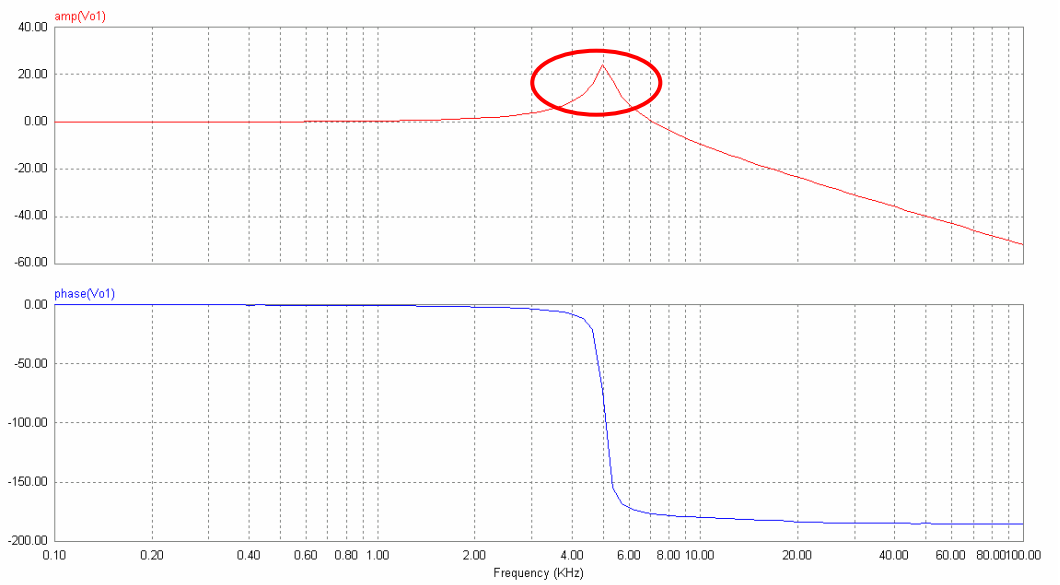


Fig. 3.15. Transfer function of L-C filter.

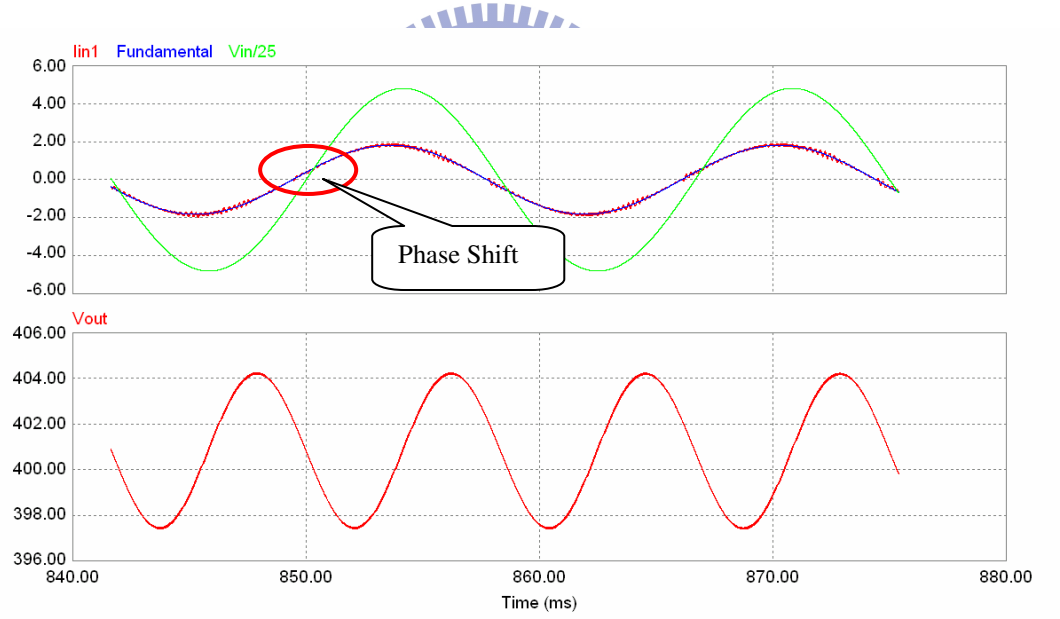


Fig. 3.16. Input current/voltage and output and PF value of L-C filter.

Using the FFT function of PSIM can see a little input current harmonics at the frequency range between minimum switching frequency, 25 kHz and its harmonics, 50 kHz as shows in Fig. 3.17.

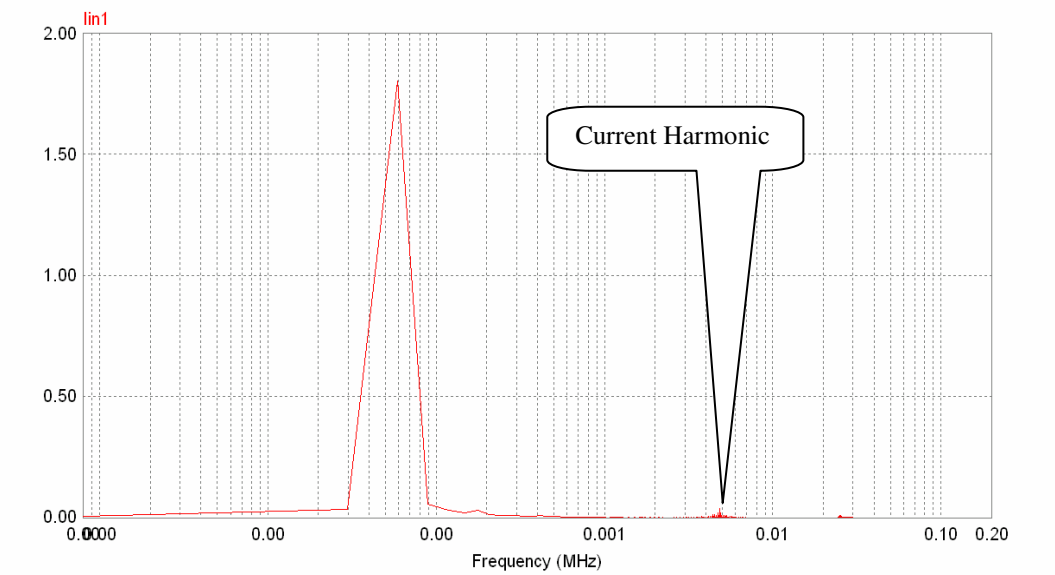


Fig. 3.17. Frequency spectrum of input current with the L-C filter.

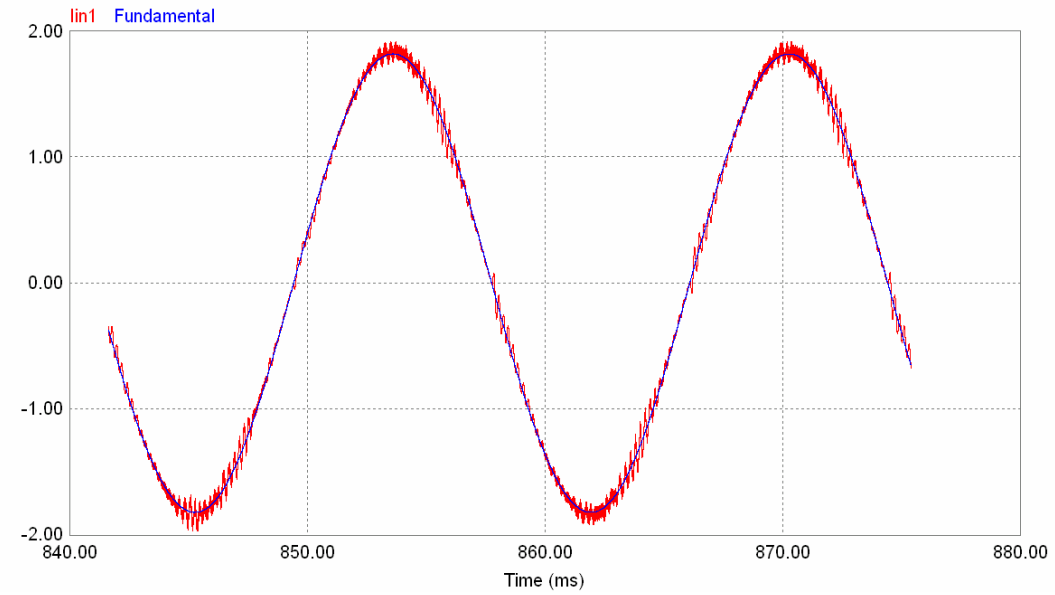


Fig. 3.18. Input current and fundamental current waveforms with L-C filter.

Parallel Damping Filter:

An improved of L-C filter is added a damping branch include a damping resistor with a capacitor into the L-C filter as shows in Fig. 3.19 [49]-[56] for the circuit of parallel damping filter. Fig. 3.20 shows the gain is reduced and under 3dB at cut-off frequency. Fig. 3.21 shows the phase shift between input current and input voltage is small than the standard L-C filter.

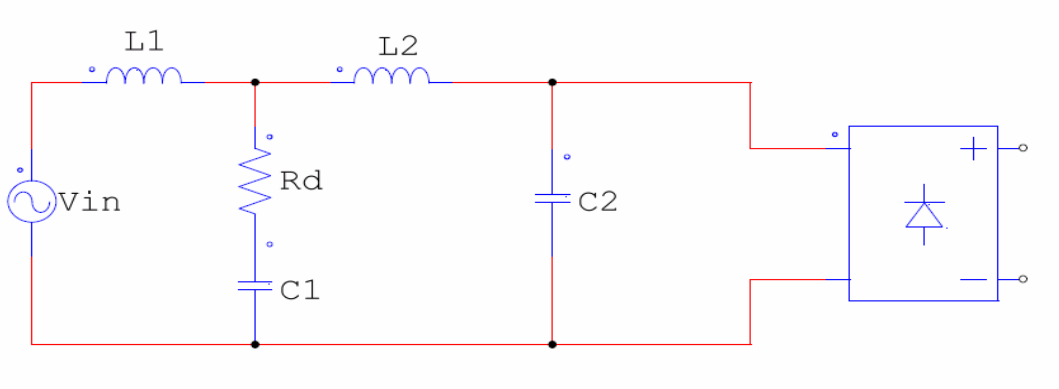


Fig. 3.19. Parallel damping filter circuit.

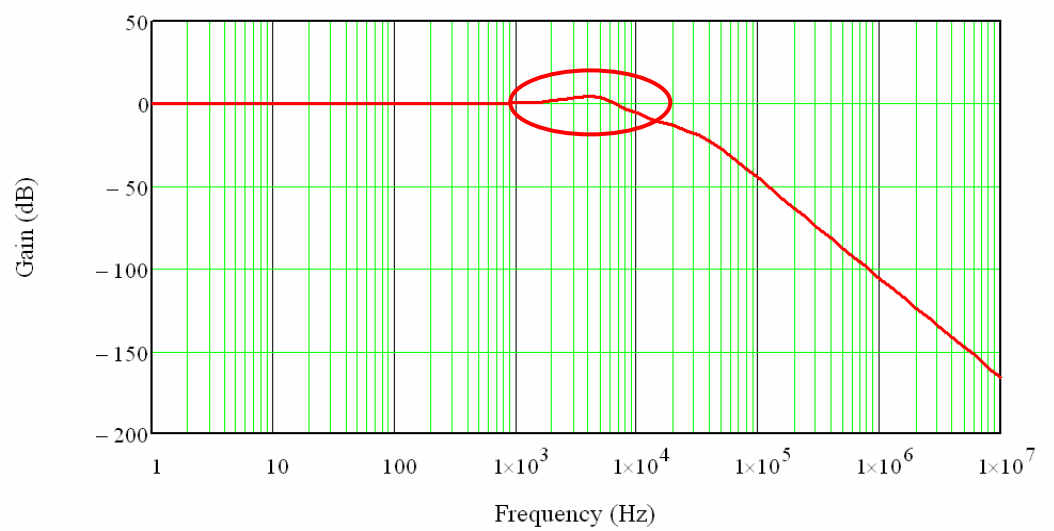


Fig. 3.20. Transfer function of damping filter.

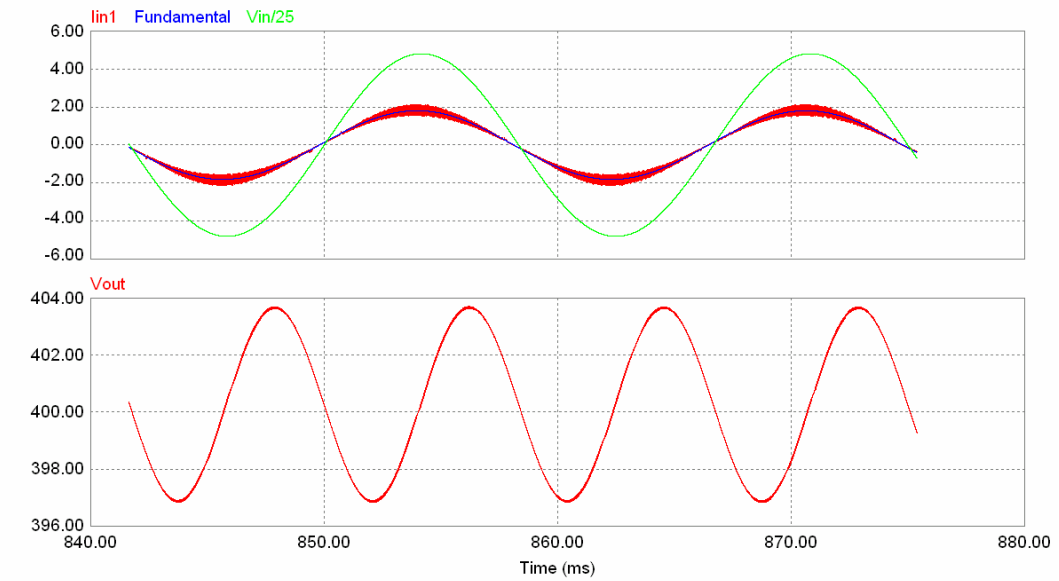


Fig. 3.21. Input current/voltage and output voltage waveforms with damping filter.

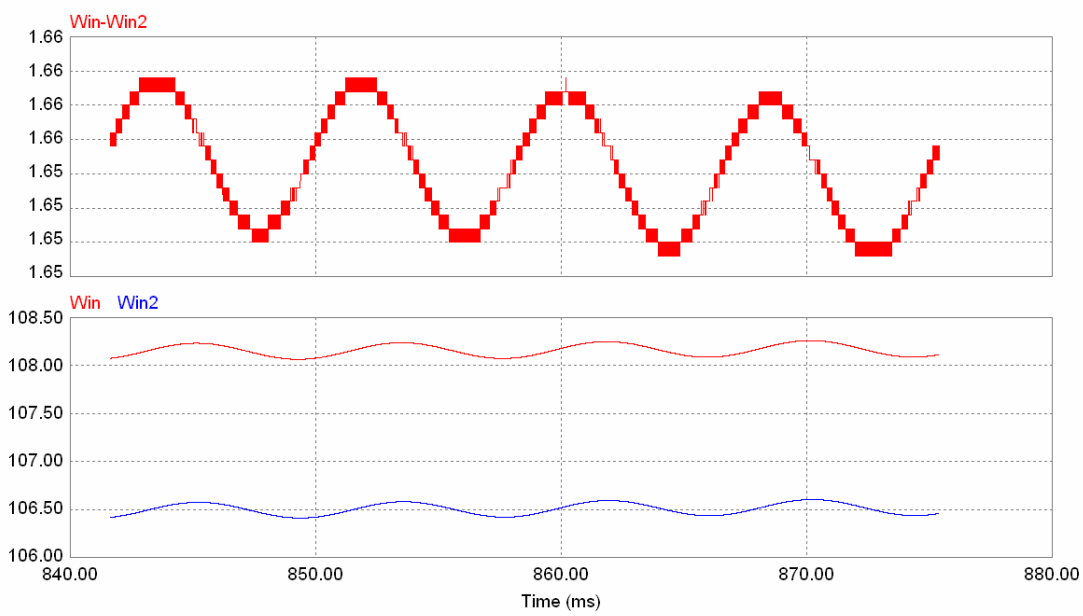


Fig. 3.22. Power losses of damping filter.

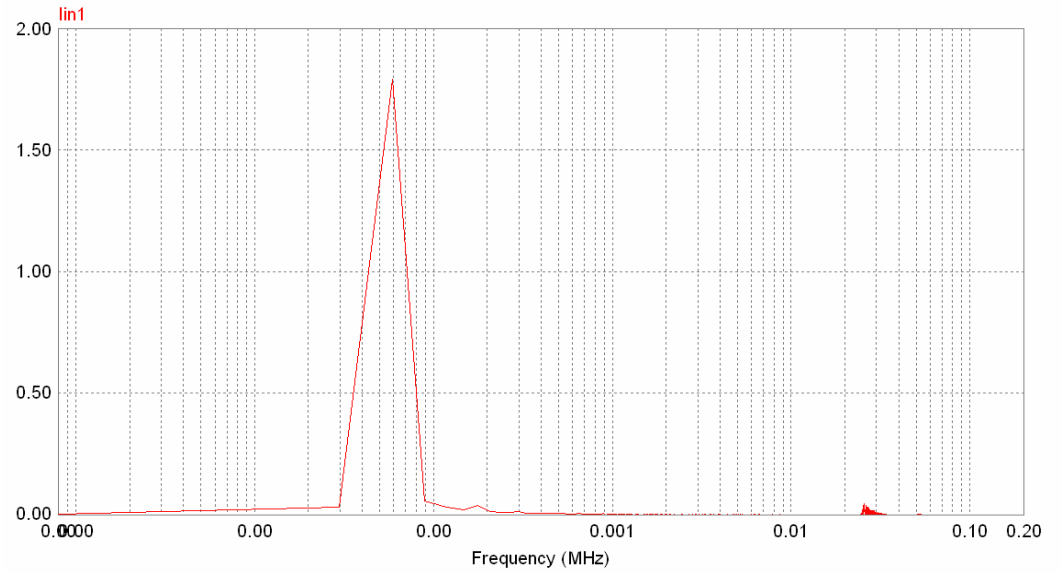


Fig. 3.23. Frequency spectrum of input current with damping filter.

The major disadvantage of damping filter is high power losses compare to others. The power losses of damping filter is around 1.65W and 1.65% of system power level. The power losses is caused by the damping resistor, Rd. as shows in Fig. 3.22

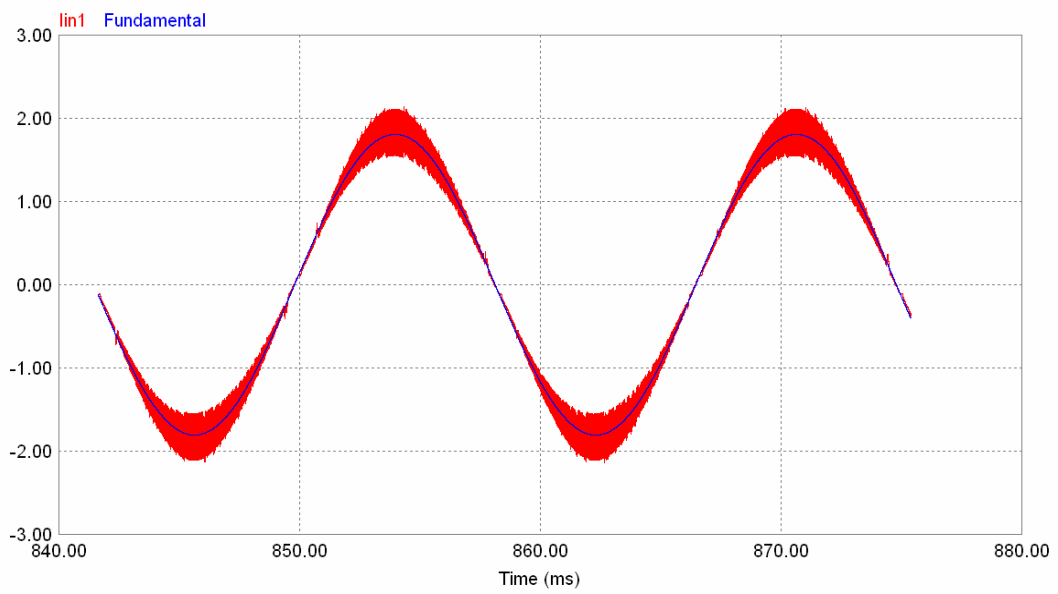


Fig. 3.24. Input current and fundamental current waveforms with damping filter.

Standard Differential Mode EMI Filter:

A standard differential mode EMI filter is shown is Fig. 3.25. It consists of two inductors and two x capacitors. The filter is designed to supply the average input current to the PFC pre-regulator despite the changes in the boost inductor current and the boost hold up capacitor. The values of two inductors are the same and can be calculated as equation (3-16) [2]. The value of two x capacitors are the same and can be found based on the values of inductors, minimum switching frequency, 25 kHz and hold up as shown in equation (3-17).

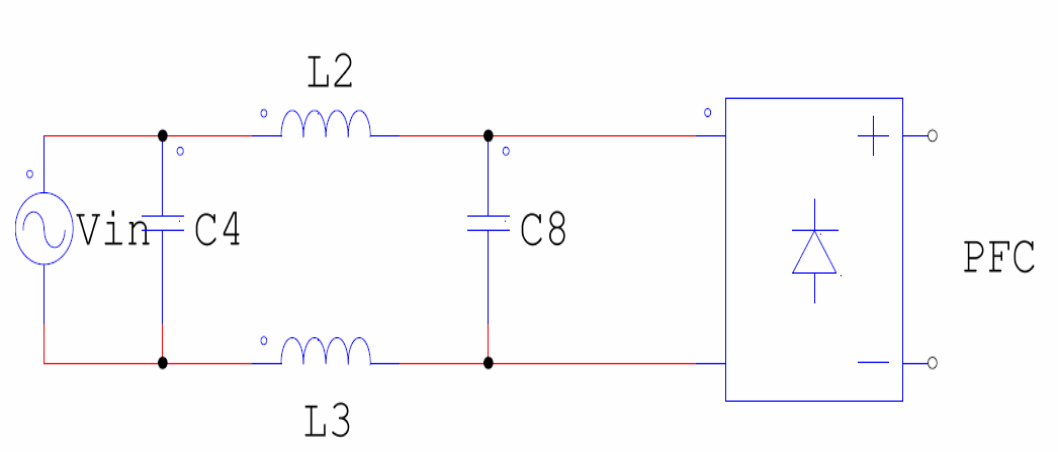


Fig. 3.25. Standard differential mode EMI filter circuit.

$$L_2 = \frac{(V_{in,min} \cdot \sqrt{2} - V_{drop}) \cdot T_{on}}{\left(\frac{P_{out} \cdot \sqrt{2}}{\eta \cdot V_{in,min}}\right)} \tag{3-16}$$

$$C_4 = \frac{1}{(2\pi \cdot f_s)^2 \cdot L_2} \tag{3-17}$$

The simulated result by PSIM is shown in Fig. 3.26, and the phase shift between input current and input voltage and the power losses are the smallest in four EMI filters. It means the IDF value and efficiency are high.

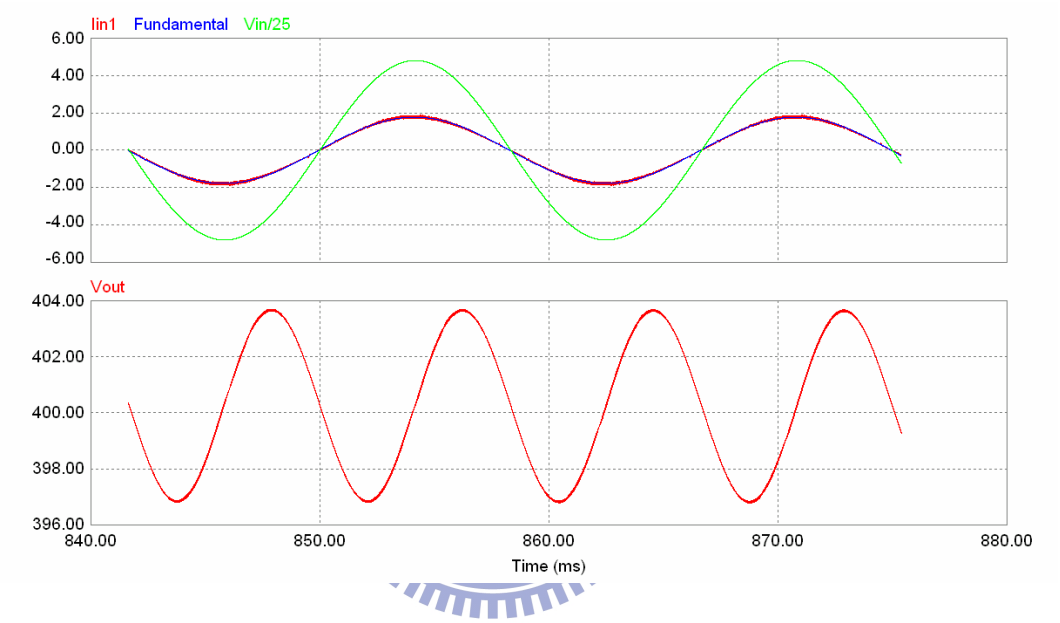


Fig. 3.26. Input current/voltage and output voltage waveforms with STD. DM filter.

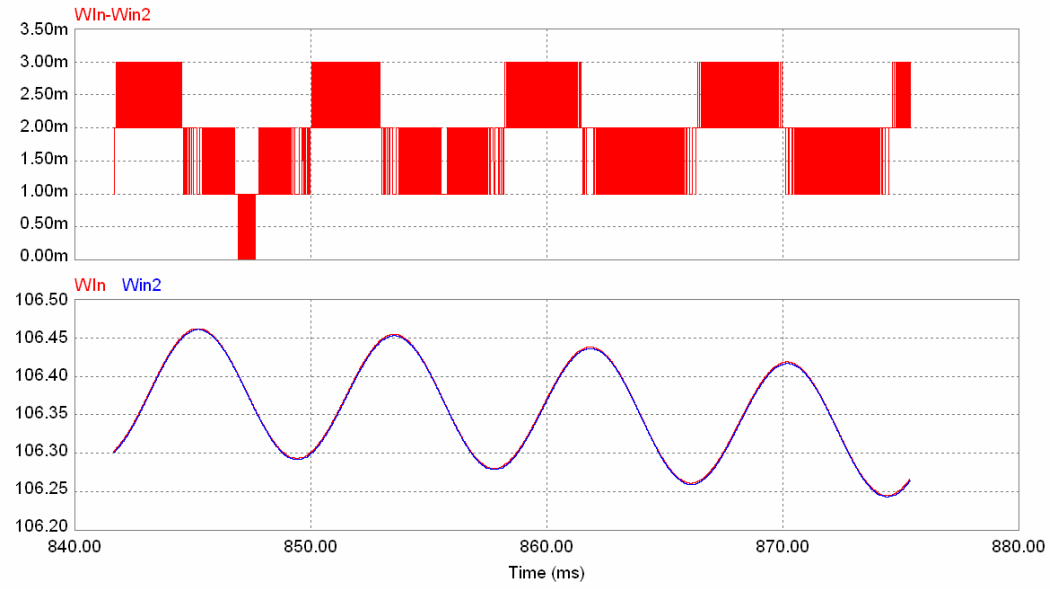


Fig. 3.27. Power losses of STD DM filter.

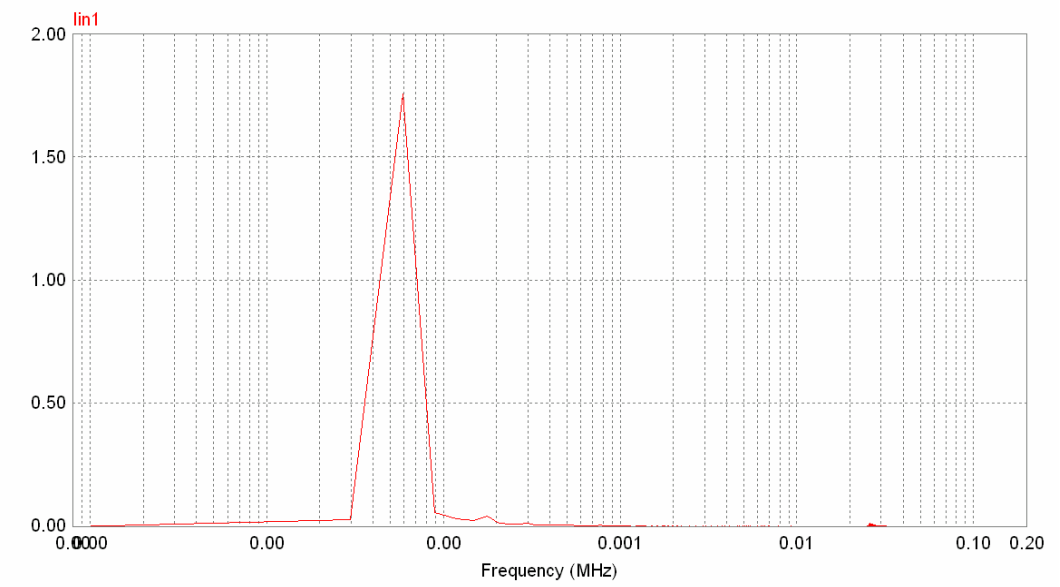


Fig. 3.28. Frequency spectrum of input current with STD DM filter.

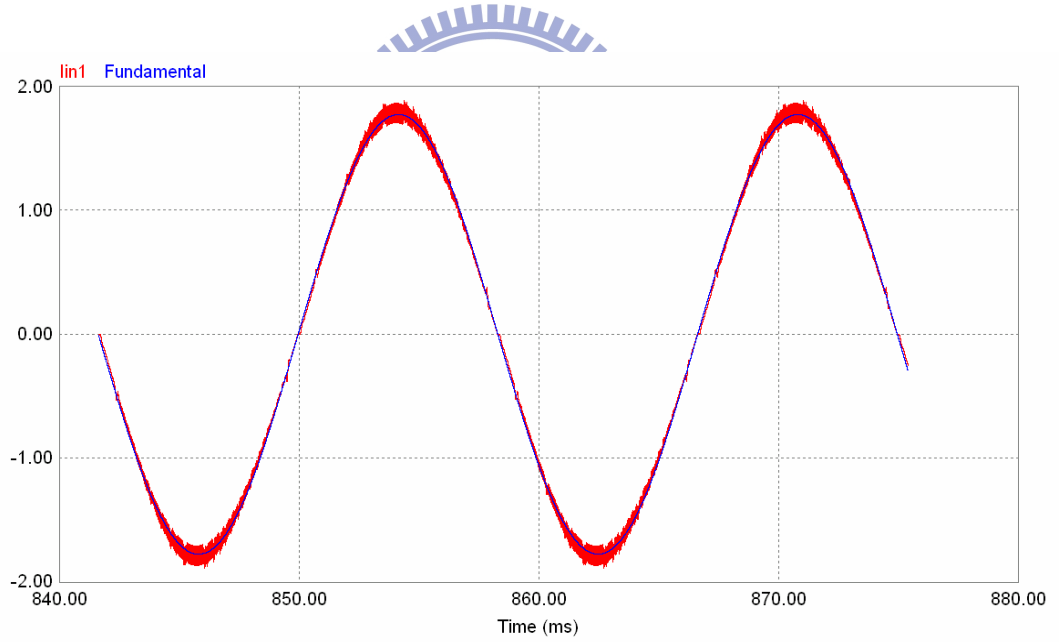


Fig. 3.29 Input current and fundamental current waveforms with STD DM filter.

Investigated two-stage DM EMI Filter:

The least EMI filter is an investigated two-stage differential mode EMI filter [57]-[58]. Fig. 3.31 shows a little phase shift between input current and input voltage.

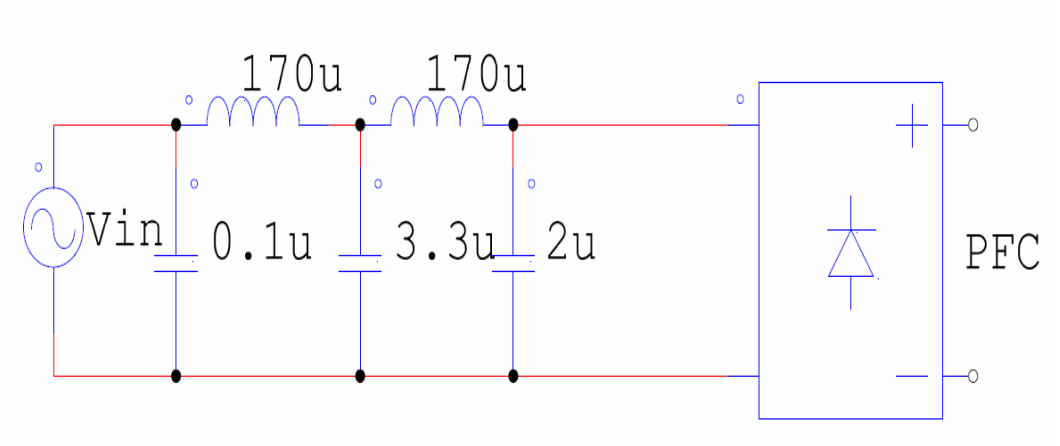


Fig. 3.30. Investigated two-stage DM EMI filter circuit.

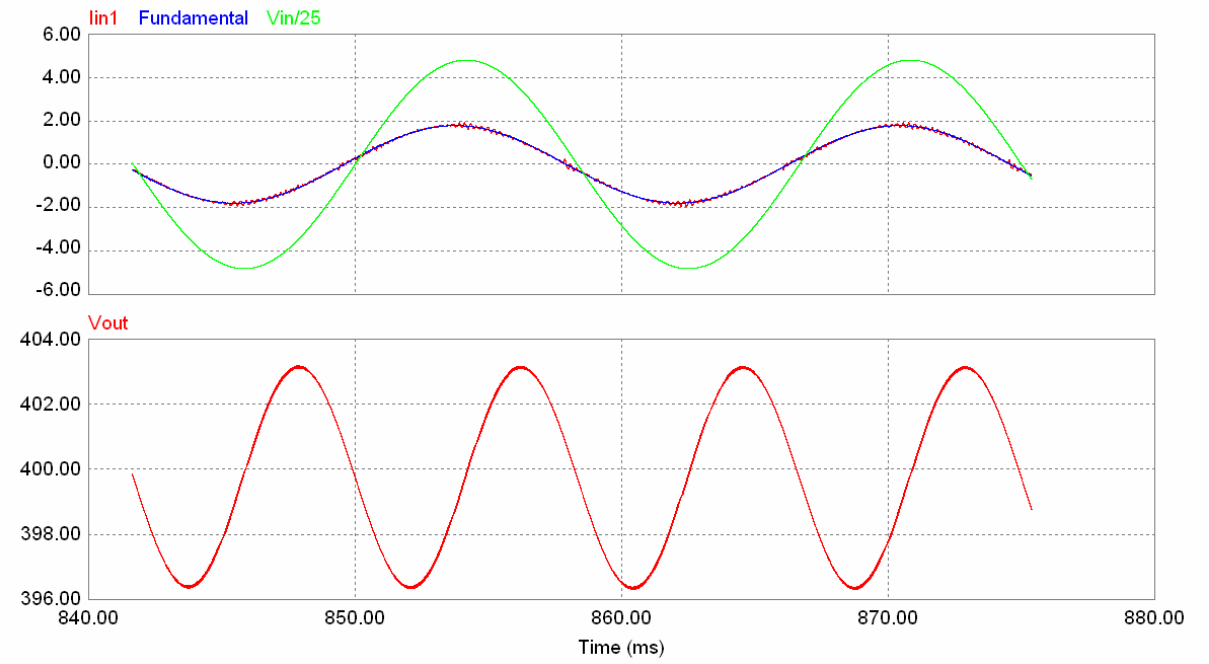


Fig. 3.31. Input and output waveforms with investigated two-stage DM EMI filter.

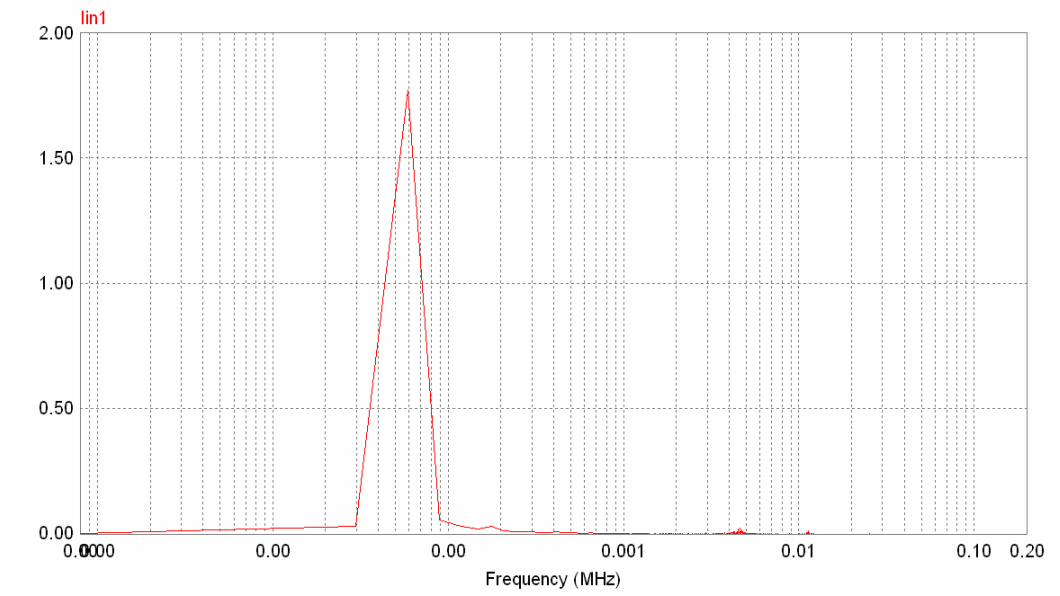


Fig. 3.32. Frequency spectrums of input current with investigated two-stage DM filter.

Fig. 3.33 shows the waveform of input current is close to the fundamental current waveform, only a few oscillations at the peak and bottom.

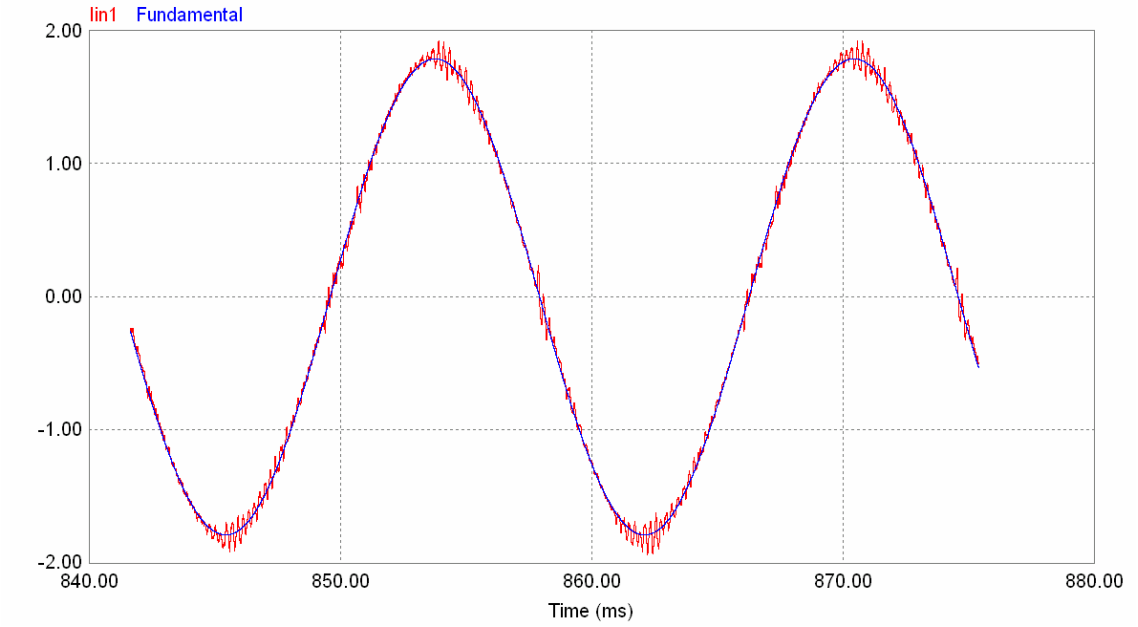


Fig. 3.33 Input current and fundamental current waveforms with investigated two-stage DM filter.

3.4.2 EMI Filter Design Summary

A review for each EMI filter is presented in Table 3.2. The standard differential mode EMI filter and the investigated two-stage EM EMI filter have better performance in power losses, and power factor. The investigated two-stage DM EMI filter has more advantage for smaller size than the standard DM EMI filter.

TABLE 3.2

COMPARISON OF FOUR EMI FILTER

Item/Filter	Standard L-C	Damping	DM-EMI	Investigated Two-Stage DM-EMI
Components	L ×1 C ×1	L ×2 C ×2 Rd×1	L × 2 C × 2	L × 2 C × 2
Maximum Inductor Value	0.125mH	0.24mH	0.545mH	0.17mH
Size	Small	Middle	large	Small
Power Losses (W) (inductor , Capacitor are ideal model)	N/A	1.65W	N/A	N/A
Power Factor	0.975	0.992	0.995	0.996
THD	0.42%	0.35%	0.2%	0.18%
Complexity	Low	Middle	Middle	High

3.5 POWER LOSSES ANALYSIS

In the following analysis, the MathCAD program is designed to calculate not only basic parameters as output voltage, ripple and input current, inductor current but also the power losses for each component and showing the result by drawing to analyze the overall characteristic of losses and switching frequency vs. different load. The similar method can be analyze the input voltage, current, turn-on time, turn –off time and switching frequency vs. input voltage phase. The simulation of PSIM is shown in second step to verify the output voltage, ripple, and input current with harmonics analysis. A simple experimental result was shows at least to realize the design of 100 W critical conduction mode PFC circuit.

3.5.1 Rectifier Power Losses

Typically the diodes of the rectifier bridge have conduction losses and reverse recovery losses. The major source of the loss is the conduction loss due to semiconductor device forward voltage drops around 0.7 V. Therefore, only conduction loss is considered in this analysis. The conduction losses of bridge diode are given in following equation [59]:

$$P_{Bridge\_loss} = \frac{4 \cdot \sqrt{2} \cdot P_{out} \cdot V_{F\_rectifier}}{\eta \cdot \pi \cdot V_{in,min}} \tag{3-18}$$

where $V_{F\_rectifier}$ is the forward voltage drop of the diodes

$V_{in,min}$ is the RMS input voltage

η is the efficiency of the CRM PFC converter

P_{out} is the output power of the converter.

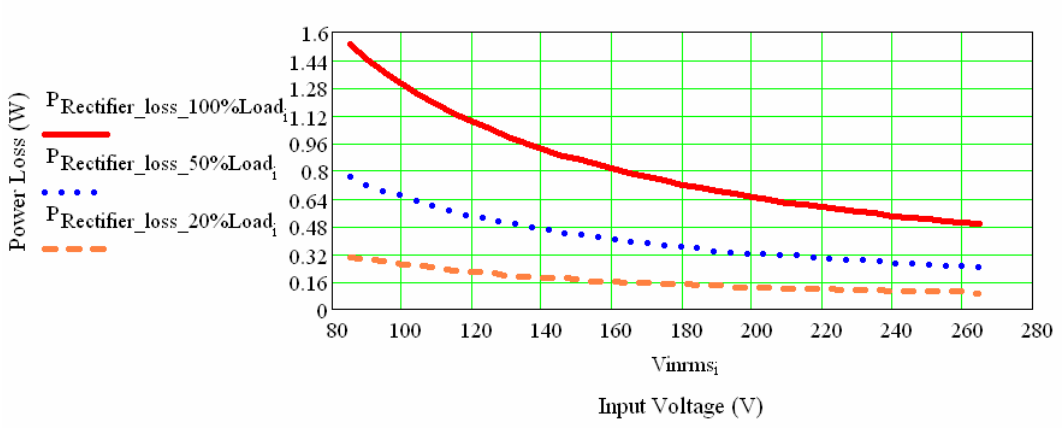


Fig. 3.34. The power losses of rectifier vs. input voltage.

3.5.2 MOSFET Power Losses

The switching losses of MOSFET are difficult to determine and calculate in critical conduction mode. Because of the type of MOSFET, gate charge, and variable switching frequency affect the analysis. Here, we will discuss four kind of main power losses of MOSFET [35], [59]-[61].

1. **Power losses of Gate:**

The following equation is shows the high gate charge value increases high power losses. High switching frequency also increases high power losses.

$$P_{gate\_loss} = Q_{gate} \cdot V_{gate} \cdot f_s \tag{3-19}$$

where Q_{gate} is the gate charge

V_{gate} is the voltage applied between the gate and the source to turn on the MOSFET

f_s is the switching frequency

2. C_{oss} Power losses:

$$P_{coss\_loss} = \frac{1}{2} \cdot C_{oss} \cdot V_{out} \cdot f_s \tag{3-20}$$

where C_{oss} is the value of output capacitor

Fig. 3.35 shown the power losses of gate and C_{oss} are fixed when input voltage change.

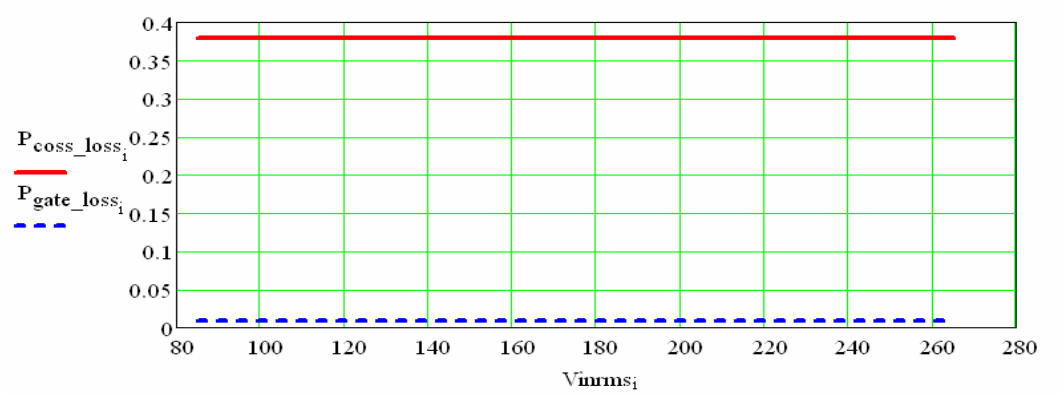


Fig. 3.35. The power losses of gate .and Coss vs. input voltage.

Fig. 3.36 and Fig. 3.37 shows losses of C_{oss} and *gate* are direct proportion as switching frequency.

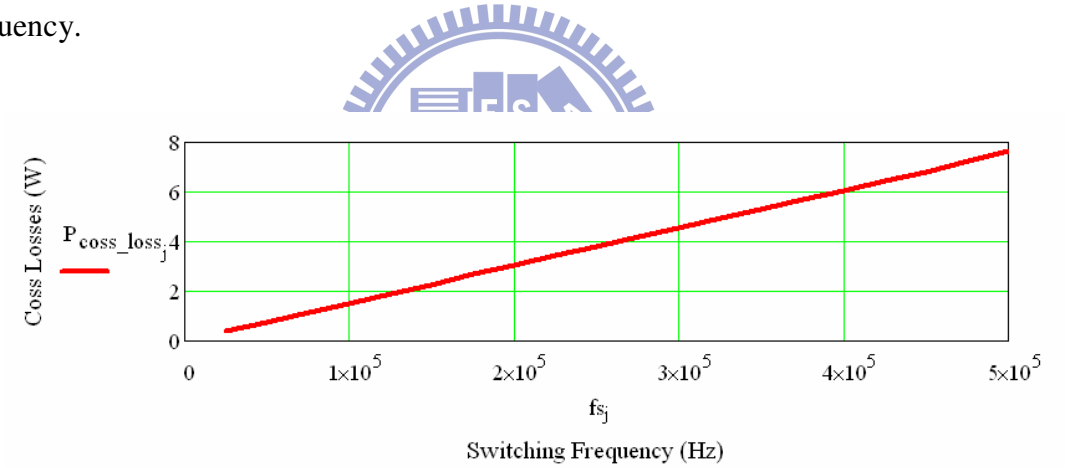


Fig. 3.36. The power losses of C_{oss} vs. switching frequency.

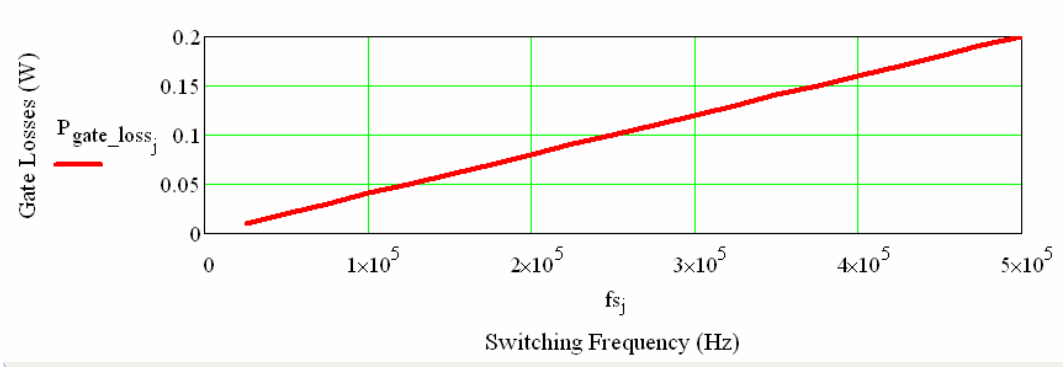


Fig. 3.37. The power losses of gate vs. switching frequency.

3. Conduction Losses:

The conduction loss is major loss in the MOSFET. The value of R_{dcon} in the MOSFET affects the loss so much. It is important to select a MOSFET with low R_{dcon} value.

$$P_{cond\_loss} = R_{dcon} \cdot \left(I_{MOSFET,rms}\right)^2 \tag{3-21}$$

where I_{rms_FET} is the rms value of the current flows through the MOSFET

R_{dcon} is the on-state resistance between drain and source

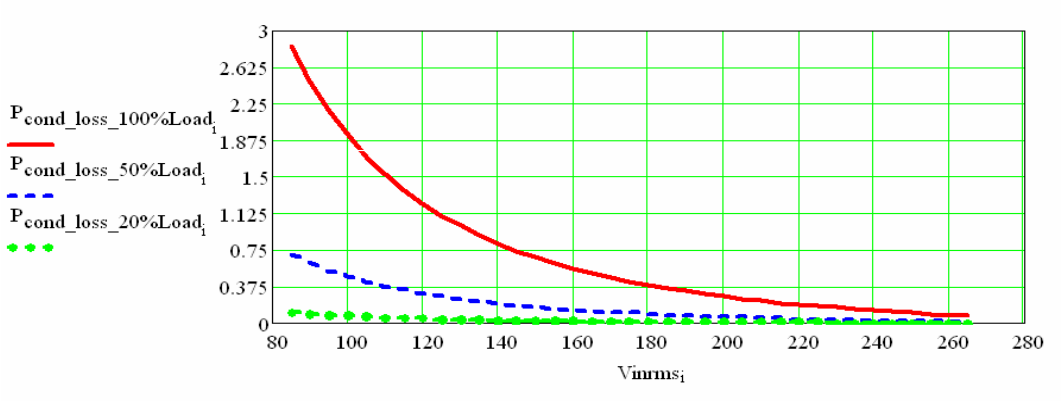


Fig. 3.38. The conduction losses of MOSFET vs. input voltage.

4. Turn on Losses:

$$P_{FET\_trloss} = \frac{1}{2} \cdot V_{out} \cdot I_{L,rms} \cdot t_r \cdot f_s \tag{3-22}$$

where Q_{gate} is the gate charge

V_{gate} is the voltage applied between the gate and the source to turn on the MOSFET

f_s is the switching frequency

t_r is the rise time

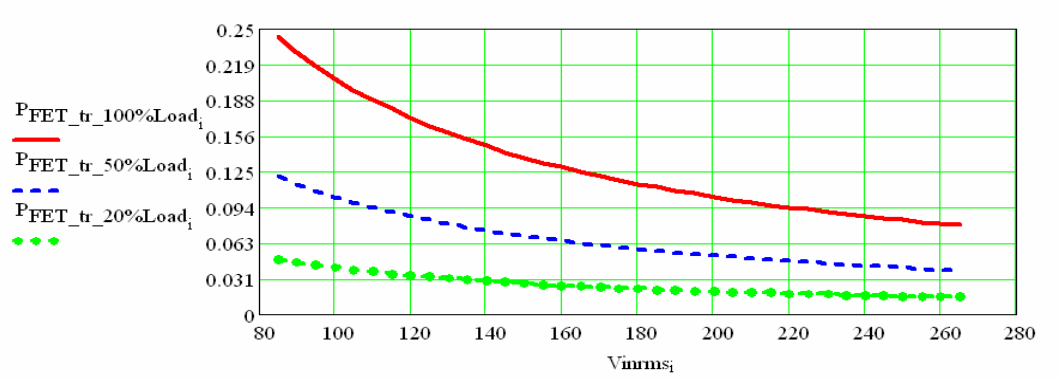


Fig. 3.39. The turn on losses of MOSFET vs. input voltage.

The total power losses of MOSFET are the sum of (3-19) - (3-22), and the major losses of MOSFET is conduction loss as the function of the RMS value of MOSFET and turn-on resistor.

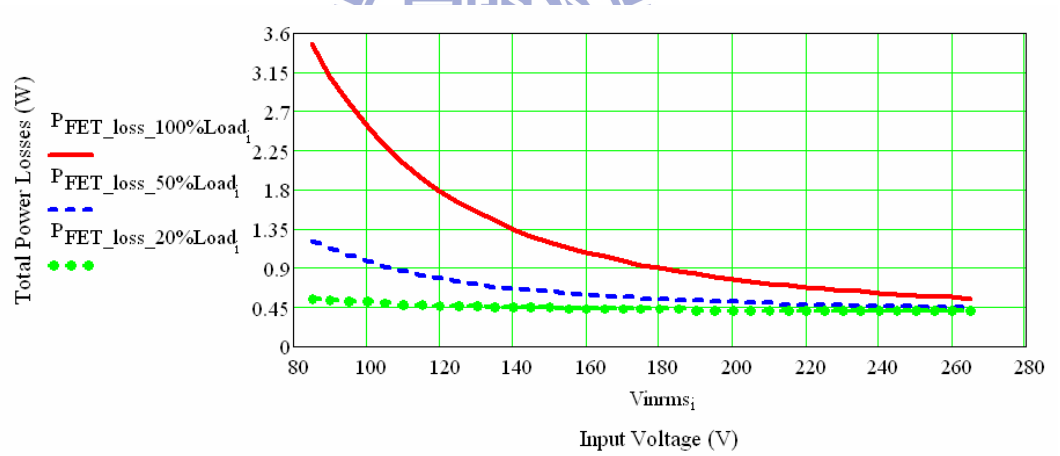


Fig. 3.40. The total power losses of MOSFET vs. input voltage.

3.5.3 Diode Power Losses

Two major power losses of diode are conduction losses as shown in equation (3-24)

$$ID_{rms} = \frac{4}{3} \cdot \frac{\sqrt{2 \cdot \sqrt{2}}}{\pi} \cdot \frac{P_{in}}{\sqrt{V_{in,min} \cdot \cdot V_{out}}} \tag{3-23}$$

$$P_{Diode\_loss} = VF_{\_diode} \cdot ID_{rms} \tag{3-24}$$

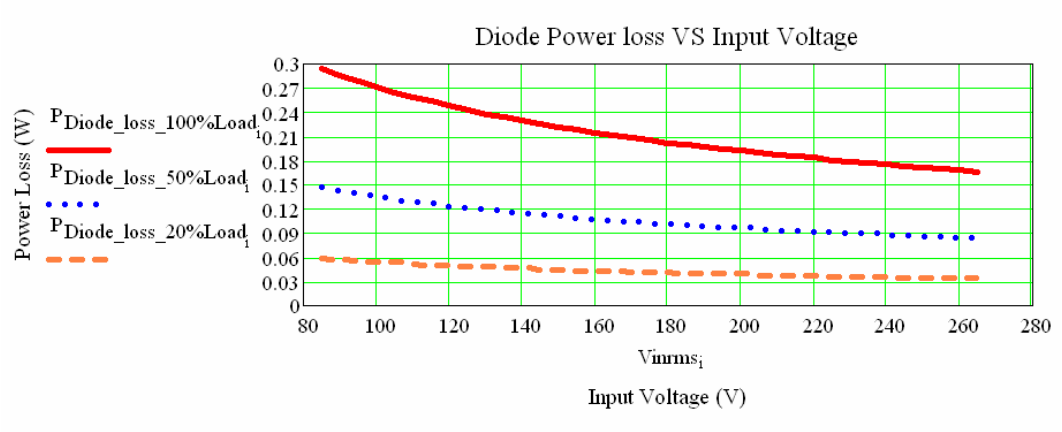


Fig. 3.41. The power losses of diode vs. input voltage.

3.5.4 *Sensor Circuit Power Losses*

The current sense resistor derives the whole coil current. The losses are given by following equation [35]:

$$P_{RS\_loss} = R_{CS} \cdot (I_{Lrms})^2 = \frac{4}{3} \cdot R_{CS} \cdot \left(\frac{P_{in}}{V_{in}} \right)^2 \quad (3\text{-}25)$$

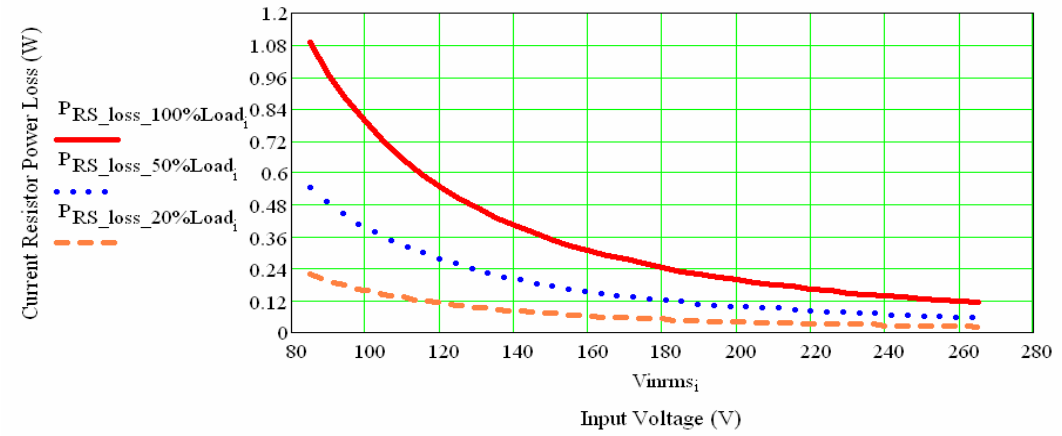


Fig. 3.42. The power losses of sensor circuit vs. input voltage.

3.5.5 *Output Capacitor Power Losses*

The loss in the capacitor occurs due to the power loss contributed by the equivalent series resistance (ESR) of the capacitor. It is given by following equation [35].

$$P_{cout\_loss} = I_{cout,rms}{}^{2} \cdot R_{cout,esr} \tag{4-9}$$

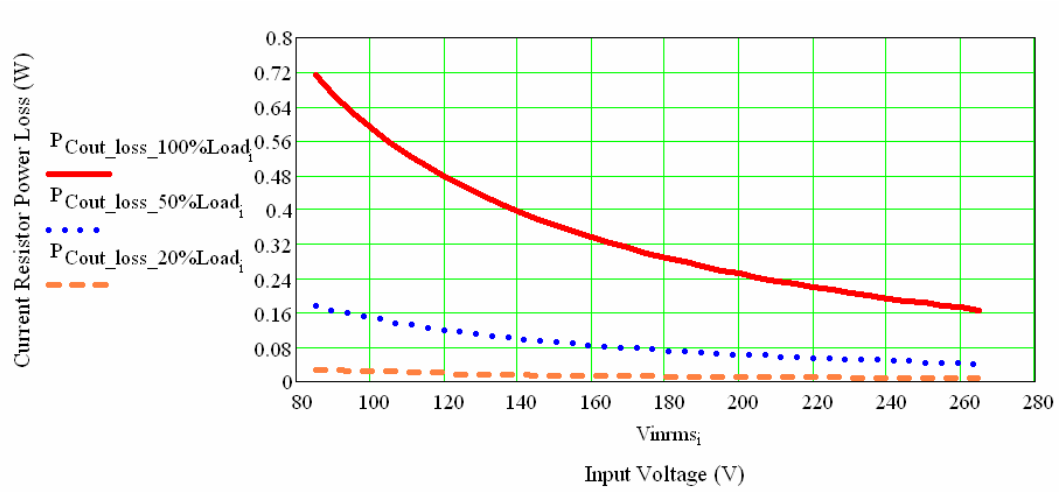


Fig. 3.43. The power losses of output capacitor vs. input voltage.

3.5.6 *Inductor Losses*

The inductor loss comprises the core loss and copper loss. Here we select E30/15/7, N67 material from EPCOS, and the power losses are 0.82W at 25 kHz [59].

3.5.7 *Summary*

Finally, the power losses for overall CRM PFC circuit are shown in Fig. 3.44 and indicate the worst-case was happened at lowest line voltage with full load condition. All selections for main component likes inductor, MOSFET, Diode and output capacitor should be considered with the condition.

The efficiency analysis is shown in Fig. 3.45, it indicate the worst-case was happened at lowest line voltage with light loading.

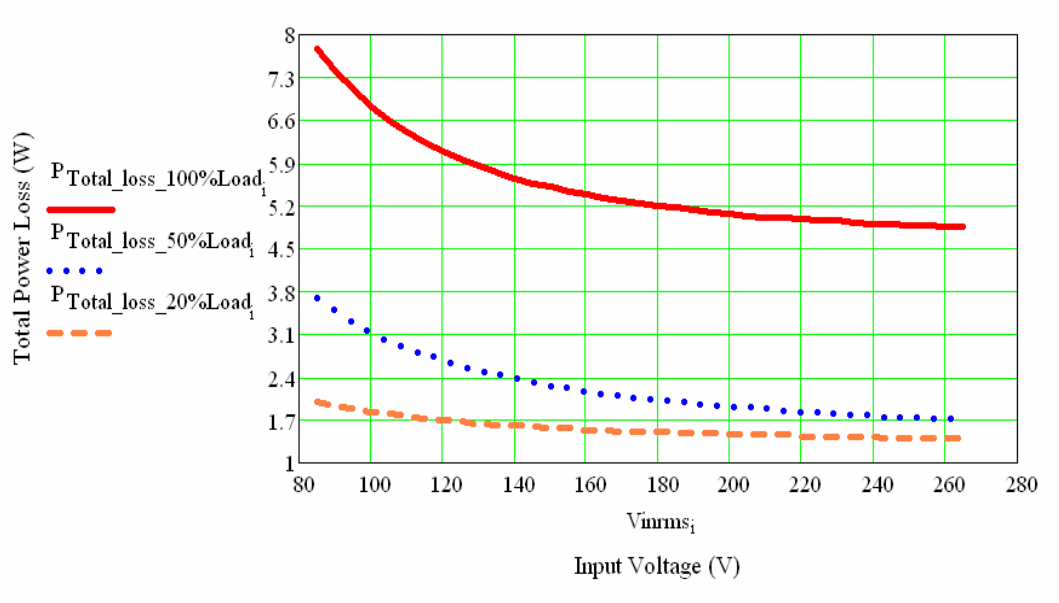


Fig. 3.44. The total power losses of PFC circuit vs. input voltage.

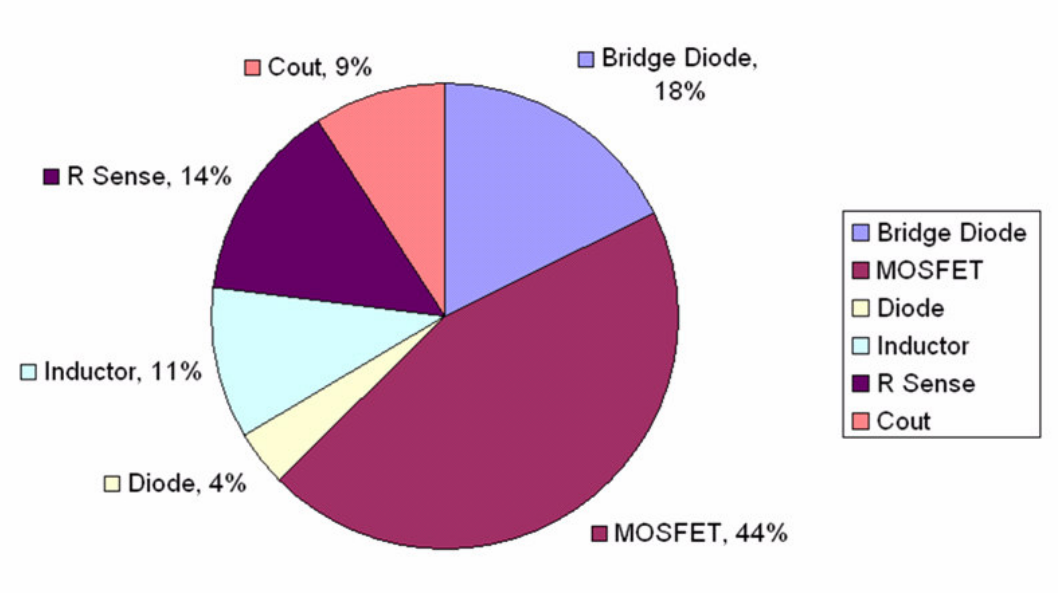


Fig. 3.45. The total power losses Pi Chart.

The operation switching frequency is shown in Fig. 3.46, it indicate the maximum frequency close to 300 kHz at line voltage 190 Vac with light load condition. And the minimum frequency closes to 21 kHz at the maximum line voltage with full load condition.

$$F_{swmin} = \frac{V_{inpk}^{\ 2} \cdot (V_{out} - V_{inpk})}{4(V_{out} \cdot P_{in} \cdot L_p)} \tag{4-10}$$

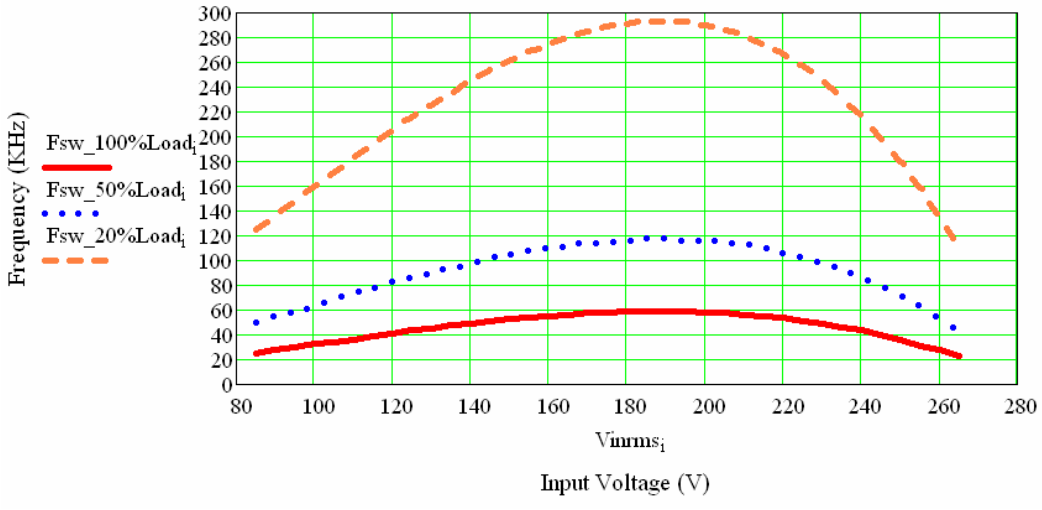


Fig. 3.46. The switching frequency of PFC circuit vs. input voltage.

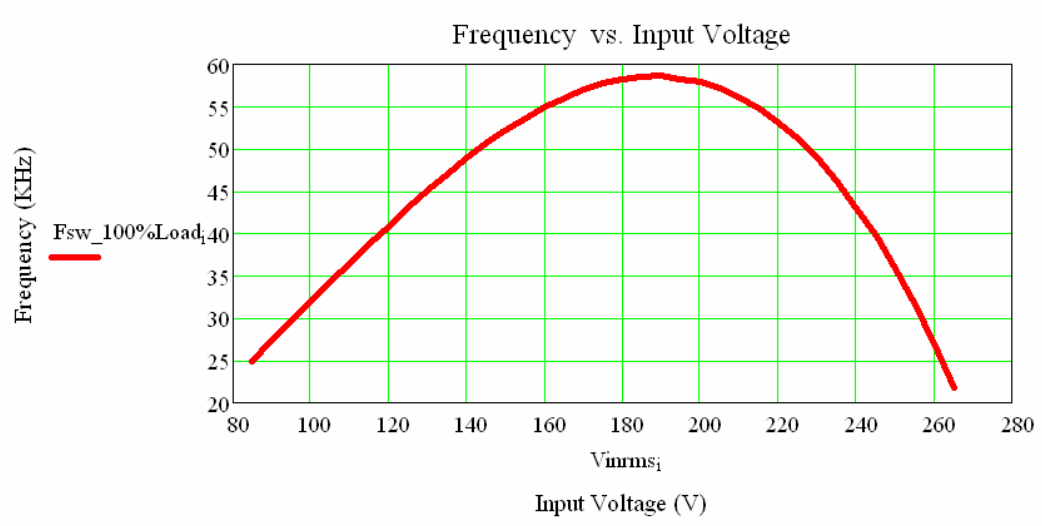


Fig. 3.47. The switching frequency vs. input voltage at full load.

3.6 PHASE EFFECT ANALYSIS

In this section, the analysis of input voltage, input current, turn-off time and switching frequency are based on three conditions, the phase angle is variable between 5 deg to 360

deg, and the input voltage range are 85 V, 175 V and 265 V with full load condition. All the calculations are using MathCAD to plot the calculated waveforms directly. It is easy to analyze the relationship between above parameters and phase angle to find out and avoid the potential design problem such as the highest switching frequency at zero cross (zero deg, 180 deg) [5] [35]. More detail calculations can be found in appendix.

3.6.1 Input Voltage vs. Phase

The min, normal and maximum input voltage waveforms are shown in Fig. 3.48.

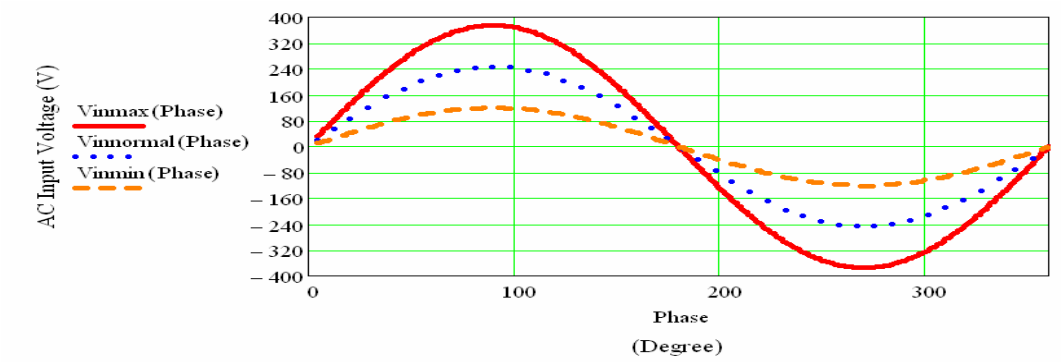


Fig. 3.48. Input voltage vs. phases.

3.6.2 Input Current vs. Phase

The input current is defined as equation (3-26) then the input current waveforms are shown in Fig. 3.49.

$$I_{in,rms} = I_{in} \cdot \sqrt{2} \cdot \sin\left(\frac{phase \cdot \pi}{180}\right) \tag{3-26}$$

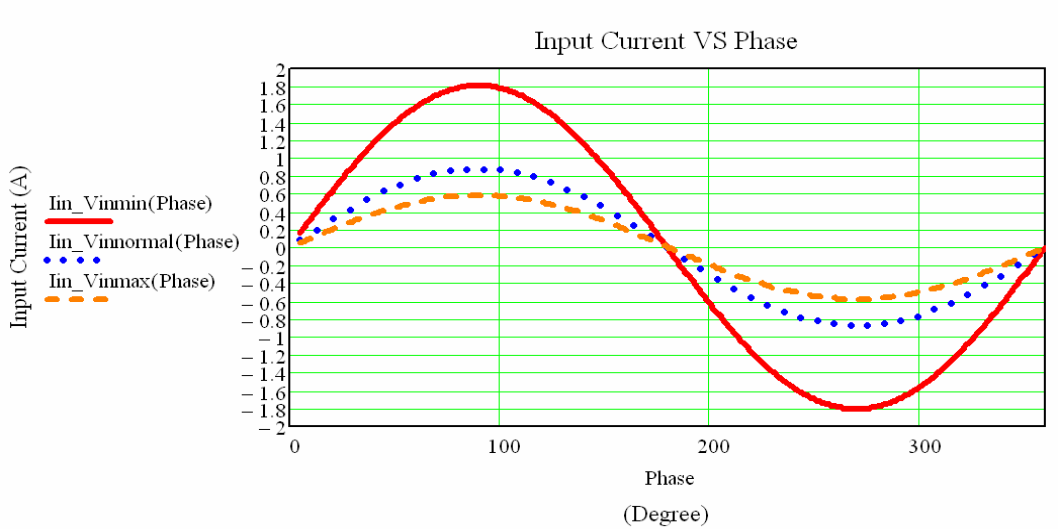


Fig. 3.49. Input current vs. phases.

3.6.3 Inductor Current vs. Phase

The inductor current is the absolute value of input current as equation (3-27) then the inductor current waveforms are shown in Fig. 3.50.

$$IL_{pk} = \left| 2 \cdot I_{in,rms}(phase) \right| \tag{3-27}$$

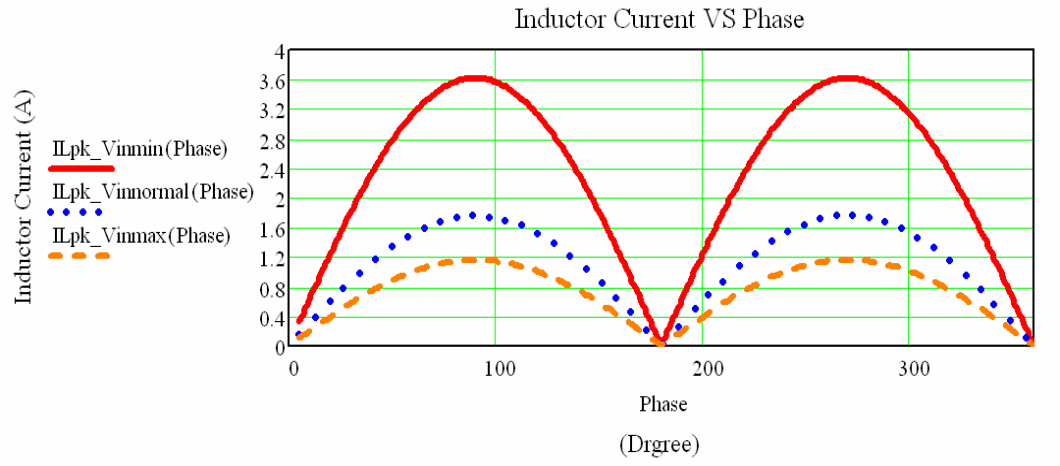


Fig. 3.50. Inductor current vs. phases.

3.6.4 Off Time vs. Phase

The turn on time (T_{on}) is fixed in this analysis and the turn off time (T_{off}) becomes important to calculate the maximum switching frequency.

$$T_{off} = \frac{L_p \left| IL_{pk}(phase) \right|}{V_{out} - \left| V_{in}(phase) \right|} \tag{3-28}$$

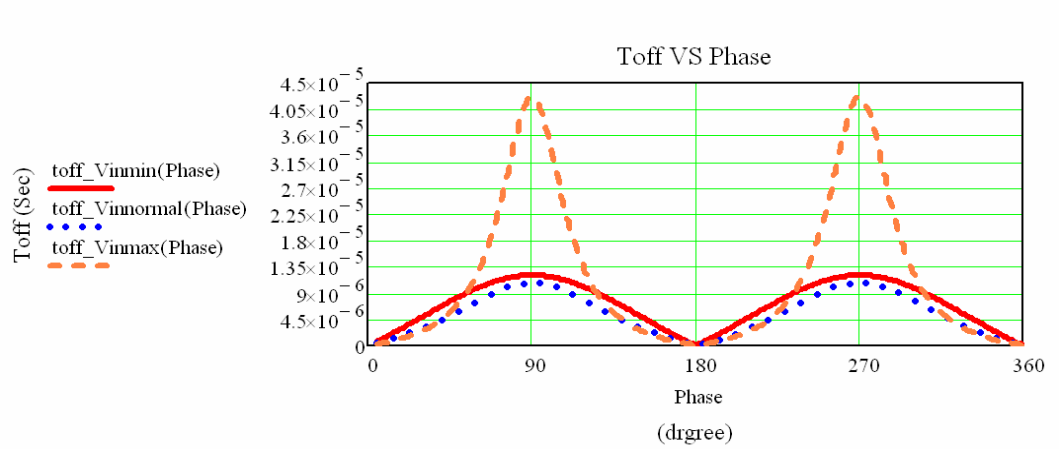


Fig. 3.51. T_{off} vs. Phases.

3.6.5 Switching Frequency vs. Phase

The switching frequency cab be defined as equation (3-29) and the plot in Fig. 3.52 to show that the maximum frequency close to 350 kHz with the maximum input voltage at 0 and 180 deg condition.

$$F_{sw} = \frac{V_{in,\,rms}{}^2}{2 \cdot L_p \cdot P_{out}} \cdot \left[1 - \frac{V_{in,\,pk} \cdot \sin(\omega t)}{V_{out}} \right] \tag{3-29}$$

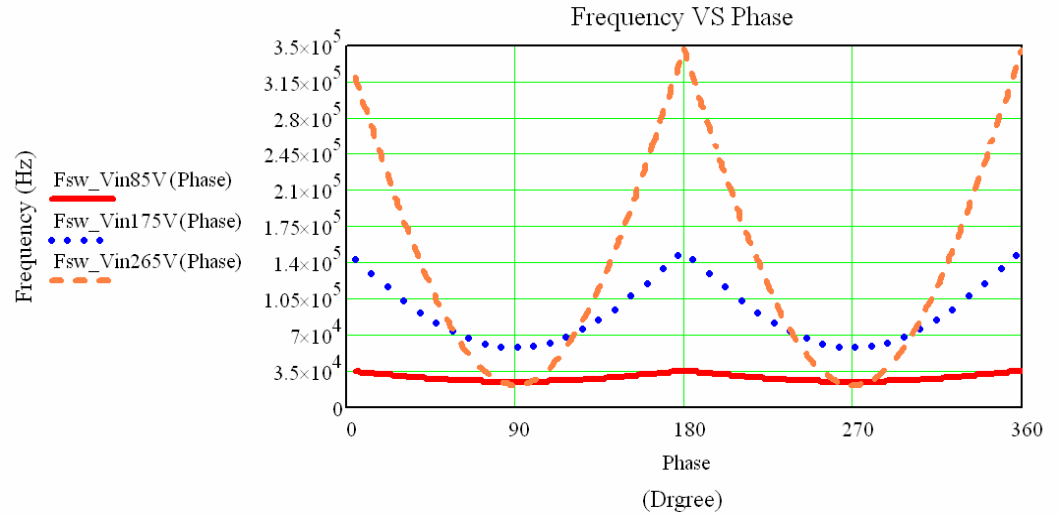


Fig. 3.52. Switching frequency vs. phases.

Chapter 4

Simulation and Experimental Results

4.1 Simulation Result

4.1.1 PSIM Circuits

Below is the modeling of MC33260 circuit by PSIM, based on the definition and description in [28]. The circuit simulates the major function such as voltage error signal, ZCD signal and some measurement for the value of PF, VA, power meter, input voltage/current and output voltage.

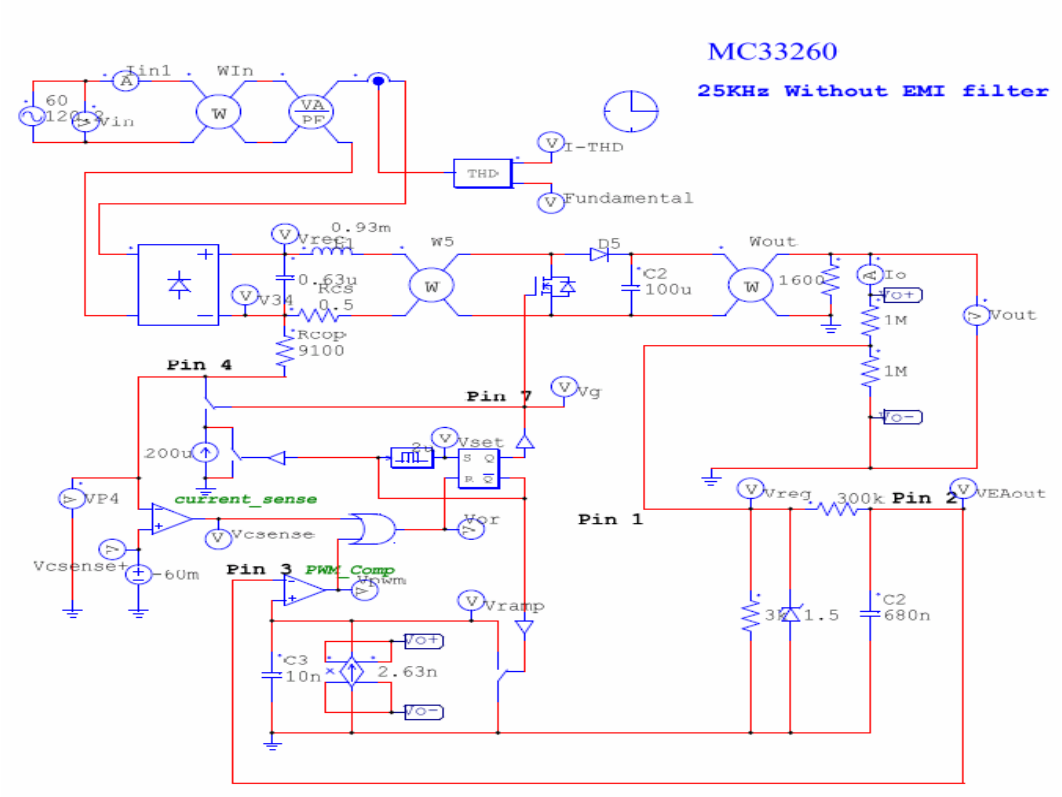


Fig. 4.1 PSIM modeling: 100W CRM PFC circuit with MC33260.

4.1.2 *Output Waveform*

The simulation of output voltage is 400 VDC with 7V ripple voltage and the result is similar with the calculation by MathCAD in Fig. 3.13.

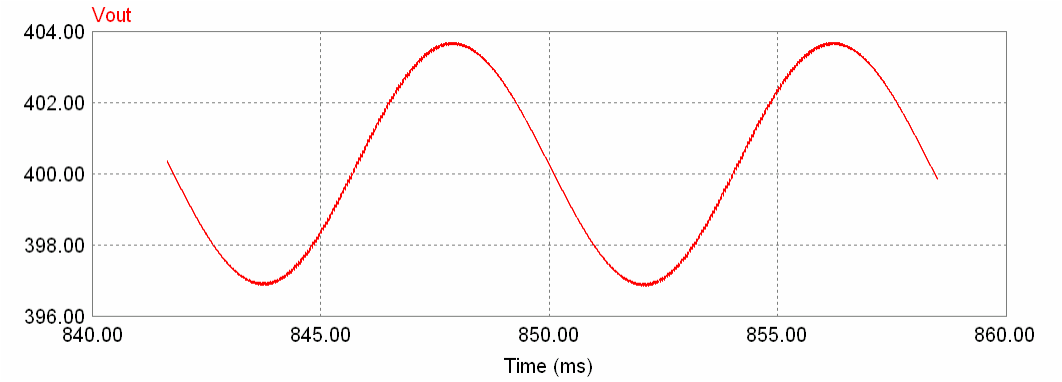


Fig. 4.2. PSIM: output waveform.

4.1.3 *Control Signal*

The Fig. 4.3 shows the output voltage error control and the MOSFET reset when V_{ramp} greater than voltage error output.

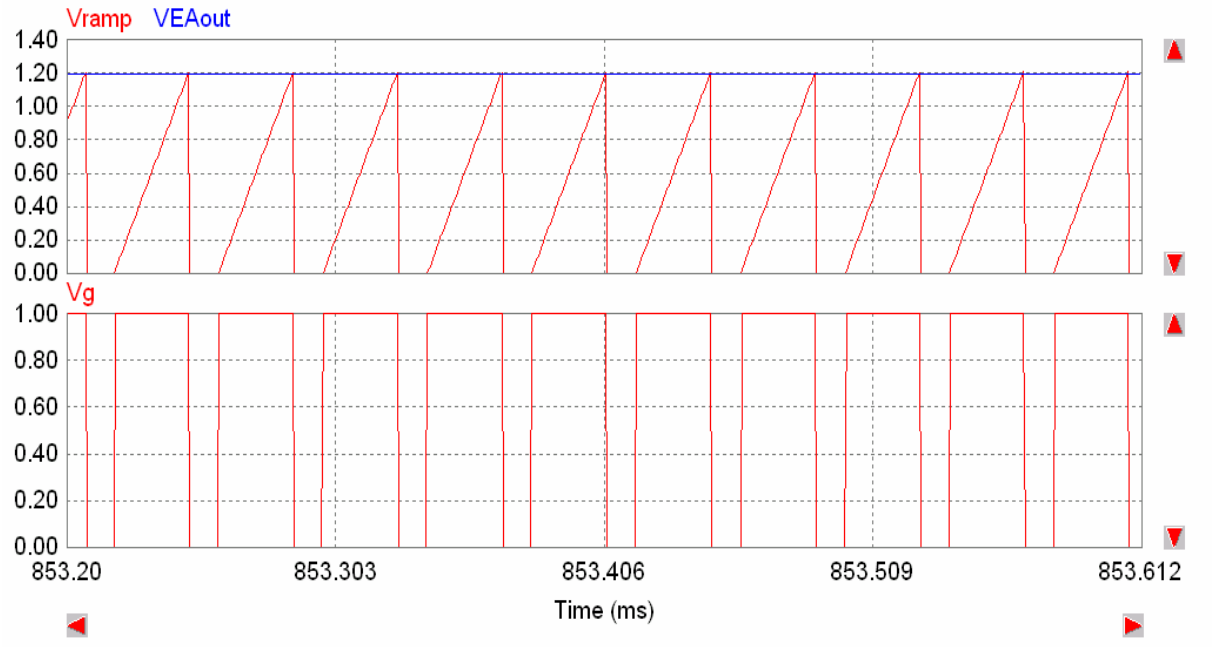


Fig. 4.3. Output voltage feedback control.

4.1.4 *Input Waveform*

The Fig. 4.4 shows simulation for the waveforms of input current, inductor current and input voltage for the PFC circuit without an EMI filter. The waveform of input voltage is ideal without any effect by current.

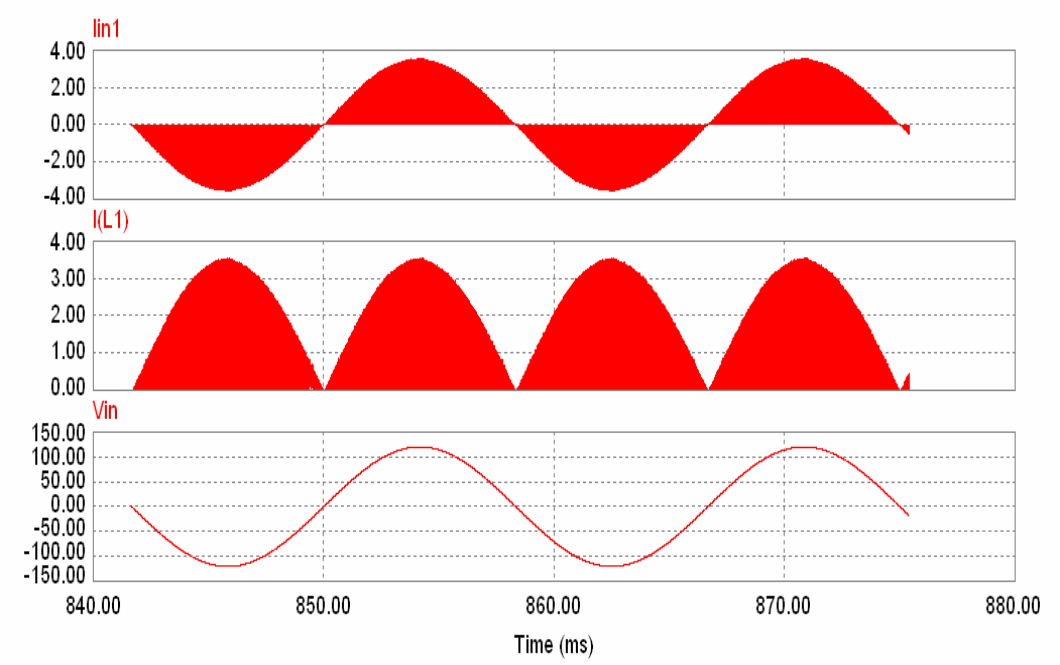


Fig. 4.4. Input current, inductor current and input voltage waveform.

4.1.5 *Input Current Harmonics Analysis*

Figure 4.5 shows the input current spectrum without EMI filter and the harmonic distributes after 25 kHz.

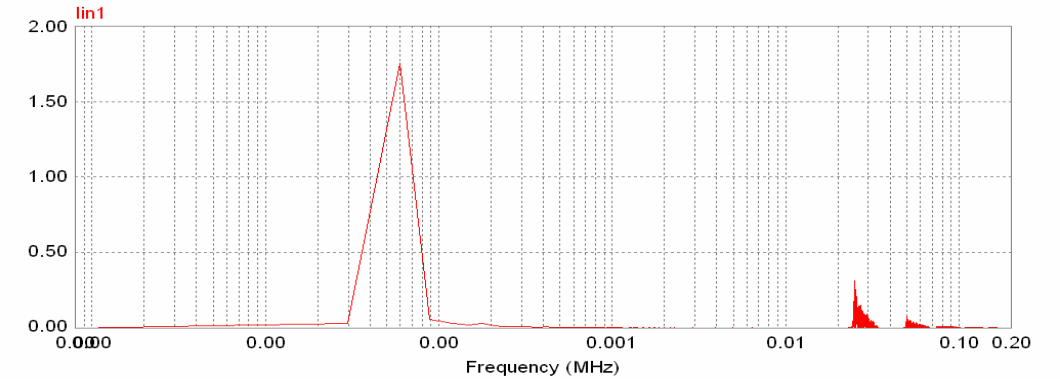


Fig. 4.5. Input current spectrum.

Import the simulated data of PSIM into the MathCAD program. The RMS value of input voltage and input current can be calculated as following equation and found the RMS of input voltage is 85 V and the input current is 1.462 A.

$$Vin_{rms} := \sqrt{\frac{1}{Points}\left[\sum_{n=1}^{Points}\left(Vin_n\right)^2\right]} \tag{4-1}$$

$$Iin_{rms} := \sqrt{\frac{1}{Points}\cdot\left[\sum_{n=1}^{Points}\left(Iin_n\right)^2\right]} \tag{4-2}$$

where the points is the sample point of one cycle of PSIM

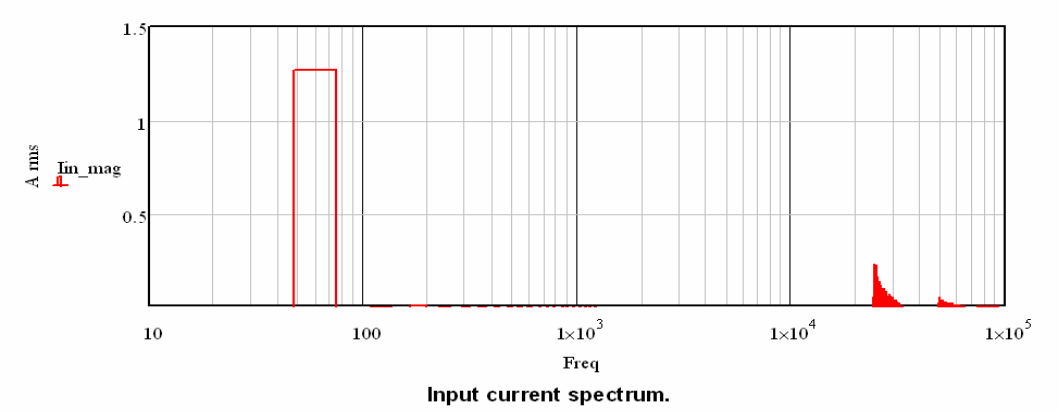


Fig. 4.6. Input current spectrum in MathCAD.

The THD of input current also can be calculated by MathCAD as equation (4-3) and the THD is 57.3%.

$$IinTHD := \frac{\sqrt{\sum_{h=1}^{H_{max}}\left[\left(AIin_h\right)^2+\left(BIin_h\right)^2\right]-\left[\left(AIin_{N_{cycle}}\right)^2+\left(BIin_{N_{cycle}}\right)^2\right]}}{\sqrt{\left(AIin_{N_{cycle}}\right)^2+\left(BIin_{N_{cycle}}\right)^2}} \tag{4-3}$$

Based on the design and analysis in cheaper 3.4.2, an investigated two-stage DM EMI filter is selected to reduce the current harmonics. Assume the EMI filter can attenuate the harmonics to 0.1% for the frequency range 18 kHz to 100 kHz. The estimation of THD is 2.4% only, and the estimation of input current waveform is shown in Fig. 4.7.

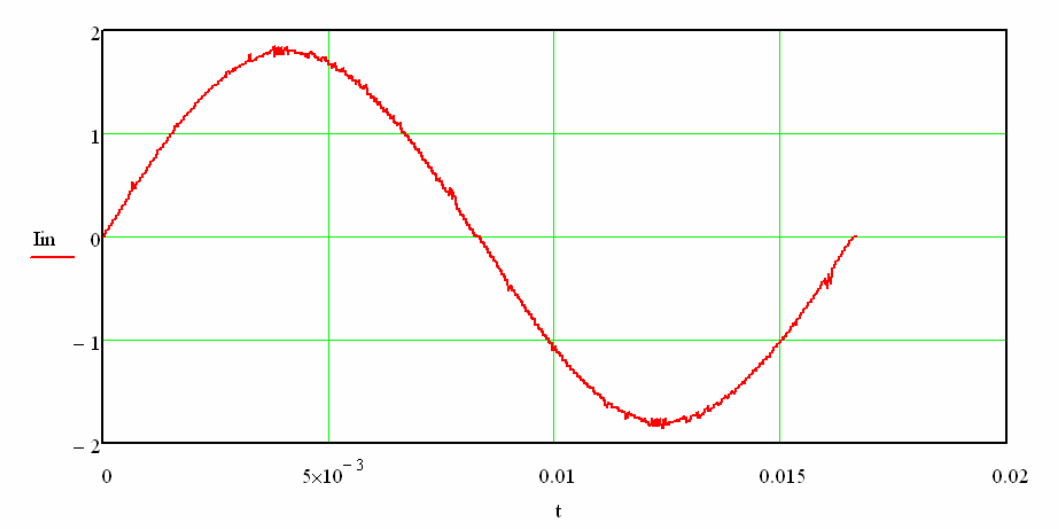


Fig. 4.7. Estimation of input current waveform in MathCAD.

The simulation of PSIM for adding an investigated two-stage DM EMI filter is shown in Fig. 4.8 and Fig. 4.9 shows the FFT result. Import the simulation data into the MathCAD, the improved THD is 3.8%.

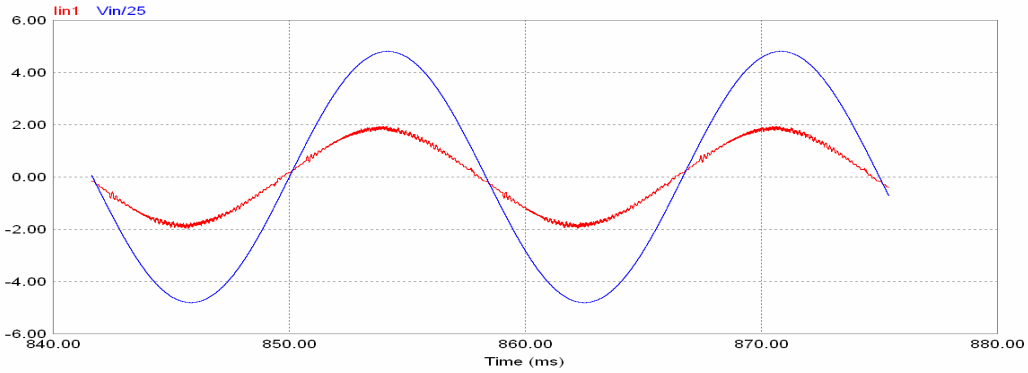


Fig. 4.8. Input current with input voltage.

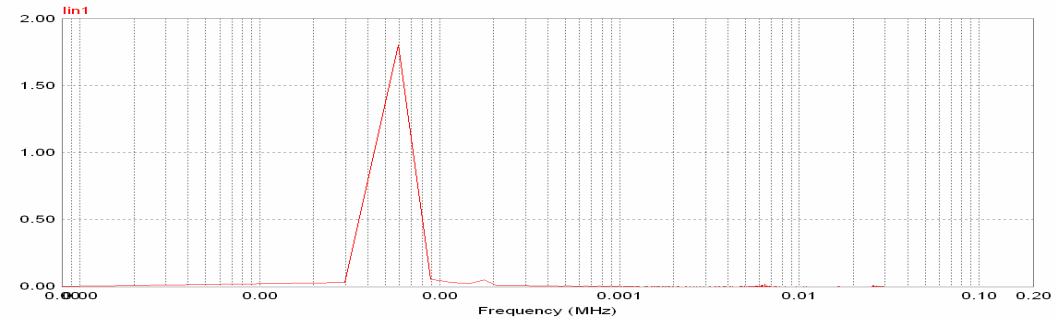


Fig. 4.9. Input current spectrum with a damping filter.

4.1.6 *Summary*

After an investigated DM EMI filter is added, the power factor increases from 0.87 to 0.995.

4.2 EXPERIMENTAL RESULTS

Some equipment is used for the measurement of input and output waveforms. They are: Oscilloscope TDS3034B x1, Current Probe x1, HV Probe P5200 x1 and a set of 1600 ohm load as shown in Fig. 4.10. The WaveStar software is selected to capture and convert the waveform from oscilloscope to CSV file.

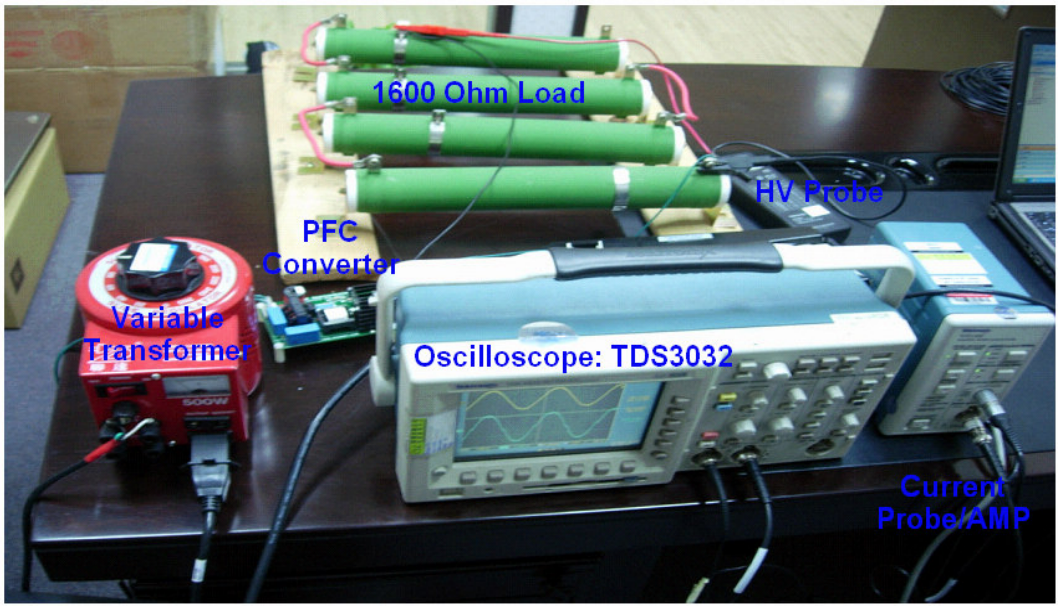


Fig. 4.10. Experimental equipments and condition.

4.2.1 *Output Waveform*

Figure 4.11 shows the output voltage is around 400 VDC and the peak-peak ripple voltage is around 23 VDC.

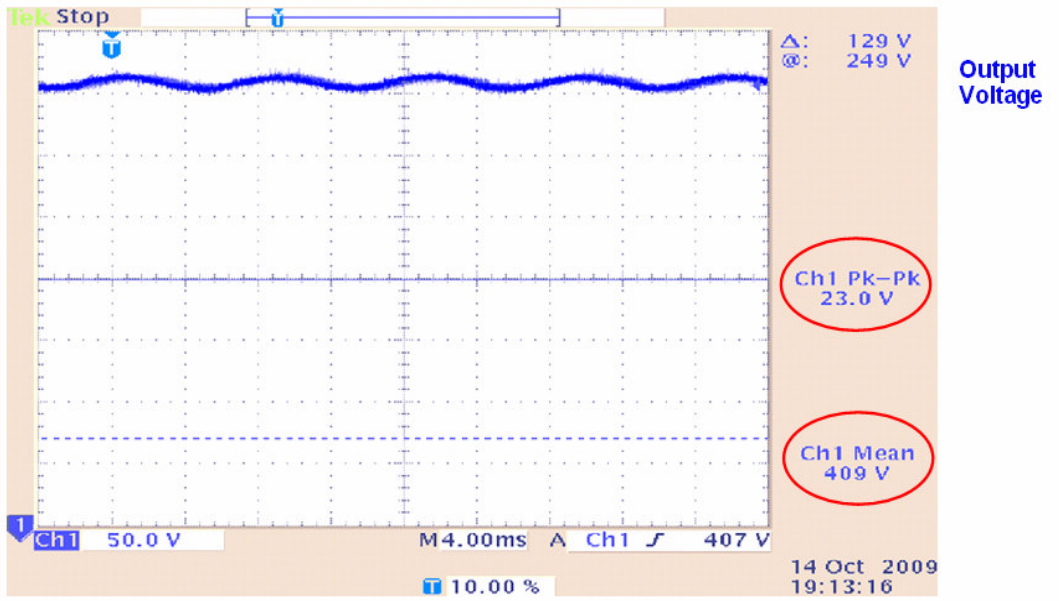


Fig. 4.11. Experimental output voltage waveform.

4.2.2 Input Waveform

The MathCAD can impact the data which transfer from WaveStar into the MathCAD program to analyze. It is easy to combine the input current and voltage waveform to check the zero-cross waveform and calculating the THD and RMS value of input voltage and current for the analysis.

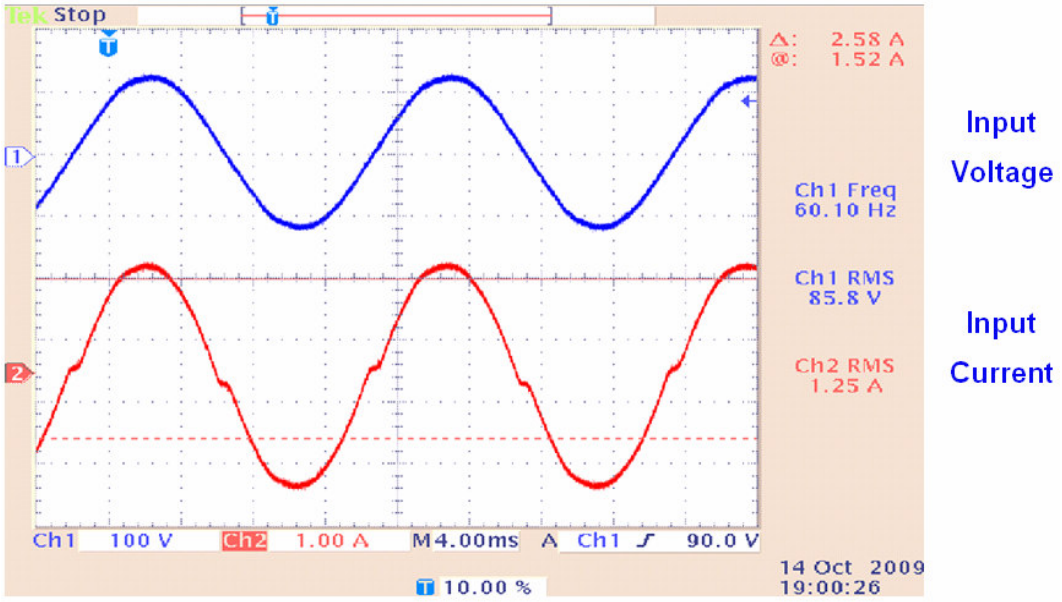


Fig. 4.12. Experimental input voltage and current waveform.

4.2.3 *Input Current Harmonics Analysis*

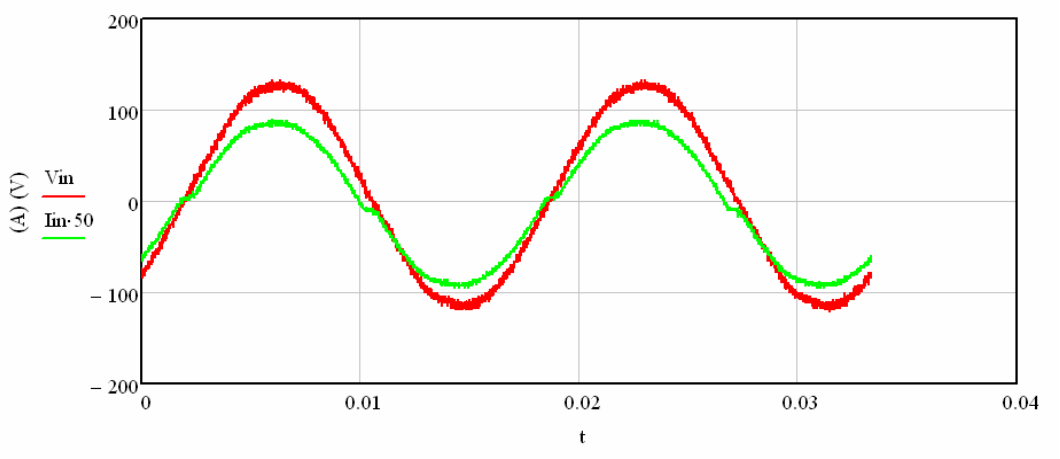


Fig. 4.13. Input current (x50) with input voltage.

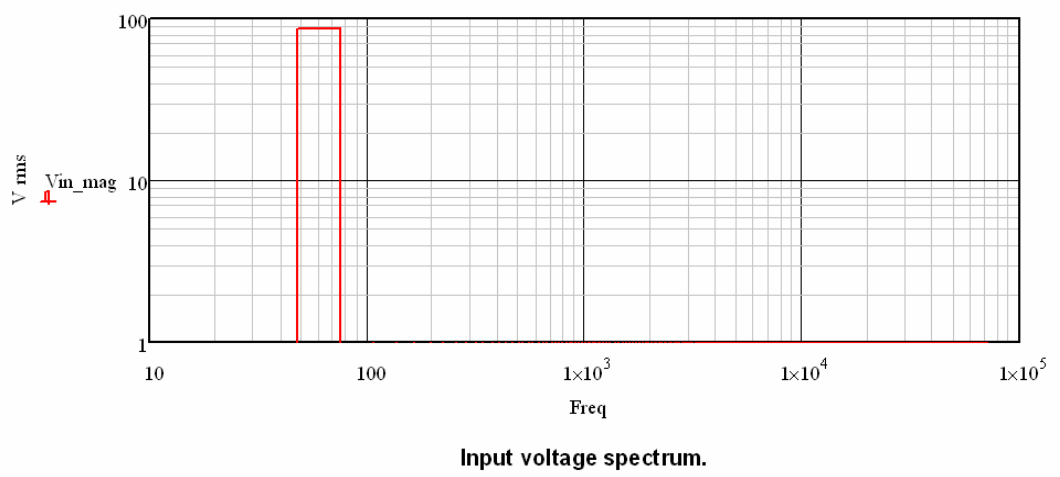


Fig. 4.14. Input voltage spectrum.

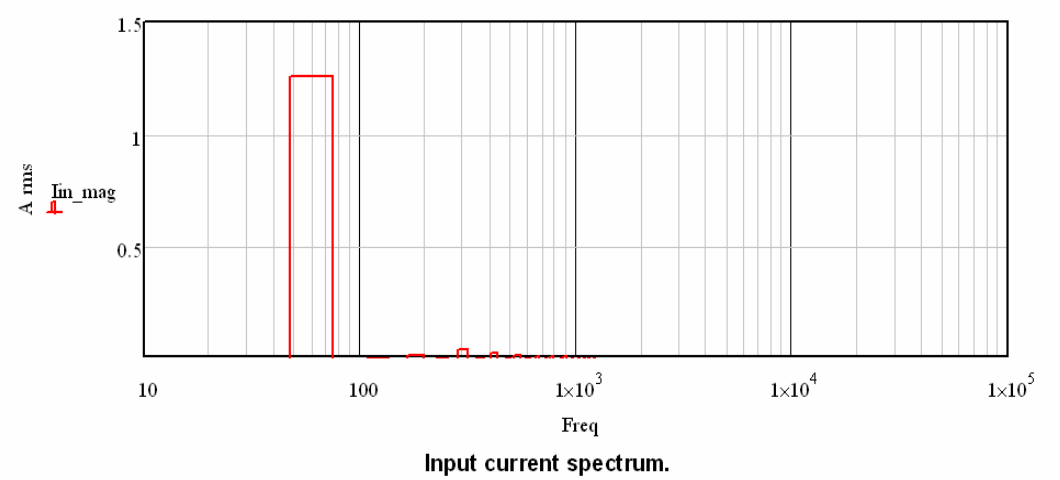


Fig. 4.15. Input current spectrum.

Fig. 4.14 and Fig. 4.15 are the spectrum of input voltage and current. The THD of input current can be calculated by MathCAD as equation (4-3) and it is 4.42%.

Assume the harmonics between 3rd and 50th can be reduced to 10% only the estimation waveform of input voltage and current are shown in Fig. 4.16 and Fig. 4.17, and the THD of input current can be improved to 1.7%.

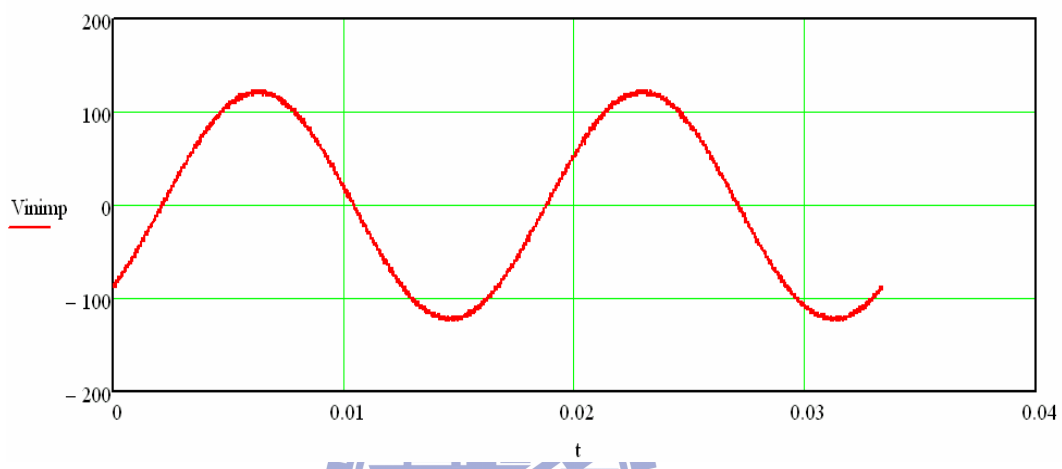


Fig. 4.16. Estimation of input voltage waveform in MathCAD.

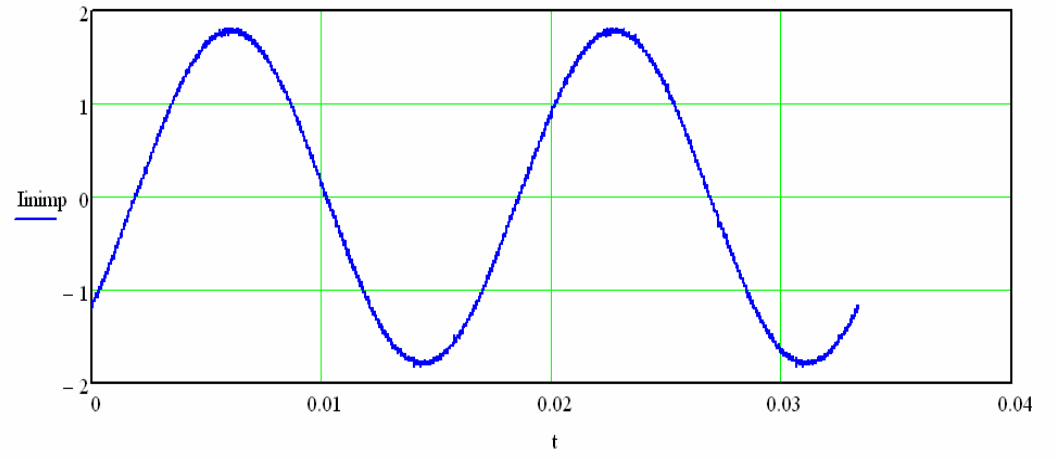


Fig. 4.17. Estimation of input current waveform in MathCAD.

4.3 SUMMARY

Fig. 4.18 shows the input current spectrum up to 40th of line frequency and all meet the limits of EN-61000-3-2 class D [5] [12]. The estimation of 90% attenuation between 3rd and 50th harmonics order is shown in Fig. 4.19 for better performance.

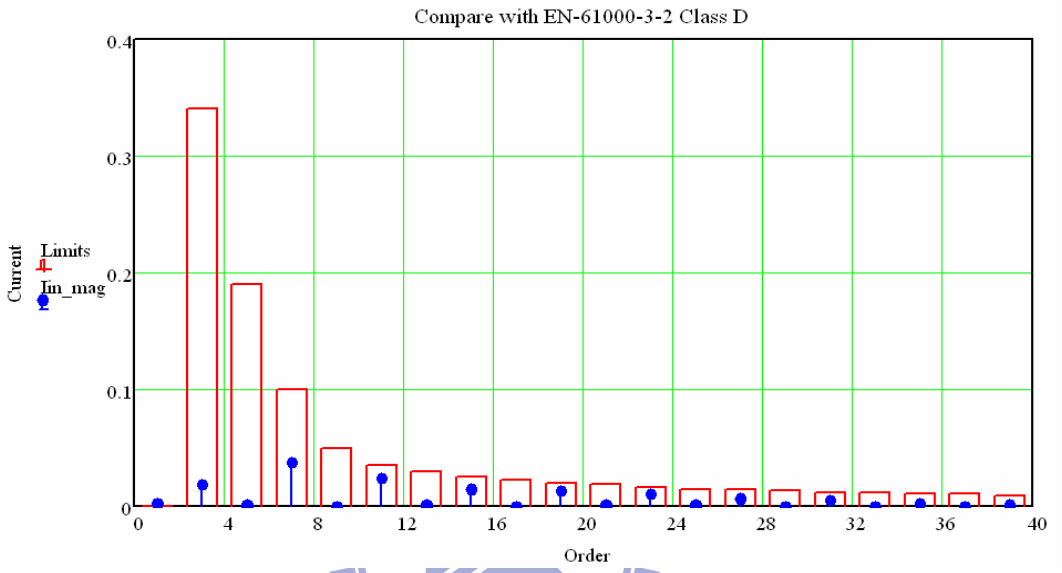


Fig. 4.18. Input current spectrum vs. EN-61000-3-2 class D limits.

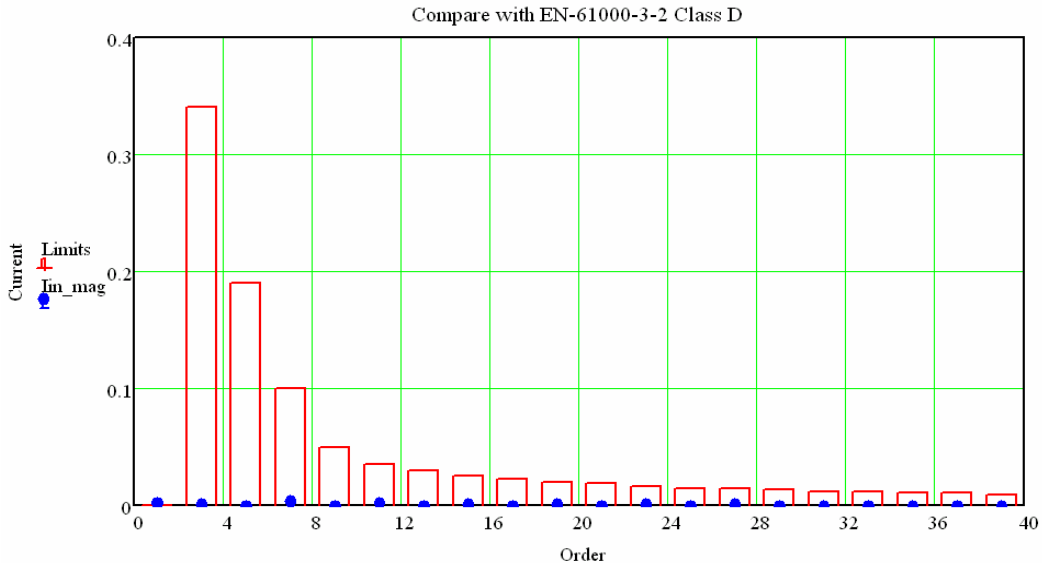


Fig. 4.19. Estimation of improved input current spectrum vs. EN-61000-3-2 class D limits.

Chapter 5

Conclusions and Future Works

5.1 CONCLUSIONS

In this thesis, a mathematical method for the analysis of the input current harmonics, EMI filter design and power losses for critical conduction mode PFC converters was proposed. Power factor and THD were simulated by PSIM and also be calculated by MathCAD in chapter 3 and 4. It is easy for a student to study the theory of CRM PFC by using above methods.

Finally, the input current was plotted by the Fourier series method in the frequency domain and compared with the EN 61000-3-2 limits up to 40th harmonic of line frequency. The simulation results of the THD of input current is less than 3%, the power factor is up to 0.995 and the experimental result of the current THD is 4.42%.

5.2 FUTURE WORKS

Future works related to this research are discussed and suggested in this section. One difficult in the realization of the CRM PFC controller is that we must limit the highest switching frequency around the zero crossing and minimizing its current distortion at the same time. The zero crossing distortion becomes significant at light load condition and special control scheme should be developed to solve this problem [62]-[69].

EMI filter design is another challenge in this research. It includes many methods such as calculation, simulation, noise, PCB layout and input current measurements with frequency spectrum analyzer and LISN [70]-[76].

Reference

[1] C. L. Sirio, “Analysis of line current harmonics for single-phase PFC converters,” in *Proc. IEEE Power Electronics Specialists Conference, 2007*, pp.1291-1297.

[2] Texas Instruments Inc., “UCC38050 100-W critical conduction power factor corrected (PFC) preregulator,” Application Notes, July 2004.

[3] S. Luo, W. Qiu, and C. Batarseh, “Optimization design of a single-stage AC-DC converter with averaging circuit model and MathCAD©,” in *Proc. IEEE Applied Power Electronics Conference and Exposition*, vol. 1, 2002, pp. 459-465.

[4] Dong Li, and Xinbo Ruan, “A high efficient boost converter with power factor correction,” in *Proc. IEEE Power Electronics Specialists Conference,* vol. 2, 2004, pp. 1653-1657.

[5] C. H. Hung, Y. Y. Tzou, “MathCAD design of critical conduction mode PFC converters,” in *Proc. IEEE Power Electronics and Motion Control Conference*, 2009, pp. 1684-1688.

[6] R. W. Larsen, *Introduction to MathCAD*. Englewood Cliffs, NJ: Prentice-Hall, 1999.

[7] Pritchard, Philip J, *Mathcad: A tool for engineering problem solving.* Boston, WCB/McGraw-Hill, 1998

[8] M. Sanz, and A. Lazaro, “Improvement of power electronics education with an interactive electronic book based on MathCAD,” in *Proc IEEE Power Electronics Education,* 2005, pp. 129-134.

[9] C. Domnisoru, “Using MathCAD in teaching power engineering,” *IEEE Trans. Education*, vol. 48, pp.157-161, Feb. 2005.

[10] Mohan, and Undeland. Robbins, *Power Electronics.* third Edition, Wiley, 2003.

[11] Christophe P. Basso, *Switch-Mode power supplies SPICE simulations and practical designs.* first Edition, New York: McGraw-Hill, 2008.

[12] S. Basu, M. H. J. Bollen, and T. M. Undeland, “PFC strategies in light of EN 61000-3-2,” in *Proc. European Power Electronics Conf. Rec.,* Sep. 2004.

[13] On-Semiconductor, “Power factor correction handbook,” 2007.

[14] K. H. Billings, “Switchmode power supply handbook,” second Edition, New York, McGraw-Hill, 1999.

[15] L. Balogh and R. Redl, “Power-factor correction with interleaved boost converters in continuous-inductor-current mode,” in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 1993, pp. 168-174.

[16] James P. Noon, “Designing high-power factor off-line power supplies,” Texas Instruments Inc., 2003.

[17] On Semiconductor, “Greenline compact power factor controller: innovative circuit for

cost effective solutions," Application Notes, 2005.

[18] Fairchild, "Design of power factor correction circuit using FAN7529," Application Notes, 2006.

[19] On Semiconductor, "MC34262, MC33262 power factor controllers," Application Notes, 2005.

[20] STMicroelectronics, "L6561, Enhanced transition mode power factor corrector," Application Notes, 2003.

[21] Texas Instruments Inc., "UCC38050 transition mode PFC controller," Datasheet, 2002.

[22] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc IEEE Ind Applicat. SOC Conf Proc.,* 1976, pp. 94-107.

[23] S Hiti, V Vlatkovic, D Borojevic, and F. C. Lee, "A new control algorithm for three-phase PWM buck rectifier with input displacement factor compensation," in *Proc. IEEE Power Electron. Spec. Conf.*, 1993, pp.648-654.

[24] B. H. Cho and B. Choi, "Analysis and design of multi-stage distributed power systems," in *Intelec,* 1991, pp. 220-226.

[25] V. Vlatkovic', D. Borojevic', and F.C. Lee, "Input filter design for power factor correction circuits," *IEEE Trans. Power Electron.,* vol. 11, pp. 199-205, Jan. 1996.

[26] Noon, J. P. and D. Dalal, "Practical design issues for PFC circuits," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, vol.1, 1997, pp. 51-58.

[27] F. Y. Shih, D. Y. Chen, Y. P. Wu, and Y. T. Chen, "A procedure for designing EMI filters for AC line applications," *IEEE Trans. Power Electron.,* vol. 11, pp. 170–181, Jan. 1996.

[28] On Semiconductor, "Design of power factor correction circuit using greenline compact power factor controller MC33260," Application Notes, 2002

[29] D. Li and X. Ruan, "A high efficient boost converter with power factor correction," in *Proc. IEEE Power Electronics Specialists Conference*, vol. 2, 2004, pp. 1653–1657.

[30] J. S. Lai, and D. Chen, "Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode," *in Proc. IEEE Appl. Power Electron. Conf*, 1993, pp. 267–273.

[31] L. Ping and K. Yong, "Design and performance of an AC/DC voltage source converter," in *Proc. IEEE INTELEC*, 2000, pp. 419–423.

[32] D. S. L. Simonetti, J. L. F. Vieira, and G. C. D. Sousa, "Modeling of the high-power-factor discontinuous boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 46, pp. 788–795, Aug. 1999.

[33] S. Basu, "Inductor design considerations for optimizing performance & cost of continuous mode boost PFC converters," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, vol.2, 2005, pp. 1133-1138.

[34] Kurachi, T. Shoyama, M. Ninomiya, T., "Analysis of ripple current of an electrolytic

capacitor in power factor controller," in *Proc. IEEE PEDS*, vol.1, 1995, pp. 48-53.

[35] On Semiconductor, "Power factor correction stages operating in critical conduction mode," Application Notes, 2003.

[36] D. Y. Chen and F. C. Lee, "Separation of the common-mode and differential-mode conducted EMI noise," *IEEE Trans. Power Electron.,* vol. 11, pp. 480-487, May, 1996.

[37] J. Zhang, J. W. Shao, P. Xu and F. C. Lee, "Evaluation of input current in the critical mode boost PFC converter for distributed power system" in *Proc. IEEE Applied Power Electronics Conference and Exposition*, vol.1, 2001, pp. 130-136.

[38] S. Wang, F.C. Lee, D.Y. Chen and W.G. Odendaal, "Effects of parasitic parameters on the performance of EMI Filters," in *proc. IEEE Power Electronics Specialist Conference,* 2003, pp.73-78.

[39] S. Wang, F.C. Lee and W.G. Odendaal, "Improving the performance of boost PFC EMI filters," in *proc. IEEE Applied Power Electronics Conference and Exposition*, 2003, pp. 368 -374.

[40] L. Zhao, J. D. V. Wyk, "A generalized two conductor model for integrated passive components," in *Proc. of CPES seminar*, 2002, pp. 428-433.

[41] B. Norman and B. Theodore, *Linear Network Theory: Analysis, Properties, Design and Synthesis.* Matrix Publishers, Inc., 1981.

[42] H. W. Ott, *Noise Reduction Techniques in Electronic Systems.* Second edition, John Wiley & Sons, Inc, 1988.

[43] M. J. Nave, *Power line filter design for switched-mode power supply.* Van Nostrand Reinhild, New York, 1991.

[44] R. D. Middlebrook, "Design techniques for preventing input filter oscillations in switched-mode regulators," *Proceedings of the Fifth National Solid-State Power Conversion Conference, Powercon 5*, 1978, pp. A3-1-A3-16.

[45] T. K. Phelps and W. S. Tate, "Optimizing passive input filter design," *Proceedings of the Sixth National Solid- State Power Conversion Conference, Powercon 6*, 1979, pp. G1-1 through G1-10.

[46] V. Grigore, J. Kyyra, and J. Rajamaki, "Input filter design for power factor correction converters operating in discontinuous conduction mode," in *Proc. IEEE International Symposium on Electromagnetic Compatibility*, vol. 1, 1999, pp. 145-150.

[47] B. M.S, C. Crebier, S. Ragon, E. Hertz, J. Wei, J. Zhang, D. Boroyevich, Z. Gurda, P. K. Lindner, A. Arpilliere, "Optimization techniques applied to the design of a boost power factor correction converter," in *Proc. IEEE Power Electronics Specialists Conference,* vol. 2, 2001, pp. 920-925.

[48] C. S. Moo, H. C. Yen , and C. R. Lee, "Implementation of orthogonal arrays on designing passive LC filters," *IEEE Power Electronics Specialists Conference*, 1998,

pp. 1662-1667.

[49] C. R. Kohut, "Input filter design criteria for switching regulators using current mode control," *IEEE Trans. Power Electron.*, vol. 7, pp. 469-479, July, 1992.

[50] Y. F. Zhang, L. Yang, and C. Q. Lee, "Optimal design of integrated EMI filter," *in Proc. IEEE Appl. Power Electron. Conf*, vol. 1, 1995, pp. 274-280.

[51] R. W. Erickson, "Optimal single resistor damping of input filters," in *Proc. IEEE Applied Power Electronics Conference and Exposition,* vol. 2, 1999, pp. 1073-1079.

[52] R. D. Middlebrook, "Power filter damping," in *Proc. IEEE Power Electronics Design Conference,* 1985, pp. 96-105.

[53] C. W. T. Mclyman, *Magnetic Core Selection for Transformers and Inductor*. Marcel Dekker, Inc., New York, 1982.

[54] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics.* second Edition, Kluwer Accademic Publishers Co., 2001.

[55] J. Sun, "Input impedance analysis of single-phase PFC converters," *IEEE Trans. Power Electron*., pp. 308-314, March 2005.

[56] F. S. R. Dos, J. C. M. Lima, V. M. Canalli, J. A. Pomilio, J. Sebastian, and J. Uceda, "Matching conducted EMI to international standards," in *Proc. IEEE Power Electronics Conf.,* vol. 1, 2002, pp. 388-393.

[57] S. Wang, F. C. Lee, W. G. Odendaal, and J. D. V. Wyk, ''Improvement of EMI filter performance with parasitic coupling cancellation,'' *IEEE Trans. Power Electron*., vol. 20, pp. 1221-1228, June. 2005.

[58] S. Wang, F. C. Lee, W. G. Odendaal, "Improving the performance of Boost PFC EMI filters," *IEEE Applied Power Electronics Conference and Exposition*, vol. 1, 2003, pp. 368–374.

[59] Y. Zhao, "Single phase power factor correction circuit with wide output voltage range," Virginia Polytechnic Institute and State University, 1998.

[60] M. O'Loughlin, "UCC38050 MathCAD design tool," Texas Instruments Inc., 2004.

[61] S. Deng, H. Mao, T. Wu, S. Xiao, I. Batarseh, "Power losses estimation platform for power converters," *IEEE Applied Power Electronics Conference and Exposition*, 2004, pp. 1784-1789.

[62] D. P. Garinto, "A new zero-ripple boost converter with separate inductors for power factor correction," *IEEE Power Electronics Specialists Conference*, 2007, pp. 1309-1313.

[63] C. H. Chan and M. H. Pong, "Input current analysis of interleaved boost converters operating in discontinues-inductor-current-mode," in *Proc. IEEE Power Electronics Specialists Conference*, 1997, pp. 392-398.

[64] T. W. Heo, Y. D. Son, and E. Santi, "Analysis of the interleaved type power factor correction (PFC) converter in discontinuous current mode," in *Proc. IEEE Industrial*

Electronics Society Conference, vol. 3, 2004, pp.2706-2711.

[65] J. D. Zhang, F. C. Lee, and M. M. Jovanovic, "A novel interleaved discontinuous-current-mode single-stage power-factor-correction technique with universal-line input," in *Proc. IEEE Power Electronics Specialists Conference*, vol. 2, 2001, pp.1007-1012.

[66] J. R. Pinheiro, H. A. Grundling, D. L. R. Vidor, and J. E. Baggio, "Control strategy of an interleaved boost power factor correction converter," in *Proc. IEEE International Conference on Power Electronics Specialists*, 1999, pp.137-142.

[67] M. Veerachary, T. Senjyu, and K. Uezato, "Modeling and analysis of interleaved dual boost converter," in *Proc. IEEE International Conference on Industrial Electronics Society*, 2001, pp.718-722.

[68] B. A. Miwa, D. M. Otten, M. E. Schlecht, "High efficiency power factor correction using interleaving techniques," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 1992. pp. 557-568.

[69] L. B. Rick, O. B. Barry, H. F. Gregory, M. Donald, Andrew Marsh, "Interleaved converter power factor correction method and apparatus," United States Patent 6,690,589 B2, Feb. 10, 2004.

[70] S. Wang, F. C. Lee and W. G. Odendaal, "Controlling the parasitic parameters to improve EMI filter performance," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, vol. 1, 2004, pp. 503-509.

[71] S. Wang , F.C. Lee, D.Y. Chen, W.G. Odendaal, "Effects of parasitic parameters on EMI filter performance," *IEEE Trans. Power Electron.*, pp. 869-877, May 2004.

[72] Y. Sheng, W. Eberle, and Y. F. Liu, "A novel EMI filter design method for switching power supplies," *IEEE Trans. Power Electron.*, vol. 19, pp. 1668-1678, Nov. 2004.

[73] J. L. SCHANEN, L. JOURDAN, J. ROUDET, "Layout optimization to reduce EMI of a switched mode power supply," session 10-6 : EMC/EMI issues for SMPS IEEE PESC 2002

[74] D. H. Liu, J. G. Jiang, "High frequency characteristic analysis of EMI filter in switch mode power supply(SMPS)," in *Proc. IEEE Power Electronics Specialists Conference*, vol. 4, 2002, pp.2039-2043.

[75] W. Zhang, M. T. Zhang, F. C. Lee, J. Roudet, and E. Clavel, "Conducted EMI analysis of a boost PFC circuit," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, vol. 1, 1997, pp. 223-229.

[76] R. G. Munoz and T. W. Hao, "Simulation of response of modeled EMI filter to measured or simulated time domain waveforms," in *Proc. IEEE International Symposium*, 1995, pp 272-275.

Appendix:

CRM PFC Design and Analysis for component selection, EMI filter, Power loss

---

Design Variables	Definition
$fline := 60Hz$	Line Frequency
$Vinmin := 85V$	Minimum Input Voltage
$Vinmax := 265V$	Maximum Input Voltage
$Pout := 100W$	Maximum Output Power
$Vout := 400V$	Output Voltage
$fs := 25 \cdot 10^{3} Hz$	Minimum Switching Frequency
$\omega := 2\pi \cdot fline$	
$t\_cycle := 16.7 \cdot 10^{-3} s$	Period of one Line Cycle
$Vdrop := 85V$	Amount of holdup voltage
$\eta := 0.92$	Efficiency
$Pin := \frac{Pout}{\eta}$	$Pin = 108.696\,W$
$t\_hold := 40 \cdot 10^{-3} s$	Output Hold up time
$Rout := \frac{Vout^{2}}{Pout} = 1.6 \times 10^{3}\,\Omega$	

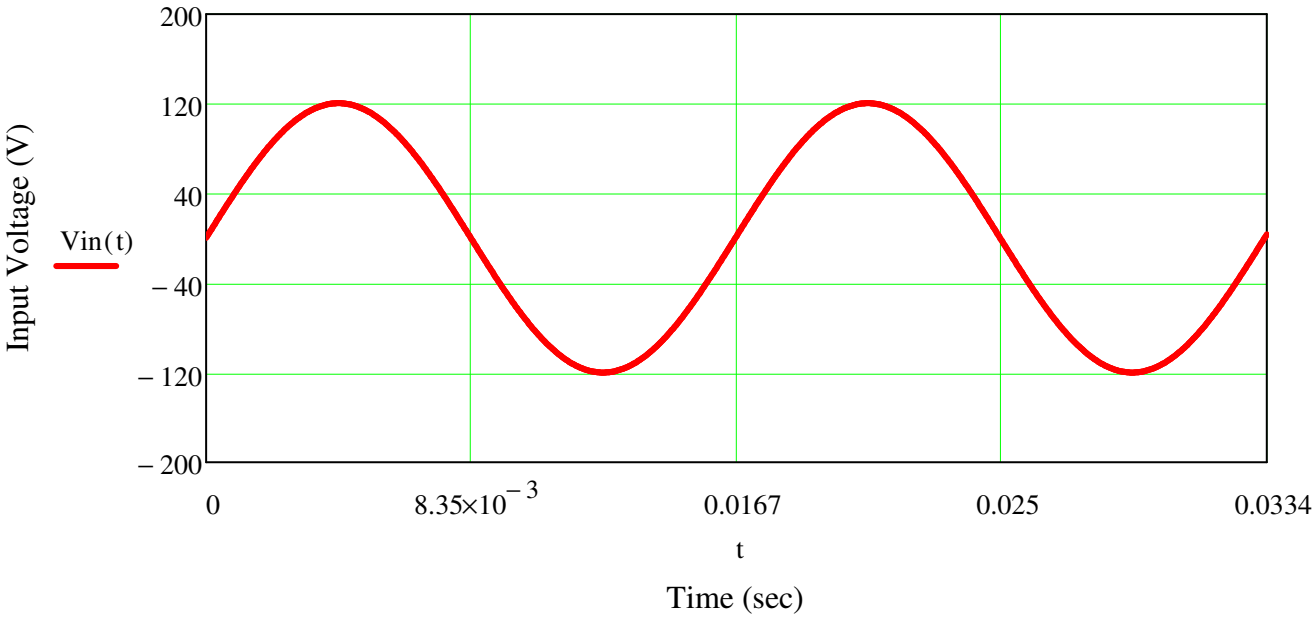
Calculation of AC Voltage and Current:

$Vinrms := Vinmin$ $\quad Vinrms = 85\,V$

$Vinpk := Vinrms \cdot \sqrt{2}$ $\quad Vinpk = 120.208\,V$

$Vin(t) := Vinpk \cdot \sin(\omega \cdot t)$

$Iinrms := \frac{Pin}{Vinrms}$ $\quad Iinrms = 1.279\,A$



Inductor Selection:

$$Iinpk := \frac{\sqrt{2}\cdot Pout}{\eta\cdot Vinmin}$$

$Iinpk = 1.808\,A$

$$ILpk := 2Iinpk$$

$ILpk = 3.617\,A$

$$Iin(t) := Iinpk\cdot\sin(\omega\cdot t)$$

$$Lp := \frac{\left(Vout - \sqrt{2}\cdot Vinmin\right)\cdot\eta\cdot Vinmin^2}{2fs\cdot Vout\cdot Pout}$$

$Lp = 9.299\times10^{-4}\,H$

Using **EPCOS E 30/15/7**, Bmax=0.3T, Ae=60mm2

$$Bmax := 0.3T$$

$$Ae := 60mm^2$$

$$Np := \frac{Lp\cdot ILpk}{Bmax\cdot Ae} = 186.851$$

$Np = 187$

Max Pk-Pk ripple current of inductor:

$$\Delta ILmax := \frac{\sqrt{2}\,Vinmin}{Lp\cdot fs}\left(1 - \frac{\sqrt{2}\,Vinmin}{Vout}\right) = 3.617\,A$$

$ILpk = 3.617\,A$

Design of the current sense circuit:

Rcs : current sense resistor losses

Choose Rcs=0.68 ohm $Rcs := 0.5\Omega$

$$Prcs := \frac{1}{6}\cdot Rcs\cdot ILpk^2$$ $Prcs = 1.09\,W$

Rocp: Overcurrent protection resistor

Set Iocp = 200uA $Iocp := 200\mu A$

$$Rocp := \frac{Rcs\cdot ILpk}{Iocp}$$ $Rocp = 9.042\times 10^3\,\Omega$ Select 9100 ohm

Calculation of Ton , Toff and Switching Frequency:

$$Ton := \frac{2\sqrt{2}\cdot Pout}{\eta\cdot Vinmin}\cdot\frac{Lp}{\sqrt{2}\,Vinmin}$$ $Ton = 2.798\times 10^{-5}\,s$

$$Tonmax := 2\cdot Lp\cdot\frac{Pout}{\eta\cdot(Vinmin)^2}$$ $Tonmax = 2.798\times 10^{-5}\,s$

$t := 0.000001s, 0.00001s .. 0.0333s$

$$Toff(t) := \left|2\cdot\sqrt{2}\cdot Lp\cdot\frac{Pin}{Vinmin\cdot\left(Vout - \left|\sqrt{2}\cdot Vinmin\cdot\sin(\omega\cdot t)\right|\right)}\cdot\sin(\omega\cdot t)\right|$$

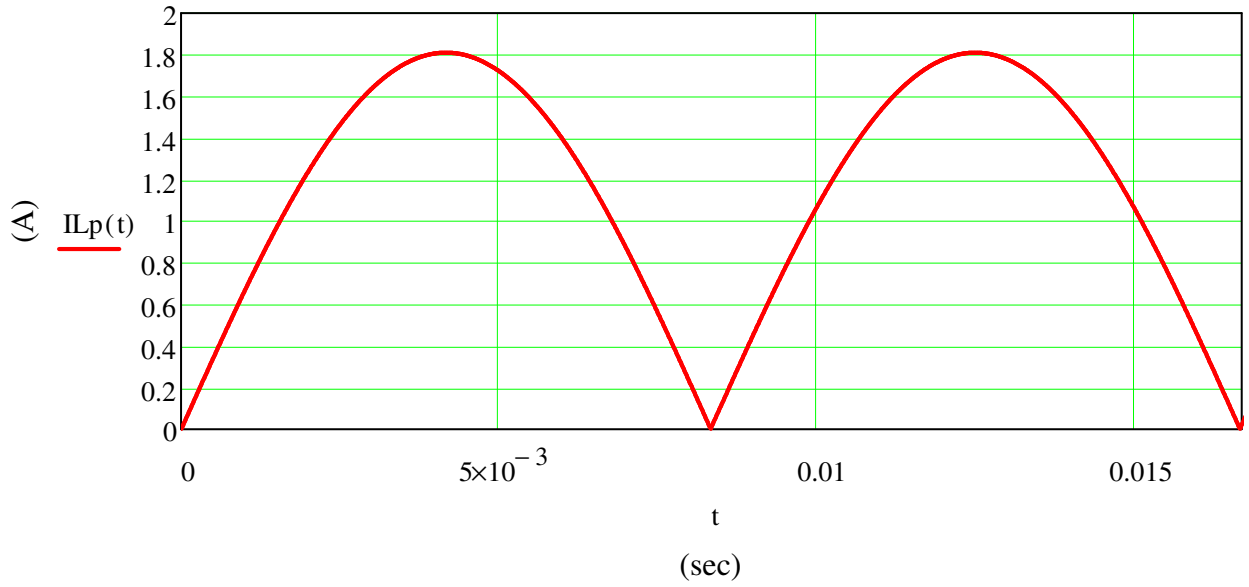
$$Toffmax := \frac{ILpk\cdot Lp}{Vout - Vinpk}$$ $Toffmax = 1.202\times 10^{-5}\,s$

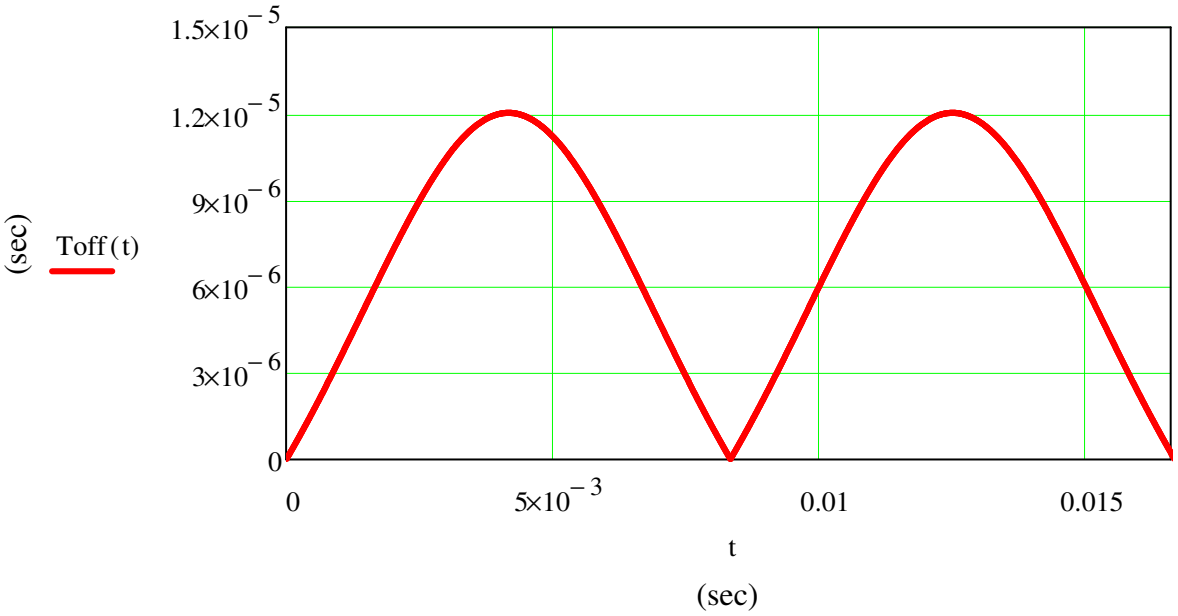
$$WL := \frac{1}{2}Lp\cdot ILpk^2$$ $WL = 6.082\times 10^{-3}\,J$

$$Ttotal := \frac{\sqrt{2}\cdot Pout\cdot Lp\cdot Vout}{Vinmin^2\cdot\eta\cdot\left(\frac{Vout}{\sqrt{2}} - Vinmin\right)}$$ $Ttotal = 4\times 10^{-5}\,s$

$$fsmin := \frac{Vinmin\cdot\left(Vout - \sqrt{2}\,Vinmin\right)}{2Lp\cdot Iinrms\cdot Vout}$$ $fsmin = 2.5\times 10^4\,\frac{1}{s}$

$$ILp(t) := \frac{\left|\frac{Vinmin}{Lp}\cdot Tonmax\cdot\sin(\omega\cdot t)\right|}{\sqrt{2}}$$





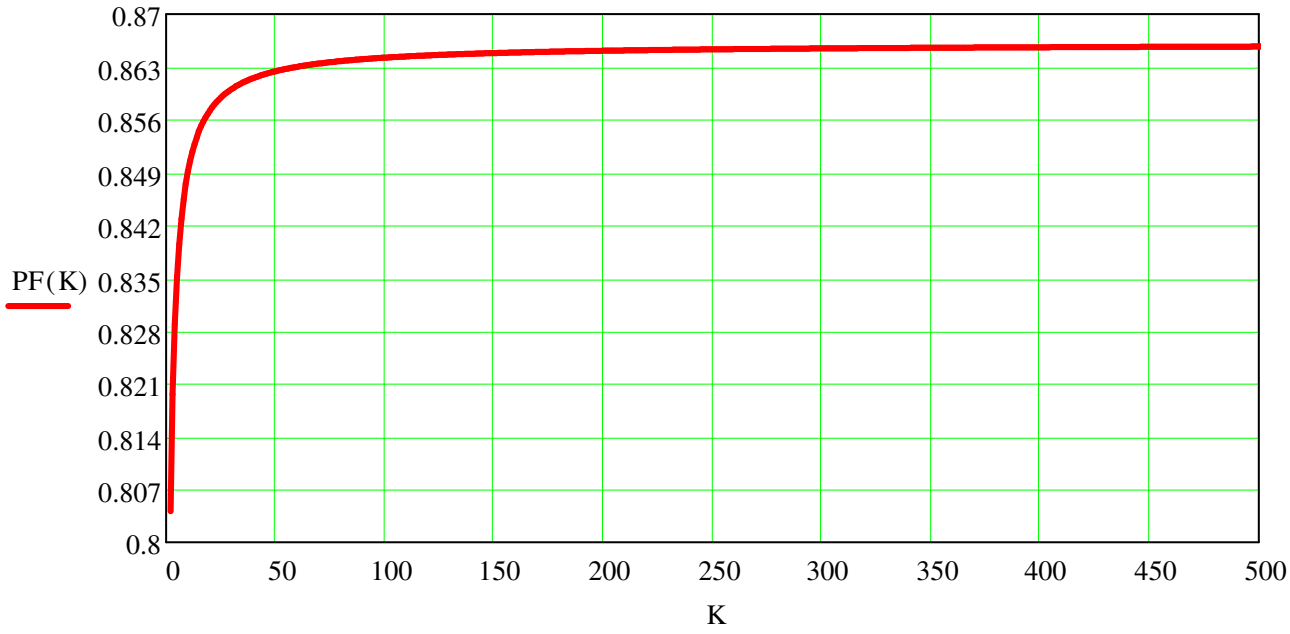
Calculate the PF with K factor

$K := 2 .. 1000$

$IL := \frac{2}{\sqrt{3}} Iinrms \qquad IL = 1.477\,A$

$IL1 := \frac{1}{\sqrt{6}} ILpk = 1.477\,A$

$PF(K) := \frac{\sqrt{2}\,ILpk \cdot \left(\frac{\pi}{4} + K\right)}{4(1+K) \cdot IL}$



Calculate the Input Capacitor

Select a attenuate rate=10%

$$\text{Atte\_rate} := 10\% \qquad \text{Req} := \frac{\text{Vinmin}}{\text{Iinrms}} = 66.47\,\Omega$$

$$\text{Cin} := \frac{1}{[\text{Atte\_rate}\cdot(2\pi\cdot\text{Req}\cdot\text{fs})]} = 9.578\times10^{-7}\,\text{F}$$

Select a 0.63uF Capacitor

EMI Filter Performance and Specification:

$\text{DPF} := 0.98$

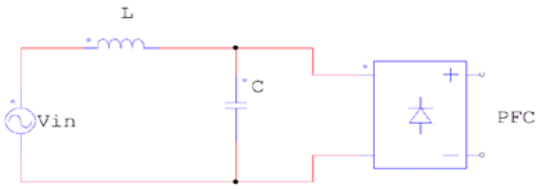
$\text{fc} := 5\text{KHz}$ Cut-off Frequency

EMI Filter Design 1: L-C Filter

$\text{Im} := \text{Iinpk} = 1.808\,\text{A}$

$\text{Vm} := \text{Vinmin}\cdot\sqrt{2} = 120.208\,\text{V}$

$\omega = 376.991\,\frac{1}{\text{s}}$



$$C_{max} := \frac{\text{Im}}{\omega\cdot\text{Vm}}\cdot\tan(\text{acos}(\text{DPF})) = 8.103\times10^{-6}\,\text{F}$$

$$\text{L} := \frac{1}{\text{fc}^2\cdot C_{max}\cdot(2\pi)^2} = 1.25\times10^{-4}\,\text{H}$$

$$Zin := \frac{Vinmin^2 \cdot \eta}{Pout} = 66.47\,\Omega$$

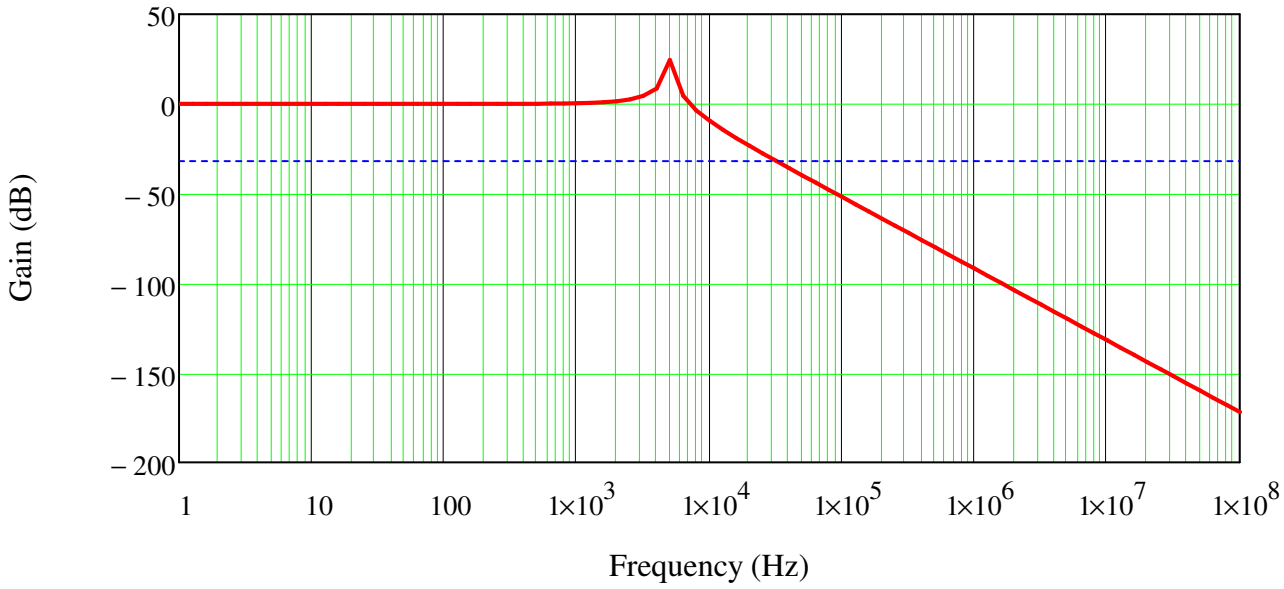
$j := 0 .. 80$ $\quad L_1 := 1.25 \times 10^{-4}$ $\quad Z_{in} := \frac{Zin}{\Omega} = 66.47$ $\quad f(j) := 10^{\left(\frac{j}{10}\right)}$

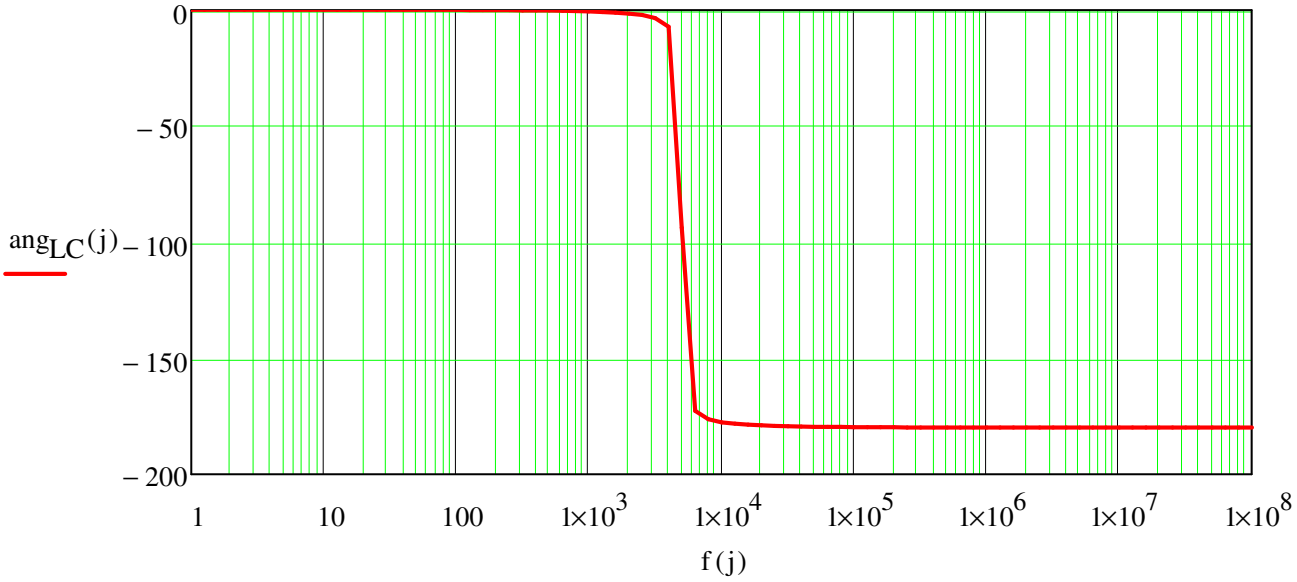
$s(j) := 2\pi f(j) \cdot \sqrt{-1}$ $\quad C_1 := 8.1 \times 10^{-6}$ $\quad C_2 := 4C_1 = 3.24 \times 10^{-5}$

$$T_{LC}(j) := \left(\frac{1}{1 + s(j)\frac{L_1}{Z_{in}} + L_1 \cdot C_1 \cdot s(j)^2} \right)$$

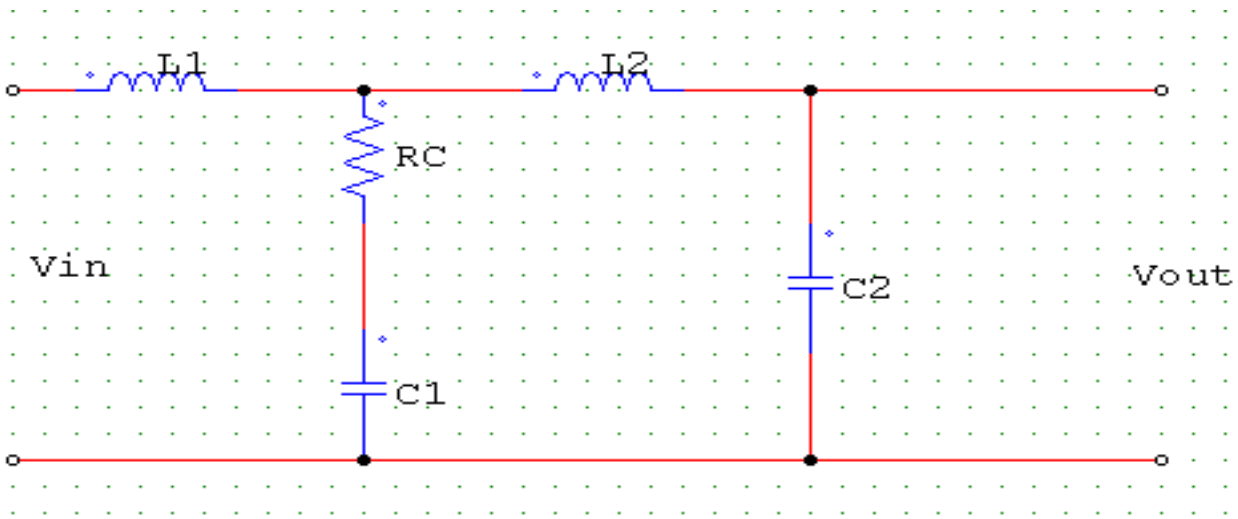
$$mag_{LC}(j) := 20\log\left(\left| T_{LC}(j) \right| \right)$$

$$ang_{LC}(j) := \frac{180}{\pi} \arg\left(T_{LC}(j) \right)$$





Damping Filter:



$$Zout := \frac{Zin}{2} = 33.235\,\Omega$$

$$Attn := 100$$

$$Attn\_rate := 20 \cdot \log(Attn) = 40 \quad \textbf{dB}$$

$$F_{filter} := \frac{fs}{\sqrt{Attn}} = 2.5 \times 10^3 \frac{1}{s}$$

$$C1 := C_{max} \qquad R_D := \sqrt{\frac{L}{C1}} = 3.928\,\Omega$$

$$C2 := 4C1 = 3.241 \times 10^{-5}\,F$$

$$RD := \frac{R_D}{\Omega} = 3.928$$

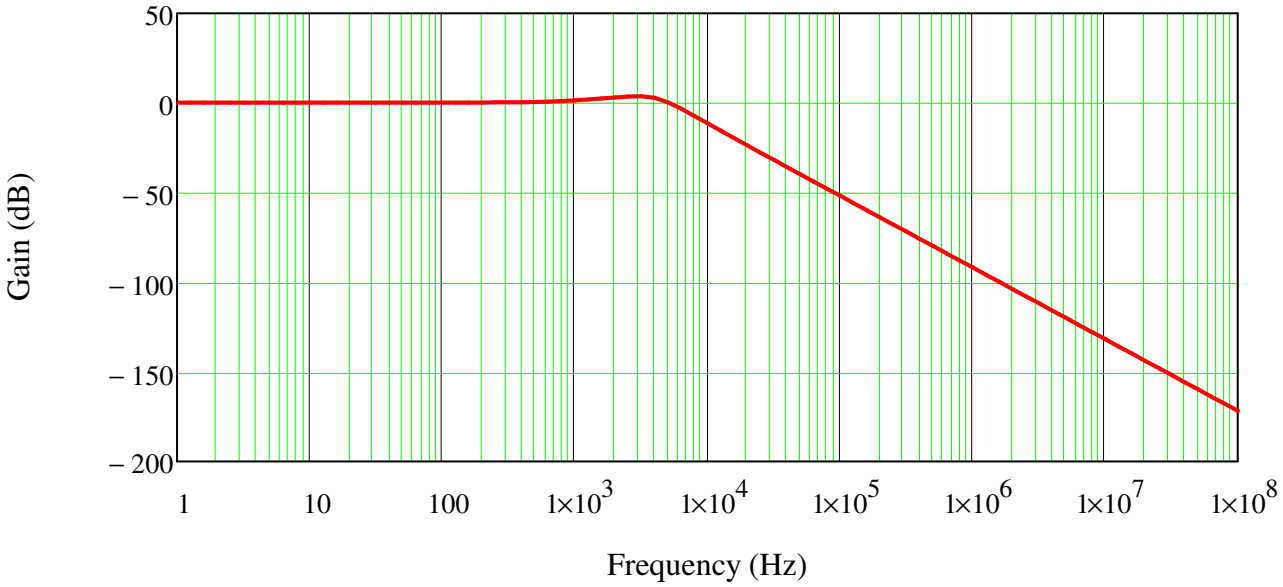
$$Zin = 66.47\,\Omega$$

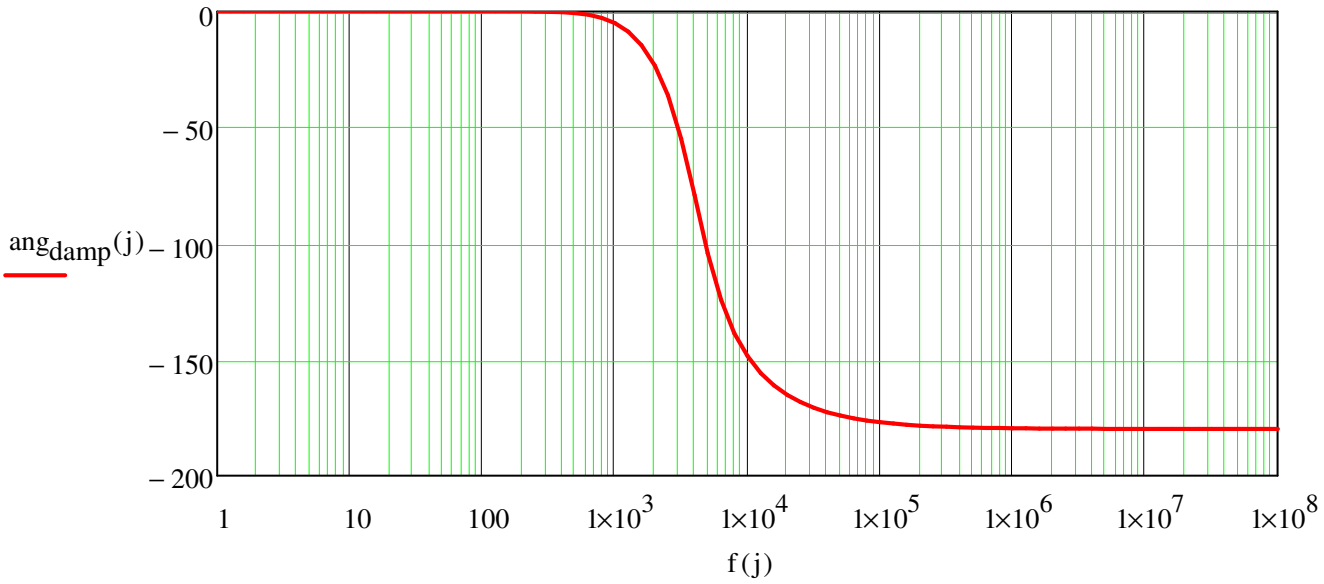
$$T_{damp}(j) := \frac{1 + RD \cdot s(j)\, C_2}{1 + s(j) \cdot C_2 \cdot RD + L_1 \cdot (C_1 + C_2)\, s(j)^2 + L_1 \cdot RD \cdot C_1 \cdot C_2 \cdot s(j)^3}$$

$$mag_{damp}(j) := 20\log\left(\left|T_{damp}(j)\right|\right)$$

$$ang_{damp}(j) := \frac{180}{\pi}\arg\left(T_{damp}(j)\right)$$

$$Z0 := \sqrt{\frac{L_1}{C_1}} = 3.928$$





$C1 := 2.2 \cdot \mu F$ $\quad C2 := \frac{C1}{8} = 2.75 \times 10^{-7} F$ $\quad C1 + C2 = 2.475 \times 10^{-6} F$

$$Amin := 20 \log\left(\frac{1000 Iinrms}{A} \cdot \frac{100\Omega}{\Omega}\right) - 72 = 30.136$$

$$V_{DM} := 72 + Amin$$

$$L2 := \frac{1}{4\pi^2 (fs)^2 C2} \cdot 10^{\left(\frac{-Amin+20}{30}\right)} = 6.77 \times 10^{-5} H \qquad L1 := 8L2$$

$L1 = 5.416 \times 10^{-4} H$ $\quad L2 = 6.77 \times 10^{-5} H$ $\quad Rd := \sqrt{\frac{L1}{1.5C1}} = 12.811\,\Omega$

$C1 = 2.2 \times 10^{-6} F$ $\quad C2 = 2.75 \times 10^{-7} F$

$$Wz1 := \frac{1}{Rd \cdot C1} = 3.548 \times 10^4 \frac{1}{s} \qquad Wo1 := \frac{1}{\sqrt{L1 \cdot C1}} = 2.897 \times 10^4 \frac{1}{s} \qquad L_1 := \frac{L1}{H} \qquad L_2 := \frac{L2}{H}$$

$$Wz2 := \frac{Rd}{L2} = 1.892 \times 10^5 \frac{1}{s} \qquad Wo2 := \frac{1}{\sqrt{L2 \cdot C2}} = 2.318 \times 10^5 \frac{1}{s} \qquad C_1 := \frac{C1}{F} \qquad C_2 := \frac{C2}{F}$$

$$fo1 := \frac{Wo1}{2\pi} = 4.611 \times 10^3 \frac{1}{s} \qquad fo2 := \frac{Wo2}{2\pi} = 3.689 \times 10^4 \frac{1}{s} \qquad Z_{01} := \sqrt{\frac{L1}{C1}} = 15.69\,\Omega$$

$$fz1 := \frac{Wz1}{2\pi} = 5.647 \times 10^3 \frac{1}{s} \qquad fz2 := \frac{Wz2}{2\pi} = 3.012 \times 10^4 \frac{1}{s} \qquad Z_{02} := \sqrt{\frac{L2}{C2}} = 15.69\,\Omega$$

$$f_{o1} := Wo1 \cdot sec = 2.897 \times 10^4 \qquad f_{z1} := Wz1 \cdot sec = 3.548 \times 10^4 \qquad Q1 := \frac{Z_{01}}{Rd} = 1.225$$

$$f_{o2} := Wo2 \cdot sec = 2.318 \times 10^5 \qquad f_{z2} := Wz2 \cdot sec = 1.892 \times 10^5 \qquad Q2 := \frac{Z_{02}}{Rd} = 1.225$$

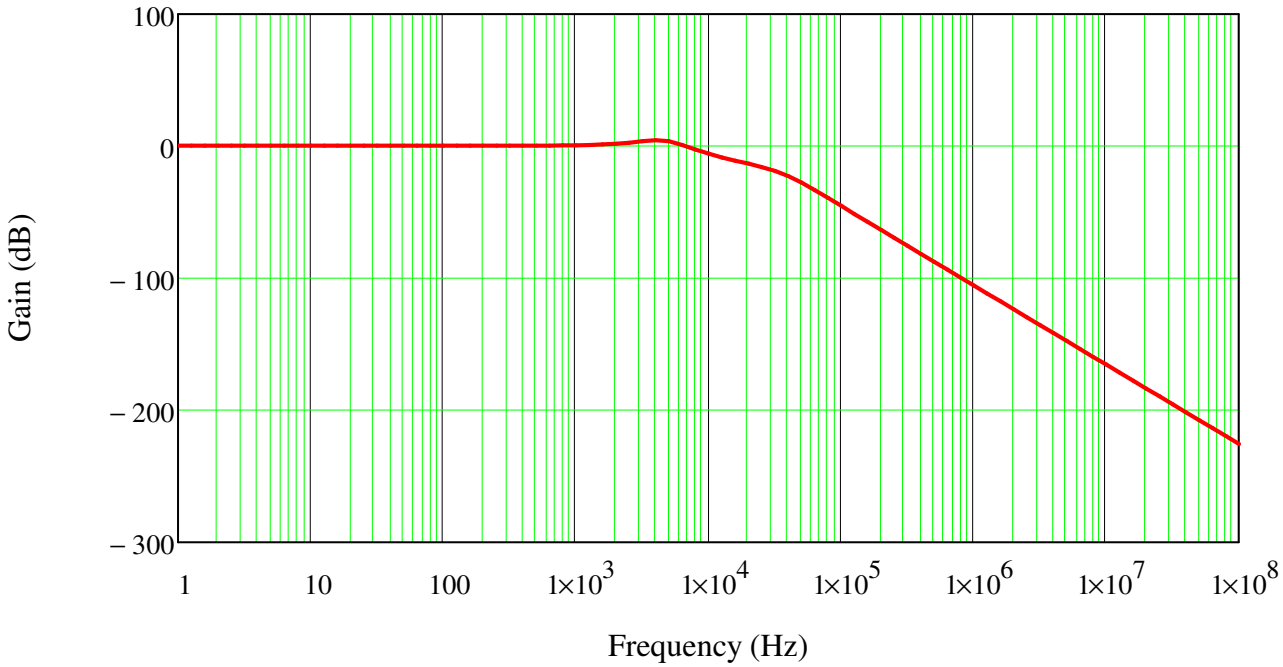
$$Gs(j) := \left[\frac{1 + \frac{s(j)}{f_{z1}}}{\left(\frac{s(j)^2}{f_{o1}^2} + \frac{s(j)}{f_{z1}} + 1 \right) \cdot \left(\frac{s(j)^2}{f_{o2}^2} + \frac{s(j)}{f_{z2}} + 1 \right)} \right] \qquad Q_1 := Q1 \qquad Q_2 := Q2$$

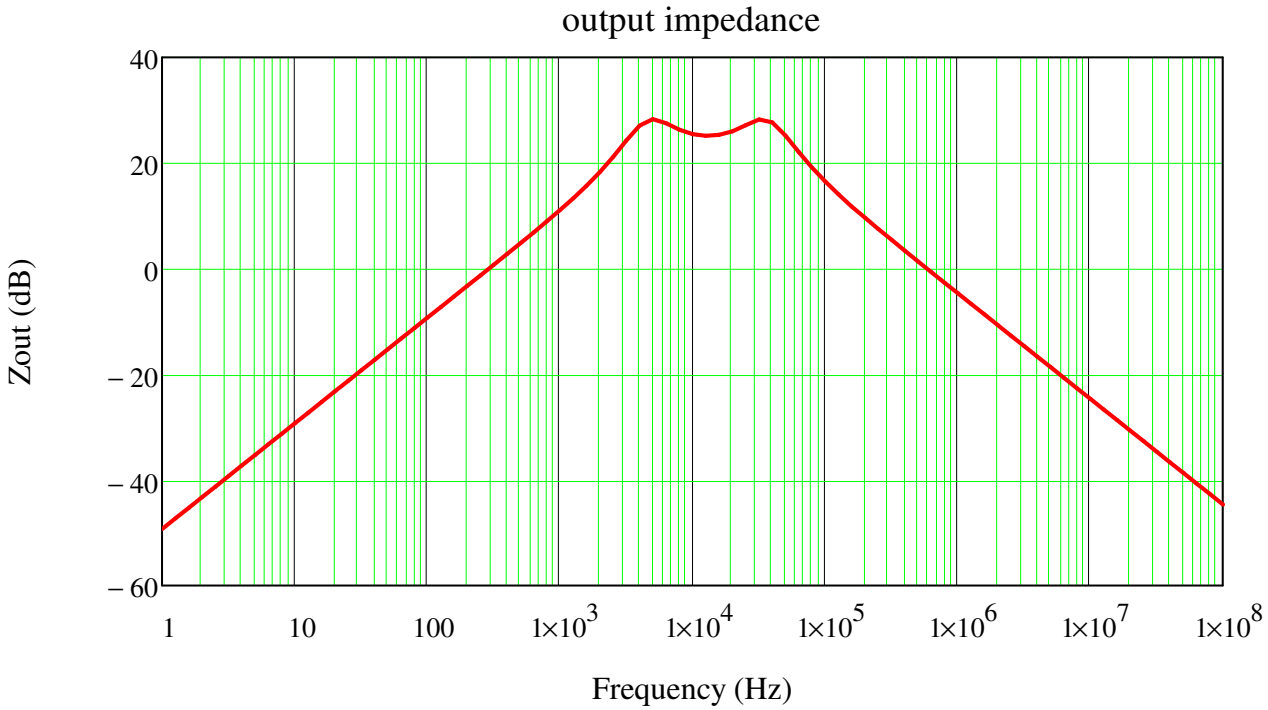
$$mag_{Gs}(j) := 20\log\left(|Gs(j)| \right)$$

$$ang_{Gs}(j) := \frac{180}{\pi} \arg(Gs(j))$$

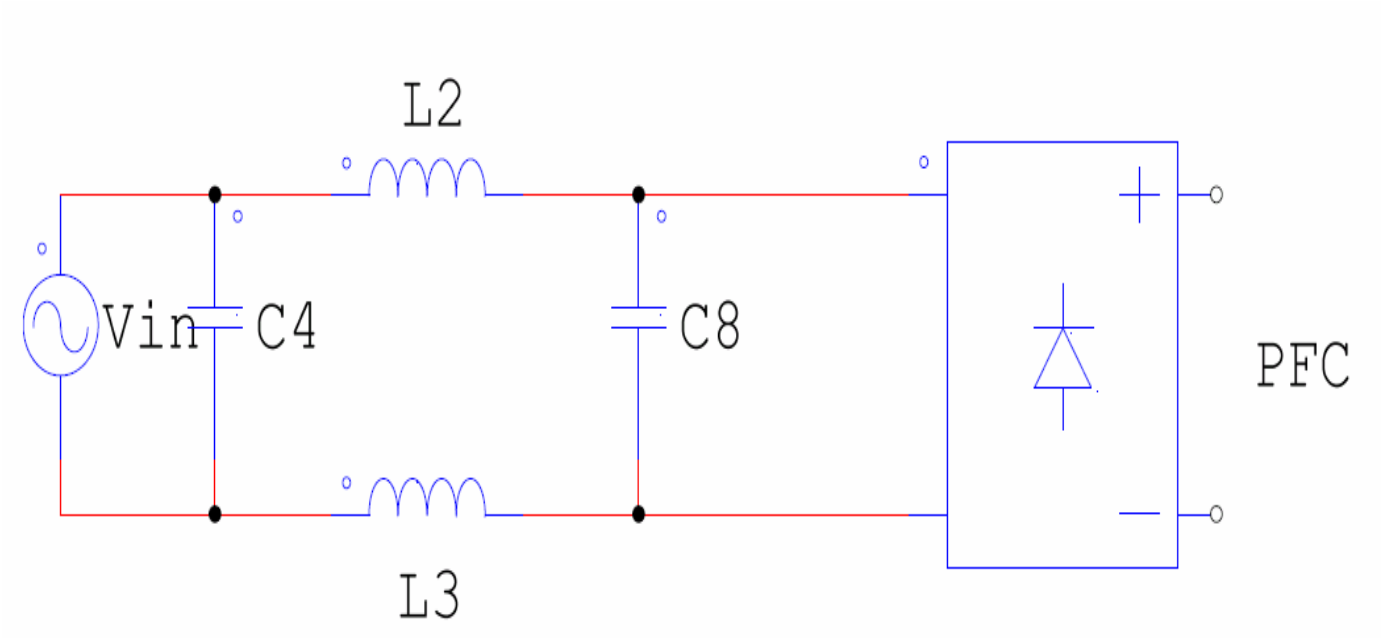
$$Zsout(j) := \frac{s(j) \cdot L_1 \cdot \left(1 + \frac{s(j)}{f_{z1}} \right) \cdot \left(1 + \frac{s(j)}{f_{z2}} \right)}{\left(\frac{s(j)^2}{f_{o1}^2} + \frac{s(j)}{Q_1 \cdot f_{o1}} + 1 \right) \cdot \left(\frac{s(j)^2}{f_{o2}^2} + \frac{s(j)}{Q_2 \cdot f_{o2}} + 1 \right)}$$

$$Zsout(j) := 20\log\left(|Zsout(j)| \right)$$


100
0
– 100
– 200
– 300
Gain (dB)
1
10
100
1×10^3
1×10^4
1×10^5
1×10^6
1×10^7
1×10^8
Frequency (Hz)


output impedance
40
20
0
– 20
– 40
– 60
Zout (dB)
1
10
100
1×10^3
1×10^4
1×10^5
1×10^6
1×10^7
1×10^8
Frequency (Hz)

Standard DM Filter Design:



$fp := 25KHz$

$$L_2 := \frac{(Vinmin \cdot \sqrt{2} - Vdrop) \cdot Ton}{\left(\frac{Pout \cdot \sqrt{2}}{\eta \cdot Vinmin}\right)} = 5.447 \times 10^{-4} H$$

$$L_3 := L_2 = 5.447 \times 10^{-4} H$$

$$C_4 := \frac{1}{(2\pi \cdot fp)^2 \cdot L_2} = 7.44 \times 10^{-8} F$$

$$C_8 := C_4 = 7.44 \times 10^{-8} F$$

Output Capacitor Selection:

$\Delta U := Pout \cdot t\_hold$ $\quad \Delta U = 4\,J$

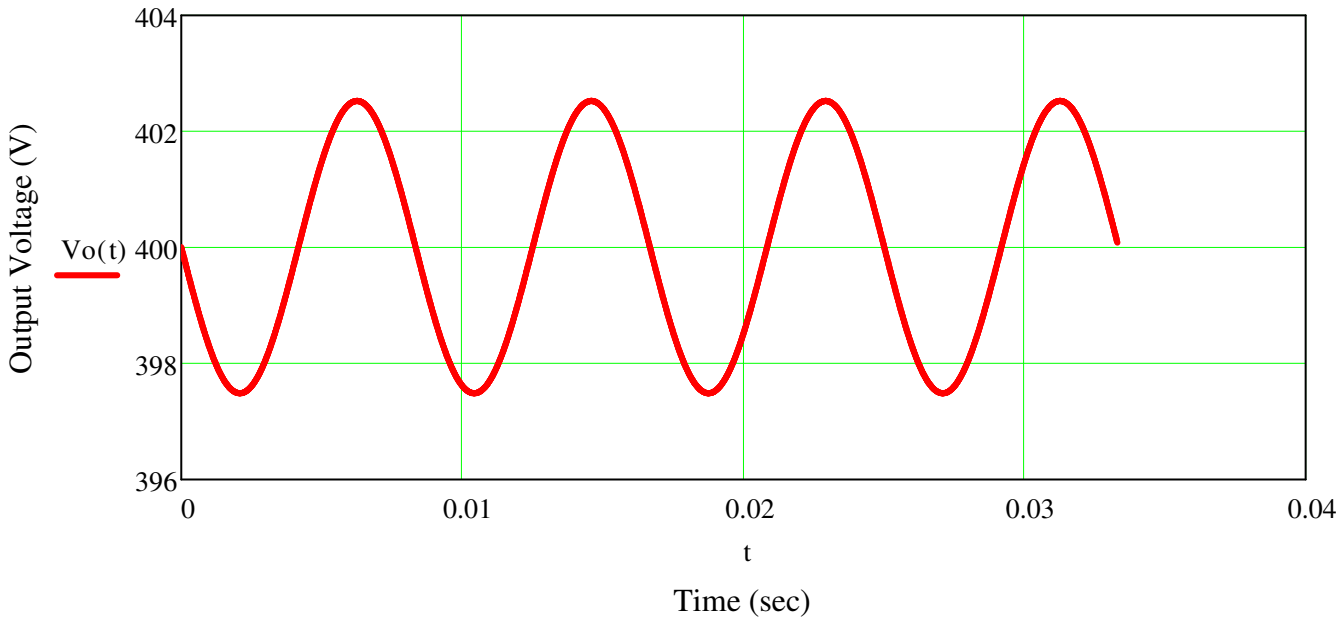
$$Cout := \frac{2 \cdot \Delta U}{Vout^2 - (Vout - Vdrop)^2} \qquad Cout = 1.316 \times 10^{-4}\,F$$

$$Irmscout := \frac{Pout}{Vout} \cdot \sqrt{\frac{16.Vout}{3\pi \cdot Vinmin \cdot \sqrt{2}} - 1} \qquad Irmscout = 0.539\,A$$

$$VOripple(t) := \frac{\eta \cdot Pin \cdot \sin(2\omega \cdot t)}{Cout \cdot \omega \cdot Vout \cdot 2}$$

$$Vout\_ripple := \frac{\eta \cdot (Pin)}{Cout \cdot \omega \cdot Vout} = 5.038\,V \qquad Vout\_ripple = 5.038\,V$$

$Vo(t) := Vout - VOripple(t)$



MOSFET Power Losses Analysis:

MTP8N50E: 500V,8A

Rds(on)~1.75Ω@100 dgree

$C_{oss} := 190pF$

$Q_{gate} := 40nC$

$tr := 33ns$

$Rd_{con} := 1.75\Omega$

$V_{gate} := 10V$

$Rdson := 1.75\Omega$

$$Irms\_FET := \frac{Pout \cdot 2\sqrt{2}}{\eta \cdot Vinmin} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2}\,Vinmin}{9\pi \cdot Vout}} = 1.274\,A$$

$$IL1_{rms} := \frac{Pout}{\eta \cdot Vinmin \cdot \sqrt{2}} = 0.904\,A \qquad IL_{rms} := \frac{2}{\sqrt{3}} \cdot \frac{Pin}{Vinmin} = 1.477\,A$$

$$PMcond := \frac{4}{3} \cdot Rdson \cdot \left(\frac{Pin}{Vinmin}\right)^2 \cdot \left[1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vinmin}{3\pi\, Vout}\right)\right] = 2.842\,W$$

$$P_{gate\_loss} := Q_{gate} \cdot V_{gate} \cdot fs = 0.01\,W$$

$$P_{coss\_loss} := \frac{1}{2} \cdot C_{oss} \cdot Vout^2 \cdot fs = 0.38\,W$$

$$P_{cond\_loss} := \frac{4}{3} \cdot Rd_{con} \cdot \left(\frac{Pin}{Vinmin}\right)^2 \cdot \left[1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vinmin}{3\pi\, Vout}\right)\right] = 2.842\,W$$

$$P_{FET\_tr} := \frac{1}{2} \cdot Vout \cdot IL_{rms} \cdot tr \cdot fs = 0.244\,W$$

$$P_{FET\_loss} := P_{gate\_loss} + P_{coss\_loss} + P_{cond\_loss} + P_{FET\_tr} = 3.476\,W$$

Diode Conduction Losses:

$V_{F\_diode} := 0.7 \cdot V$ (MUR460)

$$IDrms := \frac{4}{3} \cdot \frac{\sqrt{2 \cdot \sqrt{2}}}{\pi} \cdot \frac{Pin}{\sqrt{Vinmin \cdot Vout}} = 0.421\,A$$

$$P_{Diode\_loss} := V_{F\_diode} \cdot IDrms = 0.295\,W \qquad PDcond\_loss := V_{F\_diode} \cdot IDrms = 0.295\,W$$

Current sense resistor Power losses:

Rcs : current sense resistor losses

Choose Rcs=0.68 ohm

$$Prcs := \frac{1}{6}\cdot Rcs\cdot ILpk^2$$

$$Prcs = 1.09\,W$$

$$P_{RS\_loss} := Rcs\cdot IL_{rms}^{\ 2} = 1.09\,W$$

Rectifier Power losses:

1N5406: VF=0.6V

$$V_{F\_rectifier} := 0.6V$$

$$Pbridger := 2V_{F\_rectifier}\cdot Iinrms = 1.535\,W$$

$$Pbridger = 1.535\,W$$

$$P_{Rectifier\_loss} := \frac{4\cdot\sqrt{2}\cdot Pout\cdot V_{F\_rectifier}}{\eta\cdot\pi\cdot Vinmin} = 1.382\,W$$

Inductor Power losses:

$$P_{L\_loss} := 0.82W$$

Output Capacitor Power losses:

Cout = 100uF,
ESR=1.44ohm

$$C_{out\_ESR} := 1.44\Omega$$

$$Icrms := \sqrt{\left(\frac{32\cdot\sqrt{2}\cdot Pin^2}{9\cdot\pi\cdot Vinmin\cdot Vout}\right) - \left(\frac{Vout}{Rout}\right)^2} = 0.703\,A$$

$$P_{Cout\_loss} := Icrms^2\cdot C_{out\_ESR} = 0.711\,W$$

Total Dissipation Power losses:

$$Pall\_diss := PMcond + PDcond\_loss + Prcs + Pbridger + P_{Cout\_loss} \qquad Pall\_diss = 6.472\,W$$

$$\eta cal := \frac{Pout}{Pout + Pall\_diss} = 0.939$$

$$P_{Total\_loss} := P_{FET\_loss} + P_{Diode\_loss} + P_{RS\_loss} + P_{Rectifier\_loss} + P_{L\_loss} + P_{Cout\_loss} = 7.773\,W$$

$$\eta_{cal} := \frac{Pout}{Pout + P_{Total\_loss}} = 0.928$$

Input Voltage VS Power Losses:

$f := 60Hz$ $\qquad i := 0..36$

$Vout_i := 400V$

$Vinrms_i := Vinmin + i \cdot 5V$ $\qquad Pout_i := 100W$

$$Pin := \frac{Pout}{\eta}$$

$$Vinpk := Vinrms \cdot \sqrt{2}$$

$$Fswmin_i := \frac{(Vinpk_i \cdot Vinpk_i) \cdot (Vout_i - Vinpk_i)}{4(Vout_i \cdot Pin_i \cdot Lp)}$$

$$Iinrms := \frac{Pin}{Vinrms}$$

$Vinrms =$

	0
0	85
1	90
2	95
3	100
4	105
5	110
6	115
7	120
8	125
9	130
10	135
11	140
12	145
13	150
14	155
15	...

V

$$Iinpk := Iinrms \cdot \sqrt{2}$$

$$I1rms := \frac{2}{\sqrt{3}} \cdot Iinrms$$

$$MOSrms_i := I1rms_i \cdot \sqrt{1 - \frac{(8 \cdot \sqrt{2}\, Vinrms_i)}{3\pi \cdot Vout_i}}$$

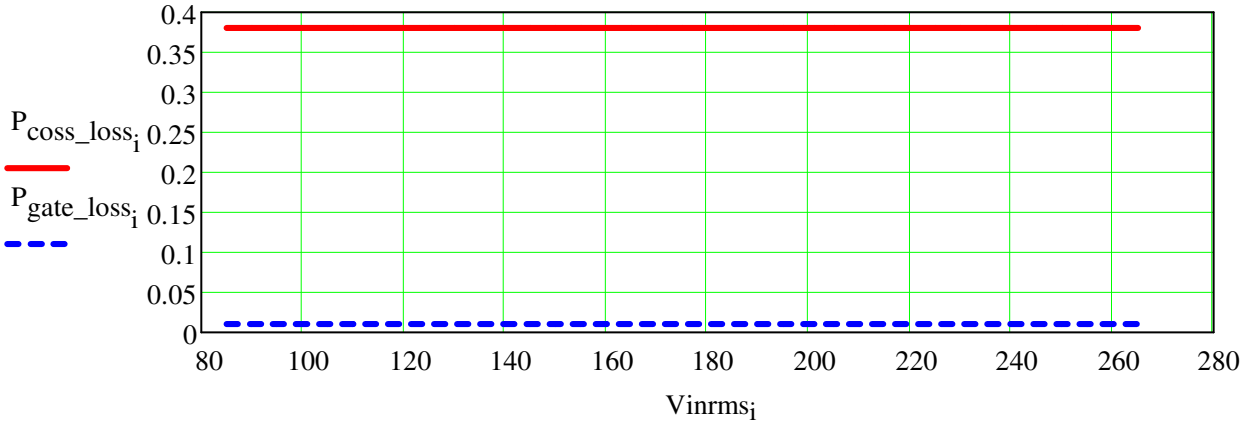
MTP8N50E: 500V,8A

Rds(on)~1.75Ω@100 dgree

$V_{gate_i} := 10V$ $\quad ILrms := \frac{2}{\sqrt{3}} \cdot \frac{Pin}{Vinrms}$

$P_{coss\_loss_i} := \frac{1}{2} \cdot C_{oss} \cdot (Vout_i)^2 \cdot fs$

$P_{gate\_loss} := Q_{gate} \cdot V_{gate} \cdot fs$

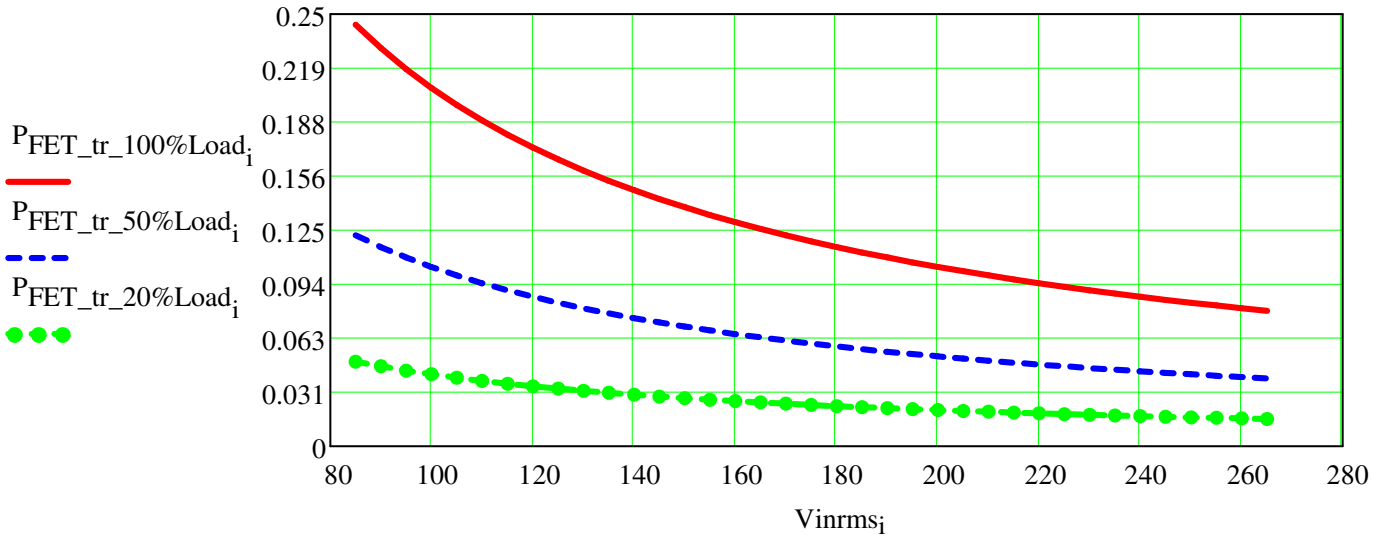


$P_{FET\_tr_i} := \frac{1}{2} \cdot fs \cdot (Vout_i \cdot ILrms_i \cdot tr)$

$P_{FET\_tr\_100\%Load_i} := \frac{1}{2} \cdot fs \cdot (Vout_i \cdot ILrms_i \cdot tr)$

$P_{FET\_tr\_50\%Load_i} := \frac{1}{2} \cdot fs \cdot \left(Vout_i \cdot \frac{ILrms_i}{2} \cdot tr\right)$

$P_{FET\_tr\_20\%Load_i} := \frac{1}{2} \cdot fs \cdot \left(Vout_i \cdot \frac{ILrms_i}{5} \cdot tr\right)$

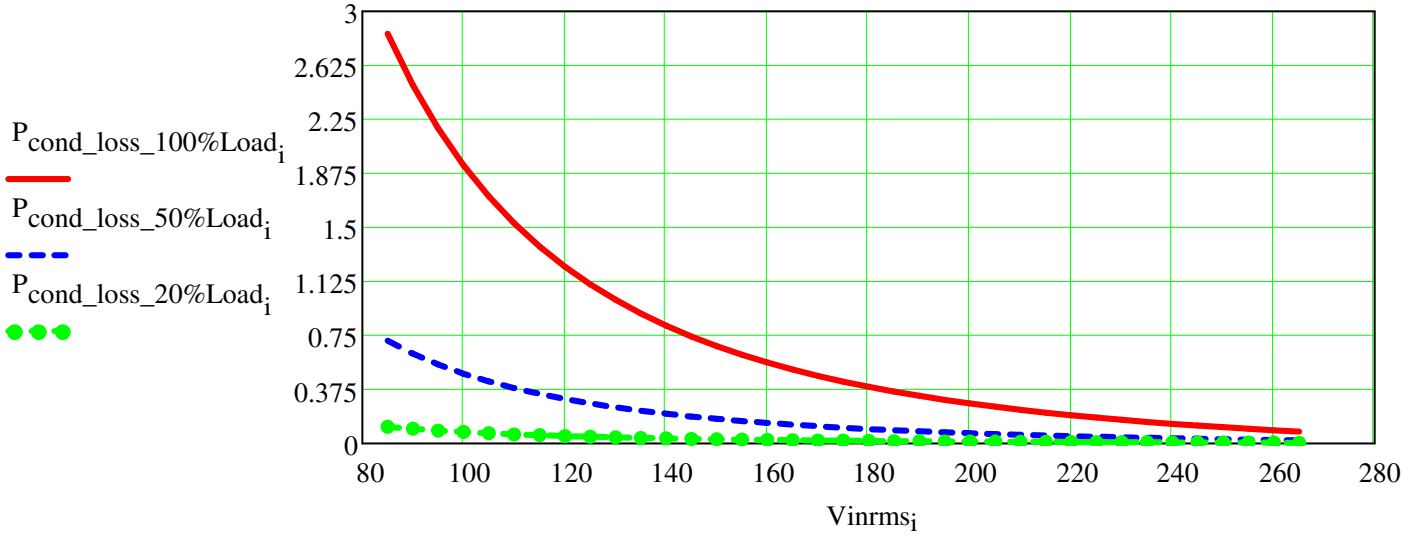

$P_{FET\_tr\_100\%Load_i}$
$P_{FET\_tr\_50\%Load_i}$
$P_{FET\_tr\_20\%Load_i}$
0.25
0.219
0.188
0.156
0.125
0.094
0.063
0.031
0
80
100
120
140
160
180
200
220
240
260
280
$Vinrms_i$

$$P_{cond\_loss_i} := \frac{4}{3}\cdot Rd_{con}\cdot\left(\frac{Pin_i}{Vinrms_i}\right)^2\cdot\left[1-\left(\frac{8\cdot\sqrt{2}\cdot Vinrms_i}{3\pi\, Vout_i}\right)\right] = \ldots$$

$$P_{cond\_loss\_100\%Load_i} := \frac{4}{3}\cdot Rd_{con}\cdot\left(\frac{Pin_i}{Vinrms_i}\right)^2\cdot\left[1-\left(\frac{8\cdot\sqrt{2}\cdot Vinrms_i}{3\pi\, Vout_i}\right)\right]$$

$$P_{cond\_loss\_50\%Load_i} := \frac{4}{3}\cdot Rd_{con}\cdot\left(\frac{\frac{Pin_i}{2}}{Vinrms_i}\right)^2\cdot\left[1-\left(\frac{8\cdot\sqrt{2}\cdot Vinrms_i}{3\pi\, Vout_i}\right)\right]$$

$$P_{cond\_loss\_20\%Load_i} := \frac{4}{3}\cdot Rd_{con}\cdot\left(\frac{\frac{Pin_i}{5}}{Vinrms_i}\right)^2\cdot\left[1-\left(\frac{8\cdot\sqrt{2}\cdot Vinrms_i}{3\pi\, Vout_i}\right)\right]$$

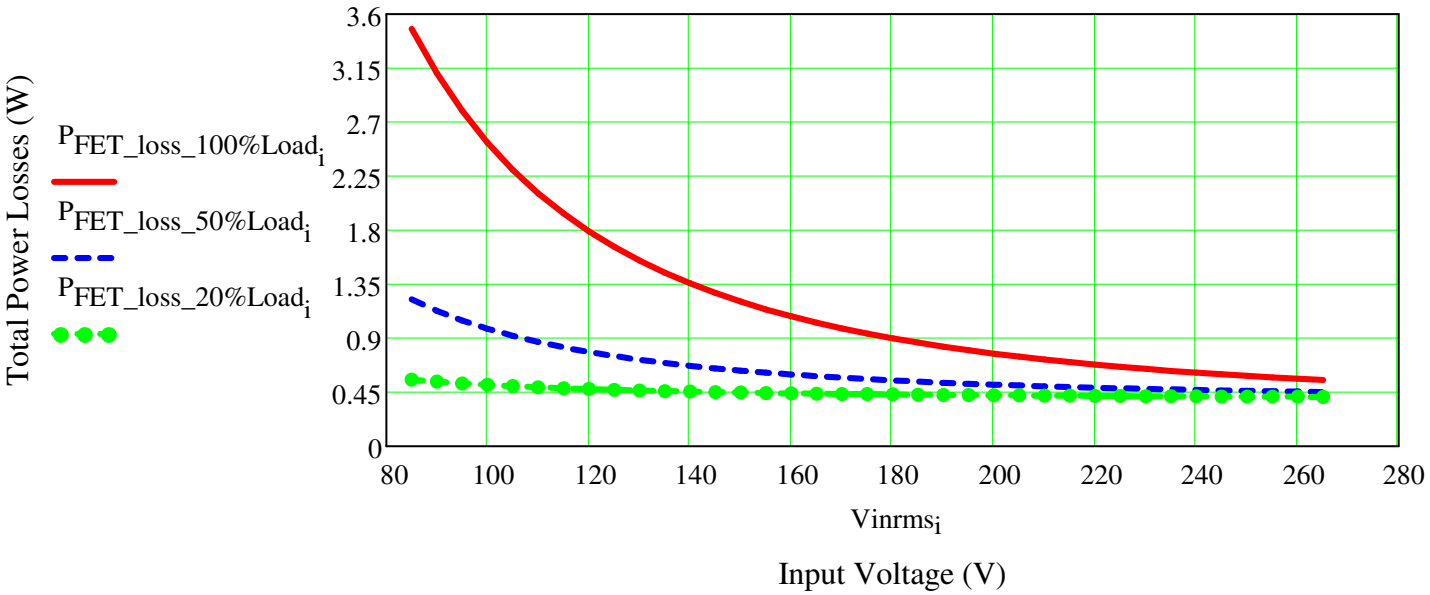


$$P_{FET\_loss} := P_{gate\_loss} + P_{coss\_loss} + P_{cond\_loss} + P_{FET\_tr}$$

$$P_{FET\_loss\_100\%Load_i} := P_{gate\_loss_i} + P_{coss\_loss_i} + P_{cond\_loss_i} + P_{FET\_tr_i}$$

$$P_{FET\_loss\_50\%Load_i} := P_{gate\_loss_i} + P_{coss\_loss_i} + \frac{P_{cond\_loss_i}}{4} + \frac{P_{FET\_tr_i}}{2}$$

$$P_{FET\_loss\_20\%Load_i} := P_{gate\_loss_i} + P_{coss\_loss_i} + \frac{P_{cond\_loss_i}}{25} + \frac{P_{FET\_tr_i}}{5}$$



Rectifier Power Losses:

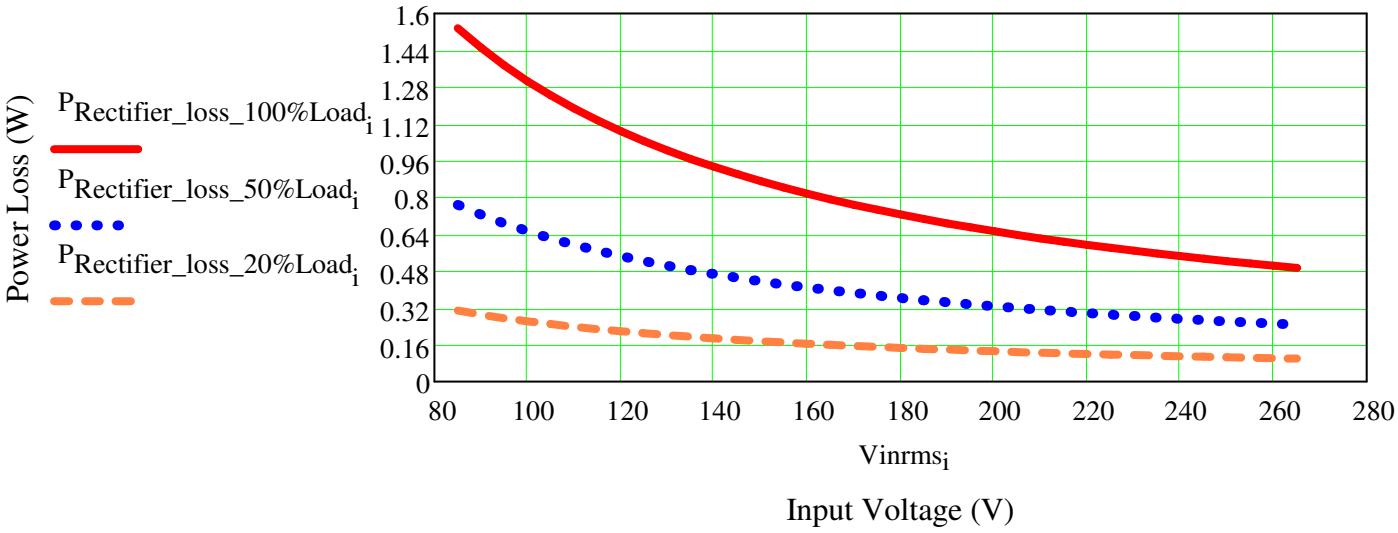
1N5406: VF=0.6V

$VF := 0.6V$

$$P_{Rectifier\_loss\_100\%Load_i} := 2VF \cdot Iinrms_i$$

$$P_{Rectifier\_loss\_50\%Load_i} := 2VF \cdot \frac{Iinrms_i}{2}$$

$$P_{Rectifier\_loss\_20\%Load_i} := 2VF \cdot \frac{Iinrms_i}{5}$$



Diode Power Losses:

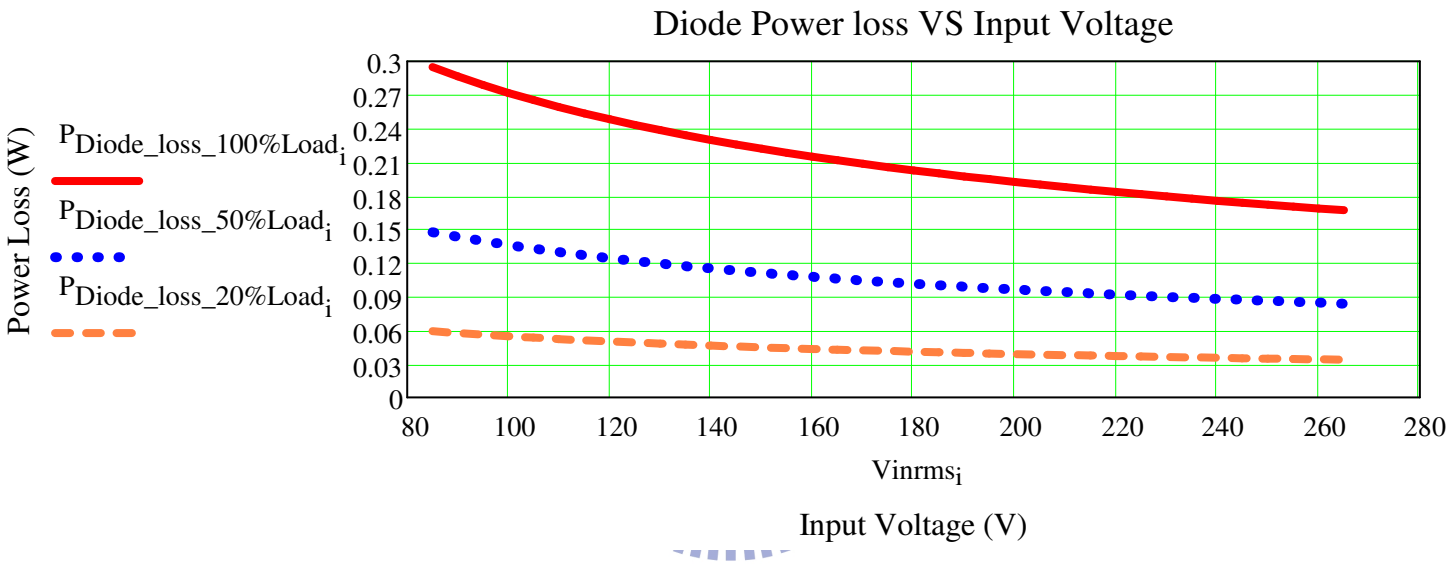
MUR460, VF=0.7V@ 100 dgree, IF=0.3A

$$ID1rms_i := \frac{4}{3}\cdot\frac{\sqrt{2\cdot\sqrt{2}}}{\pi}\cdot\frac{Pin_i}{\sqrt{Vinrms_i\cdot Vout_i}}$$

$$P_{Diode\_loss\_100\%Load_i} := ID1rms_i\cdot V_{F\_diode}$$

$$P_{Diode\_loss\_50\%Load_i} := \frac{ID1rms_i}{2}\cdot V_{F\_diode}$$

$$P_{Diode\_loss\_20\%Load_i} := \frac{ID1rms_i}{5}\cdot V_{F\_diode}$$



Current sense resistor Power loss:

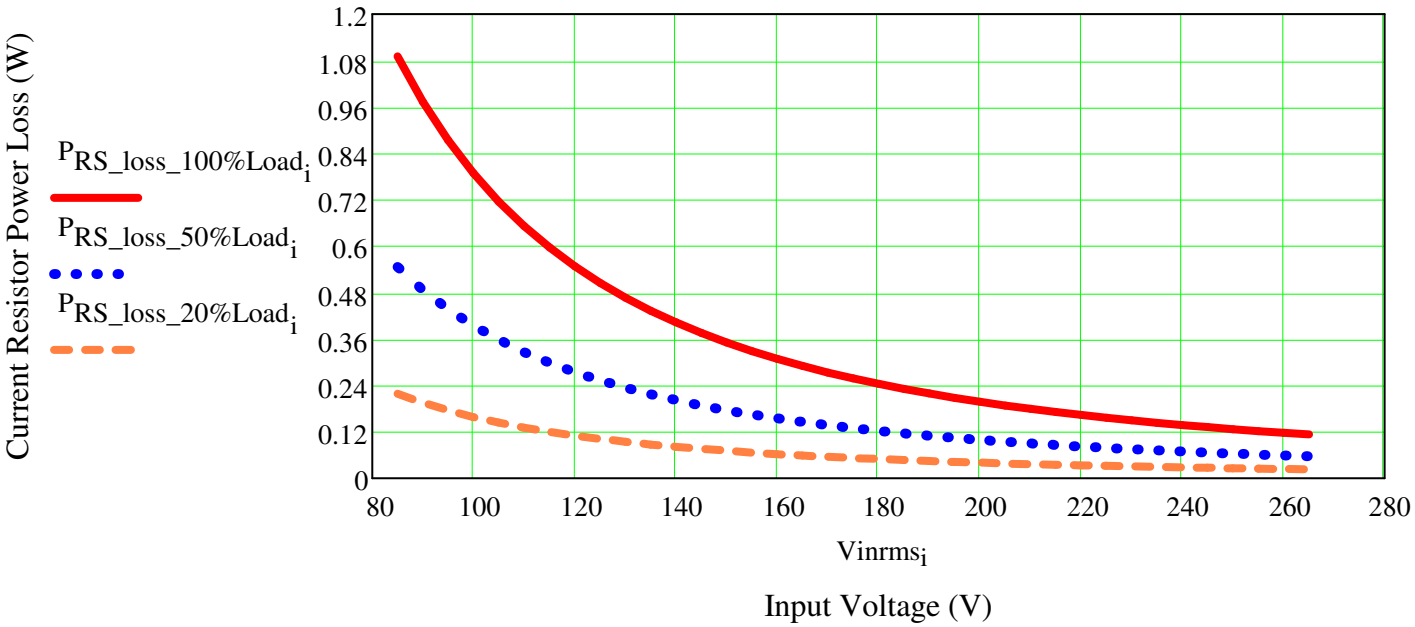
Rcs : current sense resistor losses

Choose Rcs=0.5 ohm

$$P_{RS\_loss\_100\%Load_i} := Rcs\cdot(ILrms_i)^2$$

$$P_{RS\_loss\_50\%Load_i} := \frac{Rcs\cdot(ILrms_i)^2}{2}$$

$$P_{RS\_loss\_20\%Load_i} := \frac{Rcs\cdot(ILrms_i)^2}{5}$$



Output Capacitor Power loss:

Cout_ESR=1.44 ohm

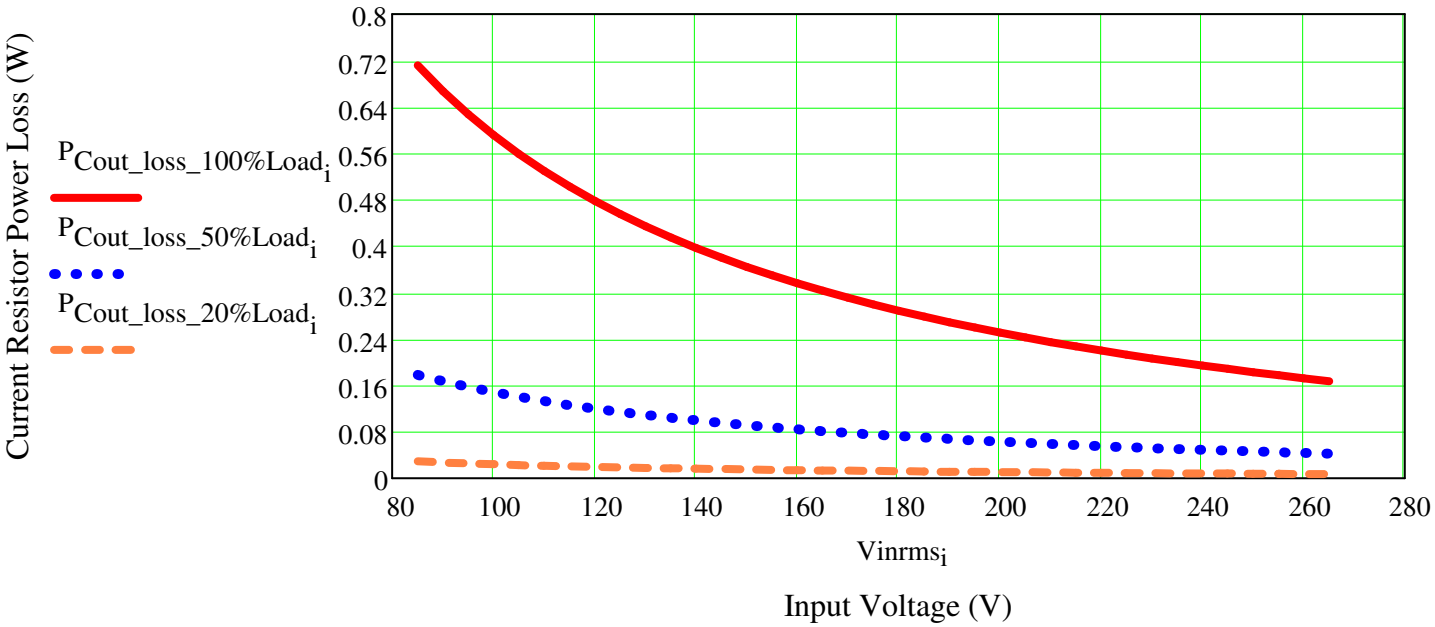
$$Vout := 400V$$

$$Ic_{rms} := \sqrt{\left[\frac{32\cdot\sqrt{2}\cdot\left(Pin^2\right)}{9\cdot\pi\cdot Vinrms\cdot Vout}\right] - \left(\frac{Vout}{Rout}\right)^2}$$

$$P_{Cout\_loss\_100\%Load_i} := C_{out\_ESR}\cdot\left(Ic_{rms_i}\right)^2$$

$$P_{Cout\_loss\_50\%Load_i} := C_{out\_ESR}\cdot\frac{\left(Ic_{rms_i}\right)^2}{4}$$

$$P_{Cout\_loss\_20\%Load_i} := C_{out\_ESR}\cdot\frac{\left(Ic_{rms_i}\right)^2}{25}$$


Current Resistor Power Loss (W)
$P_{Cout\_loss\_100\%Load_i}$
$P_{Cout\_loss\_50\%Load_i}$
$P_{Cout\_loss\_20\%Load_i}$
0.8
0.72
0.64
0.56
0.48
0.4
0.32
0.24
0.16
0.08
0
80
100
120
140
160
180
200
220
240
260
280
$Vinrms_i$
Input Voltage (V)

Total Power losses:

$$P_{Total\_loss} := P_{FET\_loss} + P_{Diode\_loss} + P_{RS\_loss} + P_{Rectifier\_loss} + P_{L\_loss} + P_{Cout\_loss}$$

$$\eta_{eal} := \frac{Pout}{Pout + P_{Total\_loss}}$$

$$P_{Total\_loss\_100\%Load} := P_{FET\_loss} + P_{Diode\_loss} + P_{RS\_loss} + P_{Rectifier\_loss} + P_{L\_loss} + P_{Cout\_loss}$$

$$P_{Total\_loss\_50\%Load1} := P_{FET\_loss\_50\%Load} + P_{Diode\_loss\_50\%Load} + P_{RS\_loss\_50\%Load}$$

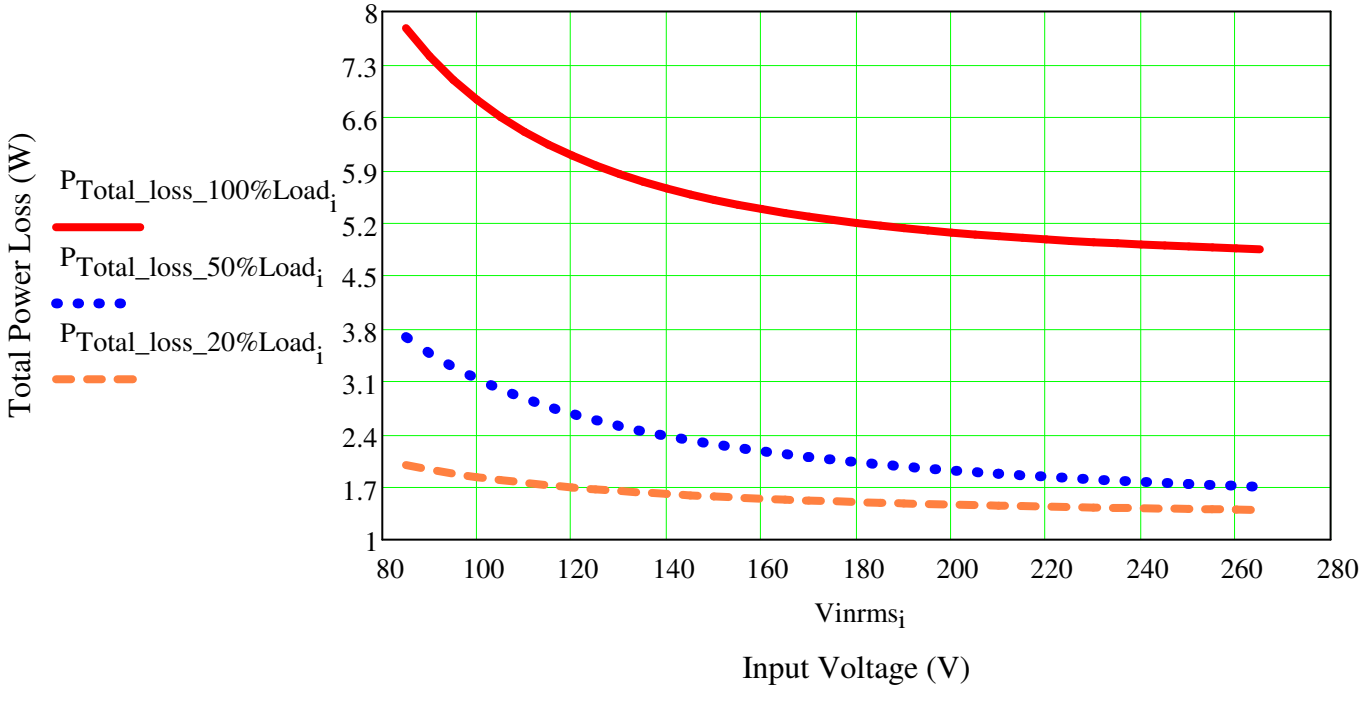
$$P_{Total\_loss\_50\%Load2} := P_{Rectifier\_loss\_50\%Load} + P_{L\_loss} + P_{Cout\_loss\_50\%Load}$$

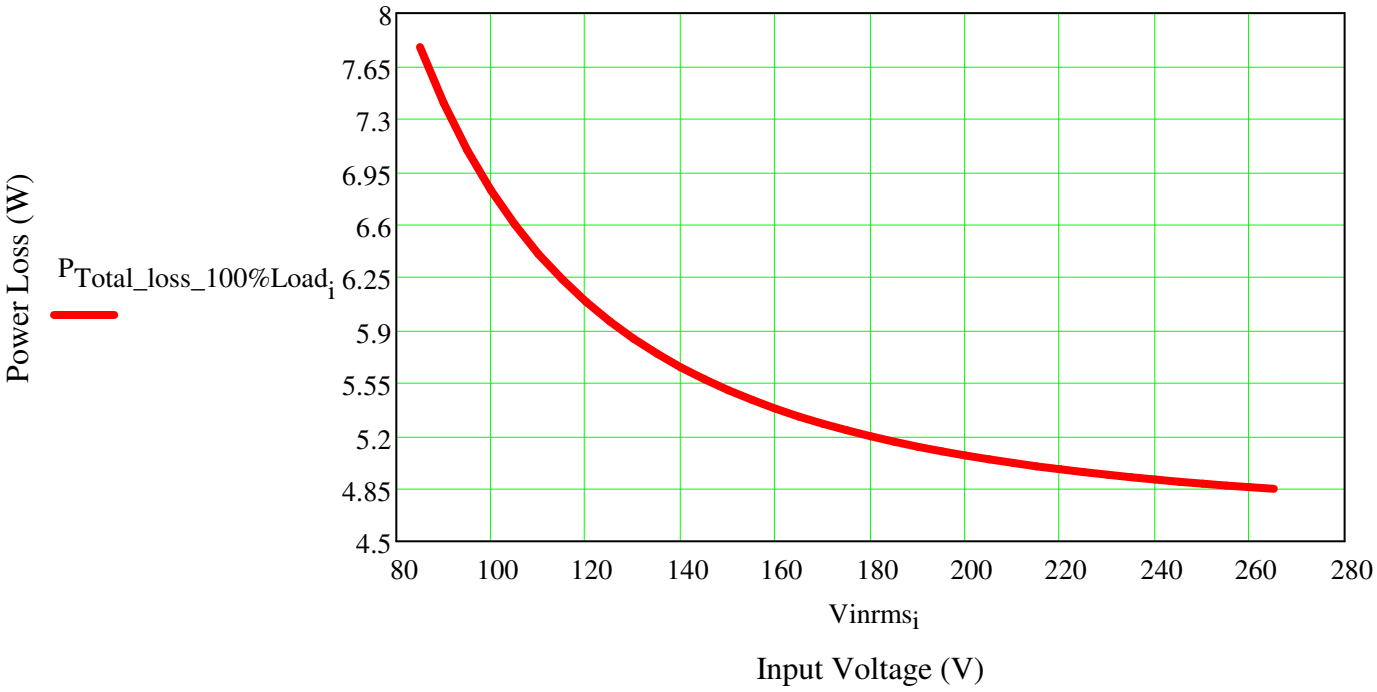
$$P_{Total\_loss\_50\%Load} := P_{Total\_loss\_50\%Load1} + P_{Total\_loss\_50\%Load2}$$

$$P_{Total\_loss\_20\%Load1} := P_{FET\_loss\_20\%Load} + P_{Diode\_loss\_20\%Load} + P_{RS\_loss\_20\%Load}$$

$$P_{Total\_loss\_20\%Load2} := P_{Rectifier\_loss\_20\%Load} + P_{L\_loss} + P_{Cout\_loss\_20\%Load}$$

$$P_{Total\_loss\_20\%Load} := P_{Total\_loss\_20\%Load1} + P_{Total\_loss\_20\%Load2}$$

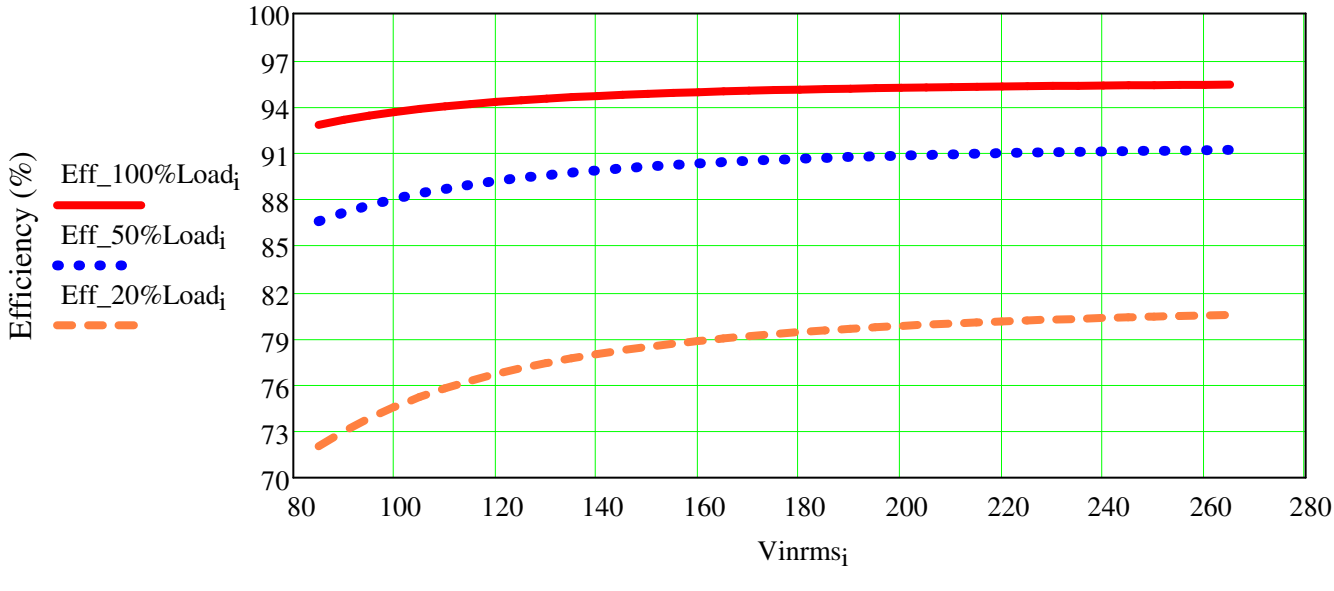


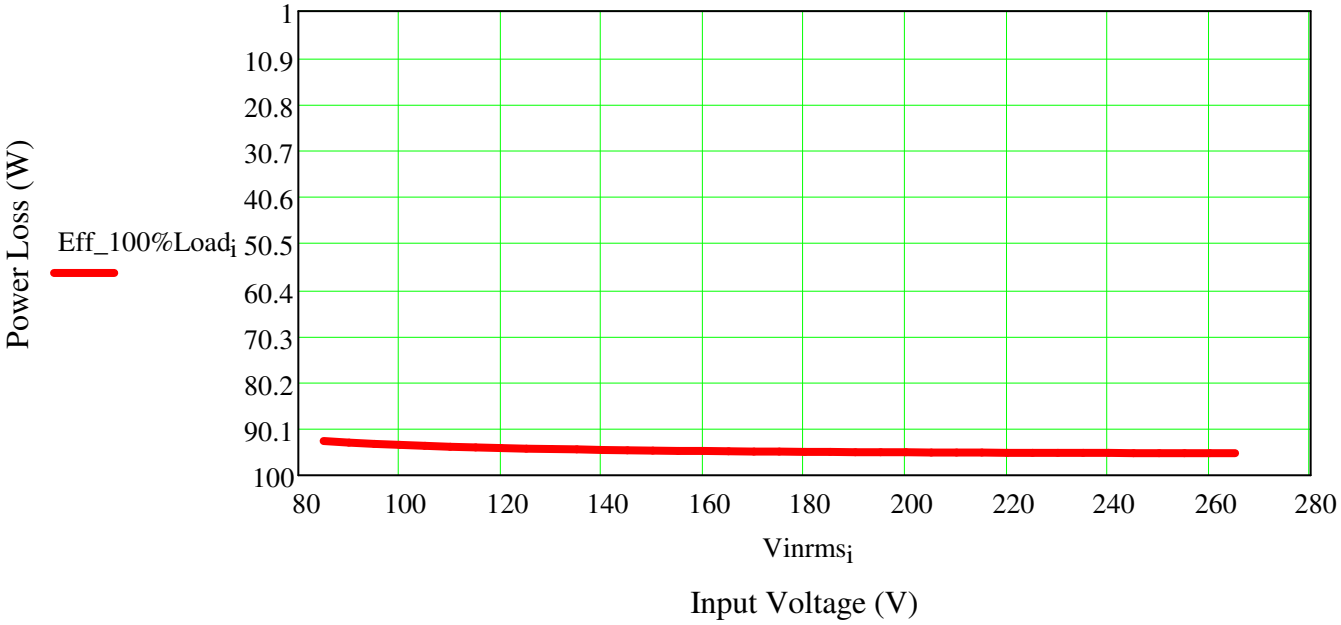


$$Eff\_100\%Load_i := \frac{Pout_i}{Pout_i + P_{Total\_loss\_100\%Load_i}} \cdot 100$$

$$Eff\_50\%Load_i := \frac{\frac{Pout_i}{2}}{\frac{Pout_i}{2} + P_{Total\_loss\_100\%Load_i}} \cdot 100$$

$$Eff\_20\%Load_i := \frac{\frac{Pout_i}{5}}{Pout_i \cdot 0.2 + P_{Total\_loss\_100\%Load_i}} \cdot 100$$





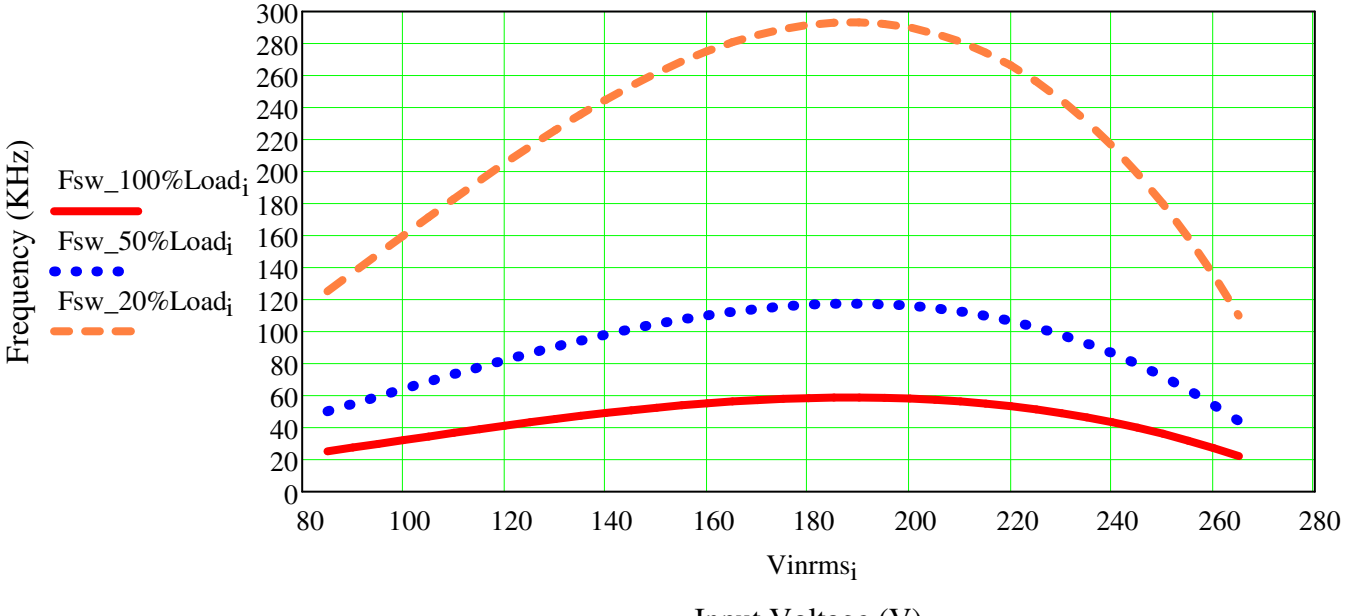
$$Fswmin := \frac{(Vinpk \cdot Vinpk) \cdot (Vout - Vinpk)}{4(Vout \cdot Pin \cdot Lp)}$$

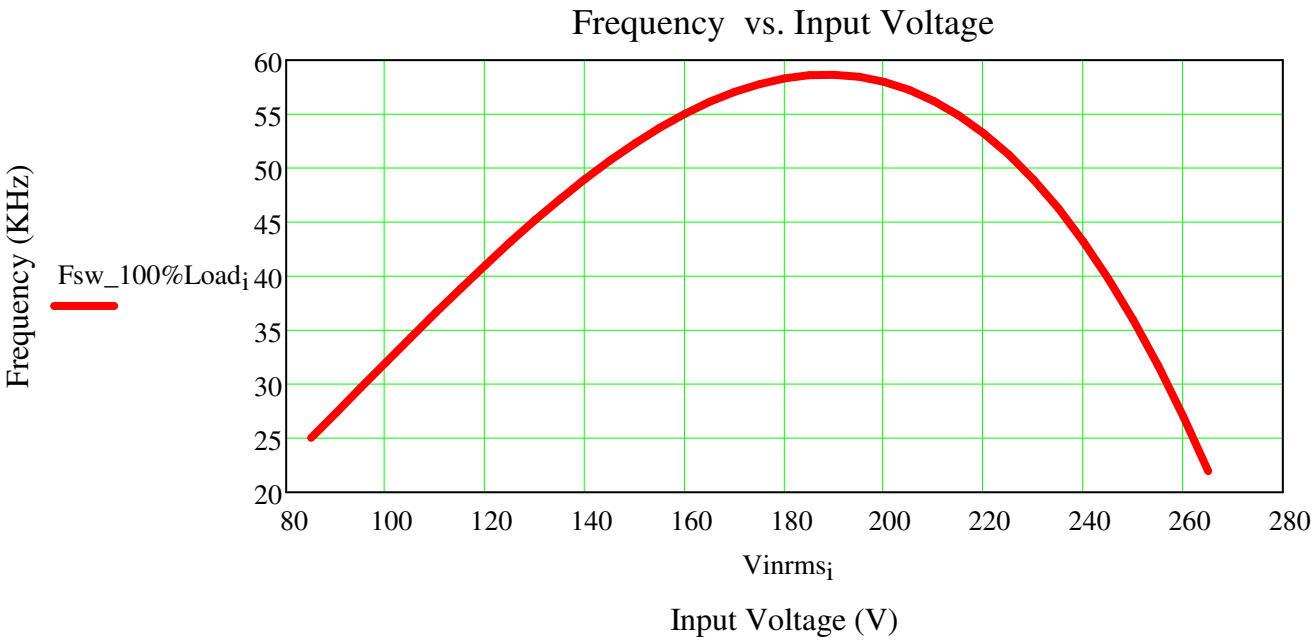
$$Vout_i := 400V$$

$$Fsw\_100\%Load_i := \frac{(Vinpk_i \cdot Vinpk_i) \cdot (Vout_i - Vinpk_i)}{4(Vout_i \cdot Pin_i \cdot Lp)} \cdot \frac{1}{1000}$$

$$Fsw\_50\%Load_i := \frac{(Vinpk_i \cdot Vinpk_i) \cdot (Vout_i - Vinpk_i)}{4\left(Vout_i \cdot \frac{Pin_i}{2} \cdot Lp\right)} \cdot \frac{1}{1000}$$

$$Fsw\_20\%Load_i := \frac{(Vinpk_i \cdot Vinpk_i) \cdot (Vout_i - Vinpk_i)}{4(Vout_i \cdot Pin_i \cdot 0.2 \cdot Lp)} \cdot \frac{1}{1000}$$




Frequency vs. Input Voltage
Frequency (KHz)
Fsw_100%Load_i
60
55
50
45
40
35
30
25
20
80
100
120
140
160
180
200
220
240
260
280
Vinrms_i
Input Voltage (V)

CRM PFC analysis for variable phase with full load condition

Design Variables	Definition
$fline := 60Hz$	Line Frequency
$Vinmin := 85V$	Minimum Input Voltage
$Vinmax := 265V$	Maximum Input Voltage
$Pout := 100W$	Maximum Output Power
$Vout := 400V$	Output Voltage
$fs := 25 \cdot 10^{3} Hz$	Minimum Switching Frequency
$\omega := 2\pi \cdot fline$	
$tholdup := 16.7 \cdot 10^{-3} s$	Period of one Line Cycle
$Vdrop := 120V$	Amount of holdup voltage
$\eta := 0.92$	Efficiency
$Pin := \frac{Pout}{\eta}$	$Pin = 108.696\,W$
$t\_hold := 40 \cdot 10^{-3} s$	

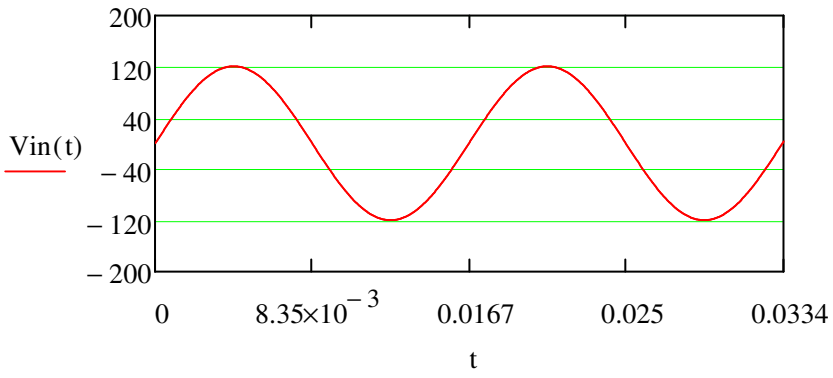
Calculation of AC Voltage and Current:

$Vinrms := Vinmin$ $\quad Vinrms = 85\,V$

$Vinpk := Vinrms \cdot \sqrt{2}$ $\quad Vinpk = 120.208\,V$

$Vin(t) := Vinpk \cdot \sin(\omega \cdot t)$

$Iinrms := \frac{Pin}{Vinrms}$ $\quad Iinrms = 1.279\,A$



Inductor Selection:

$$Iinpk := \frac{\sqrt{2}\cdot Pout}{\eta\cdot Vinmin}$$ $Iinpk = 1.808\,A$

$$ILpk := 2Iinpk$$ $ILpk = 3.617\,A$

$$Iin(t) := Iinpk\cdot\sin(\omega\cdot t)$$

$$Lp := \frac{(Vout - \sqrt{2}\cdot Vinmin)\cdot\eta\cdot Vinmin^2}{2fs\cdot Vout\cdot Pout}$$ $Lp = 9.299\times 10^{-4}\,H$

Using **EPCOS E 30/15/7**, Bmax=0.3T, Ae=60mm2

$$Bmax := 0.3T$$

$$Ae := 60mm^2$$

$$Np := \frac{Lp\cdot ILpk}{Bmax\cdot Ae} = 186.851$$ $Np = 186.851$

Design of Regulation and overvoltage protection circuit:

$$Ro := \frac{Vout}{200\mu A}$$ $Ro = 2\times 10^6\,\Omega$

Design of oscillator circuit:

Enter Cint: $Cint := 15pF$

Enter Kosc: $Kosc := 6400$

$$CT := \frac{2\cdot 6400\cdot Lp\cdot Pin\cdot Vout^2}{Vinmin^2\cdot Ro^2}$$

Design of the current sense circuit:

Rcs : current sense resistor losses

Choose Rcs=0.5 ohm $Rcs := 0.5\Omega$

$$Prcs := \frac{1}{6}\cdot Rcs\cdot ILpk^2$$ $Prcs = 1.09\,W$

Rocp: Overcurrent protection resistor

Set Iocp = 200uA $Iocp := 200\mu A$

$$Rocp := \frac{Rcs\cdot ILpk}{Iocp}$$ $Rocp = 9.042\times 10^3\,\Omega$

Input Voltage vs. phase:

$Phase := 5 .. 360$

$$Vac := \begin{pmatrix} 85 \\ 175 \\ 265 \end{pmatrix} V \qquad Vin(Phase) := Vac \cdot \sqrt{2} \cdot \sin\left(\frac{Phase \cdot \pi}{180}\right)$$

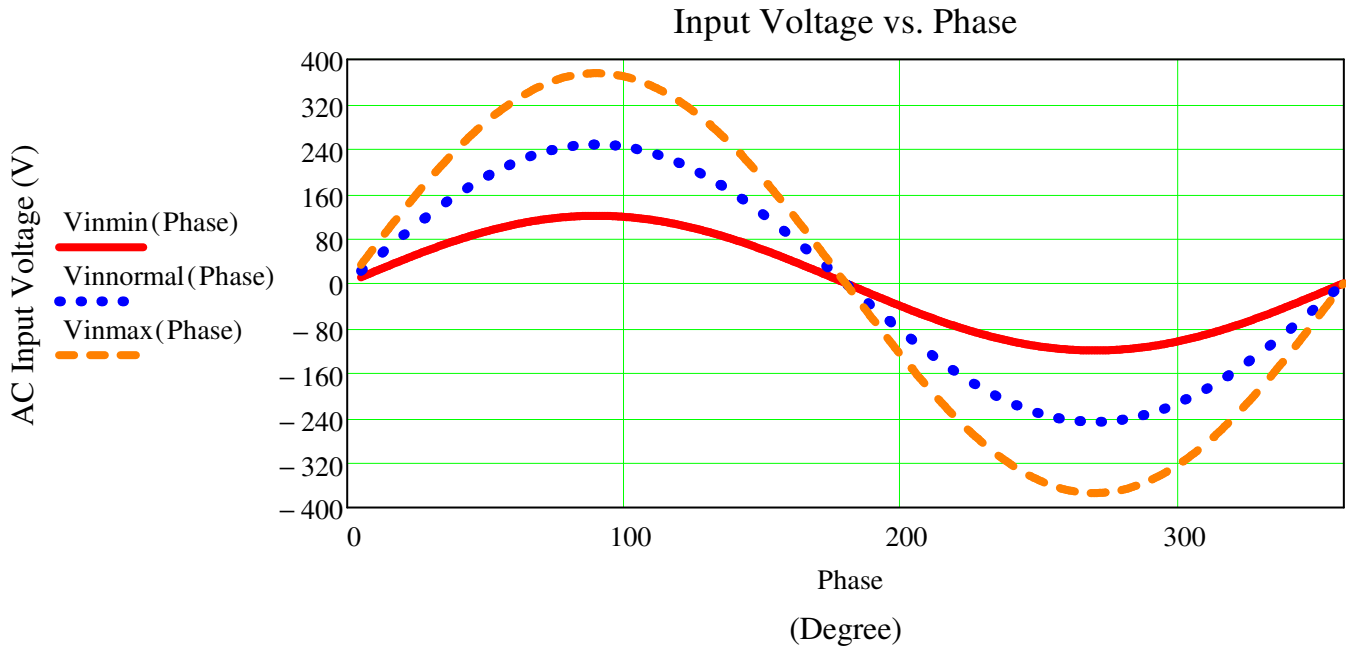
$$Pin := \begin{pmatrix} Pin \\ Pin \\ Pin \end{pmatrix} \qquad Iin := \frac{Pin}{Vac} \qquad Iin = \begin{pmatrix} 1.279 \\ 0.621 \\ 0.41 \end{pmatrix} A$$

Full Load:

$Vinmin(Phase) := Vin(Phase)_0$

$Vinnormal(Phase) := Vin(Phase)_1$

$Vinmax(Phase) := Vin(Phase)_2$



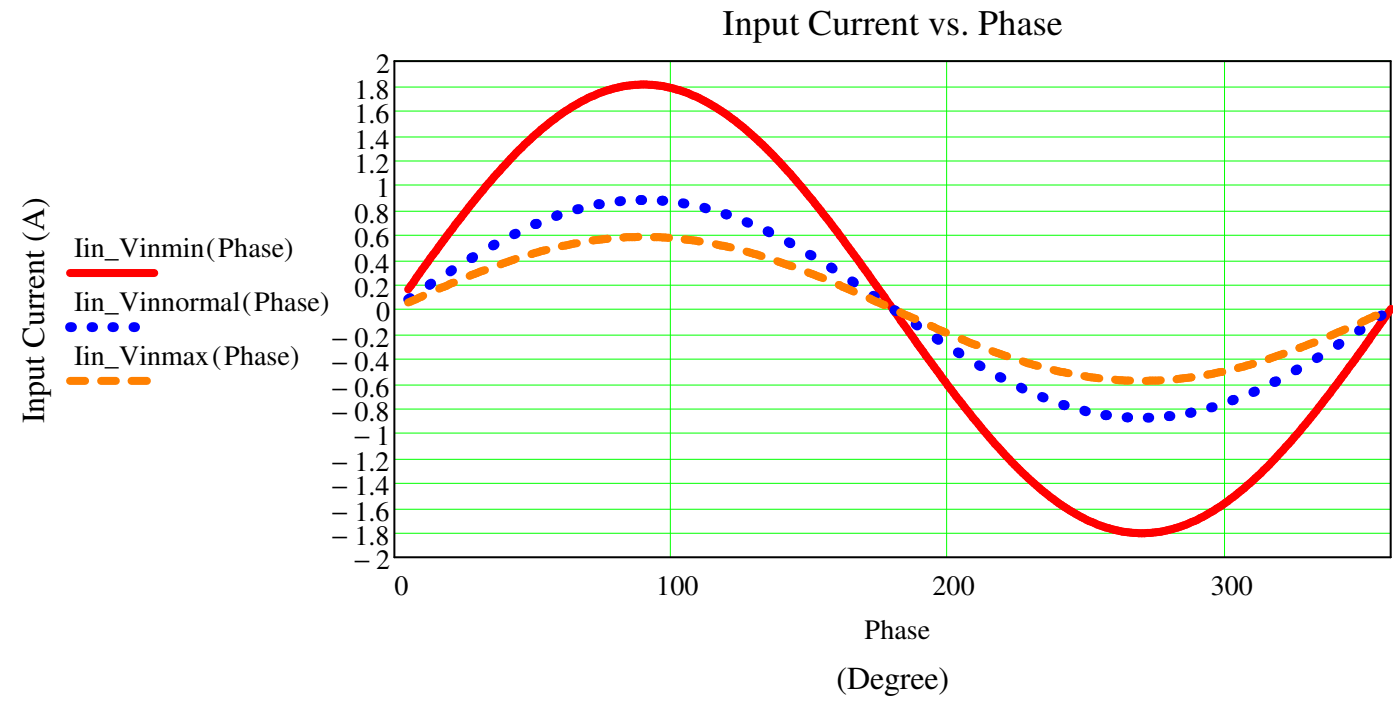
$Iinrms = 1.279\,A$

$$Iinrms(Phase) := Iin \cdot \sqrt{2} \cdot \sin\left(\frac{Phase \cdot \pi}{180}\right)$$

$Iin\_Vinmin(Phase) := Iinrms(Phase)_0$

$Iin\_Vinnormal(Phase) := Iinrms(Phase)_1$

$Iin\_Vinmax(Phase) := Iinrms(Phase)_2$

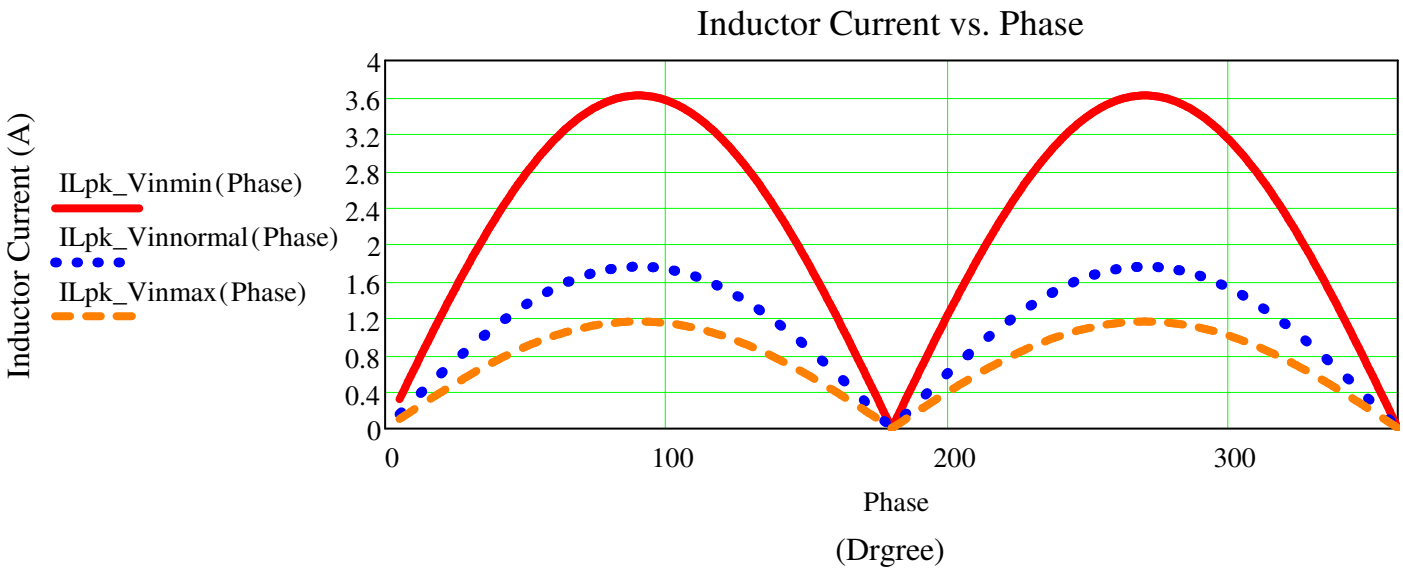


$$ILpk(Phase) := \left|2\,Iinrms(Phase)\right|$$

$$ILpk\_Vinmin(Phase) := \left|(2\,Iinrms(Phase))_0\right|$$

$$ILpk\_Vinnormal(Phase) := \left|(2\,Iinrms(Phase))_1\right|$$

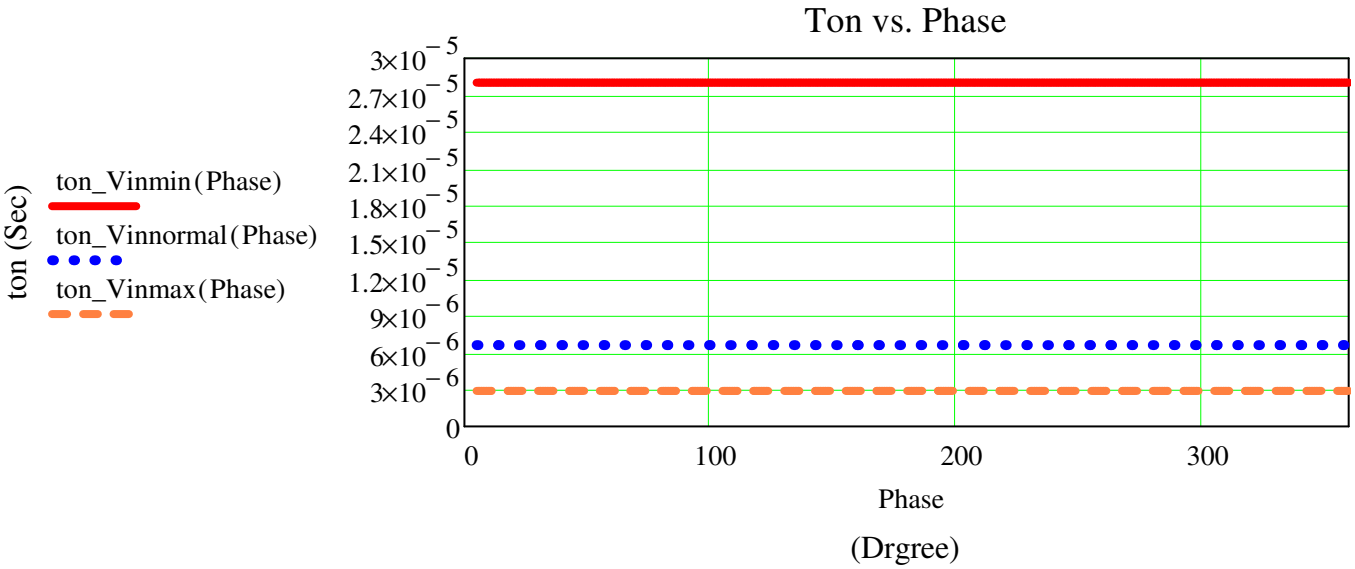
$$ILpk\_Vinmax(Phase) := \left|(2\,Iinrms(Phase))_2\right|$$

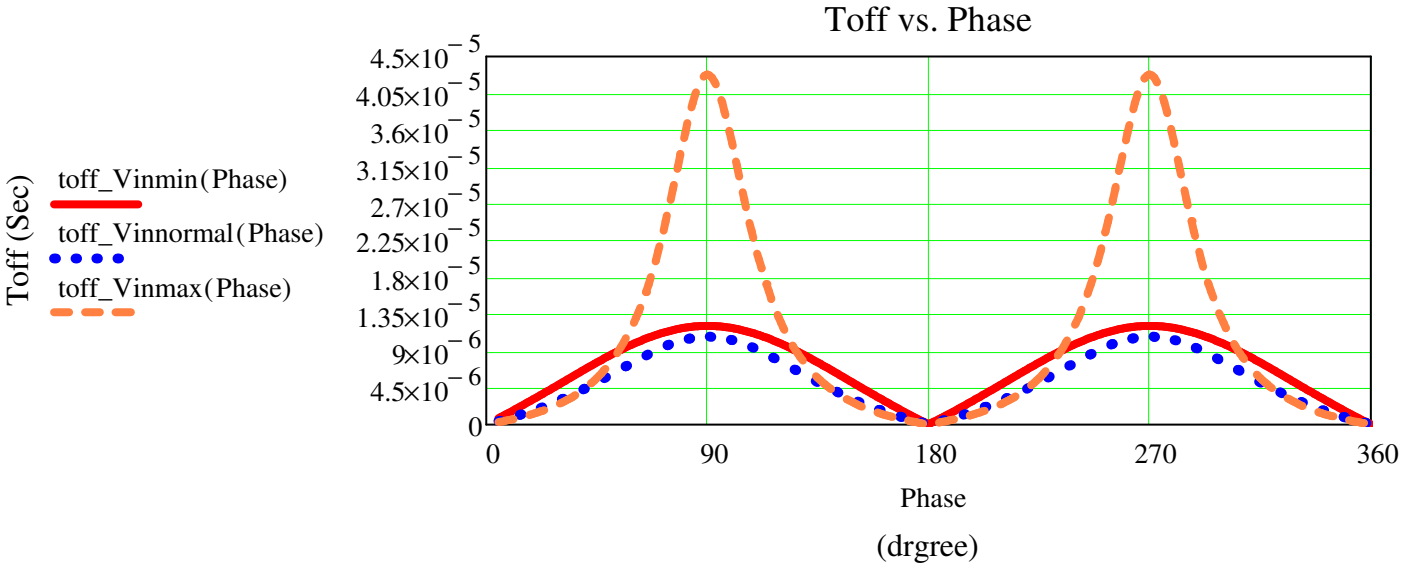


$$\text{ton\_Vinmin}(\text{Phase}) := \text{Lp}\cdot\frac{\text{ILpk\_Vinmin}(\text{Phase})}{\left|\text{Vinmin}(\text{Phase})\right|} \qquad \text{toff\_Vinmin}(\text{Phase}) := \frac{\text{Lp}\cdot\left|\text{ILpk\_Vinmin}(\text{Phase})\right|}{\text{Vout} - \left|\text{Vinmin}(\text{Phase})\right|}$$

$$\text{ton\_Vinnormal}(\text{Phase}) := \text{Lp}\cdot\frac{\text{ILpk\_Vinnormal}(\text{Phase})}{\left|\text{Vinnormal}(\text{Phase})\right|} \qquad \text{toff\_Vinnormal}(\text{Phase}) := \frac{\text{Lp}\cdot\left|\text{ILpk\_Vinnormal}(\text{Phase})\right|}{\text{Vout} - \left|\text{Vinnormal}(\text{Phase})\right|}$$

$$\text{ton\_Vinmax}(\text{Phase}) := \text{Lp}\cdot\frac{\text{ILpk\_Vinmax}(\text{Phase})}{\left|\text{Vinmax}(\text{Phase})\right|} \qquad \text{toff\_Vinmax}(\text{Phase}) := \frac{\text{Lp}\cdot\left|\text{ILpk\_Vinmax}(\text{Phase})\right|}{\text{Vout} - \left|\text{Vinmax}(\text{Phase})\right|}$$

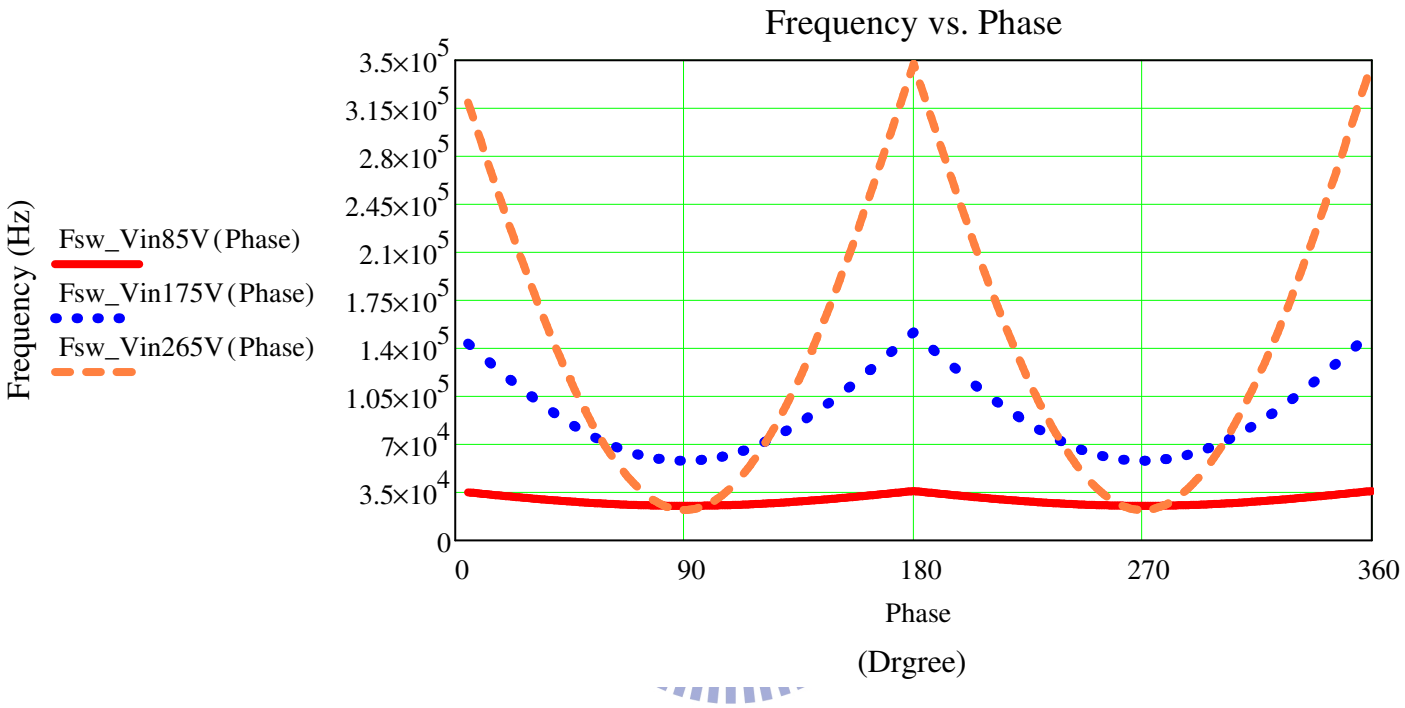




$$Fsw\_Vin265V(Phase) := \frac{1}{ton\_Vinmax(Phase) + toff\_Vinmax(Phase)}$$

$$Fsw\_Vin175V(Phase) := \frac{1}{(ton\_Vinnormal(Phase) + toff\_Vinnormal(Phase))}$$

$$Fsw\_Vin85V(Phase) := \frac{1}{(ton\_Vinmin(Phase) + toff\_Vinmin(Phase))}$$



PSIM Result: 100W CRM PFC

John Hung

May 8, 2009

Enter the names of the files that contain the waveform data in the file read box.

DATA_file := READPRN("noemi.txt")

Enter the frequency of the line voltage: $f := 60 \cdot Hz$

Enter the sample time of data log: $sample\_t := 2\mu s$

$$Pcycle := \frac{\frac{1}{f}}{sample\_t} = 8.3333 \times 10^{3}$$

Enter the number of points/cycle $P_{cycle} := 8333$

$$t_{step} := \frac{1}{P_{cycle} \cdot f} \qquad t_{step} = 2 \times 10^{-6} \cdot sec$$ Time step

Number of line voltage cycles in data set: $N_{cycle} := floor\left(\frac{rows(DATA\_file)}{P_{cycle}}\right)$ $N_{cycle} = 1$

$Points := P_{cycle} \cdot N_{cycle}$ $Points = 8333$ Number of data points

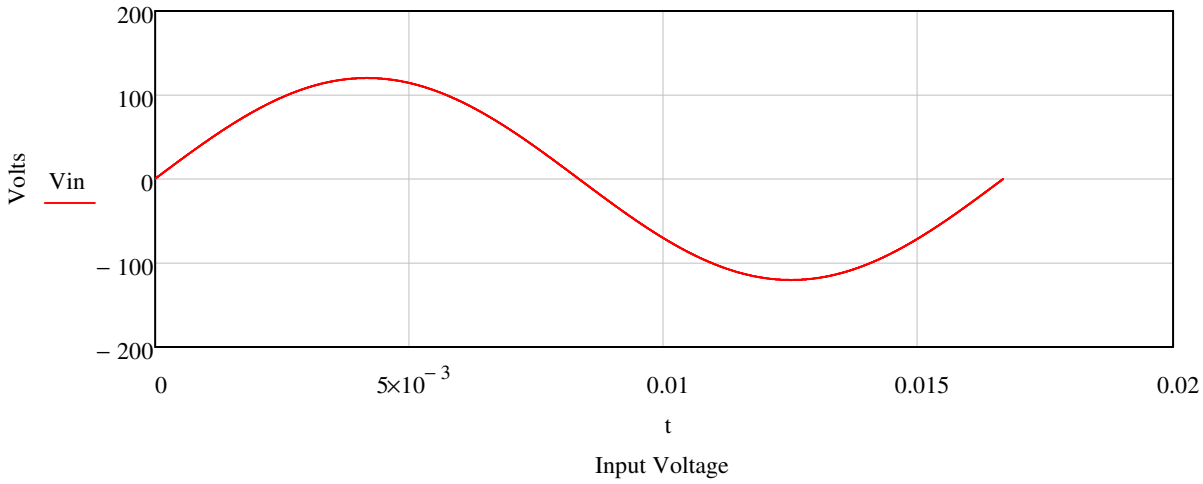
Time length of data set: $T := Points \cdot t_{step}$ $T = 0.0167\,s$

$n := 1 .. Points$

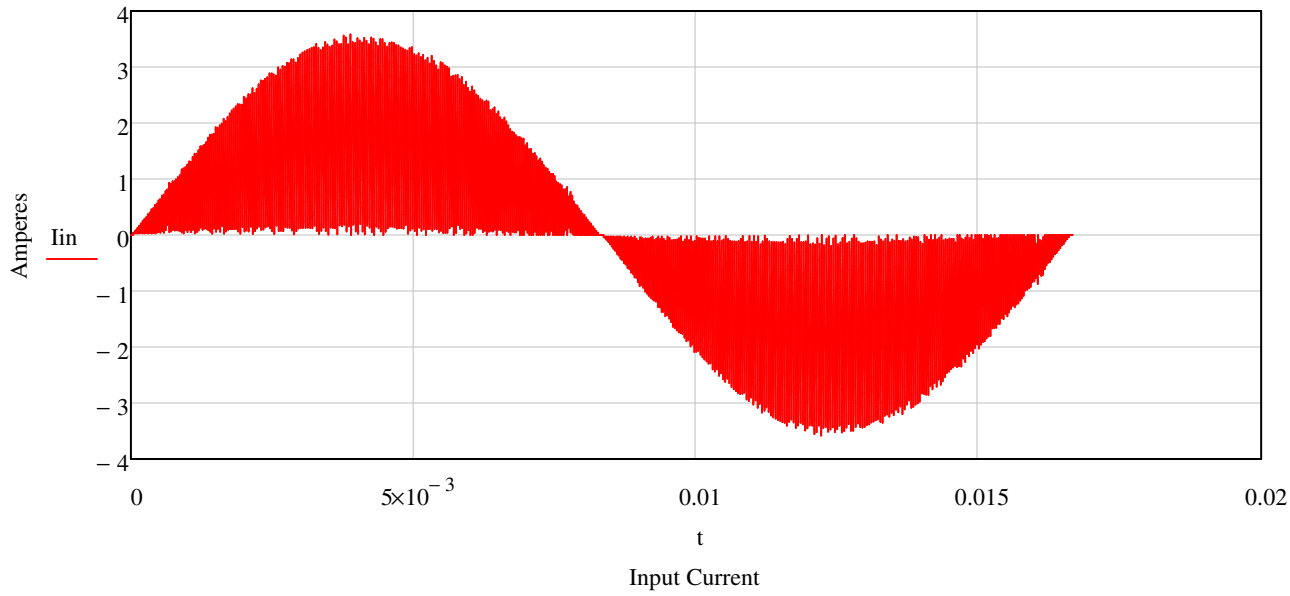
$t_n := t_{step} \cdot n$ Array of time values

Extract voltages and currents from the data file.

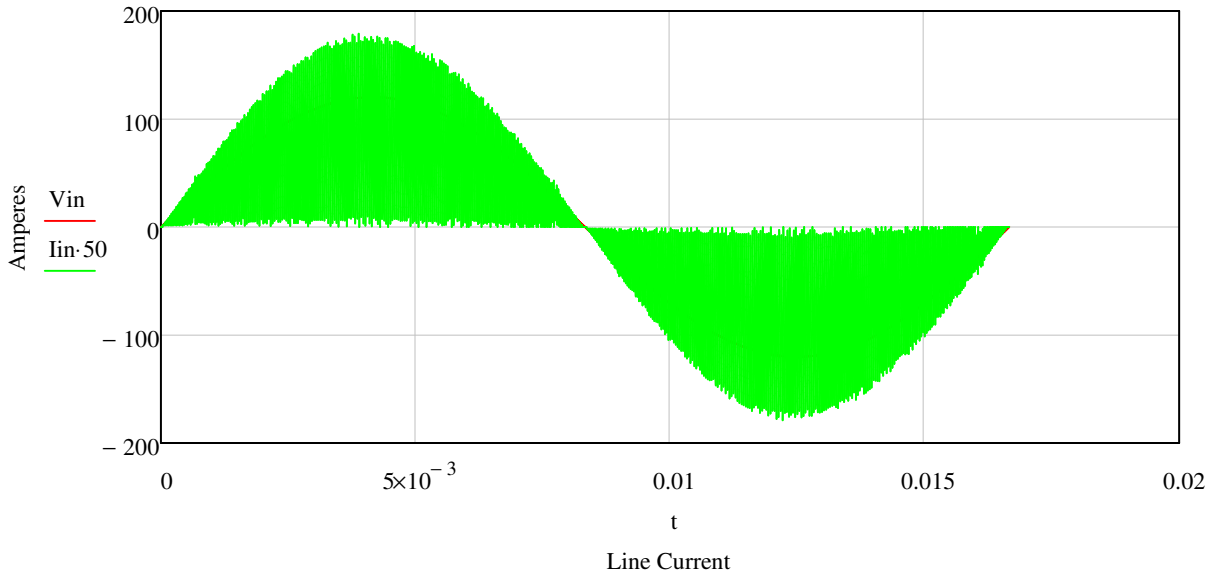
$Vin := DATA\_file^{\langle 6 \rangle} \cdot V$ $Iin := \left(DATA\_file^{\langle 4 \rangle} \cdot A\right)$



Input Voltage



Input Current



Line Current

Compute the rms Input voltage and rms Input current.

$$Vin_{rms} := \sqrt{\frac{1}{Points}\left[\sum_{n=1}^{Points}\left(Vin_n\right)^2\right]} \qquad Vin_{rms} = 85.00\,V$$

$$Iin_{rms} := \sqrt{\frac{1}{Points}\cdot\left[\sum_{n=1}^{Points}\left(Iin_n\right)^2\right]} \qquad Iin_{rms} = 1.462\,A$$

$$Sin := Vin_{rms}\cdot Iin_{rms} = 124.27\,W$$

Enter the number of the highest harmonic of the power line frequency to use in computing the Fourier coefficients of the line-line voltages: $h_{max} := 1800$

Frequency corresponding to the length of the data set. $F := \frac{1}{Points \cdot t_{step}}$ $F = 60 \frac{1}{s}$

Define the fundamental frequency

Highest harmonic of F to use in the Fourier calculations. $H_{max} := h_{max} \cdot N_{cycle}$ $H_{max} = 1800$

$h := 1 .. H_{max}$

Frequency corresponding to h. $Freq_h := F \cdot h$

Compute matrices of sine and cosine values to be used in the Fourier calculations.

Matrix size $H_{max} \cdot Points = 1.5 \times 10^7$

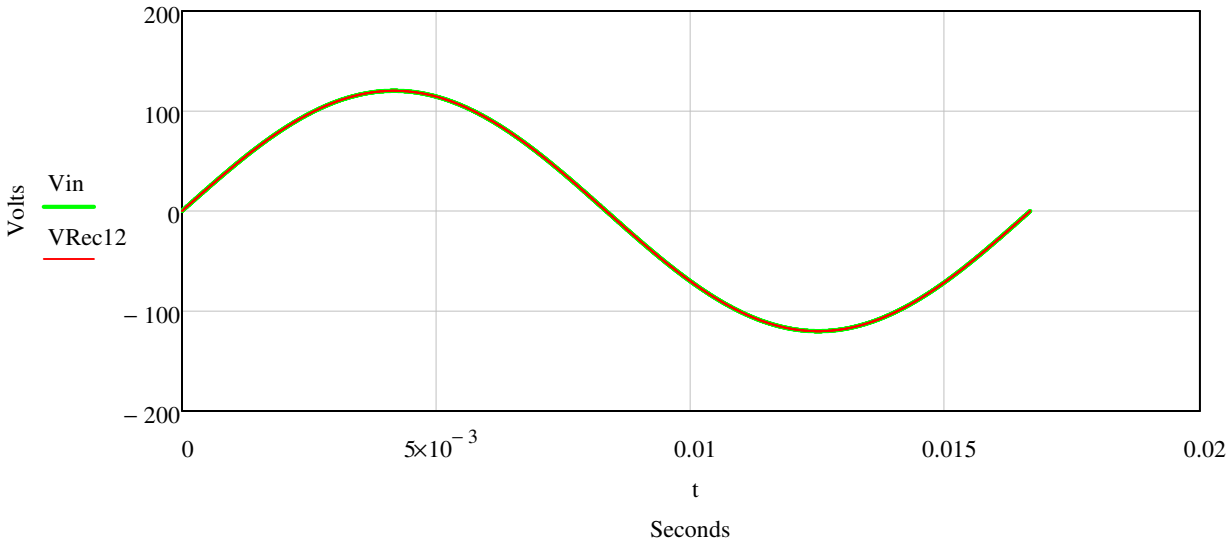
$COSFht_{h,n} := \cos(2 \cdot \pi \cdot Freq_h \cdot t_n)$ $SINFht_{h,n} := \sin(2 \cdot \pi \cdot Freq_h \cdot t_n)$

Compute the Fourier coefficients of the line-line voltages.

$$AVin_h := \frac{2}{Points} \cdot \left[\sum_{n=1}^{Points} \left(Vin_n \cdot COSFht_{h,n} \right) \right] \quad BVin_h := \frac{2}{Points} \cdot \left[\sum_{n=1}^{Points} \left(Vin_n \cdot SINFht_{h,n} \right) \right]$$

Compute reconstructed voltage waveforms from the Fourier coefficients

$$VRec12_n := \sum_{h=1}^{H_{max}} \left(AVin_h \cdot COSFht_{h,n} + BVin_h \cdot SINFht_{h,n} \right)$$



Actual and reconstructed line-line voltage waveforms.

Compute line-line voltage phasors.

$$VPH12 := \frac{AVin - j \cdot BVin}{\sqrt{2}}$$

Check to see that the sum of the phasors is approximately zero.

$$\max\left(\overrightarrow{|VPH12|}\right) = 85\,V \qquad \text{mean}\left(\overrightarrow{|VPH12|}\right) = 0.05\,V$$

Check to see that the rms voltages computed from the data points are close to the values of the rms voltages computed from the phasors.

$$Vin_{rms} = 85.0\,V$$

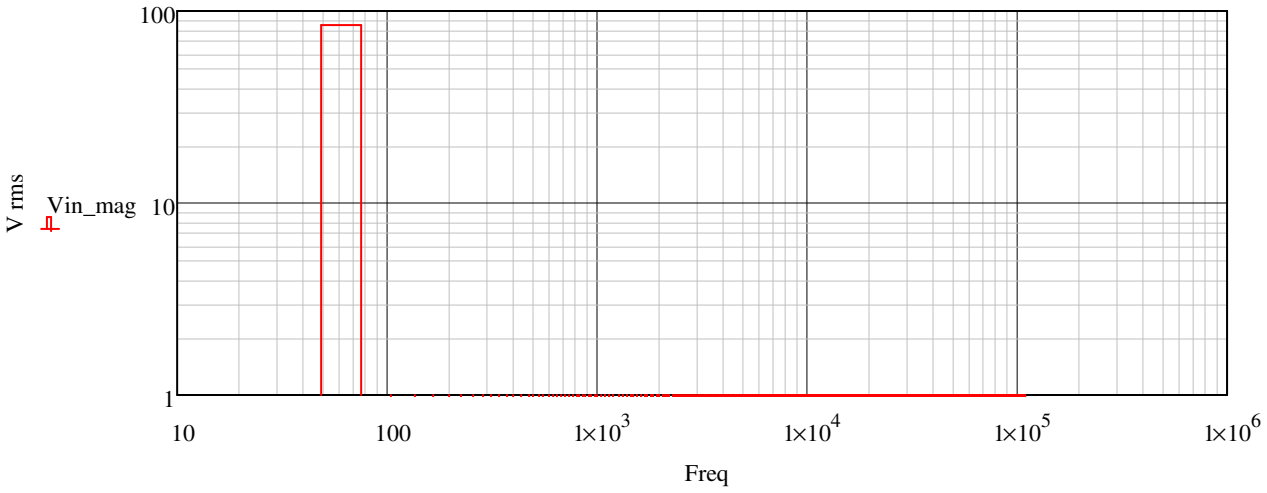
$$|VPH12| = 85.0\,V$$

Compute the magnitude of the line-line voltage at each harmonic.

$$Vin\_mag := \overrightarrow{|VPH12|}$$

Fundamental components of the line-line voltages.

$$Vin\_mag_{N_{cycle}} = 85\,V$$



Input voltage spectrum.

Compute the Fourier coefficients of the line current waveforms.

$$AIin_h := \frac{2}{Points} \cdot \left[\sum_{n=1}^{Points} \left(Iin_n \cdot COSFht_{h,n}\right)\right] \qquad BIin_h := \frac{2}{Points} \cdot \left[\sum_{n=1}^{Points} \left(Iin_n \cdot SINFht_{h,n}\right)\right]$$

Compute line current phasors.

$$IPH1 := \frac{AIin - j \cdot BIin}{\sqrt{2}}$$

Check to see that the sum of the phasors is approximately zero.

$$\max\left(\overrightarrow{|IPH1|}\right) = 1.27\,A \qquad \text{mean}\left(\overrightarrow{|IPH1|}\right) = 5.73 \times 10^{-3}\,A$$

Check to see that the rms voltages computed from the data points are close to the values of the rms voltages computed from the phasors.

$$IPH1_{rms} := |IPH1|$$

$$IPH1_{rms} = 1.461\,A$$

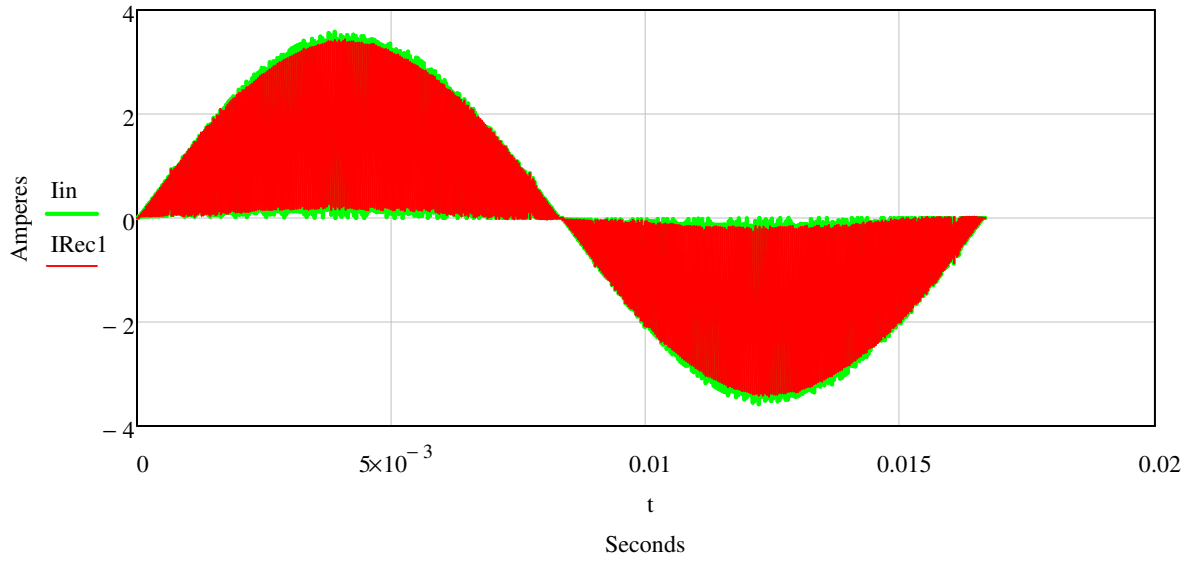
$$Iin_{rms} = 1.462\,A$$

Compute the magnitude of the line current at each harmonic.

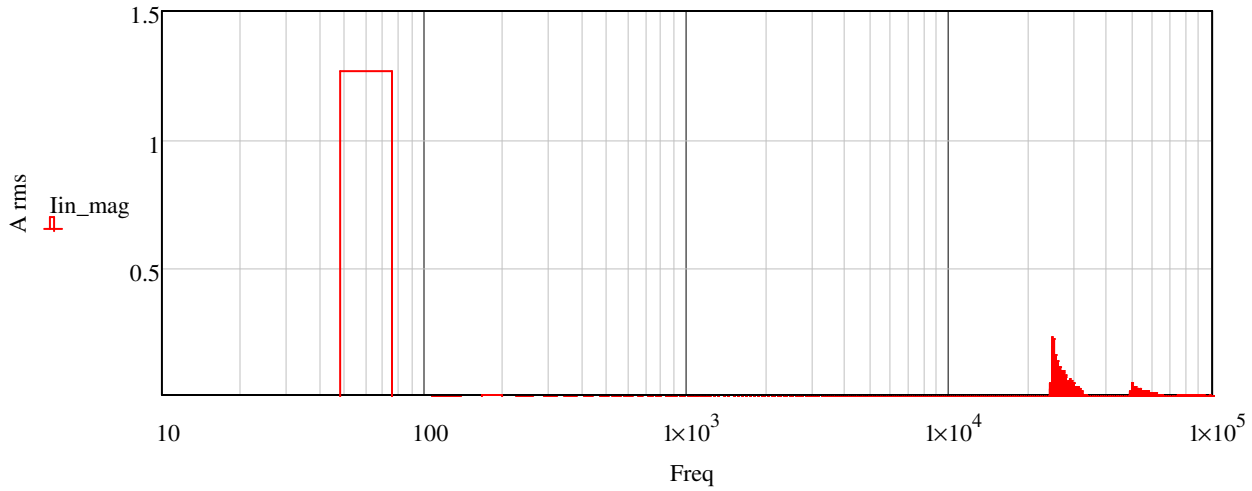
$$Iin\_mag := \overrightarrow{|IPH1|} \qquad Iin\_mag_{N_{cycle}} = 1.27\,A$$

Compute reconstructed line current waveforms from the Fourier coefficients

$$IRec1_n := \sum_{h=1}^{H_{max}} \left(AIin_h \cdot COSFht_{h,n} + BIin_h \cdot SINFht_{h,n}\right)$$



Actual and reconstructed line current waveforms.



Input current spectrum.

Compute input voltage and input current THD percentages.

$$VinTHD := \frac{\sqrt{\sum_{h=1}^{H_{max}} \left[\left(AVin_h\right)^2 + \left(BVin_h\right)^2 \right] - \left[\left(AVin_{N_{cycle}}\right)^2 + \left(BVin_{N_{cycle}}\right)^2 \right]}}{\sqrt{\left(AVin_{N_{cycle}}\right)^2 + \left(BVin_{N_{cycle}}\right)^2}} \qquad VinTHD = 7.5 \times 10^{-3} \cdot \%$$

$$IinTHD := \frac{\sqrt{\sum_{h=1}^{H_{max}} \left[\left(AIin_h\right)^2 + \left(BIin_h\right)^2 \right] - \left[\left(AIin_{N_{cycle}}\right)^2 + \left(BIin_{N_{cycle}}\right)^2 \right]}}{\sqrt{\left(AIin_{N_{cycle}}\right)^2 + \left(BIin_{N_{cycle}}\right)^2}} \qquad IinTHD = 57.3 \cdot \%$$

$$Kd := \sqrt{\frac{1}{1 + IinTHD^2}} = 0.868 \qquad Vout := 404V \qquad Rload := 1595\Omega \qquad Pout := \frac{Vout^2}{Rload} = 102.33\,W$$

If the 25KHz~50K current harmonic be reduced to 50%

$$Atte := \frac{\sqrt{0.99\left[\sum_{h=200}^{440} \left[\left(AIin_h\right)^2 + \left(BIin_h\right)^2 \right]\right] - 0.999\left[\sum_{h=440}^{H_{max}} \left[\left(AIin_h\right)^2 + \left(BIin_h\right)^2 \right]\right]}}{\sqrt{\left(AIin_{N_{cycle}}\right)^2 + \left(BIin_{N_{cycle}}\right)^2}}$$

Vita

Chia-Han Hung was born in Taichung, Taiwan, R.O. C., in 1975. He received the B.S. degree in electrical engineering from National Formosa University, Yunlin, Taiwan, in 1995. He is currently pursuing the master degree in electrical and control engineering at National Chiao Tung University, Hsinchu, Taiwan. His research interests are in the areas of power factor correction converters design, power quality analysis and PV inverter application.

姓名: 洪袈瀚

性別: 男

生日: 中華民國 64 年 7 月 8 日

論文題目: 中文:以 MathCAD 為基礎之邊界模式功率因數修正轉換器與 EMI 濾波器設計

英文:MathCAD Design of Critical Conduction Mode PFC Converters with EMI Filter

學歷:

1. 民國 84 年 6 月　國立雲林工專電機工程科系畢業
2. 民國 98 年 10 月　國立交通大學電機及控制工程研究所碩士在職專班

經歷:

1. 民國 86 年 8 月　台塑六輕汽電共生廠主辦
2. 民國 88 年 5 月　美商伊頓技術支援工程師
3. 民國 92 年 8 月　美商台灣艾儀技術支援工程師
4. 民國 94 年 8 月　美商台灣艾儀技術支援課長
5. 民國 97 年 10 月　美商台灣艾儀技術支援副理

得獎:

1. 民國 84 年 6 月　國立雲林工專電機科最佳專題製作獎(六軸教導型機械手臂設計)
2. 民國 94 年 2 月　美商台灣艾儀總經理獎
3. 民國 97 年 2 月　美商台灣艾儀總經理獎

著作目錄

研討會

[1] C. H. Hung, Y. Y. Tzou, "MathCAD design of critical conduction mode PFC converters," in *Proc. IEEE Power Electronics and Motion Control Conference*, 2009, pp. 1684-1688.

[2] C. H. Hung, Y. Y. Tzou, "MathCAD design of critical conduction mode PFC converters with EMI filters," 第三十屆電力工程研討會, 桃園, 台灣, Nov. 28-29, 2009.

[3] C. H. Hung, C. J. Chen, T. W. Yu, C. P. Huang, "Cost benefit analysis and application for transformerless inverter with bipolar PV array in 5MW PV system," 第三十屆電力工程研討會, 桃園, 台灣, Nov. 28-29, 2009.