國立交通大學

資訊學院　資訊學程

碩 士 論 文

全數位高解析度寬頻頻率合成器之設計

The Study of High-resolution and Wide-bandwidth Frequency synthesizer

研 究 生：吳青峰

指導教授：許騰尹　博士

中 華 民 國 九 十 七 年 七 月

全數位高解析度寬頻頻率合成器之設計

The Study of High-resolution and Wide-bandwidth Frequency synthesizer

研 究 生：吳青峰　　Student：Cheng-Feng Wu

指導教授：許騰尹 博士　　Advisor：Dr. Terng-Yin Hsu

國 立 交 通 大 學

資訊學院　資訊學程

碩 士 論 文

A Thesis

Submitted to College of Computer Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of Master of Science

in

Computer Science

July 2008

Hsinchu, Taiwan, Republic of China

中華民國九十七年七月

全數位高解析度寬頻頻率合成器之設計

學生：吳青峰　　指導教授：許騰尹 博士

國 立 交 通 大 學　　資 訊 學 院　　資 訊 學 程 碩 士 班

摘要

全數位頻率合成器為現今電路設計中之一個重要部份，特別是應用在個人數位行動通訊之系統晶片。而數位振盪器的輸出直接影響到頻率合成器的效能好壞，本論文特別專注於數位振盪器之效能提升，在此使用了標準元件中的 AOI/OAI 之原生電容做為數位可變電容器，可將最小控制位元之頻率解析度提高至 10fs，利用四級的微調單元及使用數位轉時間轉換器來加大頻率操作範圍並節省晶片面積，在反相延遲信號線加入反及閘做為致能開關，來降低不必要之功率消耗，並搭配低複雜度之頻率追蹤演算法，在一般條件下可在 30 週期數內鎖定頻率，達成大頻率操作範圍及高解析度之目的，並且為低功率消耗低晶片面積之設計，整個設計皆使用標準元件，因此可在更短的設計時間

內轉換不同製程 , 在數位振盪器的關鍵元件配置部份 , 採用標準元件之手動的擺放和繞線 , 以確保設計符合要求 , 也節省了若使用全客製化設計之心力 , 經由 HSpice 的模擬 , 可得本設計有 187KHz 到 345MHz 之操作範圍且最小控制位元可達 10fs 之解析度。

The Study of High-resolution and Wide-bandwidth frequency synthesizer

Student: Cheng-Feng Wu Advisor: Dr. Terng-Yin Hsu

Degree Program of Computer Science

National Chiao Tung University

Abstract

The most important part of modern circuit design is the all-digital frequency synthesizer. That especially for the personal mobile communication application in SoC design. The output of digitally-controlled oscillator (DCO) will directly impact the performance of the frequency synthesizer. This thesis is focus on the performance enhancement of the DCO. The proposed DCO used AOI/OAI standard cells to form as digital controlled varactor. It could increase the LSB frequency resolution to 10fs. Four fine tune cell and digital to time converter are used to archive wide frequency operation range without big chip area. This work added enable cell such as NAND into the inverter delay line. It can prevent unnecessary power dissipation. To combine a low complexity frequency tracking algorithm that frequency locking time is within 30 clock cycles in typical case. Thus, this work is a wide operation range, high frequency resolution, low power and small chip size design. In this work all the cells are standard cell. It makes process switch more quickly. The place and route of the DCO key components are done by manual. This ensures that the design is under specification and is also saving the effort if done by fully-customer. Through HSpice simulation, this work can operate at 187KHz~345MHz, the LSB controlled frequency resolution is 10fs.

Acknowledgement

This thesis describes research work I performed in the Integration System and Intellectual Property (ISIP) Lab during my graduate studies at National Chiao Tung University (NCTU). This work would not have been possible without the support of many people. I would like to express my most sincere gratitude to all those who have made this possible.

First and foremost I would like to thank my advisor Dr. Terng-Yin Hsu for the advice, guidance, and funding he has provided me with. I feel honored by being able to work with him.

I am very grateful to every members of ISIP Lab for their supports and suggestions. I would like to thank them for being with me through the happy and hard times.

Finally, and most importantly, I want to thank my parents for their unconditional love and support they provide me with. It means a lot to me.

Cheng-Feng Wu
June 2008

Table of Contents

摘要 I

ABSTRACT III

ACKNOWLEDGEMENT IV

TABLE OF CONTENTS V

LIST OF TABLES VII

LIST OF FIGURES VIII

CHAPTER 1 INTRODUCTION 1

1.1. THESIS BACKGROUND 1
1.2. THESIS MOTIVATION 1

CHAPTER 2 OVERVIEW OF FREQUENCY SYNTHESIZER 3

2.1. OVERVIEW OF FREQUENCY SYNTHESIZER 3
2.1.1. DIRECT ANALOG SYNTHESIS 3
2.1.2. DIRECT DIGITAL SYNTHESIS 4
2.1.3. INDIRECT SYNTHESIS USING PHASE LOCKING 4
2.2. OVERVIEW OF PHASE-LOCKED LOOP 4

CHAPTER 3 THE PROPOSED ALL-DIGITAL PHASE-LOCKED LOOP 7

3.1. ALL-DIGITAL PHASE-LOCKED LOOP ARCHITECTURE OVERVIEW 7
3.2. BASIC CONCEPT OF DCO IMPLEMENTATIONS 10
3.2.1. DIGITAL-TO-TIME CONVERTER 10
3.2.2. RING OSCILLATOR 11
3.2.3. DIGITALLY CONTROLLED VARACTOR (DCV) 11
3.3. STANDARD CELL-BASED DIGITAL-CONTROL-OSCILLATOR (DCO) 12

3.3.1. DIGITAL TO TIME CONVERTER DTC 13
3.3.2. COARSE-TUNE CELL 14
3.3.3. FINE-TUNE CELL 15

CHAPTER 4 SIMULATION AND LAYOUT 17

4.1. SPICE SIMULATION 17
4.2. LAYOUT. 19

CHAPTER 5 CONCLUSION AND FUTURE WORK 22

5.1 CONCLUSION 22
5.2 FUTURE WORK 22

BIBLIOGRAPHY 23

APPENDIX A - LAKER TOUR 24

APPENDIX B - ABSTRACT TOUR 27

List of Tables

Table 3.1 13
Table 4-1 21

List of Figures

(Fig. 2-1) 3
(Fig. 2-2) 4
(Fig. 2-3) 5
(Fig.2-4-1) (Fig.2-4-2) 5
(Fig.2-5) 6
(Fig. 3-1) 7
(Fig. 3-2) 8
(Fig.3-3-1) (Fig.3-3-2) (Fig.3-3-3) 8
(Fig.3-4-1) 9
(Fig.3-4-2) 9
(Fig.3-4-3) 10
(Fig.3-5) 11
(Fig. 3-6) 11
(Fig. 3-7) 12
(Fig. 3-8) 12
(Fig.3-9) 13
(Fig.3-10) 14
(Fig.3-11) 15
(Fig.3-12) 15
(Fig. 4-1) 17
(Fig. 4-2) 18
(Fig. 4-3-1) (Fig. 4-3-2) 18
(Fig. 4-4) 19
(Fig. 4-5) 19
(Fig. 4-6) 20
(Fig. 4-7) 20
(Fig. 4-8) 21

Chapter 1

Introduction

1.1. Thesis Background

As Very Large Scale Integrated circuits (VLSI) techniques become more and more complexity, the functions also become more and more powerful. In modern System-on-Chip (SoC) design, one single chip could contain many functions such as audio process, video process, and wireless communication. In recently year, personal mobile communication is getting more and more popular. There are many kinds of wireless communication techniques had been development and become standard. All of these communication techniques have same demand such as low power, low cost, high performance and process portable.

Frequency synthesizer is widely using in SoC applications. The SoC design needs a good performance clock generator. Because of the design of frequency synthesizer is a trade-off among phase noise, frequency resolution, power consumption, area-cost, circuit complexity and design time. How to balance those parameters and gain the most benefit in SoC? The analog design with fully-customer layout provided the high performance in SoC. However, the analog design implies the big chip area, high power consumption and variance with PVT. Fully-customer layout takes big effort and is not easy to switch process.

If the module in SoC design is reusable and portable, it may save design time. If used PLL based frequency synthesis, it may have good performance of phase noise. If used all digital phase-locked loop (ADPLL) based frequency synthesis, it could save power consumption, area-cost and circuit complexity. How to combine those advantages in a practical way is very important.

1.2. Thesis Motivation

There are some advantages compare the ADPLL based with the analog based frequency synthesizer design. Traditional analog loop filter costs a lot of chip areas, since it uses resistance and capacitor. Digital loop filters gives benefits such as programmable parameters, robustness against noise and less power consumption. Digital design also can prevent to DC offset and drift phenomena. The digital design has another advantage that is the Electronic

Design Automation (EDA) tools. With the EDA tools help, designers can do Place and Route (P&R) easily. However, it is not the same situation for the most critical components such as DCO. The designers need to set proper constraints to the EDA tools; otherwise the EDA tools will not synthesis the desired circuits. For example, a delay chain composed of cascade inverters might be optimized to one inverter by EDA P&R tools. Besides, the critical path usually cannot allow changing the routing layer. Changing the routing layer means that via has been added so that the capacitance may become unpredictable. Therefore, a semi-fully layout art has been proposed. This design only used CIC 90nm technology standard cell library without any other customer cell. The semi-fully layout art is place standard cell but routing by manual. This art gets the advantages both of analog and digital design.

Clock generator is the most important component of frequency synthesizer. In the analog designs, voltage controlled oscillator (VCO) are usually used to providing low phase noise frequency. This advantage comes with many disadvantages such as power consumption, area cost. Those issues make VCO is not suitable for mobile application. In this work, the proposed DCO is high-resolution and wide-bandwidth; moreover, it is a low power and small area design. Those good properties make the DCO to fit low power and mobile application.

1.3. Thesis Organization

The organization of this thesis is as follows:
In chapter 2, it is a brief to the applications of the Frequency synthesizer. And introduce the advantage of the Frequency synthesizer based on ADPLL.

In chapter 3, the proposed ADPLL is introduced. A detailed description of the idea and simulation are given. Including how we used standard cell to complete coarse tune and fine tune cell in DCO.

In chapter 4, we illustrated the hardware implementation and layout. A detailed description of the DCO implementation has illustrated.

In chapter 5, some concluding remarks will be derived from this research. Finally, we describe several design issues that needed to be further explored in the near future.

Chapter 2

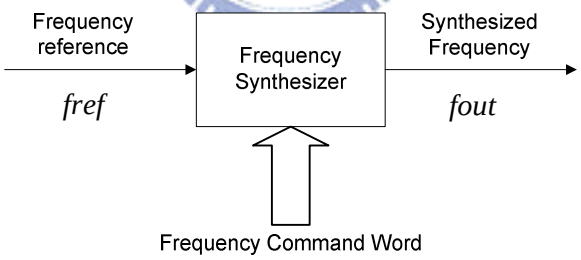
Overview of Frequency Synthesizer

There are many applications need clock synchronization or frequency multiplication. Several methods could meet the functional required but how to balance the cost and performance should never be ignored. In this chapter, gives a discussion about the advantages and disadvantages between those different approaches.

The organization of this chapter is as follows. Section 2.1 gives the overview of the frequency synthesizer. The architecture and algorithm of different digital PLL are discussed in section 2.2. Section 2.3 illustrates frequency synthesizer based on ADPLL.

2.1. Overview of Frequency Synthesizer

Frequency synthesizer (Fig. 2-1) accepts some frequency reference input signal (FREF) of a very stable frequency f_{ref} and then generates output frequency by the frequency command word (FCW).



(Fig. 2-1)

The relation between output frequency and FCW has represented in the equation.

$$f_{out} = FCW \times f_{ref} \quad \text{(Eq.2-1)}$$

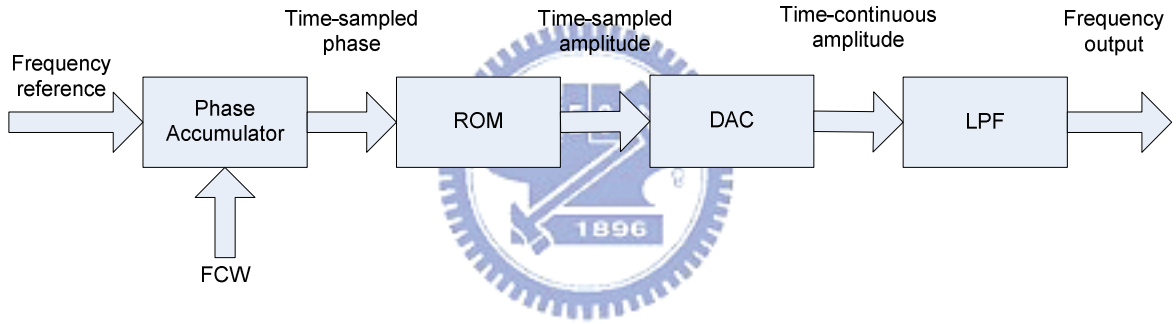
There are many applications such as date recover, wireless communication, and microprocessor need frequency synthesizers. Base on different purposes and demands, Frequency synthesizer have different implementations. From the view of techniques, there are three major types of frequency synthesis techniques [8]. 1. Direct analog mix/filter/divide. 2. Direct digital. 3. Indirect or phase-locked loop. Following section is the discussion of these three types.

2.1.1. Direct Analog Synthesis

Direct Analog Synthesis to produce the desired frequency by using frequency multipliers, dividers, filter and other mathematical manipulation. The quality of the output frequency correlates directly with the quality of the input. The advantages of this process type are the phase noise typically excellent, because the direct process and switching speed can be very fast. A broadband synthesis that used direct analog synthesis requires many references frequency, which makes it expensive. The disadvantages are high cost and high power consumption.

2.1.2. Direct Digital Synthesis

Fig. 2-2 shows the direct digital frequency synthesis (DDFS) system. A DDFS system used logic and memory to construct the desired output signal digitally, and a data conversion device to convert it from the digital to the analog domain. Although it can provide precise amplitude, frequency and phase, the power consumption could be excessive at high clock frequencies. Besides, the DAC and LPF are not pure digital designs. They contain analog components.



(Fig. 2-2)

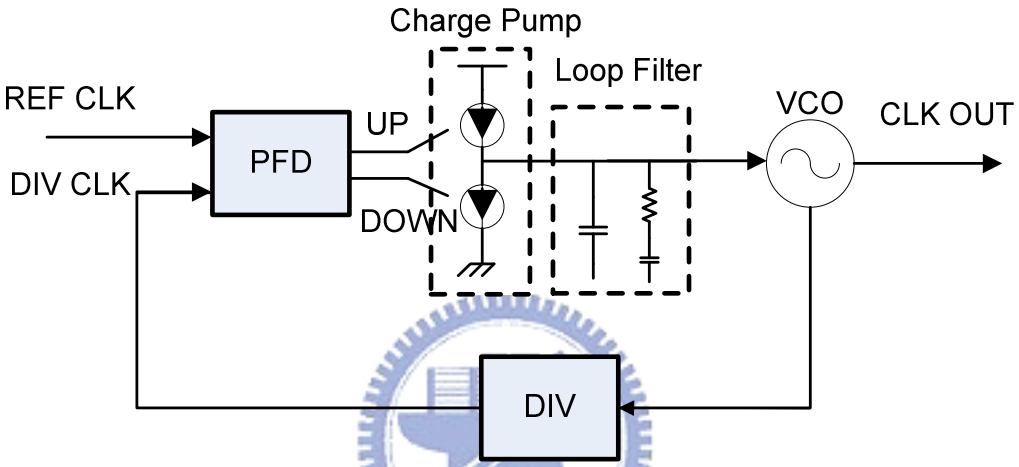
2.1.3. Indirect Synthesis Using Phase Locking

Indirect synthesis using a PLL compares the output phase of an oscillator, such as a VCO, with a phase of a reference signal FREF. As the output drifts, detected errors produce correction commands to the oscillator, which responds in a negative-feedback controller. In general, the indirect synthesizer uses a PLL and a programmable fractional-N divider, which multiplies the stable reference frequency. In the loop, a loop filter is present so as to suppress spurs produced in the phase detector so that they do not cause unacceptable frequency modulation in the VCO. However, the filter causes degradation in transient response, which limits the switching time. Therefore, the requirements for frequency switching time and suppression of spurs are in conflict.

2.2. Overview of Phase-Locked Loop

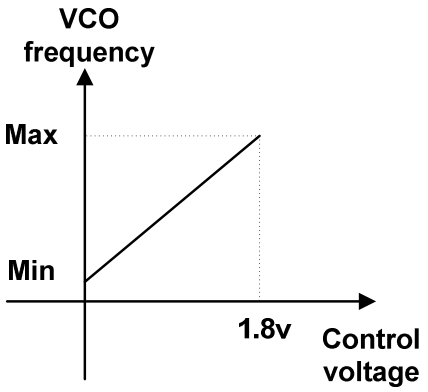
A typical Phase-locked loop (PLL) consists of phase/frequency detector (PFD), loop

filter, voltage-controlled oscillator (VCO) and frequency divider, as shown in Fig. 2-3. PFD detects the phase/frequency error between the REF CLK and DIV CLK, and sends to the Loop filter. Usually, PFD gives UP/DOWN signal into a charge pump for translate error signal from current to voltage. Loop filter provides a smooth control voltage to VCO. Therefore, VCO can provide desired output clock and feedback to frequency divider to form a negative feedback loop. The PLL has several analog devices such as charge pump, loop filter and VCO. Oscillator is one of the most important parts in PLL. There has been a significant research effort in VCO for WLAN application [2]. VCO can provide almost perfect sinusoidal signal. However, several fundamental issues such as control linearity, frequency resolution, power consumption and cost area need to be considered.

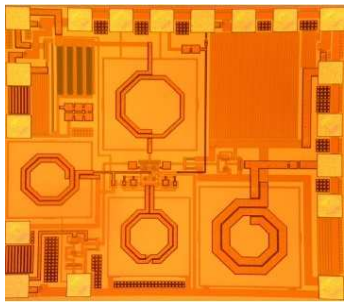


(Fig. 2-3)

Fig.2-4-1 shows the relation between control-voltage and VCO output frequency. In IEEE-802.11a [9], it uses Unlicensed National Information Infrastructure (U-NII) from 5150 to 5825MHz. It means that if the control-voltage is 1.8V, it must provide voltage resolution down to 135mV for 5MHz resolution. Besides, VCO is usually composed of inductor and capacitor for oscillator circuit. Fig.2-4-2 [2] shows the spiral structure of inductor. The inductors occupy most of the chip area. And it is usually layout by fully customer. Fully-customer layout technique is very critical part for performance.



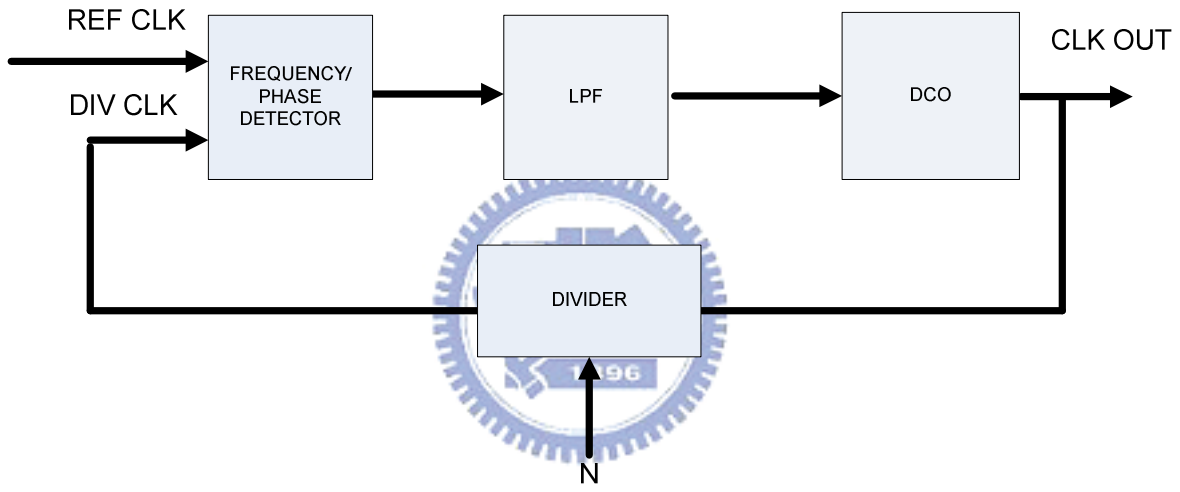
(Fig.2-4-1)



(Fig.2-4-2)

2.3. Frequency Synthesizer based on All-Digital Phase-locked Loop

Basically, ADPLL based Frequency synthesizer is the same as the induction in Section 2.1.3. It takes out the analog components such as loop filter and VCO. The architecture shows in Fig. 2-5. The divider in frequency synthesizer is usually programmable. It divided the DCO output clock by “N” before into PFD. So, divided clock synchronize with reference clock thus DCO clock will be N times of reference clock. This mechanism makes synthesizer can synthesis different clock. However, it also comes with issues such as long locking cycle and jitter.



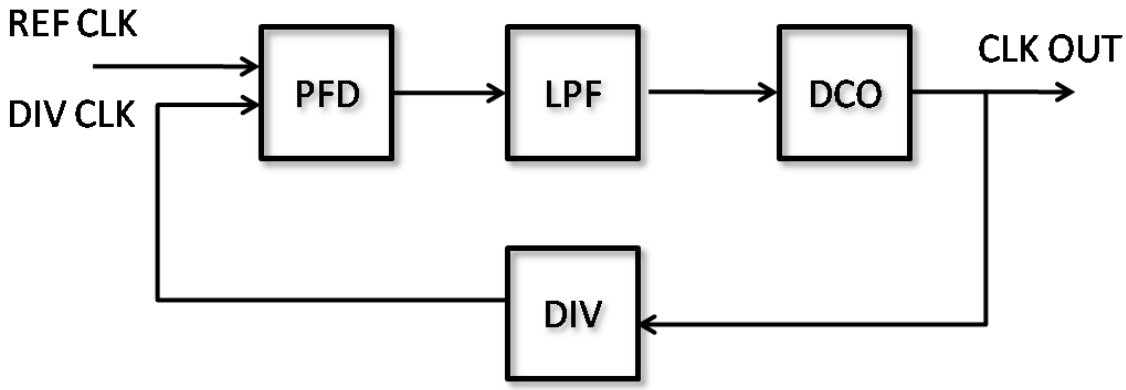
(Fig.2-5)

Chapter 3
The Proposed All-Digital Phase-Locked Loop

In this chapter, a detail description for the proposed frequency synthesizer based on ADPLL is given.

3.1. All-Digital Phase-Locked Loop Architecture Overview

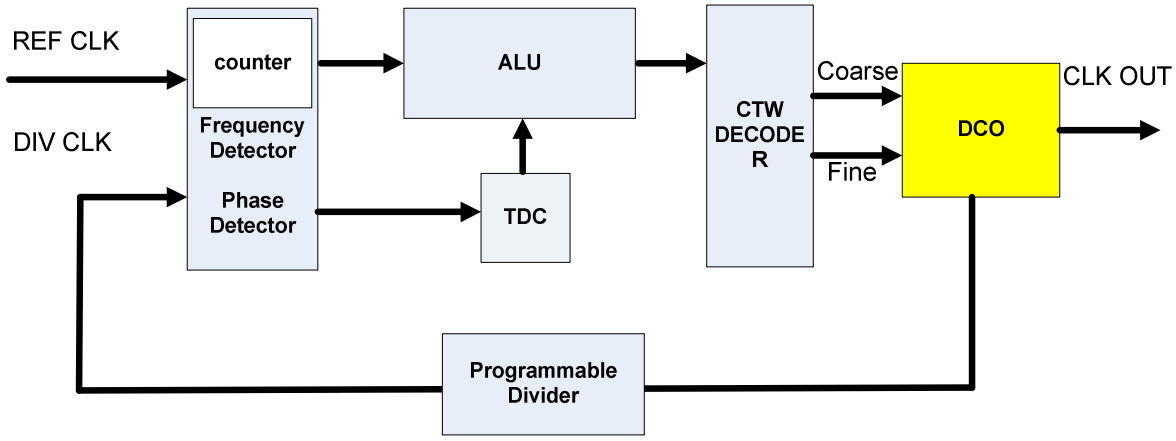
The ADPLL is shown in Fig. 3-1. It has four major function blocks, such as PFD, Loop Filter, digital-control-oscillator (DCO) and loop divider. PFD detects the difference between extern reference clock and divided clock. Its output signal indicates the divided clock slower or faster than reference clock. There are three main considerations in designing PFD, Glitch, Dead Zone and Operation Frequency. Loop filter used to eliminate glitch, jitter and smooth the control signal. DCO gives output clock by the control signal.



(Fig. 3-1)

ADPLL is the core of this proposed Frequency Synthesizer. In this paper, an ADPLL is proposed to against control linearity, frequency, power consumption and area. A low complexity of ADPLL is proposed to reduce gate count and power consumption. Standard cell is used to implement the DCO and achieve wide-bandwidth and high frequency resolution. We utilize the digital circuit design techniques to gain the analog circuit design benefit. The ADPLL can be divided into three basic functions, such as frequency tracking, frequency evaluation and clock generation. The proposed ADPLL block diagram is shown in Fig.3-2. Frequency detector, Phase detector and TDC are used for tracking frequency error. ALU is used to calculate the DCO command word from frequency error. DCO and frequency

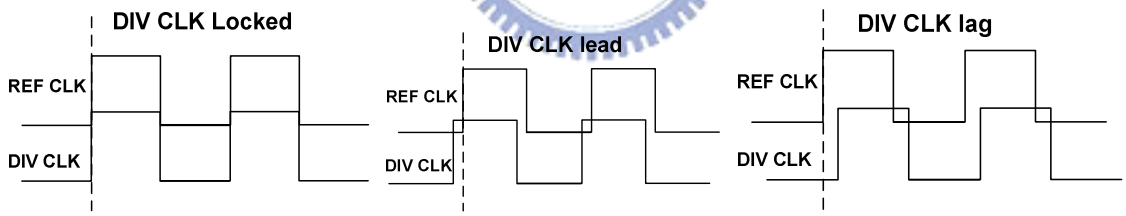
divider are used for clock generation.



(Fig. 3-2)

3.1.1. The tracking algorithm

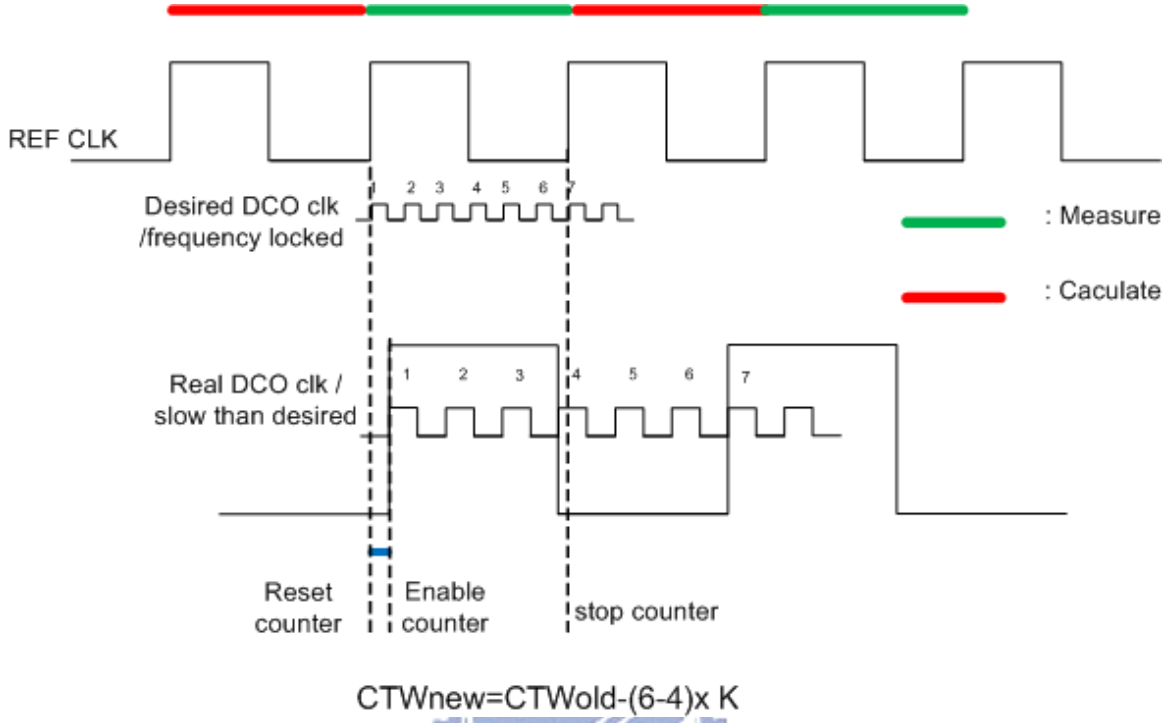
In this section, the proposed frequency/phase tracking algorithm is described. The goal of the tracking algorithm is to make different source clock “synchronized”. At beginning, we take an arbiter time to compare two clocks reference clock and internal divided clock, named REF and DIV clock respectively. Obviously, there are three schemes between the REF and DIV clock. First, the difference between two clocks (frequency error) is small enough. This scheme is called “Frequency locked” as Fig.3-3-1. Second, the internal DCO clock is faster than reference clock. This scheme called “Frequency lead” as Fig.3-3-2, whereas called “Frequency lag” as Fig.3-3-3.



(Fig.3-3-1) (Fig.3-3-2) (Fig.3-3-3)

As introduction in chapter 2, Frequency synthesizer is designed to synthesis the required frequency from reference frequency. ADPLL needs stay in locked state. If not, Controller issues the control signal to slower or faster DCO output frequency. Thus, the controller has to determine which scheme that ADPLL stays now. This proposed tracking algorithm use a frequency counter to detect frequency error instead of using PFD directly. In order to detect the scheme, a number “N” has been given in the frequency counter. The frequency counter starts to count the DCO clock from positive edge of reference clock and stop at next positive edge. This approach can prevent from doing clock retiming in ADPLL and then the ADPLL will be low complexity. First, if the counter counts number “N-counter” smaller than the number “N-set”. It means that DCO clock is slower than reference clock. For example, the target frequency is six times of reference clock. In other words, there are six DCO clock

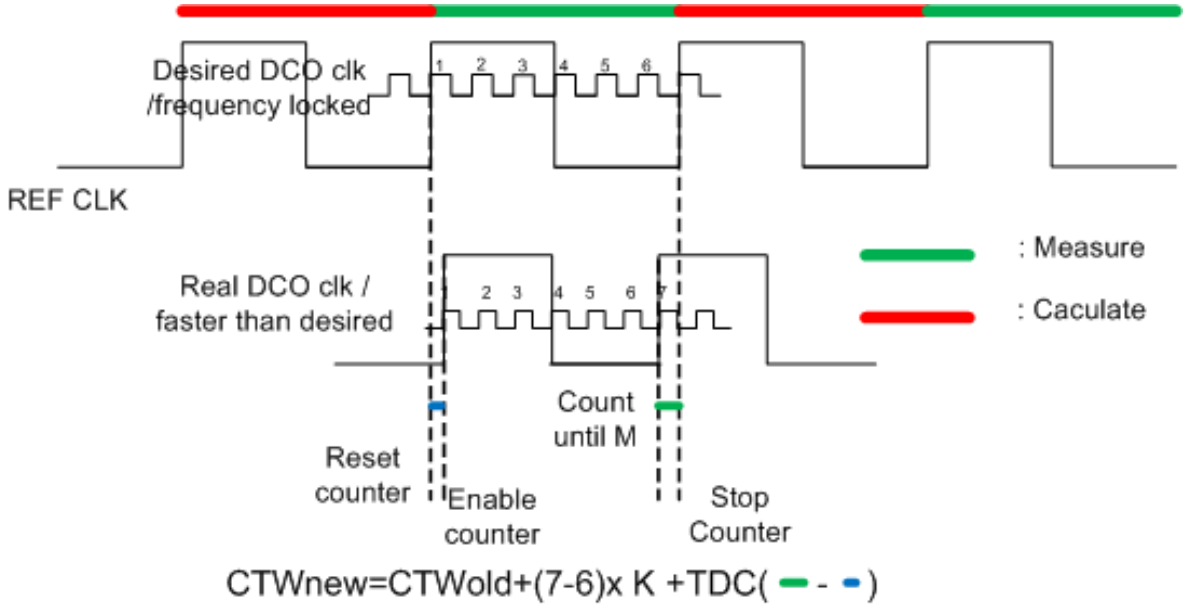
cycles in one reference clock cycle. Thus, if the frequency counter number is smaller than six, it means one reference clock cycle don't have six DCO clock cycles. So, the DCO clock is slower than the required. Fig.3-4-1 shows this scheme. The top of green line indicates the counter is active.



CTWnew=CTWold-(6-4)x K

(Fig.3-4-1)

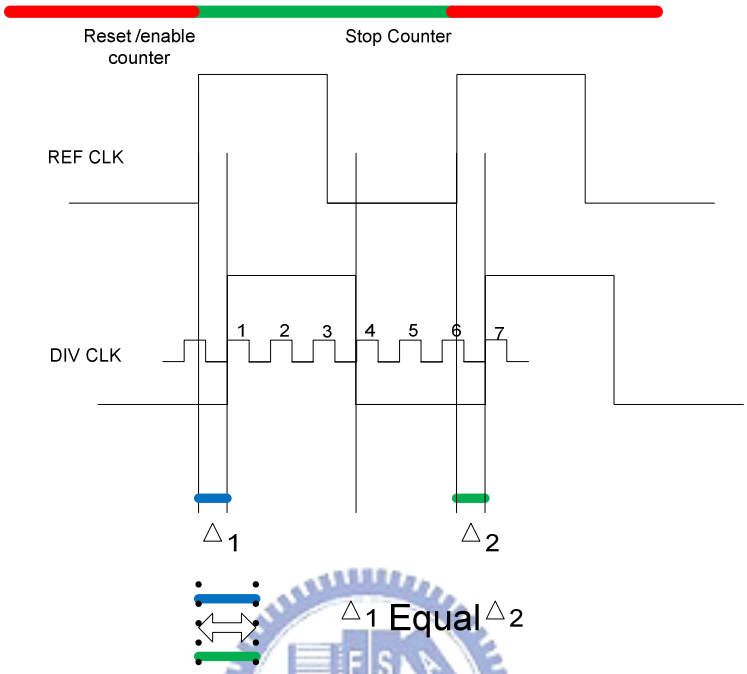
Fig.3-4-2 shows the second scheme. If the number "N-counter" of the counter is bigger than "N-set", it means that DCO clock is faster than reference clock. In this example, the target frequency is six times of reference clock. It means in one reference clock have more than six DCO clock. So, the DCO clock is faster than required.



CTWnew=CTWold+(7-6)x K +TDC(-)

(Fig.3-4-2)

Fig.3-4-3 shows the last scheme, the frequency error is smaller than frequency counter detection range. So the frequency counter count number “N-counter” exactly same as the number “N-set”. It represents the frequency is locked. In those schemes, delta1 and delta2 is the phase error. TDC is used to detect the small phase error.



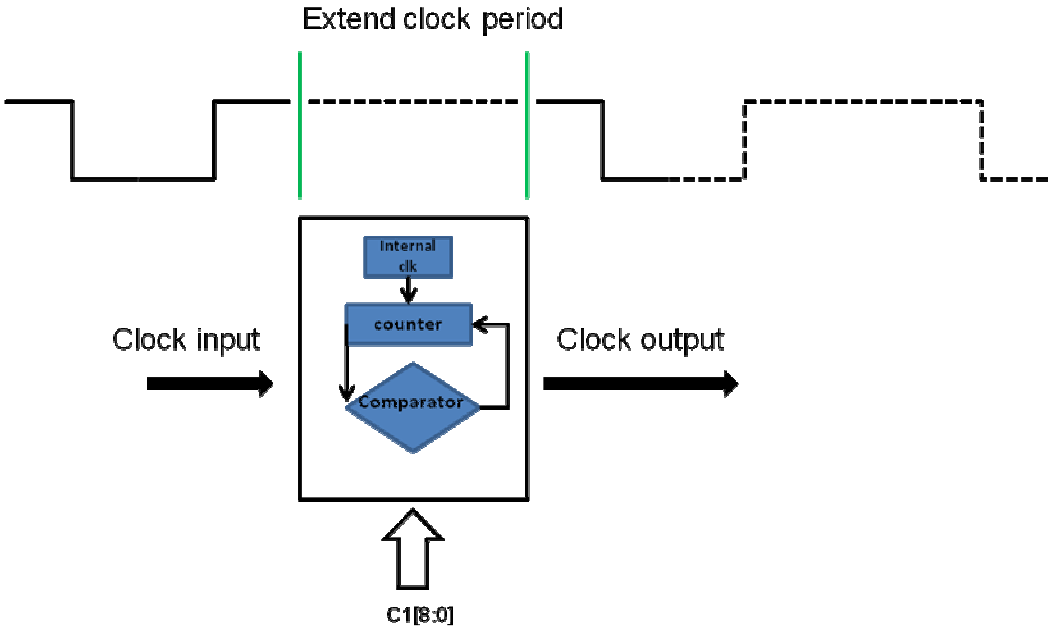
(Fig.3-4-3)

3.2. Basic concept of DCO Implementations

In this section, we will introduce basic concept of the proposed DCO. The proposed DCO are based on DTC, ring oscillator, DCV [6] techniques.

3.2.1. Digital-to-Time converter

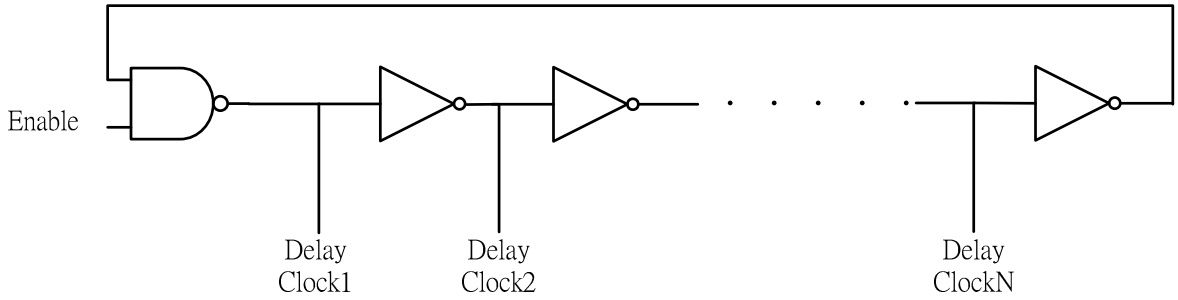
Digital-to-Time converter is used for extending DCO operation frequency range. Fig.3-5 shows the basic idea. It uses internal counter to count the extend clock cycle. The input control word C1 determines how many internal cycles will add to input clock cycle. For example, the one internal cycle is “S ns” that C1=20. It will provide 20*s ns delay to original input clock. In general, the DTC is one of the delay elements in the DCO.



(Fig.3-5)

3.2.2. Ring Oscillator

A basic Ring Oscillator is a delay chain that contains many inverters. Fig.3-6 shows the diagram. Each inverter cell has gate delay, various number of inverter can provide different delay clock. Equation $T = \frac{C_L \times \Delta V}{I_d}$ (Eq. 3-1) expressed the delay of each inverter cell. Where C_L is load capacitance, Δ_V is the output voltage swing, and I_d is the driving current to the load. From (1) we can express the Ring Oscillator Frequency in $f_{ro} = \frac{1}{2NT}$ (Eq. 3-2). Changing number of inverter stages or the load capacitance or driving current to the load, either can change the clock period. [5]

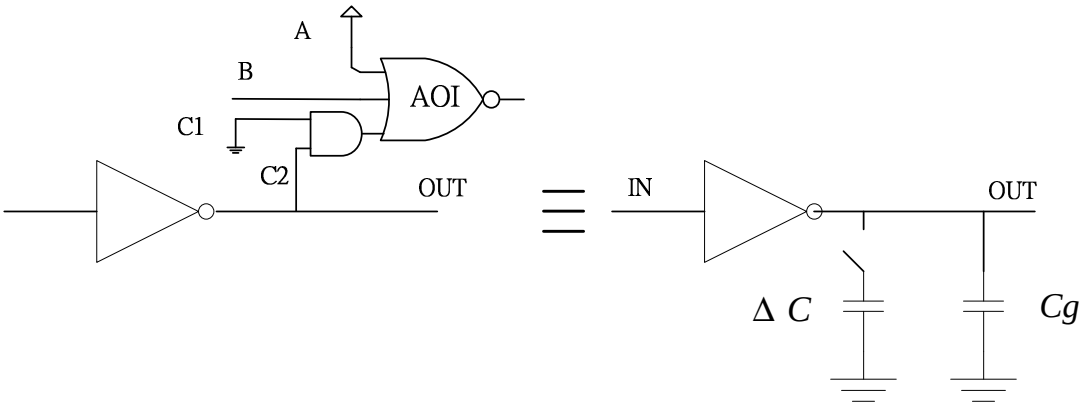


(Fig. 3-6)

3.2.3. Digitally controlled Varactor (DCV)

The minimum resolution of inverter delay chain is limited by the gate delay. According to a well know concept $\text{Delay } \tau = R\,C$, attach a delta capacitance on delay chain will change the delay time [6]. In this work, using and-or-inverter standard cell forms the digitally

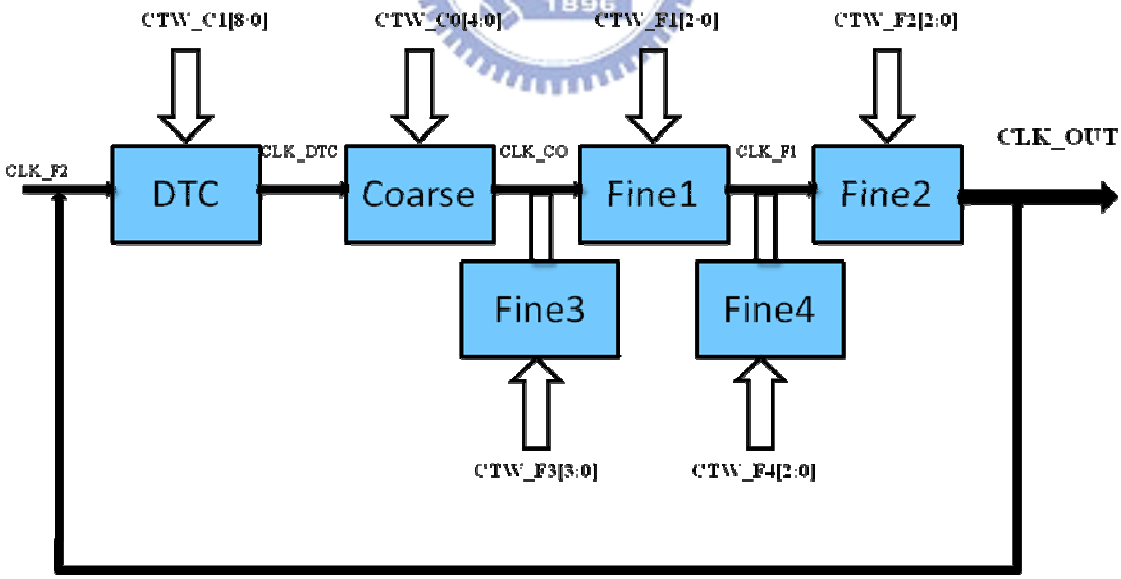
controlled varactor as shown in Fig. 3-7. The digitally controlled varactor is not limited by the gate delay, so the resolution can be enhance.



(Fig. 3-7)

3.3. Standard Cell-based Digital-Control-Oscillator (DCO)

Since DCO is the heart of the ADPLL, it domains the performance of the ADPLL like jitter. We propose a high resolution Standard Cell-based Digital-Control-Oscillator to again jitter. The architecture has three major function blocks such as Digital to Time converter, coarse tune cell and Fine tune cell. Fig.3-8 shows the function blocks.



(Fig. 3-8)

In this work, there are 27 control bits for frequency adjustment. Each cell control bits illustration as below. DTC has 9 bits (C1[8:0]) for extending operation frequency range. Coarse tune cell has 5 bits (C0[4:0]) for select different delay line. First fine tune cell has 3 bits (F1[2:0]) that would be binary decoded to 7 control stages, each stage provided 4.4ps.

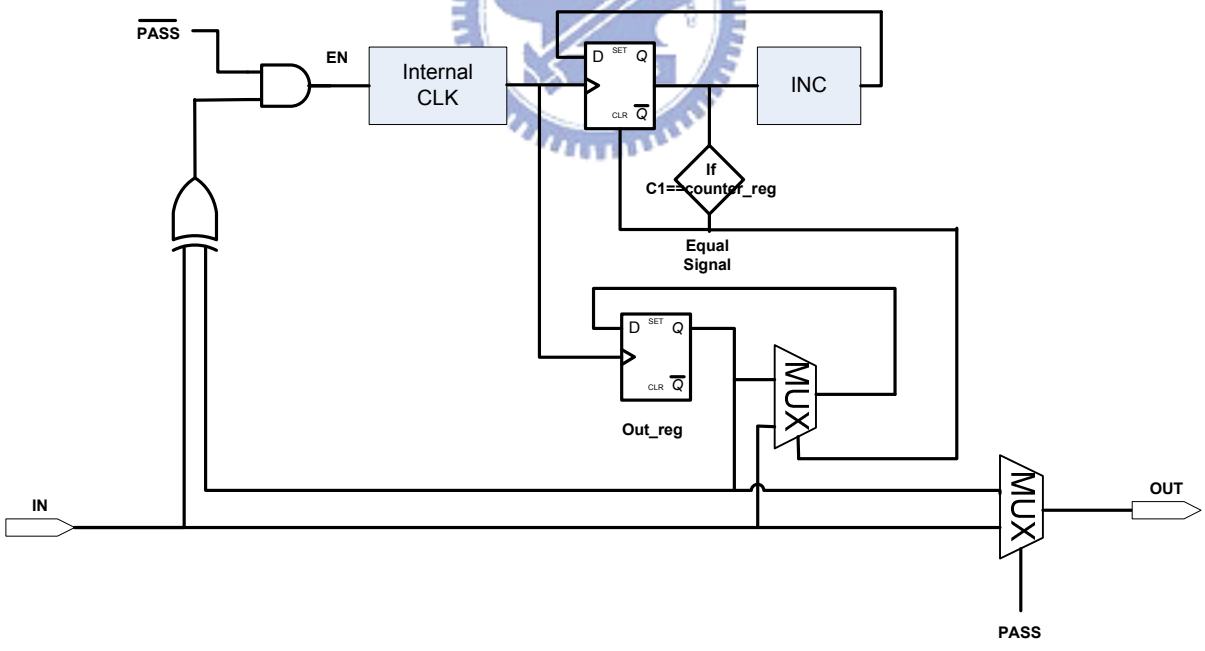
Second fine tune cell has 3 bits (F2[2:0]) that would be binary decoded to 7 control stages. Each stage provided 835fs. The third and the fourth fine-tune cell are not the same as the first and the second fine-tune cell since these didn't pass clock, these affect the clock period by using DCV [6]. Third fine tune cell has 4 bits (F3[3:0]) decoded to 15 control stage, each stage provided 67.8fs. The fourth fine-tune cell is the last fine-tune cell that influences LSB resolution. This work achieves the minimum resolution to 10fs

Table 3.1

	Coarse-search	Fine-search			
		First sub-cell	Second sub-cell	Third sub-cell	Fourth sub-cell
Cell name	Inverter and NAND	OAI	OAI	OAI	AOI
Control bits	5	3	3	4	3
stages	32	7	7	15	7
resolution	30ps	4.4ps	835fs	67.8fs	10fs

3.3.1. Digital to Time Converter DTC

DTC gives a wide-bandwidth operation function in DCO. It contains counter multiplex and an oscillator ring for internal clock generation. The basic idea is to extend an extract period by the counter. Fig.3-9 shows the architecture.



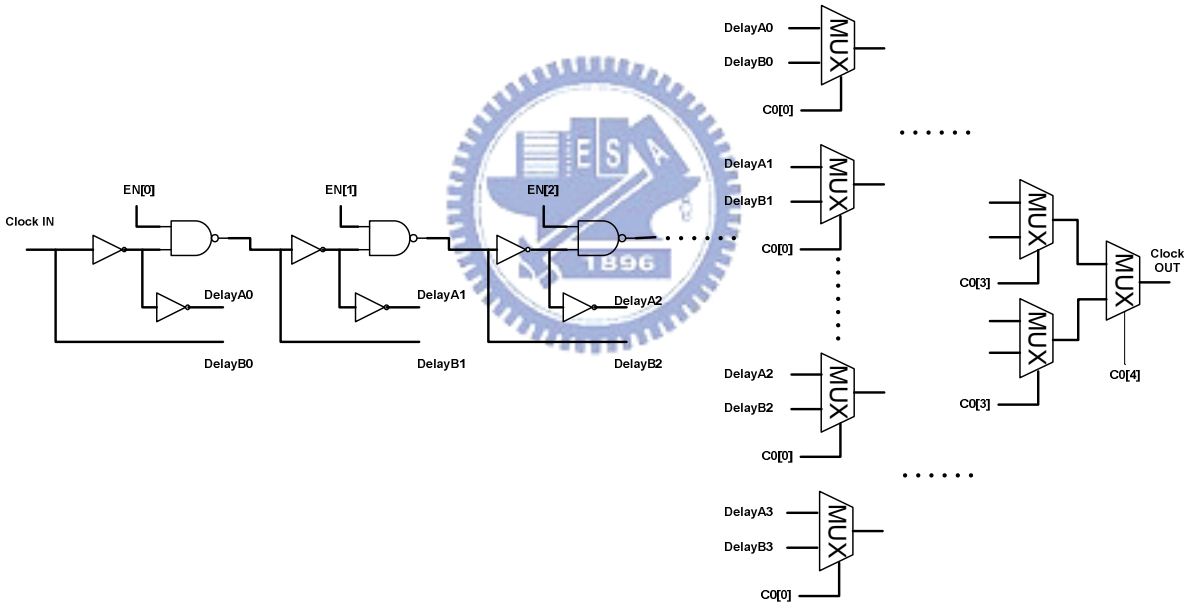
(Fig.3-9)

The counter counts internal clock compare with setting C1[8:0]. Because the input signal "IN" has different signal level that triggers the control signal "EN" to be high, the counter starts to count internal clock. If counter's value is the same as setting C1[8:0], "Equal" is asserted. Input signal "IN" passes through multiplex so the output register

“Out_reg” changes the signal level. Then output signal goes to next stage of DCO. The control setting determines the working period of the counter. If the setting C1[8:0] is “511” that has the longest counter working period so the maximum extended clock period is gotten. If the setting C1[8:0] is “0” the “Equal” is always high. The minimum clock period is gotten. The DTC internal clock period is 906ps. The maximum and minimum clock period is 930ns and 2.95ns separately. While C1[8:0] increase, the DTC increases 1.8ns by step. The frequency range is from 1MHz to 338.8MHz. The DTC has designed to the operation frequency range. Using fine tune cell can get high solution. In this work, 10fs resolution has been proposed. Besides, DTC can increase operation without increasing chip area. That is not practical to use DRV cell only for wide-bandwidth, because it needs a lot of chip area.

3.3.2. Coarse-tune cell

After DTC stage is coarse-tune cell. In this coarse-tune cell consists of many inverters and NANDs. Furthermore, the delay chain can be separated into different segments. The basic idea of coarse-tune cell is to use multiplex for selecting different delay chain.



(Fig.3-10)

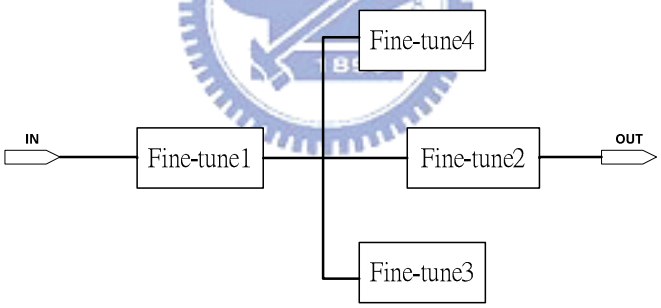
This Coarse-tune cell has 5 bits controlled word that 5 bits is decoded to 2^5 =32. Thus, this coarse-tune cell has 32 different selections. Fig.3-12 shows the delay path and multiplex select array. These multiplexers could be separated into five groups that are mapped to 5 control bits. Every multiplex has the same principle that input delay path “DelayA” is longer than input delay path “DelayB”. When the multiplex select signal is “high”, the output is selected from input “DelayA”. Therefore, the control word C0[4:0]=[11111] has the longest delay path. When C0[4:0] =[00000], the selected path is minimum, the delay time is intrinsic delay pass through 5 multiplexers. Because we used binary decode, the control words C0[4], C0[3]… C0[0] have different weight. Each control bit is just mapped to each multiplex group.

The LSB C0[0] controls the first multiplex group. In this group each multiplex input path “DelayA” is added two more delay stages then input path “DelayB”. In this group, the delay path “DelayB” is selected while multiplex select signal is high. In other words, control bit C0[0] is high will select longer delay path, hence longer delay time been provided. The next multiplex group is the same as above. Multiplex select signal is high will provide longer delay time. There is another advantage used NAND cell in delay path, if the delay path had not been selected then the signal behind won’t transition. It means save power consumption.

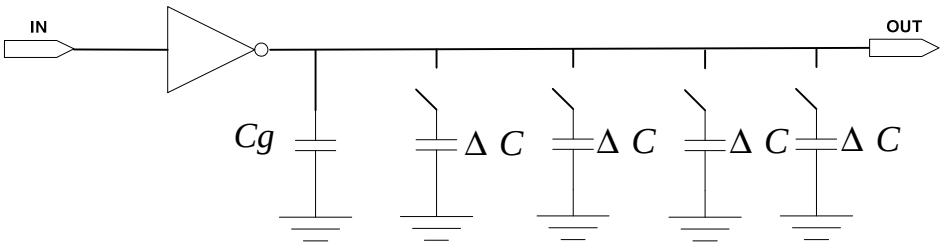
3.3.3. Fine-tune cell

Fine-tune cell is designed to provide high resolution. In order to get high frequency resolution without too many cell. Fine-tune cell separate to four stage that first (Fine1), second (Fine2), third (Fine3) and fourth (Fine4). Each stage has different resolution. First fine-tune cell and Second fine-tune cell are cascade. Fine3 and Fine4 is joint the clock path but clock didn’t pass through directly. This can decrease total gate delay, prevent the clock path pass through too much gate. The minimum resolution is 10fs provided from fourth fine-tune cell. Beside, for linearity operation each stage’s tuning range will overlap to next stage. First fine-tune cell LSB is overlapped to second fine-tune cell MSB and so on.

Fig.3-11 shows the inter-connection between fine-tune cell. Fig.3-12 present the fine-tune cell as addition capacitors.



(Fig.3-11)



(Fig.3-12)

First fine-tune cell used OAI standard cell, there are 7 stages in Fine1. The control word from F1[6:0] =[000_0000] to F1[6:0]=[000_0001] turn on one control stage, the delay time add one stage delay 4.4ps. F1[6:0]=[000_0000] to F1[6:0]=[111_1111] tun on seven control

stages, so the delay time increases : $30.8ps = 4.4ps \times 7$.

Fine2 used OAI and also has 7 stages. The control word F2[6:0]=[000_0000] to F2[6:0]=[000_0001] turn on one control stage, the delay time increases 835 Femto-second(fs). Also F2[6:0]=[000_0000] to F2[6:0]=[111_1111] turn on 7 stages, the delay time will add : $5854fs = 835fs \times 7$. Fine2 maximum delay time 5845fs is longer than Fine1 minimum delay time 4400fs.

Fine3 has 15 stages and its control word logic is opposite to other fine-tune cell. While F3[14:0]=[00…0000] to F3[14:0]=[00…0001], the delay time is decreased 67.8fs. However, it won't affect the control linearity. Fine3 maximum delay time is $1017fs = 67.8fs \times 15$ also can cover the Fine2 minimum delay time. Fine4 cell used AOI cell to achieve 10f s resolution. F4[6:0]=[000_0000] to F4[6:0]=[000_0001], the delay time is add 10fs. The maximum delay is $70fs = 10fs \times 7$

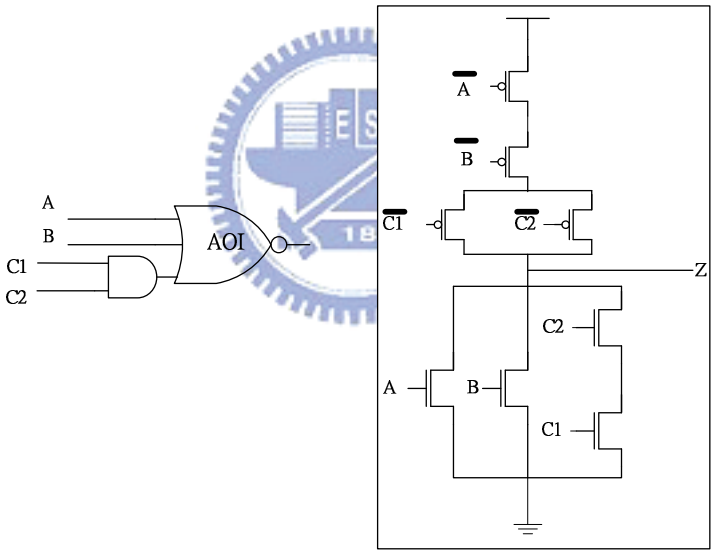
Chapter 4

Simulation and Layout

In this chapter, we illustrate the hardware implementation and simulation. The steps of the semi-fully layout are introduced in appendix A.

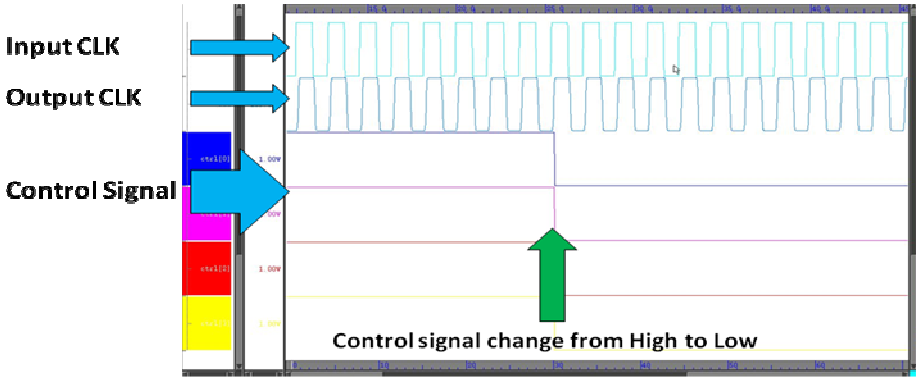
4.1.SPICE simulation

As illustration above, the minimum DCO resolution is provided by fine-tune cell. We used SPICE simulation to find out every standard cell's delay time. Fig. 4-1 shows the schematic of and-or-inverter (AOI) cell.



(Fig. 4-1)

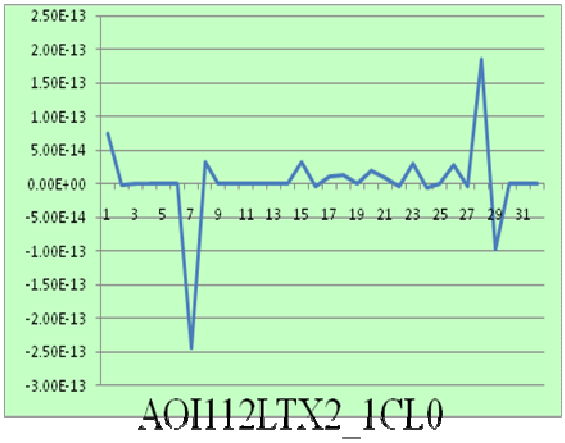
There are four input pins A, B, C1 and C2 in AOI cell. The purpose of SPICE simulation is to find the resolution by the setting of AOI input pins. As VLSI technology, we knows that measured pin A capacitance at pin's level (B,C1,C2)=[0 0 1] is different with (B,C1,C2)=[0 0 0]. Assumption the difference of capacitance is ΔC from Eq. 3-1 will get the ΔT. Thus, pin A as load and pin C2 as control pin. Fig. 4-2 shows the simulation wave form.



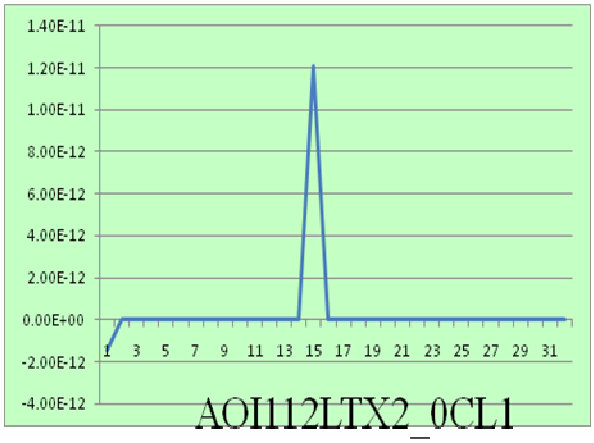
(Fig. 4-2)

That is one of the simulation conditions for pin A as load and pin C2 as control. There are total 48 simulation conditions in one standard cell, and we take all of the AOI and OAI cells in CIC 90nm cell library. The 48 simulation conditions come from selected one control pins and one load pin in 4 pins. And other two pins could be [0 0] [0 1] … [1 1] total 8 condition. The simple derivation as follow: $8 \times C_2^4 = 8 \times 6 = 48$.

Next, analyze all the simulation results then pick up which conditions can meet request. Due to the huge data, using analyze tool is necessary. First, the simulation is to select the delay time will response as control signal, as we discussion above. Fig. 4-3-1 and Fig 4-3-2 show the relation between control signal and cycle-to-cycle jitter. Both plot come from AOI standard cell named AOI112LTX2, but different pins arrange. In Fig. 4-3-1, pins arrangement is (A,B,C1,C2)=[1CL0]. In Fig. 4-3-2, pins arrangement is (A,B,C1,C2)=[1CL0].This is an opposite result; The cycle-to-cycle jitter in Fig. 4-2-1 is variance all the simulate time, changing the control signal didn't affect the delay time. The cycle-to-cycle jitter in Fig. 4-2-2 is related to control signal. It is a stable result that we can pick up for candidate.



(Fig. 4-3-1)



(Fig. 4-3-2)

After finish this step around all of the standard cells, all the result has sorted by rise and fall time as show in Fig. 4-4. The sorting table helps us to select which cell and pins arrangement

can meet our request. The rise and fall time balance is necessary. Finally, we can get what pins arrangement of standard cells as we need.

	Cell name	PIN 排列	Rise time	Fall time	Difference R/F time	
OAI	LTX1P	L01C	-2.29E-16	-2.46E-16	1.7E-17	-7.42%
OAI	LTX1	OC1L	-6.77E-16	-6.40E-16	3.7E-17	-5.47%
AOI	LTX2	C1OL	4.27E-15	4.70E-15	4.3E-16	10.07%
OAI	LTX1	C00L	-7.04E-16	-1.28E-15	5.76E-16	-81.82%
OAI	LTX1P	L0C1	-1.18E-14	-1.32E-15	1.05E-14	-88.81%
AOI	LTXLP	C1L0	-6.04E-14	-8.34E-14	2.3E-14	-38.08%
OAI	LTXLP	C00L	-1.60E-13	-1.87E-13	2.7E-14	-16.88%
AOI	LTX2	C1L0	-2.09E-13	-1.76E-13	3.3E-14	-15.79%
OAI	LTX2	0CL1	5.34E-13	4.79E-13	5.5E-14	-10.30%
OAI	LTXLP	L00C	9.14E-14	3.62E-14	5.52E-14	60.39%
OAI	LTX1	10CL	4.07E-13	3.38E-13	6.9E-14	16.95%
OAI	LTX1	01LC	1.13E-12	1.05E-12	8E-14	7.08%
OAI	LTX3	00CL	2.36E-13	3.28E-13	9.2E-14	38.98%
OAI	LTXLP	00CL	2.33E-13	3.49E-13	1.16E-13	49.79%
OAI	LTX3	0C0L	-1.25E-14	-1.44E-13	1.32E-13	-1052.00%
OAI	LTX1P	C0L1	6.59E-13	5.27E-13	1.32E-13	20.03%
OAI	LTX1	10LC	1.12E-12	9.61E-13	1.59E-13	14.20%
OAI	LTX1P	10CL	5.17E-13	3.23E-13	1.94E-13	37.52%
OAI	LTX1P	0CL1	6.94E-13	4.98E-13	1.96E-13	28.24%
OAI	LTXLP	10CL	3.29E-13	5.43E-13	2.14E-13	65.05%
OAI	LTXLP	10LC	8.56E-13	5.46E-13	3.1E-13	36.21%
AOI	LTX2	O1LC	-1.12E-13	-4.29E-13	3.17E-13	-283.04%
OAI	LTX1P	0C0L	1.97E-14	-3.23E-13	3.43E-13	1739.59%
OAI	LTX1	L0C0	-6.83E-13	-1.46E-12	7.77E-13	113.76%
OAI	LTX1	C11L	-8.19E-13	-1.92E-14	8E-13	-97.66%

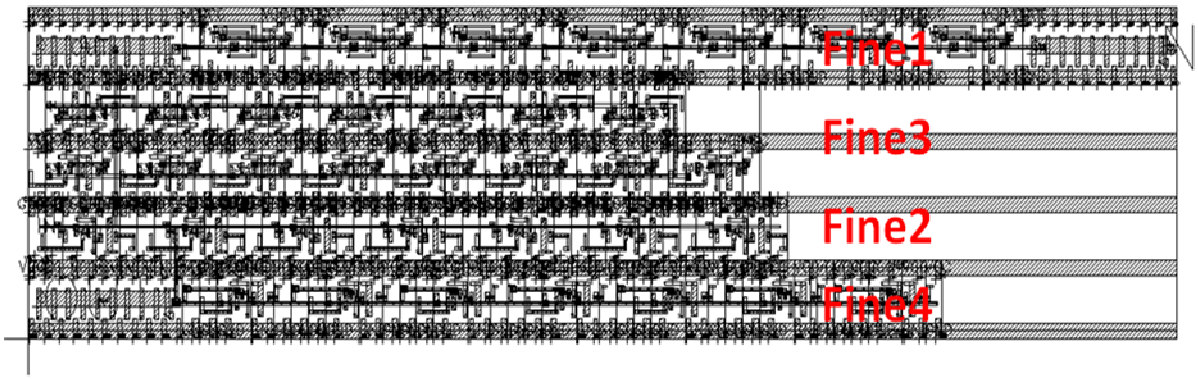
Rise Fall time unbalance

(Fig. 4-4)

4.2. Layout.

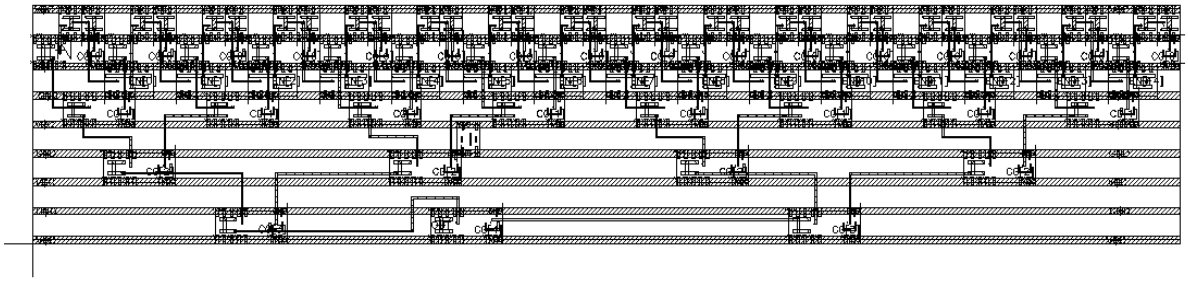
In this work, there are two layout art, one is tradition layout using EDA tools for auto place and route the other is our proposed semi-fully customer layout.

Fig. 4-4 shows the most important component, Fine-tune cell. The routing layer didn't change that can prevent extra stray capacitance. This fine-tune cell consist of four fine-tune cell. The inter connection illustrated in Fig. 3-11. The place locating is well arranged for decrease routing difficulty.



(Fig. 4-5)

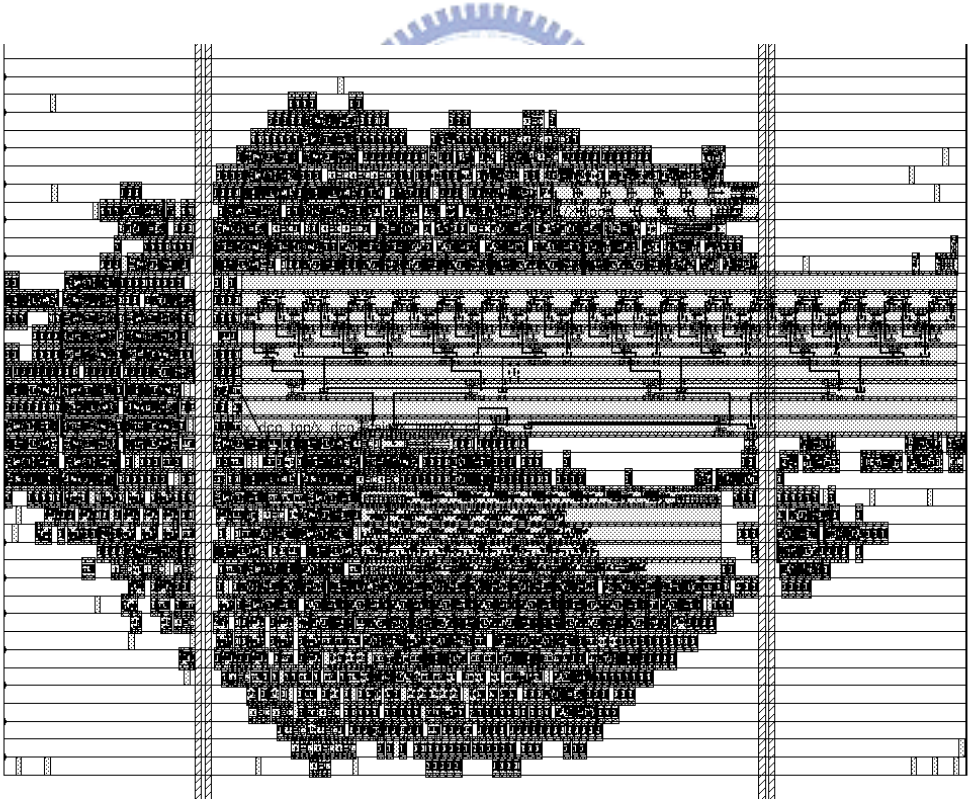
Fig. 4-5 shows the coarse tune cell. It is a delay and multiplex array. Because it is an array structure, we need to consider the path distance of the same coarse stage.



(Fig. 4-6)

Fig. 4-6 shows the whole layout. It uses EDA tool to do P&R, but contains the manual layout. The critical component layout by manual can gain the performance. The other part used EDA tools can save the time. It is similar mixed signal design flow, but in this work the fully-customer layout is unnecessary.

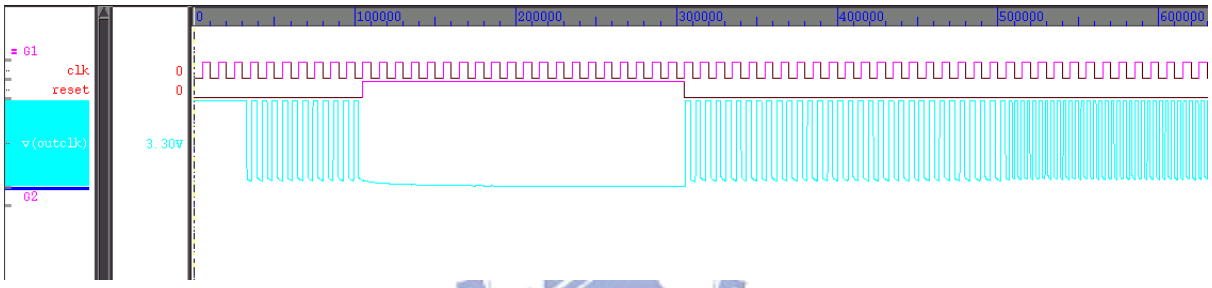
Table 4-1 shows the DCO performance. The chip area is only 687um x 687um. The power consumption is only 664.1uW in worse case. The whole chip layout shows in Fig. 4-7. We also used nano-sim to do post-layout simulation. The demonstration result shows in Fig. 4-8.



(Fig. 4-7)

Table 4-1

Item	Specification (unit)
Supply voltage	1.0 V(tc) 0.9 V(wc)
Bandwidth	187KHz~345MHz (wc) 351KHz~598MHz (tc)
Resolution	10fs
POWER Dissipation	664.1uW (wc)
Chip Size	687um*687um



(Fig. 4-8)

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In order to realize ADPLL based Frequency synthizer. The semi-fully customer layout art has proposed. It gives a new design flow in SoC design. With this art, a high-resolution of DCO can be implemented. In this work, we used standard cells which provided by CIC 90nm process to archive high resolution. The LSB resolution is 10 fs as the HSPICE simulation results. The proposed DCO frequency range is from 187 KHz~345MHz that extended by the DTC. We also give a low complexity tracking algorithm which locking time is 30 cycles in typical case.

5.2 Future Work

We have several works proposed to extend this design in the future. The proposed work is as following.

1. The coarse-tune cell was implemented by multiplexer array. It could be replaced by tri-state buffer for decrease instinct delay. If we can reduce the intrinsic delay then we can get faster operation frequency.
2. The simulations of jitter model didn't include. The performance might different with simulations. The resolution in this work is 10 fs, but the jitter induced by power bouncing noise is much more than 10 fs.
3. The tracking algorithm can be replaced for faster locking time. This algorithm is design for low complexity. The main purpose is to make sure the DCO can be controlled. This work focus on wide-bandwidth and high-resolution. However, the tracking algorithm still has 30 cycles locking time in typical case.
4. To complete the measure is our next work. Building the testing PCB board and test fixtures are also big challenge. The measure uncertainty needs to be considered.

Bibliography

[1] Terng-Yin Hsu, chung-Cheng Wang, and Chen-Yi Lee, “Design and analysis of a Portable High-Speed Clock Generator,” IEEE Transactions on Circuit and Systems II: Analog and Digital signal Processing, vol. 48, pp. 367-375, Apr. 2001.

[2] Yijoo Shin*, Taewon Kim, Sangwoo Kim, Sungkwon Jang, and Bokki Kim Department of Electronic Engineering, Kwangwoon University ‘A Low Phase Noise Fully Integrated CMOS LC VCO Using a Large Gate Length pMOS Current Source and Bias Filtering Technique for 5-GHz WLAN”.

[3] Terng-Yin Hsu, Terng-Ren Hsu, Chung-Cheng Wang, Yi-Chuan Liu, and Chen-Yi Lee “Design of a Wide-Band Frequency Synthesizer Based on TDC and DVC Techniques”.

[4] Terng-Yin Hsu, Bai-Jue Shieh, and Chen-Yi Lee “An All-Digital Phase-Locked Loop (ADPLL)-Based Clock Recovery Circuit”.

[5] Tomar, R. K. Pokharel, O. Nizhnik, H. Kanaya, and K. Yoshida “Design of 1.1 GHz Highly Linear Digitally-Controlled Ring Oscillator with Wide Tuning Range “.

[6] Pao-Lung Chen, Ching-Che Chung, and Chen-Yi Lee “A Portable Digitally Controlled Oscillator Using Novel Varactors”.

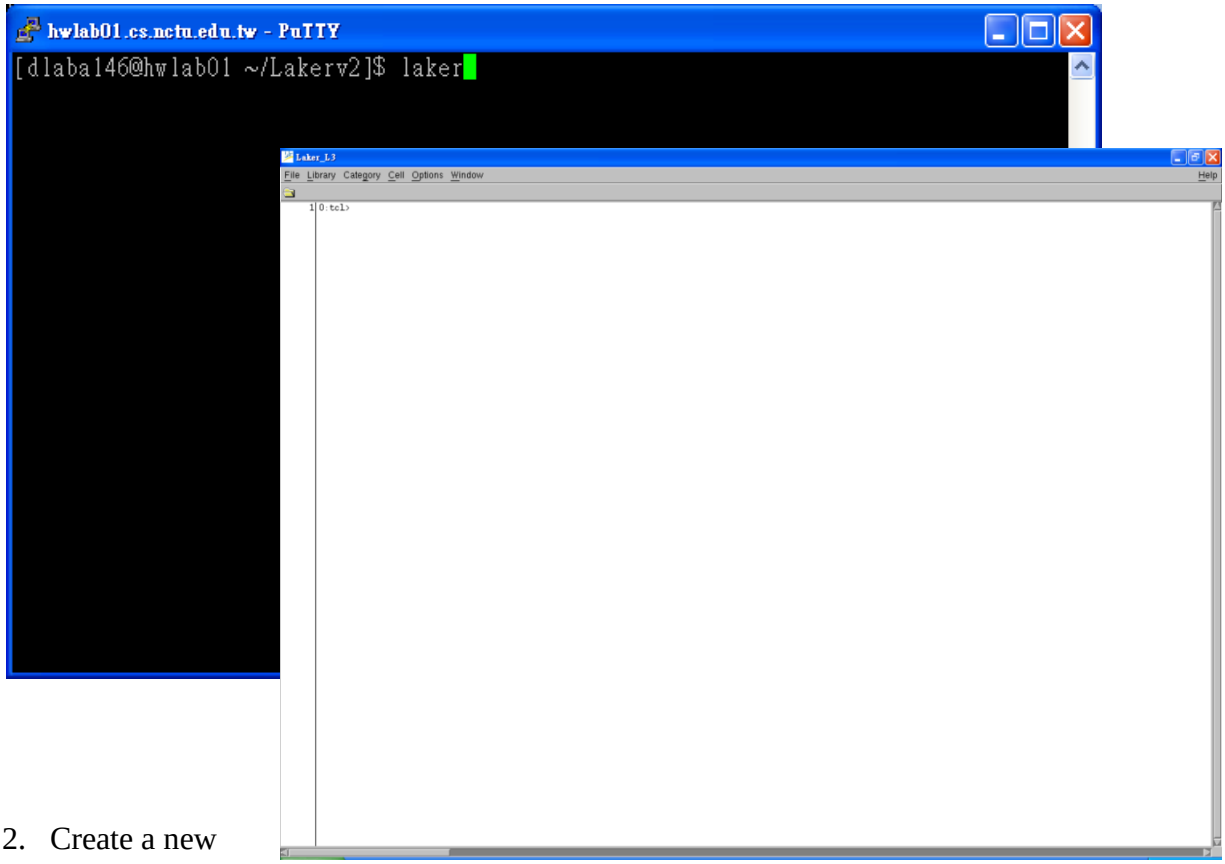
[7] Chao Xu, Winslow Sargeant, Kenneth Laker, Jan Van der Spiegel “FULLY INTEGRATED CMOS PHASE-LOCKED LOOP WITH 30MHZ TO 2GHZ LOCKING RANGE AND f35PS JITTER”.

[8] Robert Bogdan Staszewaski, Poras T. Balsara “All-Digital Frequency Synthesizer in Deep-submicron CMOS.

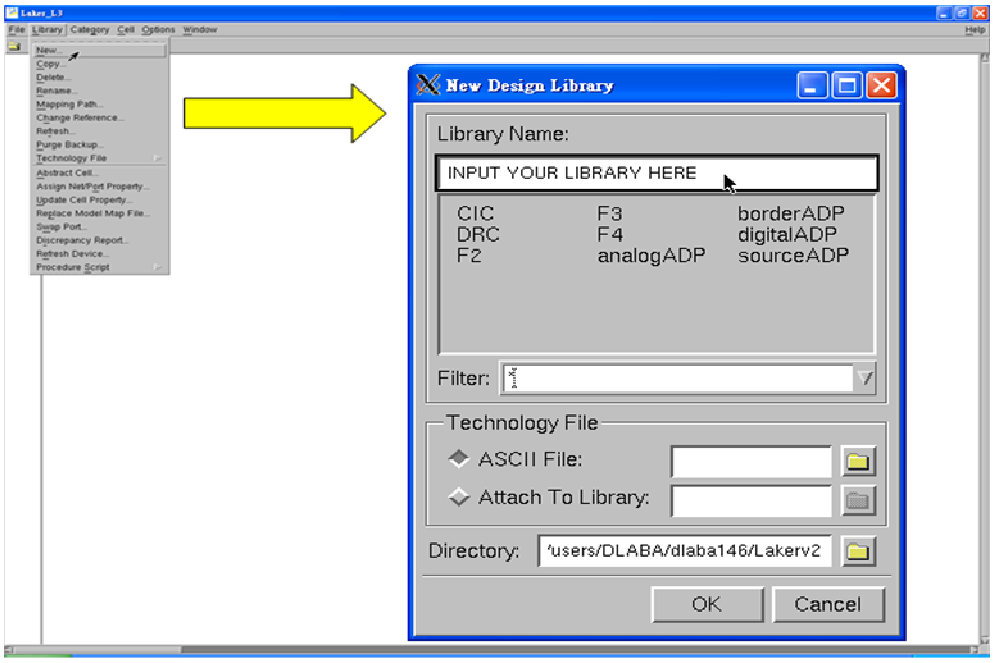
[9] Wireless Lan Medium Access Control (MAC) and Physical Layer (PHY) Specifications, IEEE Std 802.11a, 1999.

Appendix A - Laker Tour

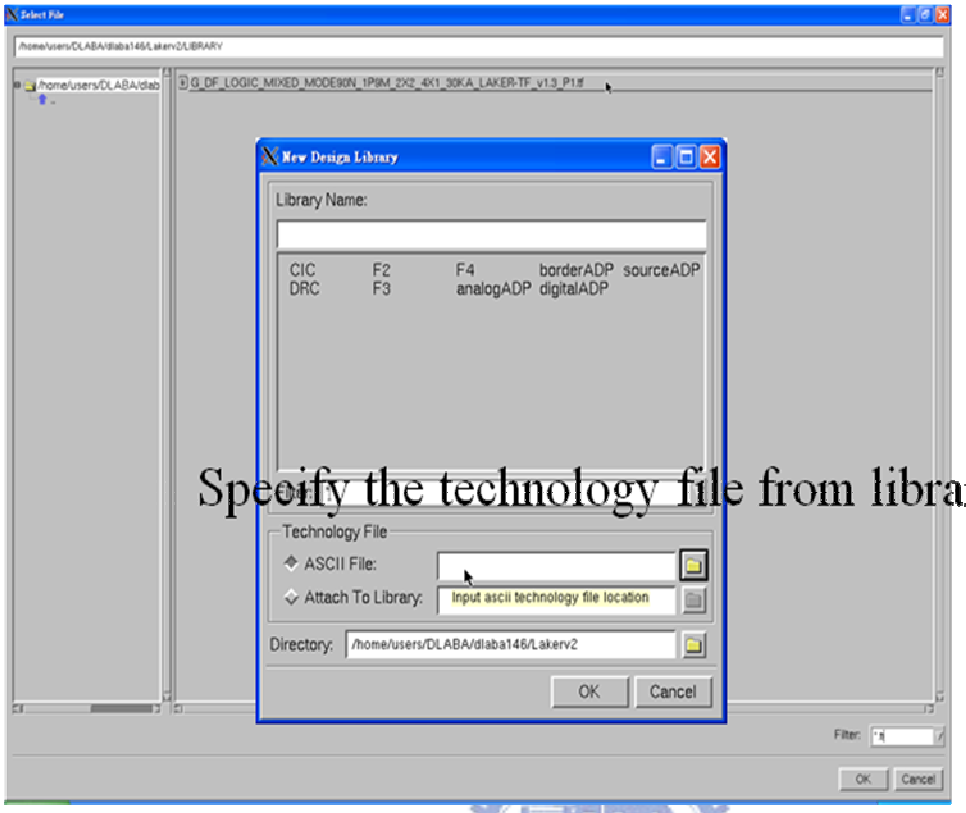
1. Type “laker” in terminal to start Laker.



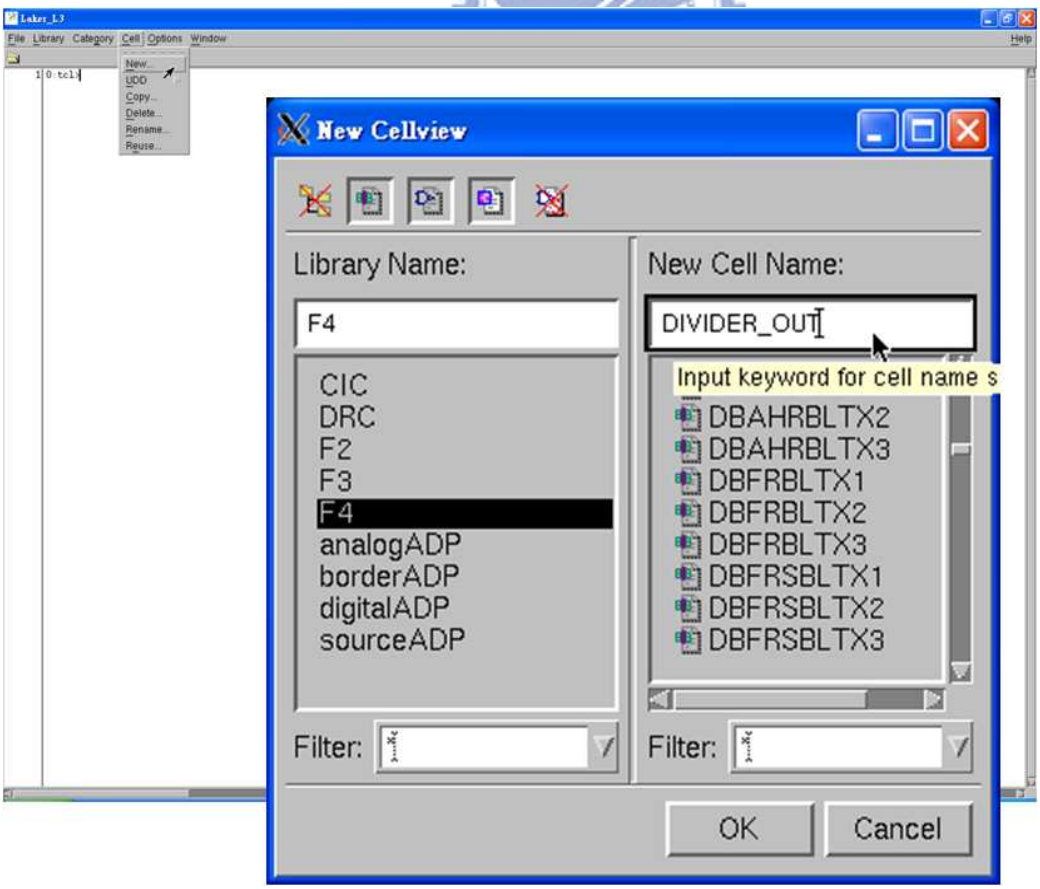
2. Create a new library and specify the library name.



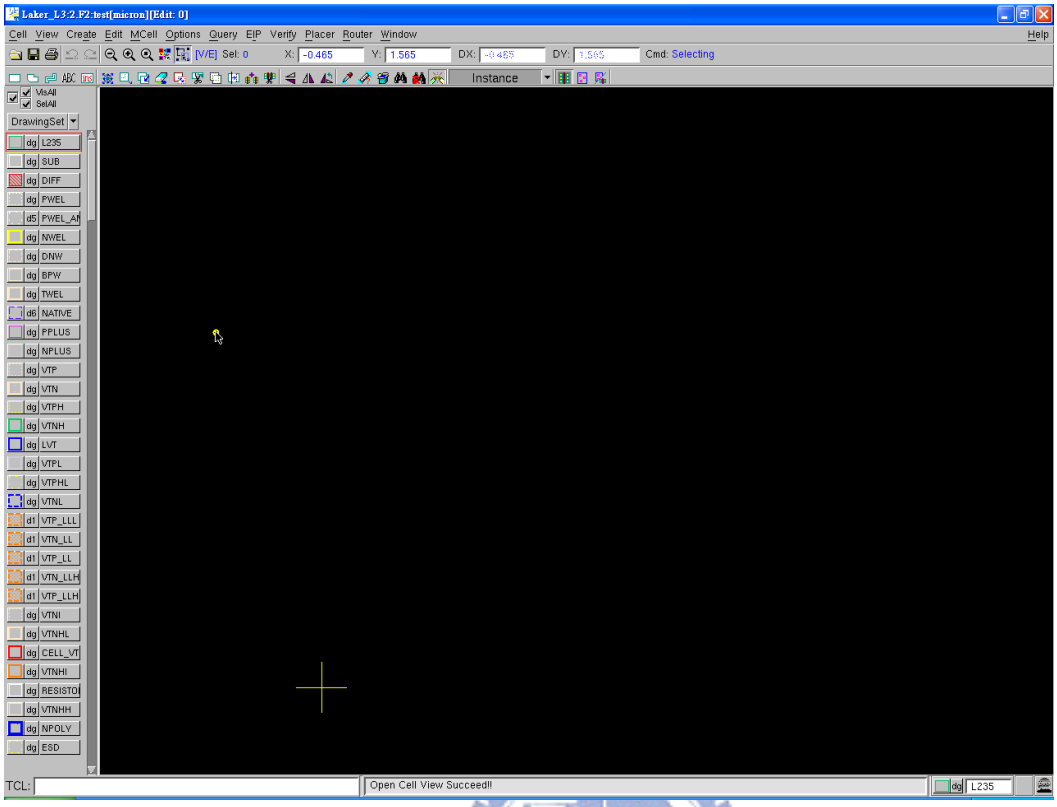
3. Specify the technology file from library.



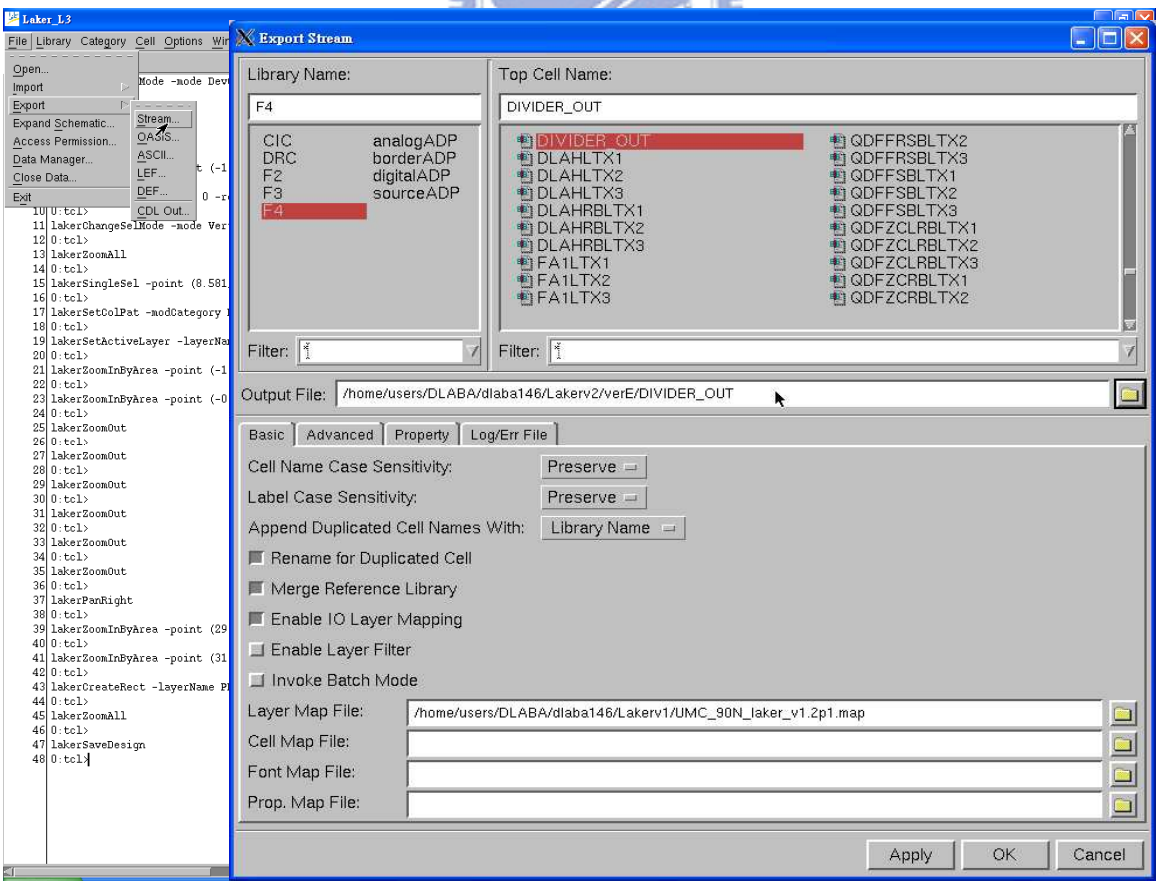
4. Create a new cell for layout



5. Start edit layout

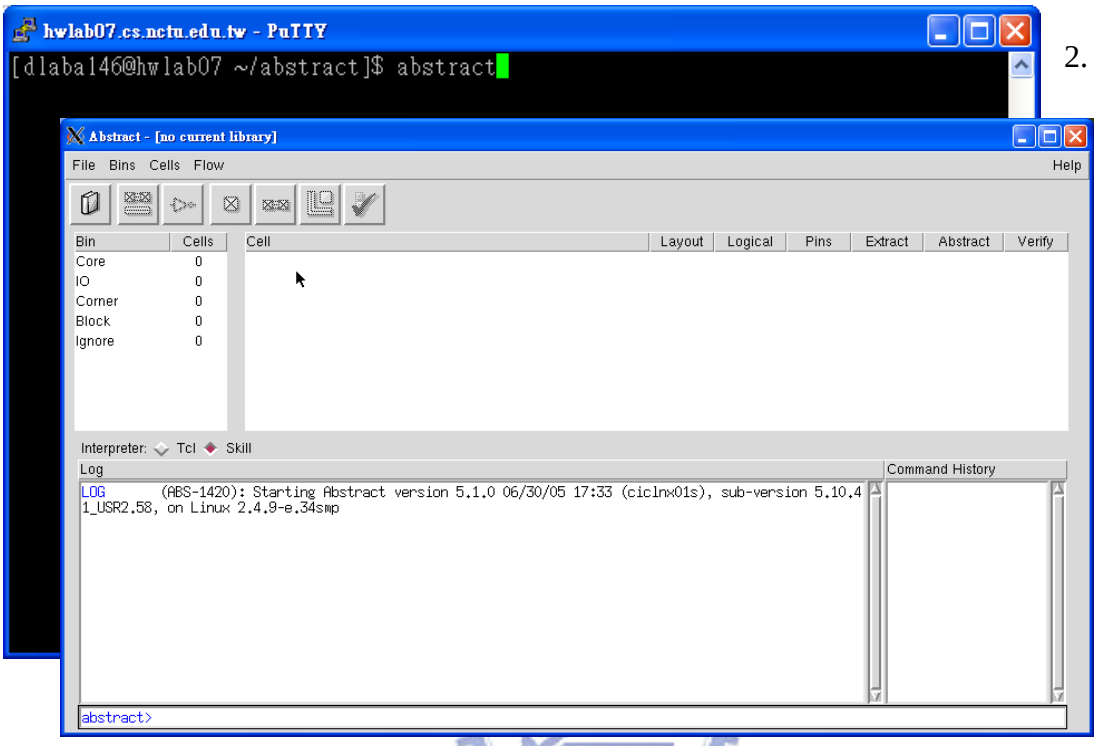


6. After finish your design layout. Export it to gds format.

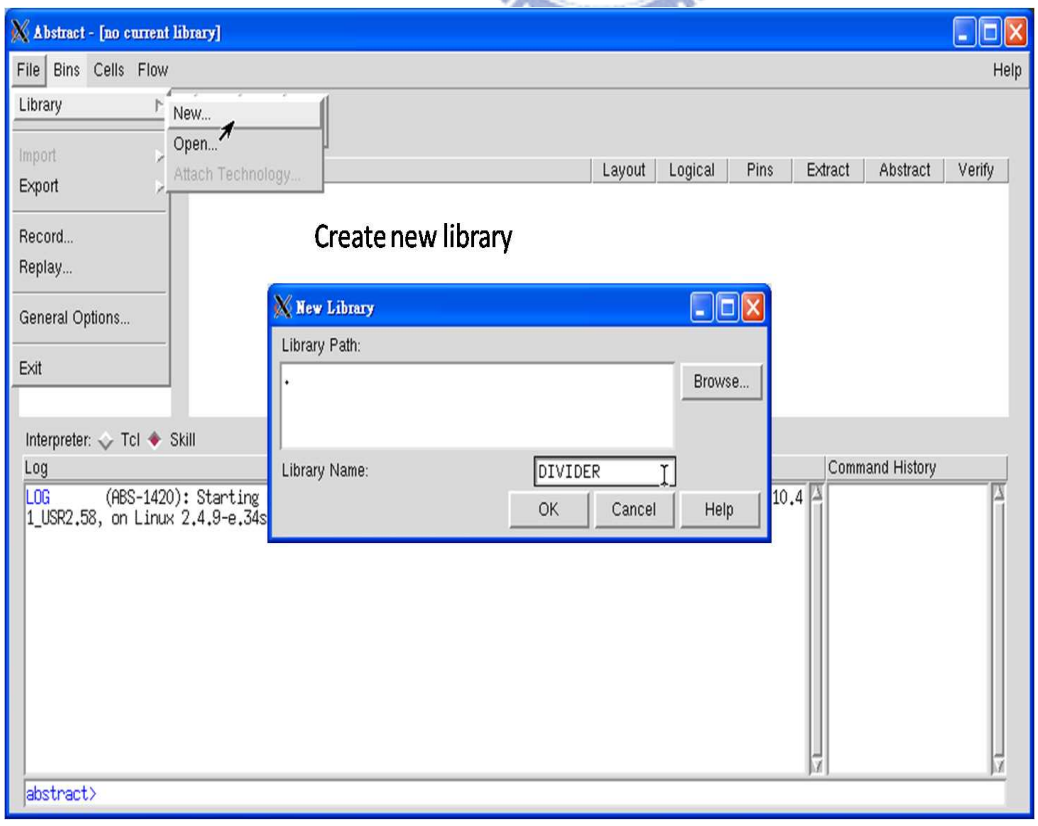


Appendix B - Abstract Tour

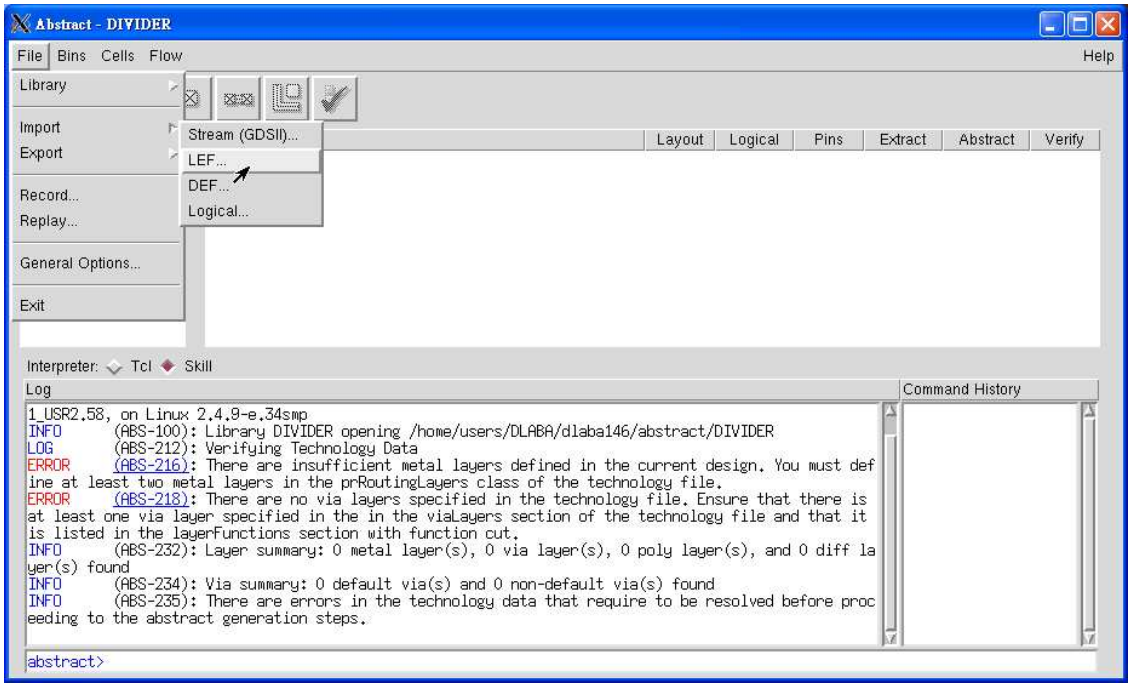
1. Type “abstract” in terminal to start abstract



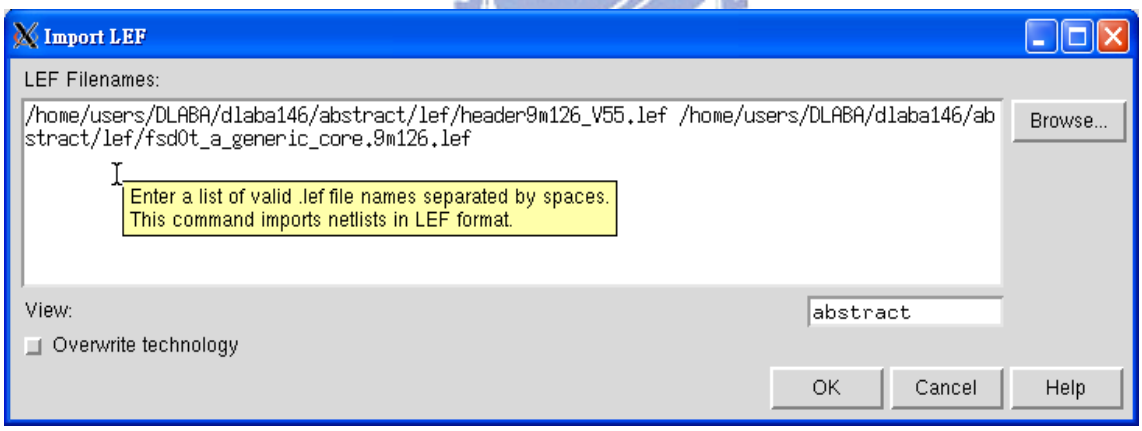
2. Create a new library



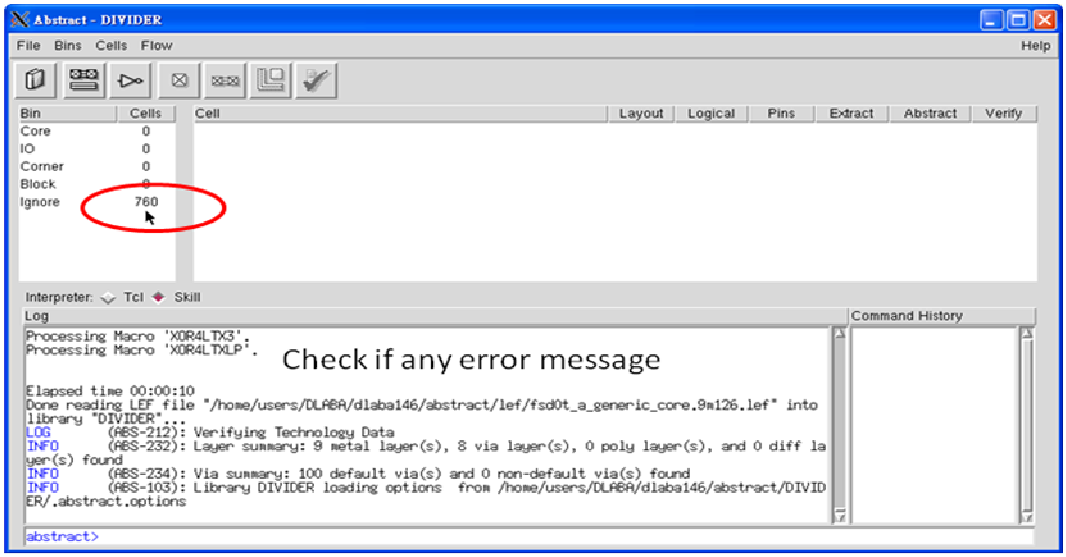
3. After create the new library, import LEF files from Cell Library.



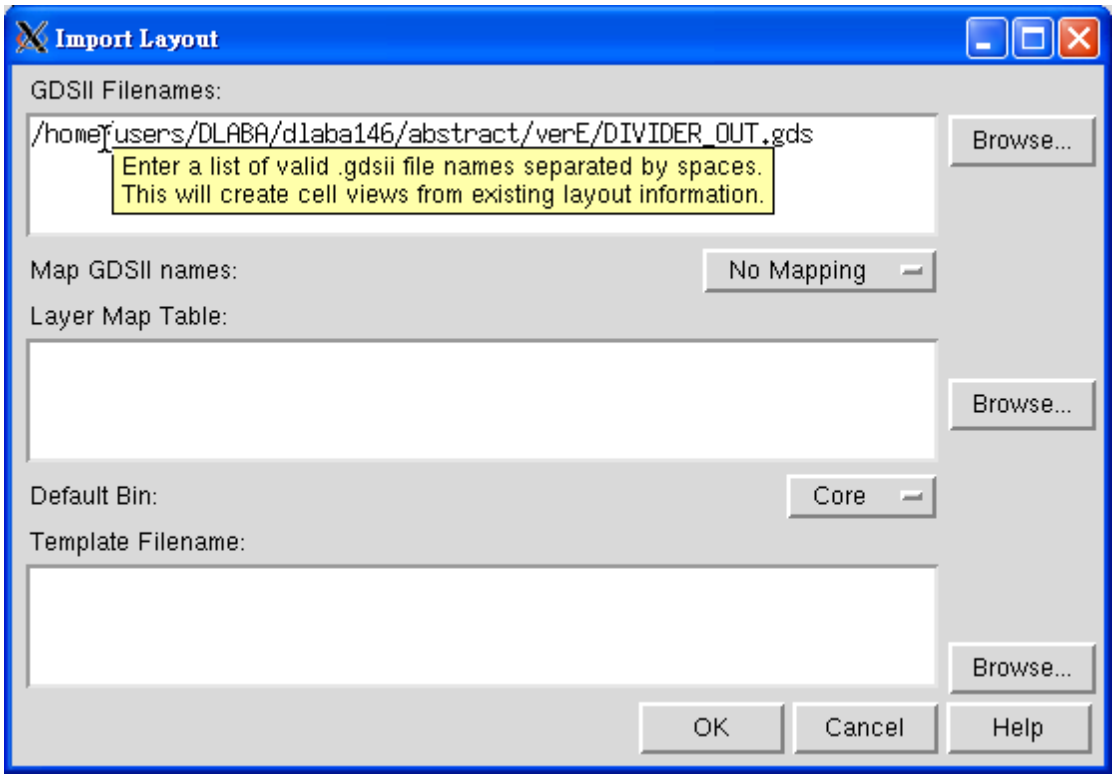
4. There are two LEF files have to import. Those two files are provided from Cell Library. In this example, one is “header9m126_V55.lef” the other is “fsd0t_a_genracic_core.9m126.lef”



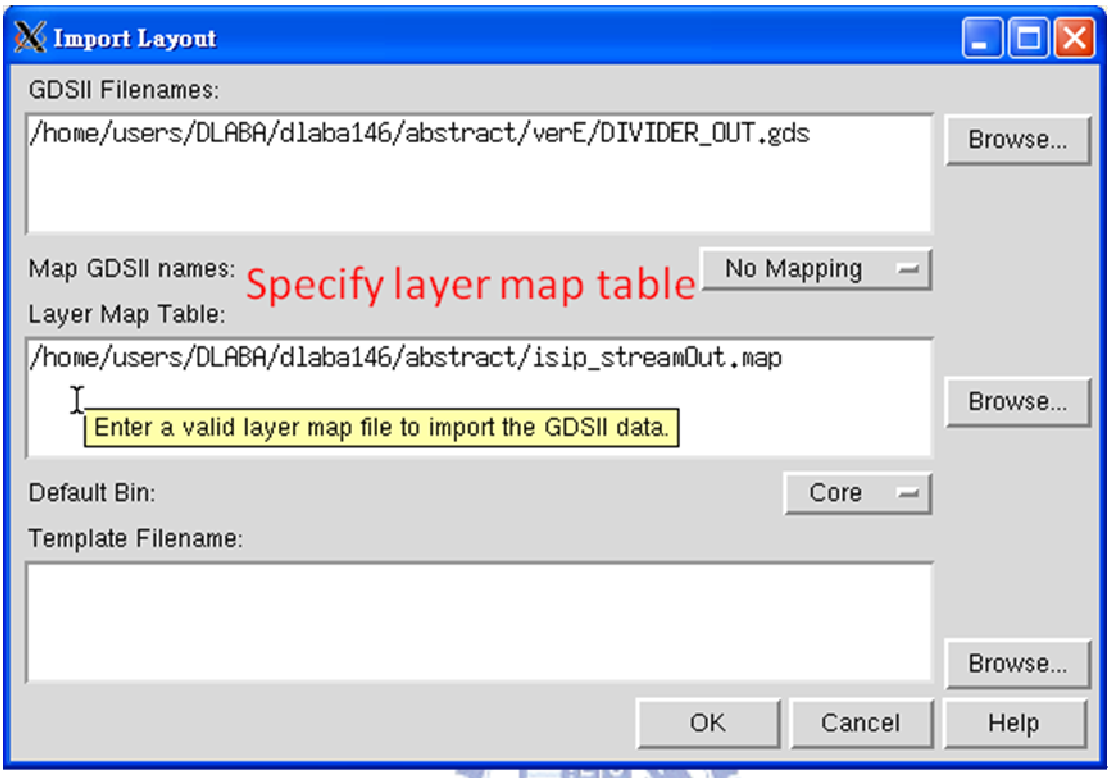
After import LEF files, there should be not any error message in log windows. And it means a user’s define library template has been created successfully.

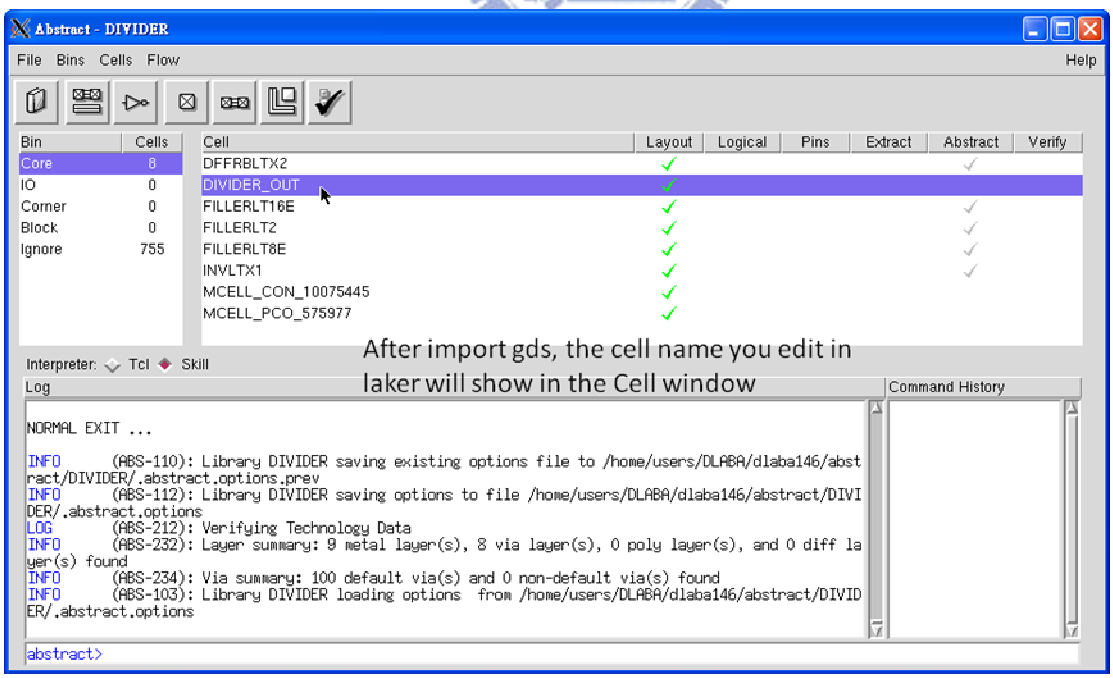


5. Import gds file that you layout and export from Laker or other layout tools.



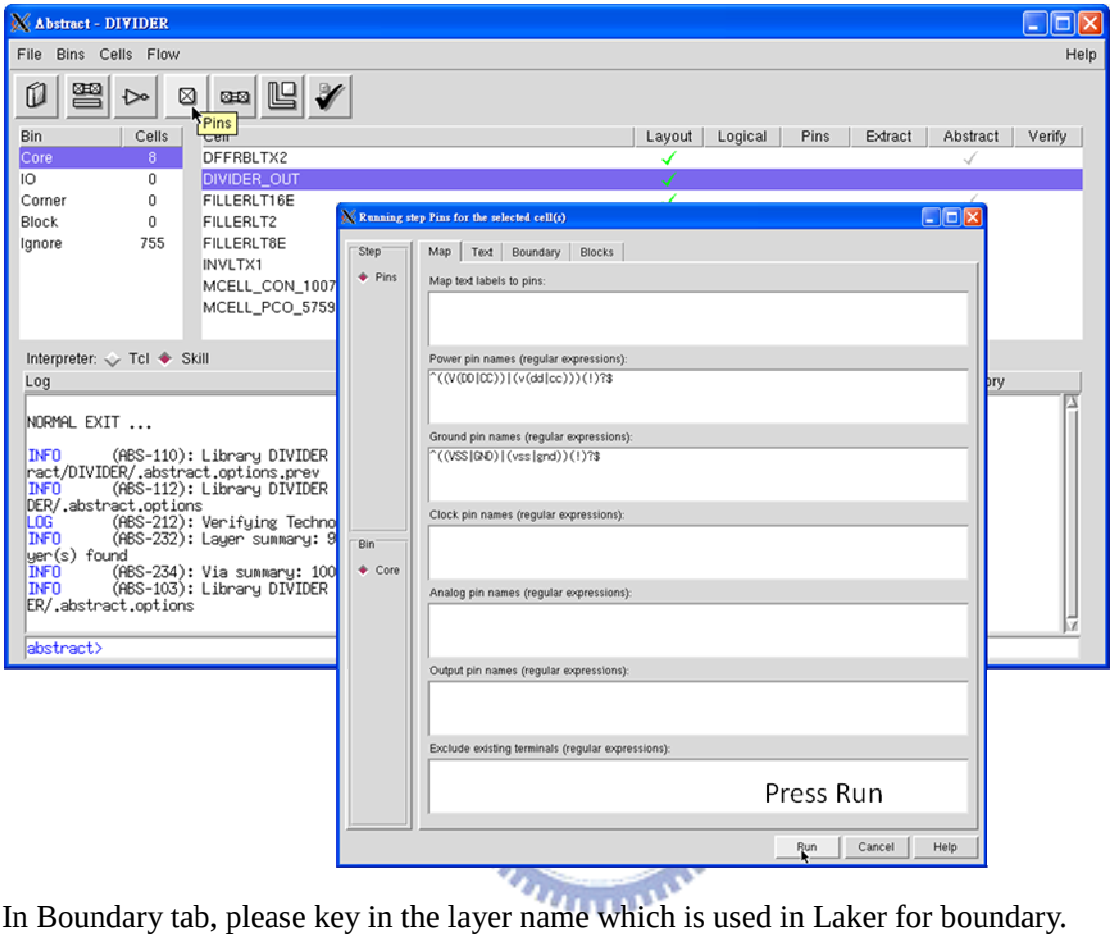
6. Specify layer map table



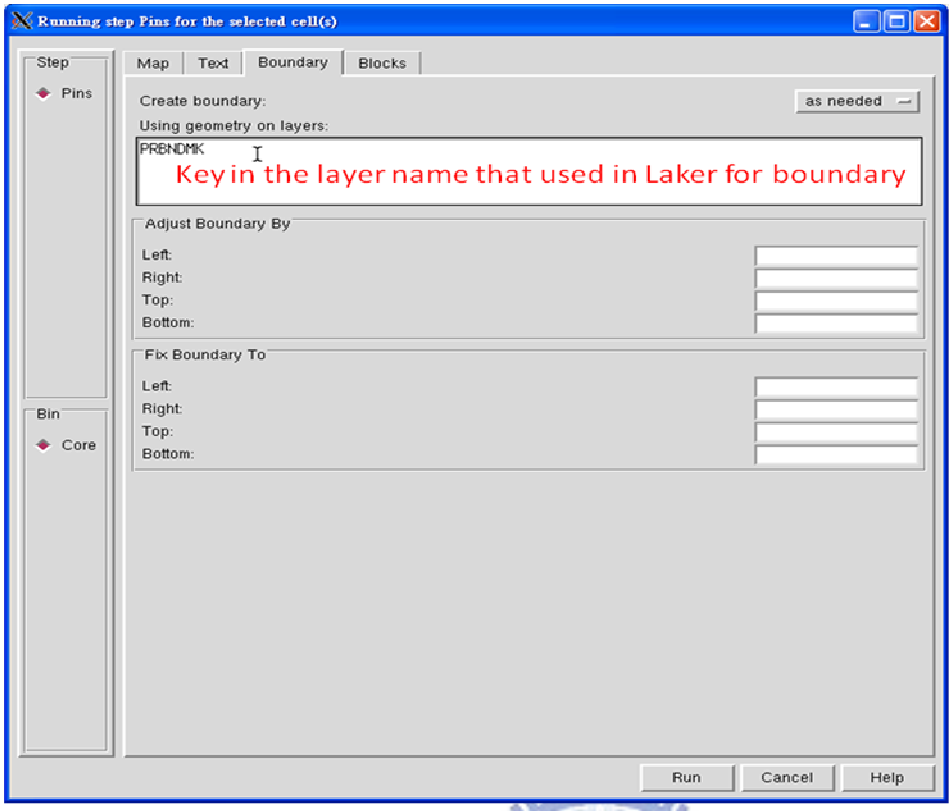


Next several steps are translate gds to LEF.

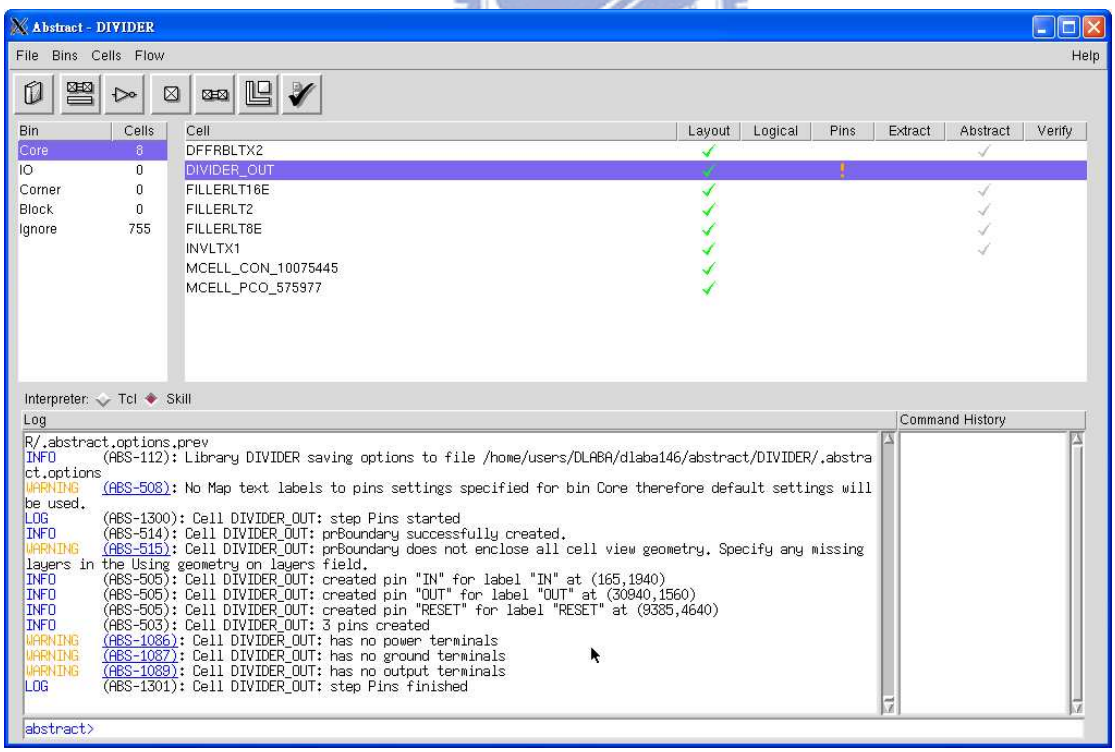
7. First, extract pin



In Boundary tab, please key in the layer name which is used in Laker for boundary.

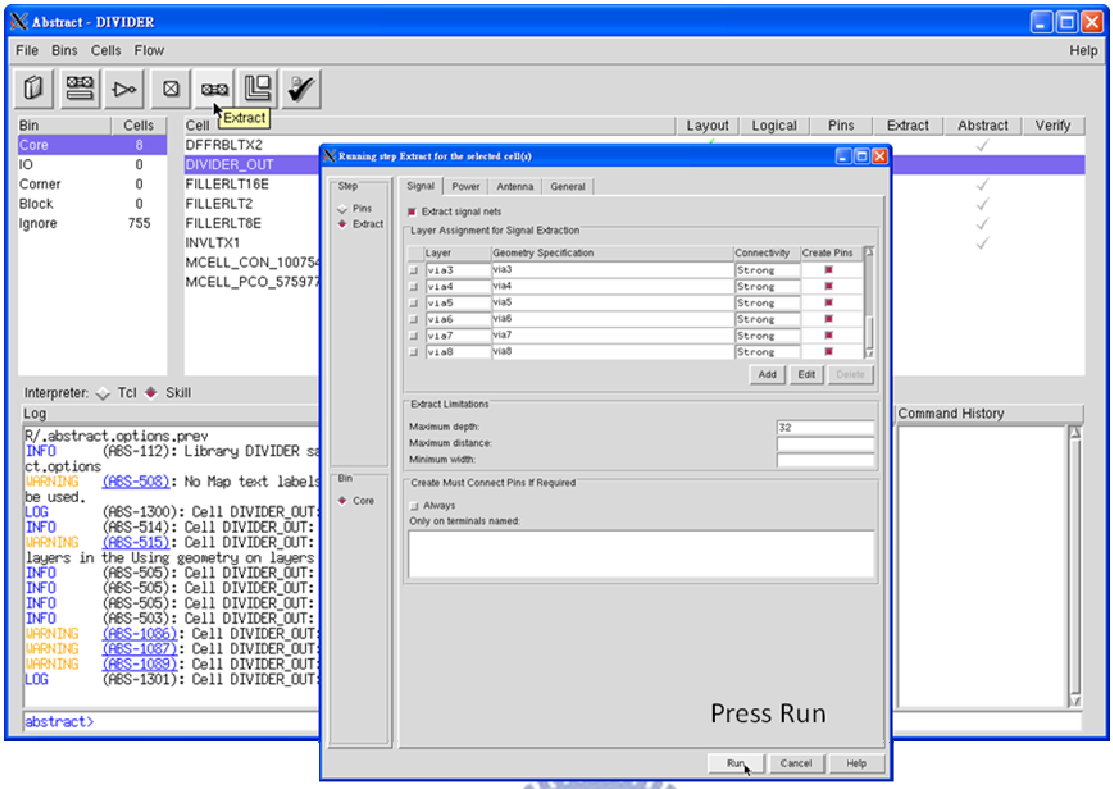


There are some warning messages, those can be ignored. One of the important thing is check out if all the pins been created. In this example is “IN, OUT and RESET”.



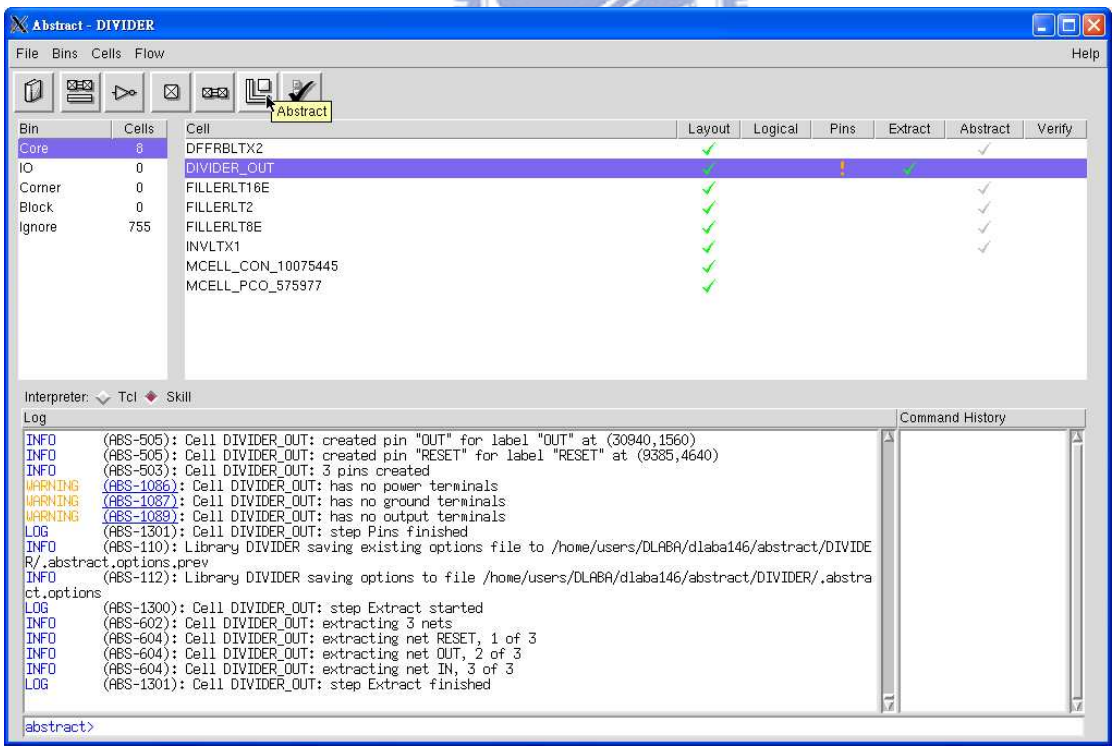
8. Second, Extract.

   Just press Run.

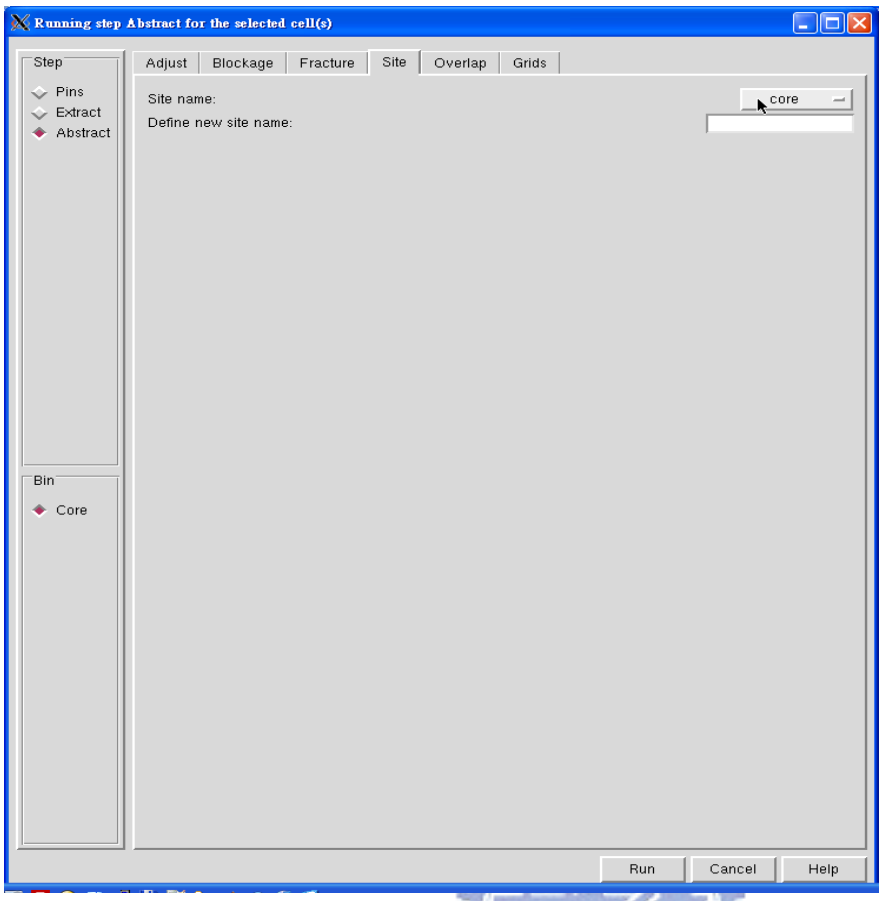


Normally, the Extract column in Cell window will show green tick.

9. Third step, Abstract

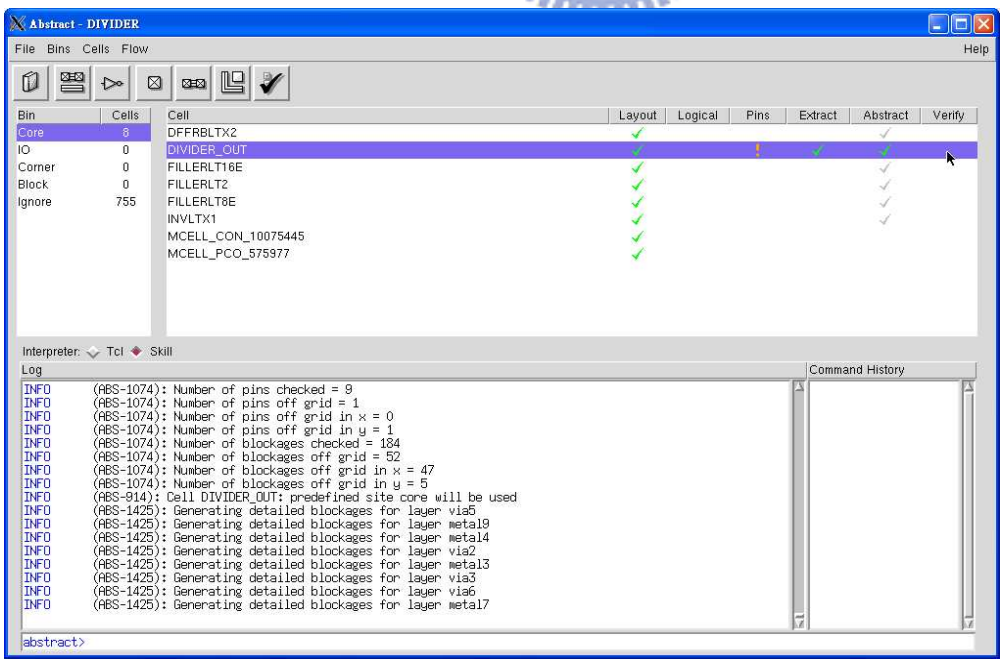


In this step, Site name must select to “core”.

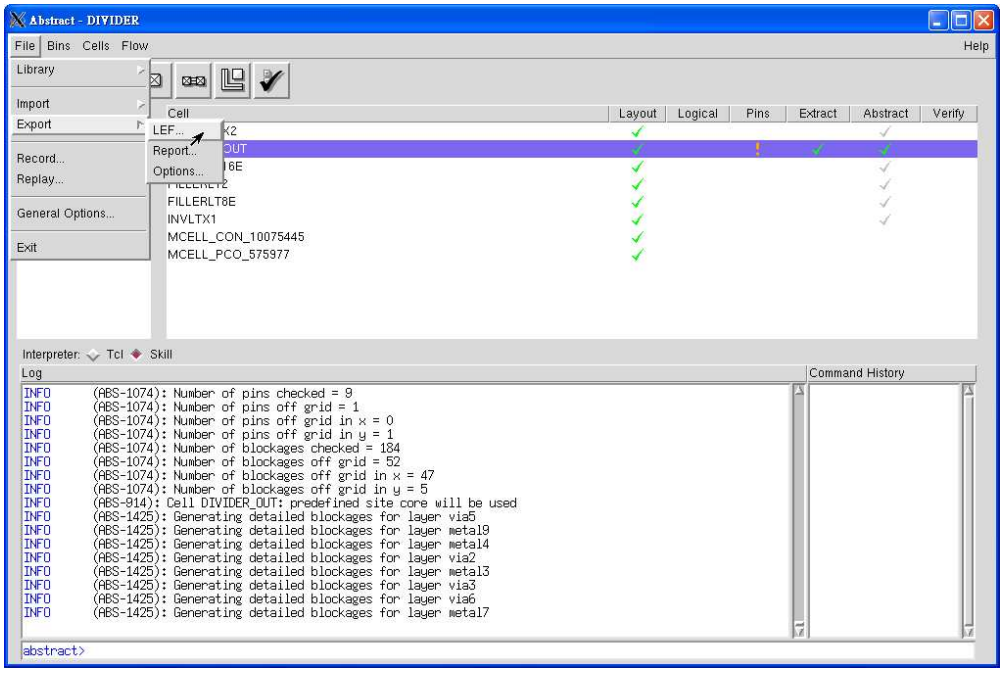


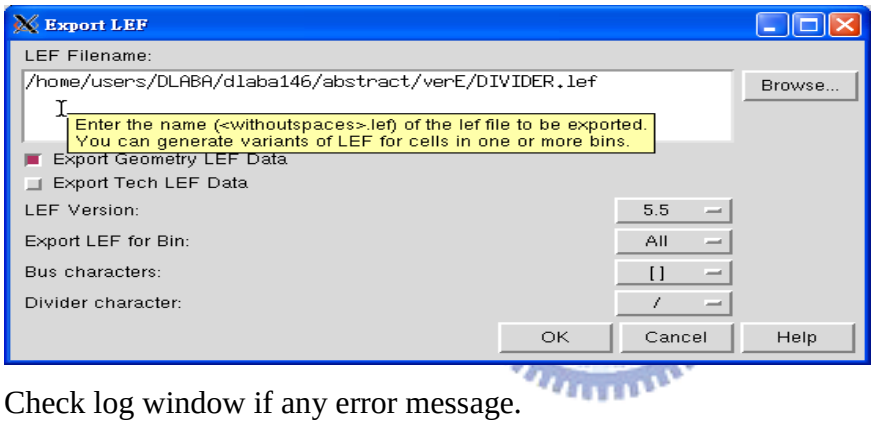
Finally, the column abstract also become green tick.

Normally, there is no any error message in log windows otherwise go back to check where is the problem.

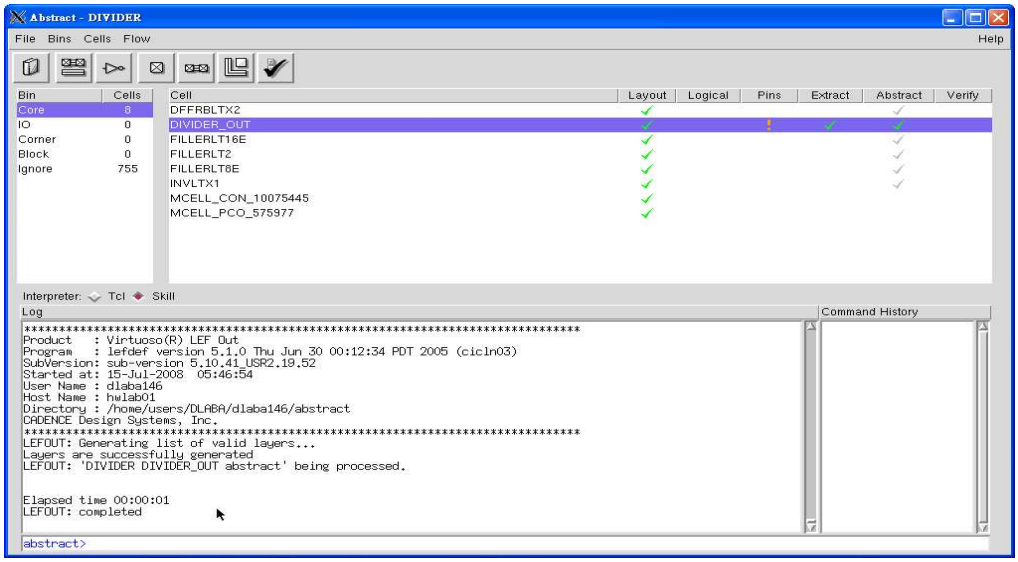


10. If those step have been done. Abstract can export LEF file we need.

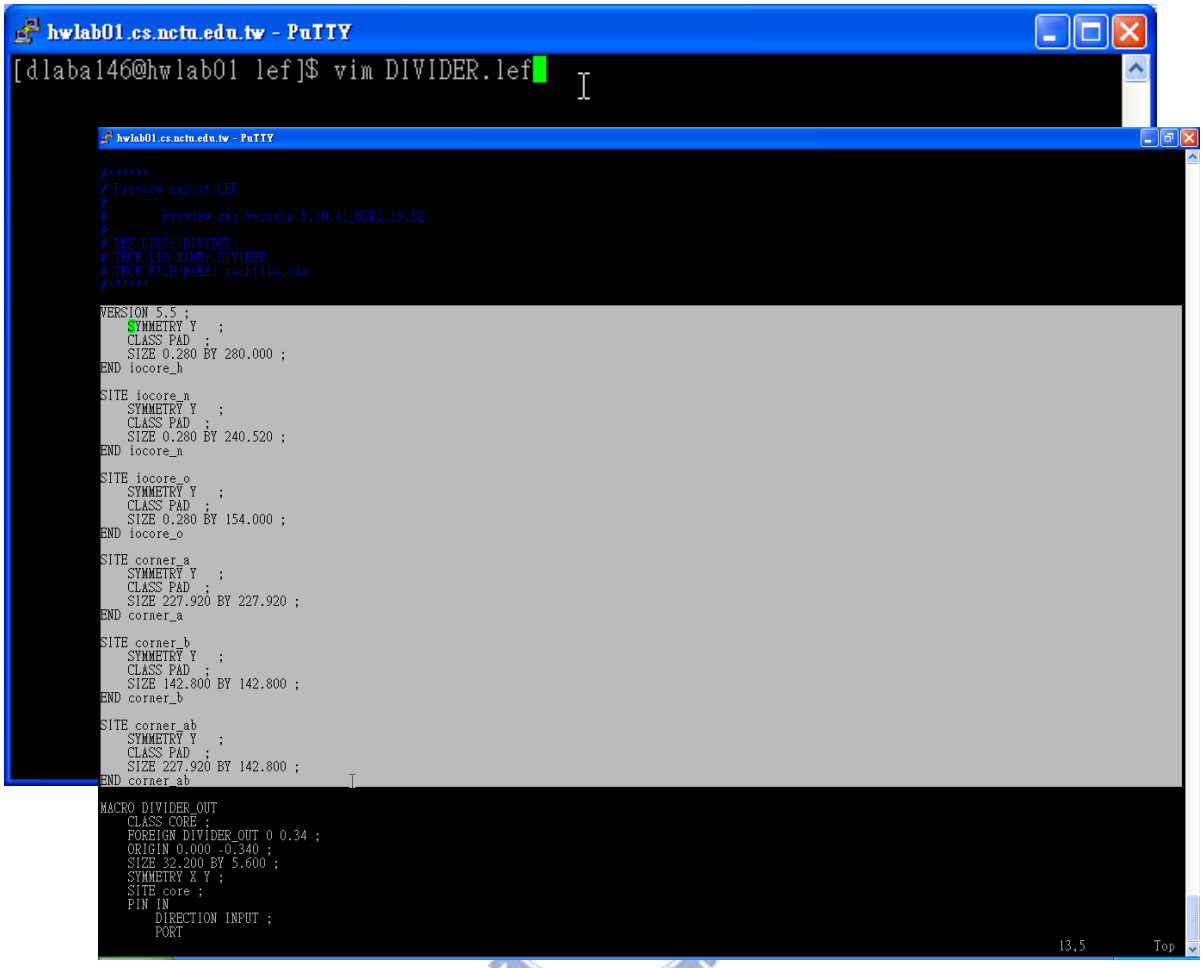




Check log window if any error message.



11. There are some step need manual. Open the lef file that just export. Delete all the text line before “”



Close and save the new LEF file.

These are all the steps that used abstract translate GDS file to LEF file.