國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

應用於高密度資料儲存與軟性電子之交錯電阻式記憶體

Cross-point Resistive Switching Memory for High-density Data Storage and Flexible Electronics

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中華民國 一〇一年 十 月

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摘　　要

利用電阻式記憶體 (RRAM)所組成的被動型陣列 (passive array) 雖具有最小單元面積 $4F^2$ 的優異微縮潛力，但位元間的讀取干擾 (read interference) 造成讀取窗口 (read margin) 對整個陣列上的非選取記憶單元 (unselected cells) 儲存狀態有相當程度的相依性，並嚴重地限制了記憶體陣列尺寸的設計，因此開發能適用於電阻式記憶體的選擇元件 (selection device) 是一個非常值得研究的議題。考慮到能與電阻式記憶體匹配的元件，以氧化物為基礎 (oxide-based) 的選擇元件結構簡單、製程微縮容易並可直接與電阻式記憶體形成垂直堆疊結構，是目前最為可行的候選。此論文探討了在室溫環境下，開發出分別適用單極切換 (unipolar RRAM) 與雙極切換 (bipolar RRAM) 的氧化物選擇元件並針對在交錯型陣列 (crossbar array) 所遇到的問題來做完整分析。

首先，我們利由 Ti/TiO_2 與 TiO_2/Pt 介面的蕭基能障特性，成功地在室溫環境下製造出有高整流特性的 Ti/TiO_2/Pt 二極體元件。在實驗的觀察中，由於 TiO_2 氧化物中的

氧離子隨外加偏壓會有不均勻分佈的移動，使得這些氧缺 (oxygen vacancy) 所造成的局部傳導路徑 (filament) 促使二極體元件擁有相當高的順向電流。接著，由於 $Ti/TiO_2/Pt$ 二極體優異的低溫整合能力，我們可以將二極體與 $Ni/HfO_2/Pt$ 記憶體元件整合至可撓式基板 (flexible substrate) 上進一步去驗證 1D1R 架構的單極電阻切換特性，其高整流開關比與穩定的切換特性可以實現至 512 Kb 大小的記憶體容量。

另一方面，我們也針對雙極切換的電阻式記憶體開發出適用的選擇器 (selector)。由於雙極的切換特性，雙極性選擇器需具有足夠高的雙向導通電流去達成組態切換的需求與高非線性程度 (nonlinearity) 去抑制讀取干擾。因此，我們藉由 Ni/TiO_2 介面的蕭基能障所控制的非線性電流-電壓特性製作出對稱結構的 $Ni/TiO_2/Ni$ 選擇器。在阻態切換特性方面，我們使用了 $Ni/TiO_2/Ni$ 選擇器與 $Ni/HfO_2/Pt$ 記憶體元件去驗證 1S1R 雙極切換能力。除了 1S1R 較穩定的雙極切換特性之外，藉著簡單的預測模型，我們也發現 1S1R 比 1D1R 俱有更優異的應用潛力。

最後，實驗的結果顯示，$Ni/HfO_2/Pt$ 記憶體元件應用到軟性基板下可以承受高度彎曲 (bending)、超過 10^6 次的操作容忍度 (endurance) 與快於 100 奈秒的操作 (SET/RESET) 速度。藉由等效電路的計算結果，我們開發出高導通電流密度 ($\sim10^5$ A/cm^2) 與高非線性程度 ($\sim10^3$) 的 $Ni/TiO_2/Ni$ 選擇器擁有應用到兆位元級記憶容量的潛力。另外，由於氧化物元件優異的低溫整合能力，我們也成功的將垂直整合結構 $Ni/TiO_2/Ni/HfO_2/Pt$ 驗證到 8 × 8 的軟性記憶體陣列上，並可以明確的判讀出陣列中記憶體元件的高低組態。我們相信此篇論文的研究成果可以提供未來應用在高效能軟性記憶體設計的重要研究方向。

Cross-point Resistive Switching Memory for High-density Data Storage and Flexible Electronics

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ABSTRACT

Cross-point RRAM with $4F^2$ cell size has attracted a great attraction because of its superior scalability. However, read interference between neighboring cells in passive arrays has become a serious issue, where the read margin depends strongly on the stored patterns of the unselected cells. This may significantly limit the maximum available array size. Therefore, it is in urgent need to design a suitable selection device for crossbar RRAM to improve read margin but without sacrificing high cell density. Considering the process compatibility, oxide-based selection devices is a promising candidate to reduce the sneak current because of its simple structure, excellent scalability and low-temperature processes allowing vertically stacking with RRAM. In this thesis, we introduced two selection devices

compatible with room-temperature process for unipolar RRAM and bipolar RRAM, respectively.

Firstly, we fabricated a room-temperature Ti/TiO_2/Pt oxide diode with an excellent rectifying characteristic by the asymmetric Schottky barriers at the Ti/TiO_2 and the TiO_2/Pt interfaces. The experimental results show that the current transport was governed by the localized oxygen-deficient TiO_2 filaments, which contributes the high forward current in the Ti/TiO_2/Pt oxide diode. Furthermore, a flexible one diode-one resistor (1D1R) memory cell, consisting of Ti/TiO_2/Pt diode with a large rectifying ratio and a stable unipolar resistive-switching (RS) Ni/HfO_2/Pt memory element, was fabricated using only room-temperature processes. Due to its superior rectification ratio of 1D1R cell, it can effectively realize a crossbar array as large as 512 Kb.

On the other hand, a nonlinear selector for bipolar RRAM in the crossbar array was fabricated using a simple Ni/TiO_2/Ni metal-insulator-metal (MIM) structure. The highly nonlinear current-voltage characteristics were realized by the Schottky barrier at Ni/TiO_2 interfaces. The series connection with a HfO_2 resistive memory shows a reproducible bipolar RS. Predicted by a simple analytical calculation, one selector-one resistor (1S1R) cell shows even more promising potential as compared with the 1D1R cell.

Finally, the flexible Ni/HfO_2/Pt memory element with superior properties, including excellent immunity to mechanical bending, reliable cycling and fast SET/RESET speed were demonstrated. Additionally, a flexible Ni/TiO_2/Ni selector with a high current density of 10^5 A/cm^2 and highly nonlinear *I-V* was capable of gigabit memory arrays implementation. We eventually realized a vertically stacked Ni/TiO_2/Ni/HfO_2/Pt 1S1R cell on a flexible 8 × 8 crossbar array, where the HRS/LRS states of the selected cell were successfully read out. We believe that our research provides a clear path for future high-performance flexible memory applications.

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Chapter 1

Introduction

1.1 Background

Metal-oxide semiconductor (MOS) transistor-based memories (such as Dynamic Random-Access Memory (DRAM) and NAND-flash memory) have played an important role for decades in the development of semiconductor industries. However, technologies scaling beyond 20 nm nodes are facing fundamental physical limits, and the increasing leakage power of DRAM has challenged the circuit and architecture concerns for future memory hierarchy designs [1-3]. One well-known limitation of NAND-flash is the time-consuming writing, which restricts its continuous scaling as a candidate for future memory technologies. Alternative memory technologies for factors, such as scalability, high-density, and writing speed, must be taken into consideration. Therefore, the best approach towards these goals is to use a two-terminal memory device with a stackable structure integrated into a crossbar geometry. Consequently, emerging memory technologies based on different concepts, including Phase Change RAM (PCRAM) [4], Spin Torque Transfer RAM (STT-RAM) [5], and Resistive Switching RAM (RRAM) [6], have been extensively explored in recent years, as shown in Fig. 1.1. Among these emerging memory technologies, the so-called RRAM memories, based on the electrically switchable resistance between at least two distinguishable states, are the most promising candidates. From the viewpoint of material choice, moreover, it is much easier to use CMOS process compatible materials. Therefore, only RRAM technologies are discussed in our study.

In addition to the considerations for emerging memories applied in “rigid electronics,”

the development of “soft electronics” has attracted progressively attention because they are lightweight, portable, inexpensive, and human-friendly interfaces [7-9]. Recently, many researchers have explored various flexible electronic devices, such as e-paper [10], flexible Radio-frequency identification (RFID) tags [11], flexible cell phones [12], and e-skins [7], as shown in Fig. 1.2. These works demonstrated the feasibility of their applications to specific components in electronics. Among which, flexible memories are required in each flexible system, showing the critical role that flexible memories play in flexible technologies. If technologies and processes used to fabricate inflexible memory devices could be adopted by flexible substrates, memory technologies could be potentially transferred into flexible substrates. Thus, it is worthwhile to explore inflexible technologies that may have the potential to be used in flexible substrates. Because of its room-temperature process, RRAM is suitable for all oxide-based devices, making it possible to be implemented in flexible electronic applications.

In this chapter, we review the development of currently established RRAM technologies in Section 1.2. Starting from basic device architectures to integrated crossbar arrays, various selection devices proposed to suppress the sneak current is reviewed. Then, the operation methods of “write” and “read” in crossbar arrays are included in Section 1.2.3. Finally, the motivation of this dissertation and thesis organization are described in Sections 1.3 and 1.4, respectively.

1.2 Development of Resistive-Switching RAM (RRAM)

Resistive-switching (RS) behaviors in MIM structures have been explored since 1962 [13]. Accompanying a large variety of high-κ materials progressively used in CMOS technologies, the further prosperous development of RRAM was triggered by Waser et al. in 2007 [6]. The RS effects were observed in various material systems under electrical stress

but only the effects, such as electrochemical, valence change, and thermochemical-related are classified in the RRAM group [14]. In this section, we start to describe the basic concepts of RRAM cell and its related structure built in crossbar arrays. Material systems and physical mechanisms of RS phenomena are not discussed in this dissertation but are reviewed in other studies in our group [15, 16].

1.2.1 Basic concepts of RRAM

As shown in Fig. 1.3(a), a RRAM element is formed at the junction between the top and bottom metal layers. Each RRAM element can be interconnected to form a typical crossbar array with an electrode pitch of 2F, where F is the feature size of a technology node. Thus, a mini-RRAM unit cell with an ultrahigh density of $4F^2$ can be achieved. In this capacitor-like MIM structure, an insulating or switching layer (I) is sandwiched between two metal electrodes (M). By electrically stimulating the devices, RS properties were observed in various binary oxides, such as NiO [17], TiO_2 [18], Ta_2O_5 [19], and HfO_2 [20]. Among which, HfO_2 is particularly favorable material in present CMOS technologies.

Typically, an initial electroforming process accompanied by an appropriate compliance current must be introduced to activate the virgin RRAM device. Afterward, by applying either a voltage or a current to the RRAM device, RS processes from the high-resistance state (HRS) to low-resistance state (LRS) and from LRS to HRS are called SET and RESET, respectively, as shown in Fig. 1.3(b). These distinctive reproducible states (HRS/LRS) are able to retain their resistance levels for a quite long period, allowing information to be retrieved when a small read voltage (V_{read}) is applied. In principle, RS in RRAM can be classified into two main switching schemes: unipolar RS and bipolar RS, which are usually identified by the polarity of voltage or current during operation. In unipolar switching, both SET and RESET operations occur on the same polarity, whereas in bipolar switching, it requires two polarities to finish one SET/RESET cycle.

1.2.2 Development of selection devices for crossbar RRAM

In the simplest case, RRAM cells are typically organized in a passive crossbar array. However, RRAM cells in passive crossbar arrays are inherently suffered from undesired sneak currents entering through the surrounding cells during the reading process. As shown in Fig. 1.4(a), a selected HRS cell surrounded by three neighboring LRS cells can easily pass sneak currents through the neighboring LRS cells. Consequently, the read interference may significantly deteriorate the read margin ($\Delta V/V_{pu}$) and limit the maximum allowed size in a crossbar array [21, 22]. It was reported that an inborn nonlinear *I*-*V* of LRS in a RS element can yield better results in an increased voltage swing (ΔV) [21-23]. However, this approach limits the freedom of the design criteria of the RS element, and its low nonlinearity is insufficient to build M-bit or G-bit array sizes [22].

Therefore, finding additional selection devices with a specific degree of nonlinearity added at each node, where current flow is allowed only for the selected cell and suppressed for the unselected cells, is inevitably required (Fig. 1.4(c)). A selection device is required to have a high-current density, as well as important to the selectivity. The turn-on current density must be sufficiently high to meet the minimum current requirement for a successful switching at a given technology node without causing itself breakdown. For example, at the technology node of 100 nm, the current density of 10^5 A/cm^2 provided by a selection device is needed for an I_{reset} of 10 μA, as shown in Fig. 1.5 [24]. Depending on the switching scheme of RRAM elements, several selection devices have been proposed, and are being considered promising solutions. The four possible configurations, shown in Table 1, One Transistor-One Resistor **(**1T1R or 1BJT1R), One Diode-One Resistor **(**1D1R), Complementary Resistive Switching (CRS), and One Selector-One Resistor (1S1R) in the operation scheme, and process complexity and feasibility are discussed in this subsection.

(a) One Transistor - One Resistor (1T1R)

A 1T1R cell organized by connecting a transistor and a resistor in an active matrix is shown in Fig. 1.6(a). Because of the transistor's superior switch ratio, the 1T1R architecture can significantly reduce crosstalk and interference signals in crossbar arrays. A 1T1R was also introduced to control the filament size by preventing the overshoot current during the forming process [24]. This work shows that the controlled forming current allows a relatively large HRS and a subsequent reset current (I_{RESET}) below 100 μA (Fig. 1.6(b)), which indicates a scalability of I_{RESET} through an integrated transistor in the series with a RRAM. In addition, it has been reported that the transient current through the parasitic capacitance of the MIM structure can be further reduced in the integrated 1T1R when the forming or the set process occurs [25]. However, 1T1R and 1BJT1R structures are not suitable for 3D stacked structures because of their high-temperature processes and additional area for transistor contact.

(b) One Diode - One Resistor (1D1R)

In the unipolar RS scheme, the sneak current can be resolved through a rectifying diode as a selection device. This stacked 1D1R structure capable of $4F^2$ crossbar array, without affecting storage density (Fig. 1.7(a)), is one of the most attractive candidates [26-29]. Considering various materials used in diodes, the types of diodes employed in the 1D1R cell mainly include Si-based diodes [27, 30] and oxide-based diodes [31-34]. However, epitaxial Si-based p-n diodes are not suitable for the stacking structure because of their high-temperature process, and they are problematic in epitaxy high-quality silicon on oxide layers.

Oxide-based diodes are powerful candidates to address these issues. Two oxide layers, one n-type oxide and one p-type oxide, were used to form a rectifying p-n oxide diode, as shown in Fig. 1.7(b) [31-33]. However, the proposed p-n oxide diodes with a high turn-on

voltage, too-high ideality factor, and insufficient Forward/Reverse (F/R) ratio still remain concerns; additionally, two thin oxide layers with specific compositions increase challenges in manufacturability. Another way to approach the rectifying behavior is to modulate the Schottky barrier at the metal/oxide interfaces during fabrication [18, 35, 36**],** or to choose applicable top and bottom metal electrodes in MIM structures [37, 38]. These Schottky-type diodes, fabricated in a relatively simple process, are capable of achieving a local forward current density of approximate 10^4 A/cm^2 (will discuss in Chapter 2) and a high F/R ratio at a relatively-low voltage, which are crucial merits of this type of diode. When a diode was integrated with a RS element, the well-behaved switching and the significant rectification could be achieved, as shown in Fig. 1.7(c).

In addition, the current density of the forward-bias diodes is an important factor that may limit the scaling, as shown in Fig. 1.5. To further improve the current density for a compatible I_{RESET} is necessary to allow a reliable unipolar RS.

(c) Complementary Resistive Switching (CRS)

CRS, consisting of two antiserially bipolar RS elements, has been proposed as a possible solution for bipolar RRAM to suppress the sneak current [39]. As shown in Fig. 1.8(a), elements A and B are merged to form one CRS cell, where a superimposed *I*–*V* characteristic can be directly obtained. In contrast to the concept of passive crossbar arrays, the overall resistance of a CRS at $V_{read}/2$, regardless of the "1" or "0" stored, is dominated by the large HRS on either element A or element B. Basically, the CRS acts by essentially the same principle as a CMOS inverter, in which one of the transistors is always OFF. To read the resistance state of CRS, V_{read} between $V_{th,1}$ and $V_{th,2,}$ or $V_{th,3}$ and $V_{th,4,}$ was chosen to read the selected cell. At this point, if an ON-state exists in the CRS, a significant current will be detected. Several studies have experimentally demonstrated the feasibility of CRS cell [40, 41]. In Fig. 1.8(b), as expected, the stacked Pt/HfO_2/ZrO_2/BE/ZrO_2/HfO_2/Pt displays a CRS

I-V curve in accordance with the predicted operation scheme. But, a critical trade-off in CRS between the read voltage window and the write voltage window must be carefully designed [42].

Furthermore, the inherently destructive reading of CRS imposes severe penalties on the design complexity, writing speed, and power consumption. In addition, a stable bipolar switching for both RS elements is also a concern to obtain reliable read/write endurances.

(d) One Selector - One Resistor (1S1R)

By considering an additional selection device, the commonly used rectifying diodes are not suitable for a bipolar RRAM because it needs two polarities to complete one SET/RESET cycle. In other words, the selection device must have a bidirectional and nonlinear *I-V* to allow the bipolar switching. Fig. 1.9(a) shows the *I-V* characteristics of a bipolar RRAM with and without a bipolar selector. When using the one bit-line pull-up read scheme (One-BLPU) to evaluate the read process, as shown, the sneak current at $V_{read}/2$ of the unselected cells was apparently eliminated, indicating a possible solution to reduce the sneak current. A so-called Zener diode was applied to this configuration. As in a regular diode, it allows current to travel in both forward and reverse directions if the voltage was larger than the reverse Zener voltage. However, like the traditional Si-based diode, the complex and high-temperature process makes Zener diode unsuitable for the stacking memory process. In addition, it has difficulty obtaining a reasonable Zener voltage to match the low-power requirement of a bipolar RRAM. Recently, a voltage-controlled varistor based on the low-temperature oxide materials, with bidirectional and symmetrical *I-V* characteristics, has been proposed [43, 44]. Cell structures composed of one nonlinear bipolar selector and one bipolar RS element (1S1R) can best use the stable bipolar RS properties. In contrast to modulating the inborn nonlinearity of RRAM, the nonlinearity of 1S1R at a small voltage can be separately controlled by the selector. In Fig. 1.9(b), the sneak

current of LRS at $V_{read}/2$ can be significantly blocked by the proposed 1S1R cell as compared to a selector-less bipolar RRAM. So far, the endurance of 1S1R cell has not yet been verified because the selector may suffer dielectric breakdown at high voltage. Additionally, the reported bipolar selector had limited nonlinearity sufficient only for a small 8 × 8 array [43]. Based on above reasons, the improved 1S1R characteristics and the flexible 1S1R array will be discussed in Chapters 4 and 5,

1.2.3 Operation methods of crossbar RRAM

The performance of write to and read from passive crossbar arrays can be improved by connecting a suitable selection device, such as diodes or bipolar selectors, but still challenged. For write to crossbar arrays, a selection device must be able to write the selected cell without inferring the unselected cells. During a read operation, on the other hand, a logical “0” must be distinguishable from a logical “1” on the selected cell and vice versa. Therefore, both read and write operations must minimize the disturbance of unselected cells, and maximize power efficiency simultaneously.

(a) “Write” operation

When a memory cell is selected to perform a write operation, the other unselected cells connected to the unselected WLs/BLs are simultaneously subjected to a certain part of bias voltage. Ideally, a desired write operation should have high bias voltage to the selected cell and avoid disturbing the unselected cells. To bias the unselected WLs/BLs, there are two famous biased schemes, which are the $V_{dd}/2$ scheme, where the unselected cells are biased to voltages of either $V/2$ or 0; and the $V_{dd}/3$ scheme, where all the unselected cells are biased to voltages of either $V/3$ or $-V/3$ [45].

In the write operation of the $V_{dd}/2$ scheme, a voltage (V) is applied to the selected WL, while the selected BL is subjected to ground. For all the other unselected WLs/BLs, a

half-voltage ($V/2$) is applied as schematically shown in Fig. 1.10(a). Consequently, the selected cell is under a forward bias of V and the other unselected cells are biased to either $V/2$ or 0. On the other hand, in the $V_{dd}/3$ scheme shown in Fig. 1.10(b), the selected cell is biased to a voltage drop (V) as in the case of $V_{dd}/2$ scheme. In contrast to the $V_{dd}/2$ scheme, the unselected WLs and BLs are subjected to bias voltages of one-third of V ($V/3$) and two-thirds of V ($2V/3$), respectively. In this scheme, the selected cell is under a forward bias of V and the other cells on the unselected WLs/BLs are under voltages of $V/3$ or $-V/3$, implying that the disturb voltage is less-severe as compared to the $V_{dd}/2$ scheme. Only one-third of V_{SET} ($V_{SET}/3$) can drop on the unselected cells, which has less probability of causing erroneous RESET if a voltage V_{SET} is applied to the selected cell. Therefore, the stability of diodes under reverse bias is also a significant concern to avoid $-V_{SET}/3$ not causing the breakdown.

(b) "Read" Operation

The read operation is of particular concern in RRAM because the read process depends strongly on the stored pattern in the crossbar array, which may restrain the maximum array size. To analyze this process, a simplified n × m crossbar array is schematically depicted in Fig. 1. 11(a). The read operation is performed by applying a pull-up voltage (V_{pu}) to the selected BL and the selected WL is grounded. A convenient way of designing an output voltage swing (ΔV_{out}) with respect to the stored pattern is by introducing a pull-up resistor (R_{pu}) parallely connected to the sensing amplifier (SA) on each BL. The R_{pu} value was particularly designed to achieve the maximum ΔV_{out}. In general, a sensing criterion of at least 10% read margin ($\Delta V_{out}/V_{pu}$) was chosen to determine the maximum available array size [39].

In the worst-case scenario, the read margin was measured at the condition where the selected cell is on the corner of the array. In this pattern, one can divide the unselected cells

into three groups: Region 1 (cells on the selected WL), Region 2 (cells on the unselected WL and BL), and Region 3 (cells on the selected BL), as shown in Fig. 1.11(b). The line resistances of interconnects were ignored under this assumption. To read information from the crossbar array, there are generally three ways to bias the unselected WLs/BLs: by V_{dd}, grounding, or floating, which contributes nine possible configurations, as shown in Fig. 1.12 [46]. The voltage configurations in the crossbar array play a crucial role in sensing margin, disturbance, and power efficiency. Specifically, V_{out} is significantly influenced by the random resistance patterns as well the configurations, giving the indistinguishable sensing margin. In addition to the sensing margin, although the parallel leakage paths (shown by dashed lines) do not affect the voltage swing, an obvious power waste is raised.

The simplest read operation is configuration 1, the so-called One-BLPU. In this configuration, only the selected WL/BL is biased, and all the unselected WLs/BLs are left floating. When multiple or all bit lines are biased, they are referred to partial or all bit-line pull-up schemes (All-BLPU). To examine the performance of selection devices applied in crossbar arrays, it is much easier to choose the simplest read configuration (configuration 1) for our study.

1.3 Motivation

Flexible electronics have attracted much attention because of their advantages of simplicity, foldability and low manufacturing costs over conventional Si-based technologies [9, 11]. One critical concern of flexible electronics is to implement inflexible nonvolatile memories into flexible nonvolatile memories. Crossbar RRAM has been considered to be best solution in flexible memories. However, the reported flexible memories, consisting of only a few memory elements in the passive crossbar array, are not enough to provide a breakthrough evidence for flexible memory applications [47-49]. Furthermore, it is an

important project not only to further improve the switching reliability of RRAM cells, but also to find a suitable selection device to suppress the sneak current. Although traditional Si-based transistors have been the best solutions for DRAM and NAND-flash arrays, a high-temperature fabrication process and a cell size of at least $6F^2$ confine their continuous utilization in the crossbar RRAM [31]. In addition, CRS suffers from the issue of destructive read, which also increases the complexity of circuit design. Hence, 1D1R and 1S1R architectures appear to be the leading contenders for crossbar RRAM applications. Based on the present RRAM technologies, various oxide-based diodes have been explored in unipolar 1D1R architectures, but low rectification ratios and insufficient current densities are unable to achieve a reliable switching.

This dissertation employs TiO_2-based selection devices on flexible substrates by simple and room-temperature processes. To prove a fully oxide-based functional flexible memory, and prevent an undesired sneak current, each memory cell was integrated with a selection component. Based on the switching polarities, a unipolar Ti/TiO_2/Pt diode with a unipolar RS element and a bipolar Ni/TiO_2/Ni selector with a bipolar RS element were fabricated to construct a 1D1R and a 1S1R architectures, respectively. Endurance characteristics of 1D1R unipolar and 1S1R bipolar switching were also investigated. The top and bottom metal lines of 1S1R cells were further interconnected to construct an 8×8 crossbar array on a flexible substrate to examine the rad margin.

The goal of this study is to find low-temperature process available selection devices and demonstrate their roles in suppressing sneak currents, especially for their implementations on plastic substrates. These results can assist designers in writing new guidelines for realizing a fully-oxidized crossbar RRAM for high-performance flexible memories.

1.4 Thesis Organization

In this thesis, a TiO_2-based material through a simple process to construct flexible selection devices is proposed. The well-behaved Ti/TiO_2/Pt diode shows superior 1D1R switching characteristics by externally connecting a HfO_2-based memory element. Nonlinear Ni/TiO_2/Ni bipolar selectors were investigated using the stable bipolar 1S1R switching. This study also highlights the scaling potentials of 1D1R and 1S1R in future RRAM technology from the viewpoint of nonlinearity using a One-BLPU read scheme. Finally, an 8×8 1S1R array on flexible substrates was successfully realized. This dissertation contains four main concepts, which are organized into six chapters, as follows:

In Chapter 1, the development of currently established RRAM technologies are reviewed, starting from the device cell to the integrated crossbar array. Various selection devices based on the switching polarities to suppress the sneak current are discussed. The operation methods of crossbar RRAM are also described.

In Chapter 2, the stable rectifying and resistive-switching properties of a Ti/TiO_2/Pt MIM structure are investigated. Oxygen migration and localized conductive filaments play important roles in the resistive switching of RRAM and the rectification of oxide diodes. After forming at higher voltages, significantly stronger filaments destroying the interface Schottky barrier denotes reproducible resistive switching. Moreover, the current density of TiO_2 MIM diodes at -3 V more than 10^4 A/cm^2 can be achieved, showing satisfactory requirements in TiO_2 MIM diodes for future 1D1R RRAM applications.

In Chapter 3, a rectifying Ti/TiO_2/Pt oxide diode and a unipolar RS Ni/HfO_2/Pt memory element were fabricated on a flexible PI substrate with excellent characteristics using only room-temperature processes. No significant device degradations are found under the bending states. Additionally, the impact of I_{RESET} on the programming margin of unipolar RS has been discussed. The heterogeneous TiO_2-HfO_2 1D1R cell not only shows more sreliable unipolar switching compared to the monolithic TiO_2 1D1R cell but also effectively suppresses the sneak current. The maximum allowed array size with an at least 10% read margin was

predicted to be able to build 512 Kb memory size based on a simple equivalent circuit model.

In Chapter 4, a Ni/TiO_2/Ni MIM with highly nonlinear *I*-*V* characteristics was used as the bipolar selector for high-density 1S1R crossbar arrays. The nonlinear *I*-*V* is attributed to the Schottky barriers at the Ni/TiO_2 interfaces. When the selector element was further connected with the HfO_2 RS element, the combined 1S1R cell exhibits a robust and reliable bipolar switching, and can effectively suppress the sneak current. In addition, 1D1R and 1S1R crossbar arrays are compared in this chapter. These results demonstrate the promising potential of the 1S1R crossbar array for future high-density memory and reconfigurable logic circuit applications.

Chapter 5 shows a high-performance 8 × 8 1S1R crossbar array on plastic substrates realized by a simple and low-temperature fabrication process. The flexible Ni/TiO_2/Ni and Ni/HfO_2/Pt elements also had excellent mechanical stability upon harsh bending. Furthermore, the vertically stacked 8 × 8 1S1R array with superior read margin and immunity to disturb has been demonstrated, showing the potential application of future extremely low-cost flexible nonvolatile memories.

Finally, Chapter 6 states the conclusion as well as the recommendation for further research is addressed in this chapter.

Table 1.1 Comparison of various unit cell structures for RRAM.

Cell Structure	Cell Size	Selection Device	Destructive Read	Process Temp
1R	$4F^2$	No	No	Low
1T1R	$> 8F^2$	Yes	No	High
1BJT1R	$4F^2$	Yes	No	High
CRS	$4F^2$	Yes	Yes	Low
1D1R	$4F^2$	Yes	No	Low
1S1R	$4F^2$	Yes	No	Low

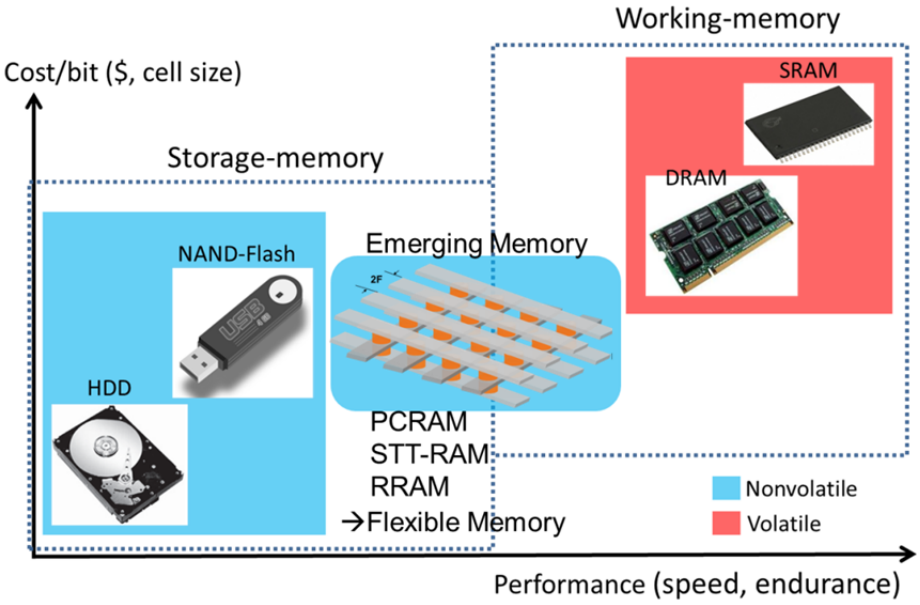

Fig. 1.1 Emerging memories based on the cross-point structure for future low-cost and high-performance memory applications.

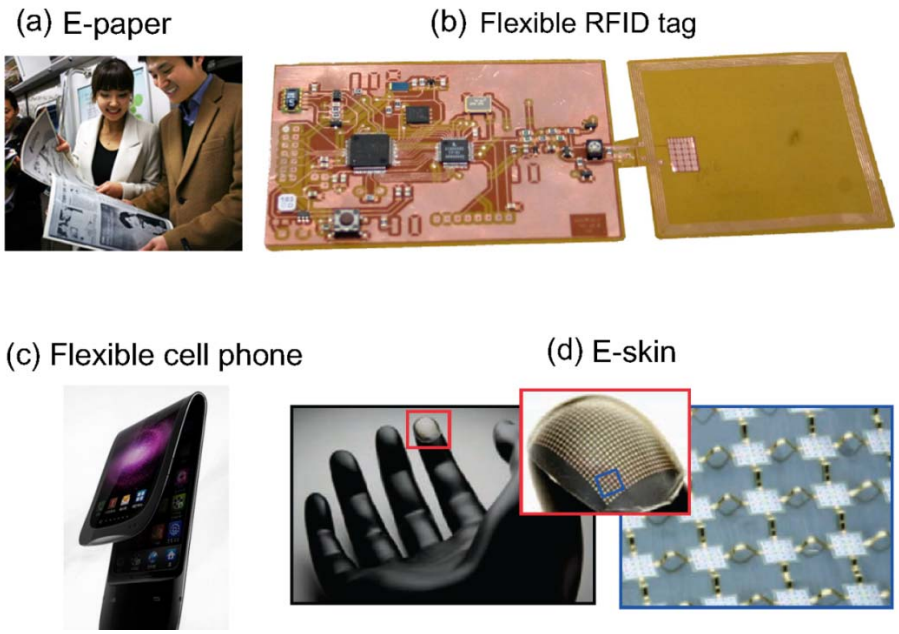

Fig. 1.2 Examples of flexible electronics: (a) prototype of the flexible e-paper display [10], (b) photograph image of the flexible circuit and the flexible antenna [11], (c) a bendable cell phone [12] and (d) stretchable electronics with a mesh design wrapped onto a model of a fingertip [7].

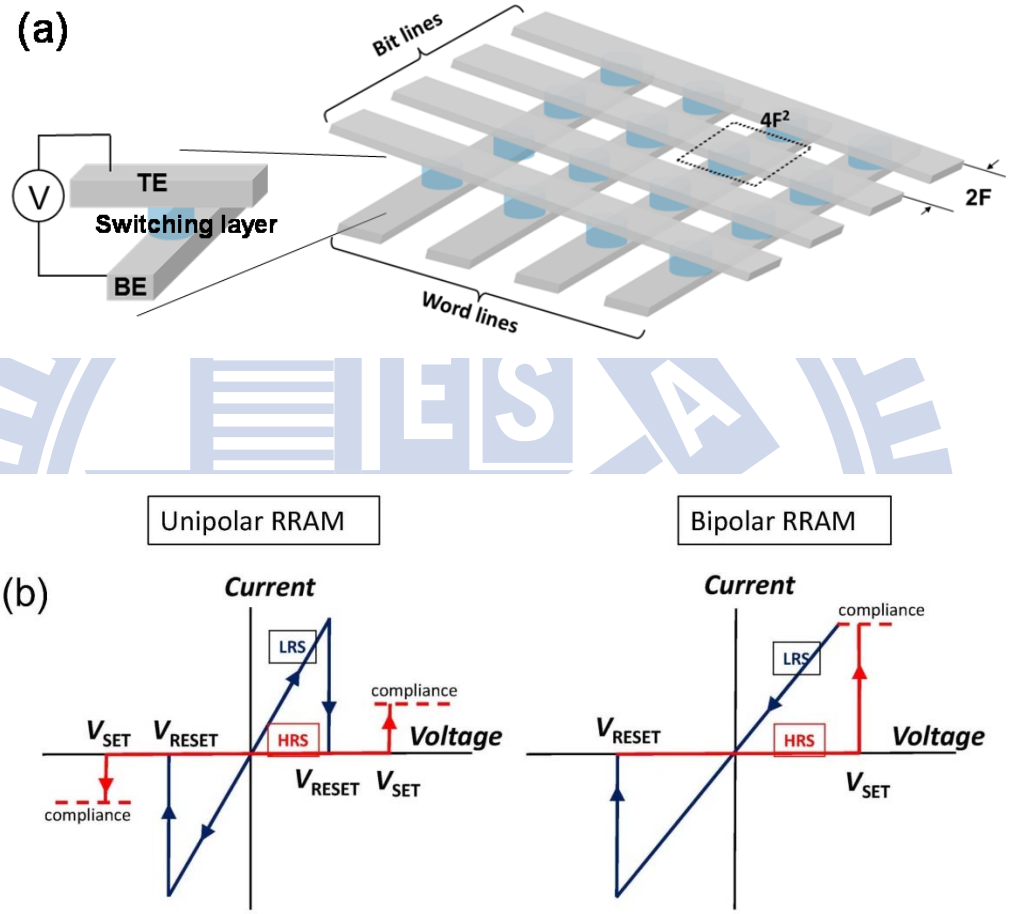

Fig. 1.3 (a) Schematic diagram of a crossbar RRAM, consisting of each memory element sandwiched between top and bottom electrodes with an electrode pitch of 2F, and (b) *I-V* switching curves of unipolar switching (left) and bipolar switching (right).

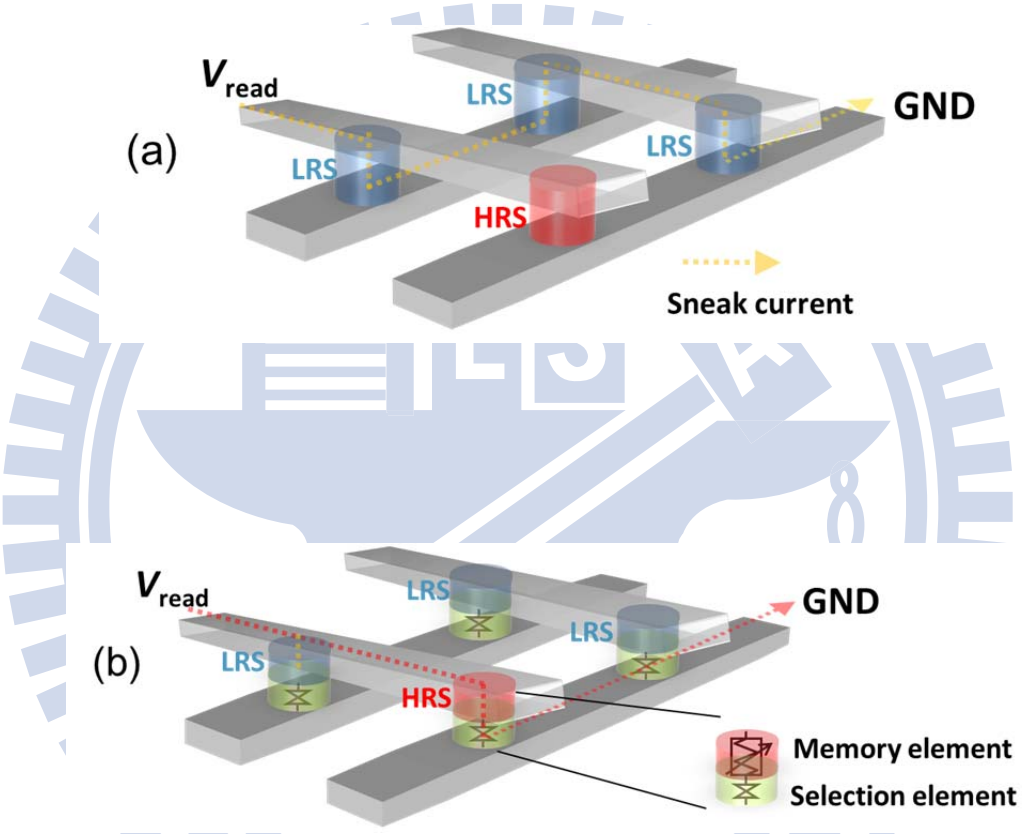

Fig. 1.4 Schematic diagrams of a crossbar structure: (a) without selection elements, where the sneak current through surrounding cells during a reading process and (b) with selection elements to cut off the sneak current through LRS cell.

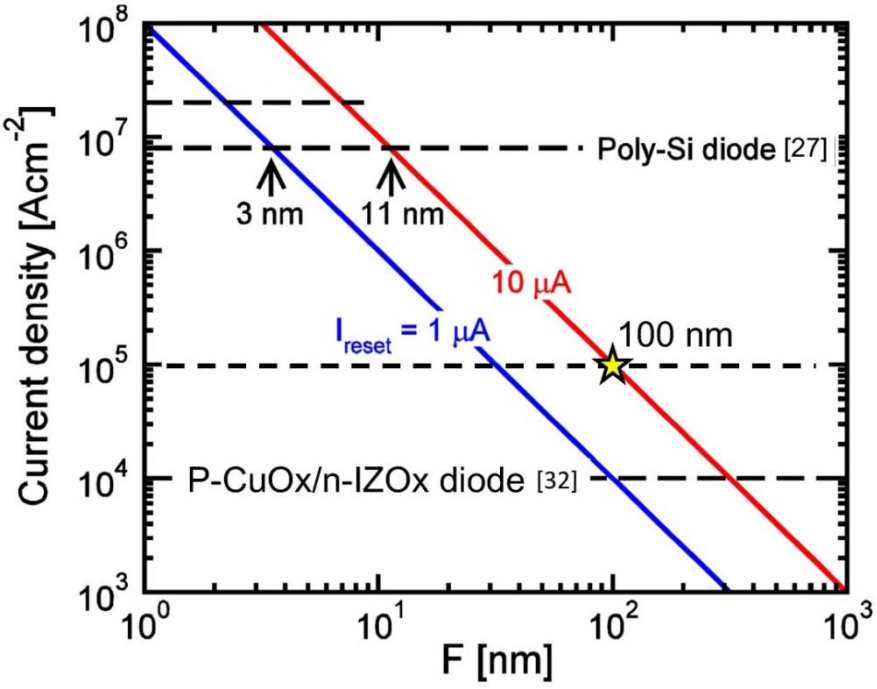

Fig. 1.5 Calculated minimum current requirement of I_{RESET} as a function of technology node F, in which current density of 10^5 A/cm^2 is required for I_{RESET} of 10 μA at 100 nm technology node [24].

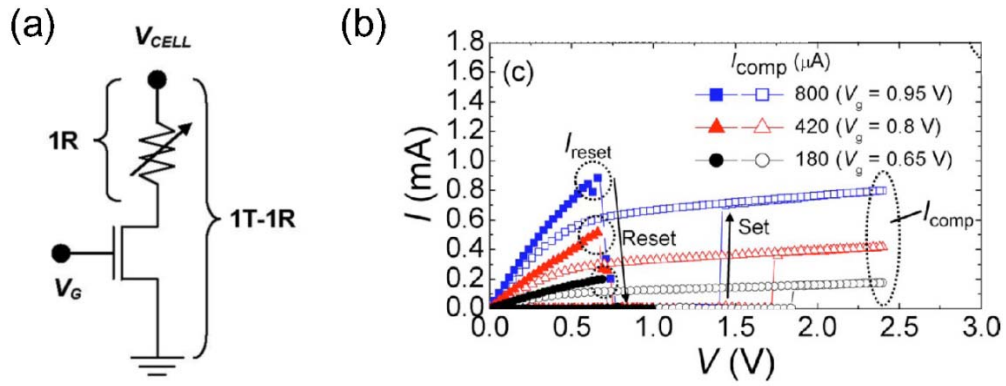

Fig. 1.6 (a) Circuit configuration of a 1T1R cell and (b) the measured SET/RESET characteristics for 1T1R devices, where a higher V_G was used for RESET process and a lower V_G for SET process [24].

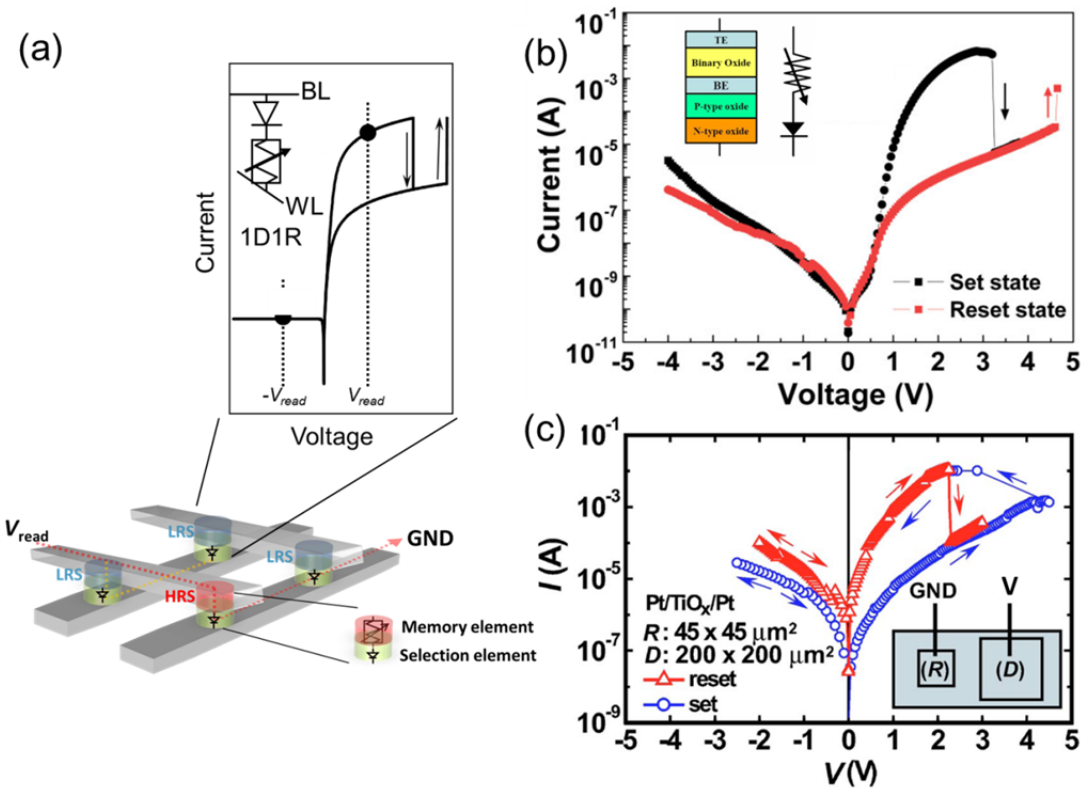

Fig. 1.7 (a) Schematic structure of a 1D1R crossbar array and its typical *I-V* switching curve, and (b) 1D1R *I-V* characteristics of the combined RRAM element and p-oxide/n-oxide diode [31] and (c) the series connected Pt/TiO$_x$/Pt/TiO$_x$/Pt device [35].

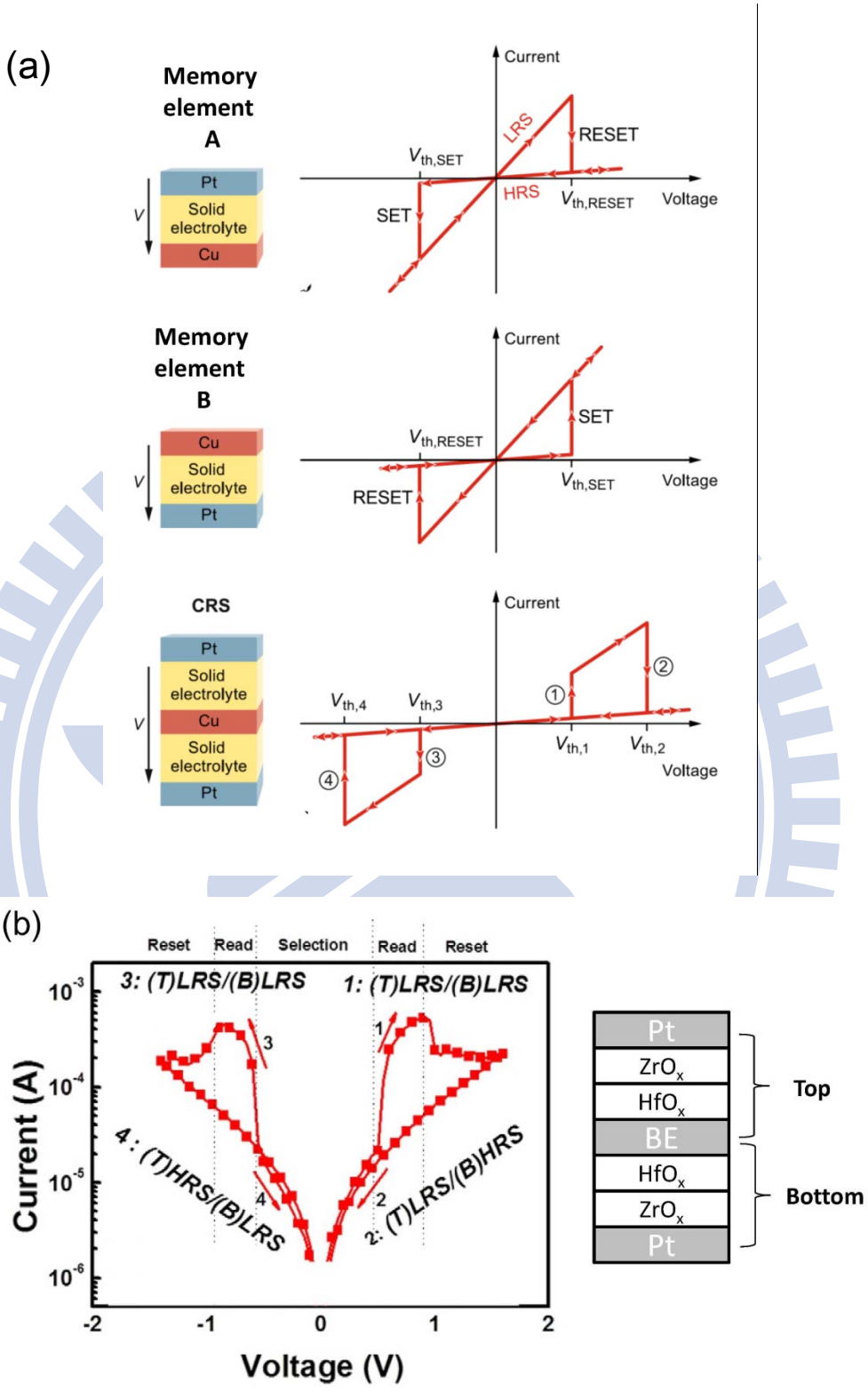

Fig. 1.8 (a) Schematic concepts of Complementary Resistive Switches (CRS) and their representative CRS *I*-*V* curves [39], and (b) the measured CRS *I*-*V* characteristics of an anti-serial connected Pt/ZrO_x/HfO_x/BE/HfO_x/ZrO_x/Pt stacking structure [41].

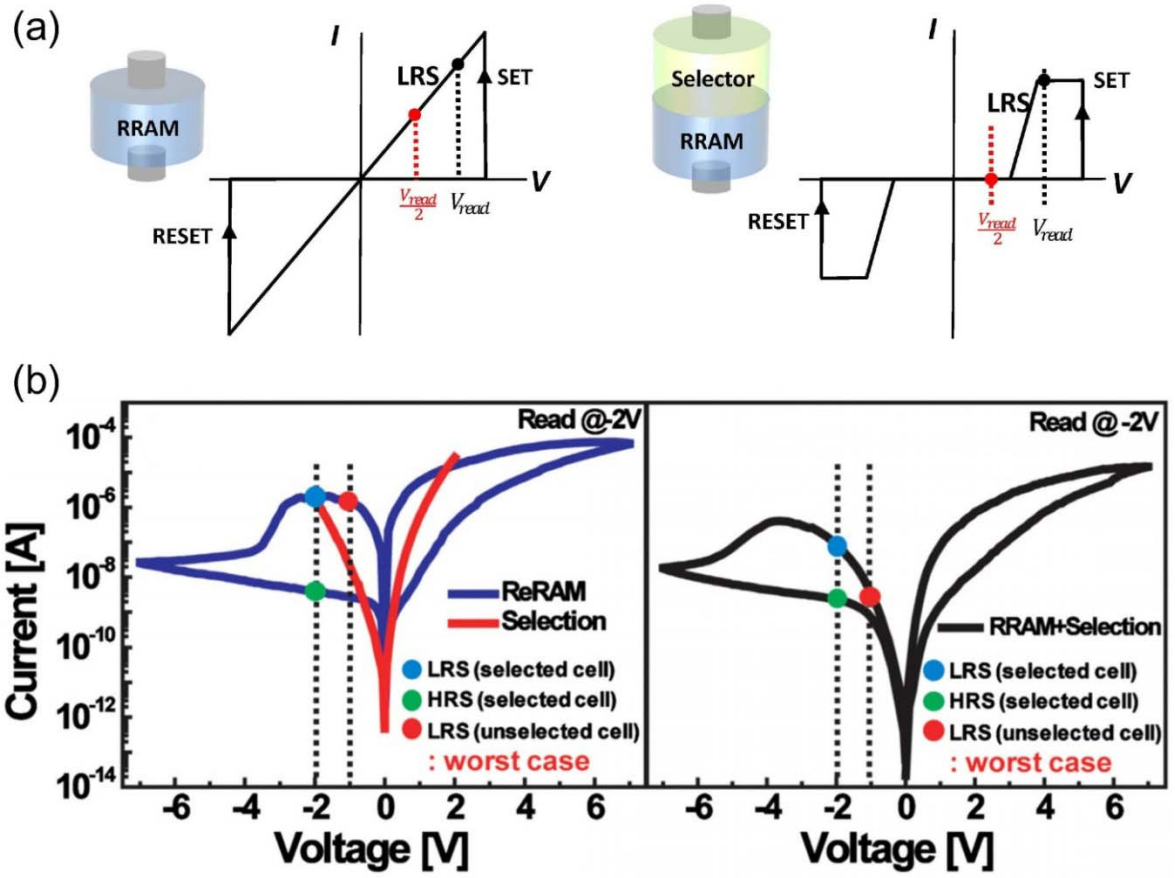

Fig. 1.9 Comparison of $V_{dd}/2$ reading characteristics of a bipolar RRAM without and with a selector and (b) the measured bipolar 1S1R *I*-*V* curve of externally connected Pt/TiO_{2-x}/TiO_2/W and Pt/TiO_2/TiN device [43].

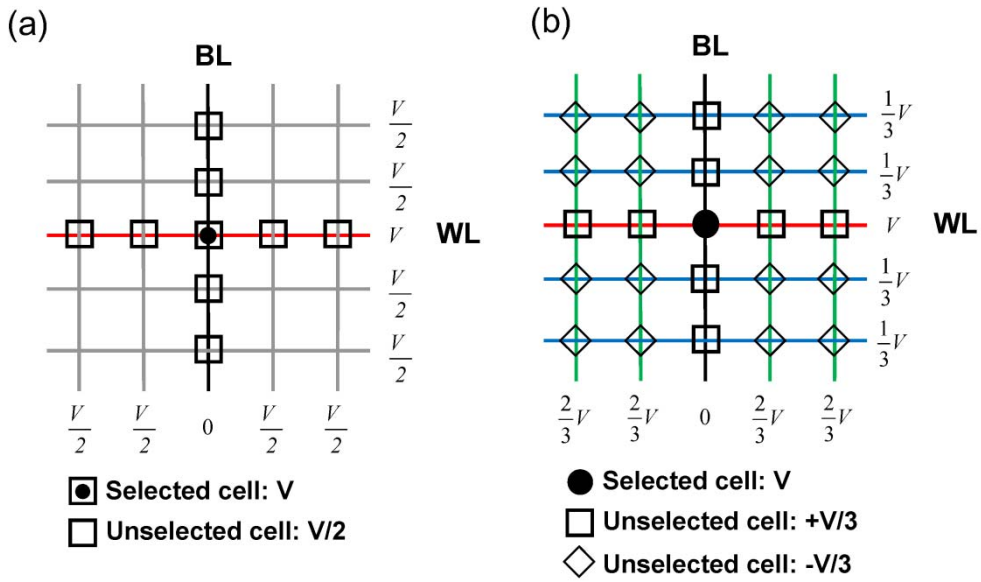

Fig. 1.10 Schematic of the $V_{dd}/2$ and (b) $V_{dd}/3$ SET/RESET scheme. Only the selected cells on the activated WL and BL are subjected to a writing voltage of V.

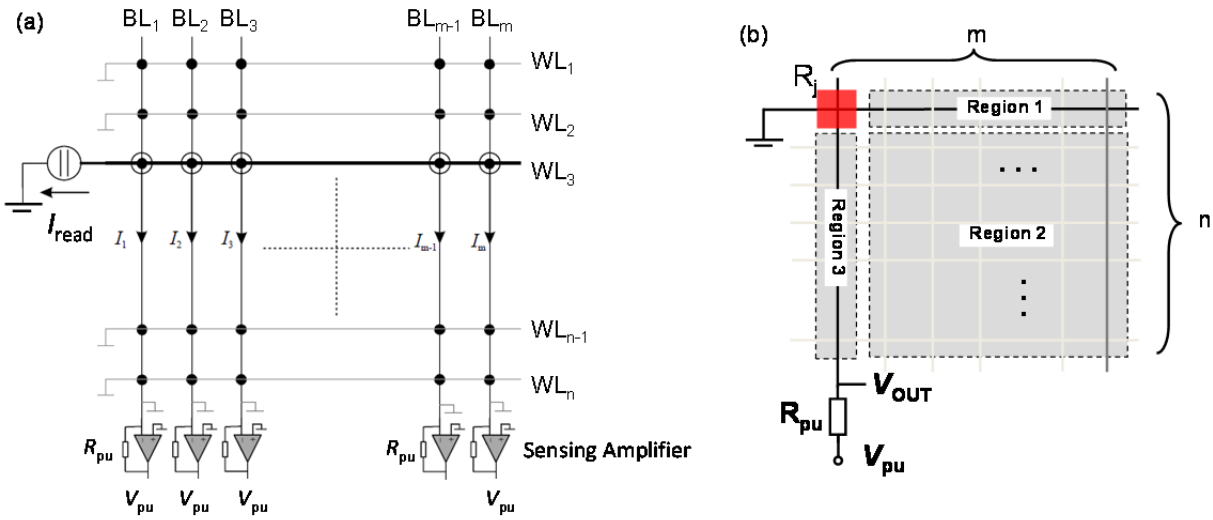

Fig. 1.11 Circuit diagram of an n × m crossbar array and (b) its corresponding equivalent circuit when V_{read} was applied at the corner of the crossbar array.

Configuration	1	2	3	4	5	6	7	8	9
Unsel. WLs	F	F	F	V_{dd}	V_{dd}	V_{dd}	0	0	0
Unsel. BLs	F	V_{dd}	0	F	V_{dd}	0	F	V_{dd}	0
Accessibility	No	No	Yes	No	No	No	Yes	Yes	Yes

Labels: “0” = grounded; “F” = floating

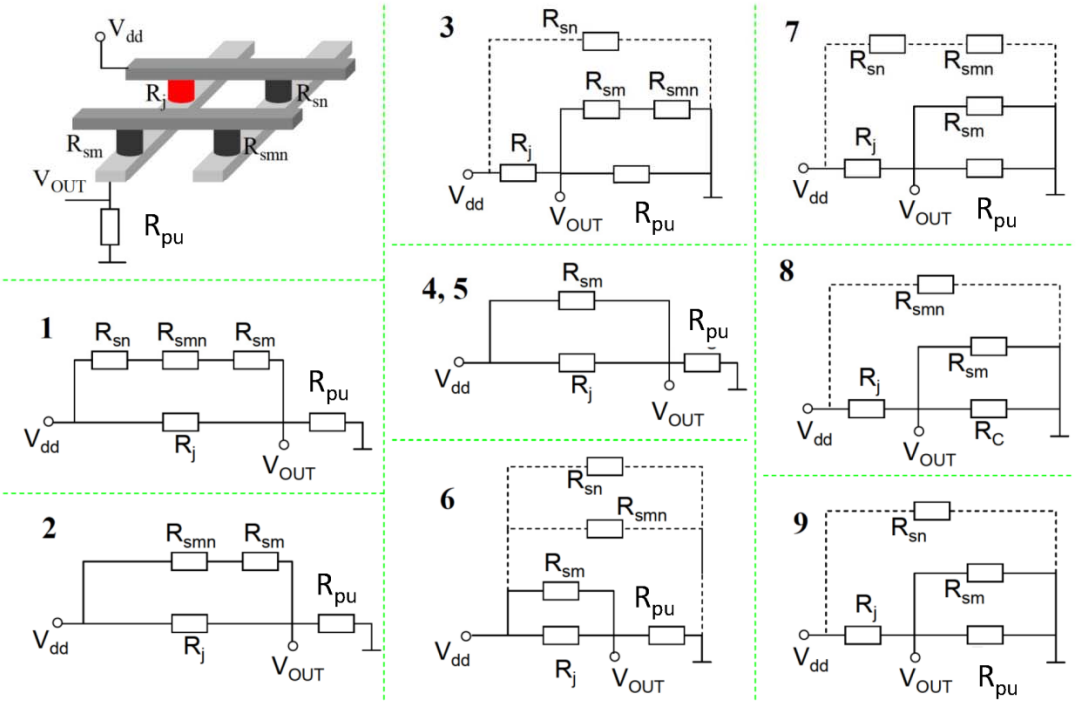

Fig. 1.12 Summary of possible voltage configurations and their equivalent circuits during read operation [46].

Chapter 2

Stable Rectification to Resistive-Switching in $Ti/TiO_2/Pt$ MIM Diode

2.1 Introduction

RRAM consists of simply a layer of TMO sandwiched between two metal electrodes, ideal for high-density $4F^2$ cross-point memory array. However, read and write disturbance due to the sneak current among neighboring cells is a serious concern in RRAM where the memory states are partially determined by the cell resistance of the sneak path [21, 22]. The unit cell of RRAM inevitably requires an extra transistor or diode to alleviate the problem of disturbance. The one transistor-one resistor (1T1R) cell best leverages the maturity of transistor technology. Nevertheless, it is unfavorable to high-density memory array where the size of unit cell and the low-temperature three-dimensional (3D) stacking is of the interest. On the other hand, the one diode-one resistor (1D1R) cell where oxide diodes with high forward current are utilized possesses compact cell structure and low thermal budget. It holds particular promise for future high-density stackable nonvolatile memory applications [26, 31].

The metal/insulator/metal (MIM) and metal/insulator/insulator/metal (MIIM) structures are among popular implementations of high-current oxide diodes. In MIIM, the rectifying p-n junction is formed by two different oxide layers, one n-type oxide and one p-type oxide. High current density and sufficient ON/OFF ratio have been reported but the high turn-on voltage and ideality factor are less than ideal [31, 50]. The requirement of two thin oxide layers with specific composition also poses challenges in manufacturability. In MIM, the rectifying Schottky junction is formed at the metal/oxide interface. Well-behaved diode

characteristics applicable for the 1D1R RRAM have been achieved [37, 51]. Moreover, most TMOs used in MIM diodes also show pronounced resistive switching properties. For example, Shima et al. [35] have reported the rectifying and resistive-switching behavior in a Pt/TiOx/Pt MIM. However, the study on the transition and controllability between the resistive-switching and the rectification has been largely overlooked in the literature but critical to guarantee stable operation in the 1D1R.

Therefore, in this chapter we fabricated a high-forward-current Ti/TiO_2/Pt MIM diode at room temperature by a very simple evaporation process. Excellent rectifying characteristics including a rectifying ratio of 10^5 at ± 3 V, a forward current density of 2×10^3 A/cm^2, an ideality factor of 1.2, and a turn-on voltage of 0.5V are estimated. We also show that the conduction through the interface of Schottky barrier is inhomogeneous in nature because of the localized oxygen migration. We can therefore furthermore identify the evidence of high current density of TiO_2 diode is due to the local current conduction. In addition, TiO_2 has been known for its excellent resistive-switching properties [18, 53]. Here, we demonstrate the coexistence of diode rectification and bipolar resistive-switching in the identical TiO_2 MIM structure by controlling the electrical forming process. Both operation modes are stable without interference with each other up to 125°C. The physical origins of resistive-switching to rectification are also included in this work.

2.2 Experimental Procedure

Pt bottom electrodes of 80nm with a thin Ti adhesion layer were deposited onto heavily doped n-type Si wafers by electron beam evaporation. After SiO_2 deposition by plasma-enhanced chemical vapor deposition (PECVD), contact-hole structures with size of 0.36 μm^2 to 10^4 μm^2 were defined by photolithography and SiO_2 dry etching. TiO_2 with thickness of 8 nm to 20 nm were deposited by electron beam evaporation using TiO_2

granules (Admat Midas Inc., 99.9 wt% purity) as the source at room temperature. Finally, Ti top electrodes of 80 nm were deposited by electron beam evaporation and lift-off process. The detailed process flow and device structures are illustrated in Fig. 2.1. The as-deposited TiO_2 appeared amorphous can be examined from the *X*-ray Diffraction (XRD) as shown in Fig. 2.2, where no crystalline signal was detected except the signal of Pt bottom electrode. The estimated dielectric constant (κ) was around 18.5 from inspections of cross-section TEM and capacitance measurement. In Fig. 2.3, *X*-ray Photoelectron Spectroscopy (XPS) revealed considerable non-lattice oxygen in TiO_2 layer, indicating substantial deficient oxygen existed in the as-deposited TiO_2 film. After an additional 400^{o}C annealing in O_2 ambient, the binding energy of oxygen peaked at 531 eV and the broaden tail from the non-lattice oxygen vanished. All electrical measurements were carried out by applying voltage on the Ti top electrode while the Si substrate was grounded.

2.3 Results and Discussion

2.3.1 Current-voltage characteristics of Ti/TiO_2/Pt diode

Figure 2.4 illustrates the rectifying characteristics of the Ti/TiO_2/Pt MIM diode. The asymmetry of current density-voltage (*J*-*V*) curves is the consequence of different Schottky barrier heights at the Ti/TiO_2 and the TiO_2/Pt interfaces. When a positive voltage applies on Ti, electrons inject from Pt to TiO_2 and experience a substantial Schottky barrier. On the other hand, when applying a negative voltage on Ti, electrons inject from Ti to TiO_2 and first experience the diode build-in potential owing to the metal work function difference between Ti and Pt. As the negative voltage increases, the current increases exponentially by modulating the potential barrier of the injected electrons. Finally, the forward current is limited by the smaller barrier at the Ti/TiO_2 interface. The current dependence on the electric field *E*, Ln (*J*) versus $E^{1/2}$, shown in the inset of Fig. 2.4, confirms that the Schottky

emission is the dominant transport mechanism at high forward bias. Furthermore, we found the first *I-V* sweep of the diode is distinctly different from the rest of sequential sweeps. The turn-on voltage was lowered by 0.7 V with an improved ideality factor of 1.2. While the reverse current increases about one order of magnitude, the forward-bias current at voltage of −2 V remains the same. The turn-on voltage in the Ti/TiO_2/Pt MIM diode is controlled by the build-in potential while the reverse and forward currents are governed by the Schottky barriers at the TiO_2/Pt and Ti/TiO_2 interfaces, respectively. The discussion of Schottky barrier at the TiO_2/Pt interface modulated by the first *I-V* sweep will be evaluated in next section, strongly supported by the evidences of physical observation.

2.3.2 Physical characteristics of Ti/TiO_2/Pt diode

Figure 2.5 shows a series of snapshots of visible bubbles, as different voltages were applied, observed by the optical microscope. After the voltage sweeps from 0 to +3 V, oxygen bubbles appeared and randomly distributed in the active region. This is attributed to the migration of oxygen ions triggered by the external voltage and thus accumulating beneath the top electrode (Fig. 2.5(b)) [53]. After the external voltage was removed, a much bigger bubbles were formed, which was originated from the migration and combination of neighboring bubbles, as shown in Fig. 2.5(c). With a relatively-large voltage (e.g. +10 V) was applied, a ruin region (permanent breakdown) was observed as indicated by the arrow in Fig. 2.5 (d). The physical deformation of the top electrode was attributed to the drift of oxygen ions in TiO_2 toward the anode where they evolve O_2 gas. Similar bubble formation was previously reported in a Pt/TiO_2/Pt RRAM cell [18]. The degree of bubble formation depends strongly on the thickness of TiO_2 and the polarity of applied voltage. Therefore, 18 nm TiO_2 instead of 8 nm TiO_2 was utilized for the physical characterization in this section.

To further investigate the effect of bubble formation on the diode characteristics, the Ti top electrode was carefully removed in dilute sulfuric acid where the etching rate of TiO_2

film is negligible. The scanning electron microscope (SEM) image in Fig. 2.6(a) reveals scattered surface residues, which are lacking in the virgin samples without the bubble formation. The atomic force microscope (AFM) and the conductive AFM (C-AFM) in Figs. 2.6(b) and 2.6(c) further evidence these residual regions are the local current paths (filaments). This is attributed to the negatively charged oxygen ions that drift towards the anode under the positive bias and become oxygen-deficient at the Ti/TiO_2 interface. The defects at the TiO_2/Pt interface may cause substantial Fermi-level pinning that shifts the Pt workfunction upward and reduces the Schottky barrier at the TiO_2/Pt interface [37]. As a result, lower turn-on voltage and higher reverse-bias current are expected with oxygen-deficient TiO_2. The oxygen piling up at the anode may react with Ti top electrode to form TiO_x, which is insoluble in dilute sulfuric acid and results in the observed residues. Moreover, because the migration of oxygen ions is not homogeneous, the diode current is the superposition of the components through the conduction channel with oxygen-deficient TiO_2 and through the rest of intact TiO_2. The prior dominates at the low voltage regime while the latter becomes more important and eventually prevails at the high voltage regime owing to its larger area within the device. In Fig. 2.7, higher current density with smaller contact-hole size patterned by photolithography can be directly observed, showing another evidence of inhomogeneous conduction in the Ti/TiO_2/Pt diode.

2.3.3 Conduction mechanism

Figure 2.8 shows the temperature-dependent Schottky fitting of the Ti/TiO_2/Pt MIM diode measured from 25 to 125°C. The extracted barrier height at the TiO_2/Pt interface is estimated 0.73 eV by extrapolating to V=0. The smaller than expected barrier height is the result of the Fermi-level pinning phenomenon. The extracted barrier height at the Ti/TiO_2 interface is estimated 0.13 eV at V= −0.85 V, which eventually limits the maximum forward-current density. J= 10^4 A/cm^2 at |3V| reported here is comparable with other

TiO_2-based MIM diodes [35, 37]. Future optimization to reduce the interface barrier will be the key factor to increase the current density. Note that in comparison with the Pt/TiO_x/Pt MIM, where the rectification is achieved by the asymmetrical oxygen composition in TiO_x [35], the Ti/TiO_2/Pt MIM not only shows improved rectifying characteristics but also requires less complexity in fabrication.

2.3.4 Rectifying mode to resistive-switching mode

Figures 2.9(a) and (b) illustrate the stable rectifying characteristics of the MIM diode at 25 and 125 °C up to at least a thousand cycles under ±3 V sweep. The ON/OFF ratio keeps at least three orders of magnitudes even at 125 °C, and the forward-current density remains larger than 6×10^2 A/cm^2 at 25 °C. A separate measurement also confirms no significant degradation of the diode characteristics under a constant 3 V stress up to 1000 s at 25 °C. In considering a practical 1D1R RRAM cell with SET/RESET pulse width of 100 ns, the result guarantees stable operation at least 10^{10} times. In Figs. 2.9(a) and (b), both forward and reverse current are reduced gradually after repeated cycling, especially at high temperature. The exact cause is still under investigation. One plausible explanation is that the bulk defects in TiO_2 generated under stress deviate the current transport from the simple Schottky emission. In addition, the Ti/TiO_2/Pt MIM may switch from the rectifying mode to the resistive-switching mode by applying a voltage larger than the soft-breakdown (forming) voltage around +5 V and appropriate current compliance. Figure 2.9(c) shows the reproducible bipolar resistive-switching with very tight distribution on SET/RESET voltages and high/low resistances. At the low voltage regime of the rectifying mode, the current transport is limited by the Schottky emission in local filaments. After forming, much stronger filaments across the entire thickness of TiO_2 are developed by oxygen migration plus joule heating [55]. The filaments extending into the metal/oxide interfaces may completely destroy the Schottky barriers and thus the corresponding rectification. Therefore,

controlling the forming process is critical to ensure no interference between rectification and resistive-switching. According to the popular E-model for oxide breakdown [56], the time to breakdown t_{BD} is expressed as follows:

$$t_{BD} = A\exp(-\gamma E_{ox})\exp(\frac{E_a}{k_B T}) \qquad (Eq.\ 1.1)$$

where A is a constant, is the field acceleration factor, E_{ox} is the oxide field, E_a is the thermal activation energy for oxide breakdown, k_B is the Boltzmann constant, and T is the absolute temperature. The experimental value of E_a for TiO_2 in the literature is 0.5–0.7 eV [56]. γ increases with the dielectric constant in the thermochemical model for oxide breakdown [57]. Therefore, for our TiO_2 (k=18.5) should be close to 13.6 MV/cm reported for Ta_2O_5 (k= 26) [57]. Reasonable E_a and high γ in TiO_2 enable the stable diode rectification at ±3 V without triggering the forming in our interested time span even at 125 ° C.

2.4 Summary

In this study, we report the transition of stable rectification and resistive-switching properties in a Ti/TiO_2/Pt MIM. The oxygen migration and localized conductive filaments play important roles in not only the resistive-switching of RRAM but also the rectification of oxide diodes. When the current conduction through the oxygen-deficient TiO_2 filaments is limited by the interface Schottky barriers, the diode rectification prevails. After forming at higher voltage, much stronger filaments destroying the interface Schottky barrier give rise to the reproducible resistive-switching. The rectification properties are stable up to 125 °C and 10^3 cycles under ±3 V sweep without interference with resistive-switching. Moreover, the current density of TiO_2 MIM diodes more than 10^4 A/cm^2 can be achieved, showing satisfactory requirement of TiO_2 MIM diodes for future 1D1R RRAM applications.

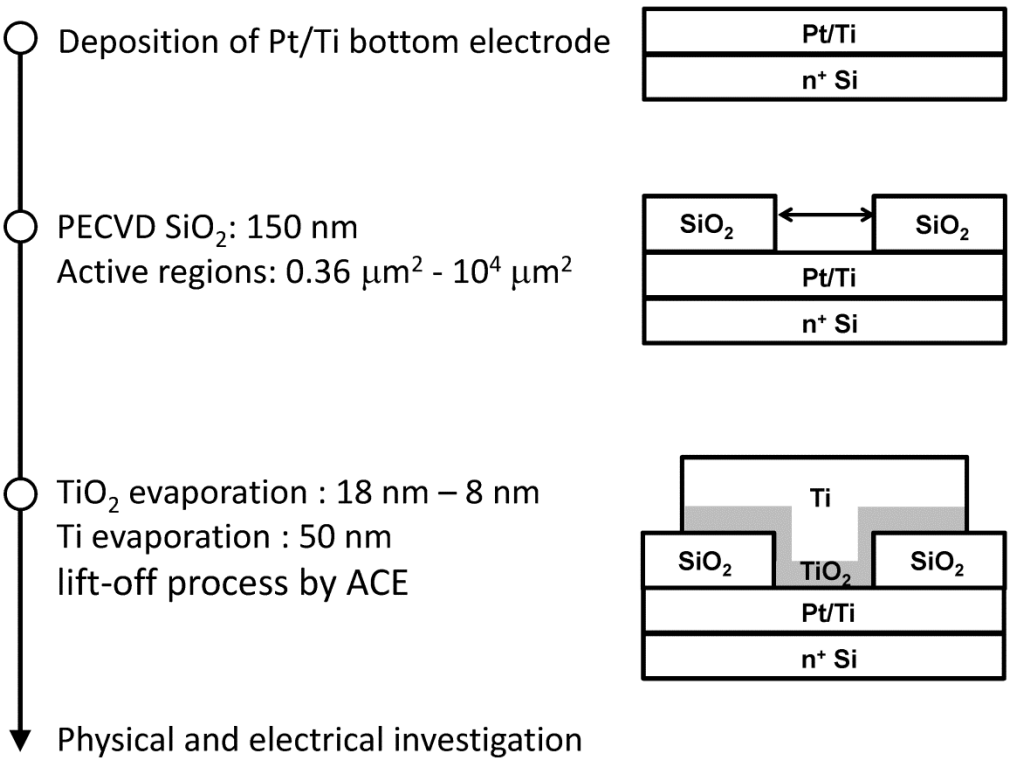

Fig. 2.1 Process flow of the room-temperature fabricated TiO_2 oxide diode

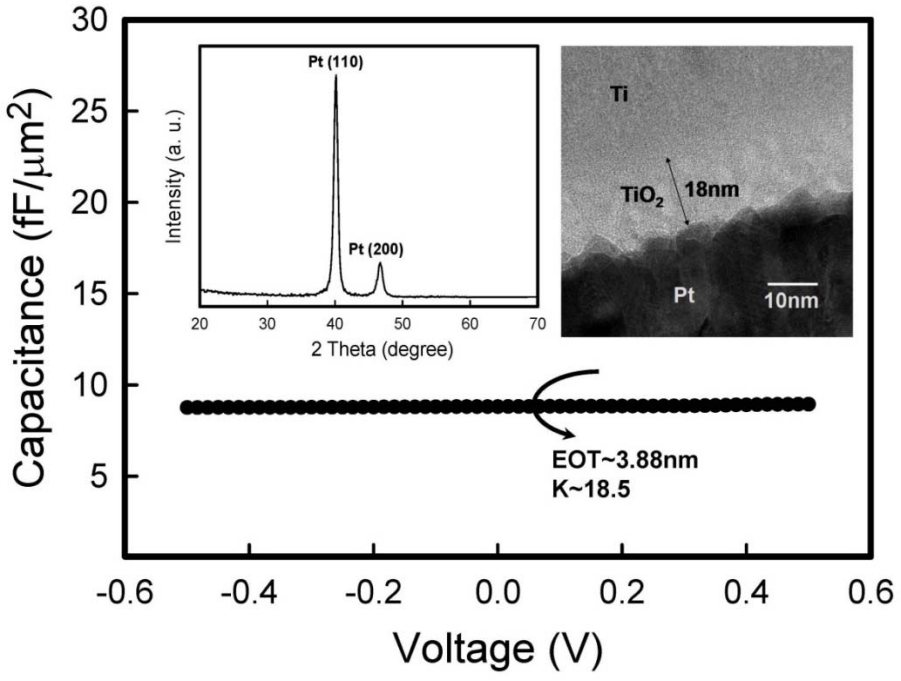

Fig. 2.2 Capacitance measurement of $Ti/TiO_2/Pt$ MIM diode in the area of 10^4 μm^2. Inserts show the XRD pattern and the TEM image of the as-deposited TiO_2.

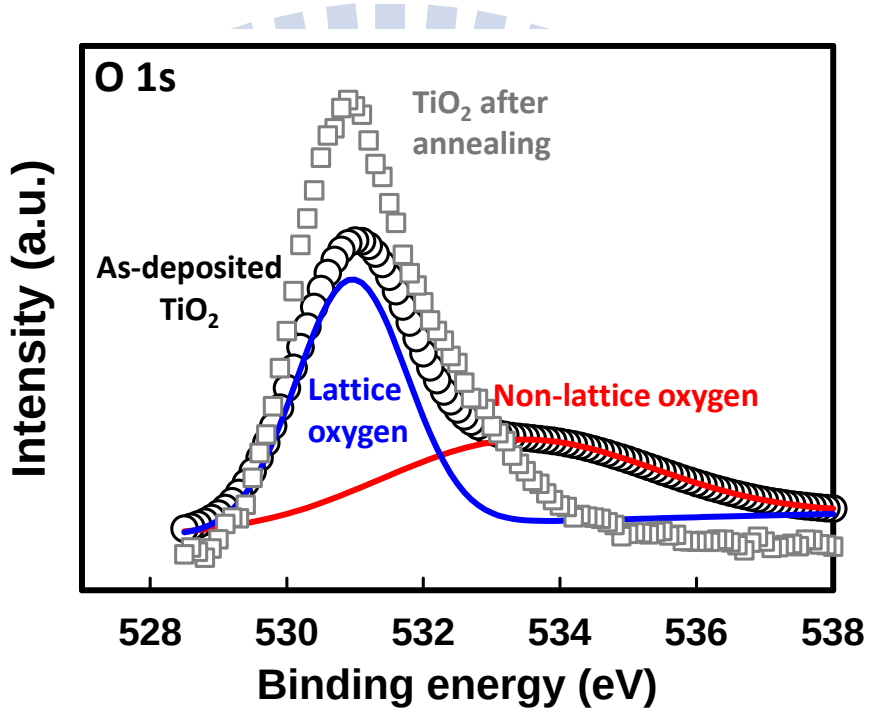

Fig. 2.3 XPS spectrum of the O 1s core level in TiO_2 film. The signal of non-lattice oxygen in TiO_2 was eliminated by an additional 400 ^oC annealing in O_2 ambient.

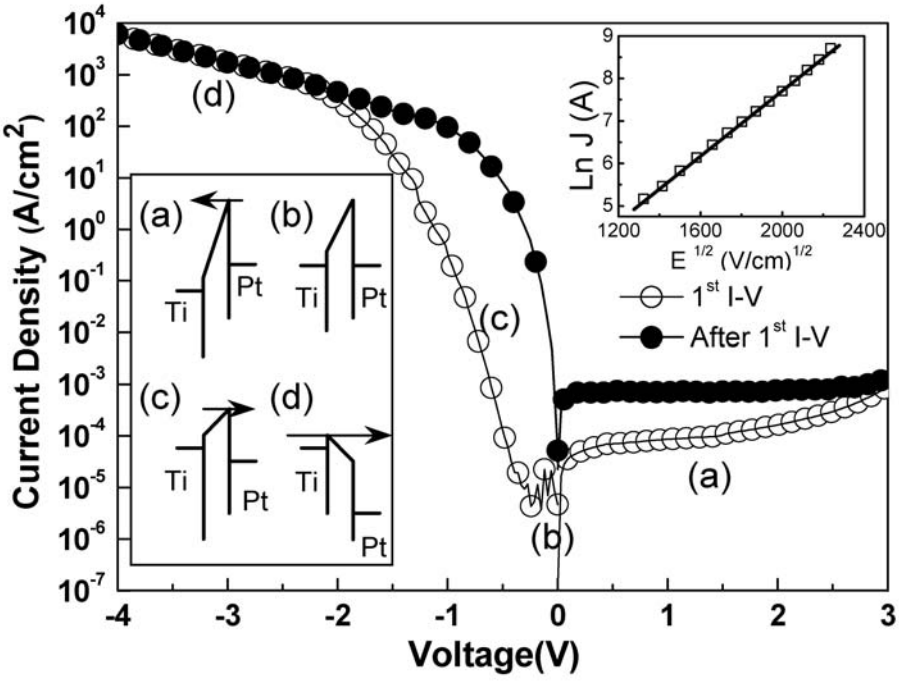

Fig. 2.4 *J-V* characteristics of a typical Pt/TiO_2/Ti MIM diode. The thickness of TiO_2 is 8 nm. Insets show the band structures of the MIM under different biases and the Schottky-emission fitting of Ln *J* vs $E^{1/2}$ from -1.4 to -4 V, respectively.

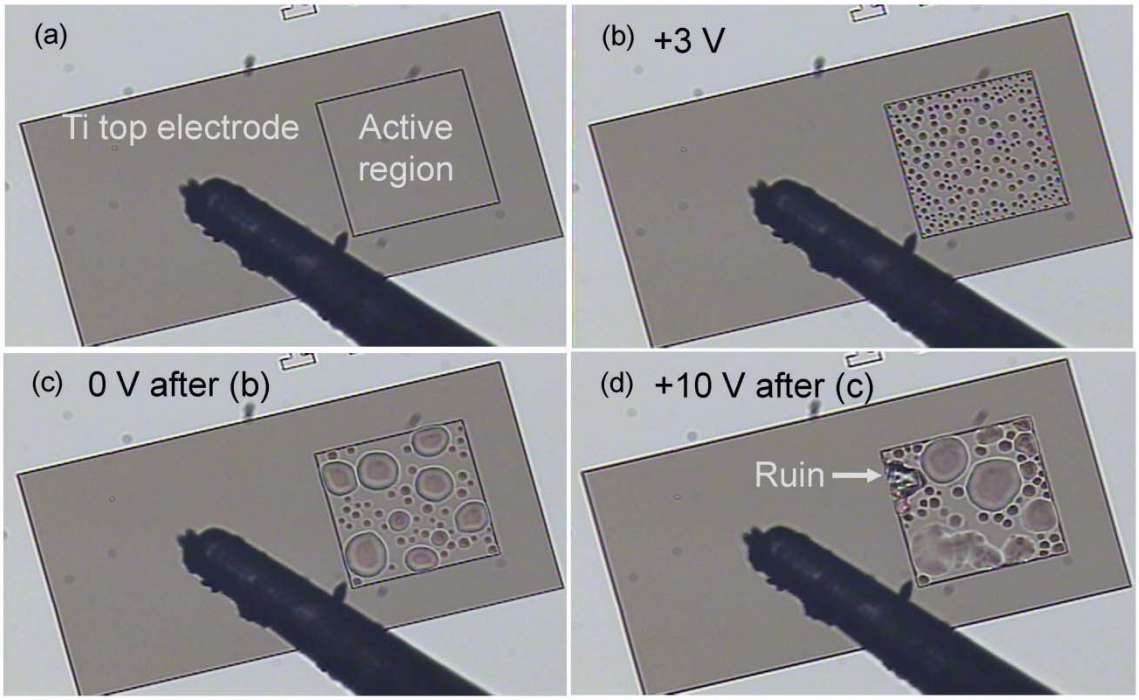

Fig. 2.5 Optical microscopy images of top-view Ti/TiO_2/Pt diode. The thickness of TiO_2 is 18 nm and the area of active region is 100 μm × 100 μm. Gas bubbles were induced by a series of voltage configurations from +3 V to +10 V.

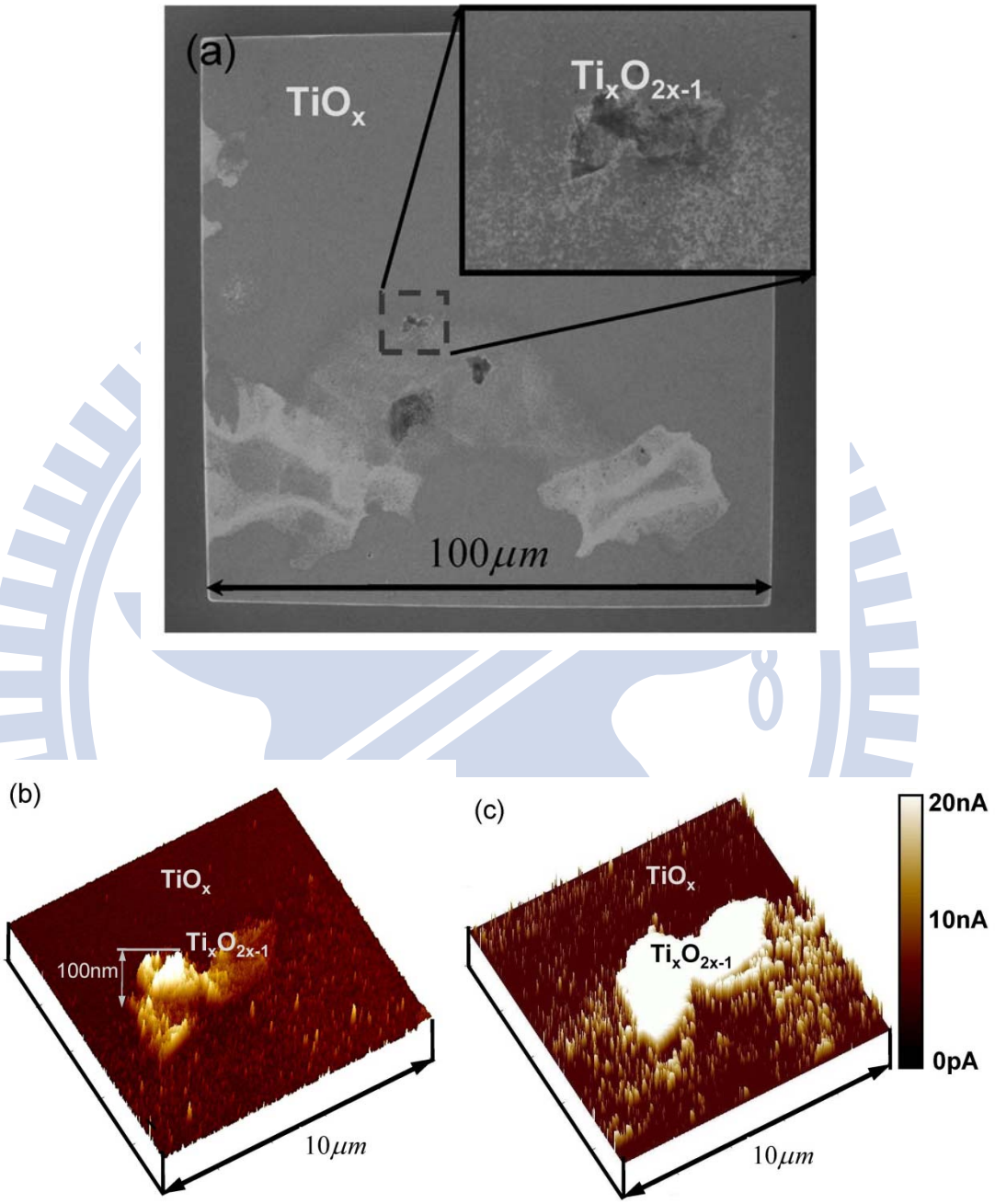

Fig. 2.6 (a) SEM image after removing the Ti top electrode, (b) Surface morphology by AFM and (c) surface conductivity by C-AFM on the specific position labeled in (a).

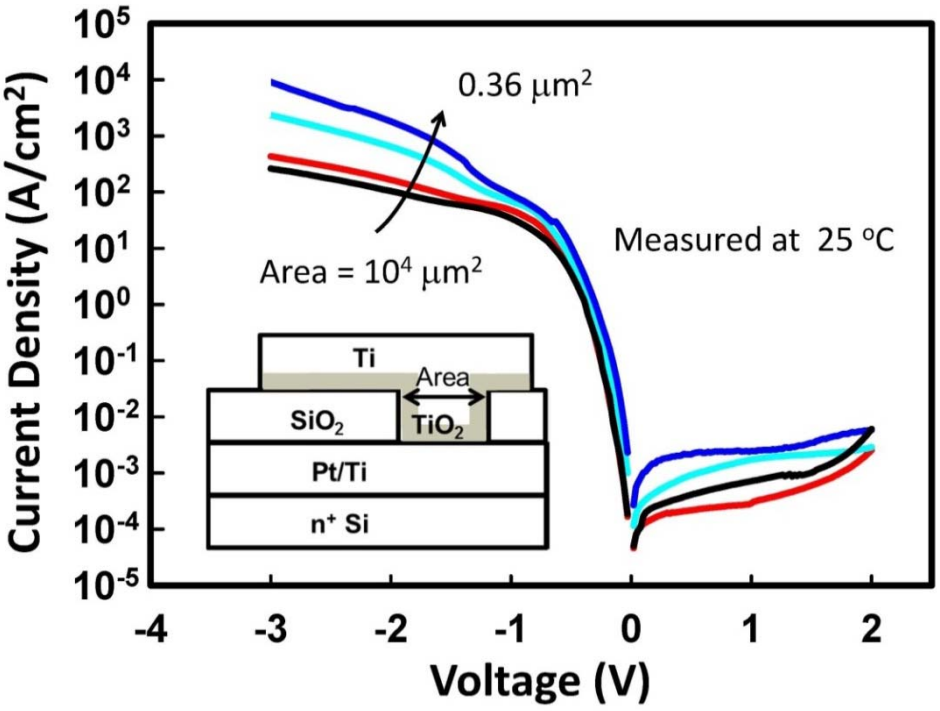

Fig. 2.7 *J-V* characteristics of $Ti/TiO_2/Pt$ MIM diodes with various device areas fabricated by photolithography process. Current density of 10^4 A/cm^2 at －3 V with device area down to 0.36 μm^2 was obtained.

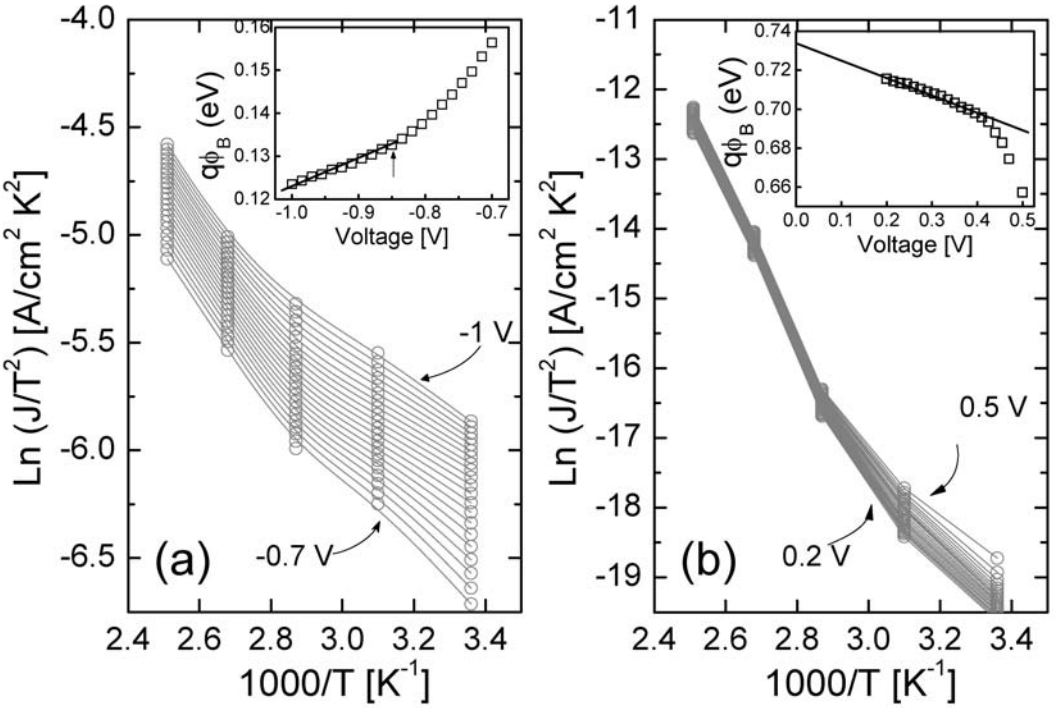

Fig. 2.8 Temperature-dependent Schottky-emission fitting of the Ti/TiO_2/Pt MIM diode at (a) forward and (b) reverse bias measured from 25 ^{o}C to 125 ^{o}C. Insets show the extracted Schottky barrier heights as a function of applied voltages.

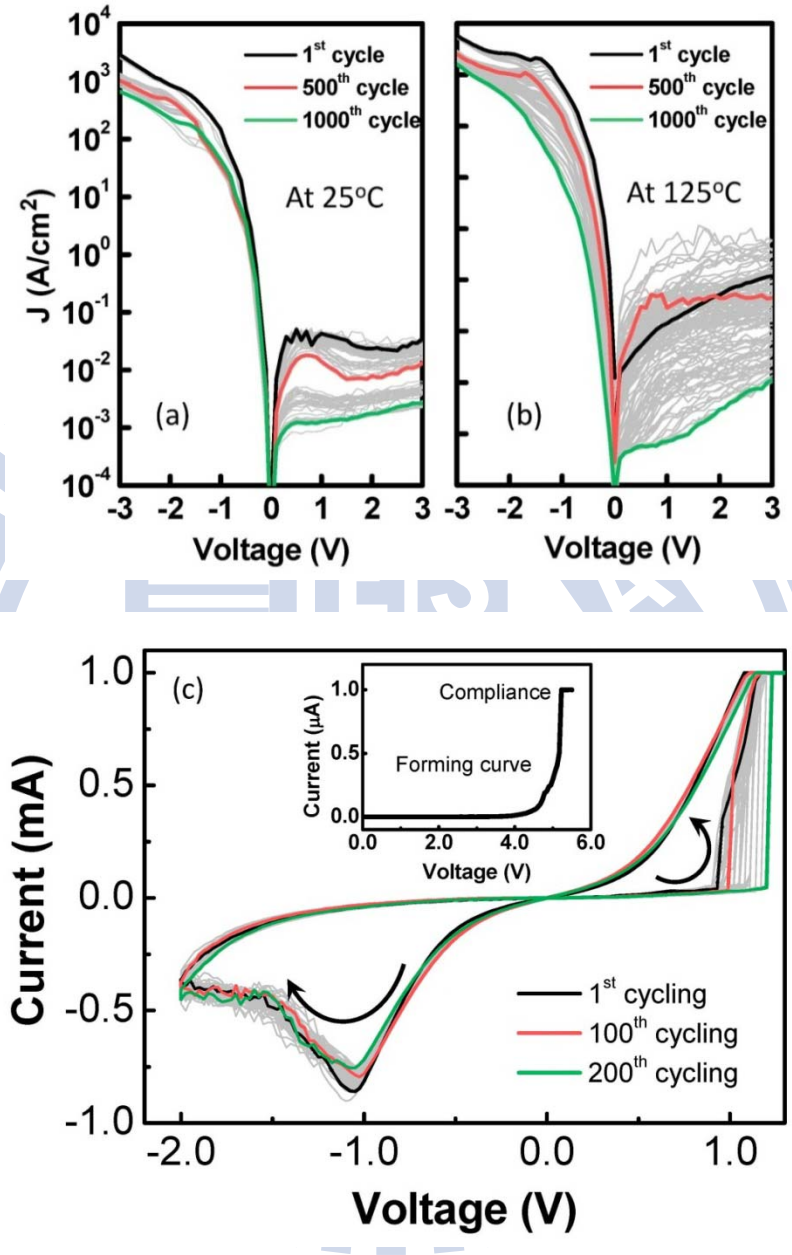

Fig. 2.9 Endurance characteristics of the TiO_2 MIM diode at (a) 25 °C and (b) 125 °C, showing a stable operation more than 10^3 cycles under ±3V sweep. (c) 200 successive bipolar resistive-switching cycles after the forming at +5V. Inset shows the forming process with compliance current of 1 μA.

Chapter 3

Ti/TiO_2/Pt Oxide Diode for 1D1R Resistive-Switching Memory on Flexible Substrates

3.1 Introduction

It is well known that flexible electronics have received increasing attention because of their advantages of low cost, light weight, flexibility, and capability of large-area process. However, traditional Si technology requiring high-temperature process is incompatible with the low glass transition temperature of flexible substrates. In contrast, oxide-based materials deposited at low temperature have shown promising candidates for flexible electronics applications, such as indium-gallium-zinc oxide for thin film transistors in the flexible active matrix backplane [58]. To realize another fundamental building block of flexible electronics, namely nonvolatile memory, considerable efforts are being made to develop RRAM on flexible substrates, exploring the nonvolatile variable resistance in transition metal oxides [47, 49, 59]. In addition to its superior memory characteristics, RRAM is highly attractive for flexible nonvolatile memory because of its simple crossbar architecture and low-temperature fabrication [14]. However, a passive crossbar array is known to suffer from the so-called sneak current problem and difficult to scale up beyond 64 bits because of severe read interference [21, 22]. The development of low-temperature selection devices in series with resistive-switching (RS) memory elements on flexible substrates is critical, but significantly less emphasized. In Chapter 2, we have successfully demonstrated a rectifying oxide diode fabricated at room temperature on Silicon substrates [60, 61]. The TiO_2-based metal-insulator-metal (MIM) devices with a Pt bottom electrode exhibited excellent

rectifying, bipolar switching and unipolar switching characteristics by choosing appropriate top-electrode materials. The rectifying oxide diode is applicable to the compact one diode-one resistor (1D1R) crossbar architecture and suppresses the read interference in high-density crossbar arrays [26, 32, 62].

In this chapter, we discuss 1D1R memory cells, consisting of a Ti/TiO_2/Pt diode element and two different types of RS memory elements, namely Pt/TiO_2/Pt and Ni/HfO_2/Pt. The TiO_2-based diode and RS element are interesting because of the potential for just using a monolithic TiO_2 to form the 1D1R cell, but the high reset current (I_{RESET}) of the TiO_2 RS element led to unstable unipolar switching in the 1D1R cell. On the other hand, when integrating with the HfO_2 RS element with lower I_{RESET}, stable unipolar RS characteristics can be realized. Additionally, the excellent rectifying characteristics with rectification ratio at reverse and forward bias was capable of realizing a compact 512-kilobit (Kb) crossbar memory array with at least 10% readout margin. Because all device fabrication was completed at room temperature, the proposed 1D1R cell was successfully demonstrated on a polyimide (PI) substrate and promising for flexible and high-density memory applications by roll-to-roll processing at an extremely low cost in the future [63].

3.2 Experimental Procedure

Prior to the device fabrication, 75-μm-thick Kapton® polyimide (PI) substrates were cut and ultrasonically cleaned in acetone solution for 10 min to remove particles and contamination, followed by a 100^{o}C baking for 30 min. The cleaned PI substrates were then electrostatically attached to silicon wafers. Because the PI substrate is susceptible to water absorption, a buffer layer of SiO_2 with a thickness of 300 nm was deposited by plasma-enhanced chemical vapor deposition (PECVD). Platinum bottom electrodes of 80 nm with a thin Ti adhesion layer were deposited onto substrates by electron beam evaporation.

To fabricate the TiO_2 oxide diode and RS memory element, the TiO_2 active layers with a thickness of 50 nm were deposited by electron beam evaporation at room temperature, and then 100-nm thick Ti and Pt top electrodes were patterned by shadow-mask technique for the $Ti/TiO_2/Pt$ diode and the $Pt/TiO_2/Pt$ RS element, respectively. To fabricate the HfO_2 RS memory element, the HfO_2 active layers with a thickness of 80 nm were prepared by dc magnetron reactive sputtering using a Hf target (99.5%) in a mixture of Ar and O_2 at room temperature, and then 100-nm thick Ni top electrodes were patterned by shadow-mask technique for the $Ni/HfO_2/Pt$ RS element. All devices reported in this study were fabricated completely at room temperature without any additional thermal treatment. In addition to the flexible devices, conventional devices on silicon substrates were also prepared using the identical process by photolighography processes. The detailed process flow is shown in Fig. 3.1. All electrical measurements were performed using a HP-4156B semiconductor analyzer. The 1D1R cells were externally connected and voltage was applied to the Ni or Pt top electrode of the RS memory element while the Ti top electrode of the TiO_2 diode element was grounded.

Figure 3.2 (a) shows the photograph of a fabricated flexible device under highly mechanical strain. The measurement setup using a concave stage with a radius of 30 mm to characterize devices at the bending state is shown in Fig. 3.2 (b).

3.3 Results and Discussion

3.3.1 Flexible $Ti/TiO_2/Pt$ diode

Figure 3.3 displays the rectifying characteristics of the $Ti/TiO_2/Pt$ diode at both flat and bending conditions. Even though fabricated on the flexible substrate, $Ti/TiO_2/Pt$ diodes exhibit a large rectifying ratio of 10^6 at ±1 V, an ideality factor of 1.2, and robust endurance up to hundreds of successive DC sweeps without dielectric breakdown. The results are

comparable with those fabricated on Si, showing minimal substrate effect [61]. A rectifying ratio of more than 10^5 at ±1 V can be maintained in the bended devices, indicating negligible degradation on the diode characteristics under bending. The asymmetry of current-voltage (*I*-*V*) curves was explained by the different Schottky barrier heights at the Ti/TiO_2 and the TiO_2/Pt interfaces as we have discussed in Chapter 2. When applying negative voltage to the Pt electrode, electrons injected from Pt to TiO_2, but encountered a substantial Schottky barrier. When applying positive voltage to Pt, electrons injected from Ti to TiO_2. The current increased exponentially with the voltage bias and was eventually limited by the smaller barrier at the Ti/TiO_2 interface and parasitic series resistances.

3.3.2 Pt/TiO_2/Pt memory element and monolithic TiO_2 1D1R cell

In contrast to the Ti/TiO_2/Pt bipolar RS memory element, the Pt/TiO_2/Pt RS memory was nonpolar and applicable to the 1D1R crossbar array utilizing unipolar RS. The oxygen-deficient filament was believed to be responsible for the observed RS [61]. Figure 3.4 shows the typical unipolar RS curves of the Pt/TiO_2/Pt RS memory by positive SET (V_{SET}) and RESET (V_{RESET}) voltages. Although the unipolar RS in our structure was stable, the I_{RESET} was over 10 mA, comparable to the maximum current a TiO_2 diode can provide. The high I_{RESET} not only resulted in excessive switching power undesirable for low-power operation, but also deteriorated the stability of RS in a 1D1R cell. Because of the comparable current in the diode and RS element, the diode series resistance was not negligible in the 1D1R cell when the RS element was at the low resistance state (LRS). Hence V_{RESET} was significantly increased. In contrast, V_{SET} was less sensitive to the diode series resistance because of the considerably larger resistance of the RS element at high resistance state (HRS). As a result, the programming margin between unipolar V_{SET} and V_{RESET} diminished and unipolar RS became less stable as shown in Fig. 3.5 that the TiO_2 1D1R cell exhibits only a few stable switching cycles without programming error. Figure 3.6 further shows the

predicted programming margin as a function of I_{RESET} at a fixed diode on-current of 10 mA. For a RS memory element with V_{RESET} of 0.5 V and V_{SET} between 2 to 4 V considering cycling variations, I_{RESET} below 1 mA would be required for stable unipolar RS in the 1D1R cells.

3.3.3 Ni/HfO_2/Pt memory element and heterogeneous HfO_2-TiO_2 1D1R cell

The RS in the Ni/HfO_2/Pt memory fabricated on the flexible PI substrate was also nonpolar. Similar to the Ni/HfO_2/Si RS memory reported previously [71], the RS was attributed to the formation of Ni filaments through HfO_2 by Ni ion migration from the top electrode after electrical forming, and rupture and connection of Ni filaments by joule heating and ion migration. The typically unipolar RS with positive V_{SET} and V_{RESET} was highly reproducible as shown in Fig. 3.7(a) with a resistance ratio of HRS to LRS (R_{HRS}/R_{LRS}) of about 10^2 and I_{RESET} less than 1 mA even under bending. Figure 3.7 (b) shows the cumulative plot of HRS/LRS resistance at both the flat and bending states with remarkably tight distributions. Figure 3.8 shows superior immunity to read disturbance and retention characteristics of the HfO_2 RS element regardless of whether the substrate was flat or bended. The reproducible and reliable unipolar RS at the bending state demonstrates the feasibility of RS memory for flexible electronics applications. In Fig. 3.9, by connecting the HfO_2 RS memory with low I_{RESET} and the TiO_2 diode in series, highly reproducible unipolar RS with substantial R_{HRS}/R_{LRS} ratio was realized at positive bias, whereas the current at negative bias remained extremely low due to the reverse-biased diode even when the RS memory was at LRS. The high rectifying ratio shown here is among the best ever reported for the 1D1R cells, including those fabricated on Si substrates [65-67]. Furthermore, Figure 3.10(a) shows the cross-sectional TEM image and the schematic diagram of the vertically stacked Ti/TiO_2/Pt/Ni/HfO_2/Pt structure fabricated by a 3-mask photolithography process. Although,

there is a slight roughness located in the 2nd Pt layer, this stacked structure displays a reproducible unipolar 1D1R RS, indicating the feasibility of stacked 1D1R for crossbar RRAM.

3.3.4 Prediction on read margin in 1D1R crossbar array

In this section, the prediction on the read margin of 1D1R crossbar array is explained using the device parameters extracted from the standalone 1D1R cell in Fig. 3.9. Figure 3.11 depicts the equivalent circuit of an $N \times N$ crossbar memory array in the scenario of read interference where all unselected cells are in LRS [21, 39]. Considering a one bit line pull-up (One-BLPU) read scheme [21], the sneak current can flow through the unselected cells, represented by the parallel resistor networks of R_1, R_2, and R_3 in Fig. 3.11, which leads to read error when the selected cell is in HRS ($R_{selected} = R_{HRS}$). In the 1D1R crossbar array as shown in Fig. 3.12, R_2 contributed by all unselected cells at unselected word/bit lines in parallel is considerably larger than the sum of R_1 and R_3 because of the reverse biased diodes. Therefore, the resistance in the sneak current path can be approximated by $R_{LRS\_R}/(N\text{-}1)^2$, where R_{LRS_R} is the resistance of the standalone 1D1R cell in LRS dominated by the reverse biased diode at the negative read voltage $-V_{read}$, as shown in Fig. 3.12. R_{LRS_F} and R_{HRS_F} are also defined as the resistances of the standalone 1D1R cell in LRS and HRS, respectively, when read at V_{read}. When $R_{LRS\_R}/(N\text{-}1)^2$ decreases as N increases and eventually becomes comparable to R_{LRS_F} of the selected bit, the sneak current begins to interfere with the read process in the large 1D1R array. Thus, the ratio of R_{LRS_R} to R_{LRS_F} is a good measure of the maximum crossbar array size with a tolerable read margin. The readout voltage on the pull-up resistor R_{pu} can be calculated when $R_{selected} = R_{LRS\_F}$ and $R_{selected} = R_{HRS\_F}$, using an equivalent circuit method similar to that applied for a complementary resistive switch (CRS) crossbar array [39]. When R_1 and R_3 are omitted in Fig. 3.12, the readout voltage swing ΔV normalized to the pull-up voltage V_{pu} can be quantitatively estimated using the resistor

voltage divider equation as follows:

$$\frac{\Delta V}{V_{pu}} = \frac{R_{pu}}{[R_{LRS\_F} \parallel \frac{R_{HRS\_R}}{(N-1)^2}] + R_{pu}} - \frac{R_{pu}}{[R_{HRS\_R} \parallel \frac{R_{LRS\_R}}{(N-1)^2}] + R_{pu}} \quad (Eq.\ 3.1)$$

where R_{pu} is the resistance of the pulled-up resistor that is set to R_{LRS_F} for maximum read margin. For a 10% readout margin, Figure 3.13 shows that the maximum allowed word lines in a square crossbar array increased dramatically from 2 in a passive array to 750, i.e. equivalent to about 512 Kb, in a 1D1R array utilizing the parameters extracted from Fig. 3.9. The 1D1R array can be further scaled up to 1 G-bit with an improved R_{LRS_R}/R_{LRS_F} ratio of 10^9.

3.4 Summary

A rectifying Ti/TiO_2/Pt oxide diode and a unipolar RS Ni/HfO_2/Pt memory element have been fabricated on a flexible PI substrate with excellent characteristics using only room-temperature processes. No significant device degradation was found at bending states. Additionally, the impact of I_{RESET} on the programming margin of unipolar RS has been discussed. The heterogeneous TiO_2-HfO_2 1D1R cell not only demonstrates more stable unipolar RS compared to a monolithic TiO_2 1D1R cell because of the lower I_{RESET} in the HfO_2 memory element, but also effectively suppresses the sneak current. The maximum allowed array size with at least 10% read margin is predicted to exceed 512 Kb based on a simple equivalent circuit model. Therefore, the proposed 1D1R cell is extremely attractive for implementing high-density nonvolatile memory in future low-cost flexible electronics.

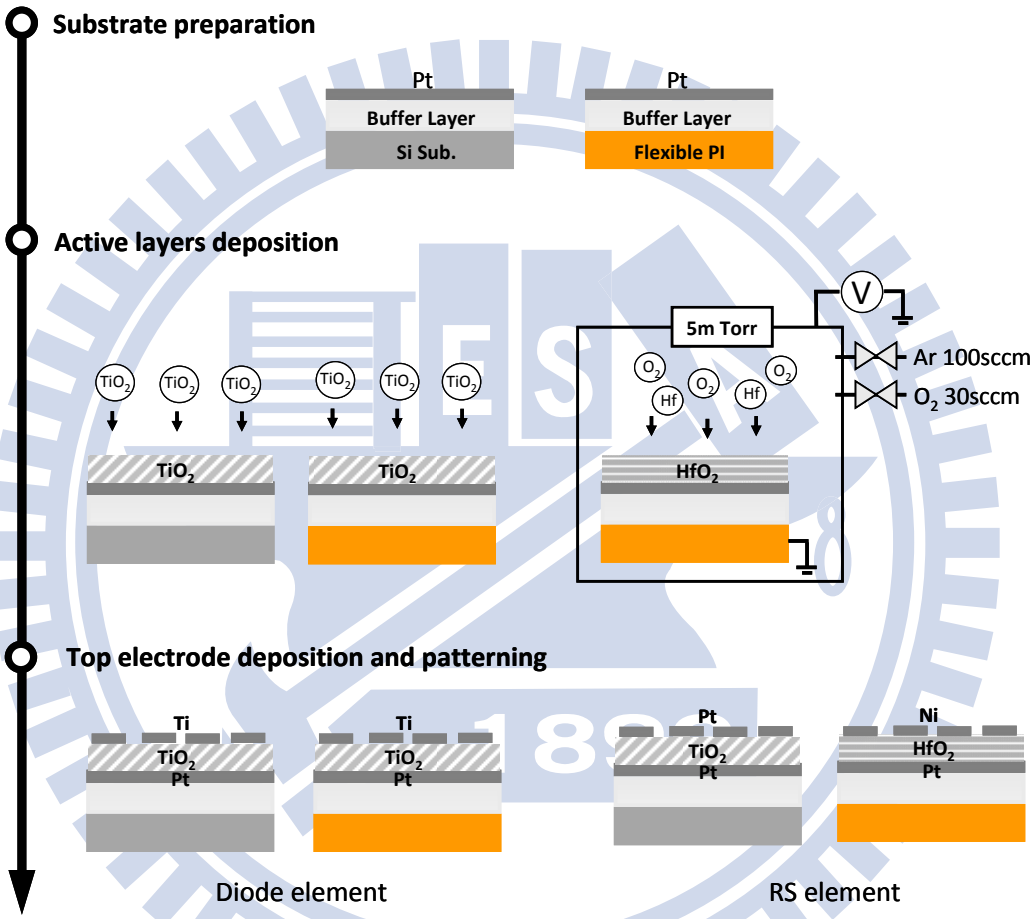

Fig. 3.1 Fabrication flow of $Ti/TiO_2/Pt$, $Pt/TiO_2/Pt$ and $Ni/HfO_2/Pt$ devices on PI and Si substrates.

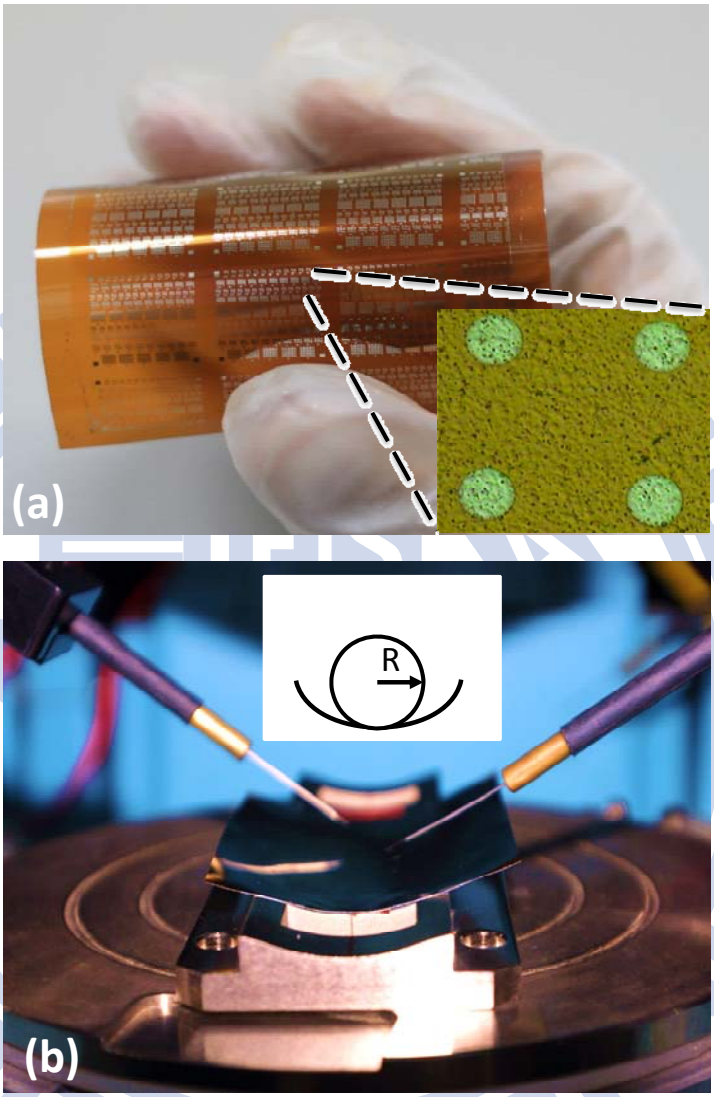

Fig. 3.2 (a) Photograph of a fabricated flexible device under bending. Insert shows the microscope image of patterned devices on the PI substrate. (b) Measurement setup using a concave stage with a radius of 30 mm to characterize devices at the bending state.

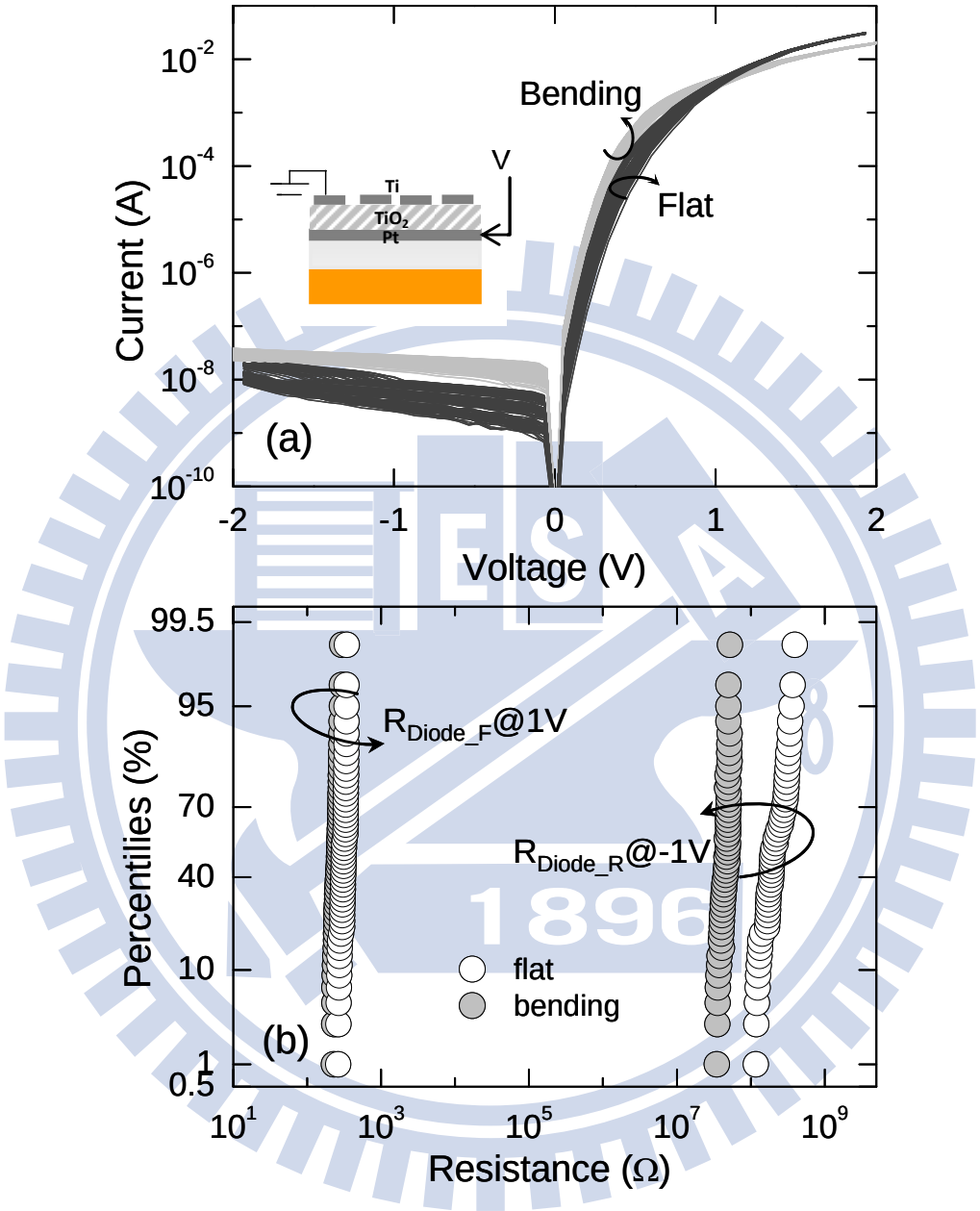

Fig. 3.3 (a) 100 successive cycling of ±2 V dc sweeps, and (b) cumulative plot of forward/reverse resistances at +1V/-1V of the flexible Ti/TiO_2/Pt diodes at both flat and bending states.

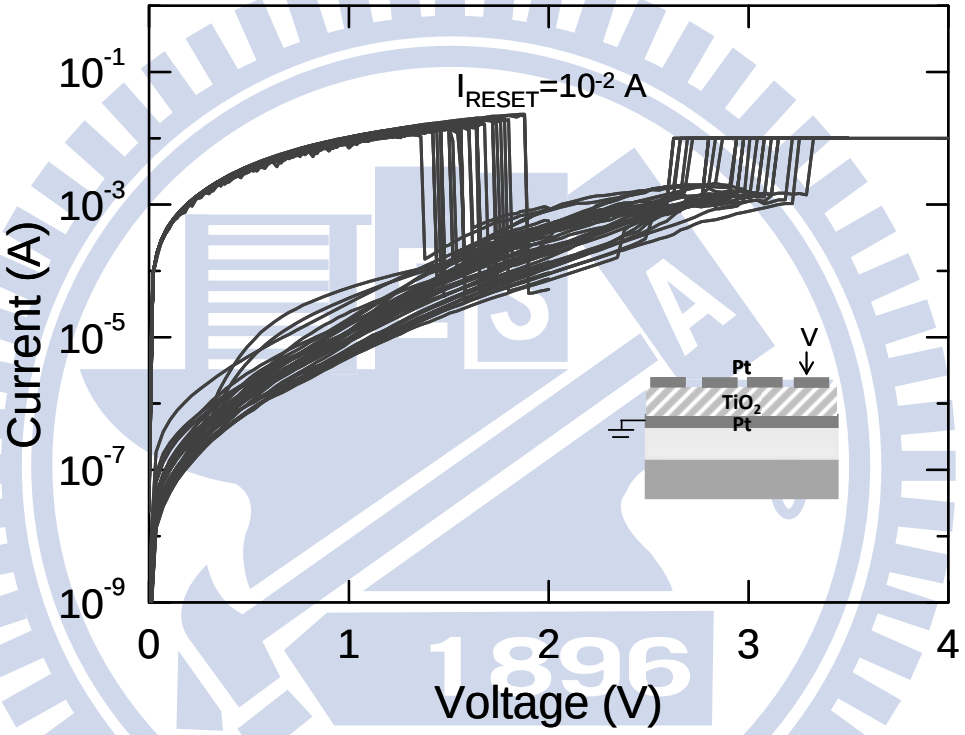

Fig. 3.4 Typical unipolar RS characteristics of the Pt/TiO_2/Pt memory element with I_{RESET} over 10 mA.

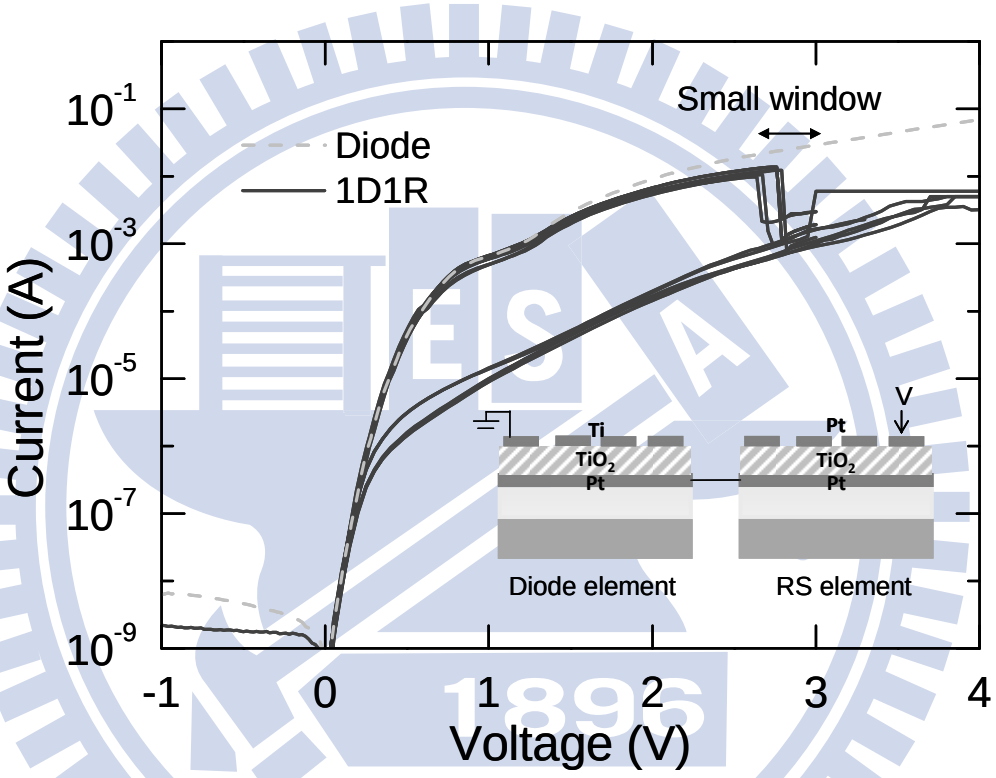

Fig. 3.5 Unstable unipolar RS in the monolithic TiO_2 1D1R cell because of the small programming margin.

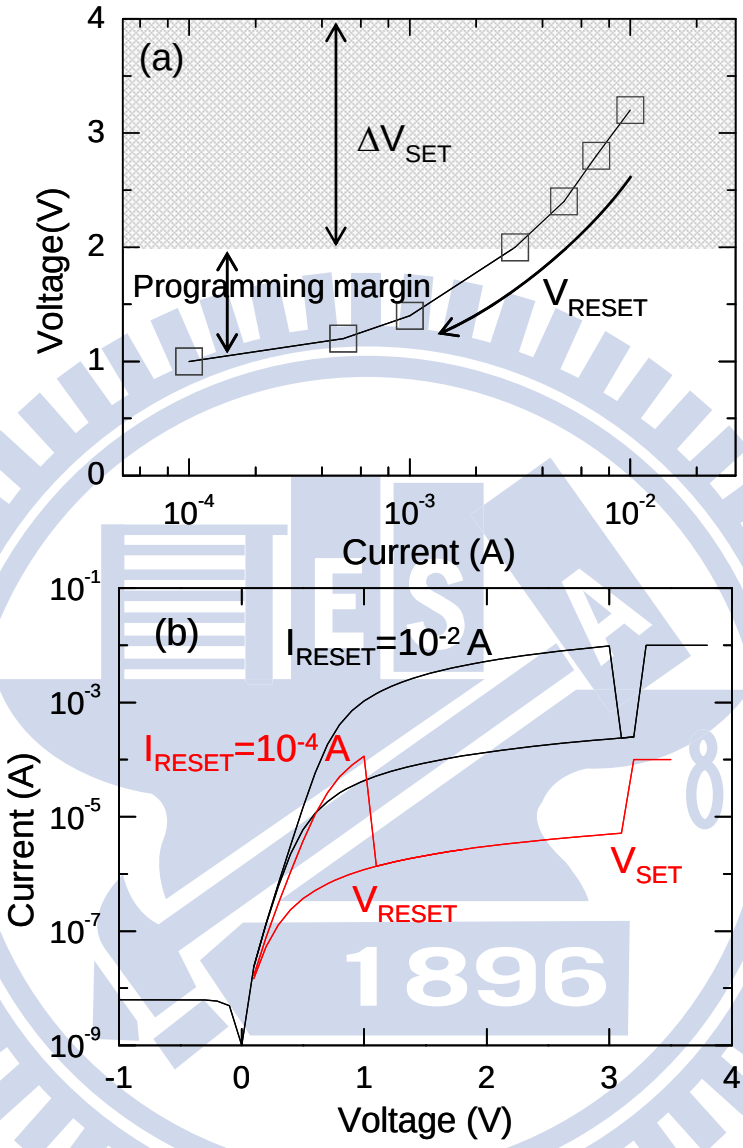

Fig. 3.6 (a) Programming margin of a 1D1R cell as a function of I_{RESET}. The diode on-current was fixed at 10 mA. A R_{HRS}/R_{LRS} ratio of 100, V_{RESET} of 0.5 V and V_{SET} between 2 to 4 V considering cycling variations were assumed for the RS element. (b) Simulated 1D1R unipolar switching curves for RS elements with I_{RESET} of 0.1 mA and 10 mA, respectively.

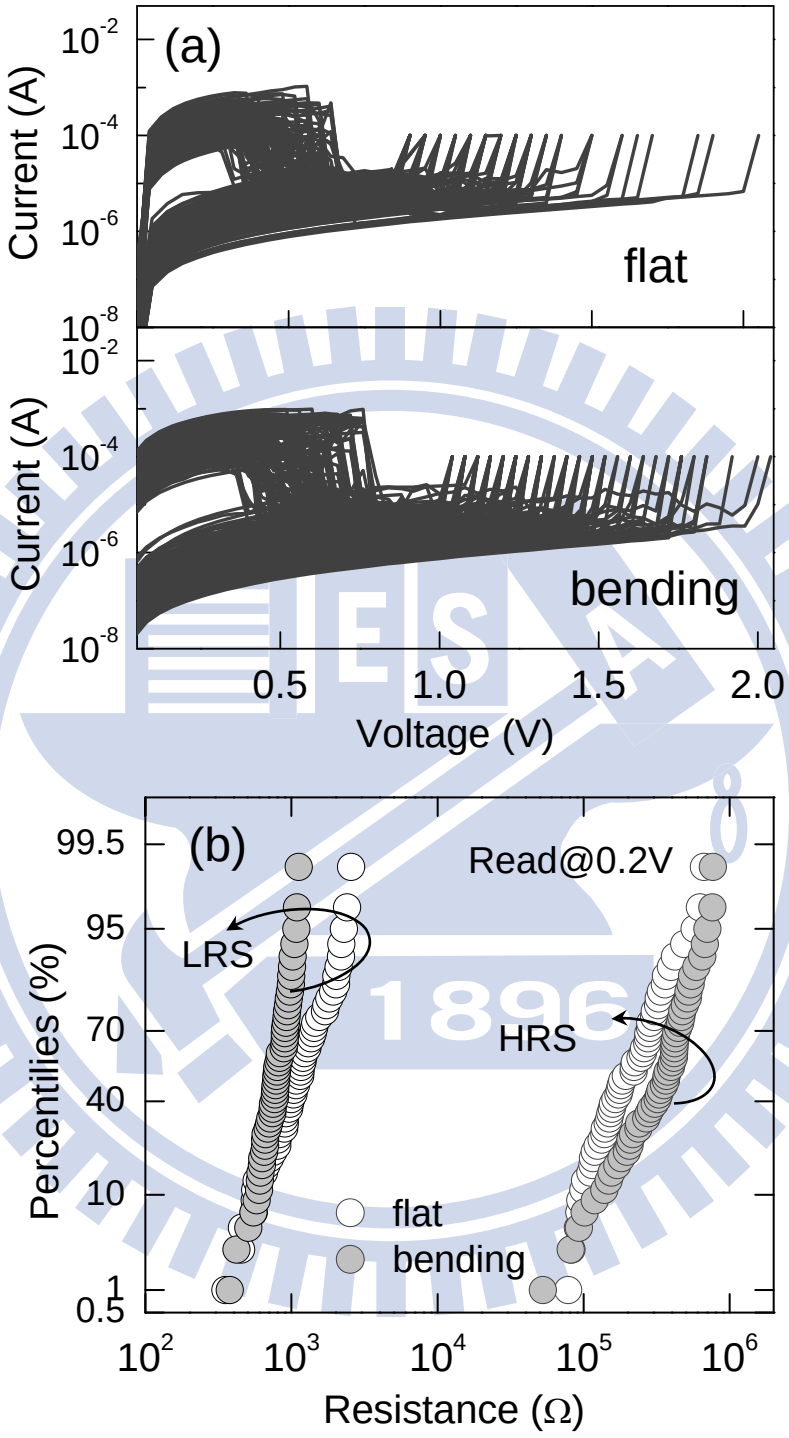

Fig. 3.7 (a) 100 successive unipolar RS cycles with I_{RESET} less than 1 mA, and (b) cumulative plot of HRS/LRS resistance at 0.2 V of the flexible Ni/HfO_2/Pt memory element at both flat and bending states.

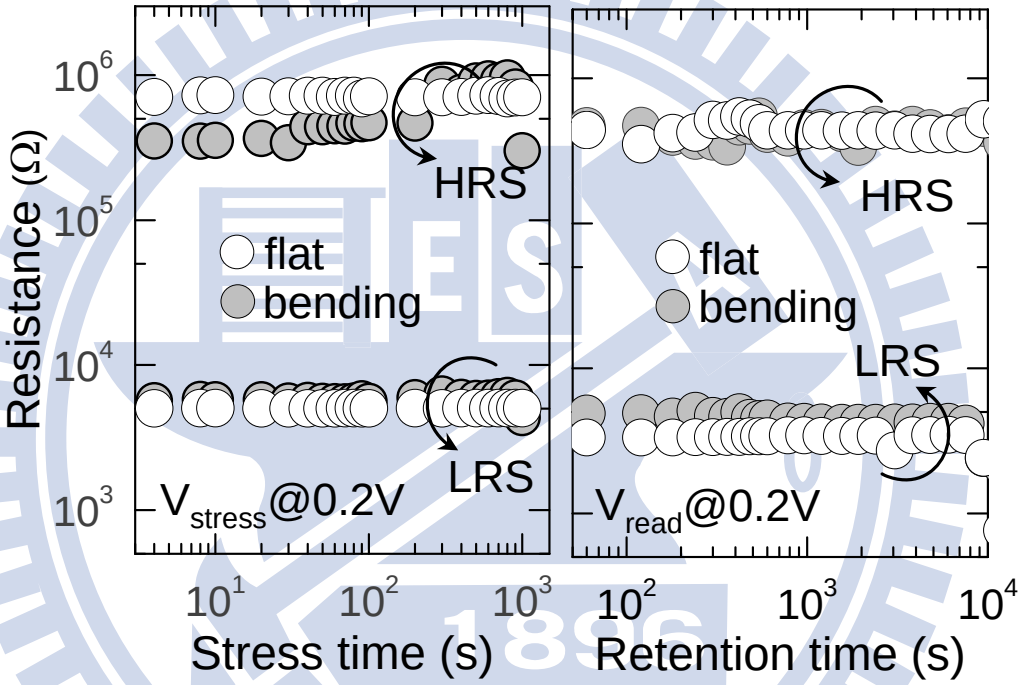

Fig. 3.8 Read disturb and retention characteristics of the flexible Ni/HfO_2/Pt memory element at both flat and bending states.

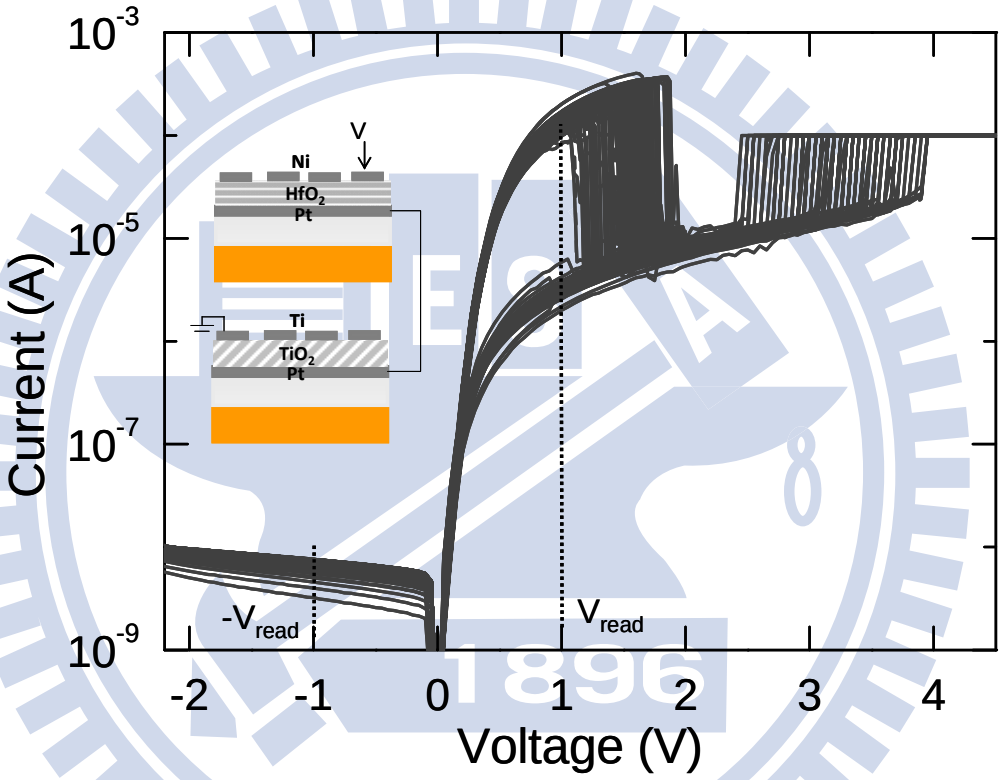

Fig. 3.9 More than 200 successive unipolar RS cycles with a high rectifying ratio at ±1 V in the heterogonous TiO_2-HfO_2 1D1R cell.

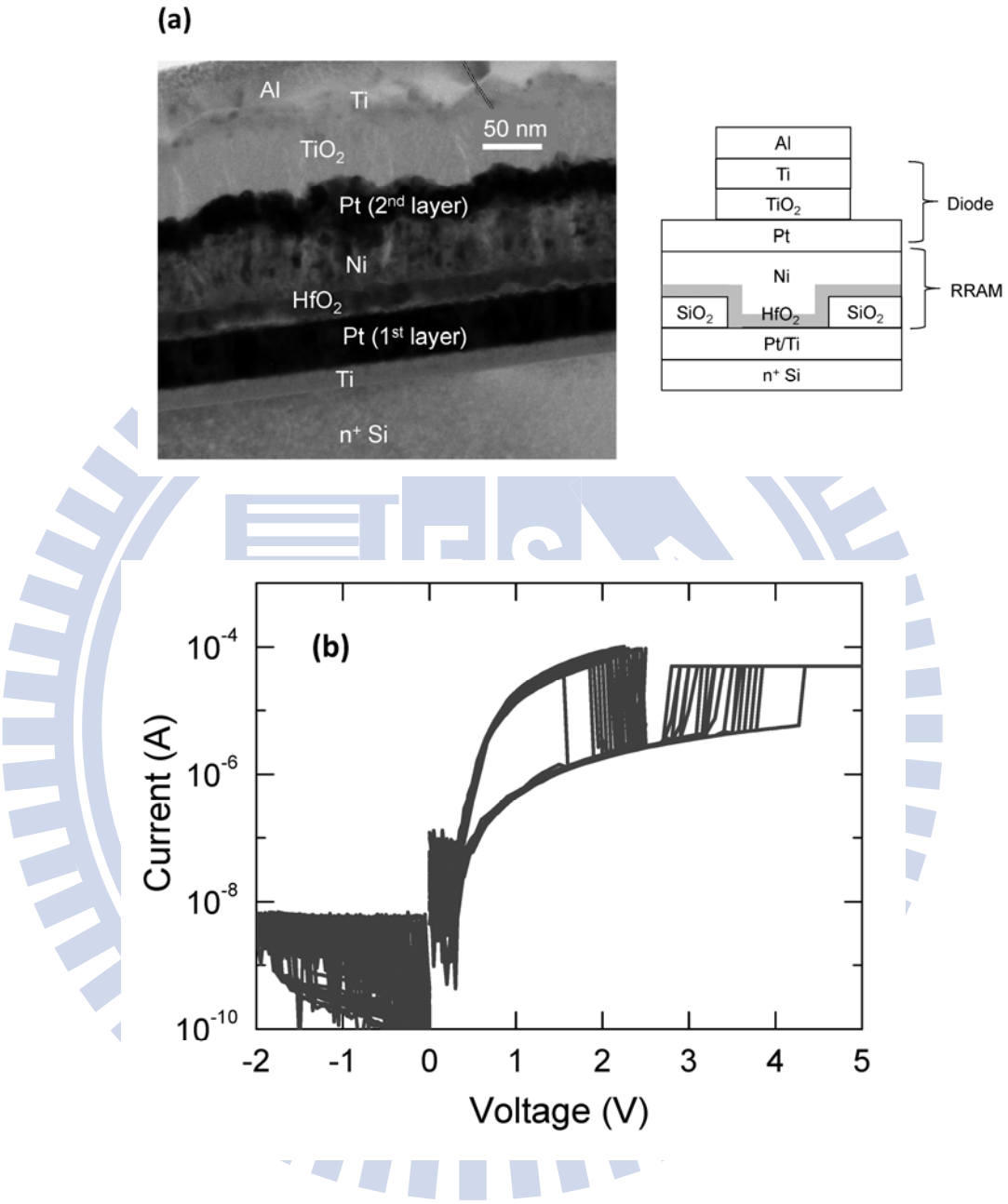

Fig. 3.10 (a) TEM image and schematic structure of a vertically stacked Ti/TiO_2/Pt/Ni/HfO_2/Pt 1D1R cell and (b) unipolar RS *I-V* with a high rectifying ratio of the vertically stacked 1D1R cell.

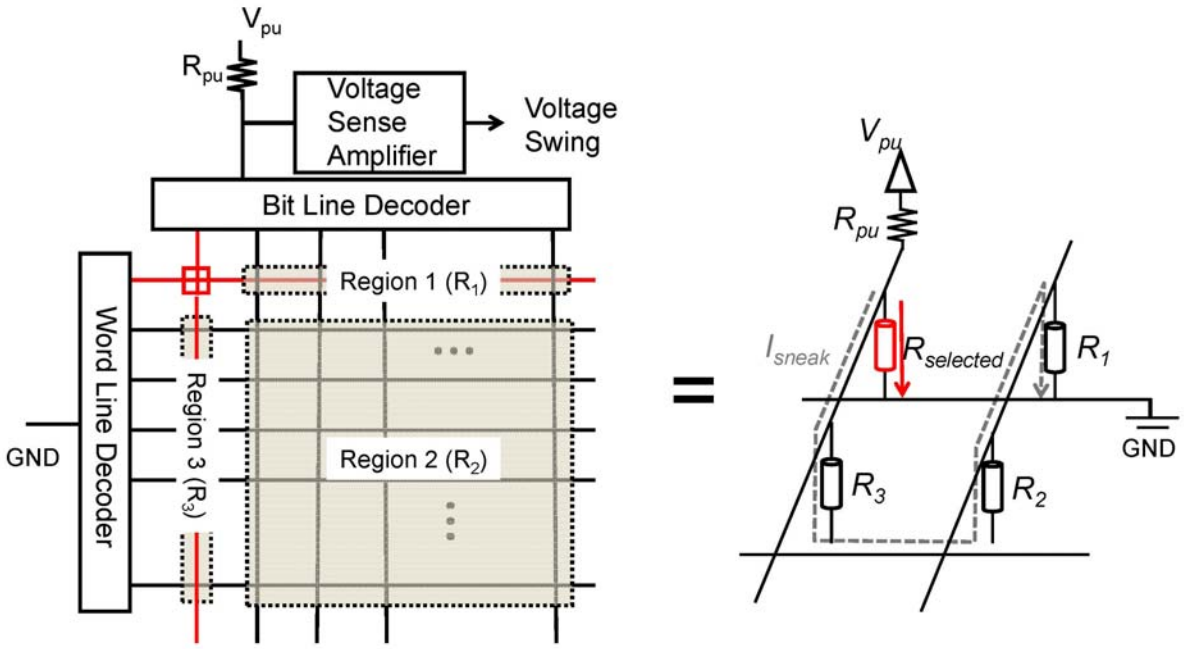

Fig. 3.11 Schematic of an $N \times N$ crossbar memory array and its equivalent circuit at the worse-case read scenario where all unselected cells are at LRS. The sneak current through R_1, R_2 and R_3 results in severe read interference.

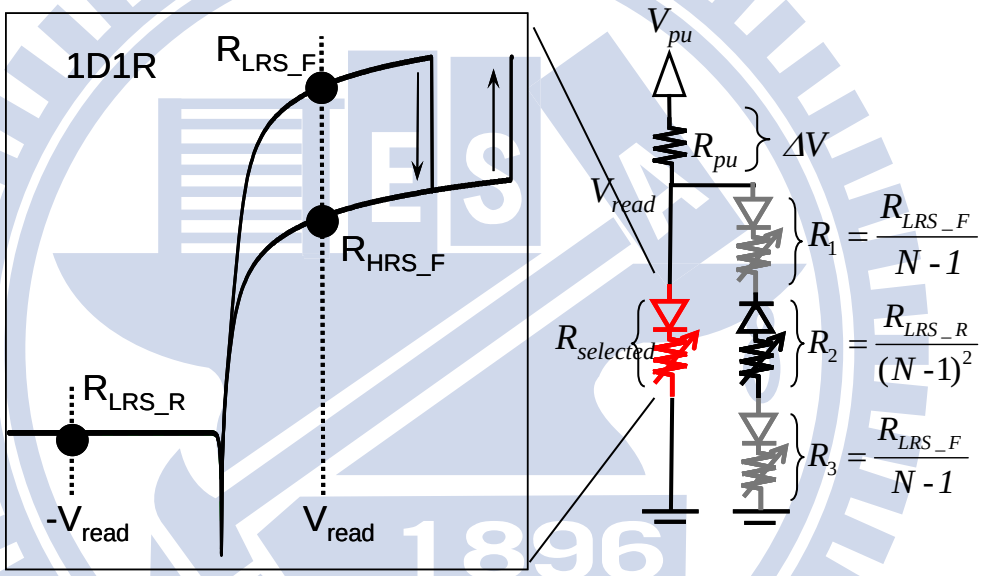

Fig. 3.12 Equivalent circuit of a 1D1R crossbar array at read. The total resistance of the sneak current path is dominant by R_2 because of the reverse-biased diodes.

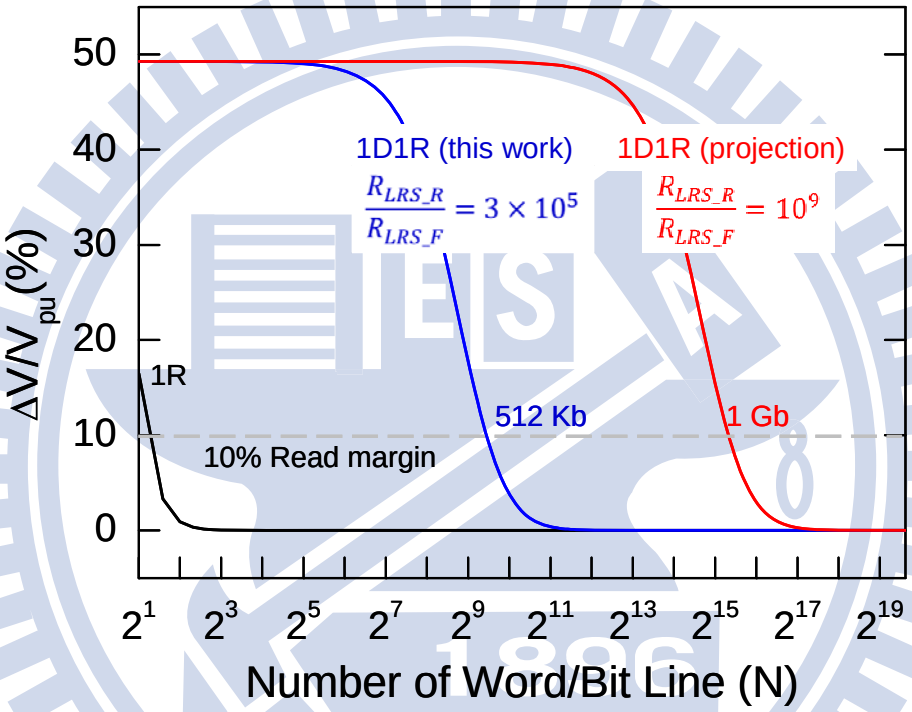

Fig. 3.13 Normalized readout margin $\Delta V/V_{pu}$ as a function of the number of word/bit line in an $N \times N$ crossbar array. The maximum allowed array size with at least 10 % readout margin can be dramatically increased in 1D1R arrays compared to 1R passive arrays.

Chapter 4

Bipolar Nonlinear Ni/TiO_2/Ni Selector for 1S1R Crossbar Array Applications

4.1 Introduction

Compatible with the $4F^2$ crossbar array, the stacking one diode-one resistor (1D1R) structure appears as one of the most attractive candidate. Their superior unipolar RS properties have been discussed in previous chapters. However, diodes with sufficient high forward current density and stable unipolar RS elements are still under investigation. Considering a bipolar RS element, a selection device should be able to exhibit a bidirectional current to allow the bipolar switching and nonlinear *I-V* characteristics to cut-off the sneak current. Although complementary resistive switching (CRS) using two bipolar RS elements connected in anti-series has been considered a soultion to reduce the sneak current [39, 41, 69], the inherent destructive read process imposes severe penalties on the design complexity, operational speed and power consumption. On the other hand, a cell structure, consisting of one bipolar nonlinear selector and one bipolar RS element (1S1R), can best utilize the stable bipolar RS properties while the read process is nondestructive [68]. However, the reported bipolar selector had limited nonlinearity only sufficient for a small array. Significant improvements on the selector characteristics are needed for the high-density 1S1R crossbar array. Moreover, the endurance of 1S1R cells has not yet been verified, but remains a great concern because the selector may suffer dielectric breakdown at high voltage [68].

In this chapter, we fabricated a Ni/TiO_2/Ni metal–insulator–metal (MIM) by a very simple low-temperature process. Excellent bipolar nonlinear characteristics, including current difference of 6 orders of magnitude for a voltage swing from 0 to ±2 V and

breakdown voltage larger than 4 V, are realized by Schottky emission over the Ni/TiO_2 barriers. By connecting the bipolar selector to a HfO_2 RS element in series, we report very reproducible bipolar RS with highly nonlinear *I-V* characteristics applicable for large megabit (Mb)-size crossbar arrays. In addition, the tradeoff between the maximum array size and the power consumption, which is important for the high-density array design, is also discussed.

4.2 Comparison of 1D1R and 1S1R Crossbar Arrays

For simplicity, the sneak current path at read and an equivalent circuit of a data pattern where all unselected bits were at low resistance state (LRS) are illustrated in Fig. 4.1(a). The simplified equivalent circuit of crossbar array using one bit-line pull-up (One-BLPU) read scheme [21, 46] is shown in Fig. 4.1(b). Note that the interconnect resistances of WLs/BLs are not included in our discussion. In order to ensure sufficient read margin in high-density arrays, a unipolar diode (or a bipolar selector) may be connected with a unipolar (or a bipolar) RS element in series to increase the nonlinearity of the LRS resistance, as shown in Fig. 4.2. The nonlinearity factor α was defined differently for 1D1R and 1S1R because approximately a full read voltage (V_{read}) would drop across the cells on unselected WLs/BLs subjected to a reverse bias (R_{II} in Fig. 4.2(a)) in 1D1R, while only $V_{read}/2$ would drop across the unselected cells on the selected WLs/BLs (R_I and R_{III} in Fig. 4.2(b)) in 1S1R. It can be shown that the maximum allowed number of word lines N in a square array scaled proportionally to $\alpha^{0.5}$ for 1D1R but to α for 1S1R in a first approximation. Figure 4.3 shows the calculated read margin using the equivalent circuits in Fig. 4.2. α of 10^6 and 10^9 were required for a megabit and a gigabit 1D1R array, respectively. The best 1D1R cell ever reported had α less than 10^5 [68]. In contrast, 1S1R deserves serious consideration in high-density crossbar arrays because of much relaxed requirement on α, 3×10^2 and 10^4, for a megabit and a gigabit array.

Furthermore, programming margin between set voltage (V_{SET}) and reset voltage (V_{RESET}) in 1S1R is inherently larger because of the bipolar RS nature, favorable for stable memory operations with minimal soft error.

4.3 Device Fabrication Process

To fabricate the Ni/TiO_2/Ni selector (S1), the TiO_2 films of 15 nm were deposited on Ni/SiO_2/Si substrates by reactive sputtering at 200 ^oC using a Ti target (99.5%) in a mixture of Ar and O_2. Ni top electrodes were then deposited by sputtering and patterned by standard lithography process with cell size from 0.36 μm^2 to 10^4 μm^2. As for the RS element, Ni/HfO_2/Pt structures were deposited on a Ti/SiO_2/Si substrate by sputtering at room temperature. After initial forming, reproducible bipolar RS with RESET current of 100 μA [see R1 in Fig. 4.4(a)] to 1 mA [see R2 in Fig. 4.4(a)] was obtained by adjusting the compliance current at SET. The RS in Ni/HfO_2/Pt was attributed to the electromigration of Ni from the top electrode, which is similar to what we have discussed in the Ni/HfO_2/Si structures [71]. The series 1S1R measurements were carried out by connecting the Ni/TiO_2/Ni and Ni/HfO_2/Pt devices externally, where the voltage was applied on the Ni top electrode of the Ni/TiO_2/Ni device, and the Pt bottom electrode of the Ni/HfO_2/Pt device was grounded.

4.4 Results and Discussion

4.4.1 *I–V* characteristics of bipolar Ni/TiO_2/Ni selector

Figure 4.4(a) illustrates the current–voltage (*I–V*) characteristics of the Ni/TiO_2/Ni MIM selector with an exponential current increase over six orders of magnitude for a voltage swing from 0 to ±2 V. No dielectric breakdown occurred within ±4 V. The TEM images of Ni/TiO_2/Ni structure and the Ni/TiO_2 interfaces are illustrated in Figs. 4.4(b) and 4.4(c),

respectively. The nonlinearity in *I–V* with direct-current cycling up to 1000 times neither degraded nor reduced were observed as we show in Fig. 4.5(a), implying the stable operation property of bipolar selector. Figure 4.5(b) shows Schottky emission fitting of log (*I*) versus $V^{1/2}$. The observed highly nonlinear *I–V* curves were mainly dominated by the Schottky emission over the Ni/TiO_2 barriers at low voltage, whereas an additional current component, which is likely related to other defect assisted transport mechanisms, led to the slight current increase at high negative bias. Note that the maximum current was eventually limited by a parasitic series resistance estimated about 50 Ω. Figure 4.5 (c) exhibits the field-dependent Schottky barrier height Φ_b extracted from temperature-dependent fitting of log (I/T^2) versus $1/T$ measured from 25 to 125 °C at low voltage regime. The Φ_b of both the top and bottom Ni/TiO_2 interfaces were extrapolated to be 0.58 eV at 0 V. The value was between that of Ti/TiO_2 (0.13 eV) and that of Pt/TiO_2 (0.85 eV) and desirable for high nonlinearity within the interesting range of voltage swing. The strong dependence on the electrode materials further supported that the Schottky emission instead of the Poole–Frenkel emission assisted by TiO_2 bulk traps was mainly responsible for current conduction. Figure 4.6 further shows the *I-V* characteristics of Ni/TiO_2/Ni bipolar selectors with various device areas fabricated by conventional lithography. Current density more than 10^5 A/cm^2 with device area scaling down to 0.36 μm^2 can be achieved, indicating the applicability of driving a sub-20 nm bipolar RRAM with RESET current (I_{RESET}) below sub-μA [24].

4.4.2 Bipolar 1S1R resistive switching

Figure 4.7(a) shows the *I–V* characteristics of S1 in series with R1, where more than 200 successive bipolar switching cycles were plotted. The *I–V* characteristics were determined by the superposition of S1 and R1, dominated by S1 and R1 at low and high voltage regimes, respectively. As a result, the resistance was highly nonlinear and bias dependent. The wide separation of SET and RESET voltages at opposite polarities ensured

reliable programming, in contrast to the smaller separation at the same polarity for the unipolar RS. Moreover, very tight distribution of SET/RESET voltages and SET-state/RESET-state resistance was clearly observed. The SET and RESET voltages in the 1S1R device were higher, as compared to those of the single R1 due to the additional voltage drop on S1. Figure 4.7(b) shows excellent immunity to read disturb at +2 V and −2 V for the high- and low-resistance states, respectively. To read the 1S1R crossbar array, a full read voltage V_{read} was applied to read the selected cell, while only half of V_{read} drop on the unselected cells. As apparent in Fig. 4.7(a), for a V_{read} of 4V, sneak current at 1/2 V_{read}, i.e. 2V, was low enough to prevent read disturb.

4.4.3 Read margin analysis

To read from the 1S1R array, one read scheme, One-BLPU was considered [21, 46]. Only one bit line was pulled up, and all other bit lines were floating when each word line was selected. Thus, a specific data pattern was assumed, where all unselected cells were simultaneously at the low-resistance state with resistance of R_{LRS} or high-resistance state with resistance of R_{HRS}. The simplified equivalent circuit of a square $N \times N$ 1S1R array with negligible line resistances is depicted in Fig. 4.1(b). R_I, R_{II} and R_{III} are the equivalent resistance of region I, II and III in Fig. 4.1(a), respectively. The voltage on the pull-up resistor (R_{pu}) connected to the selected bit line was evaluated to measure voltage swing (ΔV_{pu}) when reading the selected cell ($R_{selected}$). For a large array, the read voltage (V_{read}) along the sneak current path across the parallel resistor network of the unselected WLs/BLs (R_{II}=R_{LRS}/$(N-1)^2$) in Fig. 4.2(b)] can be analytically ignored and was shared by the R_I and R_{II}. In other words, only half of the voltage (V_{read}/2) would drop on R_I and R_{II}, respectively. To a first approximation, $2R_{LRS}/(N-1)$ at $V_{read}/2$ through the sneak path should not be less than R_{LRS} at V_{cell} to ensure a sufficient read margin between the high- and low-resistance states of the selected cell. In other words, the nonlinearity factor α of the low-resistance state in 1S1R

cells, i.e., the ratio of R_{LRS} at $V_{read}/2$ to R_{LRS} at V_{read}, was the primary factor of determining the maximum array size instead of the resistance ratio between the high/low-resistance states (R_{HRS}/R_{LRS}), which plays an important role in the optimization of the passive crossbar array [21]. A more quantitative assessment on the read margin ΔV normalized to the pull-up voltage V_{pu} can be calculated by solving the Kirchhoff equation

$$\frac{\Delta V}{V_{pu}} = \frac{R_{pu}}{[R_{LRS}(V_{cell}) \parallel \frac{2R_{HRS}(\frac{V_{cell}}{2})}{N-1}] + R_{pu}} - \frac{R_{pu}}{[R_{HRS}(V_{cell}) \parallel \frac{2R_{LRS}(\frac{V_{cell}}{2})}{N-1}] + R_{pu}} \quad (Eq.\ 4.1)$$

where R_{pu} is the resistance of the pulled-up resistor, set to R_{LRS} at V_{read} for maximum read margin [21]. We used a sensing criterion of a minimal 10 $\%\Delta V/V_{pu}$ to determine the maximum crossbar array size [39]. The calculated maximum array size with at least 10% read margin increased from N = 5 (R1 only) to N = 501 (S1 + R1), as shown in Fig. 4.7, where V_{read} of 2 V was chosen not only to maximize α but also to guarantee a sufficient margin of the read disturb. The superposed nature of 1S1R provided additional freedom in engineering nonlinearity by tuning the resistance of the RS element. That means that we can independently modulate the current-voltage behaviors of LRS at high/low voltage regions to get the benefit of nonlinearity. On the other hand, R1 can be replaced by R2 with lower R_{LRS} to further improve α. The maximum array size can be further scaled up to N > 3k with V_{read} of 2.5 V or nearly 10 Mb, among the largest of all existing projections on the bipolar crossbar array based on the xperimental results [41, 68]. However, this also unavoidably increased the RESET power mainly due to the larger RESET current. The RESET voltage also increased from 3.7 to 4.6 V. Therefore, design optimization in choosing the appropriate RS element is required to tradeoff array size, operational voltages, and power for a given nonlinear selector. Finally, Table I summarizes the extracted parameters and the calculated maximum array size from the 1S1R cells measured in this study.

4.5 Summary

A Ni/TiO_2/Ni MIM with highly nonlinear *I-V* characteristics has been proposed as the bipolar selector for high-density 1S1R crossbar arrays. The nonlinearity is attributed to the Schottky barriers at the Ni/TiO_2 interface. The selector in series with an HfO_2 RS element exhibits robust and stable bipolar RS, and can effectively suppress the sneak current to allow large Mb-size array implementation. The results demonstrate the significant potential of 1S1R crossbar array architectures for the future high-density memories and reconfigurable logic circuits.

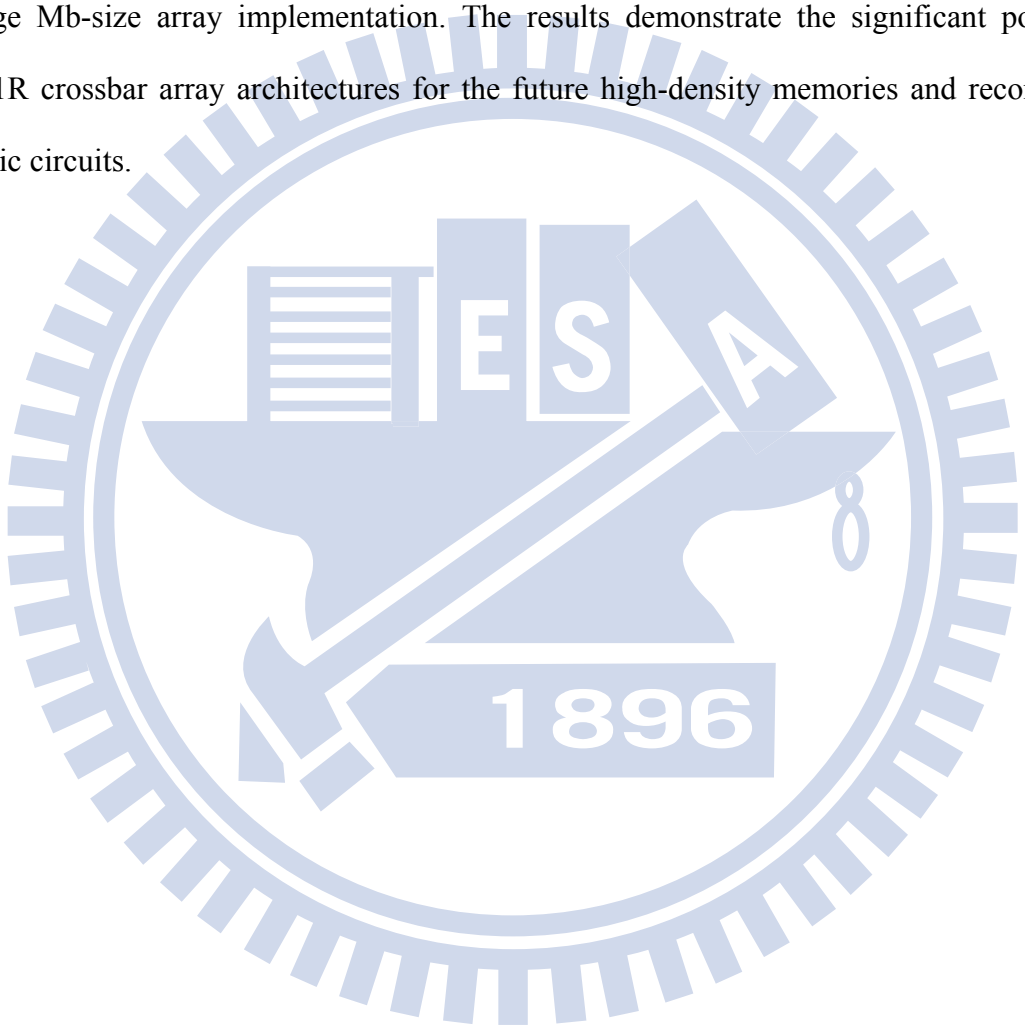

Table 4.1 Extracted parameters from the 1S1R cells measured in this chapter.

	V_{cell} (V)	$\frac{R_{HRS}(V_{cell})}{R_{LRS}(V_{cell})}$	$\frac{R_{LRS}(\frac{V_{cell}}{2})}{R_{LRS}(V_{cell})}$	P_{RESET} (mW)	N@10% $\Delta V / V_{pu}$
R1	2 or 2.5	220	1	0.16	5
S1+R1	2	68	155	0.37	501
S1+R2	2.5	65	980	4.57	3162

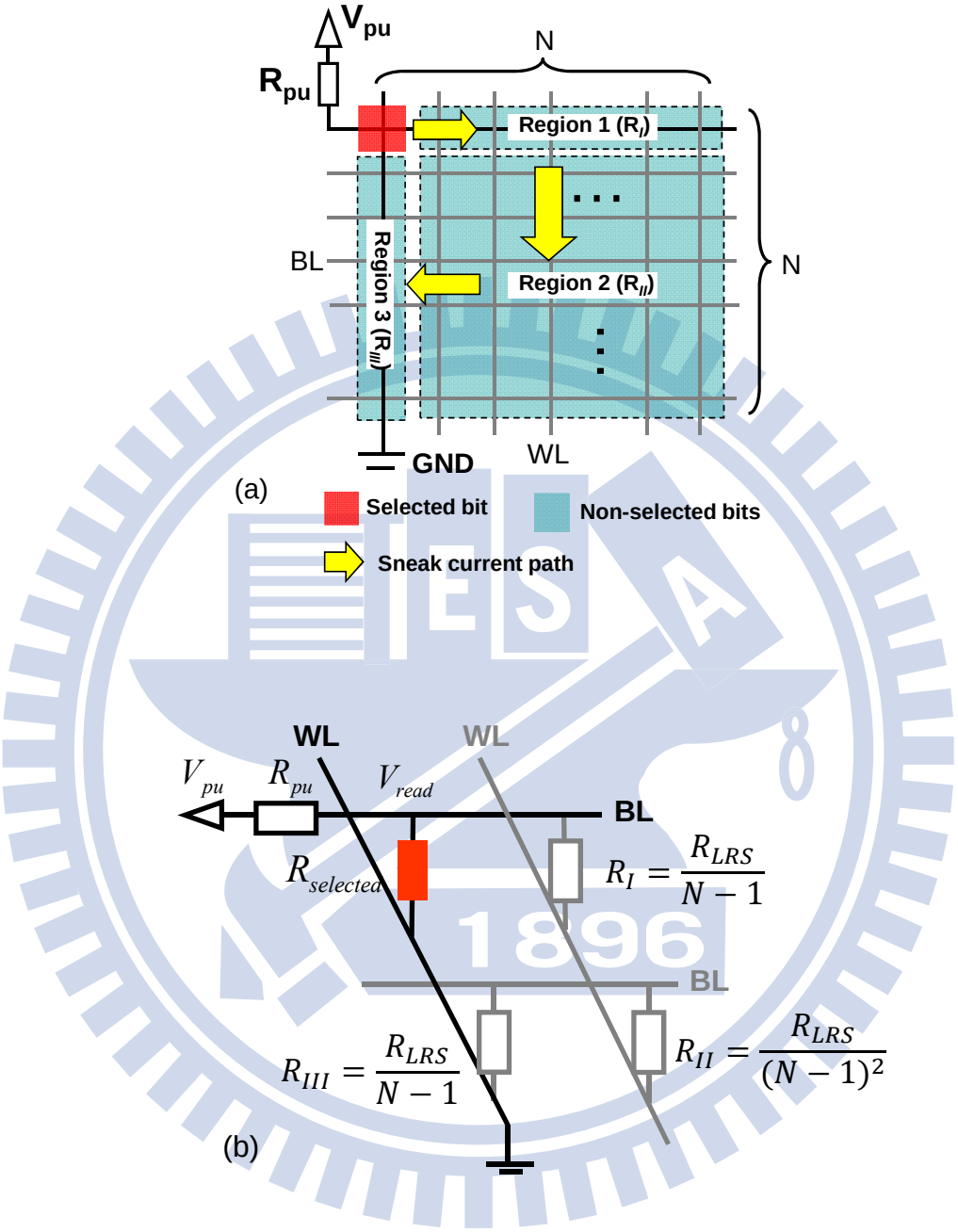

Fig. 4.1 Sneak current path at read in a square crossbar array where all bits except the selected one are at LRS, and (b) the equivalent circuit can be represented by R_{I}, R_{II}, and R_{III} of parallel resistor networks in region 1 (bits on selected BL), region 2 (bits on unselected WL and BL), and region 3 (bits on selected WL).

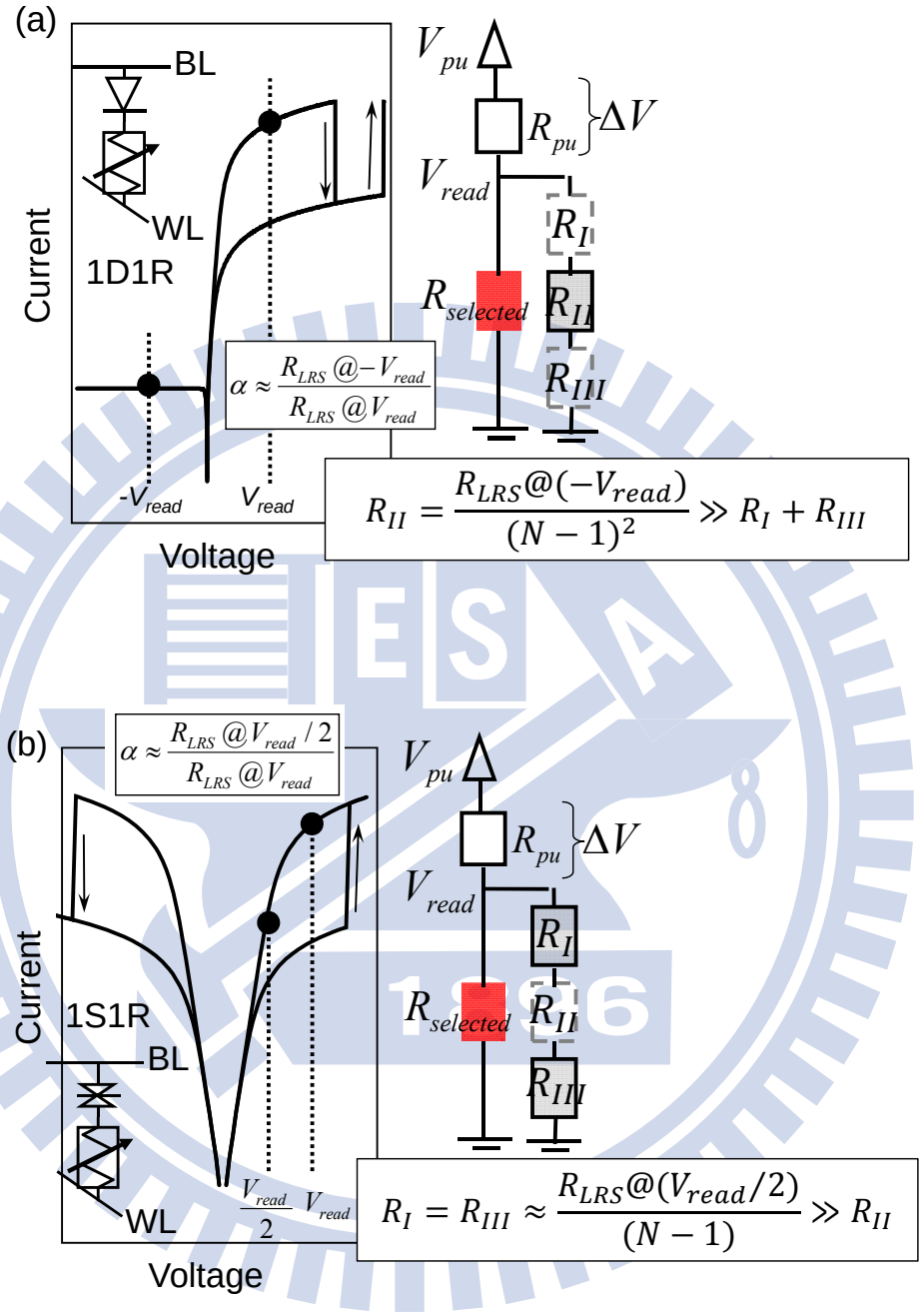

Fig. 4.2 RS *I-V* curves for (a) 1D1R and (b) 1S1R RRAM cells, and their nonlinearity factor α and equivalent circuits in a crossbar array. R_{II} subjected to a reverse bias is much larger than R_I and R_{III} in 1D1R, while R_{II} scaled with $(N\text{-}1)^2$ is much smaller than R_I and R_{III} scaled with $(N\text{-}1)$ in 1S1R.

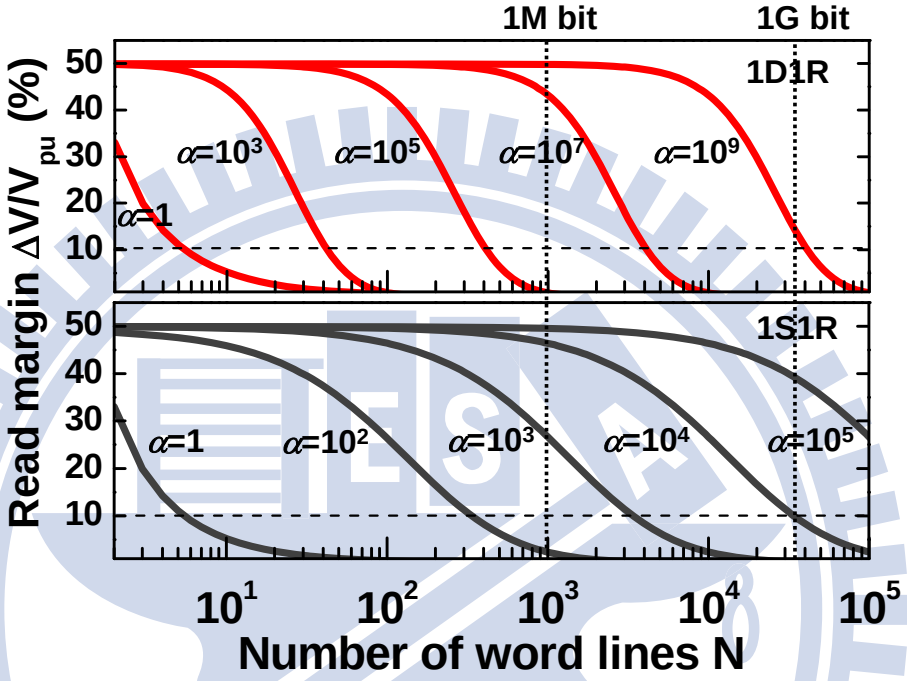

Fig. 4.3 Calculated read margin as a function of α for both 1D1R and 1S1R using the equivalent circuits in Fig. 4.1 and $R_{HRS}/R_{LRS} = 10^3$.

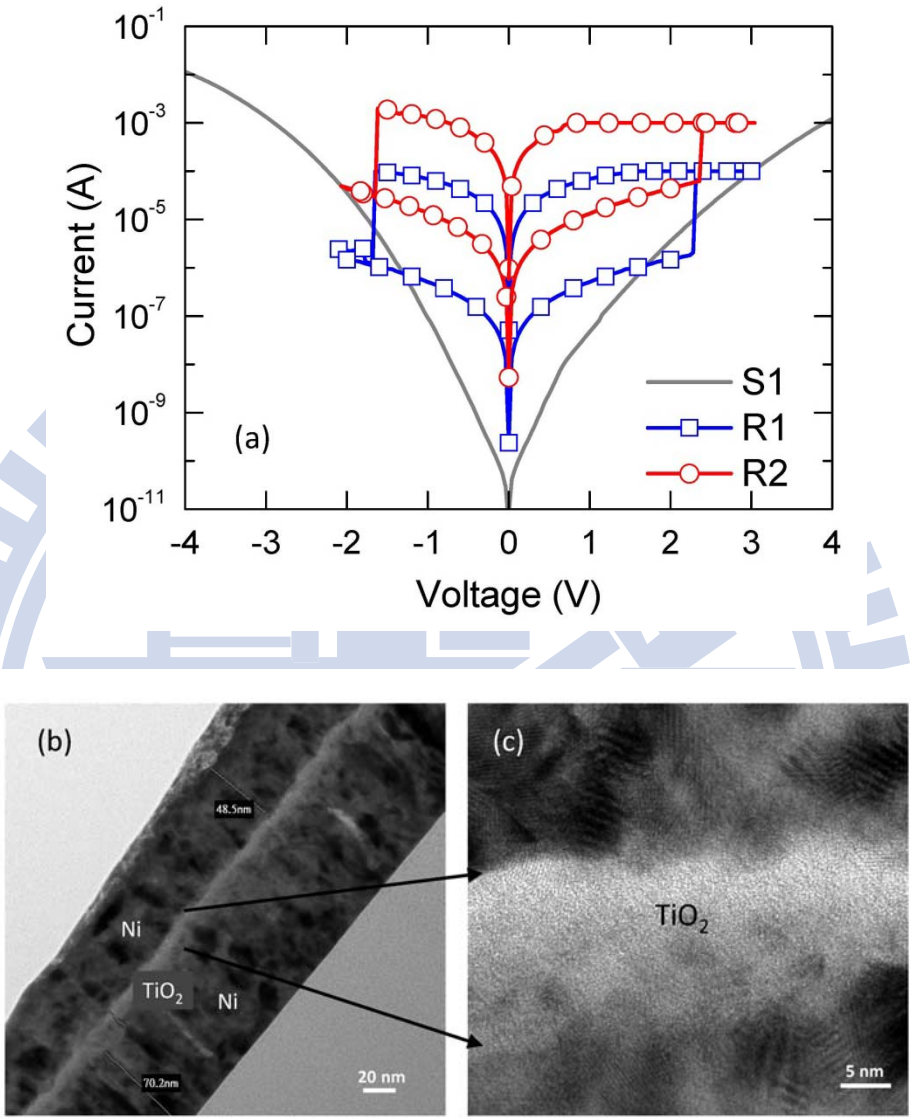

Fig. 4.4 (a) *I–V* characteristics of the bipolar Ni/TiO_2/Ni MIM selector (S1) and bipolar Ni/HfO_2/Pt RS elements (R1 and R2). (b)(c) TEM cross-section images of the Ni/TiO_2/Ni selector.

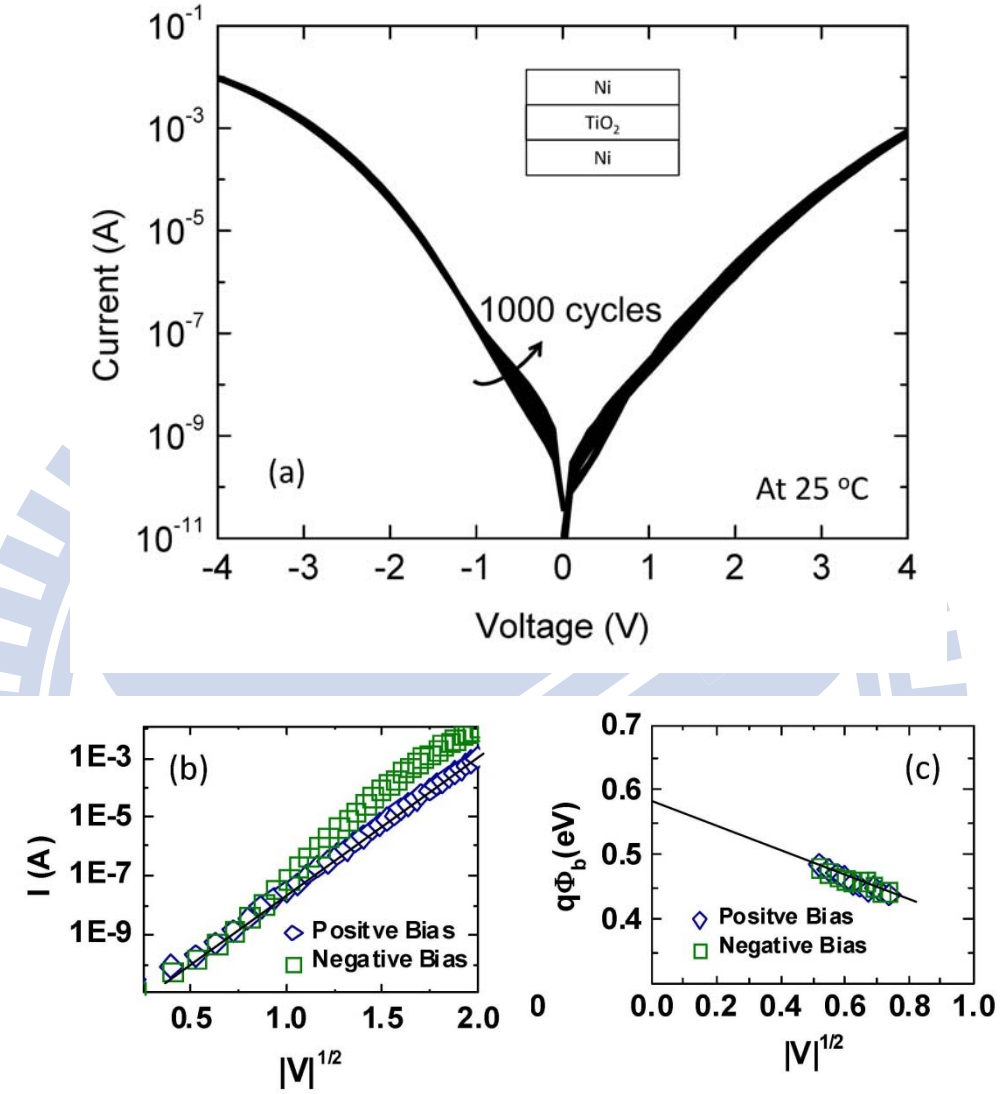

Fig. 4.5 (a) Endurance *I-V* of Ni/TiO_2/Ni selector over 1000 cycles. (b) Schottky emission fitting of log (*I*) versus $V^{1/2}$ at both voltage polarities of S1. (c) Extracted Schottky barrier height Φ_b by temperature-dependent fitting from the low voltage regime of S1.

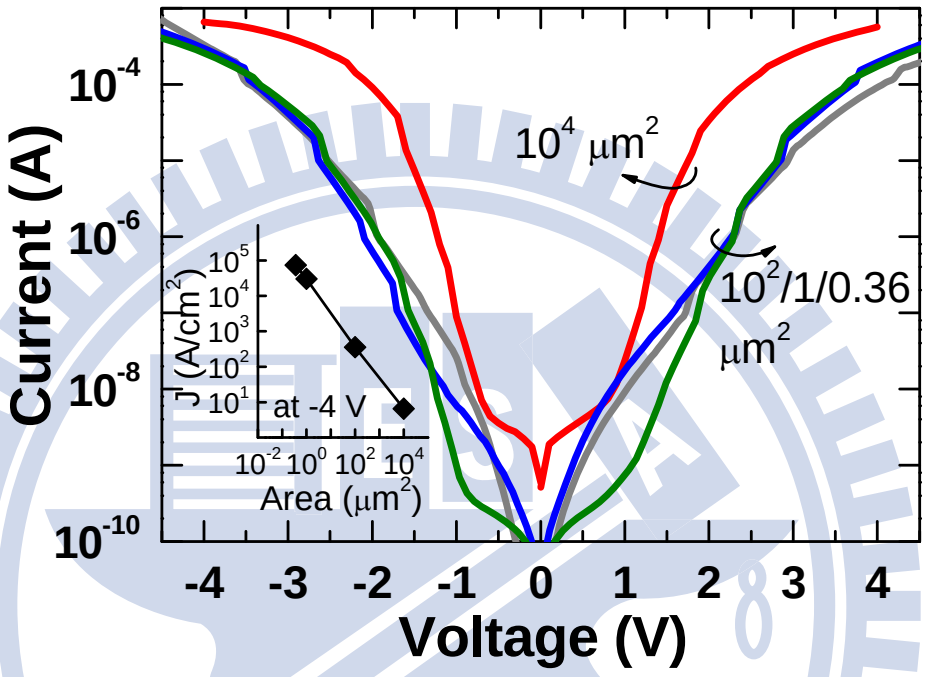

Fig. 4.6 *I-V* characteristics of Ni/TiO_2/Ni bipolar selectors with various device areas fabricated by conventional lithography on Si substrates. Insert shows that current density higher than 10^5 A/cm^2 with device area scaling down to 0.36 μm^2 can be achieved.

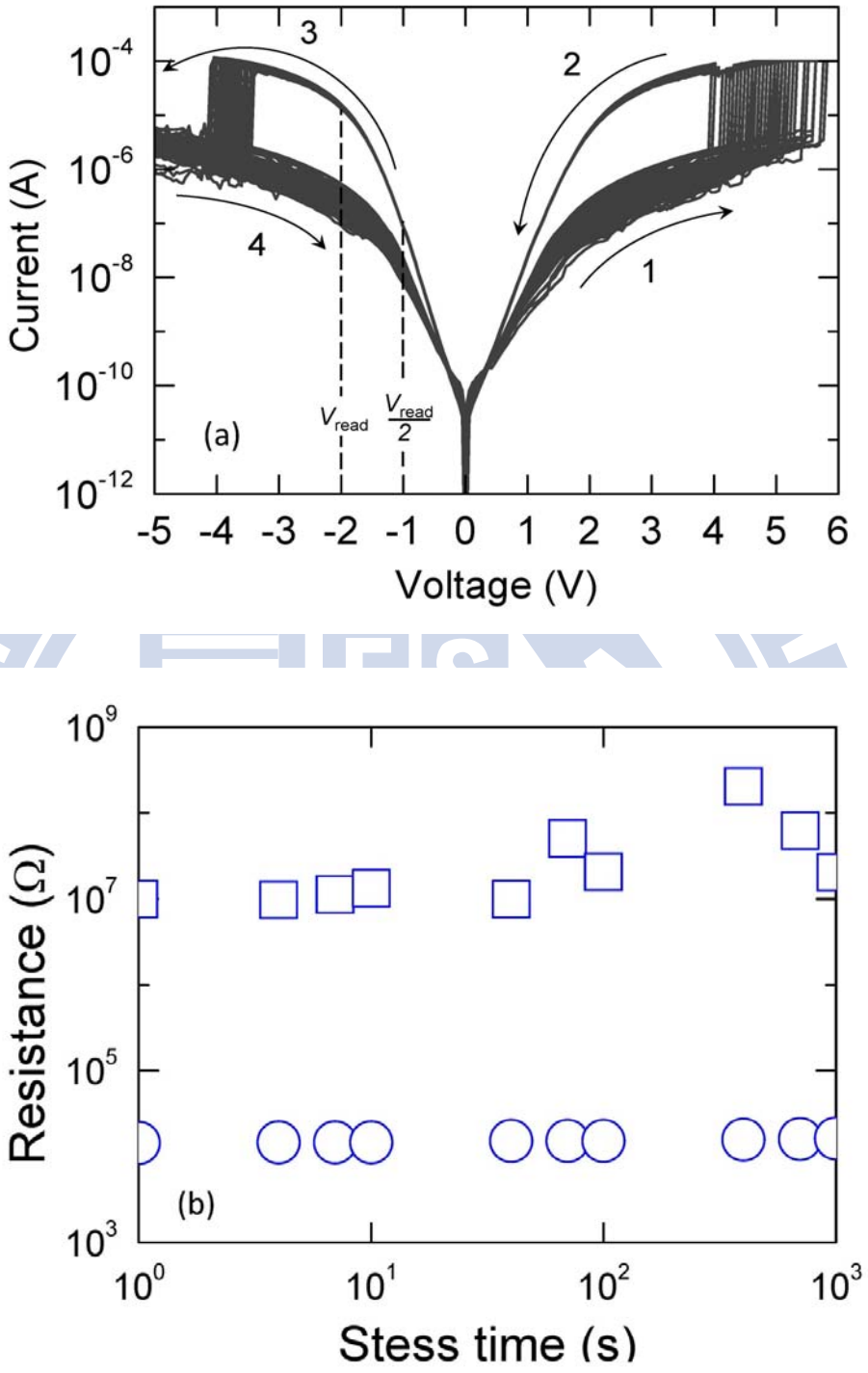

Fig. 4.7 (a) More than 200 successive bipolar switching cycles of S1 and R1 connected in series with 100 μA compliance current and (b) read disturb for the HRS stressed at +2 V and the LRS stressed at − 2 V.

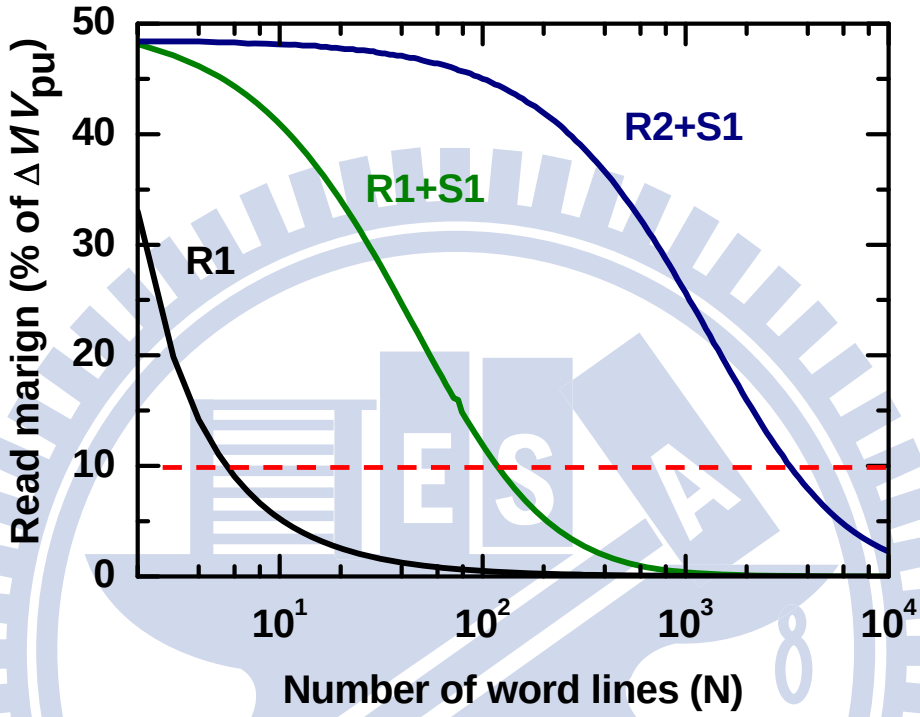

Fig. 4.8 Read margin $\Delta V/V_{pu}$ as a function of N in various crossbar configurations calculated from (*Eq*. 4.1) based on the equivalent circuit shown in Fig. 4.2(b).

Chapter 5

1S1R Crossbar Array for Low-cost Flexible Electronic Applications

5.1 Introduction

Low-cost flexible electronics on plastic substrates are excellent complements to present Silicon electronics built by costly fabrication technology on rigid substrates in multi-billion-dollar fabs [72]. Their success depends strongly on the development of novel devices fabricated at a very low temperature process. In Chapter 3, unipolar 1D1R cells, consisting of a Ti/TiO_2/Pt diode and Ni/HfO_2/Pt RS memory elements have been proposed and examined on plastic substrates for flexible nonvolatile memory applications [73]. In contrast to unipolar RS, bipolar RS due to its inherently distinguishable programming margin should be greatly emphasized. In Chapter 4, we have proposed a Ni/TiO_2/Ni structure with highly nonlinear *I*-*V* characteristics and demonstrated the meaningful potential of effectively suppressing the sneak current to build large array size. Additionally, the combined bipolar Ni/TiO_2/Ni selector and Ni/HfO_2/Pt RS element displayed a robust and stable 1S1R bipolar RS on Si substrates [70]. Because those devices are low-temperature process available, it is of great interest to evaluate their novel applications not only on rigid substrates but also on plastics substrates. However, previous studies were limited to only one component, and their integration on high-density crossbar arrays had never been realized [68, 70], even though 1S1R exploits more favorable bipolar switching. On the other hand, although solution-based process, such as sol-gel coating, has advantages of low cost and simple processing to achieve low-temperature fabrication, an additional annealing process is required for densified films and additionally, cell-to-cell uniformity has not yet been confirmed [47].

In this chapter, we use a low-temperature and simple sputtering process to fabricate a high-performance Ni/TiO_2/Ni bipolar selector and a reproducible RS Ni/HfO_2/Pt memory element on plastic substrates. Furthermore, by a simple 5-mask process, we report for the first time a vertically stacked Ni/TiO_2/Ni/HfO_2/Pt 8×8 1S1R array completely fabricated at room temperature, nevertheless showing promise of realizing unprecedented G-bit NVM in extremely low-cost flexible electronics.

5.2 Experimental Procedure

Prior to the device fabrication, 75-μm-thick Kapton® polyimide (PI) substrates were cut and ultrasonically cleaned in acetone for 10 min to remove particles and contamination, followed by a 100°C baking for 30 min. The cleaned PI substrates were then electrostatically attached to silicon wafers. Then, a buffer layer of SiO_2 with a thickness of 300 nm was deposited on PI substrates by plasma-enhanced chemical vapor deposition (PECVD). To fabricate the 1S1R crossbar array, a Ni/TiO_2/Ni/HfO_2/Pt 8×8 crossbar array was fabricated by reactive sputtering system using a 5-mask shadow-mask process on a flexible polyimide substrate. As illustrated in Fig. 5.1, mask 1 was used to define Pt/Ti bottom electrodes with width of 220 μm. HfO_2 switching layer were then deposited through mask 2, followed by Ni top electrodes of memory elements (or bottom electrodes of selector elements) deposition through mask 3, where electrical properties of the single element could be separately measured through the metal contact by mask 3. Next, TiO_2 active layer and Ni top electrodes of selector elements were defined sequentially by mask 4 and mask 5.

Among which, the active layers, HfO_2 with thickness of 80 nm and TiO_2 with thickness of 60 nm were prepared by dc magnetron reactive sputtering using Hf target (99.5%) and Ti target (99.5%) in a mixture of Ar and O_2, respsctively. The chamber working pressure was 5 mTorr. In addition, a single element, Ni/TiO_2/Ni metal-insulator-metal (selector element) and

a Ni/HfO_2/Pt (memory element) were fabricated at the same time by a simple shadow-mask process. All devices reported in this study were fabricated completely at room temperature without any additional thermal treatment. Figures 5.2(a) depicts a 8 × 8 1S1R crossbar array and the cross-section view of fabricated Ni/TiO_2/Ni/HfO_2/Pt stack. The top-view photograph of a flexible 8 × 8 1S1R array under a curly bending and the image inspected by the optical microscope are shown in Figs. 5.2 (d) and (c), respectively. In our electrical measurement setup, a bending vehicle with a radius of 10 mm was used to characterize flexible devices as shown in Fig. 5.3.

5.3 Results and Discussion

5.3.1 Flexible Ni/TiO_2/Ni and Ni/HfO_2/Pt

Figure 5.4 shows the bipolar *I–V* characteristics of the flexible Ni/TiO_2/Ni selector, where the highly nonlinear and symmetric *I–V* characteristics of at both polarities were determined through Schottky emission over the Ni/TiO_2 barriers of 0.58 eV as we have evaluated in Chapter 4. The barriers at the Ni/TiO_2 interfaces significantly affect the nonlinearity of current conduction. Therefore, to further modulate the interfaces is necessary to obtain a high nonlinearity and symmetric *I–V* characteristics of the Ni/TiO_2/Ni selector. It is particularly important for selectors used in flexible electronics that the bipolar *I-V* characteristics are not affected by the bending condition of the plastic substrate. Figure 5.5(a) shows excellent cycling endurance at both flat and bending states, where data more than 1000 cycles under ±4 V sweep were collected. Even though fabricated on the flexible substrate, Ni/TiO_2/Ni selector exhibits a superior stability with nonlinearity factor α of ~10^3 at V_{read} of 1.2 V. The selector current increased at the bending state, but can be recovered after removing the strain as evidenced in Fig. 5.5(b). It is possible due to the distribution of localized defects induced by the local fields of bending strain, as reflected in an increasing

shift of conduction current [74, 75].

As for the memory element, it is also particularly important for devices used in flexible electronics that the RS characteristics are not affected by the flexing of the devices. Figure 5.6(a) displays extremely reproducible bipolar RS in both flat and bending devices with a resistance ratio of at least 10^3. During 100 endurance cycles, tight distributions on high resistance state (HRS) resistance, LRS resistance, V_{SET}, and V_{RESET} in both flat and bending devices retain their values without significant change at the reading voltage, as shown in Fig. 5.6(b). Note that the bipolar RS was attributed to the connection/rupture of Ni filaments in HfO_2 though electromigration [71]. Read disturb and retention tests were conducted in order to investigate the reliability of the flexible RRAM. Figure 5.7 (a) and (b) show superior immunity to read disturb and retention characteristics at a reading voltage of 0.5 V for both flat and bending devices. The bipolar RRAM on the flexible substrate shows good retention characteristics up to 10^4 s without electrical degradation in both LRS and HRS under flat and bending devices, indicating the applicability of flexible RRAM in flexible electronics. A fast bipolar RS transient by a set pulse (+4 V, 100 ns) pulse and reset pulse (− 4 V, 100 ns) is exhibited in Fig. 5.8(a), in which a read pulse (1 V, 400 ns) was applied to determine the resistance state. We can further identify the robust endurance of Ni/HfO_2/Pt memory element without degradation up to 10^6 pulse cycles by the condition of 100 ns at ±4 V in Fig. 5.8(b). After 10^6 cycles, each memory cell exhibited two resistance states with LRS/HRS ratio > 10^3.

Overall, the bipolar selector and bipolar memory element represent an extremely promising solution of potentially flexible memories. The stacked bipolar selector and RRAM were further constructed together to examine the 1S1R electrical characteristics with the plastic substrate used.

5.3.2 Flexible and vertically stacked 1S1R array

Figure 5.9 shows reproducible nonlinear bipolar RS curves in the stacked $Ni/TiO_2/Ni/HO_2/Pt$ cell, where high nonlinearity at low voltage regime was dominated by the bipolar selector, and resistive-switching at high voltage regime was dominated by the memory element. V_{SET}/V_{RESET} below ±4 V, I_{RESET} less than 150 μA, and α of 10^3 at 1.2 V V_{read} were realized. As we have discussed in Chapter 4 (Fig. 4.3), this reported α is sufficient to implement a high-density array of 10 Mb, the largest ever reported for a 1D1R or 1S1R crossbar array. A gigabit memory chip partitioned into 16 banks would require a single array (bank) size of 64 Mb [76]. In order to evaluate the 8 × 8 1S1R crossbar array, all unselected cells were firstly programmed to LRS except the selected cell as shown in the equivalent circuit in Fig. 5. 10. To read the selected bit (as marked in red square), a voltage V_{pu} was applied between the selected top electrode and bottom electrode, while all unselected top/bottom lines were floating. As displayed in Fig. 5. 10, the read current with respect to the LRS/HRS of the selected cell in 8 × 8 crossbar arrays can be compared. With an R_{pu} load line was plotted, we can estimate the voltage swing (ΔV) between the 1S1R and 1R only crossbar arrays. Though device uniformity has not yet been optimized in the 8 × 8 1S1R array, successfully read margin of 0.82 V can be performed even when all unselected bits were at LRS, in sharp contrast to the collapsed read margin in an 8×8 1R array.

Moreover, program disturb in crossbar arrays is also a serious issue. To reduce disturbs to neighboring cells in the 1S1R array, the $V_{dd}/2$ write scheme, a much severe condition as compared to the $V_{dd}/3$ scheme, was used to evaluate the 1S1R write operation as illustrated in Fig. 5.11(a). In this scheme, a full V_{SET} or V_{RESET} was applied to the selected cell, but only those unselected cells along the selected word line or bit line endured one half of V_{SET} or V_{RESET}. Figure 5.11(b) shows the excellent immunity of both LRS and HRS to program disturb at 1/2 V_{SET} and 1/2 V_{RESET}. In this case, stress voltages of +2 V for HRS and − 2 V for LRS were applied to perform the immunity of SET/RESET disturbance of stacked

$Ni/TiO_2/Ni/HfO_2/Pt$. Finally, we conclude three possible architectures, 1S1R, 1D1R and CRS in Fig. 5.12. Based on the analytical calculation used in Chapter 4, the maximum allowed array number with the corresponding architectures as a function of nonlinear factor (α) can be plotted. Note that we redefined the R_{HRS}/R_{LRS} ratio of memory elements in CRS from the reported data [39] as the nonlinear factor. From the best reported CRS data [41], nonlinearity ~10^2 can only be utilized up to 16K-bit for CRS array. In comparison with our reported data, 512K-bit for 1D1R and 10M-bit for 1S1R have been demonstrated and realized on flexible substrates, showing their potential applications for future flexible electronics.

5.4 Summary

In this chapter, we demonstrate the bipolar *I–V* characteristics of flexible $Ni/TiO_2/Ni$ selector with high nonlinearity and the stable RS characteristics of $Ni/HfO_2/Pt$. The flexible $Ni/TiO_2/Ni$ and $Ni/HfO_2/Pt$ elements also had excellent mechanical stability upon harsh bending. Furthermore, a vertically stacked 8 × 8 1S1R array with superior read margin, endurance, immunity to read/program disturbs and retention has been realized. The simple cell structure and room-temperature process are particularly attractive for implementing high-density NVM in future low-cost flexible electronics and three-dimensional integrated circuits.

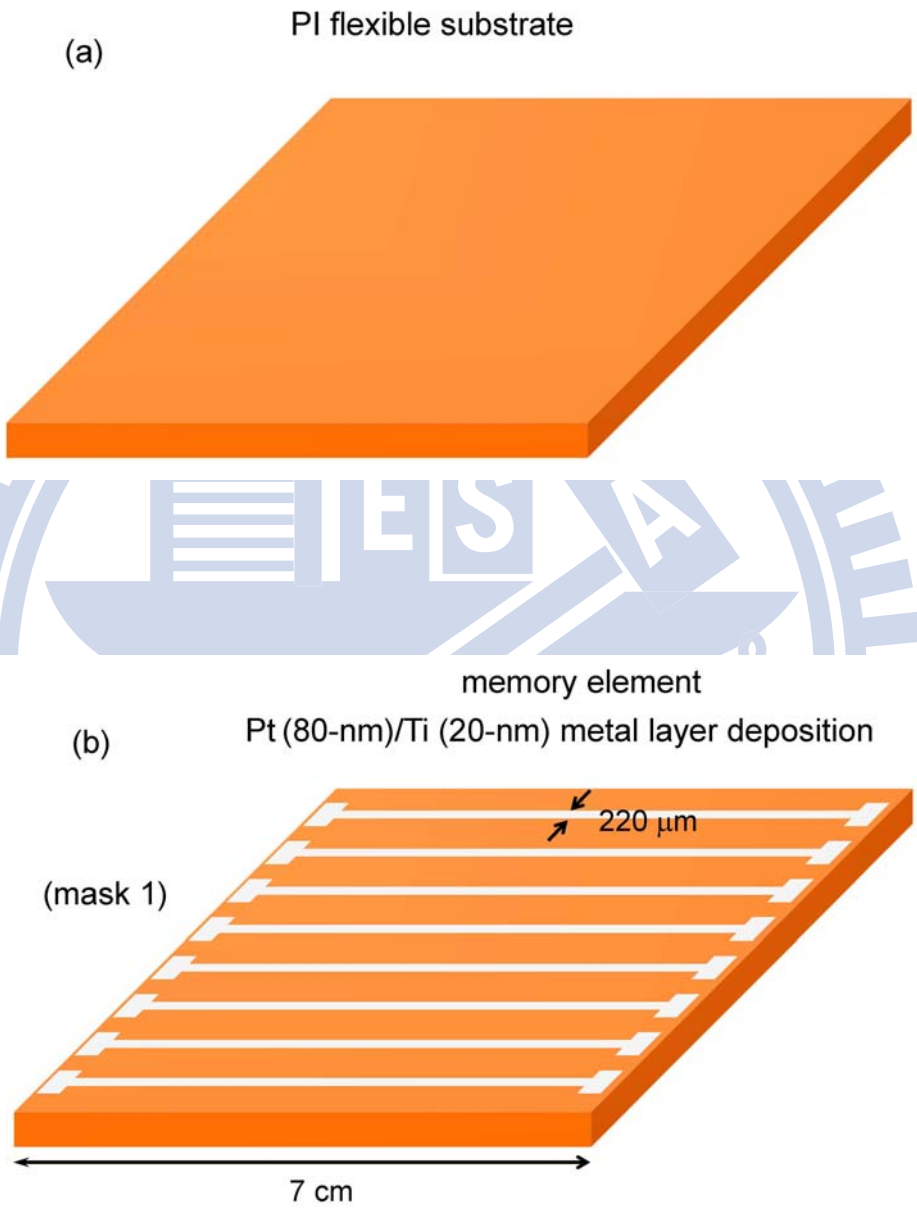

Fig. 5.1 (a) Polyimide (PI) substrates were prepared and ultrasonically cleaned in acetone. (b) Pt/Ti bottom electrodes deposition through mask 1.

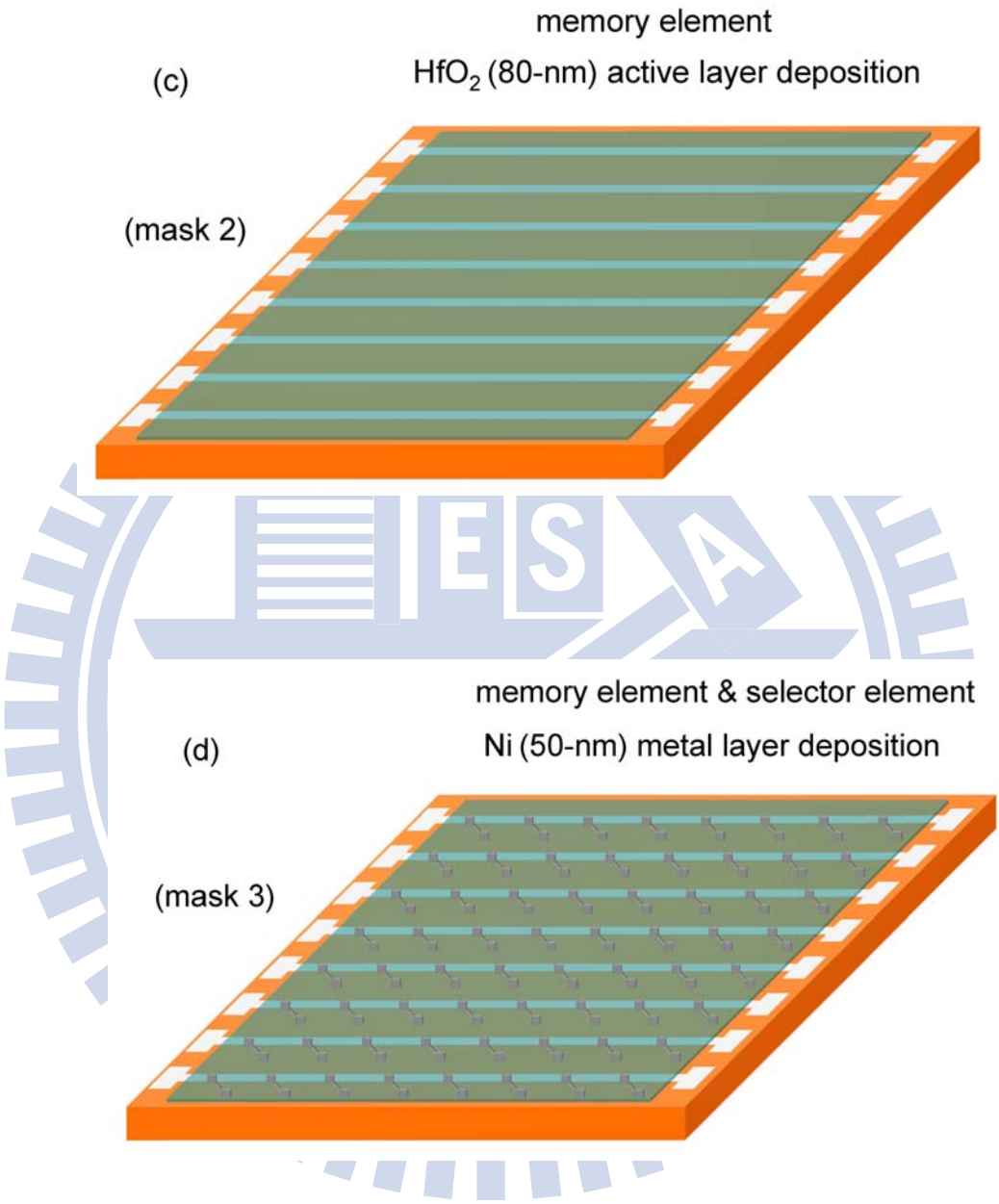

Fig. 5.1 (c) HfO_2 deposition through mask 2 and (d) Ni metal layer deposition through mask 3.

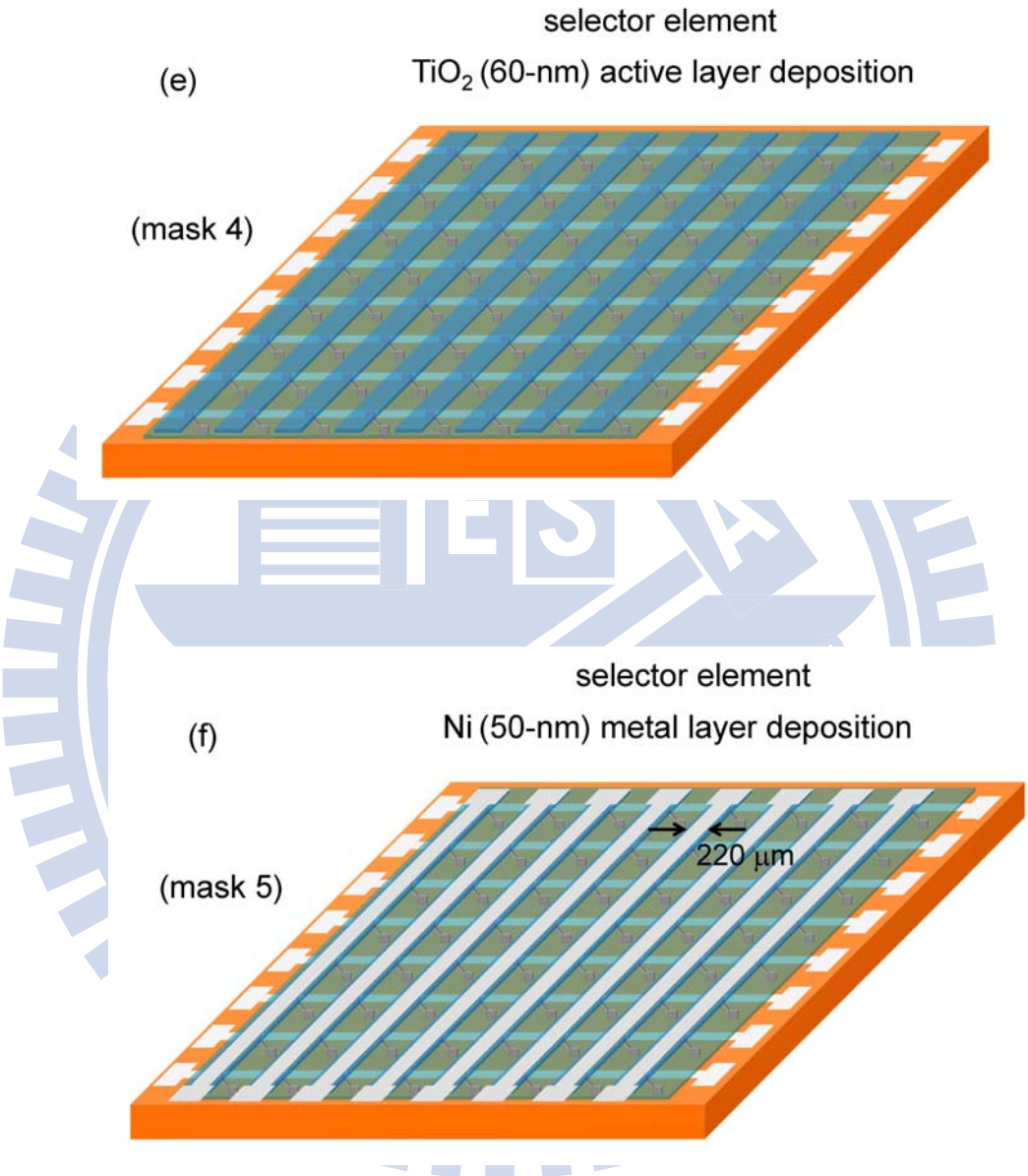

Fig. 5.1 (e) TiO_2 deposition through mask 4 and (f) Ni top electrode deposition through mask 5.

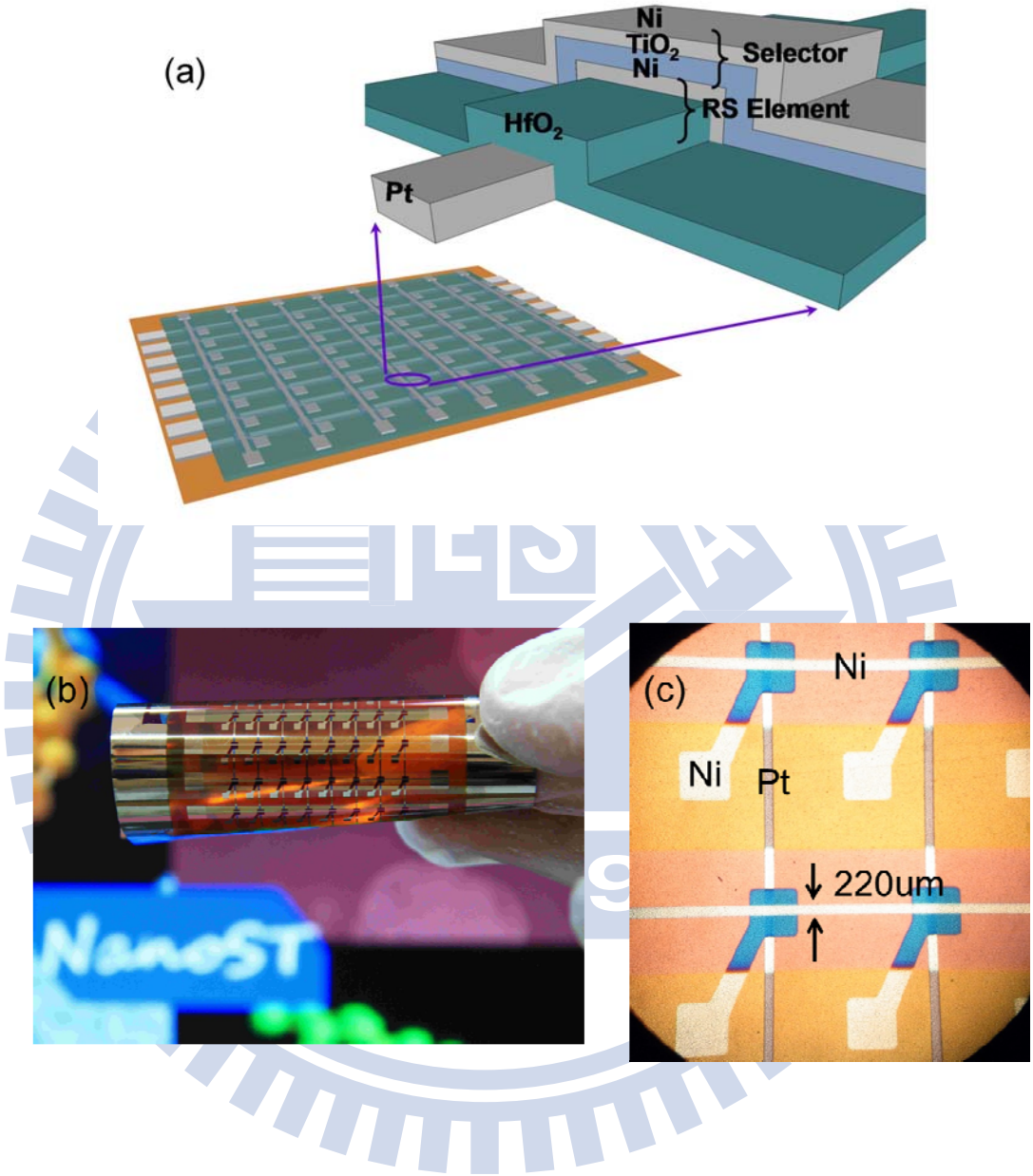

Fig. 5.2 (a) Cross-sectional view and (b) photograph of a flexible 8×8 1S1R memory array with a curly bending, and (c) optical microscope image of a vertically stacked Ni/TiO_2/Ni/HfO_2/Pt cell.

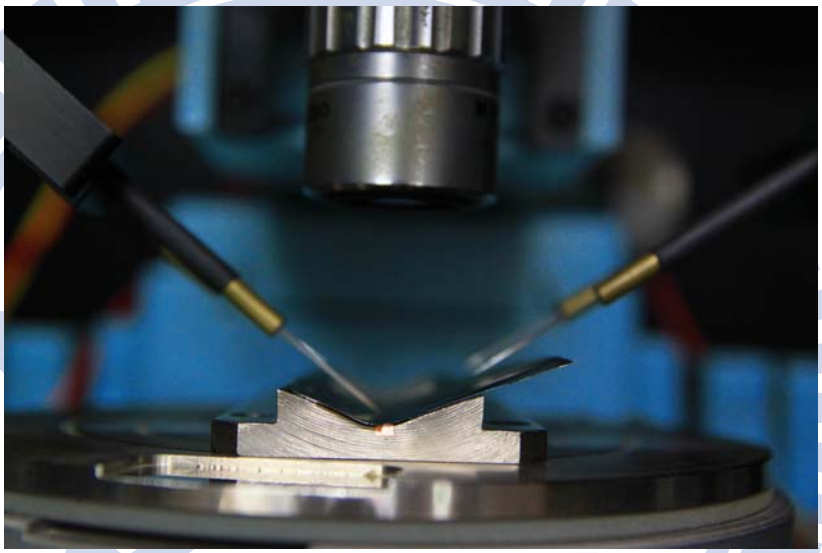

Fig. 5.3 Photograph of a flexible device with a bending radius of 10 mm under electrical testing.

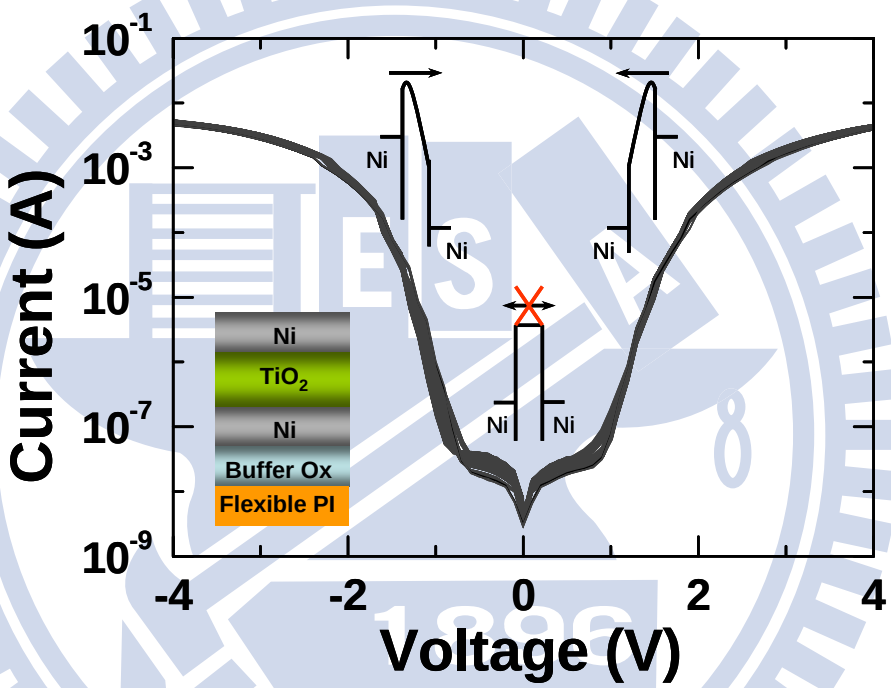

Fig. 5.4 Highly nonlinear and reproducible *I-V* curves of Ni/TiO_2/Ni bipolar selector (1000 successive cycles) by Schottky emission over Ni/TiO_2 barriers.

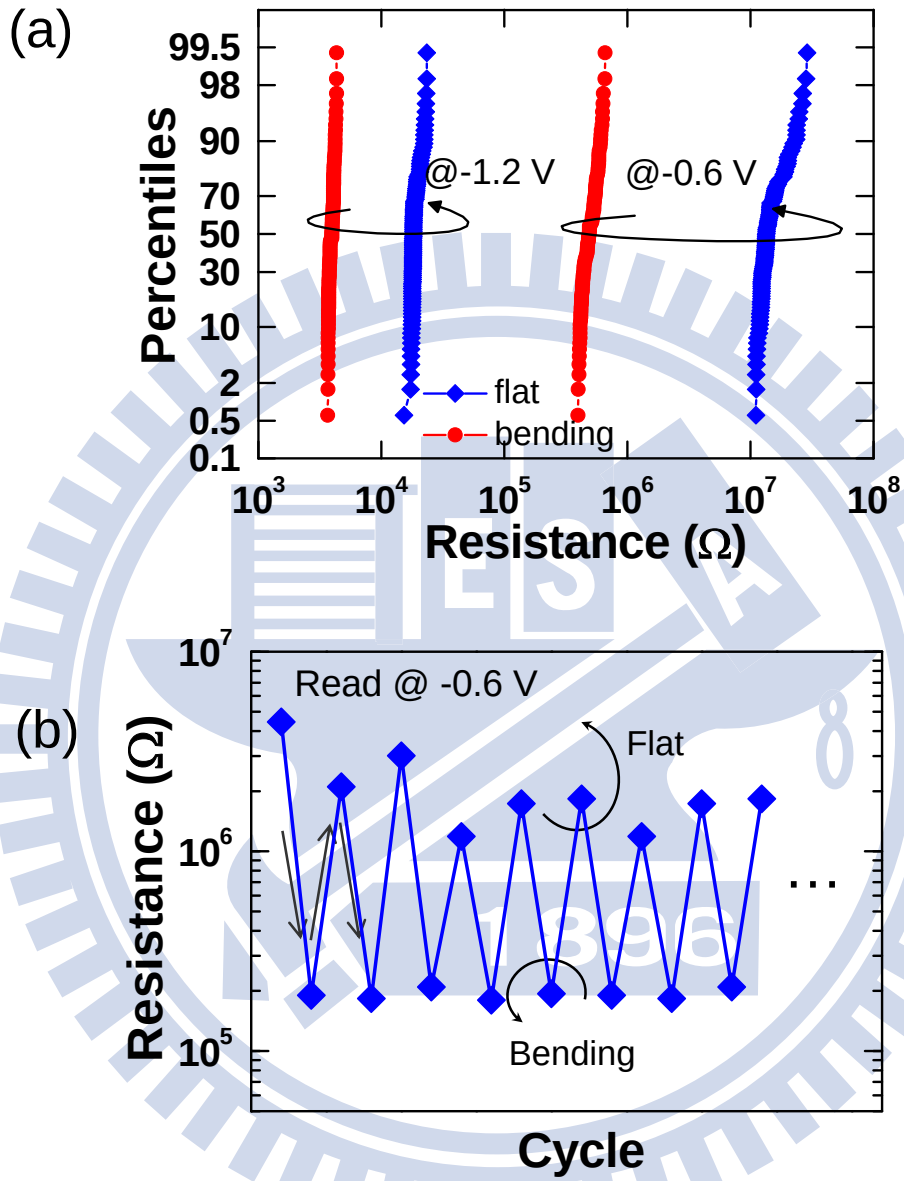

Fig. 5.5 (a) Endurance of the flat and bending Ni/TiO_2/Ni bipolar selectors under ±3 V DC cycling and (b) measured resistance of Ni/TiO_2/Ni bipolar selector at alternate flat and bending states.

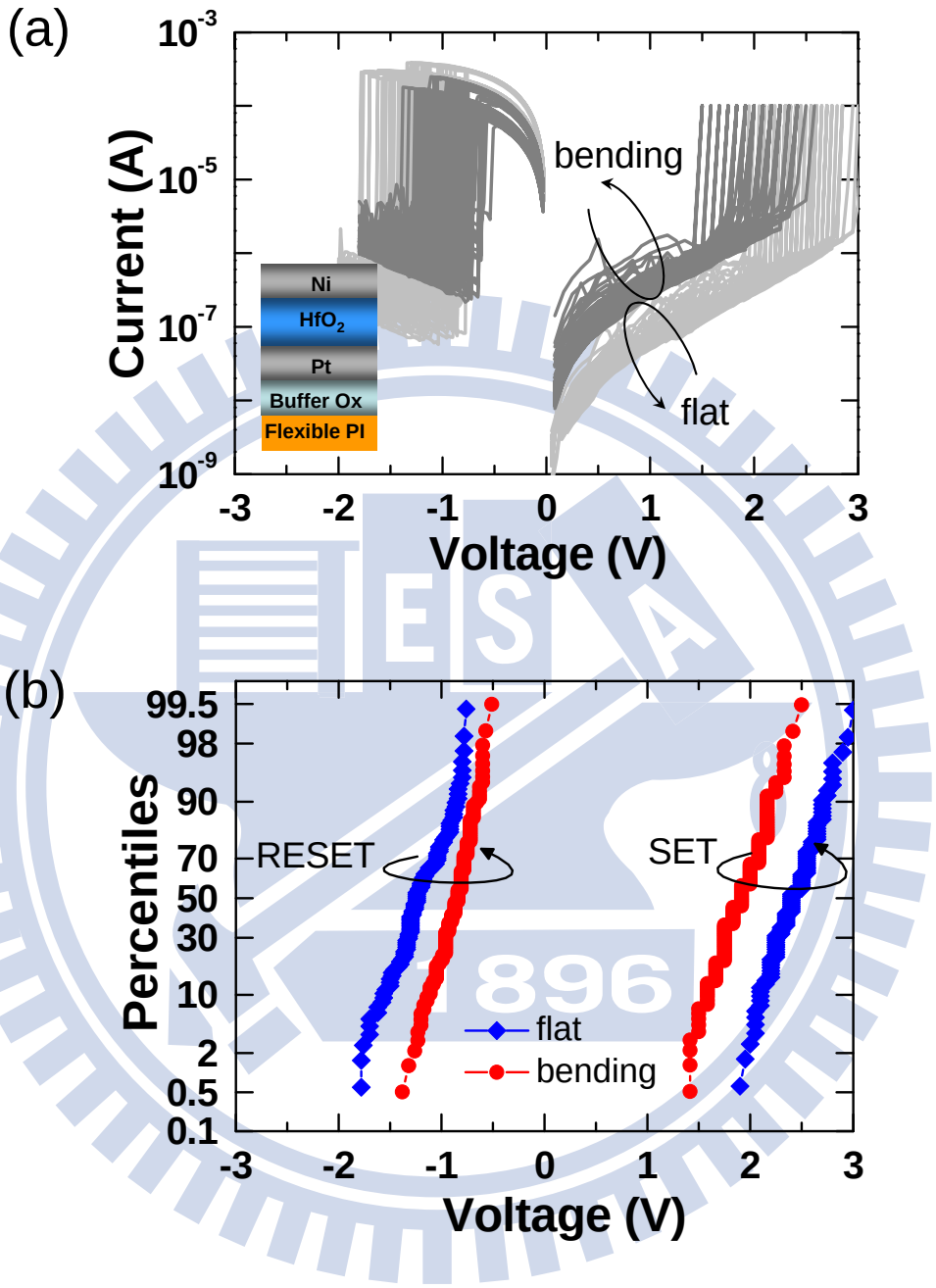

Fig. 5.6 (a) 100 successive bipolar RS *I-V* curves and (b) cumulative distribution of SET voltage and RESET voltage for both flat and bending Ni/HfO_2/Pt memory elements.

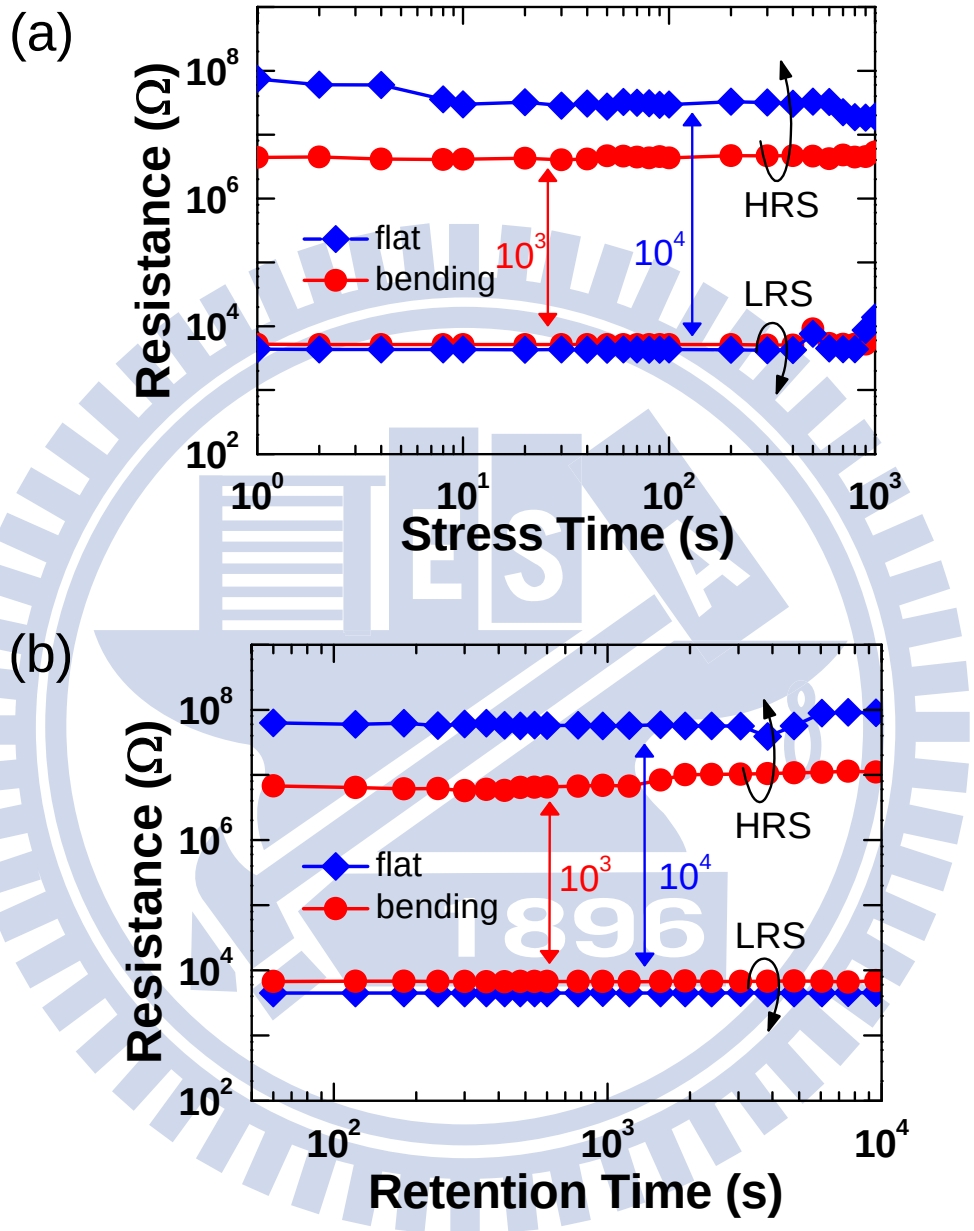

Fig. 5.7 (a) Read disturbance measurement stressed at 0.2 V and (b) retention measurement of flat and bending Ni/HfO_2/Pt memory elements.

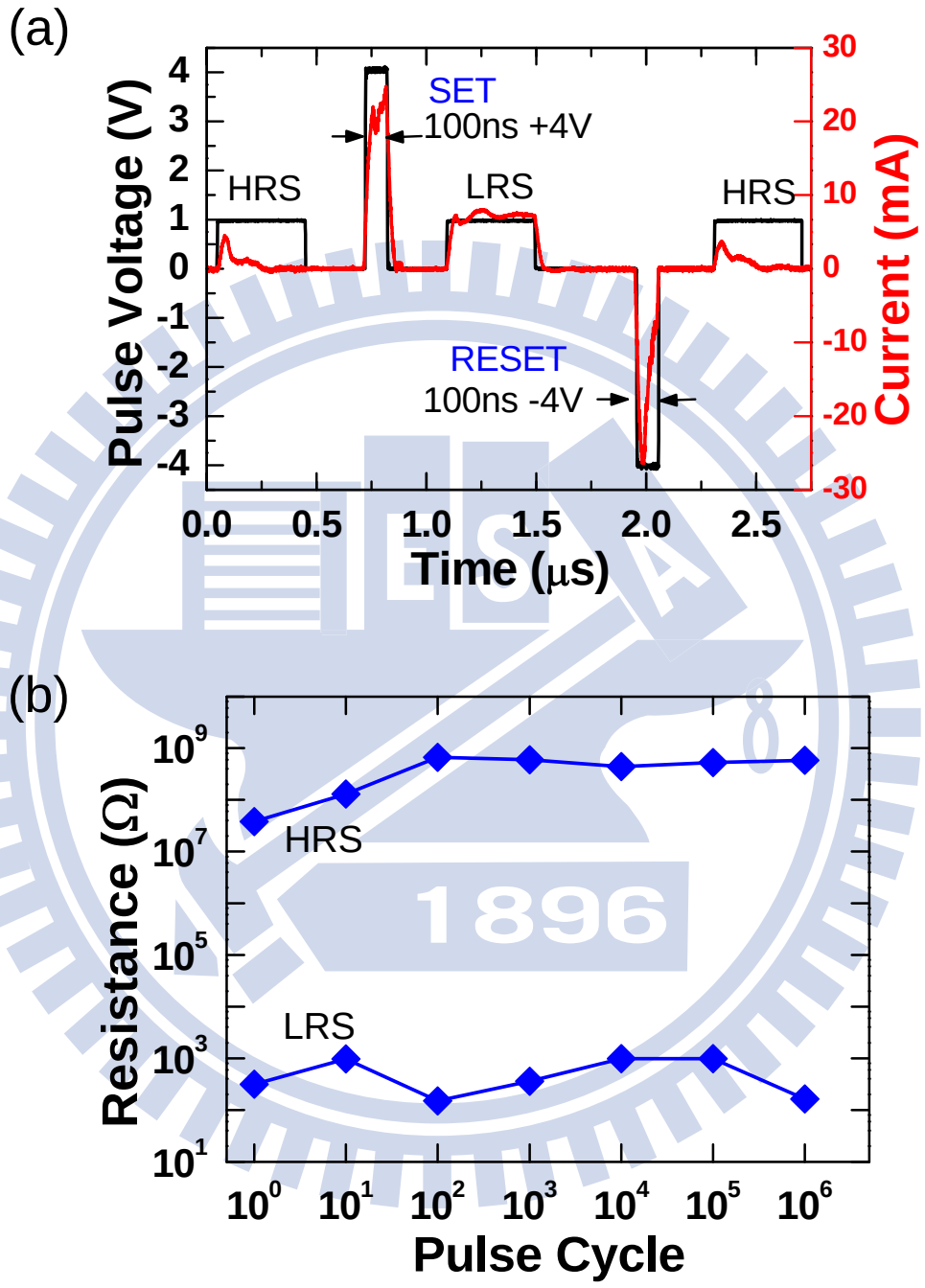

Fig. 5.8 (a) Transient response of RS by a 100 ns pulse at ±4 V and (b) robust endurance of Ni/HfO_2/Pt memory element under 10^6 cycles of ±4 V, 100 ns pulse switching.

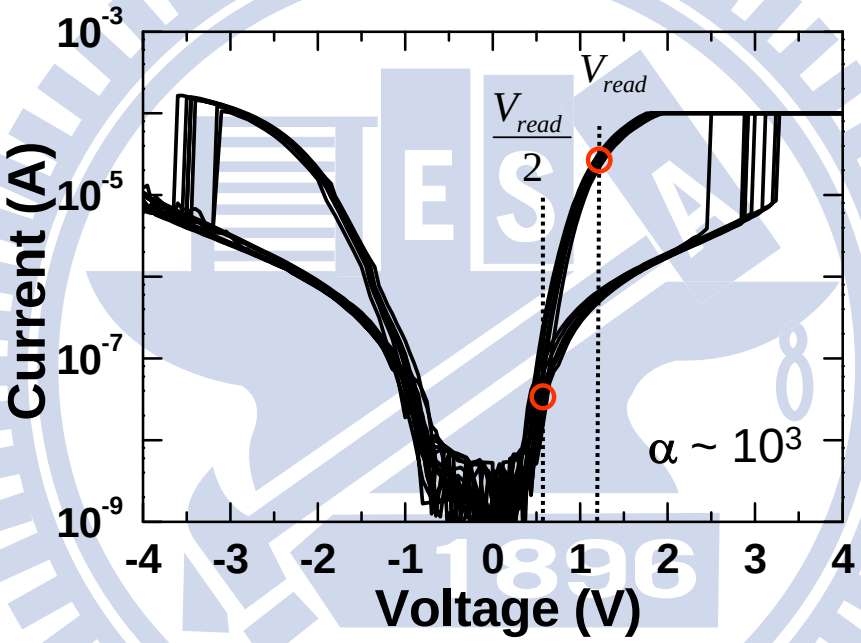

Fig. 5.9 Bipolar *I-V* RS cycles of vertically stacked Ni/TiO_2/Ni/HfO_2/Pt with α of 10^3 at V_{read} of 1.2 V.

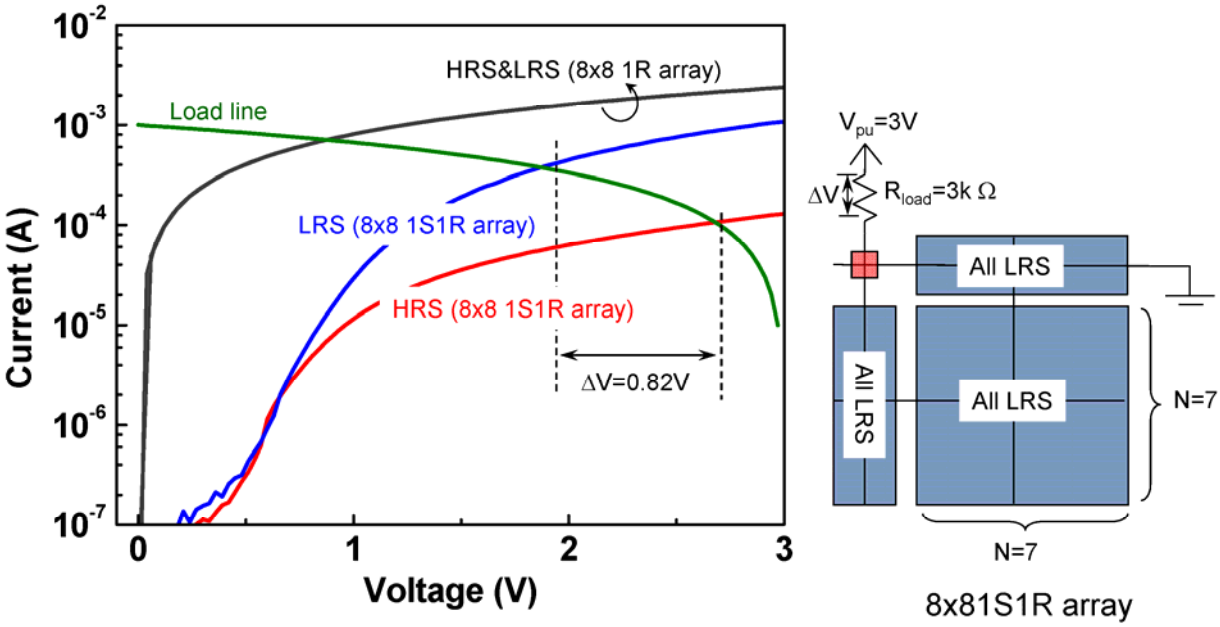

Fig. 5.10 Read margin between LRS and HRS in an 8 × 8 1R array and 1S1R array where all unselected bits were at LRS (See equivalent circuits in Fig. 4.1 & 4.2).

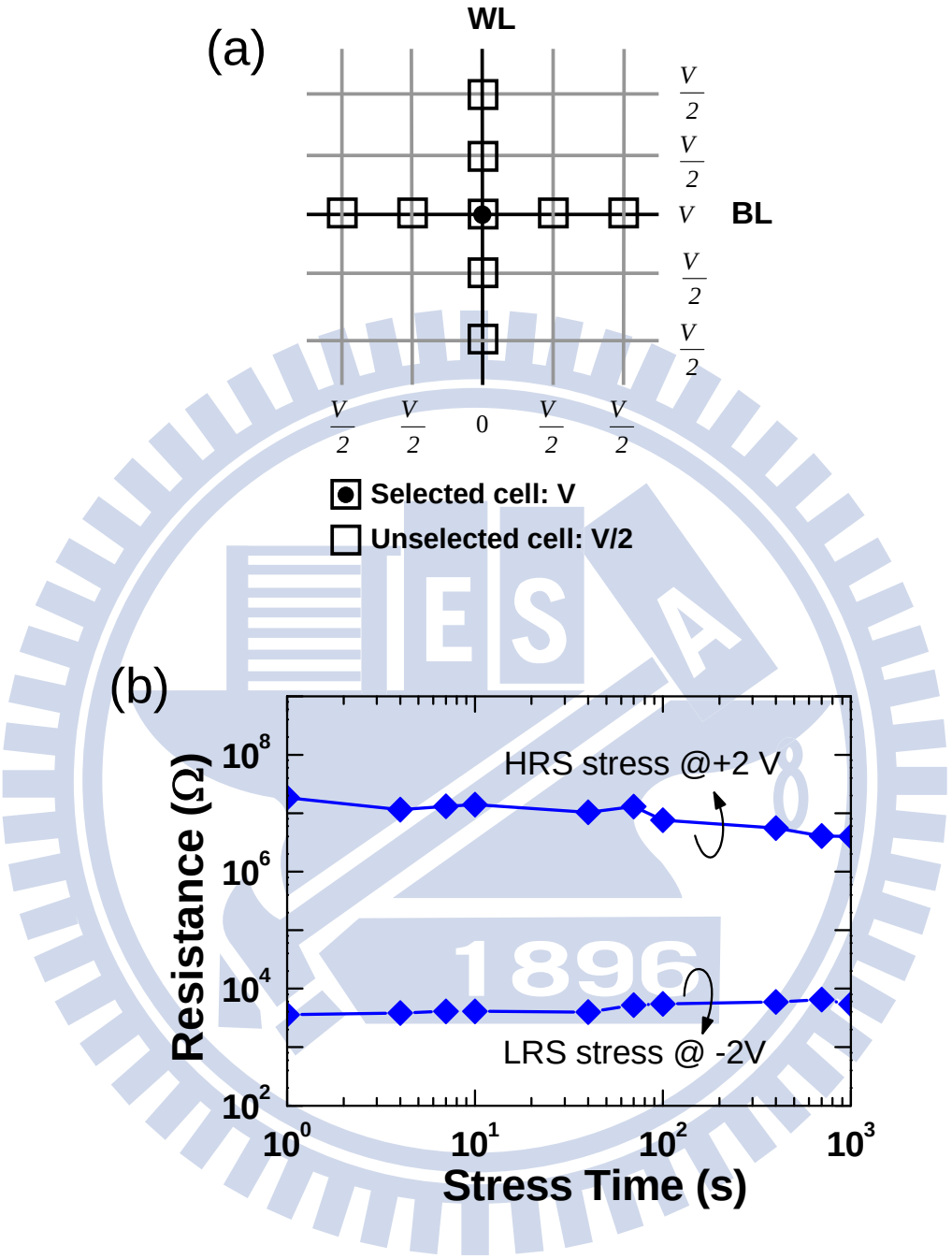

Fig. 5.11 (a) $V_{dd}/2$ SET/RESET scheme where only the unselected bits on the activated WL and BL are subjected to disturb voltage of $V/2$ and (b) SET/RESET disturbance measurement at 1/2 V_{SET}/V_{RESET} on vertically stacked Ni/TiO_2/Ni/HfO_2/Pt. HRS was stressed at +2 V while LRS was stressed at -2 V.

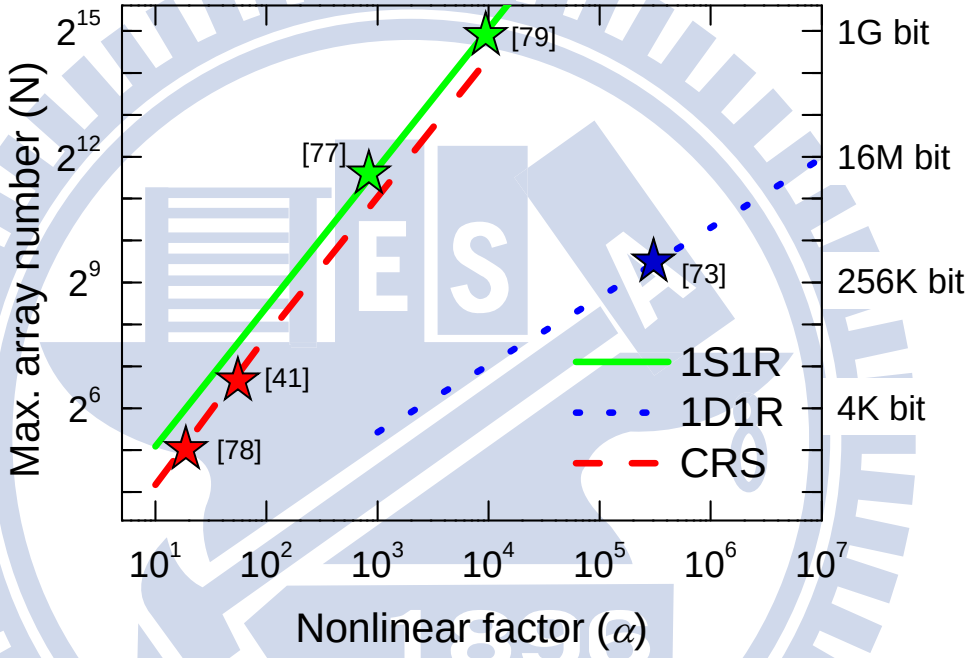

Fig. 5.12 Comparison of the maximum allowed array number based on the reported 1S1R [77, 79], 1D1R [73] and CRS [41, 78] architectures.

Chapter 6

Conclusion and Further Recommendation

6.1 Conclusion

Two TiO_2-based selection devices were proposed to reduce the sneak current in this dissertation. The unipolar Ti/TiO_2/Pt diode shows superior capability of conducting unipolar 1D1R switching by externally connecting a Ni/HfO_2/Pt memory element. Meanwhile, a bipolar Ni/TiO_2/Ni selector was investigated to perform the stable bipolar 1S1R switching with a bipolar RS element connected. Finally, an 8×8 1S1R array on the flexible substrate was successfully realized. The main results of these studies are summarized below.

In Chapter 2, we report the transition of stable rectification to resistive-switching behaviors in a Ti/TiO_2/Pt MIM. The oxygen migration and localized conductive filaments play important roles in not only the resistive-switching of RRAM devices but also the rectification of oxide diodes. When the current flows through the oxygen-deficient TiO_2 filaments, current behaviors were limited by the interfaces of Schottky barrier, resulting in the diode rectifying properties. After forming at higher voltage, much stronger filaments destroy the interface Schottky barrier, giving rise to the reproducible resistive-switching. The rectification properties are stable up to 125 °C and 10^3 cycles under ±3 V sweep without interference with the resistive-switching. Moreover, the current density of TiO_2 MIM diodes more than 10^4 A/cm^2 can be achieved, showing the satisfactory requirement of TiO_2 MIM diodes for future 1D1R RRAM applications.

In Chapter 3, a rectifying Ti/TiO_2/Pt oxide diode and a unipolar Ni/HfO_2/Pt memory element have been fabricated on flexible PI substrates using only room-temperature

processes. No significant device degradation was found at bending states. Additionally, the impact of I_{RESET} on the programming margin of unipolar RS has been discussed. The heterogeneous TiO_2-HfO_2 1D1R cell not only demonstrates more stable unipolar RS compared to the monolithic TiO_2 1D1R cell because of the lower I_{RESET} of the HfO_2 memory element, but also effectively suppresses the sneak current. The maximum allowed array size with at least 10% read margin was predicted to exceed 512 Kb based on a simple equivalent circuit model.

In Chapter 4, a Ni/TiO_2/Ni MIM with highly nonlinear *I-V* characteristics has been proposed by a very simple low-temperature process. Excellent bipolar nonlinear characteristics, including current difference of 6 orders of magnitude for a voltage swing from 0 to ±2 V and a breakdown voltage larger than 4 V are demonstrated. The nonlinearity was attributed to the Schottky emission over the Ni/TiO_2 barriers. By connecting the bipolar selector and a HfO_2 memory element, 1S1R exhibits robust and stable bipolar RS, and can effectively suppress the sneak current. In addition, the trade-off between the maximum array size and the power consumption is also discussed.

In Chapter 5, we used a low-temperature and simple sputtering process to fabricate a flexible Ni/TiO_2/Ni selector and Ni/HfO_2/Pt memory element. The flexible Ni/TiO_2/Ni and Ni/HfO_2/Pt elements also had excellent mechanical stability upon harsh bending. Furthermore, by a simple 5-mask process, we report for the first time a vertically stacked Ni/TiO_2/Ni/HfO_2/Pt 8×8 1S1R array fabricated completely at room temperature on a plastic substrate. This stacked 8×8 1S1R array with superior read margin, endurance, immunity to read/write disturbs and retention were examined. The simple cell structure and room-temperature process are particularly attractive for implementing high-density NVM in extremely low-cost flexible electronics.

6.2 Further Recommendation

It is necessary to further pursue the selection devices with high turn-on current density and high nonlinearity for the 1D1R or 1S1R architectures. Meanwhile, the improvement of process integration of selection devices and RS elements is an important research direction for 3D stackable crossbar arrays as well. There are some interesting topics related to this dissertation that are worthy to be further investigated:

(1) As described in Chapters 1, 2 and 3, a unipolar diode with high turn-on current density and high rectifying ratio is considerably required to build high-density crossbar memory arrays. Although the $Ti/TiO_2/Pt$ oxide diode with current density of ~10^4 A/cm^2 and rectifying ratio of ~10^5 have been achieved in this dissertation, current density and rectifying ratio of oxide diodes should be further improved to 10^7 and 10^9, respectively, in order to implement 1 G-bit memory size at the technology node of 100 nm (Fig. 1.4). To modulate interface barriers with other various materials considered is a key direction to increase the current density and rectifying ratio. Furthermore, the process integration of 1D1R structure also dominates the electrical properties. As shown in Fig. 3. 10(a), surface roughness at the 2^{nd} Pt layer may cause unstable operation of the $Ti/TiO_2/Pt$ diode. Hence, a smooth interface is needed to be investigated carefully.

(2) In Chapters 4 and 5, we proposed a nonlinear $Ni/TiO_2/Ni$ bipolar selector for implementing 1S1R architectures. It is highly required that if the nonlinearity can be further enlarged to 10^4, 1 G-bit of memory size will be available in our 1S1R architecture. The nonlinearity of $Ni/TiO_2/Ni$ may be improved by introducing the bandgap engineering, i.e. using MIIIM structure to replace MIM structure. This has been reported in FLASH

memory technologies to improve the tunneling efficiency of tunneling oxide. Here, we believe that this tri-layer structure can increase the required nonlinearity for high-density crossbar memory applications. Furthermore, it is worthy to use NEGF simulation to predict and examine the current transportations and discuss the effects of barrier heights and thicknesses of tri-layer structures.

(3) By a first approximation, we discuss the prediction model using the simplified One-BLPU read scheme. For simplicity, we ignored the voltage drop on R_{I} and R_{III} for 1D1R configuration, and R_{II} for 1S1R configuration, respectively. The proper way to predict the read margin as a function of array size is by using HSPICE, where the lines resistance, voltage drop on each node could be included in the HSPICE calculation. In addition, as we have discussed in Chapter 1, there are nine possible voltage configurations to conduct a read process, so it is recommended that each read configuration must be carefully investigated based on the three architectures, 1S1R, 1D1R, CRS.

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