國立交通大學

電子工程學系 電子研究所

博士論文

先進CMOS元件結構的解析模型建立—量子侷限效應及製程變異敏感度之探討

Analytical Modeling of Advanced CMOS Device Structures — Quantum Confinement and Sensitivity to Process Variations

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A Dissertation
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

October 2011
Hsinchu, Taiwan, Republic of China

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摘要

本論文建立一個理論架構，以 Poisson 和 Schrödinger 方程式的解析解為基礎，考慮量子侷限效應，探討多種先進元件結構的微縮性及對於製程變異的敏感度。這個理論架構包含多重閘極元件(Multi-Gate)、環閘極元件(Gate-All-Around)、超薄層通道元件(Ultra-Thin-Body)等先進元件結構，並可應用於使用高遷移率(high mobility)通道材料的元件。

利用三維 Poisson 方程式的解析解，我們可由靜電完整性的角度，比較多重閘極元件及環閘極元件的臨界電壓對於製程變異的敏感度。結論指出採用輕摻雜通道的環閘極元件受到製程變異及隨機摻雜擾動的影響最小。對於重摻雜通道的元件，摻雜數目的變異會決定元件的臨界電壓變異，而環閘極元件由於其較大的表面積-體積比(surface-to-volume ratio)，其臨界電壓受到摻雜數目變異的影響將會大於多重閘極元件。

當元件尺度更加微縮，我們利用 Schrödinger 方程式的解析解，探討量子侷限效應對於短通道元件鰭狀電晶體及環閘極元件的臨界電壓變異的影響。結論指出，由於量子侷限效應，通道寬度變異對於極小尺寸的鰭狀電晶體及環閘極元件的重要性提升。對於採用不同通道表面方向鰭狀電晶體而言，(100)表面方向的矽元件及(111)表面方向的鍺元件在通道寬度變異時，表現出較低的臨界電壓敏感度。由於臨界電壓對通道寬度的敏感度會由短通道效應及量子侷限效應共同決定，因此環閘極元件的通道寬度可經由最佳化

設計以減少臨界電壓變異。

利用 Schrödinger 方程式的解析解，我們探討量子侷限效應對於超薄層通道元件及多重閘極元件的短通道效應的影響。結論指出，當元件的通道厚度小於某一臨界值時，量子侷限效應可改善超薄層鍺元件的臨界電壓下降(threshold voltage roll-off)。由於鍺通道較為顯著的量子侷限效應，超薄層鍺元件可能比矽元件有更小的臨界電壓下降。對於多重閘極結構，砷化銦鎵(InGaAs)通道的臨界電壓下降問題可被鰭狀通道高度(fin height)方向的量子侷限效應抑制，使其與鍺通道元件相比有更小的臨界電壓下降。此二維的量子侷限效應對於多重閘極元件的微縮性有顯著的影響。我們改變通道寬度及高度，觀察不同高寬比(aspect ratio)的元件，發現當元件的 subthreshold swing 相同時，三閘極(Tri-gate)電晶體由於其較顯著的二維量子侷限效應，比鰭狀電晶體(FinFET)有更佳的微縮性。

我們提供一個適用於高介電閘極絕緣層平坦式矽及鍺通道元件的量子侷限效應形成的載子層厚度(dark space)的封閉形式(closed-form)模型。這個模型對於(絕緣層及通道間)能障高度、表面電場、通道及閘極絕緣層中的等效質量等參數的相依性皆有良好的準確度。此模型亦適用於通道採用後退型摻雜(retrograde doping)的元件。此模型可應用於預測鍺元件考慮量子侷限效應後的 subthreshold swing 及臨界電壓上升量。由於量子侷限效應會放大摻雜擾動造成的臨界電壓變異，我們進一步建立了此量子侷限效應造成的倍增因數模型。利用此量子模型，我們可以更準確地評估各個參數(如有效氧化層厚度(EOT)、溫度等)對於摻雜擾動造成的臨界電壓變異的影響。

應用等效趨動電流法(effective drive current approach)，可分析隨機摻雜擾動(RDF)及線邊緣粗糙(LER)對於平坦式 Bulk 元件及鰭狀電晶體(FinFET)的切換時間(switching time)變異的影響。研究結論指出，對於平坦式 Bulk 元件，雖然隨機摻雜擾動被視為是臨界電壓變異的主要來源，但是當考量切換時間變異時，線邊緣粗糙的相對重要性會提升。對於鰭狀電晶體，雖然鰭狀通道寬度方向的邊緣粗糙被視為是臨界電壓變異的主要來源，但是當考量切換時間變異時，鰭狀通道長度方向的邊緣粗糙的相對重要性將會提升。

關鍵字：臨界電壓變異、量子侷限效應、超薄層通道元件、多重閘極元件、環閘極元件、高遷移率元件、切換時間

Analytical Modeling of Advanced CMOS Device Structures－Quantum Confinement and Sensitivity to Process Variations

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Abstract

Based on the analytical solution of Poisson and Schrödinger equation, this dissertation establishes a theoretical framework to investigate the device scalability and sensitivity to process variations considering the impact of quantum-confinement effects. This theoretical framework includes advanced CMOS device structures such as multi-gate, and Gate-All-Around (GAA), and Ultra-Thin-Body (UTB) devices, and can be applied to devices with high-mobility channel materials.

From the prospective of electrostatic integrity, we compare the sensitivity of threshold voltage (V_{th}) to process variations for multi-gate devices with various aspect ratio (AR) and GAA device using analytical solutions of 3-D Poisson's equation. Our study indicates that lightly doped GAA device shows the smallest V_{th} variation caused by process variation and dopant number fluctuation. For heavily doped devices, dopant number fluctuation may dominate the overall V_{th} variation. The V_{th} dispersion of GAA device may therefore be larger than that of multi-gate MOSFETs because of its larger surface-to-volume ratio. We also analyze the impact of AR on the V_{th} dispersion due to dopant number fluctuation for

multi-gate MOSFETs.

Using the derived analytical solutions of Schrödinger equation for short-channel devices, we investigate the impact of quantum-confinement effect on the sensitivity of V_{th} to process variations. Our study indicates that, for ultra-scaled FinFET and GAA devices, the importance of channel thickness (t_{ch}) variation increases due to the quantum-confinement effect. For FinFET, the Si-(100) and Ge-(111) surfaces show lower V_{th} sensitivity to the t_{ch} variation as compared with other orientations. As the V_{th} sensitivity to t_{ch} for short-channel device is determined by the short-channel effect and the quantum-confinement effect, the t_{ch} of GAA MOSFETs can be optimized to reduce the V_{th} variation.

The impact of quantum-confinement on the short-channel effect for UTB and multi-gate MOSFETs are investigated using the derived analytical solutions of Schrödinger equation. When the t_{ch} is smaller than the critical thickness, the quantum-confinement effect may decrease the V_{th} roll-off of GeOI MOSFETs. Thus, Ge devices may exhibit better V_{th} roll-off than the Si counterpart because of the more significant quantum confinement. For multi-gate structure, by exploring the quantum-confinement effect along the H_{fin} direction, the V_{th} roll-off of InGaAs devices can be suppressed and become smaller than the Ge counterpart. This 2-D quantum-confinement effect is also crucial to the scalability of multi-gate device. Our study indicates that for a given subthreshold swing, Tri-gate (AR=1) with significant 2-D confinement effect exhibits better V_{th} roll-off than FinFET (AR>1).

We provide a closed-form model of quantum "dark space" for Ge and Si MOSFETs with high-k gate dielectric. This model shows accurate dependences on barrier height, surface electric field, and quantization effective mass of channel and gate dielectric. Our model can also be used for devices with the steep retrograde doping profile. This physically accurate dark space model will be crucial to the prediction of the subthreshold swing and quantum-confinement induced V_{th} shift of advanced Ge devices. Using this closed-form dark

space model, we also provide a closed-form model for the quantum-confinement induced amplification factor (AF_{QC}) in V_{th} variation due to random dopant fluctuation (RDF). Using our model, various factors such as EOT and temperature that may modulate/reduce the impact of RDF on Ge and Si MOSFETs can be accurately assessed.

The impact of RDF and LER on the switching time variations of bulk MOSFETs and FinFET have been assessed using the effective drive current approach that decouples the switching time variation into transition charge (ΔQ) and effective drive current (I_{eff}) variations. Our results indicate that for bulk MOSFETs, although the RDF has been recognized as the main variation source to V_{th} variation, the relative importance of LER increases as the switching time variation is considered. As for lightly-doped FinFET, although the impact of fin-LER is more crucial to V_{th} variation, the relative importance of gate-LER increases as the switching time variation is considered.

Keywords: threshold voltage variation, quantum-confinement, Ultra-Thin-Body, Multi-Gate, Gate-All-Around, high mobility channel, switching time

誌謝

進入交大以來漫長而充實的旅程，如今即將抵達終點。在碩博兩階段共七年多的時間，是養成我專業能力的精華時期，這段研究生涯中，感謝蘇彬老師多年的指導，拓展了我的研究視野以及培養我對問題的思考邏輯。老師總能未雨綢繆地考量到未來所需，一步步地建構起研究環境。在無數次和老師的討論中，不斷激發出新的想法，也慢慢勾勒出這本論文的雛形。每次完成的研究片段要發表時，老師總是再三斟酌修改字句，以期能更準確地表達出研究內容。當投稿不順利令我士氣受沮時，老師的客觀分析總能讓我重拾信心，有動力再繼續嘗試。如今這幾年的研究成果能夠集結而成這篇論文，首先要謝謝老師的督導和鼓勵。

最後階段的畢業口試終於得以順利通過。感謝汪大暉教授擔任口試召集人，以及林鴻志教授、趙天生教授、李佩雯教授、楊富量主任在百忙之中抽空來擔任我的口試委員，耐心回覆我在邀集過程中的多次叨擾，並且提供我許多的寶貴建議。在我的口試當天，感謝實驗室成員幫忙事前準備，也謝謝電機學院的廖郁雁小姐，對於口試場地的借用以及行政事務的鼎力協助。

從碩士班時就一直欣羨著李維、陳柏年、王生圳三位學長的背影，或許這也是當時促使我想繼續唸博士班的動機之一，很感謝你們提供的建議與經驗分享。同時和我進入實驗室的 Vita 和俊延，我們是一同經歷過各個大小戰役的老兵，很高興最終都能順利通過考驗，一起完成博士學業。銘隆、昆諺、昌鴻三位博班學弟，有你們的幫忙，這本論文中的許多部分才得以完成，你們也讓我的生活點綴了許多有趣回憶。已畢業的欣原，感謝你對我的個人電腦的照料以及研究上的幫助。在和劭衡、俊賢、青維、克駿相處時，常會讓我想起碩士班時的生活，和你們的閒聊也常讓我驚覺我們年齡上的差異。謝謝嘉麈學弟、孟漢、明琦，你們常常熱心分享博士班的生活點滴，為我們增添了許多話題。

謝謝我的家人，這幾年一直支持我繼續博士學業，提供我生活上和心理上的強力後

盾，在我遭受挫折時安慰我，在我通過難關時分享我的喜悅。感謝秉真的陪伴，少了你，我的生活將只是單調的例行記事，除了在課業研究外，還鼓勵我多方面去嘗試新的興趣，讓我對於研究和生活更有熱情。此外，謝謝你在口試前的最後階段還充當聽眾，幫助我修飾講述內容。

這本論文的完成還要感謝國家高速網路與計算中心長期提供學術界模擬軟體的license，讓我的理論計算得以進行驗證。另外，李素萍小姐和黎裕群學長提供的協助，讓我們能更有效率地解決軟體使用的問題。我的研究需要倚賴實驗室的工作站，都是由銘隆和劭衡負責維護和管理，這繁重的工作讓我由衷地欽佩與感謝。

2011 年十一月 誌于交通大學

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Chapter 1
Introduction

To continue the MOSFET scaling, advanced device structures with better gate control are promising candidates to extend the roadmap of CMOS. Recently, Ultra-Thin-Body (UTB) and multi-gate structures have been promoted as parallel device types with the planar bulk MOSFETs [1]. In the long term, Gate-All-Around (GAA) nanowire with an ideal structure to provide superior gate control is also an important candidate for ultimate CMOS structure [1]. In addition to the innovation of device structure, Ge and III-V channels with intrinsically higher mobility than Si have been proposed to improve the performance of highly-scaled MOSFETs [1]. Eventually, MOSFET may possess the features of both advanced device structure and high mobility channel material.

With the scaling of device dimensions, the impact of process variations has become a crucial issue to device design. As the random dopant fluctuation are significant to heavily-doped devices such as planar bulk MOSFETs [2]-[4], fluctuations associated with the geometry variations such as line edge roughness are especially important to lightly-doped devices [5]-[7]. The threshold voltage (V_{th}) dispersion due to these process variations becomes increasingly important with the supply voltage scaling down. In addition to the V_{th} variation, the switching time variation is important to the logic circuits. Although the V_{th} variation has attracted extensive attention, detailed study regarding the switching time variation due to process variations has rarely been seen.

For planar bulk MOSFETs, the gate control against the short-channel effect depends on the enhancement of the surface electric field (by increasing the channel doping). The increasing surface electric field results in significant electrical confinement [8], which will increase the carrier centroid distance from the interface. This increased carrier centroid distance (or dark space [9], [10]) will degrade the device electrostatic integrity because it increases the electrical EOT [1]. For undoped devices, the enhancement of gate control is through the scaling of channel thickness, which will result in significant structural confinement [8]. As compared with Si devices, the quantum-confinement effect becomes more significant when high mobility channel materials (which usually possess smaller effective mass) are used. Since the quantum-confinement effect reduces the carrier density and increases the V_{th}, it may also alter the V_{th} sensitivity to process variations.

This work has established a theoretical framework that can be used to assess the electrostatic integrity and quantum-confinement effect of various device candidates for CMOS scaling. This theoretical framework is based on the analytical solutions of Poisson and Schrödinger equations for planar bulk, UTB SOI, multi-gate, and GAA devices. By tackling the scalability and sensitivity to process variations, we can assess the feasibility and optimum design of these promising device options. The organization is as follows.

From the perspective of the electrostatic integrity, Chapter 2 comprehensively compares the sensitivity of V_{th} to dopant number fluctuation and process variations for multi-gate and GAA MOSFETs using the derived analytical solutions of Poisson's equation for multi-gate and GAA devices. The impact of aspect ratio on the V_{th} variation due to dopant number fluctuation for multi-gate devices is investigated. Besides the dopant number fluctuation, impacts of geometry variations such as gate length and channel thickness variations are examined to assess an optimum design between multi-gate and GAA devices.

When the device dimensions are further scaled, Chapter 3 investigates the impact of quantum-confinement effect on the V_{th} sensitivity to process variations. By considering the short-channel potential, analytical solutions of Schrödinger equation for short-channel FinFET and GAA devices are derived. We investigate the V_{th} sensitivity to process variations for short-channel FinFET with various surface orientations [11] using the derived short-channel quantum-confinement model. For GAA MOSFETs, we demonstrate that there is an optimum channel thickness design to reduce the V_{th} sensitivity to process variations.

Since the high mobility channel devices are more susceptible to short-channel effects [12], [13], Chapter 4 investigates the impact of quantum-confinement effect on the V_{th} roll-off of high mobility channel MOSFETs. A detailed study of quantum-confinement effect on the V_{th} roll-off of UTB Ge devices is conducted. To assess the scalability of InGaAs multi-gate MOSFETs, the analytical solution of 2-D Schrödinger equation for multi-gate devices is used to consider the 2-D quantum-confinement effect. With these derived short-channel quantum-confinement models, we can fairly compare the V_{th} roll-off of high mobility channels.

The quantum dark space is crucial to the electrostatic integrity of heavily-doped planar bulk MOSFETs [10]. Chapter 5 provides a closed-form dark space model that considers the wavefunction penetration into the high-k dielectric and the parabolic potential well. With this closed-form dark space model, the quantum-confinement induced amplification of V_{th} variation due to RDF can be further modeled. Combined with the classical model for V_{th} variation, a quantum-mechanical V_{th} variation model can be derived.

Besides the V_{th} variation, the process variations also results in switching time variation. Chapter 6 investigates the impacts of random dopant fluctuation and line edge roughness on the switching time variations for heavily-doped planar bulk MOSFET and lightly-doped FinFET. Using the effective drive current approach [14], the switching time variation can be decoupled into the effective drive current variation and the transition charge variation. Thus, we can fill the gap between the V_{th} variation and the switching time variation due to process variations, and provide more physical insights in the switching time variations.

Chapter 7 summarizes essential research results and contributions of this dissertation work.

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Chapter 2

Sensitivity of Threshold Voltage to Process Variations－A Perspective from Electrostatic Integrity

2.1 Introduction

For nano-CMOS device design, the challenge lies in dispersions [1]. They are mainly due to process variations and dopant fluctuation that result in the dispersion of threshold voltage, and are closely related to the device electrostatics [1]. In other words, electrostatic integrity and variability are crucial in assessing the feasibility of various device structure options.

Due to their better gate control, multi-gate [2]-[4] and Gate-All-Around (GAA) [5]-[7] structures are considered as important candidates for the future CMOS scaling. Dependent on the aspect ratio (AR), FinFET (AR>1) and Tri-gate (AR=1) are two main options in the multi-gate device design. Whether there is an optimum choice for the multi-gate structure between the two options merits investigation. The GAA structure features the surrounding gate channel, which is an ideal structure to provide better gate control. However, with the scaling of device geometry, the impact of process variations has become a crucial issue to device design. Although GAA structure is a promising alternative for future device scaling, its immunity to process variations remains an important question [8]-[10]. Moreover, whether there is an optimum choice between GAA and multi-gate structures merits further examination.

In this chapter, we assess the sensitivity of GAA device to process variations compared with multi-gate MOSFETs using theoretical calculation. A theoretical framework that can be used to assess the feasibility of GAA and multi-gate devices by tackling their electrostatic integrities and sensitivities to process variations will be provided [11]. First, we derive the channel potential and the subthreshold current models for GAA [11] and multi-gate structure [12], respectively. The threshold voltage (V_{th}) can be determined using the calculated subthreshold current. Based on our theoretical calculation, we investigate the V_{th} sensitivity to process variations for GAA structure compared with that of multi-gate devices.

2.2 Modeling of Subthreshold Characteristics for Multi-Gate and GAA Structures

An analytical channel potential solution is crucial to the derivation of subthreshold characteristics such as subthreshold current and V_{th}. The channel potential solutions for multi-gate and cylindrical GAA structures are described as follows.

2.2.1 Analytical Channel Potential Solution for Multi-Gate Structure

Figure 2-1 shows the schematic sketch of a multi-gate SOI structure. The Si-fin body covered by gate insulator is a cuboid with six faces, and each face is connected to a voltage bias. In the subthreshold regime, the Si-fin body is fully depleted with negligible mobile carriers. Therefore, the potential distribution, $\phi(x, y, z)$, satisfies the Poisson's equation:

$$\frac{\partial^2\phi(x,y,z)}{\partial x^2}+\frac{\partial^2\phi(x,y,z)}{\partial y^2}+\frac{\partial^2\phi(x,y,z)}{\partial z^2}=-\frac{qN_a}{\varepsilon_{si}} \qquad (2\text{-}1)$$

where N_a is the doping concentration of the Si-fin. The required boundary conditions can be described as:

$$\phi(W_{fin},y,z)+t_{i,f}\,\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial x}\right|_{x=W_{fin}}=V_{fg}-V_{fb} \qquad (2\text{-}2a)$$

$$\phi(0,y,z)-t_{i,b}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial x}\right|_{x=0}=V_{bg}-V_{fb} \tag{2-2b}$$

$$\phi(x,y,H_{fin})+t_{i,t}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial z}\right|_{z=H_{fin}}=V_{tg}-V_{fb} \tag{2-2c}$$

$$\phi(x,y,0)-t_{ox,u}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial z}\right|_{z=0}=V_{ug}-V_{fb} \tag{2-2d}$$

$$\phi(x,0,z)=-\phi_{ms} \tag{2-2e}$$

$$\phi(x,L_{eff},z)=-\phi_{ms}+V_{DS} \tag{2-2f}$$

where ε_{si} ,ε_i and ε_{ox} are dielectric constants of the Si-fin, gate dielectric and oxide, respectively. W_{fin}, H_{fin}, and L_{eff} are defined as fin width, fin height, and channel length, respectively. $t_{i,t}$, $t_{i,f}$, $t_{i,b}$, and $t_{ox,u}$ are thicknesses of top gate dielectric, front gate dielectric, back gate dielectric, and buried oxide, respectively. V_{fg}, V_{bg}, V_{tg}, V_{ug} and V_{DS} are the voltage biases of front gate, back gate, top gate, buried gate and drain terminal, respectively. V_{fb} is the flat-band voltage for these gate terminals. ϕ_{ms} is the built-in potential of the source/drain to the channel.

This 3-D boundary value problem can be divided into three sub-problems, including 1-D Poisson's equation, 2-D and 3-D Laplace equation. Using the superposition principle, the complete potential solution is $\phi(x, y, z) = \phi_1(z) + \phi_2(x, z) + \phi_3(x, y, z)$, where $\phi_1(z)$, $\phi_2(x, z)$, and $\phi_3(x, y, z)$ are solutions of the 1-D, 2-D, and 3-D sub-problem, respectively. The 1-D solution $\phi_1(z)$ can be expressed as:

$$\phi_1(z)=-\frac{qN_a}{2\varepsilon_{si}}z^2+az+b \tag{2-3a}$$

$$a=\frac{(V_{tg}-V_{fb})-(V_{ug}-V_{fb})+\frac{qN_a}{2\varepsilon_{si}}\left(H_{fin}{}^2+2\cdot\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,t}H_{fin}\right)}{H_{fin}+\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,t}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox,u}} \tag{2-3b}$$

$$b = \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox,u} a + \left(V_{ug} - V_{fb}\right) \qquad \text{(2-3c)}$$

In solving the 2-D and 3-D sub-problems, approximation was made to avoid the numerical iterations required in finding the eigenvalues [13] and to simplify the solution form. The boundary conditions [Equation (2-2a) to (2-2d)] are simplified by converting the gate dielectric thickness to ($\varepsilon_{si}/\varepsilon_i$) times and replacing the gate dielectric region with an equivalent Si region [14]. The electric field discontinuity across the gate dielectric and Si-fin interface can thus be eliminated. In other words, the Si-fin body and the gate dielectric region are treated as a homogeneous silicon cuboid with an effective width W_{eff} and an effective height H_{eff} given by Equation (2-4) and (2-5), respectively.

$$W_{eff} = W_{fin} + \frac{\varepsilon_{si}}{\varepsilon_i}\left(t_{i,f} + t_{i,b}\right) \qquad \text{(2-4)}$$

$$H_{eff} = H_{fin} + \frac{\varepsilon_{si}}{\varepsilon_i} t_{i,t} + t_{ox,u} \qquad \text{(2-5)}$$

The 2-D solution $\phi_2(x, z)$ can be obtained using the method of separation of variables:

$$\phi_2(x,z) = \sum_{i=1}^{\infty}\left[c_i \sinh\left(\frac{i\pi}{H_{eff}}\left(x + \frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}\right)\right) + c_i' \sinh\left(\frac{i\pi}{H_{eff}}\left(W_{eff} - \left(x + \frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}\right)\right)\right)\right] \cdot \sin\left(\frac{i\pi}{H_{eff}}\left(z + t_{ox,u}\right)\right)$$

(2-6a)

where

$$c_i = \frac{1}{\sinh\left(i\pi \frac{W_{eff}}{H_{eff}}\right)}\left[2\left(V_{fg} - V_{fb} - b\right)\frac{1-(-1)^i}{i\pi} + 2a\left(\frac{t_{ox,u}}{i\pi} + \frac{\left(H_{eff} - t_{ox,u}\right)(-1)^i}{i\pi}\right)\right.$$

$$\left.+ \frac{qN_a}{\varepsilon_{si}}\left(\frac{\left(t_{ox,u}\right)^2}{i\pi} - \frac{\left(H_{eff} - t_{ox,u}\right)^2(-1)^i}{i\pi} + 2H_{eff}{}^2\frac{(-1)^i - 1}{(i\pi)^3}\right)\right] \qquad \text{(2-6b)}$$

$$c_i' = \frac{1}{\sinh\left(i\pi\dfrac{W_{eff}}{H_{eff}}\right)}\Bigg[2\left(V_{bg}-V_{fb}-b\right)\frac{1-(-1)^i}{i\pi}+2a\left(\frac{t_{ox,u}}{i\pi}+\frac{\left(H_{eff}-t_{ox,u}\right)(-1)^i}{i\pi}\right)$$

$$+\frac{qN_a}{\varepsilon_{si}}\left(\frac{\left(t_{ox,u}\right)^2}{i\pi}-\frac{\left(H_{eff}-t_{ox,u}\right)^2(-1)^i}{i\pi}+2H_{eff}{}^2\frac{(-1)^i-1}{(i\pi)^3}\right)\Bigg] \qquad \text{(2-6c)}$$

Similarly, the 3-D solution $\phi_3(x, y, z)$ can also be obtained and expressed as

$$\phi_3(x,y,z)=\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\left[e_{m,n}\sinh\left(k_y y\right)+e'_{m,n}\sinh\left(k_y\left(L_{eff}-y\right)\right)\right]\cdot\sin\left(\frac{m\pi}{W_{eff}}\left(x+\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)\right)\cdot\sin\left(\frac{n\pi}{H_{eff}}\left(z+t_{ox,u}\right)\right)$$

(2-7a)

where

$$k_y=\sqrt{\left(\frac{m\pi}{W_{eff}}\right)^2+\left(\frac{n\pi}{H_{eff}}\right)^2} \qquad \text{(2-7b)}$$

$$e_{m,n}=\frac{1}{\sin\left(k_y L_{eff}\right)}\Bigg\{\Bigg[\bigg[\left(-\phi_{ms}+V_{DS}-b\right)\cdot\frac{1-(-1)^m}{m\pi}+\frac{qN_a}{2\varepsilon_{si}}\Bigg(-\frac{\left(W_{eff}-\dfrac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)^2(-1)^m-\left(\dfrac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)^2}{m\pi}+\frac{2W_{eff}{}^2\left((-1)^m-1\right)}{(m\pi)^3}\Bigg)$$

$$+a\left(\frac{\left(W_{eff}-\dfrac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)(-1)^m+\dfrac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}}{m\pi}\right)\bigg]\Bigg]\cdot\frac{4\cdot\left(1-(-1)^n\right)}{n\pi}+2c_m\frac{\dfrac{(-1)^n}{n\pi}\sinh\left(m\pi\dfrac{H_{eff}}{W_{eff}}\right)}{1+\left(\dfrac{m}{n}\dfrac{H_{eff}}{W_{eff}}\right)^2}-2c_m'\frac{\dfrac{1}{n\pi}\sinh\left(m\pi\dfrac{H_{eff}}{W_{eff}}\right)}{1+\left(\dfrac{m}{n}\dfrac{H_{eff}}{W_{eff}}\right)^2}\Bigg\}$$

(2-7c)

$$e'_{m,n}=\frac{1}{\sin\left(k_y L_{eff}\right)}\Bigg\{\Bigg[\bigg[\left(-\phi_{ms}-b\right)\cdot\frac{1-(-1)^m}{m\pi}+\frac{qN_a}{2\varepsilon_{si}}\Bigg(-\frac{\left(W_{eff}-\dfrac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)^2(-1)^m-\left(\dfrac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)^2}{m\pi}+\frac{2W_{eff}{}^2\left((-1)^m-1\right)}{(m\pi)^3}\Bigg)$$

$$+a\left(\frac{\left(W_{eff}-\dfrac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)(-1)^m+\dfrac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}}{m\pi}\right)\bigg]\Bigg]\cdot\frac{4\cdot\left(1-(-1)^n\right)}{n\pi}+2c_m\frac{\dfrac{(-1)^n}{n\pi}\sinh\left(m\pi\dfrac{H_{eff}}{W_{eff}}\right)}{1+\left(\dfrac{m}{n}\dfrac{H_{eff}}{W_{eff}}\right)^2}-2c_m'\frac{\dfrac{1}{n\pi}\sinh\left(m\pi\dfrac{H_{eff}}{W_{eff}}\right)}{1+\left(\dfrac{m}{n}\dfrac{H_{eff}}{W_{eff}}\right)^2}\Bigg\}$$

(2-7d)

Our potential solution has been verified by 3-D device simulation [15]. Figure 2-2(a) and (b) compare the derived channel potential distribution with device simulation (at $V_{GS} = -0.2V$) for heavily doped devices and lightly doped devices, respectively. Note that a smaller EOT is used in the lightly-doped case to sustain the electrostatic integrity [3]. It can be seen that our model shows satisfactory accuracy.

2.2.2 Analytical Channel Potential Solution for GAA Structure

For GAA structure, the cylindrical channel is wrapped by gate insulator and connected to the gate terminal. Since the GAA structure is symmetrical in the θ-direction (Figure 2-3), the 2-D potential distribution $\phi(r, y)$ satisfies the 2-D Poisson's equation:

$$\frac{\partial^2 \phi(r,y)}{\partial r^2} + \frac{1}{r}\frac{\partial \phi(r,y)}{\partial r} + \frac{\partial^2 \phi(r,y)}{\partial y^2} = -\frac{qN_a}{\varepsilon_{si}} \qquad (2\text{-}8)$$

The boundary conditions for GAA MOSFETs are

$$\left.\frac{\partial \phi(r,y)}{\partial r}\right|_{r=0} = 0 \qquad (2\text{-}9a)$$

$$\varepsilon_{si} \cdot \left.\frac{\partial \phi(r,y)}{\partial r}\right|_{r=D/2} = C_i \cdot \left[V_{GS} - V_{fb} - \phi(r = D/2, y)\right] \qquad (2\text{-}9b)$$

$$C_i = 2\varepsilon_i / \left[D \cdot \ln(1 + 2t_i / D)\right] \qquad (2\text{-}9c)$$

$$\phi(r, y = 0) = -\phi_{ms} \qquad (2\text{-}9d)$$

$$\phi(r, y = L_{eff}) = -\phi_{ms} + V_{DS} \qquad (2\text{-}9e)$$

where D and t_i are the channel diameter and thickness of gate insulator, respectively. Note that

Equation (2-9c) is the capacitance per unit length for an infinite long cylindrical capacitor, which neglects the fringing effect of the field near the edges of the capacitor [16].

Similar to the procedure used in the multi-gate structure, this 2-D boundary value problem can be divided into two sub-problems, including 1-D Poisson's equation and 2-D Laplace equation. Using the superposition principle, the complete potential solution is $\phi(r, y) = \phi_1(r) + \phi_2(r, y)$, where $\phi_1(r)$ and $\phi_2(r, y)$ are solutions of the 1-D and 2-D sub-problems, respectively. Solving the boundary value problem in cylindrical coordinate [17], the solution can be expressed as

$$\phi_1(r) = Ar^2 + B \qquad \text{(2-10a)}$$

where

$$A = -\frac{qN_a}{4\varepsilon_{si}} \qquad \text{(2-10b)}$$

$$B = V_{GS} - V_{fb} + \frac{qN_a}{\varepsilon_{si}}\frac{D}{2}\left(\frac{D}{2} + 2\frac{\varepsilon_{si}}{C_i}\right) \qquad \text{(2-10c)}$$

$$\phi_2(r, z) = \sum_n \left[k_n \cdot \sinh(\lambda_n \cdot y) + k_n' \cdot \sinh\left(\lambda_n\left(L_{eff} - y\right)\right)\right] \cdot J_0(\lambda_n \cdot r) \qquad \text{(2-11)}$$

where $J_v(x)$ is called Bessel function of the first kind of order v [17]. λ_n can be determined by

$$J_0\left(\lambda_n \frac{D}{2}\right) - \frac{\varepsilon_{si}}{C_i}\lambda_n J_1\left(\lambda_n \frac{D}{2}\right) = 0 \qquad \text{(2-12)}$$

The coefficients k_n and k_n' can be expressed as

$$k_n = \frac{2}{\left[\left(\frac{C_i}{\lambda_n \varepsilon_{si}}\right)^2 + 1\right] \cdot J_0^{\,2}\left(\lambda_n \frac{D}{2}\right) \cdot \sinh\left(\lambda_n L_{eff}\right)} \cdot$$

$$\left\{-A \cdot \left[\frac{1}{\lambda_n}\left(\frac{D}{2}\right)^3 \cdot J_1\left(\lambda_n \frac{D}{2}\right) - 2\left(\frac{1}{\lambda_n}\right)^2\left(\frac{D}{2}\right)^2 \cdot J_2\left(\lambda_n \frac{D}{2}\right)\right] + \left(V_{DS} - \phi_{ms} - B\right)\frac{1}{\lambda_n}\frac{D}{2} \cdot J_1\left(\lambda_n \frac{D}{2}\right)\right\}$$

(2-13a)

$$k'_n = \frac{2}{\left[\left(\frac{C_i}{\lambda_n \varepsilon_{si}}\right)^2 + 1\right] \cdot J_0^{\,2}\left(\lambda_n \frac{D}{2}\right) \cdot \sinh\left(\lambda_n L_{eff}\right)} \cdot$$

$$\left\{ -A \cdot \left[\frac{1}{\lambda_n}\left(\frac{D}{2}\right)^3 \cdot J_1\left(\lambda_n \frac{D}{2}\right) - 2\left(\frac{1}{\lambda_n}\right)^2 \left(\frac{D}{2}\right)^2 \cdot J_2\left(\lambda_n \frac{D}{2}\right) \right] + \left(-\phi_{ms} - B\right) \frac{1}{\lambda_n} \frac{D}{2} \cdot J_1\left(\lambda_n \frac{D}{2}\right) \right\} \quad (2\text{-}13b)$$

Figure 2-4 compares the derived channel potential distribution with 3-D device simulation for both lightly doped ($1\times10^{15}\text{cm}^{-3}$) and heavily doped ($3\times10^{18}\text{cm}^{-3}$) GAA devices. It can be seen that our model shows satisfactory accuracy for various channel doping.

2.2.3 Modeling of Subthreshold Current and V_{th} Using the Channel Potential Solution

The subthreshold current can be derived using the channel potential solution. For example, the current density $J_n(r, y)$ of a GAA device at the position (r, y) can be expressed as [18]:

$$J_n(r,y) = -q\mu_n n(r,y) \cdot \frac{dV(y)}{dy} = -q\mu_n \cdot \frac{n_i^2}{N_a} \exp\left[\frac{\phi(r,y) - V(y)}{kT/q}\right] \cdot \frac{dV(y)}{dy} \qquad (2\text{-}14)$$

where $n(r, y)$ is the electron density at the position (r, y) and $V(y)$ is the quasi-Fermi potential. μ_n is the carrier mobility. The current I_{DS} (y) can be derived by integrating in r and θ directions:

$$I_{DS}(y) = -q\mu_n \left\{ -2\pi \int_0^{D/2} r \cdot \frac{n_i^{\,2}}{N_a} \exp\left[\frac{\phi(r,y) - V(y)}{kT/q}\right] dr \right\} \cdot \frac{dV(y)}{dy} \qquad (2\text{-}15)$$

Since the electron current flow is continuous, the subthreshold current I_{DS} is independent of y and can obtained by

$$I_{DS}=\frac{q\mu_n(kT/q)\left(n_i^2/N_a\right)\left[1-\exp\left(-V_{DS}/(kT/q)\right)\right]}{\int_0^{L_{eff}}dy\Big/\left[2\pi\int_0^{D/2}r\cdot\exp[\phi(r,y)/(kT/q)]dr\right]} \qquad (2\text{-}16)$$

Since the derivation procedure of I_{DS} for multi-gate structure is similar, the expression of I_{DS} for multi-gate structure is similar to Equation (2-16) except for the integral term in the denominator. For multi-gate structure,

$$I_{DS}=\frac{q\mu_n(kT/q)\left(n_i^2/N_a\right)\left[1-\exp\left(-V_{DS}/(kT/q)\right)\right]}{\int_0^{L_{eff}}dy\Big/\left[\int_0^{H_{fin}}\int_0^{W_{fin}}\exp[\phi(x,y,z)/(kT/q)]dxdz\right]} \qquad (2\text{-}17)$$

The subthreshold current derived by Equation (2-16) and (2-17) has been verified by 3-D device simulation. Figure 2-5(a) and (b) compares the derived subthreshold current with device simulation for heavily doped devices and lightly doped devices, respectively. Besides, we define the V_{th} as the gate voltage at which the calculated subthreshold current I_{DS} = 300nA × W_{total}/L_{eff} [19], where W_{total} is the total width. For multi-gate structure, $W_{total} = 2H_{fin}+W_{fin}$ and for GAA structure, $W_{total} = \pi\cdot D$. Since our calculated subthreshold current is applicable for the subthreshold regime, we focus on the accuracy for V_{GS} below V_{th}. For heavily doped devices [Figure 2-5(a)], the V_{th} is around 0.4V and for lightly doped case [Figure 2-5(b)] the V_{th} is around 0.2V. It can be seen that our model shows satisfactory accuracy.

Compared with the TCAD device simulation, our methodology shows higher efficiency in determining the subthreshold current and V_{th} of multi-gate and GAA devices. In our calculation, the CPU time needed is less than 20% of that needed for TCAD simulation. More importantly, this theoretical framework provides more scalable and predictive results than experimental or TCAD simulation does.

2.3 Impact of Aspect Ratio on Random Dopant Fluctuation for Multi-Gate MOSFETs

With the scaling of device geometry, random dopant fluctuation (RDF) has become a crucial issue to device design. In this section, we compare the V_{th} dispersion caused by RDF for FinFET, Tri-gate and Quasi-planar devices with both heavily doped and lightly doped channels [20]. Through our theoretical model, the impact of device aspect ratio on the random dopant fluctuation in multi-gate MOSFETs is examined.

Although the actual 3-D charge distribution is not uniform, we can incorporate the dopant number fluctuation in our theoretical framework to assess the feasibility of various multi-gate device designs. The dopant number in the channel has been found to follow Poisson distribution [21] and the V_{th} distribution caused by random dopant fluctuation can be approximated as Gaussian distribution [21]-[23]. With MOSFET scaling, the V_{th} distribution gradually changes its shape from the Gaussian to a Poisson-like distribution [23]. To assess the V_{th} variation of multi-gate devices caused by dopant number fluctuation, we assume that the dopant number in the channel follows Poisson distribution [23], [24] and the standard deviation (σ) of the dopant number is $n_a^{1/2}$, where n_a is the average dopant number in the Si-body. The V_{th} variation for dopant number fluctuation can then be calculated as $\Delta V_{th}=|V_{th}(+3\sigma)-V_{th}(-3\sigma)|/2$.

To compare the multi-gate devices with various aspect ratio ($AR=H_{fin}/W_{fin}$), we focus on the FinFET (AR=2), Tri-gate (AR=1), and Quasi-planar (AR=0.5) structures (Figure 2-6). The total width ($W_{total}=2H_{fin}+W_{fin}$) of various AR devices are all equal to 75nm to make fair comparison. Besides heavily doped devices, we also examined the impact of RDF on the V_{th} dispersion of lightly doped devices. For heavily doped devices, the channel doping is equal to $6\times10^{18}cm^{-3}$. For lightly doped channel the channel doping is $1\times10^{17}cm^{-3}$. Note that gate oxide (t_{ox}=1nm) is used for heavily doped devices, while high-k dielectric (t_{HfO2}=2nm and the dielectric constant of HfO_2 is 25) is used for lightly doped ones to sustain the device electrostatics [3].

Figure 2-7 shows the AR dependence of ΔV_{th} caused by RDF, and the results are verified with device simulation [15]. For heavily doped channel, the ΔV_{th} increases with AR, and the minimum ΔV_{th} occurs at AR=0.5, i.e., Quasi-planar device. This is because for a given W_{total}, the devices with AR=0.5 possess the largest channel volume (Figure 2-8). Since

$$\Delta V_{th} = \frac{dV_{th}}{dN_a} \cdot \Delta N_a \qquad (2\text{-}18)$$

$$\Delta N_a = \frac{\Delta n_a}{V} \propto \frac{\sqrt{n_a}}{V} = \frac{\sqrt{N_a \cdot V}}{V} = \frac{\sqrt{N_a}}{\sqrt{V}} \qquad (2\text{-}19)$$

where V is the channel volume, the devices with larger channel volume show smaller ΔV_{th}. In addition to channel volume, Equation (2-18) demonstrates that the V_{th} sensitivity to the channel doping (dV_{th}/dN_a) may also determine the ΔV_{th}. Figure 2-9 shows the channel doping dependence of V_{th} for devices with heavily doped channel. It can be seen that FinFET, Tri-gate and Quasi-planar devices show similar V_{th} sensitivity. Therefore, for heavily doped channel, Quasi-planar device shows better immunity to RDF than FinFET and Tri-gate because of its larger channel volume.

Figure 2-10 shows that for lightly doped channel, the ΔV_{th} increases as AR decreases. This is because for lightly doped channel, devices with different AR show different V_{th} sensitivity to channel doping (Figure 2-11). For lightly doped channel, FinFET shows the smallest V_{th} sensitivity to channel doping because of its narrower W_{fin} for a given W_{total}. In other words, W_{fin} scaling enhances the gate control and reduces the V_{th} dependence on the channel doping. Therefore, FinFET shows the best immunity to dopant fluctuation for lightly doped channel.

To assess the impact of random dopant fluctuation on the overall V_{th} variation, we have calculated the proportion of V_{th} dispersion due to random dopant fluctuation to the overall V_{th} variation (Figure 2-12). The ΔV_{th} caused by L_{eff} variation ($\Delta V_{th,Leff}$), W_{fin} variation ($\Delta V_{th,Wfin}$), H_{fin} variation ($\Delta V_{th,Hfin}$) and random dopant fluctuation ($\Delta V_{th,RDF}$) are considered in our calculation. We assume that the 3σ process variations of these device parameters are ±10% of their nominal values, and the V_{th} variation is defined as $\Delta V_{th}=|V_{th}(+10\%)-V_{th}(-10\%)|/2$ [24]. The overall V_{th} variation is defined as $\Delta V_{th}^2 = \Delta V_{th,Leff}^2 + \Delta V_{th,Wfin}^2 + \Delta V_{th,Hfin}^2 + \Delta V_{th,RDF}^2$. Figure 2-12(a) shows that for heavily doped channel, random dopant fluctuation dominates the overall V_{th} dispersion and the Quasi-planar device shows better immunity than devices with other AR to dopant fluctuation. Our theoretical result is consistent with the experimental data from [25], which showed that for doped channel, the σV_{th} of the devices with smaller volume is larger than that of the devices with larger volume. Although lightly doped channel has been suggested [26] to suppress the V_{th} variation caused by dopant fluctuation, Figure 2-12(b) shows that the V_{th} variation caused by dopant fluctuation is still significant for lightly-doped Tri-gate and Quasi-planar devices. The impact of RDF may still be an issue to the V_{th} dispersion of lightly doped channel unless devices with good electrostatic integrity such as FinFET are used.

2.4 Sensitivity of GAA MOSFETs to Process Variations – A Comparison with Multi-Gate MOSFETs

To assess the sensitivity of GAA and multi-gate MOSFETs to process variations, we assume that the device parameters such as L_{eff}, channel diameter (*D*) of GAA structure, and W_{fin} of multi-gate MOSFETs vary by ±2.5nm (±3σ value, σ is the standard deviation) [26]. This 3σ value is estimated from the combination of process variations such as lithography variation, etch variation, and resist trim variation [26]. Similar to the previous section, the impact of dopant number fluctuation is considered assume that the channel dopant number follows the Poisson distribution and the σ of the dopant number is $n_a^{1/2}$, where n_a is the average dopant number in the Si-channel. The corresponding V_{th} variation for process variations and dopant number fluctuation can be calculated as $\Delta V_{th} = [V_{th}(+3\sigma)-V_{th}(-3\sigma)]/2$

[24].

To compare the GAA structure with multi-gate MOSFETs, the total width (W_{total}) of GAA ($W_{total} = \pi \cdot D$) and multi-gate MOSFETs ($W_{total} = 2H_{fin} + W_{fin}$) are equal to make fair comparison. Multi-gate structures with various ARs (AR = H_{fin} / W_{fin}) are considered, including FinFET (AR = 2) and Tri-gate (AR = 1). Devices with various channel doping are considered. For heavily doped devices, the channel doping is equal to 6×10^{18}cm^{-3}. For lightly doped devices, the channel doping is equal to 1×10^{17}cm^{-3}.

Figure 2-13 shows the calculated ΔV_{th} caused by dopant number fluctuation ($\Delta V_{th,RDF}$) for W_{total} = 75nm and L_{eff} = 25nm, and the results are verified with device simulation [15]. The $\Delta V_{th,RDF}$ for heavily-doped GAA device is larger than that of multi-gate MOSFETs. This is because for a given total width, GAA device possesses smaller channel volume than FinFET and Tri-gate. Besides, it can seen that for heavily doped channel, the $\Delta V_{th,RDF}$ is significantly larger than that of lightly doped ones. The V_{th} dispersion due to dopant number fluctuation is a crucial concern for heavily doped device design.

Figure 2-14 shows the calculated ΔV_{th} caused by L_{eff} variation ($\Delta V_{th,Leff}$) for W_{total} = 75nm and L_{eff} = 25nm. The discrepancies of $\Delta V_{th,Leff}$ for heavily doped devices are not significant. For lightly doped channel, the $\Delta V_{th,Leff}$ of GAA device is also close to that of FinFET. However, the $\Delta V_{th,Leff}$ of GAA device is much smaller that that of Tri-gate. The $\Delta V_{th,Leff}$ is determined by the V_{th} roll-off characteristics. Figure 2-15(a) demonstrates that for heavily doped channel, the V_{th} roll-off of the three devices are similar because channel doping reduces the geometry dependence of electrostatic integrity. In Figure 2-15(b), the V_{th} roll-off of lightly doped GAA MOSFET is close to that of lightly doped FinFET. Since W_{fin} scaling is more effective than H_{fin} scaling in the suppression of V_{th} roll-off, especially for lightly doped case, the V_{th} variation for narrower W_{fin} devices like FinFET is smaller than Tri-gate.

Figure 2-16 shows the calculated ΔV_{th} caused by channel thickness (t_{si}) variation ($\Delta V_{th,tsi}$)

for W_{total} = 75nm and L_{eff} = 25nm. W_{fin} variation and Diameter variation are considered for multi-gate MOSFETs and GAA devices, respectively. It can be seen that for heavily doped case, the ΔV_{th} of FinFET is larger than that of Tri-gate. For lightly doped case, however, the ΔV_{th} of Tri-gate is significantly larger than that of FinFET. This can be explained by the W_{fin} dependence of V_{th}. Figure 2-17(a) shows that for heavily doped devices, the V_{th} decreases with W_{fin} because of the reverse narrow width effect. Also shown in Figure 2-17(a) is that the V_{th} sensitivity to W_{fin}, $|dV_{th}/dW_{fin}|$, is larger for devices with narrower W_{fin}. Therefore, FinFET with its inherently narrower W_{fin} shows larger ΔV_{th} as W_{fin} varies. Figure 2-17(b) shows that for lightly doped devices, the V_{th} increases as W_{fin} decreases because of smaller V_{th} roll-off in narrower devices. Also shown in Figure 2-17(b) is that the V_{th} sensitivity to W_{fin} is larger for devices with wider W_{fin}. Therefore, Tri-gate with its inherently wider W_{fin} shows larger ΔV_{th} as W_{fin} varies.

Figure 2-16 shows that for lightly doped channel, the $\Delta V_{th,tsi}$ of GAA device is smaller than that of multi-gate MOSFETs. This is because the surrounding gate structure of GAA device reduces the channel thickness dependence of V_{th}. Figure 2-18 shows that the GAA structure with a square cross section (which possesses the same channel volume as cylindrical GAA structure) shows similar V_{th} sensitivity (dV_{th}/dW_{fin}) as that (dV_{th}/dD) of the cylindrical GAA structure. Although multi-gate structures with higher AR can be used to improve the immunity to W_{fin} variation, Figure 2-19 shows that with the scaling of W_{total}, the $\Delta V_{th,tsi}$ of GAA device decreases more rapidly than that of FinFET.

To assess the overall V_{th} variation ($\Delta V_{th,total}$) for GAA device and multi-gate devices, we assume that the variation sources such as dopant number fluctuation, L_{eff} variation, and channel thickness variation are independent. The overall V_{th} variation can then be calculated as $\Delta V_{th,total}^2 = \Delta V_{th,RDF}^2 + \Delta V_{th,Leff}^2 + \Delta V_{th,tsi}^2$. Figure 2-20 compares the calculated $\Delta V_{th,total}^2$ of GAA device and AR = 2 FinFET for W_{total} = 75nm and L_{eff} = 25nm. For heavily doped channel, dopant number fluctuation dominates the overall V_{th} dispersion, and the $\Delta V_{th,total}$ of GAA device is larger than that of FinFET because of its smaller channel volume. For lightly doped channel, process-induced geometry variations dominate the overall V_{th} dispersion, and the $\Delta V_{th,total}$ of GAA device is smaller than that of FinFET because of its better immunity to channel thickness variation.

2.5 Summary

In this chapter, we compare the sensitivity of threshold voltage to process variations for multi-gate devices with various aspect ratio and GAA device using analytical solutions of 3-D Poisson’s equation verified with device simulation. Our study indicates that lightly doped GAA device shows the smallest V_{th} variation caused by process variation and dopant number fluctuation. Especially, GAA device shows better immunity to channel thickness variation than multi-gate structure because of its inherently superior surrounding gate structure. For heavily doped devices, dopant number fluctuation may become the dominant factor in the determination of overall V_{th} variation. The V_{th} dispersion of GAA device may therefore be larger than that of multi-gate MOSFETs because of its larger surface-to-volume ratio. We also analyze the impact of aspect ratio on the V_{th} dispersion due to dopant number fluctuation for multi-gate MOSFETs. For heavily doped channel, Quasi-planar device shows smaller V_{th} dispersion because of its larger channel volume. The V_{th} dispersion due to random dopant fluctuation may still be significant in the lightly doped channel, especially for Tri-gate and Quasi-planar devices because of the larger V_{th} sensitivity to the channel doping.

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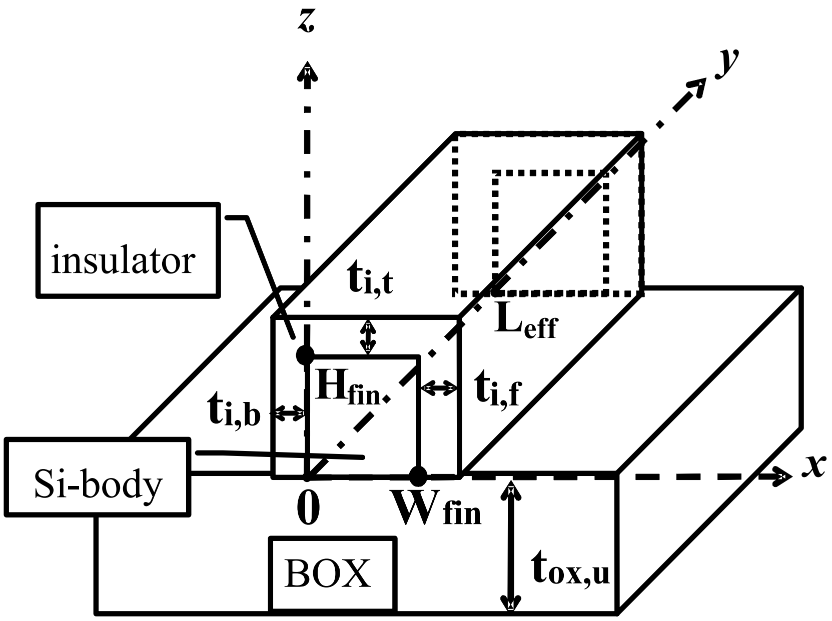
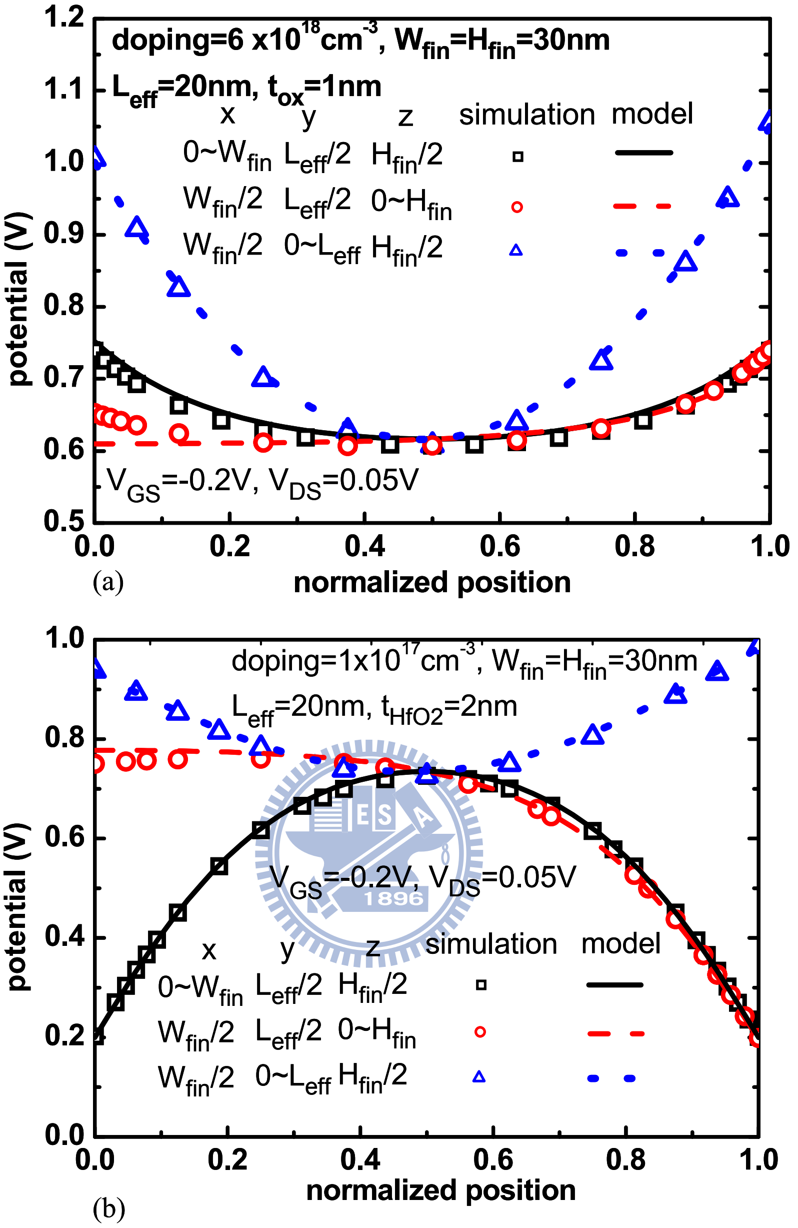


Figure 2-1 Schematic sketch of the multi-gate device structure investigated in this study.



(a)

(b)

Figure 2-2 Analytical potential distribution compared with the result of 3-D device simulation. For the lightly doped case, a midgap workfunction is used (4.7eV).

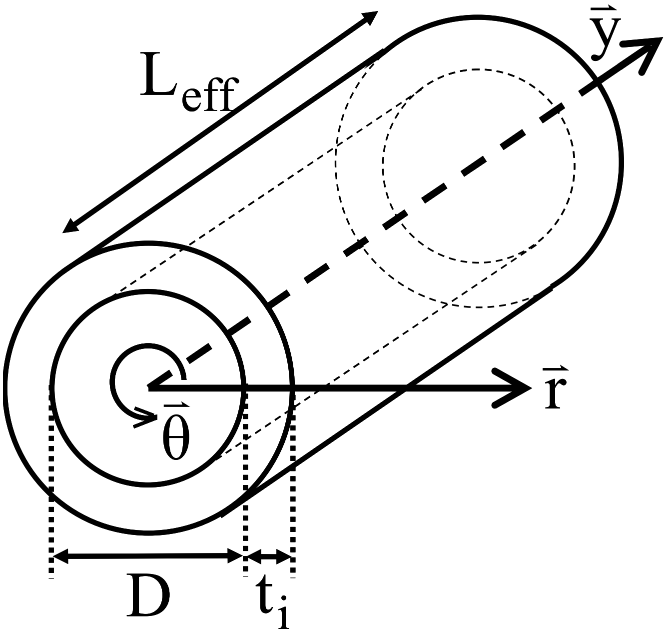


Figure 2-3 The schematic sketch of cylindrical GAA structure investigated in this study. The origin ($r = 0$, $y = 0$) is defined at the center of the channel/source junction.

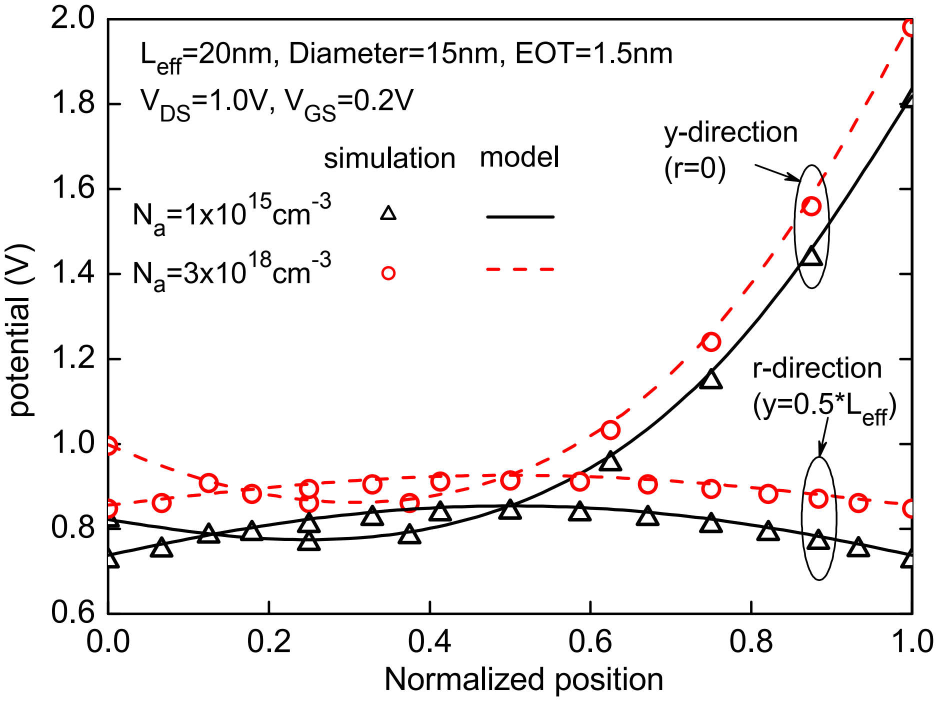
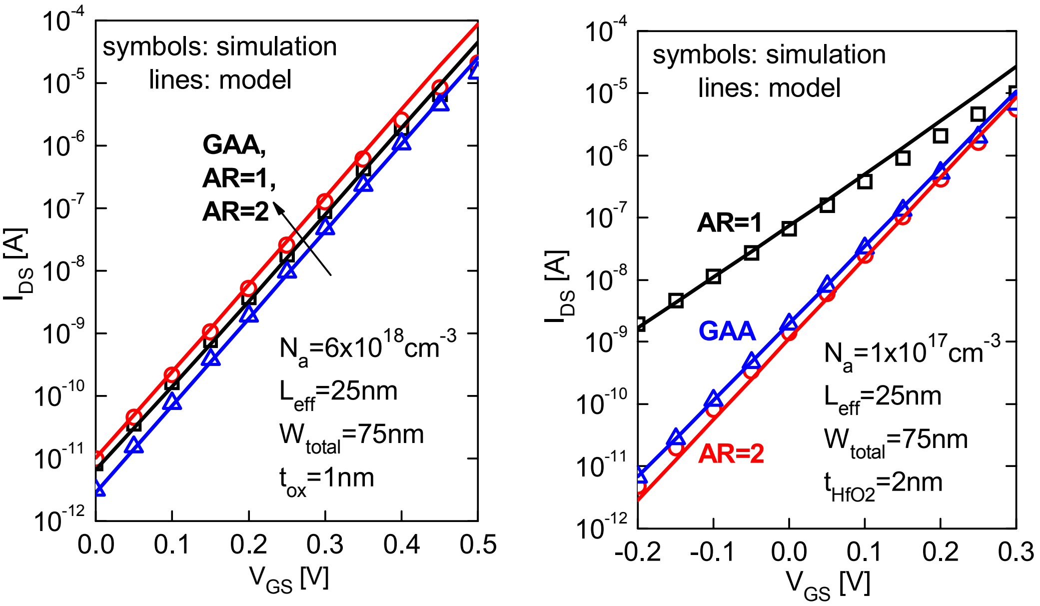


Figure 2-4 Analytical potential distribution compared with the result of 3-D ISE simulation. A midgap workfunction is used (4.5eV).



(a) (b)

Figure 2-5 The calculated subthreshold current compared with the result of 3-D device simulation. (a) Heavily doped channel. (b) Lightly doped channel with high-k dielectric (the dielectric constant of HfO_2 is 25). A midgap workfunction is given for both heavily and lightly doped devices (4.5eV).

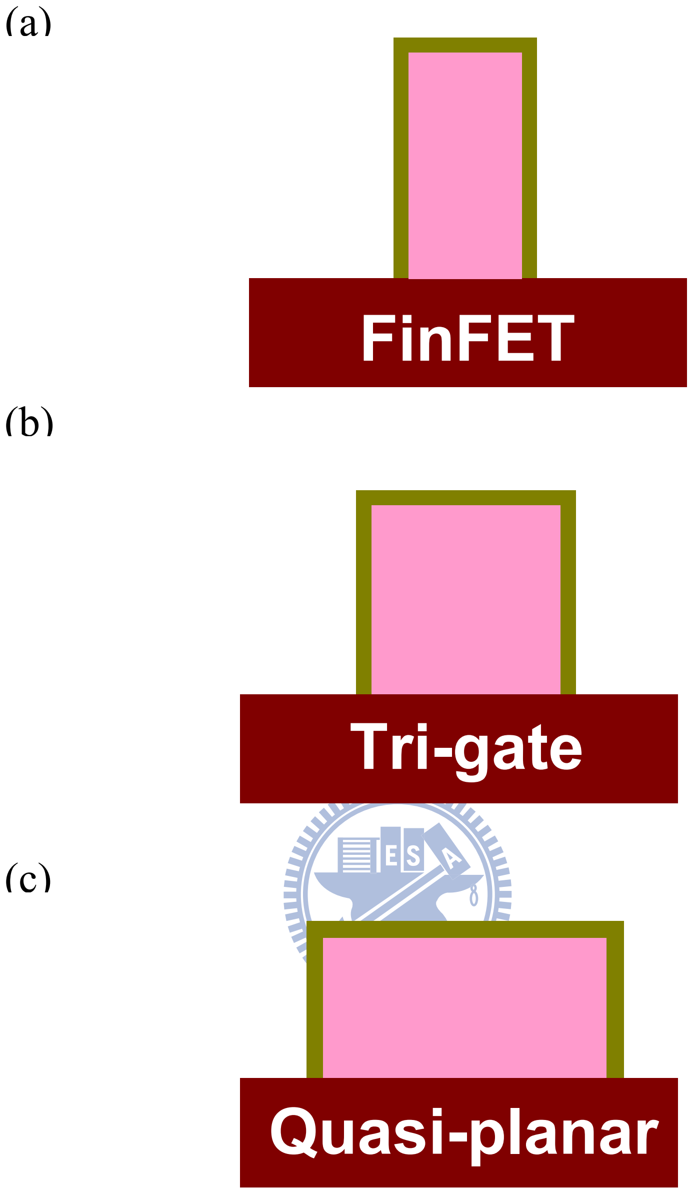


Figure 2-6 Illustration of three different AR devices for a given total width: (a) FinFET (AR=2), (b) Tri-gate (AR=1) and (c) Quasi-Planar device (AR=0.5).

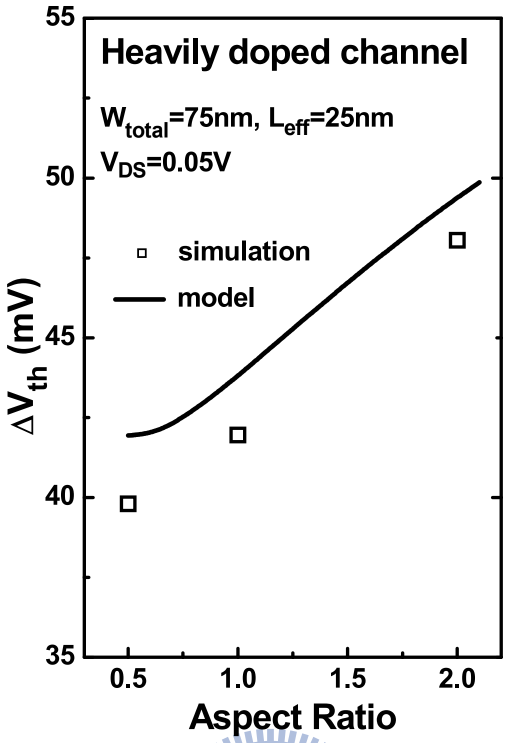


Figure 2-7 The AR dependence of ΔV_{th} caused by random dopant fluctuation in the heavily doped channel.

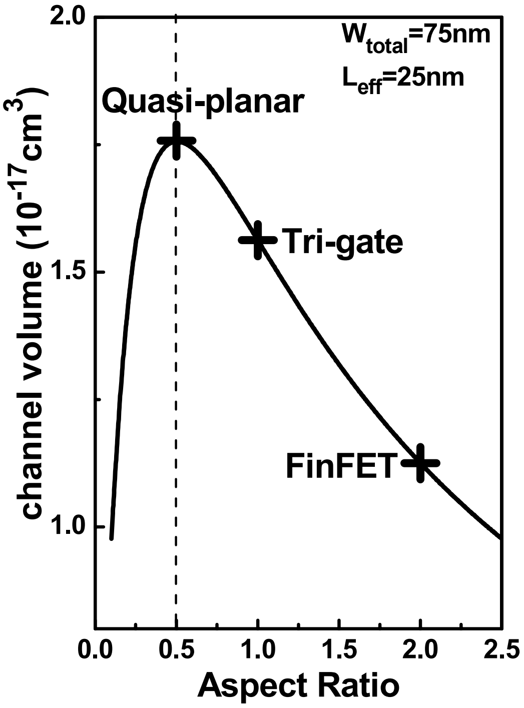


Figure 2-8 For a given total width, devices with AR=0.5 possess the largest channel volume. Devices with larger volume will show less doping variation caused by random dopant fluctuation.

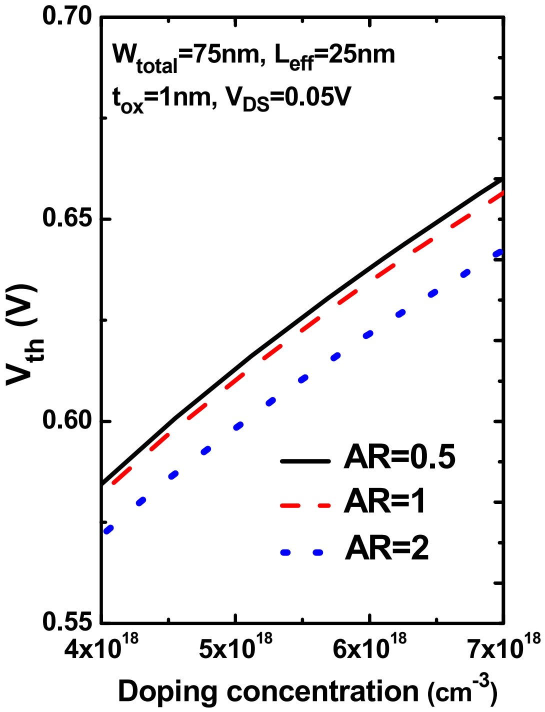


Figure 2-9 Model prediction of the doping dependence of V_{th} for heavily doped channel with the same total width.

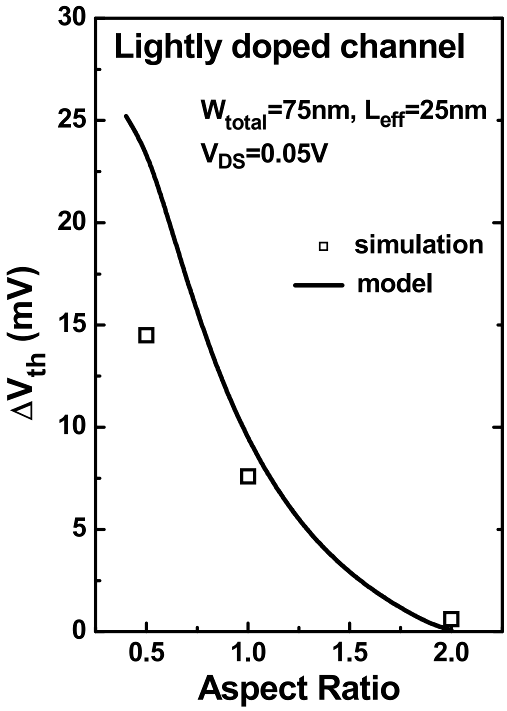


Figure 2-10 The AR dependence of ΔV_{th} caused by dopant number fluctuation in the lightly doped channel.

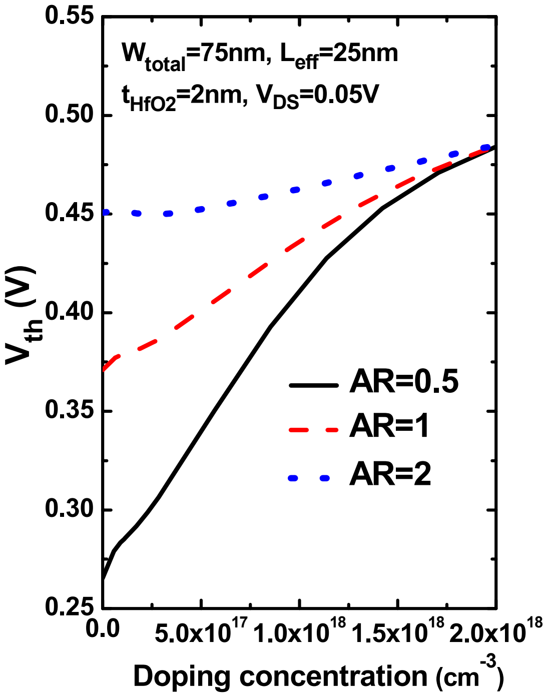


Figure 2-11 Model prediction of the doping dependence of V_{th} for lightly doped channel with the same total width.

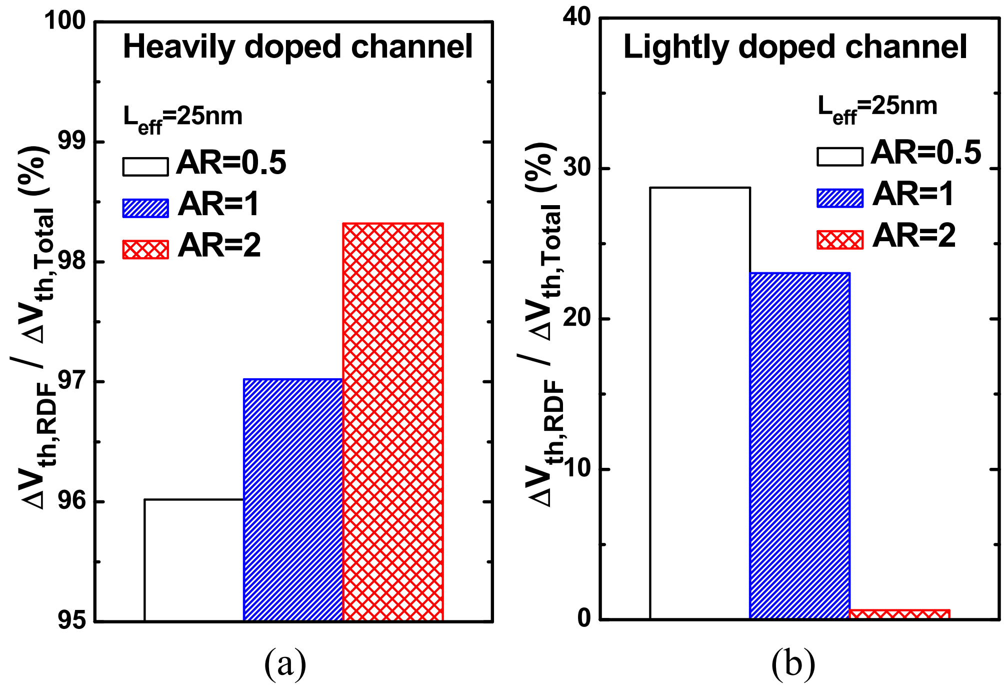


Figure 2-12 The proportional of the ΔV_{th} caused by dopant number fluctuation to the overall ΔV_{th} for (a) heavily doped channel and (b) lightly doped channel.

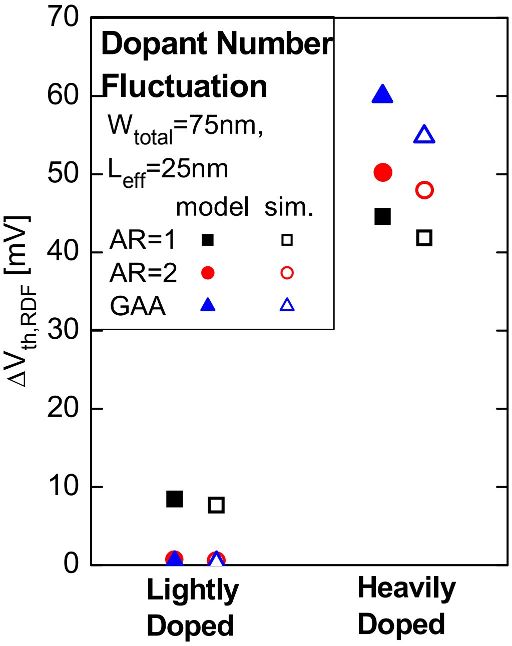


Figure 2-13 Comparison of ΔV_{th} caused by dopant number fluctuation ($\Delta V_{th,RDF}$) between GAA device and multi-gate MOSFETs (AR = 1 and 2). Both heavily doped and lightly doped channels are considered.

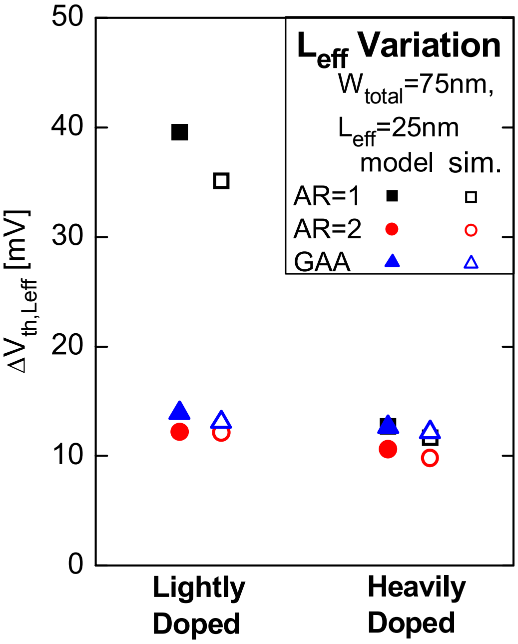


Figure 2-14 Comparison of ΔV_{th} caused by L_{eff} variation ($\Delta V_{th,Leff}$) between GAA NW and multi-gate MOSFETs (AR = 1 and 2).

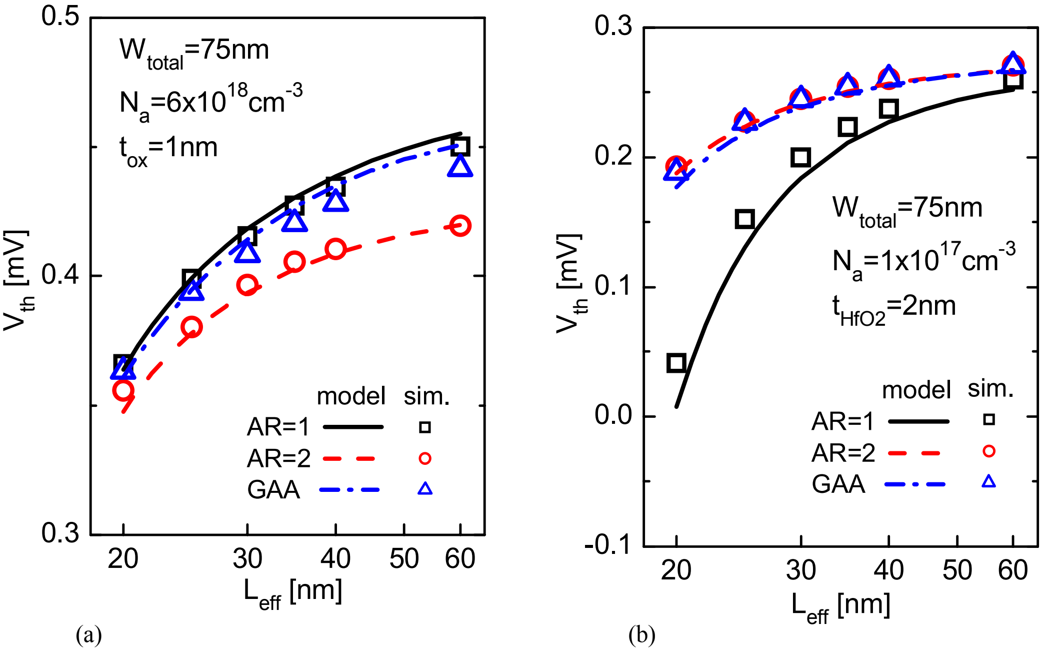


Figure 2-15 The V_{th} roll-off behaviors of GAA device and multi-gate MOSFETs (AR = 1 and 2). (a) Heavily doped channel. (b) Lightly doped channel with high *k* dielectric.

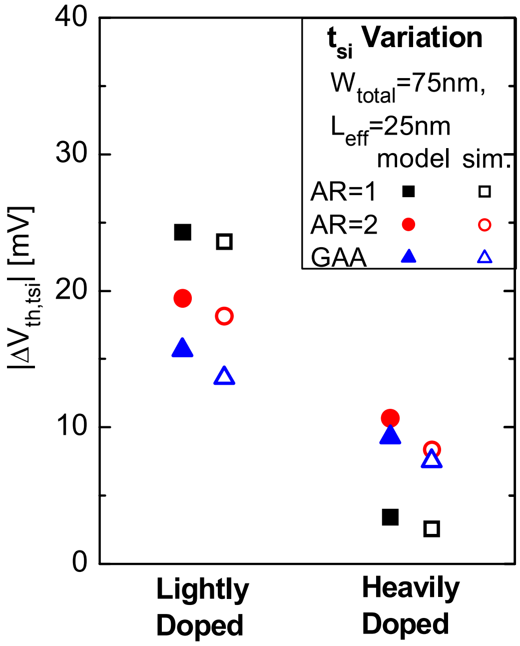


Figure 2-16 Comparison of ΔV_{th} caused by channel thickness (t_{si}) variation ($\Delta V_{th,tsi}$) between GAA NW and multi-gate MOSFETs (AR = 1 and 2). W_{fin} variation and Diameter variation are considered for multi-gate MOSFETs and GAA NW, respectively.

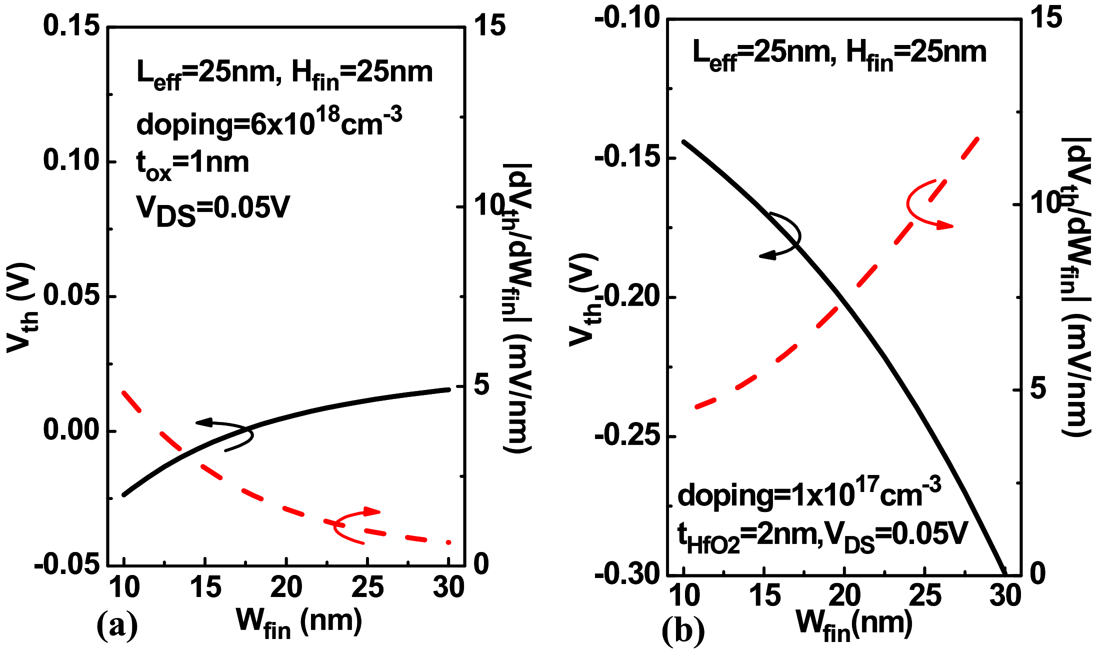


Figure 2-17 The W_{fin} dependence of V_{th} and $|dV_{th}/dW_{fin}|$ for (a) heavily doped and (b) lightly doped multi-gate devices.

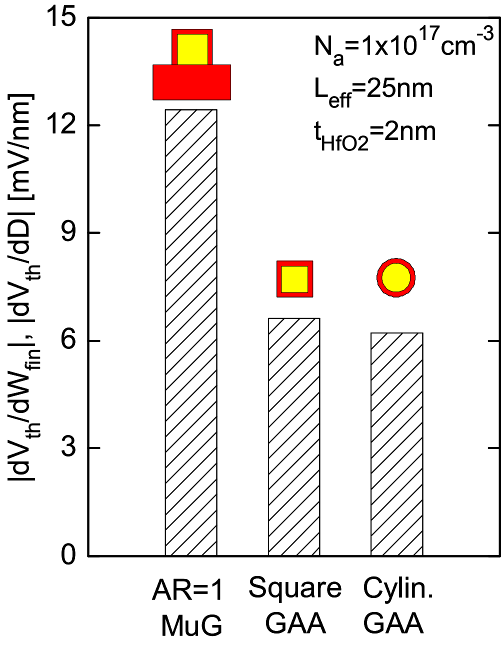


Figure 2-18 Comparison of V_{th} sensitivity to channel thickness for Tri-gate (AR = 1), GAA structure with a square cross section, and cylindrical GAA NW.

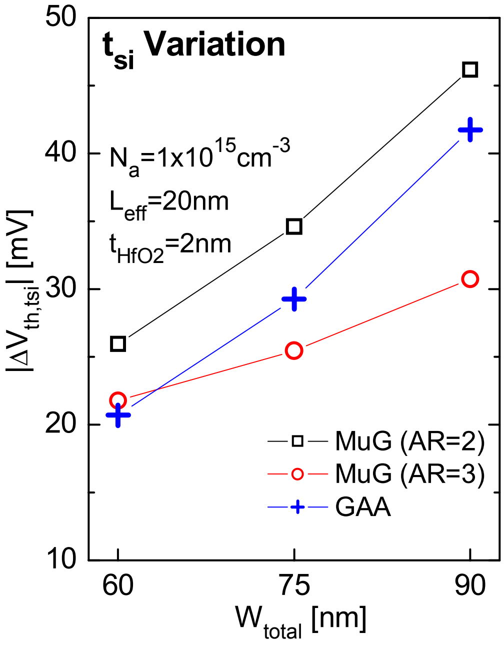
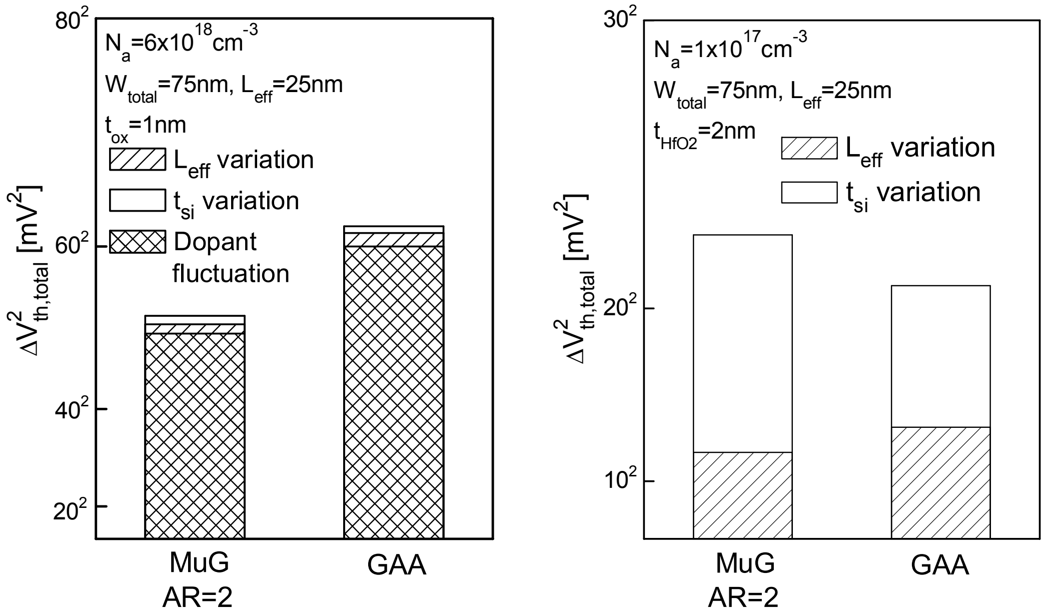


Figure 2-19 Model prediction of $\Delta V_{th,tsi}$ dependence on total width (W_{total}) for lightly doped GAA NW and FinFET (AR = 2 and AR = 3).



(a) (b)

Figure 2-20 Comparison of overall V_{th} variation ($\Delta V_{th,total}$) between GAA NW and AR = 2 FinFET. (a) Heavily doped channel. (b) Lightly doped channel with high *k* dielectric.

Chapter 3

Impact of Quantum Confinement Effects on the Sensitivity of FinFET and GAA MOSFETs to Process Variations

3.1 Introduction

In Chapter 2, we have assessed the V_{th} sensitivity to process variations using analytical solutions of Poisson's equation. With the scaling of device geometry, however, the quantum-confinement effect becomes significant [1], [2] and results in carrier reduction and hence the V_{th} shift. Therefore, the quantum-confinement effect may impact the sensitivity of V_{th} to process variations [3], [4].

The V_{th} sensitivity to process variations shows surface orientation dependence because of the different degree of quantum-confinement effect for various surface orientations. Since the carrier mobility of a MOSFET also depends on the surface orientation, it has been proposed that with an optimized surface orientation, the circuit performance of a FinFET structure can be enhanced [5], [6]. Thus, the immunity of a FinFET structure with various surface orientations to process variations is an important issue.

Since the GAA structure is considered as an important candidate for ultimate CMOS scaling, the impacts of quantum-confinement effects may be especially significant because of the ultra-scaled channel thickness for GAA devices. The results in Chapter 2 indicate that the down-scaling of channel thickness decreases the sensitivity of V_{th} to process variations. However, the impact of quantum-confinement effect is becoming crucial to the V_{th} sensitivity to process variations with the down-scaling of the channel thickness. Whether there is an optimum channel thickness design regarding the minimization of the V_{th} variation for GAA devices merits further investigation.

To account for the impacts of quantum-confinement effect, analytical solutions of Schrödinger equation needs to be included in our theoretical framework. The quantum-confinement effect is often considered to be independent of the carrier flow direction (i.e., channel length direction). Thus, the quantum-confinement model for long-channel and undoped devices was proposed using the flat-well approximation [1], [2], [7]. For short channel devices, however, the center of the potential well is altered by the source/drain coupling due to the short-channel effect, and the flat-well approximation is no longer valid. An accurate quantum-confinement model considering the short-channel effects is crucial to the determination of V_{th} for short-channel FinFET and GAA devices.

In this chapter, we investigate the impacts of quantum-confinement effect on the sensitivity of V_{th} to process variations for short-channel FinFET and GAA devices using analytical solutions of Schrödinger equation verified with TCAD simulation. Specifically, the impacts of surface orientation on the V_{th} sensitivity [3] for FinFET and the optimized channel thickness design for GAA devices are assessed [4] using our theoretical framework.

3.2 Modeling of Eigen-Energy for Short-Channel FinFET

Figure 3-1 shows a schematic sketch of a FinFET structure. The eigen-energy of channel carriers for FinFET can be determined either by directly solving the 1-D Schrödinger equation [3] or by the perturbation theory [8]. With emphasis on the short-channel devices, the potential well considering the short-channel effect is considered in the eigen-energy calculation.

3.2.1 Analytical Solution of Schrödinger Equation for Short-Channel FinFET

To consider the quantum-confinement effect along the fin-width (i.e., *x*) direction, the

Schrödinger equation can be expressed as

$$-\frac{\hbar^2}{2m_x}\cdot\frac{d^2\Psi_j(x)}{dx^2}+E_C(x)\cdot\Psi_j(x)=E_j\cdot\Psi_j(x) \qquad \text{(3-1)}$$

where E_j is the j-th eigen-energy, $\Psi_j(x)$ is the corresponding wavefunction, $\hbar$ is the reduced Plank constant, and m_x is the carrier quantization effective mass. For electrons in Si- and Ge-channel, the m_x for various surface orientations are listed in Table 3-1 [9]. Appendix 1 shows more details of the effective masses in Table 3-1. If the conduction band edge $E_C(x)$ is treated as a flat well with potential energy β, the solution of Equation (3-1) is $\Psi_{j,flat}(x) = (2/t_{ch})^{1/2}\cdot \sin((j+1)\pi(x + t_{ch}/2)/t_{ch})$ and $E_{j,flat} = \beta + (j+1)^2\pi^2\hbar^2/(2m_x\cdot t_{ch}^2)$ [2]. However, to account for the source/drain coupling due to the short-channel effects, the conduction band edge $E_C(x)$ in Equation (3-1) should be treated as a parabolic-well with potential energy $E_C(x) = \alpha x^2 + \beta$ [3]. The α and β are length-dependent coefficients and can be obtained from the channel potential solution of Poisson's equation under subthreshold region.

In Chapter 2, we have derived the 3-D channel potential solution $\phi(x,y,z)$ for multi-gate MOSFETs in the subthreshold region. For the FinFET structure in this study, the potential solution can still be applied after neglecting the top gate potential coupling along the fin-height direction. In other words, the channel potential solution for the FinFET structure in Figure 3-1 can be expressed as $\phi(x,y) = \phi_1(x) + \phi_2(x, y)$:

$$\phi_1(x)=-\frac{qN_a}{2\varepsilon_{ch}}\cdot\left(x+\frac{1}{2}t_{ch}\right)^2+a\cdot\left(x+\frac{1}{2}t_{ch}\right)+b \qquad \text{(3-2a)}$$

$$a=\frac{(qN_a/2\varepsilon_{ch})\cdot\left(t_{ch}^2+2(\varepsilon_{ch}/\varepsilon_{in})\cdot\left(t_{ch}^2+2(\varepsilon_{ch}/\varepsilon_{in})\cdot t_{in}\cdot t_{ch}\right)\right)}{W_{eff}} \qquad \text{(3-2b)}$$

$$b=(V_{GS}-V_{fb})+\frac{\varepsilon_{ch}}{\varepsilon_{in}}\cdot t_{in}\cdot a \qquad \text{(3-2c)}$$

$$\phi_2(x,y)=\sum_{i=1}^{\infty}\left[c_i\cdot\sinh\left(\frac{i\pi}{W_{eff}}\cdot y\right)+c_i'\cdot\sinh\left(\frac{i\pi}{W_{eff}}\left(L_{eff}-y\right)\right)\right]\cdot\sin\left(\frac{i\pi}{W_{eff}}\left(x+\frac{1}{2}t_{ch}+\frac{\varepsilon_{ch}}{\varepsilon_{in}}t_{in}\right)\right)$$

(3-2d)

$$c_i=\frac{1}{\sinh\left(i\pi\left(L_{eff}/W_{eff}\right)\right)}\cdot\left[2\left(-\phi_{ms}+V_{DS}-b\right)\cdot\frac{1-(-1)^i}{i\pi}+2a\left(\frac{t_{in}}{i\pi}+\frac{\left(W_{eff}-t_{in}\right)\cdot(-1)^i}{i\pi}\right)\right.$$
$$\left.+\frac{qN_a}{\varepsilon_{ch}}\cdot\left(\frac{t_{in}{}^2}{i\pi}-\frac{\left(W_{eff}-t_{in}\right)^2(-1)^i}{i\pi}+2W_{eff}{}^2\,\frac{(-1)^i-1}{(i\pi)^3}\right)\right]$$

(3-2e)

$$c_i'=\frac{1}{\sinh\left(i\pi\left(L_{eff}/W_{eff}\right)\right)}\cdot\left[2\left(-\phi_{ms}-b\right)\cdot\frac{1-(-1)^i}{i\pi}+2a\left(\frac{t_{in}}{i\pi}+\frac{\left(W_{eff}-t_{in}\right)\cdot(-1)^i}{i\pi}\right)\right.$$
$$\left.+\frac{qN_a}{\varepsilon_{ch}}\cdot\left(\frac{t_{in}{}^2}{i\pi}-\frac{\left(W_{eff}-t_{in}\right)^2(-1)^i}{i\pi}+2W_{eff}{}^2\,\frac{(-1)^i-1}{(i\pi)^3}\right)\right] \qquad (3\text{-}2f)$$

where $W_{eff}=t_{ch}+2(\varepsilon_{ch}/\varepsilon_{in})\cdot t_{in}$ with ε_{ch} and ε_{in} being the dielectric constants of channel and gate insulator, respectively. t_{in} is the thickness of gate insulator. N_a is the channel doping, V_{GS} is the voltage bias of the gate terminal, V_{fb} is the flat-band voltage, V_{DS} is the voltage bias of the drain terminal, and ϕ_{ms} is the built-in potential of the source/drain to the channel.

After further reducing ϕ_2 to a parabolic form, E_C can be expressed as $E_C(x)=\alpha\cdot x^2+\beta$ with

$$\alpha=(-q)\cdot\left\{\sum_{i=1}^{\infty}\left[c_i\sinh\left(\frac{i\pi}{W_{eff}}\cdot y\right)+c_i'\sinh\left(\frac{i\pi}{W_{eff}}\cdot\left(L_{eff}-y\right)\right)\right]\cdot\left(-\frac{1}{2}\left(\frac{i\pi}{W_{eff}}\right)^2\right)\cdot\sin\left(\frac{i\pi}{2}\right)\right\}$$

(3-3a)

$$\beta=(-q)\cdot\left\{b+\sum_{i=1}^{\infty}\left[c_i\sinh\left(\frac{i\pi}{W_{eff}}\cdot y\right)+c_i'\sinh\left(\frac{i\pi}{W_{eff}}\cdot\left(L_{eff}-y\right)\right)\right]\cdot\sin\left(\frac{i\pi}{2}\right)-\left[\frac{1}{2}\cdot\frac{E_g}{q}+\frac{1}{2}\frac{kT}{q}\cdot\ln\left(\frac{N_c}{N_v}\right)\right]\right\}$$

(3-3b)

where kT/q is the thermal voltage, E_g is the bandgap of the channel material, and N_c and N_v are effective density of states for conduction and valence bands, respectively. Using the parabolic-well approximation, the solution of Equation (3-1) can be expressed as power series [10]

$$\Psi_j(x) = \sum_{n=0}^{\infty} d_n \cdot x^n \qquad \text{(3-4a)}$$

with the coefficients d_n's being determined by the following recurrence relationship:

$$d_2 = -\frac{m_x(E_j - \beta)}{\hbar^2} \cdot d_0\,, \quad d_3 = -\frac{m_x(E_j - \beta)}{3\hbar^2} \cdot d_1\,,$$

$$d_{n+2} = -\frac{2m_x(E_j - \beta)/\hbar^2}{(n+1)(n+2)} \cdot d_n + \frac{2m_x\alpha/\hbar^2}{(n+1)(n+2)} \cdot d_{n-2}\,, \quad n \geq 2\,. \qquad \text{(3-4b)}$$

It should be noted that as $\alpha = 0$ (i.e., E_C is spatially constant), $\Psi_j(x)$ will return to the form of sinusoidal functions, which is the solution for the flat-well approximation [2]. The jth eigen-energy E_j can be determined by the boundary condition $\Psi_j\ (x = t_{\text{ch}} / 2) = 0$. Thus, the eigen-energy and eigenfunction of short-channel FinFET under subthreshold region can be derived.

To validate the accuracy of this analytical solution of Schrödinger equation, we compare the calculation results with the TCAD simulation that numerically solves the self-consistent solution of 2-D Poisson and 1-D Schrödinger equations [11]. The Schrödinger equation is solved along the fin-width (x) direction to consider the quantum-confinement effect. The effective masses used for various surface orientations in the TCAD simulations are listed in Table 3-1. We assume that the barrier height across gate insulator/channel is infinite and the wavefunctions vanish at the interface. In this study, we focus on FinFETs with lightly doped channel ($N_a = 10^{15}$ cm^{-3}). The EOT is 0.5nm to sustain the electrostatic integrity, and a mid-gap gate workfunction (4.5eV) is used. Figure 3-2 shows that for a short-channel lightly-doped FinFET, the conduction band edge E_C is bended from a flat well to a parabolic-like well due to the source/drain coupling. It can be seen that the eigen-energy calculated by our model considering the parabolic-well approximation agrees well with the TCAD simulation. Since E_C is not spatially constant along the x-direction for short-channel devices, we choose E_C at the channel center (i.e., $x = 0$) as the reference energy. Figure 3-3 shows the channel length ($\mathrm{L_{eff}}$) dependence of the energy difference of E_0' (ground-state energy in 4-fold valley) and the bottom of well $E_C(x = 0)$. In contrast to the constant $E_0'-E_C(x = 0)$ calculated from the flat-well approximation, both the TCAD simulation and our model show that the $E_0'-E_C(x = 0)$ increases with decreasing $\mathrm{L_{eff}}$. In addition to eigen-energy, the bended potential well due to the short-channel effect also affects the shape of the wavefunction. Figure 3-4 shows that the $|\Psi_0'|^2$ for lightly-doped FinFET with shorter $\mathrm{L_{eff}}$ (i.e., $\mathrm{L_{eff}} = 15\mathrm{nm}$) is more centralized to the channel center. This is because the E_C barrier at the channel center ($x = 0$) is lower than that near the insulator/channel interface ($x = 0.5t_{ch}$) and thus the electron density becomes larger at $x = 0$.

Using this power series method, the eigen-energy needs to be numerically determined through the non-linear equation. Nevertheless, the derived eigen-energy is fairly accurate (as shown in Figure 3-2 and 3-3). In the Section 3.2.2, an approximated and explicit form of eigen-energy can be derived using the perturbation theory.

3.2.2 Closed-Form Model of Eigen-Energy Using the Perturbation Theory

Besides solving the Schrödinger equation directly, the eigen-energy can also be derived using the approximated methods such as the perturbation theory [8]. The advantage of the perturbation approach is that the derived eigen-energy is a closed-form expression, which shows clear physical insights and can be applied in the compact modeling for circuit simulation.

For short-channel undoped devices, a parabolic channel potential well $E_C(x) = \alpha \cdot x^2 + \beta$ needs to be considered in the derivation of the ground-state eigen-energy E_0. Using the perturbation theory and treating the $\alpha \cdot x^2$ term as a perturbation to the flat well with energy level β, the first-order approximated eigen-energy $E_0{}^1$ for a parabolic well can be expressed as

$$E_0^1 \cong E_{0,flat} + \alpha \cdot \int_{-tch/2}^{tch/2} x^2 \cdot \Psi_{0,flat}{}^2(x)dx \qquad (3\text{-}5)$$

where $E_{0,flat} = \beta + \pi^2\hbar^2/(2m_x \cdot t_{ch}^2)$ is the ground-state eigen-energy of the flat well, and $\Psi_{0,flat}(x) = (2/t_{ch})^{1/2} \cdot \sin(\pi(x + t_{ch}/2)/t_{ch})$ is the ground-state wavefunction of the flat well. It can be further shown that:

$$E_0^1 = \beta + \frac{\pi^2\hbar^2}{2m_x t_{ch}{}^2} + \frac{\alpha}{12} \cdot t_{ch}{}^2 \cdot \left(1 - \frac{6}{\pi^2}\right) \qquad (3\text{-}6)$$

Equation (3-6) can provide a mathematical support for Figure 3-3. As the source/drain coupling due to short-channel effect results in a parabolic potential well $\alpha \cdot x^2$, the E_0 for a short-channel device is raised from the long-channel $E_{0,flat}$. The decreasing L_{eff} increases the α and hence E_0.

Higher order terms can be further considered to derive a more accurate ground-state eigen-energy for a parabolic well. In our calculation, we keep the second-order term: $(\alpha \cdot \int x^2 \cdot \Psi_{0,flat}(x) \cdot \Psi_{1,flat}(x)dx)^2/(E_{1,flat} - E_{0,flat})$ [8] where $E_{1,flat}$ and $\Psi_{1,flat}(x)$ are eigen-energy and wavefunction of first eigen-state, respectively. Therefore, the second-order approximated eigen-energy (E_0^2) for a parabolic well can be further shown as

$$E_0^2 = \beta + \frac{\pi^2\hbar^2}{2m_x t_{ch}{}^2} + \frac{\alpha}{12} \cdot t_{ch}{}^2 \cdot \left(1 - \frac{6}{\pi^2}\right) - \frac{9\alpha^2}{256} \cdot \frac{m_x t_{ch}{}^6}{\pi^6\hbar^2} \qquad (3\text{-}7)$$

Figure 3-5(a) compares the E_0 calculated by the power series method in Section 3.2.1 and the perturbation theory [Equation (3-7)]. It can be seen that the L_{eff} dependences of E_0

calculated by Equation (3-7) for FinFETs with t_{ch} = 6nm and 7nm are consistent with the power series method. Nevertheless, the E_0 calculated by the perturbation theory for t_{ch} = 10nm differs from the power series method when L_{eff} is smaller than 20nm. For FinFET with t_{ch} = 10nm, the error is growing with increasing α due to the down-scaling of L_{eff}, as shown in Figure 3-5(b). However, Figure 3-5(c) shows that although the α is similar for L_{eff} = 15nm FinFET with various t_{ch}, the error of E_0 calculated by the perturbation theory is larger for t_{ch} = 10nm. Thus, this error also depends on the t_{ch}.

The error source of Equation (3-7) may be attributed to the truncation of higher order terms. The higher order terms are roughly proportional to the inverse of the differences between adjacent eigen-energies for a flat well [12]. In other words, these higher order terms are related to t_{ch} and m_x because the eigen-energies for a flat well are proportional to $1/(m_x \cdot t_{ch}^2)$. Thus, the error of Equation (3-7) increases with m_x and t_{ch}. Figure 3-6(a) shows $E_0 - E_{0,flat}$ (the E_0 increase due to the parabolic well) dependence on the t_{ch}^2 for FinFET with L_{eff} = 15nm. It can be seen that the error of $E_0 - E_{0,flat}$ calculated by Equation (3-7) becomes larger with t_{ch}^2, which can explain the discrepancy of E_0 in Figure 3-5(a) for FinFET with relatively larger t_{ch} = 10nm. In addition to t_{ch}, Figure 3-6(b) shows that the error of $E_0 - E_{0,flat}$ increases with m_x. As the m_x for (100) surface is larger than (110) and (111) surfaces for Si-NFET, the error of Equation (3-7) is larger for Si-(100) FinFET.

In summary, using the perturbation theory, we can derive a closed-form model of E_0 for short-channel FinFET. Although the perturbation approach that keeps the lowest-order terms may not be as accurate as the power series method, it will exhibit satisfactory accuracy for devices with ultra-scaled t_{ch} and smaller m_x such as high mobility channel materials. This closed-form E_0 model can provide physical insights and suitable for compact modeling purposes.

3.3 Impact of Surface Orientation on the Sensitivity of V_{th} for FinFET

For FinFET structure, different surface orientations such as (100), (110), and (111) can be achieved by rotating the device layout in the wafer plane [5]. Thus, the V_{th} variation for various surface orientations is crucial to FinFET technology. In this section, we investigate the impact of surface orientation on the sensitivity of V_{th} to process variations and temperature.

3.3.1 Sensitivity of V_{th} to Process Variations

To assess the impact of quantum confinement on threshold voltage (V_{th}), the V_{th} is defined as the V_{GS} at which the average electron density of the cross-section at y = L_{eff} /2 (highest potential barrier for low V_{DS}) exceeds the critical concentration 1×10^{16} cm^{-3} [13] in this chapter. The electron density is determined by the eigen-energy and eigenfunction as

$$n(x,y) = N_{C,QM} \cdot \exp\left(-\frac{E_C - E_F}{kT}\right) \tag{3-8a}$$

$$N_{C,QM} = \frac{kT}{\pi\hbar^2} \cdot \sum_{v,j} g_v \cdot m_d^v \cdot \left|\Psi_{v,j}(x,y)\right|^2 \cdot \exp\left(-\frac{E_{v,j} - E_C}{kT}\right) \tag{3-8b}$$

where g_v is the valley degeneracy and m_d^v is the density-of-state effective mass of valley v. The g_v and m_d^v for Si and Ge channels are listed in Table 3-1. In other words, the impact of quantized eigen-energies and eigen-functions on the electron density is incorporated into the effective density of states for conduction band ($N_{C,QM}$) [2]. The eigen-energies $E_{v,j}$ is calculated using the power series method, as demonstrated in Section 3.2.1. It can be seen from Equation (3-8b) that the flat-well approximation may overestimate the electron density for short-channel devices because it underestimates eigen-energies E_j (as shown in Figure 3-3). Figure 3-7 compares the electron density distribution calculated from the flat-well approximation and our model. The electron density predicted by our model agrees well with the TCAD simulation, while the flat-well approximation shows higher electron density in both sides of the channel.

Figure 3-8 shows that for Si-FinFETs with a small t_{ch}, the V_{th} and its sensitivity to channel thickness (t_{ch}) variations considering the quantum-confinement effect is larger than that predicted by the CL model. Moreover, the V_{th} of (111)- and (110)-surface increase more rapidly than that of (100)-surface with decreasing t_{ch}. This is because the quantum-confinement effect depends on surface orientation, as indicated by the inset of Figure 3-8. For FinFET with small t_{ch}, the V_{th} is mainly determined by the E_0. In addition, as the m_x and thus the ground-state energy of 2-fold and 4-fold valleys for (100)- and (110)-surface are different (see Table 3-1), the overall lowest state occurs for the valley with larger m_x because (to the first order) the eigen-energy is inverse proportional to m_x. Therefore, the m_x of 2-fold valley determines the E_0 for (100)-surface and the m_x of 4-fold valley determines the E_0 for (110)-surface. Since the dominant m_x of various surface orientations for Si-channel is (111) < (110) < (100), the E_0 and thus V_{th} is (111) > (110) > (100) as shown in Figure 3-8.

For high-mobility channel such as Ge-FinFETs, the V_{th} dispersion due to quantum-confinement becomes more significant. Figure 3-9 shows that the V_{th} of (100)-surface increases more rapidly than (110)- and (111)-surface with reducing t_{ch}. This is because the quantum-confinement effect of (100)-surface is larger than that of (110)- and (111)-surface, as indicated by the inset of Figure 3-9. Since the dominant m_x of various surface orientations for Ge-channel is (111) > (110) > (100), the E_0 and hence V_{th} is (100) > (110) > (111).

Besides the V_{th} sensitivity to the t_{ch} variation, the quantum-confinement effect also affects the V_{th} sensitivity to the L_{eff} variation. Figure 3-10 shows that for Ge-FinFETs, the degree of V_{th} roll-off predicted by our quantum-confinement model is (100) < (110) < (111) <

CL, which is opposite to the V_{th} sensitivity to the t_{ch} variations (Figure 3-9). In other words, while the quantum-confinement effect enhances the V_{th} sensitivity to the t_{ch} variation, it reduces the V_{th} sensitivity to the L_{eff} variation. This can be explained as follows. The V_{th} shift due to the quantum-confinement effect can be expressed as $\Delta V_{th}^{QM} = S / (\ln 10 \cdot kT/q) \cdot \Delta\psi_s^{QM}$ with S being the subthreshold swing and $\Delta\psi_s^{QM}$ being the equivalent surface potential shift [14]. The S for a short-channel device is larger than that for a long-channel device because of enhanced drain coupling with decreasing L_{eff}. Therefore, for devices with a given surface orientation, the ΔV_{th}^{QM} (which increases the V_{th}) of the short-channel device is larger than that of the long-channel one, as indicated by the inset of Figure 3-10. The discrepancy in ΔV_{th}^{QM} between short- and long-channel devices reduces the V_{th} roll-off, and the V_{th} roll-off considering the quantum-confinement effect becomes smaller than the CL model. In addition, as the $\Delta\psi_s^{QM}$ is determined by E_0, a larger E_0 (and thus $\Delta\psi_s^{QM}$) results in a larger ΔV_{th}^{QM} and hence smaller V_{th} roll-off. This explains why the degree of V_{th} roll-off is (100) < (110) < (111) for Ge-FinFETs.

In addition to the eigen-energies (Figure 3-3) and the electron density (Figure 3-7), the V_{th} calculated by our model is physically more accurate than that calculated by the flat-well approximation. Figure 3-11 shows that the V_{th} calculated using our model and the flat-well approximation are fairly close for devices with small t_{ch}. However, the discrepancy between the two models increases with t_{ch} because the impact of short-channel effects becomes more significant for devices with larger t_{ch}. As compared with the flat-well approximation, the V_{th} calculated by our model is more physical because it returns to the classical one for devices with larger t_{ch}, in which the quantum-confinement effect is negligible.

For Ge-FinFETs, only L-valley is considered in our calculation. The relative importance of other conduction band bottoms such as Γ-valley and X-valley will be discussed in the Appendix 2.

3.3.2 Sensitivity of V_{th} to Temperature

Besides the V_{th} sensitivity to process variations, the quantum-confinement effect may also alter the V_{th} sensitivity to temperature. In this section, we assess the V_{th} sensitivity to temperature for long-channel FinFET with various surface orientations.

Figure 3-12(a) and (b) shows the V_{th} sensitivity to temperature (dV_{th} / dT) at 150K for long-channel Si and Ge FinFET with various surface orientations, respectively. Note that the dV_{th} / dT is negative (i.e., the V_{th} decreases with increasing temperature). As the dV_{th} / dT for various surface orientations return to the classical (CL) value for FinFET with large t_{ch}, the dV_{th} / dT depends on the surface orientation when the quantum-confinement effect becomes significant. It can be seen that, similar to the V_{th} sensitivity to t_{ch} (Figure 3-9), the dV_{th} / dT for (111) surface is larger than (110) and (100) surfaces for Si-FinFET. For Ge-FinFET, the dV_{th} / dT for (100) surface is larger than (110) and (111) surfaces.

The temperature dependence of V_{th} for NFET can be explained through the effective density of state (DOS) for the conduction band (N_C). When the quantum-confinement effect is not considered, the degree of freedom for electron is 3. This 3-D N_C can be expressed as $N_C^{3D} = 2\cdot[m_n kT/(2\pi\hbar^2)]^{3/2}$ with m_n being the classical DOS effective mass. The m_n is equal to $g_{total}^{2/3}\cdot(m_t^2 m_l)^{1/3}$ with m_t and m_l being the transverse and longitudinal effective masses of the constant energy ellipsoid, respectively, and g_{total} being the total number of the ellipsoids. When 1-D quantum-confinement effect is considered for FinFET structure, the degree of freedom for electron is 2, and the 2-D N_C can be expressed as

$$N_C^{2D} = \frac{1}{t_{ch}} \cdot \frac{kT}{\pi\hbar^2} \cdot \sum_{v,j} g_v \cdot m_d^v \cdot \exp\left(-\frac{E_{v,j} - E_C}{kT} \right) \qquad (3\text{-}9)$$

where m_d^v and $E_{v,j}$ are the DOS effective mass for 1-D confinement (as listed in Table 3-1) and the j^{th} eigen-energy for the v-valley, respectively. The V_{th} shift due to quantum-confinement effect (ΔV_{th}^{QC}) can be expressed as $m\cdot kT/q\cdot\ln(Q_{i,CL}/\,Q_{i,QC})$ with $Q_{i,CL}$ and $Q_{i,QC}$ being the sheet charge density calculated by the classical model and the quantum-confinement model, respectively. The ΔV_{th}^{QC} can be further expressed as $m\cdot kT/q\ \cdot\ln(N_C^{3D}/N_C^{2D})$. Using the ground-state approximation (i.e., most carriers populate at the ground-state), the ΔV_{th}^{QC} can be simplified as

$$\Delta V_{th}^{QC} = m\cdot\left[\frac{k}{q}\cdot T\cdot\ln\left(t_{ch}\cdot\frac{g_{total}\cdot\left(m_t^{\,2}m_l\right)^{1/2}}{g_v\cdot m_d^v}\cdot\left(\frac{k}{2\pi\hbar^2}\right)^{1/2}\cdot T^{1/2}\right)+\frac{E_{v,0}-E_C}{q}\right] \qquad (3\text{-}10)$$

where g_v and $m_d^{\,v}$ are the degeneracy and the DOS effective mass of the valley v, in which the ground-state electrons occupy. Using the relation $m_x^{\,v}\cdot(m_d^{\,v})^2 = m_t^2 m_l$ [9] with $m_x^{\,v}$ being quantization effective mass of valley v, the sensitivity of ΔV_{th}^{QC} to temperature ($d\Delta V_{th}^{QC}/dT$) can be expressed as

$$\frac{d\Delta V_{th}^{QC}}{dT} = m\cdot\frac{k}{q}\cdot\left[\ln\left(t_{ch}\cdot\frac{g_{total}}{g_v}\cdot\left(\frac{m_x^v}{m_0}\right)^{1/2}\cdot\left(\frac{m_0 k}{2\pi\hbar^2}\right)^{1/2}\right)+1/2+\frac{1}{2}\cdot\ln(T)\right]$$

$$= m\cdot\frac{k}{q}\cdot\left[\ln\left(t_{ch}\right)+\ln\left(\frac{g_{total}}{g_v}\cdot\left(\frac{m_x^v}{m_0}\right)^{1/2}\right)+\frac{1}{2}\ln\left(T\right)+16.91\right] \qquad (3\text{-}11)$$

where m_0 is the static effective mass for electron. Note that the $d\Delta V_{th}^{QC}/dT$ is independent of the ground-state eigen-energy under the ground-state approximation.

As the impact of quantum-confinement effect on dV_{th}/dt_{ch} stems from the $m_x^{\,v}$ (see Section 3.3.1), the impact of quantum-confinement effect on dV_{th}/dT is also determined by the $m_x^{\,v}$. This explains why the dV_{th}/dT and dV_{th}/dt_{ch} are similar when comparisons between various orientations are made. Since the $(g_{total}/g_v)\cdot(m_x^{\,v}/m_0)^{1/2}$ and hence the $d\Delta V_{th}^{QC}/dT$ for Si-FinFET is (100) > (110) > (111), Figure 3-12(a) shows that the degree of dV_{th}/dT is (111) > (110) > (100) because the dV_{th}/dT are negative. Similarly, for Ge-FinFET, since the $(g_{total}/g_v)\cdot(m_x^{\,v}/m_0)^{1/2}$ and hence the $d\Delta V_{th}^{QC}/dT$ is (111) > (110) > (100), Figure 3-12(b) shows that the degree of dV_{th}/dT is (100) > (110) > (111).

Equation (3-11) exhibits good accuracy when the impact of quantum-confinement effect is significant (i.e., the ground-state approximation is valid). In addition to m_x, Equation (3-11) indicates that the $d\Delta V_{th}^{QC}/dT$ also depends on the t_{ch} and temperature. Figure 3-13(a) shows that the $d\Delta V_{th}^{QC}/dT$ for Si, Ge, and InGaAs FinFET is proportional to $\ln(t_{ch})$, and the slope for FinFET with small t_{ch} is independent of channel material. Figure 3-13(b) shows that the slope of $d\Delta V_{th}^{QC}/dT$ dependence on ln(T) for low temperature is also independent of channel material, as predicted by Equation (3-11).

3.4 Impact of Quantum-Confinement Effect on the Sensitivity of V_{th} to Process Variations for GAA MOSFET

Due to the surrounding gate configuration, GAA devices with ultra-scaled channel thickness will exhibit significant two-dimensional quantum-confinement effect. Therefore, an accurate quantum-confinement model is crucial to the device design using the GAA structure. Chapter 2 indicates that the channel diameter variation is crucial to the V_{th} variation of GAA devices, and the V_{th} sensitivity to channel diameter can be reduced by the down-scaling of channel diameter. However, the quantum-confinement effect becomes significant and increases the V_{th} sensitivity to channel diameter for GAA devices with small diameter. In this section, we investigate the sensitivity of V_{th} to process variations for short-channel GAA MOSFETs using analytical solution of Schrödinger equation [15].

3.4.1 Analytical Solution of Schrödinger Equation for Short-Channel GAA MOSFETs

The Schrödinger equation in the cylindrical coordinate is

$$-\frac{\hbar^2}{2m_r}\left(\frac{\partial^2}{\partial r^2}+\frac{1}{r}\frac{\partial}{\partial r}+\frac{1}{r^2}\frac{\partial^2}{\partial \theta^2}\right)\Psi_j(r,\theta)+E_C(r,\theta)\cdot\Psi_j(r,\theta)=E_j\cdot\Psi_j(r,\theta) \qquad (3\text{-}12)$$

where E_j is the eigen-energy, and $\Psi_j(r,\theta)$ is the corresponding wavefunction. $\hbar$ is the reduced Plank constant. m_r is the effective mass of electron. For Si GAA channel, we consider the effective mass of the 4-fold degenerate valleys as $2m_l{\cdot}m_t$ / $(m_l + m_t)$ and that of the 2-fold degenerate valleys as m_t [11], [16]-[18] with m_l and m_t the longitudinal and transverse effective masses, respectively. It should be noted that an approximated isotropic effective mass is used in Equation (3-9) to preserve the symmetric property in the cylindrical coordinate. This isotropic-mass approximation has also been employed by [15]-[17] in the studies of silicon nanowires, and has been shown to yield reasonably accurate subband energy levels [16]-[18].

The conduction band edge $E_C(r,\theta)$ in Equation (3-12) can be obtained from the channel potential solution of Poisson's equation. In Chapter 2, we have derived the channel potential solution $\phi(r,y)$ for GAA MOSFETs in the subthreshold region. To simplify the solution of the Schrödinger equation, the Bessel-function-based ϕ_2 is further reduced to the parabolic form, and E_C can be expressed as $E_C = \alpha{\cdot}r^2 + \beta$ with

$$\alpha = (-q)\cdot\left[A + \sum_n\left(-\frac{1}{4}\lambda_n{}^2\right)\cdot\left[k_n\cdot\sinh(\lambda_n\cdot y) + k_n'\cdot\sinh\left(\lambda_n\left(L_{eff}-y\right)\right)\right]\right] \quad \text{(3-10a)}$$

$$\beta = (-q)\cdot\left\{B + \sum_n\left[k_n\cdot\sinh(\lambda_n\cdot y) + k_n'\cdot\sinh\left(\lambda_n\left(L_{eff}-y\right)\right)\right] - \left[\frac{1}{2}\cdot\frac{E_g}{q} + \frac{1}{2}\frac{kT}{q}\cdot\ln\left(\frac{N_c}{N_v}\right)\right]\right\}$$

(3-13b)

The coefficients A, B, λ_n, k_n and k_n' are shown in Section 2.2.1. Using the separation of variables technique, the solution of Equation (3-12) can be expressed as $\Psi_{n,l}(r,\theta) = R_n(r){\cdot}\exp(i{\cdot}l{\cdot}\theta)$ [19] with n and l the principle quantum number and the angular quantum number, respectively. It should be noted that the angular quantum number l is restricted to integers (0, ±1, ±2, ….) because of the periodicity of θ. Thus, $R_n(r)$ is the solution of

$$r^2\cdot\frac{d^2R_n(r)}{dr^2}+r\cdot\frac{dR_n(r)}{dr}+\left\{\frac{2m_r r^2}{\hbar^2}\left[E_n-\left(\alpha\cdot r^2+\beta\right)\right]-l^2\right\}\cdot R_n(r)=0 \tag{3-14}$$

$R_n(r)$ can be expressed as power series

$$R_n(r)=\sum_{i=0}^{\infty}c_i\cdot r^{2i+l} \tag{3-15a}$$

with the coefficients c_i determined by the recurrence relationship

$$c_1=-\frac{2m_r}{\hbar^2}\cdot\frac{(E_n-\beta)}{4(l+1)}\cdot c_0,\quad c_i=-\frac{2m_r}{\hbar^2}\cdot\frac{(E_n-\beta)\cdot c_{i-1}-\alpha\cdot c_{i-2}}{4\cdot i^2+4\cdot i\cdot l},\ i\geq 2. \tag{3-15b}$$

Generally, 20 terms in the summation of (3-15a) are needed to give sufficiently accurate results. It should be noted that as $\alpha = 0$ (i.e., E_C is spatially constant), $R_n(r)$ will return to the form of Bessel function, which is the solution for long-channel and undoped GAA devices [1], [7]. The n^{th} eigen-energy E_n can be determined by the boundary condition $R_n(r = D/2) = 0$. Thus, the eigen-energy and eigen-function for short-channel GAA MOSFETs under the subthreshold region can be derived.

Using the calculated eigen-energies and eigen-functions, we can calculate the electron density in the channel. The electron density can be expressed as

$$n(r,y)=N_{C,QM}\cdot\exp\left(-\frac{E_C-E_F}{kT}\right) \tag{3-16a}$$

$$N_{C,QM}=\sqrt{\frac{2kT}{\pi\hbar^2}}\cdot\sum_{v,n,l}g_v\cdot\sqrt{m_d^v}\cdot\left|\Psi_{v,n,l}(r,y)\right|^2\cdot\exp\left(-\frac{E_{v,n,l}-E_C}{kT}\right) \tag{3-16b}$$

where g_v is the valley degeneracy, and $m_d^{\,v}$ is the density-of-state (DOS) effective mass of valley v.

Figure 3-14 shows the calculated quantized j^{th} eigen-energy (E_j) and the square of j^{th} eigen-function ($|\Psi_j|^2$) for lightly-doped long-channel GAA devices, and the results are verified with TCAD simulation that numerically solves the self-consistent solution of 3-D Poisson and

2-D Schrödinger equations [11]. It can be seen that E_j and the difference between two distinct eigen-energies increase with decreasing channel diameter (D). Due to the cylindrical symmetry in the θ direction, the E_2 and E_3 are degenerate because they correspond to the states of $l = 1$ and -1. Similarly, the E_4 and E_5 are degenerate. The results in Figure 3-14 can also be predicted by the quantum confinement model using the flat well approximation [1], [7]. For short-channel lightly-doped GAA devices, however, the conduction band edge E_C is lowered by source/drain coupling and is bended from a flat well to a parabolic-like well (Figure 3-15). Since the E_C is not spatially constant for short-channel devices, we choose the E_C at the channel center ($r = 0$) as the reference energy. Figure 3-15 shows that the E_j's can be correctly predicted by our analytical solution considering the short-channel potential barrier. Figure 3-16(a) shows that the lowest eigen-energy (E_1) increases as channel length decreases. This eigen-energy shift results from the bending of E_C due to the short channel effect. Figure 3-16(b) shows that the square of lowest eigen-function ($|\Psi_1|^2$) for short-channel lightly-doped device is more centralized to the channel center. This is because the E_C barrier at the channel center ($r = 0$) is lower than that near the insulator/channel interface ($r = D/2$), and the electron density becomes larger at $r = 0$. Figure 3-17 shows that the E_1 increases with V_{DS}. In other words, the drain-induced-barrier-lowering (DIBL) increases the E_C bending and affects the quantum confinement effects.

Figure 3-18 compares the electron density distribution calculated from the classical model (see Chapter 2) and the quantum confinement model using Equation (3-16). It can be seen that for lightly-doped short-channel GAA MOSFET, the electron density near the interface ($r = D/2$) predicted by the quantum confinement model is smaller than classical model. Furthermore, the average electron density can be calculated by $\int 2\pi \cdot r \cdot n(r,y)dr/A_{ch}$ with $n(r,y)$ the electron density derived from Equation (3-16) and A_{ch} the cross-sectional area of the channel. Figure 3-19 compares the average electron density at $y = 0.5L_{eff}$ calculated from the classical model and the quantum confinement one for lightly-doped short-channel devices. It can be seen that the discrepancy becomes larger with reducing channel diameter.

3.4.2 Sensitivity of V_{th} to Process Variations for GAA MOSFETs

Figure 3-20 shows that the classical V_{th} ($V_{th,CL}$) of long channel GAA devices remains constant with decreasing *D*, while the V_{th} considering quantum confinement ($V_{th,QM}$) increases significantly with decreasing *D*. For short-channel GAA MOSFETs, the $V_{th,CL}$ increases with decreasing *D* [Figure 3-21(a)], and $dV_{th,CL}/dD$ decreases with *D* [Figure 3-21(b)]. This is because the *D* scaling suppresses the SCE. However, for devices with small *D*, $V_{th,QM}$ increases more significantly than $V_{th,CL}$ due to the quantum confinement effect [Figure 3-21(a)], and hence the $dV_{th,QM}/dD$ increases with decreasing *D* [Figure 3-21(b)]. In other words, an optimum design for *D* can be chosen to reduce the V_{th} sensitivity to *D* variation. This optimized *D* depends on the L_{eff}. Figure 3-22 shows that the optimized *D* for minimum dV_{th}/dD decreases with L_{eff}. It is worth noting that although the *D* is optimized for minimum $dV_{th,QM}/dD$, the $dV_{th,QM}/dD$ increases with decreasing L_{eff}.

Besides the V_{th} sensitivity to D, the V_{th} sensitivity to L_{eff} (i.e., V_{th} roll-off) is also crucial to GAA devices. Figure 3-23 shows the V_{th} roll-off of GAA devices with various *D*. The $V_{th,QM}$ roll-off is smaller than the $V_{th,CL}$ roll-off as *D* decreases. Figure 3-24 shows that the discrepancy between $dV_{th,CL}/dL_{eff}$ and $dV_{th,QM}/dL_{eff}$ becomes larger with decreasing *D*. Besides, it can be seen that the dV_{th}/dL_{eff} decreases with *D* because of the suppression of the SCE. Therefore, GAA devices with small *D* can be designed to reduce the V_{th} sensitivity to L_{eff}. However, as indicated in Figure 3-21(b), device design with small *D* results in significant V_{th} sensitivity to channel diameter. Thus, to minimize the V_{th} variation, both dV_{th}/dD and dV_{th}/dL_{eff} have to be considered. Figure 3-25 shows that although the V_{th} roll-off becomes significant in short-channel GAA devices, the V_{th} sensitivity to *D* is larger than that to L_{eff}

because of the quantum confinement effect.

In summary, our model indicates that the V_{th} variation due to D variation is larger than that due to L_{eff} variation because of the significant quantum confinement in ultra-scaled devices. Our model indicates that the D of GAA MOSFETs can be optimized to reduce the V_{th} variation [4].

3.5 Summary

In this chapter, we investigate the impact of quantum-confinement effect on the sensitivity of V_{th} to process variations using the derived analytical solutions of Schrödinger equation for short-channel FinFET and GAA MOSFETs. The effective mass approximation is employed to deal with the Schrödinger equation. Our theoretical models consider the parabolic potential well due to short-channel effects and therefore can be used to assess the quantum-confinement effect in short-channel devices. Our study indicates that, for ultra-scaled FinFET and GAA devices, the importance of channel thickness variations increases due to the quantum-confinement effect. For FinFET, the Si-(100) and Ge-(111) surfaces show lower V_{th} sensitivity to the t_{ch} variation as compared with other orientations. On the contrary, the quantum-confinement effect reduces the V_{th} sensitivity to the L_{eff} variation, and Si-(111) and Ge-(100) surfaces show lower V_{th} sensitivity as compared with other orientations. As the V_{th} sensitivity to t_{ch} for short-channel device is determined by the short-channel effect and the quantum-confinement effect, the t_{ch} of GAA MOSFETs can be optimized to reduce the V_{th} variation.

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Table 3-1 The quantization effective mass (m_x) and the density-of-state effective mass (m_d) for electrons in Si- and Ge-channel with various surface orientations [9].

Surface orientation	Si			Ge		
	m_x	m_d	degeneracy	m_x	m_d	degeneracy
(100)	0.916	0.191	2	0.120	0.299	4
	0.191	0.418	4			
(110)	0.316	0.325	4	0.223	0.219	2
	0.191	0.418	2	0.082	0.361	2
(111)	0.260	0.359	6	1.590	0.082	1
				0.092	0.342	3

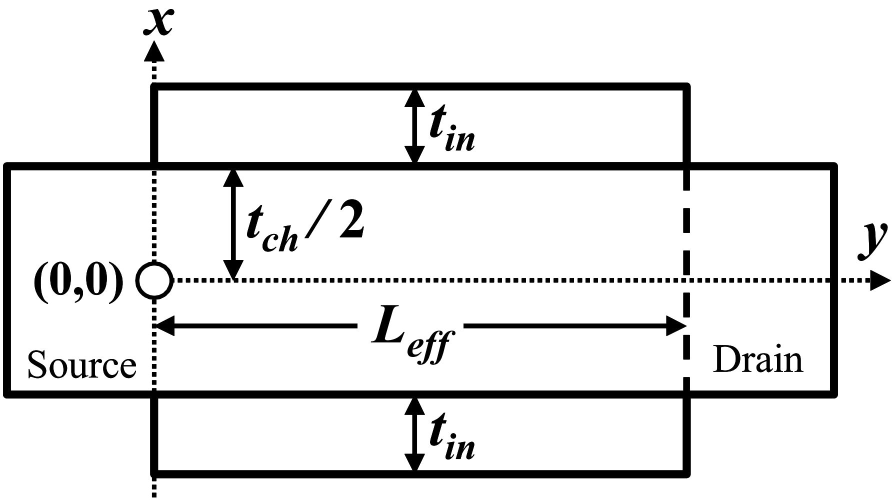


Figure 3-1 Schematic sketch of the FinFET structure investigated in this paper. L_{eff} is the channel length, t_{ch} is the channel thickness, and t_{in} is the gate insulator thickness.

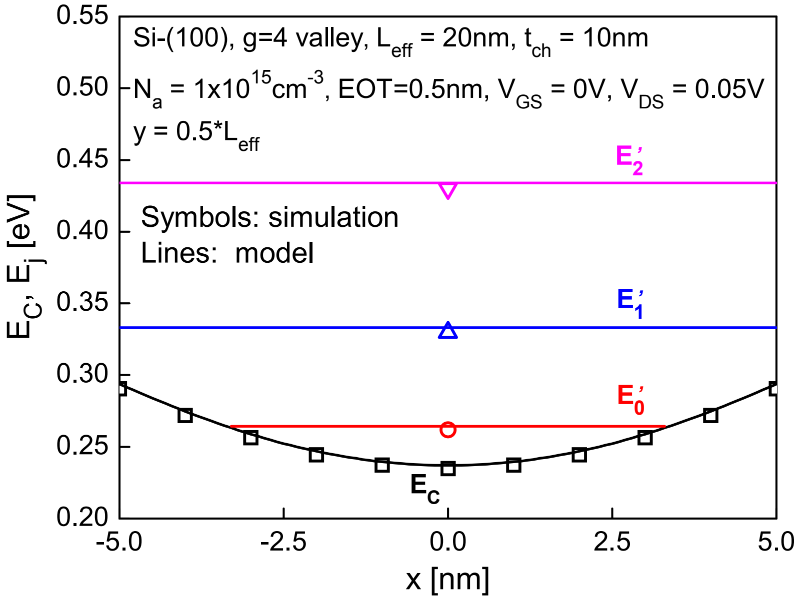


Figure 3-2 Conduction band edge and quantized eigen-energies of a short-channel lightly-doped FinFET.

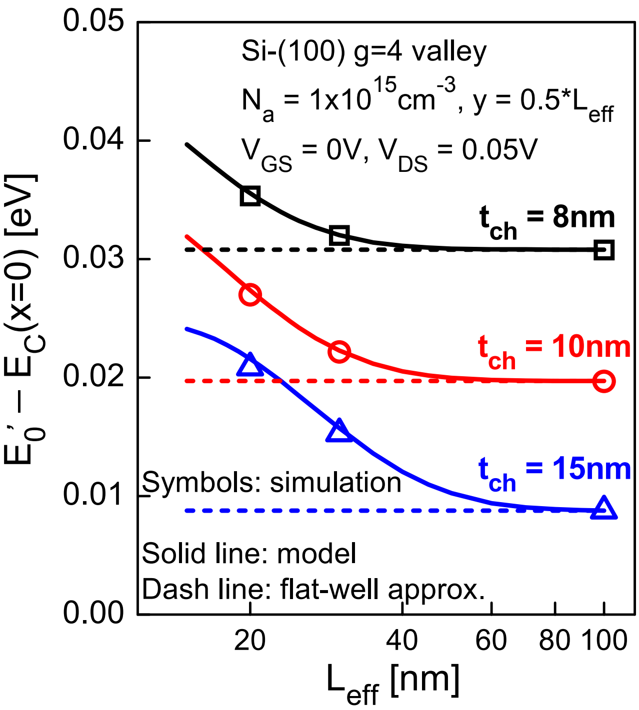


Figure 3-3 Channel length dependence of the E_0' for lightly-doped FinFETs with various t_{ch} showing the accuracy of our model.

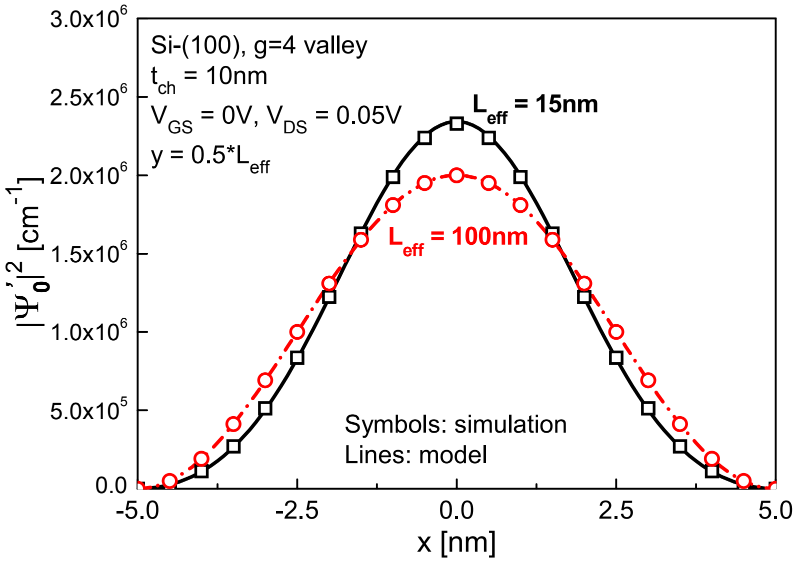


Figure 3-4 Comparison of the square of Ψ_0' for long-channel and short-channel FinFETs.

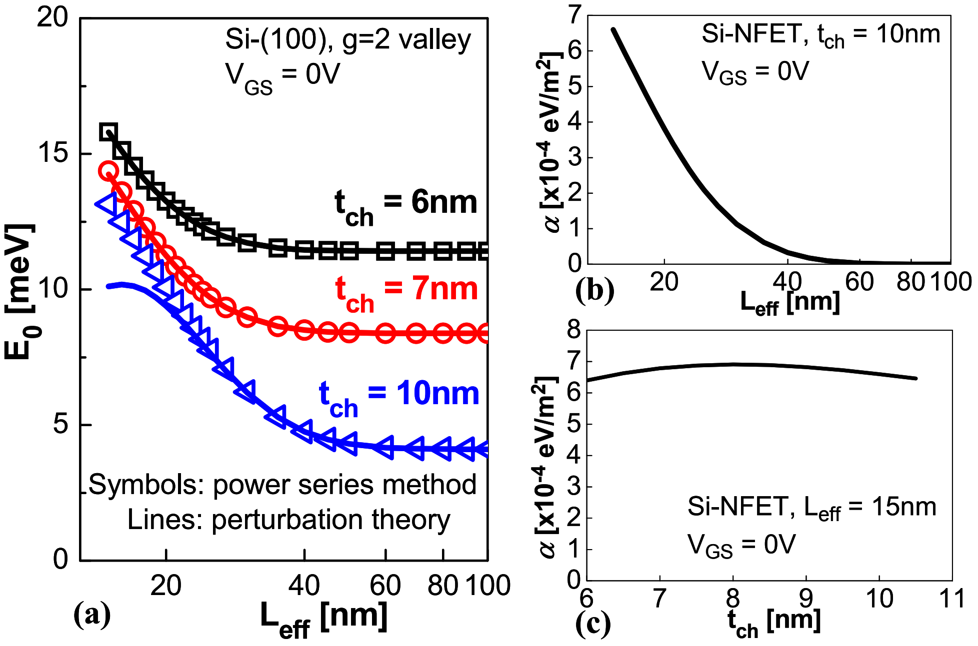


Figure 3-5 (a) Comparison of E_0 for various t_{ch} calculated from the power series method and the perturbation theory. (b) α dependence on L_{eff} for a given t_{ch}. (c) α dependence on t_{ch} for a given L_{eff}.

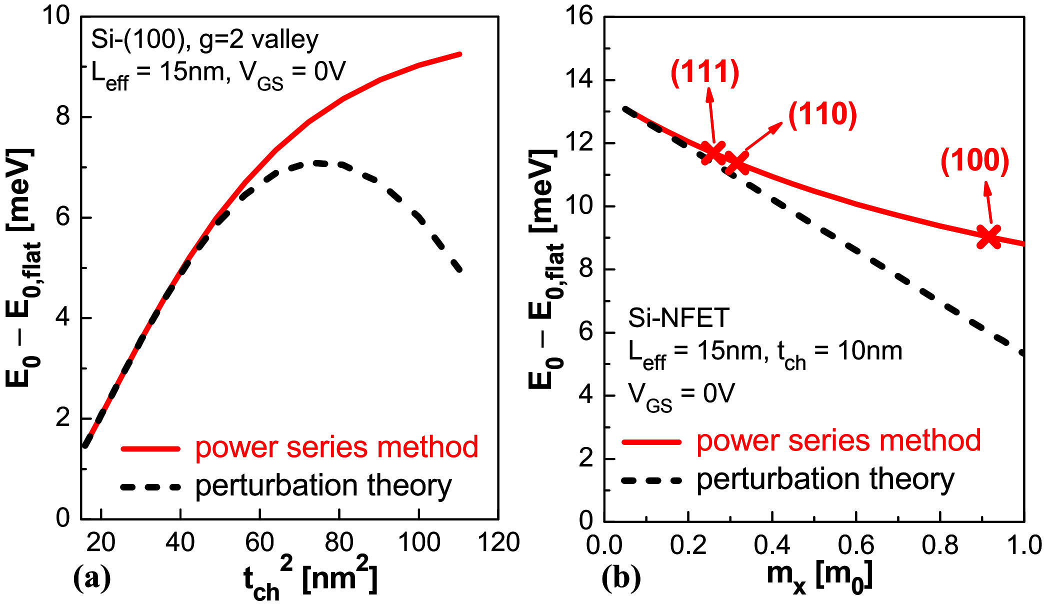


Figure 3-6 (a) The discrepancy of E_0 calculated by the perturbation theory and the power series method increases with t_{ch}^2. (b) The discrepancy of E_0 calculated by the perturbation theory and the power series method increases with m_x.

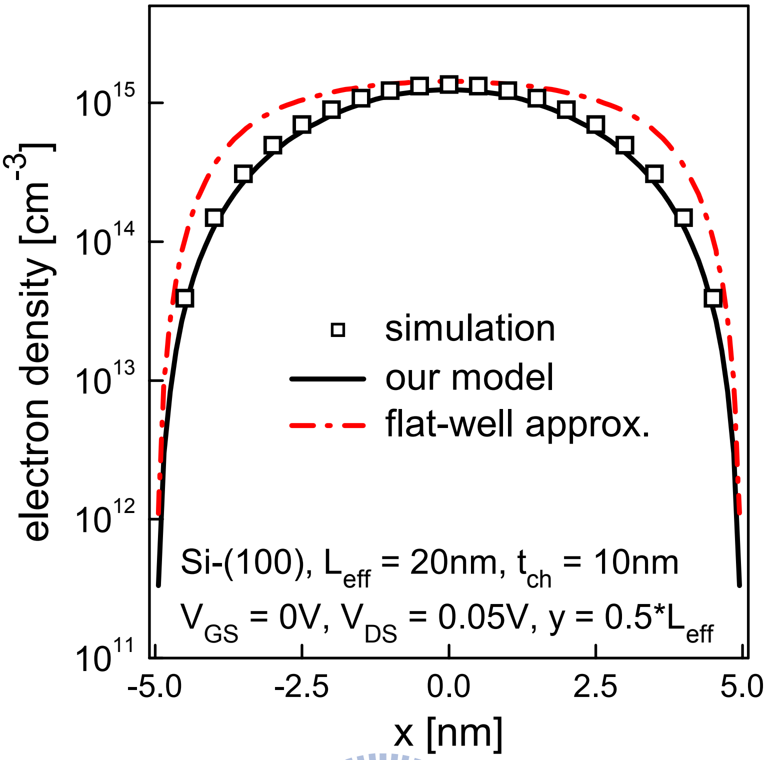


Figure 3-7 Comparison of the electron density calculated from our model and the model using the flat-well approximation.

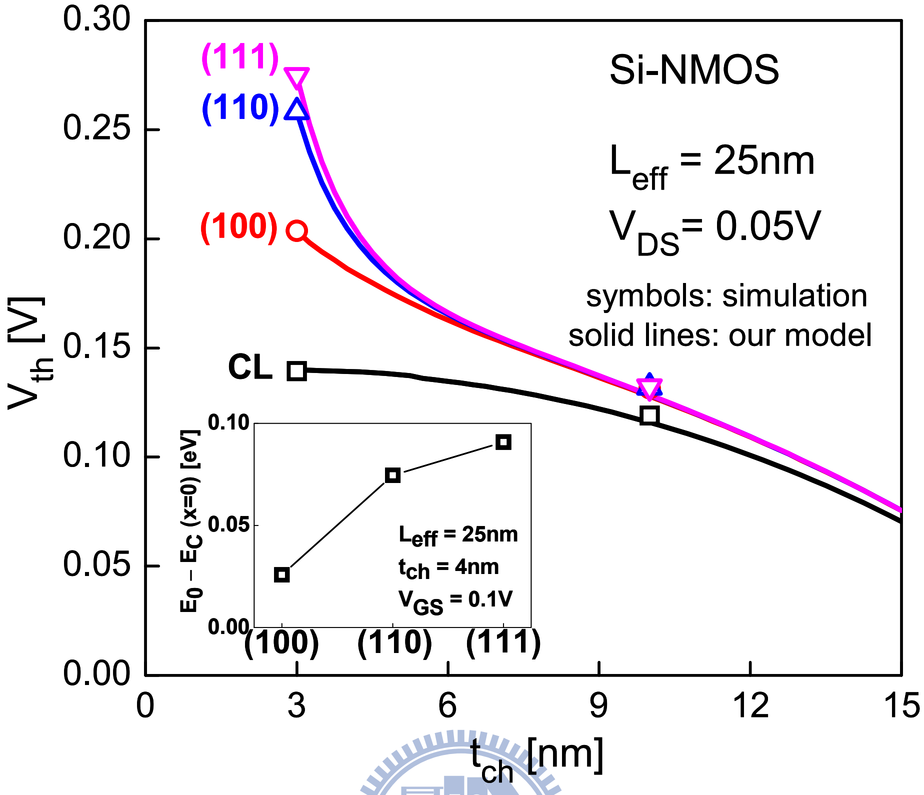


Figure 3-8 Comparison of the t_{ch} dependence of V_{th} for Si-FinFETs with various surface orientations and the classical model (CL). The V_{th} shift due to quantum confinement is mainly determined by the E_0 as indicated by the inset.

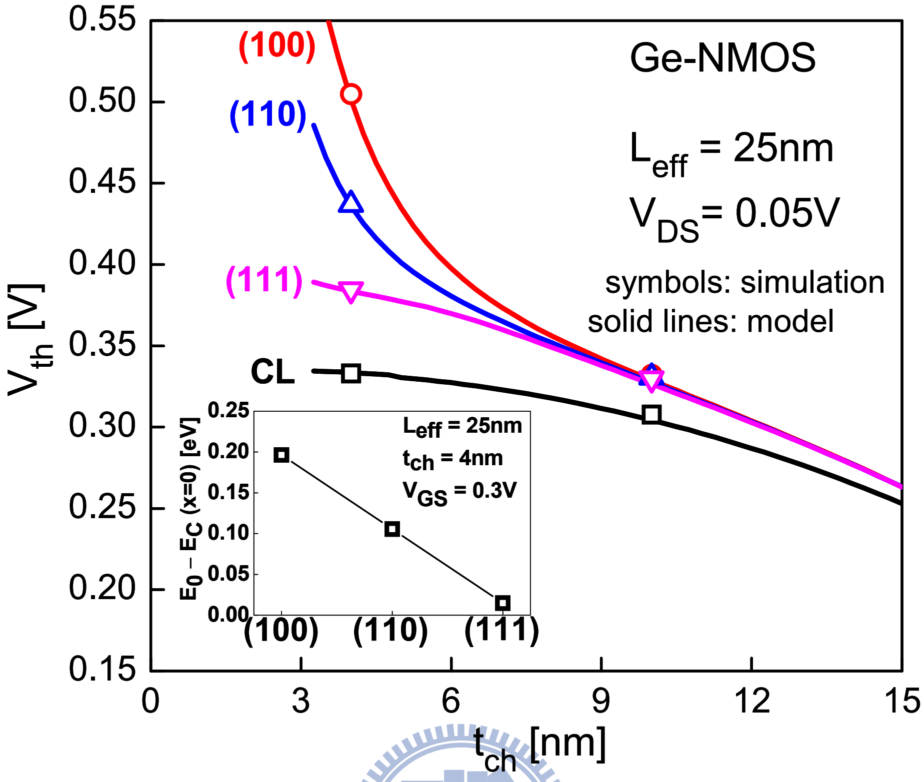


Figure 3-9 Comparison of the t_{ch} dependence of V_{th} for Ge-FinFETs with various surface orientations and the classical model (CL). The inset shows the comparison of the E_0 for various surface orientations.

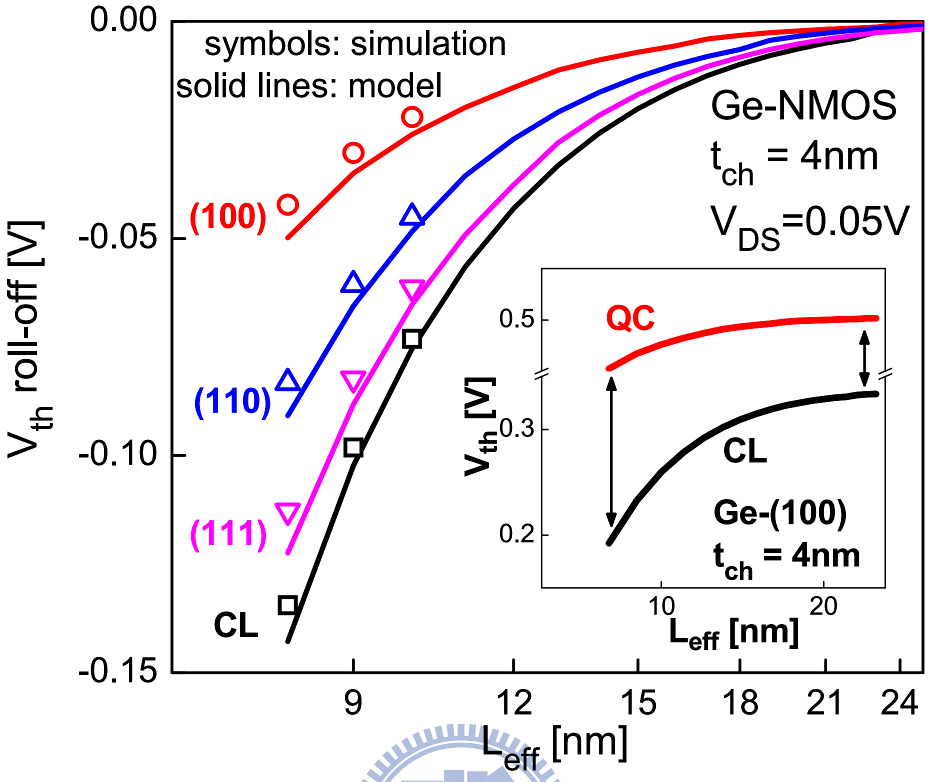


Figure 3-10 Comparison of the L_{eff} dependence of V_{th} (V_{th} roll-off) for Ge-FinFETs with various surface orientations and the classical model (CL). The V_{th} roll-off is defined as V_{th} (L_{eff}) – V_{th} (L_{eff} = 100nm). The inset indicates that the devices with smaller L_{eff} show larger V_{th} shift due to quantum-confinement (QC) effect than the devices with larger L_{eff}.

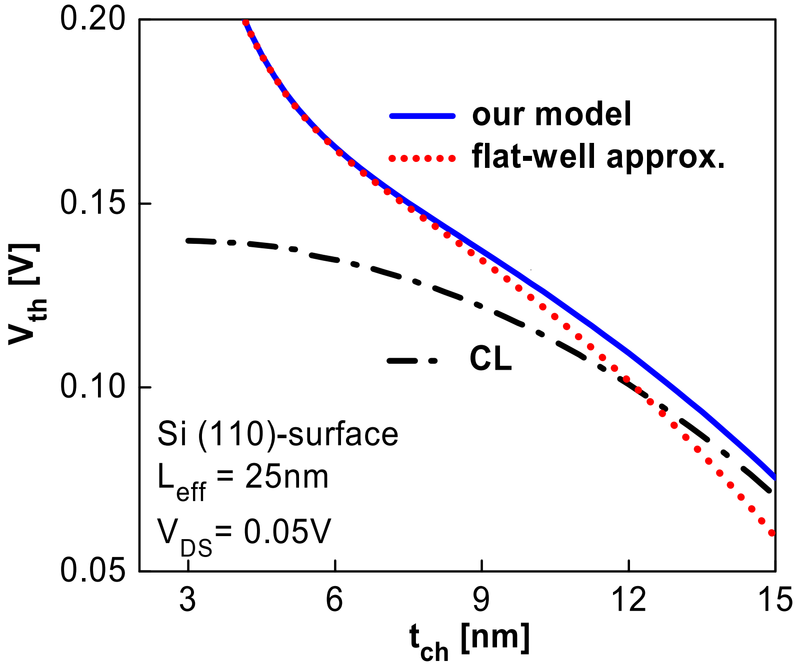


Figure 3-11 Comparison of the t_{ch} dependence of V_{th} of short-channel FinFETs calculated from the classical model (CL), our model, and the model using flat-well approximation.

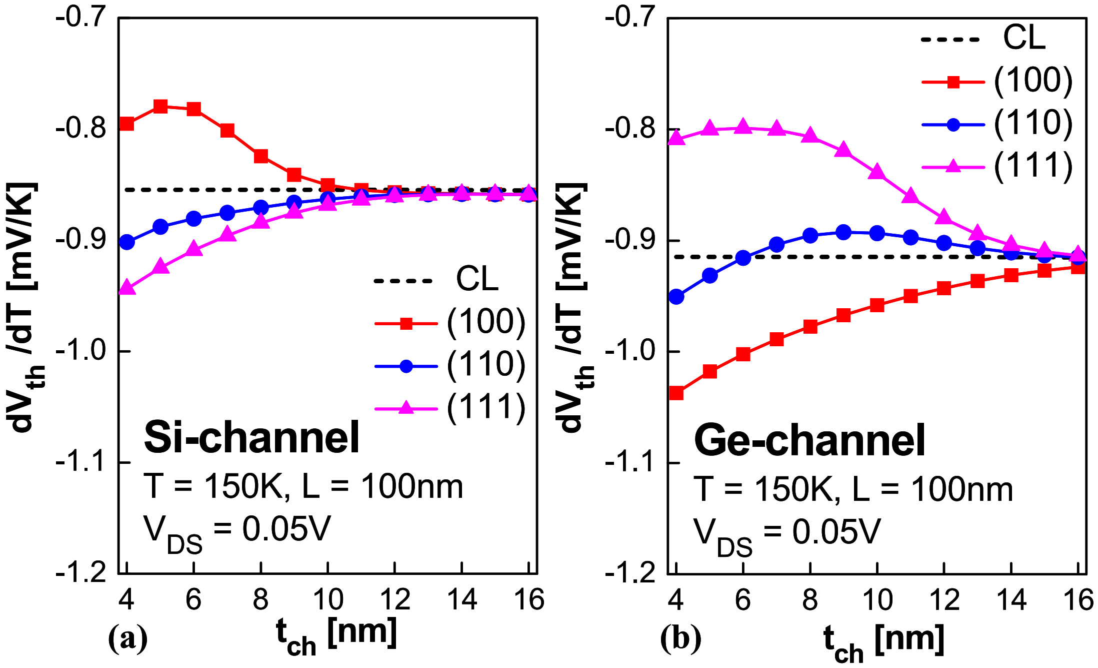


Figure 3-12 Model predicted dV_{th}/dT at 150K for (a) Si-NFET with various surface orientations (b) Ge-NFET with various surface orientations. Our calculations return to the classical result for devices with large t_{ch}, in which the quantum-confinement effect can be neglected.

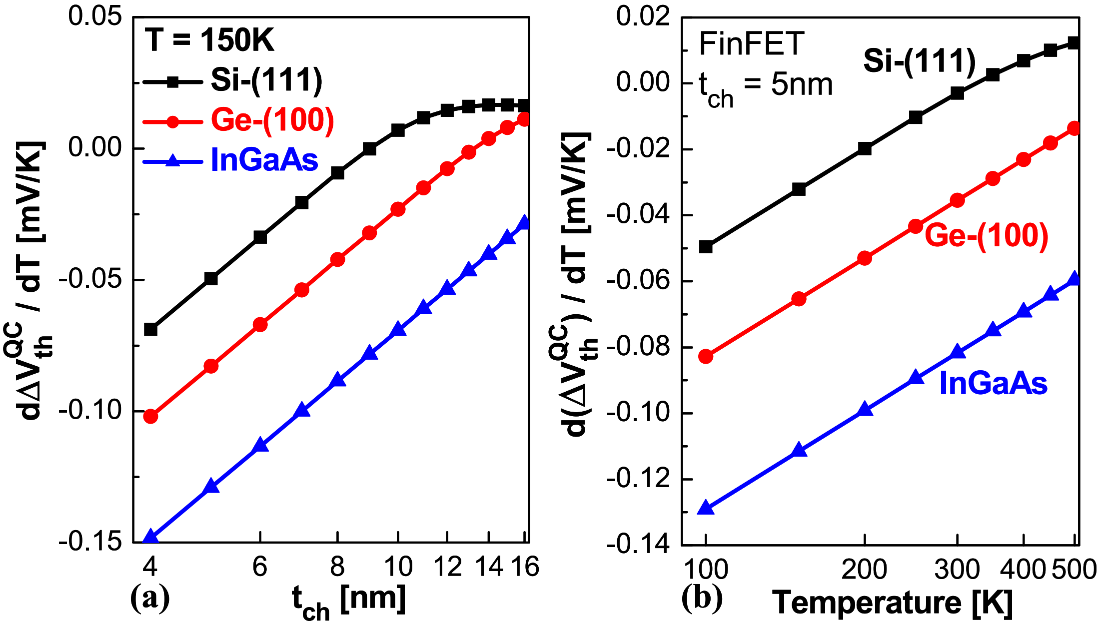
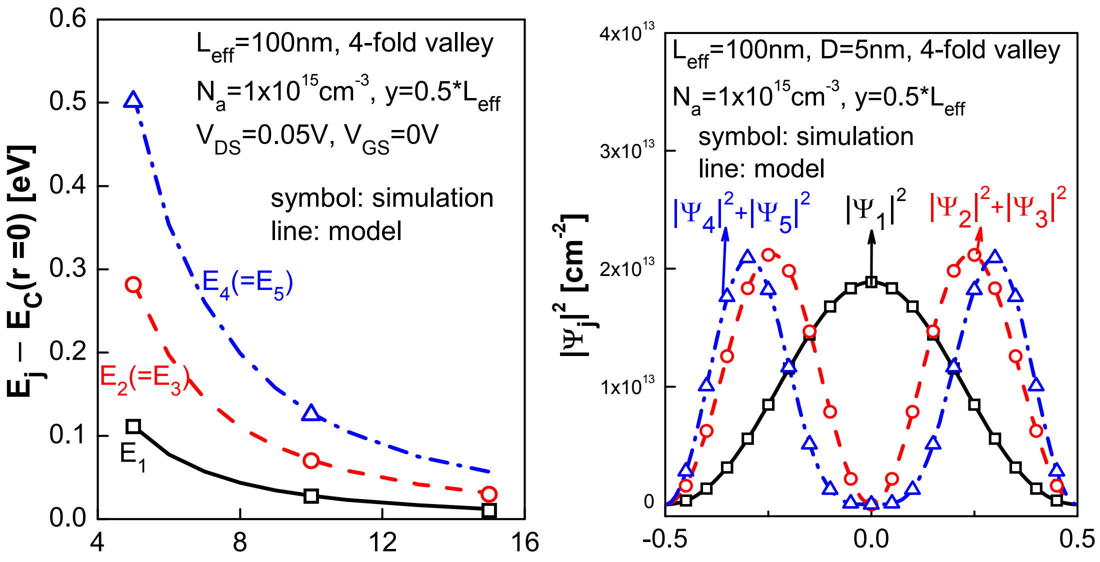


Figure 3-13 (a) The $d\Delta V_{th}^{QC}/dT$ depends on $\ln(t_{ch})$ with the slope independent of channel materials. (b) The $d\Delta V_{th}^{QC}/dT$ depends on $\ln(T)$ with the slope independent of channel materials.



(a) (b)

Figure 3-14 (a) Quantized eigen-energies for long-channel lightly-doped GAA devices. (b) The square of wavefunctions corresponding to the eigen-energies of GAA device with D=5nm in (a).

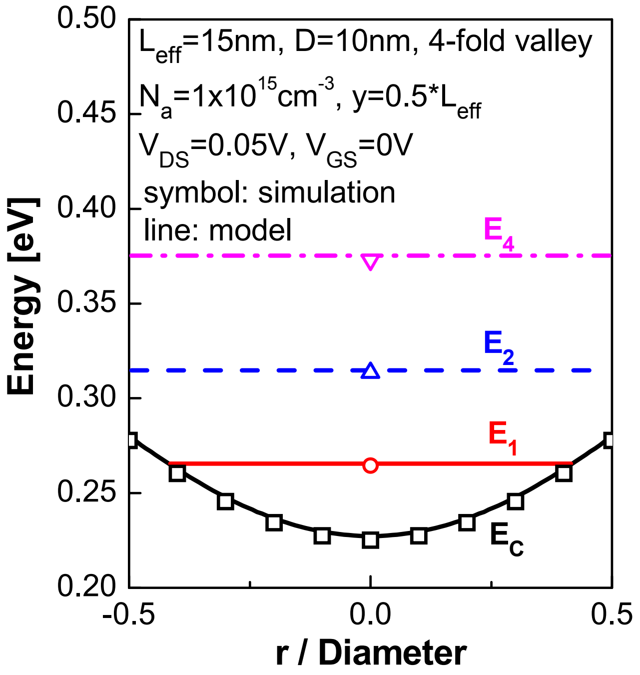


Figure 3-15 Conduction band edge and quantized eigen-energies of a short-channel lightly-doped GAA device.

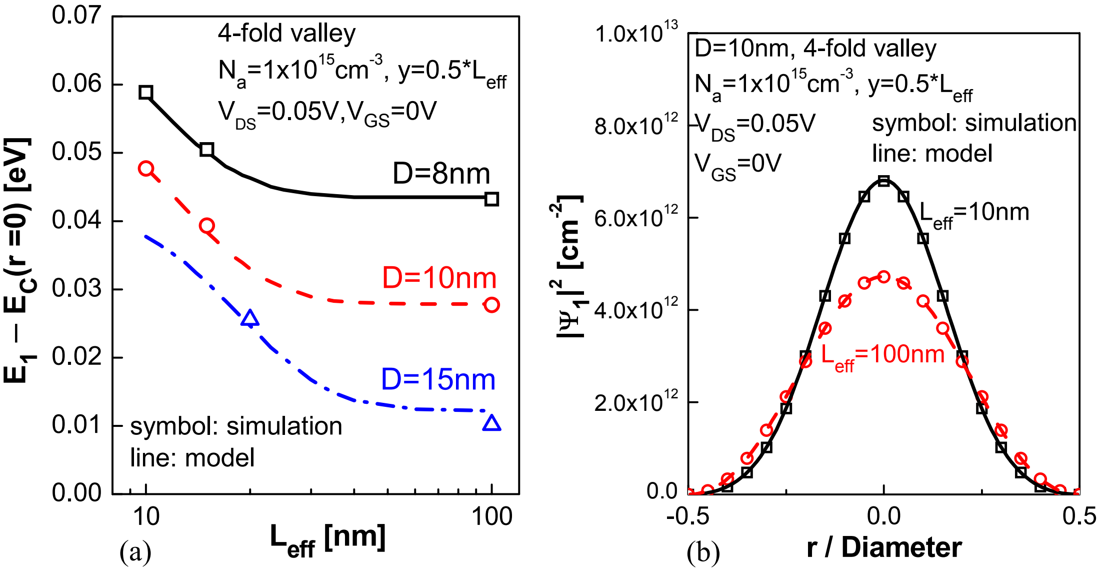


Figure 3-16 (a) Channel length dependence of the first eigen-energy for lightly-doped GAA devices with various channel diameter. (b) Comparison of the square of first eigen-function for long-channel and short-channel GAA MOSFETs.

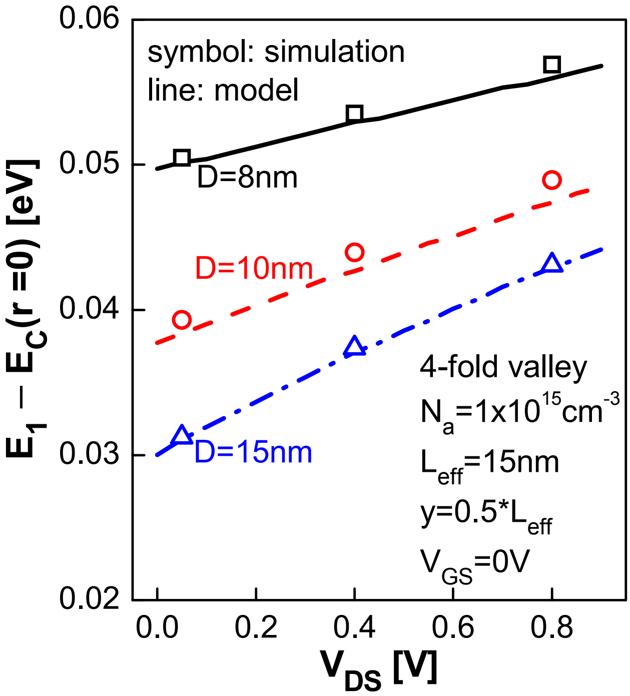
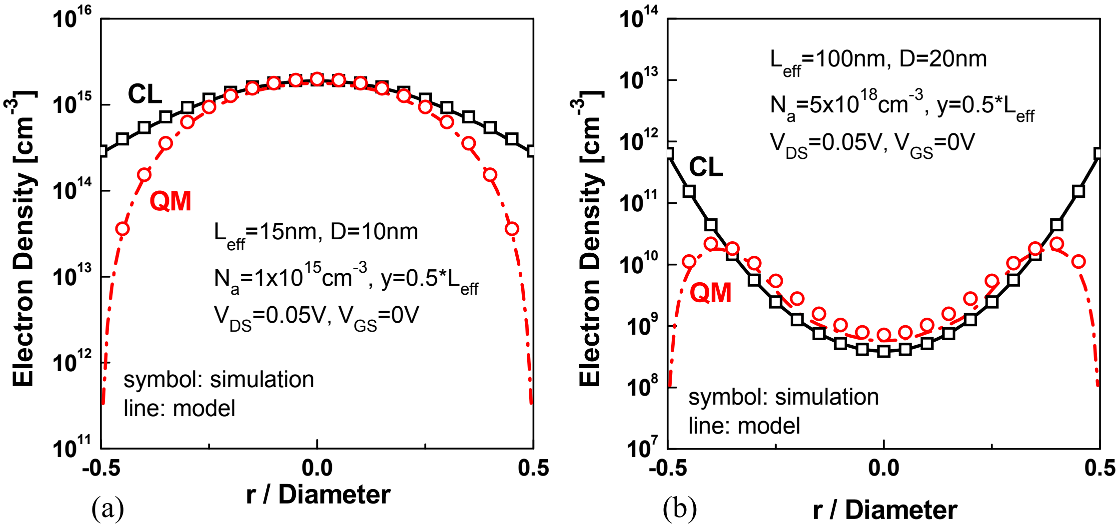


Figure 3-17 Drain bias dependence of the first eigen-energy of short-channel lightly-doped GAA devices with various channel diameter.



(a) (b)

Figure 3-18 Comparison of electron density distribution between classical model (CL) and quantum confinement model (QM). (a) Lightly-doped short-channel GAA device. (b) Heavily-doped long-channel GAA device.

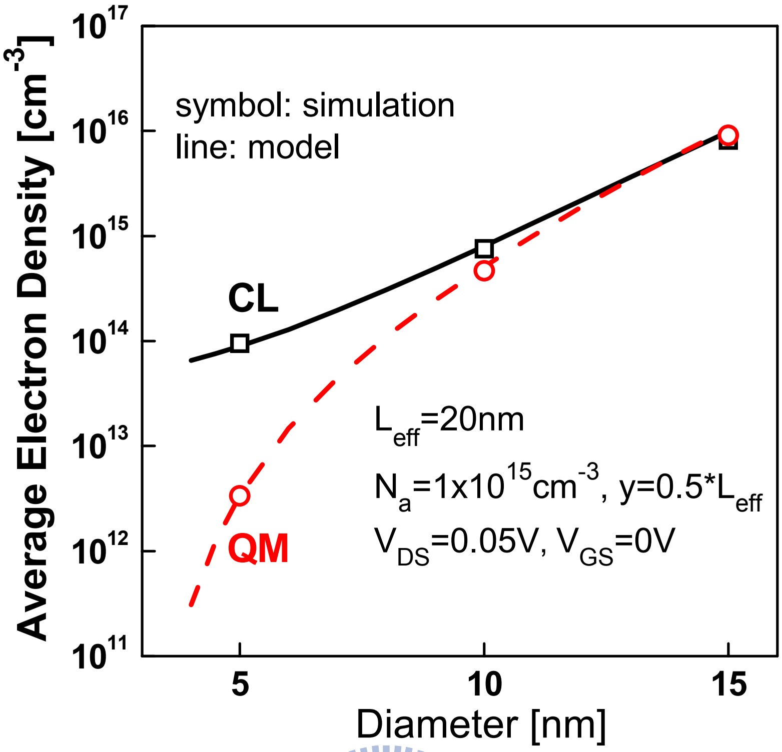


Figure 3-19 Comparison of average electron density between CL model and QM model for lightly-doped short-channel GAA MOSFETs with various channel diameter.

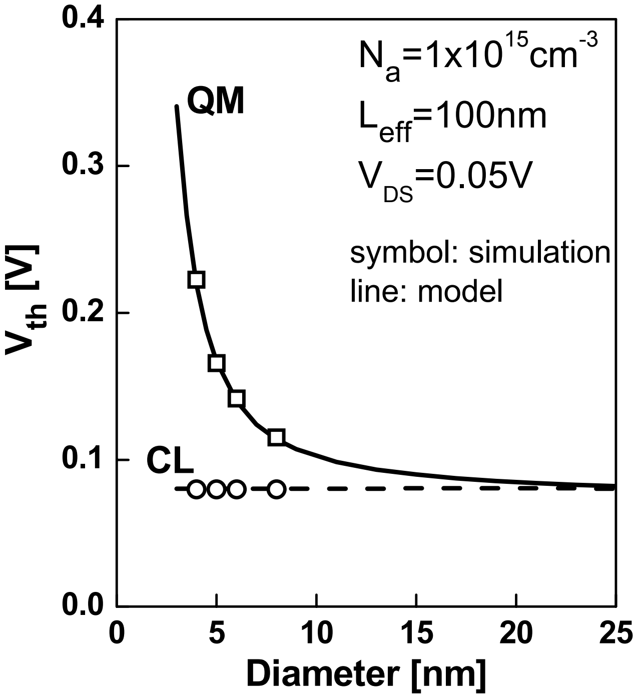


Figure 3-20 Channel diameter dependence of V_{th} for long-channel lightly doped devices calculated from classical (CL) model and quantum confinement (QM) model.

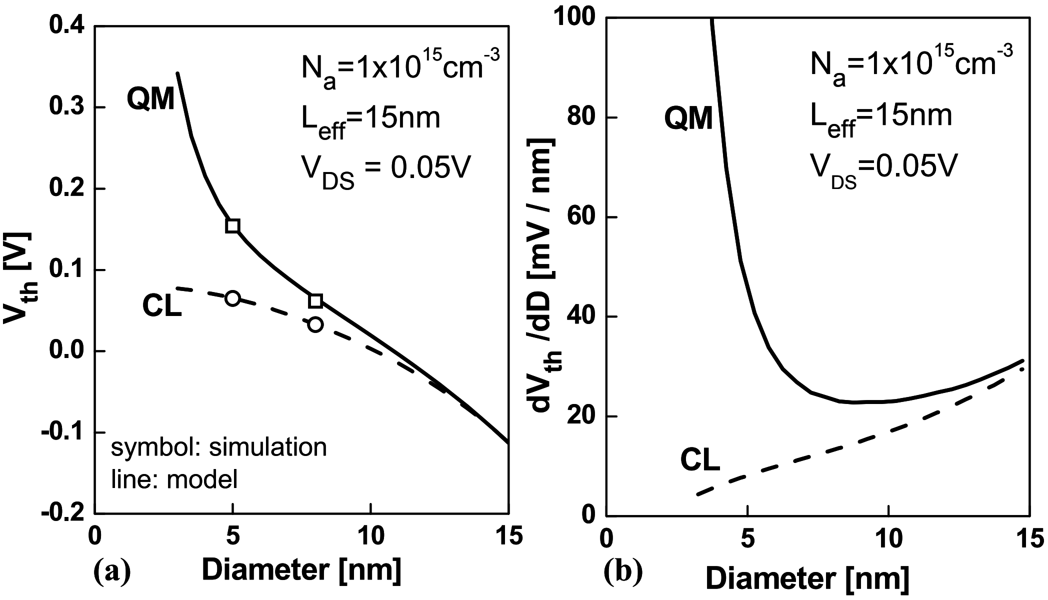


Figure 3-21 (a) Channel diameter dependence of $V_{th,CL}$ and $V_{th,QM}$. (b) V_{th} sensitivity to channel diameter (dV_{th}/dD) by classical model and quantum confinement model.

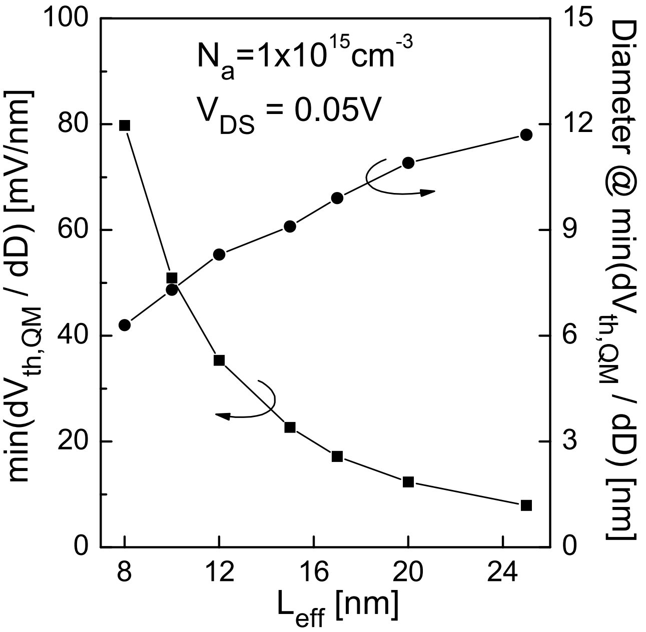


Figure 3-22 (Right) Optimized channel diameter for minimum dV_{th}/dD. (Left) The corresponding dV_{th}/dD for GAA devices with optimized channel diameter designs.

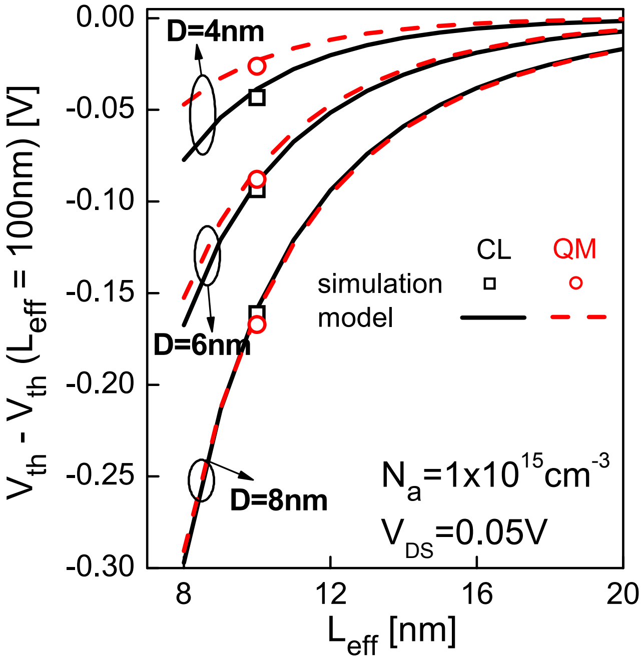


Figure 3-23 Comparison of V_{th} roll-off calculated from CL model and QM model.

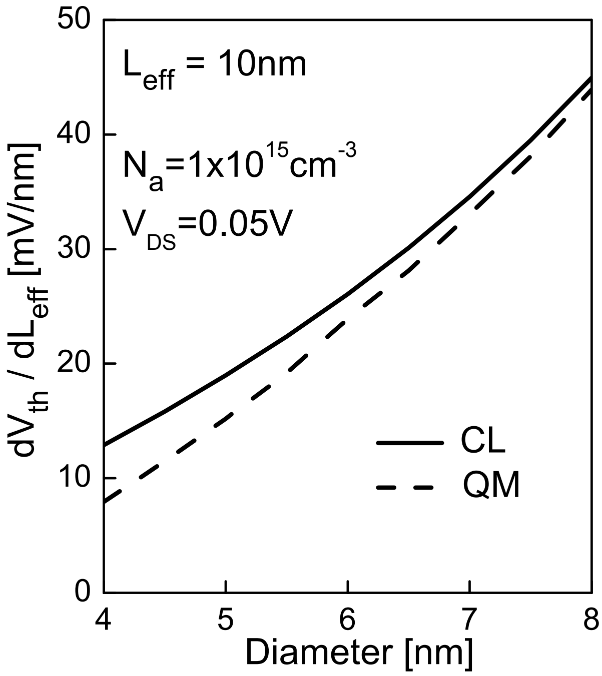


Figure 3-24 Comparison of channel diameter dependence of V_{th} sensitivity to L_{eff} (dV_{th}/dL_{eff}) calculated from CL model and QM model.

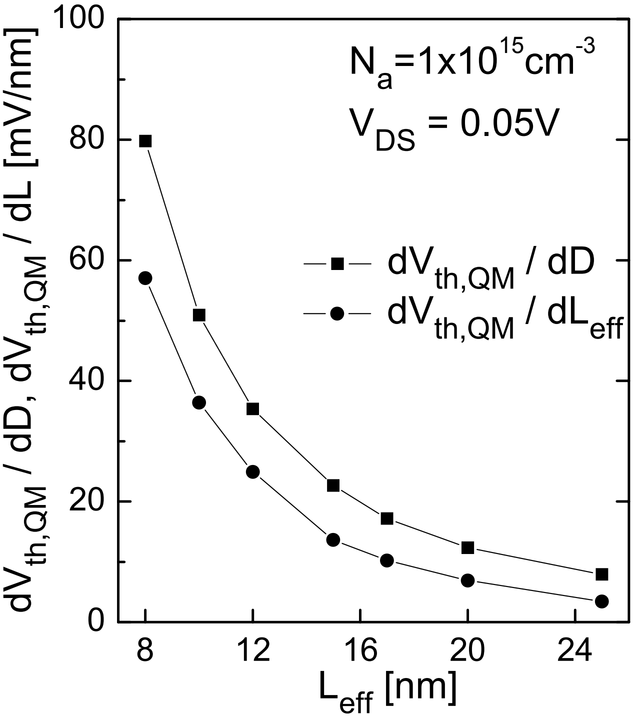


Figure 3-25 Comparison of $dV_{th,QM}/dD$ and $dV_{th,QM}/dL_{eff}$ for GAA MOSFETs with optimized channel diameter design for minimum $dV_{th,QM}/dD$ in Figure 3-22.

Chapter 4
Suppressed Threshold Voltage Roll-Off by Quantum-Confinement Effects for High Mobility Channel MOSFETs

4.1 Introduction

To attain sufficient drive current for highly-scaled MOSFETs, high mobility channel materials such as Ge and III-V materials have been proposed to enable the mobility scaling [1]. As the short-channel effects (SCEs) are more severe to these high mobility materials because of the higher permittivity, ultra-thin-body (UTB) [2], [3] and multi-gate structure [4]-[6] has been proposed to improve the device electrostatic integrity. With the scaling of channel dimension, the quantum-confinement effect becomes significant and may determine the electrostatic behavior and become crucial to the UTB and multi-gate device design. In this chapter, we tackle the problem using the analytically derived solutions of Schrödinger equation verified with TCAD simulation.

4.2 Quantum-Confinement Effect on V_{th} Roll-Off for UTB MOSFETs

Using density gradient model [7], Omura *et al.* [8] have observed increased V_{th} roll-off due to quantum confinement in UTB Si-on-insulator (SOI) devices. Whether there exists any difference between GeOI and SOI devices regarding the impact of quantum confinement on SCEs is not clearly known and merits investigation. We propose an analytical solution of Schrödinger equation for short-channel UTB devices to assess the impact of quantum confinement on V_{th} roll-off for UTB GeOI MOSFETs [9].

4.2.1 Analytical Solution of Schrödinger Equation for UTB MOSFETs

To consider the quantum-confinement (QC) effect along the channel thickness (i.e., x-) direction, the Schrödinger equation can be express as

$$-\frac{\hbar^2}{2m_x}\cdot\frac{d^2\Psi_j(x)}{dx^2}+E_C(x)\cdot\Psi_j(x)=E_j\cdot\Psi_j(x) \qquad (4\text{-}1)$$

where E_j is the j^{th} eigen-energy, $\Psi_j(x)$ is the corresponding wavefunction, and m_x is the carrier quantization effective mass. For long-channel undoped UTB MOSFETs, the conduction band edge $E_C(x)$ was usually treated as a triangular well [10]. However, to account for the source/drain coupling due to SCEs, the conduction band edge $E_C(x)$ in Equation (4-1) should be treated as a parabolic well with potential energy $E_C(x) = \alpha x^2 + \beta x + \gamma$ where α, β, and γ are channel-length-dependent coefficients and can be obtained from the channel potential solution of Poisson's equation under subthreshold region [11]. Using the parabolic-well approximation, the solution of Equation (4-1) can be expressed as $\Psi_j(x) = \sum d_n \cdot x^n$ with the coefficients d_n's:

$$d_2=-\frac{m_x}{\hbar^2}\left(E_j-\gamma\right)\cdot d_0 \qquad d_3=-\frac{m_x}{3\hbar^2}\left[\left(E_j-\gamma\right)\cdot d_1-\beta\cdot d_0\right]$$

$$d_n=-\frac{2m_x}{n(n-1)\hbar^2}\left[\left(E_j-\gamma\right)\cdot d_{n-2}-\beta\cdot d_{n-3}-\alpha\cdot d_{n-4}\right],\ n\geq 4 \qquad (4\text{-}2)$$

The j^{th} eigen-energy E_j can be determined by the boundary condition $\Psi_j(x=0) = \Psi_j(x=\mathrm{T_{ch}}) = 0$ where $x=0$ and $x=\mathrm{T_{ch}}$ (channel thickness) are defined as the interface positions of BOX/channel and channel/gate oxide, respectively. Thus, the eigen-energy and eigenfunction of short-channel UTB MOSFETs under subthreshold region can be derived. We have verified our model using the TCAD simulation that numerically solves the self-consistent solution of 2-D Poisson and 1-D Schrödinger equations [12]. Figure 4-1(a) and (b) show that for both the triangular potential well of long-channel devices and the parabolic well (due to SCEs) of short-channel ones, the E_j's calculated by our model are fairly accurate. It should be noted that a scalable quantum-confinement model with accurate channel length dependence is crucial to this study.

4.2.2 Enhanced and Suppressed V_{th} Roll-Off by Quantum-Confinement Effect

To assess the impact of quantum-confinement effect on V_{th}, the V_{th} is defined as the V_{GS} at which the average electron density of the cross-section at $y = y_{min}$ (the minimum potential along the carrier flow direction) exceeds a critical concentration equal to the channel doping. Note that the choice of other critical concentrations for determining V_{th} [13], [14] will result in a shift in V_{th}, but will not affect the results of V_{th} comparisons in this study. Using the calculated eigen-energies and wavefunctions, the electron density can be derived [15]. Figure 4-2 shows that the peak of electron density calculated by the classical (CL) model is not located at the channel/BOX interface (x=0) because the use of thin BOX (10nm) instead of thick BOX suppresses the buried-insulator-induced-barrier-lowering (BIIBL) [8]. Although the peak of electron density calculated by the quantum-confinement model is shifted toward the channel center, the main current flow paths predicted by both models are quite similar for the UTB structure with thin BOX.

Figure 4-3 shows that for GeOI MOSFETs with channel thickness (T_{ch}) = 10nm, the V_{th} roll-off (defined as $V_{th}(L)–V_{th}(L=100nm)$) predicted by the quantum-confinement model is larger than that predicted by the CL model. This is consistent with the result reported for SOI MOSFET [8], and can be explained as follows. The V_{th} shift due to the quantum-confinement effect can be expressed as $\Delta V_{th}^{QM} \cong S/(\ln 10 \cdot kT/q) \cdot \Delta\psi_s^{QM}$ with S being the subthreshold swing and $\Delta\psi_s^{QM}$ being the equivalent surface potential shift due to the quantum-confinement effect [10], [16]. The inset of Figure 4-3 shows that for GeOI devices with larger T_{ch} (10nm), the "electrical confinement" [10] dominates the carrier quantization. The E_0 (ground-state energy) of the triangular well (for long-channel devices) is much larger than that of the parabolic well (for short-channel devices) because of the larger electric field in the triangular one. As $\Delta\psi_s^{QM}$ is mainly determined by E_0, the $\Delta\psi_s^{QM}$ and thus ΔV_{th}^{QM} for the long-channel device is larger than that of the short-channel one. Therefore, the V_{th} roll-off considering the quantum-confinement effect is larger.

As the T_{ch} scales down, however, a different trend can be observed. Figure 4-4 shows that for GeOI MOSFETs with T_{ch} = 5nm, the V_{th} roll-off predicted by the QC model becomes smaller than that predicted by the CL model, which is opposite to the larger T_{ch} case and [8]. This can not be explained by the reduction of BIIBL due to the quantum-confinement effect [8] because in this study, thin BOX (T_{BOX} = 10nm) is used and the impact of BIIBL is not significant (see Figure 4-2). Since the "structural confinement" [10] dominates the carrier quantization for GeOI devices with smaller T_{ch} (5nm), the inset of Figure 4-4 shows that the E_0 (and hence $\Delta\psi_s^{QM}$) of the long-channel device is close to that of the short-channel one. Nevertheless, due to the SCE, the subthreshold swing S of the short-channel device is larger than the long-channel one. Therefore, the ΔV_{th}^{QM} of the short-channel device is larger than that of the long-channel device and the V_{th} roll-off considering the quantum-confinement effect is smaller. This mechanism is important because it may alter the comparison result for V_{th} roll-off between Si, Ge, and $In_{0.53}Ga_{0.47}As$ devices. Figure 4-5 shows that, contrary to the prediction of CL model, the V_{th} roll-off for InGaAs device is smaller than the Si counterpart because of the QC effect. Moreover, a crossover can be seen when Si and Ge devices are compared, and Ge device exhibits better V_{th} roll-off than the Si counterpart as T_{ch} < 4nm.

In summary, depending on T_{ch}, the quantum-confinement effect may increase or decrease the SCE of UTB devices. The critical channel thickness ($T_{ch,crit}$) determining whether the quantum-confinement effect enhances or decreases the V_{th} roll-off depends on the BOX thickness (T_{BOX}) and the channel material. Figure 4-6 shows that the $T_{ch,crit}$ of GeOI

MOSFETs increases with T_{BOX}. In addition, for a given T_{BOX}, the $T_{ch,crit}$ of SOI MOSFETs is smaller than that of the GeOI MOSFETs. This may explain why the suppression of V_{th} roll-off by the quantum-confinement effect was not observed for the UTB SOI devices (with T_{ch} = 10nm) in [8].

4.3 Two-Dimensional Quantum-Confinement Effect for Multi-Gate MOSFETs

For multi-gate devices, the 2-D quantum-confinement effect along the W_{fin} and H_{fin} directions may determine the electrostatic behavior and become crucial to the multi-gate device design. Since the impact of quantum-confinement effect is especially important to $In_{0.53}Ga_{0.47}As$ channel because of its small effective mass, we assess this 2-D quantum-confinement effect on the V_{th} roll-off of $In_{0.53}Ga_{0.47}As$ multi-gate MOSFETs using a derived analytical solution of 2-D Schrödinger equation verified with TCAD simulation.

4.3.1 Analytical Solution of Schrödinger Equation for Multi-Gate MOSFETs

To consider the 2-D QC effect in the W_{fin} (i.e., x) and H_{fin} (i.e., z) directions, the Schrödinger equation can be expressed as

$$-\frac{\hbar^2}{2}\left(\frac{1}{m_x}\frac{\partial^2}{\partial x^2}+\frac{1}{m_z}\frac{\partial^2}{\partial z^2}\right)\Psi_{i,j}(x,z)+E_C(x,z)\cdot\Psi_{i,j}(x,z)=E_{i,j}(x,z)\cdot\Psi_{i,j}(x,z) \qquad (4\text{-}3)$$

where i and j are the principle quantum numbers for the carrier quantization in the W_{fin} and H_{fin} directions, respectively. $E_{i,j}$ is the eigen-energy of the (i, j)-state, $\Psi_{i,j}(x,z)$ is the corresponding wavefunction, m_x and m_z are the carrier quantization effective mass in the W_{fin} and H_{fin} directions, respectively. For $In_{0.53}Ga_{0.47}As$ with isotropic effective mass, $m_x = m_z = 0.04m_0$ [17] is used. For an undoped multi-gate device, the conduction band edge $E_C(x,z)$ was usually assumed as a flat well [18], [19]. However, to account for the source/drain coupling due to SCEs, the $E_C(x,z)$ in Equation (4-3) should be treated as a parabolic well with potential energy $E_C(x,z) = (\alpha_x \cdot x^2) + (\alpha_z \cdot z^2 + \beta_z \cdot z) + \gamma$, where α_x, α_z, β_z, and γ are length-dependent coefficients and can be obtained from the channel potential solution of Poisson's equation under subthreshold region as derived in Chapter 2. Using this parabolic-well treatment and separation of variables technique, the solution of Equation (4-3) can be expressed as $\Psi_{i,j}(x,z) = W_i(x) \cdot H_j(z) = (\Sigma d_m \cdot x^m) \cdot (\Sigma e_n \cdot z^n)$ with the coefficients d_m's and e_n's being determined by the following recurrence relationships:

$$d_2 = -\frac{m_x}{\hbar^2} E_{W,i} \cdot d_0 \qquad d_3 = -\frac{m_x}{3\hbar^2} E_{W,i} \cdot d_1$$

$$d_{m+2} = -\frac{2m_x}{(m+1)(m+2)\hbar^2}\left[E_{W,i} \cdot d_m - \alpha_x \cdot d_{m-2}\right],\ m \geq 2 \tag{4-4a}$$

$$e_2 = -\frac{m_z}{\hbar^2}\left(E_{H,j} - \gamma\right) \cdot e_0 \qquad e_3 = -\frac{m_z}{3\hbar^2}\left[\left(E_{H,j} - \gamma\right) \cdot e_1 - \beta_z \cdot e_0\right]$$

$$e_{n+2} = -\frac{2m_z}{(n+1)(n+1)\hbar^2}\left[\left(E_{H,j} - \gamma\right) \cdot e_n - \beta_z \cdot e_{n-1} - \alpha_z \cdot e_{n-2}\right],\ n \geq 2 \tag{4-4b}$$

The eigen-energy $E_{i,j}$ can be determined by the boundary conditions that the wavefunction vanishes at the channel/ insulator interfaces, and can be expressed as $E_{i,j} = E_{W,i} + E_{H,j}$, where $E_{W,i}$ is the i^{th} eigen-energy derived by $W_i(x = 0) = W_i(x = \mathrm{W_{fin}}) = 0$, and $E_{H,j}$ is the j^{th} eigen-energy derived by $H_j(z = 0) = H_j(z = \mathrm{H_{fin}}) = 0$. Thus, the eigen-energy and wavefunction for a short-channel multi-gate MOSFET under subthreshold region can be derived.

We have verified our model using the TCAD simulation that numerically solves the self-consistent solution of 3-D Poisson and 2-D Schrödinger equations [12]. Figure 4-7(a) shows that our model can predict the asymmetric ground-state wavefunction $\Psi_{0,0}$ along the $\mathrm{H_{fin}}$ direction due to the asymmetric gate configuration (and hence the asymmetric E_C) in the

H_{fin} direction. For long-channel multi-gate devices, this E_C asymmetry along the H_{fin} direction results in larger eigen-energy than that predicted by the flat-well approximation, as shown in Figure 4-7(b). For short-channel devices, the SCEs further alter the E_C and hence increase the eigen-energy. Thus, in contrast to the constant $E_{0,0}–E_{C,min}$ ($E_{C,min}$ is the minimum E_C for a given x-z cross-section) calculated by the flat-well approximation, both the TCAD simulation and our model show that the $E_{0,0}–E_{C,min}$ varies with the L_{eff}. It should be noted that a scalable QC model with accurate L_{eff} and H_{fin} dependences is crucial to this study.

4.3.2 Suppressed V_{th} Roll-Off for InGaAs Multi-Gate MOSFET

To assess the impact of quantum-confinement effect on the V_{th} roll-off, the V_{th} is defined as the gate voltage at which the subthreshold current equal to $300nA \times W_{total}/L_{eff}$, where $W_{total} = 2H_{fin} + W_{fin}$ is the total width of the multi-gate device. Using the calculated eigen-energies and wavefunctions, the subthreshold current considering the QC effect can be derived. Figure 4-8 shows the V_{th} roll-off [defined as $V_{th}(L_{eff}=100nm)–V_{th}(L)$] for InGaAs multi-gate devices predicted by the quantum-confinement model is smaller than that predicted by the classical (CL) model, and the discrepancy becomes larger with decreasing H_{fin}. In other words, the enhanced 2-D quantum-confinement effect due to H_{fin} down-scaling suppresses the V_{th} roll-off of InGaAs multi-gate MOSFETs. This can be explained as follows.

The QC effect increases the V_{th}, and this quantum-confinement induced V_{th} shift (ΔV_{th}^{QC}) can be expressed as $S/(\ln 10 \cdot kT/q) \cdot \Delta\psi_s^{QC}$ [16], as mentioned in Section 4.2.2. Since the short-channel device exhibits larger S, Figure 4-9(a) shows that the ΔV_{th}^{QC} for the short-channel device is larger than that for the long-channel device. In other words, the V_{th} roll-off of InGaAs devices is reduced by the quantum-confinement effect. Figure 4-9(b) shows that down-scaling H_{fin} increases the ground-state eigen-energy $E_{0,0}$ and hence the $\Delta\psi_s^{QC}$ of InGaAs devices. That is, the ΔV_{th}^{QC} for a short channel InGaAs multi-gate device can be raised by the quantum confinement along the H_{fin} direction, and hence the V_{th} roll-off can be significantly improved. It is also worth noting that this 2-D quantum-confinement effect on V_{th} roll-off for multi-gate devices with the Ge channel will not be as significant as the InGaAs counterpart, as indicated in Figure 4-9(b).

Figure 4-10 shows that, contrary to the prediction of the CL model, a discrepancy can be seen when the V_{th} roll-off for InGaAs and Ge multi-gate devices are compared. The CL model predicts that the V_{th} roll-off of InGaAs devices is similar with the Ge counterpart. With decreasing H_{fin}, however, the 2-D quantum-confinement effect for InGaAs devices becomes significant, and results in significantly smaller V_{th} roll-off than the Ge counterparts.

4.4 Scalability of Ge and InGaAs Channel Multi-Gate MOSFETs

Using the derived analytical solution of 2-D Schrödinger equation in 4.3.1, we can investigate the scalability of high-mobility Ge and InGaAs multi-gate devices with various aspect ratio (AR). With this physical and predictive approach, we can efficiently evaluate the Ge and InGaAs multi-gate devices in a wide design space.

The contours of SS and V_{th} roll-off [$V_{th}(L_{eff}$=100nm)–$V_{th}(L_{eff}$=17nm)] considering the QC effect in the W_{fin} and H_{fin} domain can be efficiently derived using our theoretical model. Figure 4-11(a) shows that to achieve a given SS criterion, various AR designs can be chosen. When we further assess the contours of $V_{th,QC}$ roll-off, Figure 4-11(b) shows that the $V_{th,QC}$ roll-off contours are not parallel to those of SS for InGaAs devices. As shown in Figure 4-12, for multi-gate devices with the same SS, the $V_{th,QC}$ roll-off decreases with the AR. This stems mainly from the 2-D quantum-confinement effect demonstrated in 4.3.2. In addition to the carrier confinement along the W_{fin} direction, the confinement along the H_{fin} direction becomes significant with decreasing AR (i.e., H_{fin}). Thus, the eigen-energy (and hence the quantum-confinement induced V_{th} shift) increases (Figure 4-13) with decreasing AR. The suppression of V_{th} roll-off due to this 2-D quantum-confinement effect is more significant than the 1D-confinement effect. Therefore, as compared with the AR dependence of the classical V_{th} roll-off, Figure 4-12 shows that the $V_{th,QC}$ roll-off exhibits more significant decrease with the AR after considering the 2-D quantum-confinement effect.

Using the contours in Figure 4-14(a), Figure 4-14(b) shows that to maintain a given SS, the W_{fin} required for low-AR devices is larger than that for high-AR devices. This is consistent with the result in [20]. Thus, the Tri-gate (AR=1) is more scalable than the FinFET (AR>1). In addition to the advantage of scalability, Figure 4-14 indicates that for a given SS, the $V_{th,QC}$ roll-off for Tri-gate is smaller than FinFET because of the more significant 2-D confinement effect for Tri-gate (as explained in Figure 4-12).

Figure 4-14(a) compares the SS contours for Ge and InGaAs multi-gate devices. It can be seen that the InGaAs devices exhibit smaller SS than the Ge counterpart because of the smaller permittivity. Thus, to maintain a given SS, Figure 4-14(b) shows that the InGaAs device possesses more relaxed W_{fin} than the Ge counterpart. Figure 4-15 shows that the $V_{th,QC}$ roll-off for the InGaAs device is smaller than the Ge counterpart. This is because the degree of quantum confinement for InGaAs devices is larger and hence the improvement of V_{th} roll-off is more significant (Figure 4-13). Thus, the InGaAs devices possess better scalability and smaller $V_{th,QC}$ roll-off than the Ge devices.

4.5 Summary

In this chapter, we investigate the impact of quantum-confinement on the short-channel effect of UTB and multi-gate MOSFETs using derived analytical solutions of Schrödinger equation verified with TCAD simulation. Our study indicates that when the T_{ch} is smaller than critical thickness, the quantum-confinement effect may decrease the V_{th} roll-off of GeOI MOSFETs. Thus, Ge devices may exhibit better V_{th} roll-off than the Si counterpart because of more significant quantum confinement. For multi-gate structure, by exploring the quantum-confinement effect along the H_{fin} direction, the V_{th} roll-off of InGaAs devices can be suppressed and become smaller than the Ge counterpart. This 2-D quantum-confinement effect is also crucial to the scalability of multi-gate device. By exploring a wide design space with various aspect ratio (AR), our study indicates that for a given subthreshold swing, Tri-gate (AR=1) with significant 2-D confinement effect exhibits better V_{th} roll-off than FinFET (AR>1).

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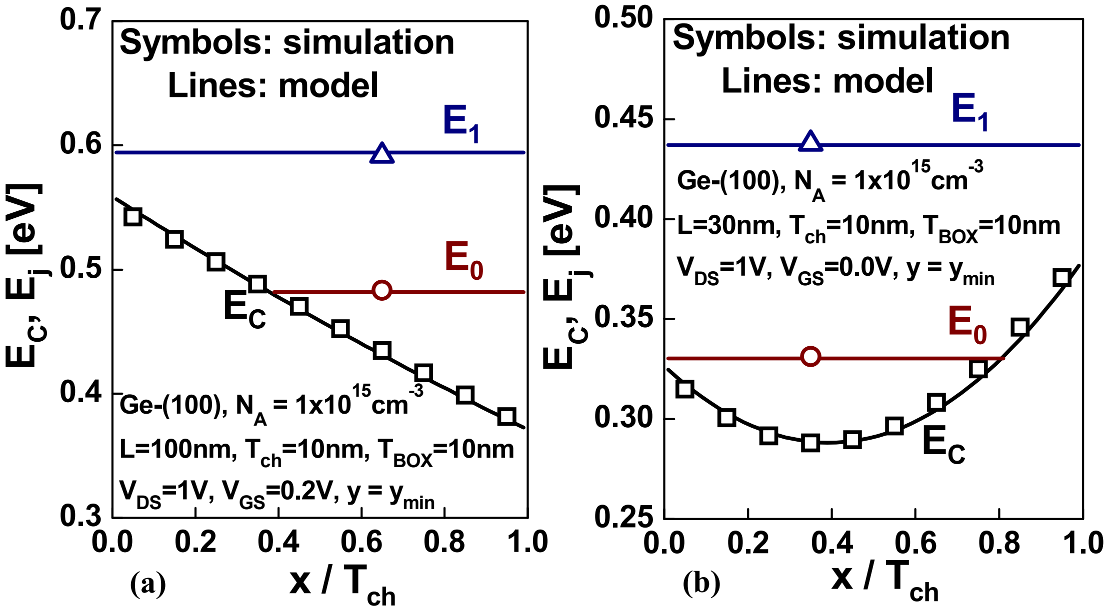

Figure 4-1 Conduction band edge and quantized eigen-energies of lightly doped GeOI MOSFETs. (a) A long-channel device with triangular well. (b) A short-channel device with parabolic well.

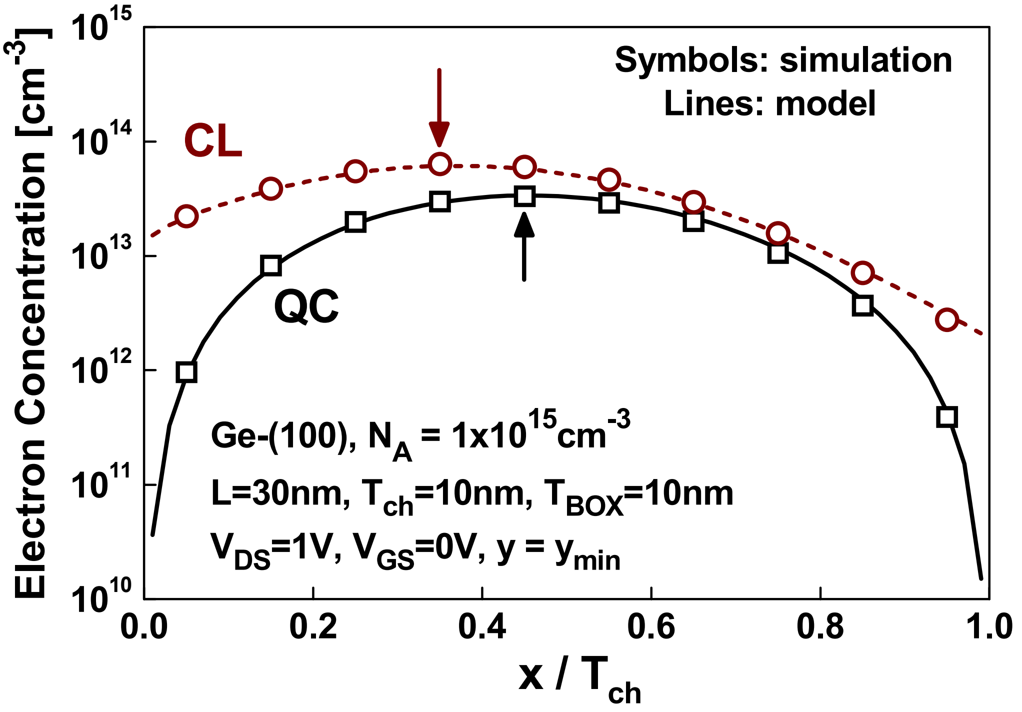

Figure 4-2 Comparison of the electron density distribution with and without considering quantum-confinement (QC) effect. The electron density is calculated from 2-D density-of-states, eigen-energies, and wavefunctions.

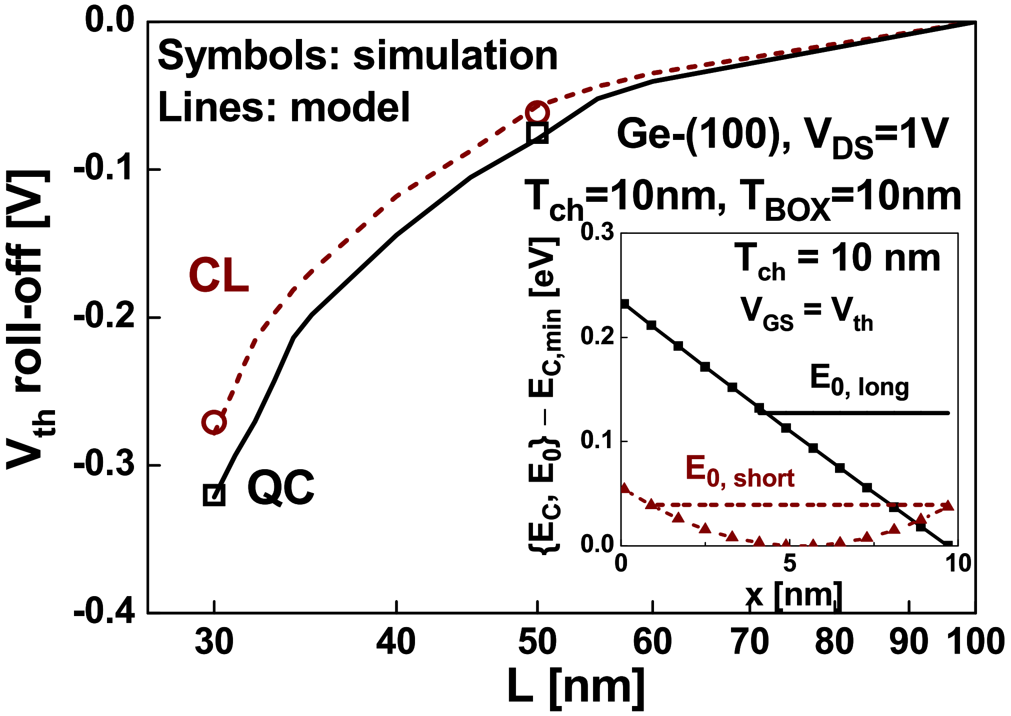

Figure 4-3 Comparison of the V_{th} roll-off between QC and CL models for T_{ch} = 10nm. The QC effect alters L_{min} (where the V_{th} roll-off = -0.2V [16]) by about +2nm. The inset indicates that for GeOI MOSFETs with larger T_{ch}, the difference in E_0 for long-channel ($E_{0,long}$) and short-channel ($E_{0,short}$) devices is significant due to electrical confinement.

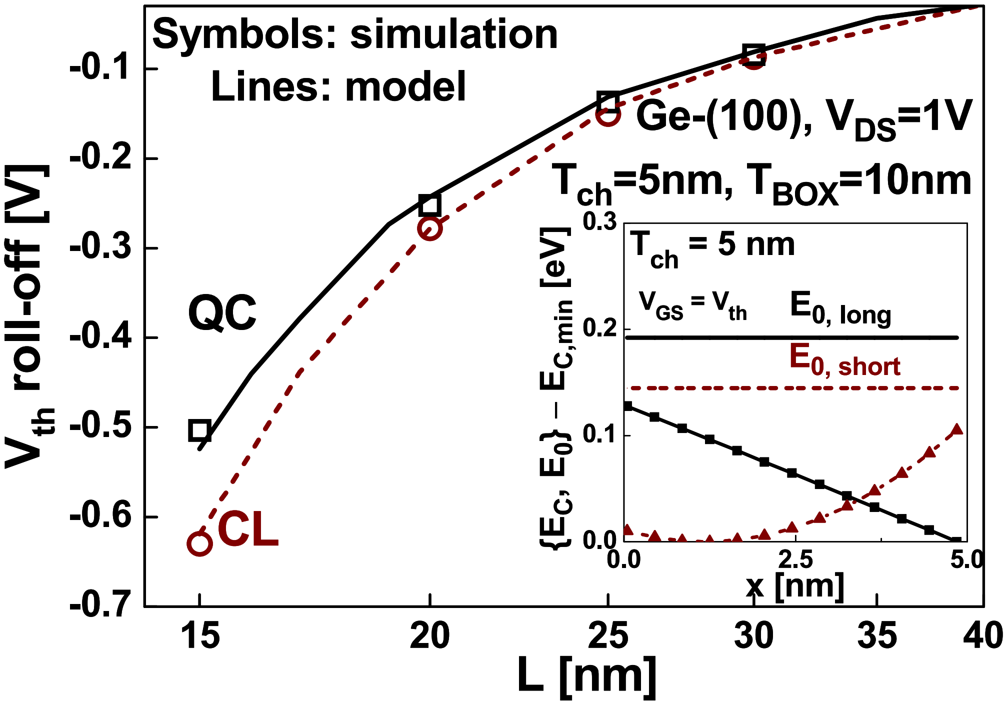

Figure 4-4 Comparison of the V_{th} roll-off between QC and CL models for T_{ch} = 5nm. The QC effect alters L_{min} by about -1nm. The inset indicates that for GeOI MOSFETs with smaller T_{ch}, the difference in E_0 for long-channel ($E_{0,long}$) and short-channel ($E_{0,short}$) devices is small because the degree of structural confinement is similar.

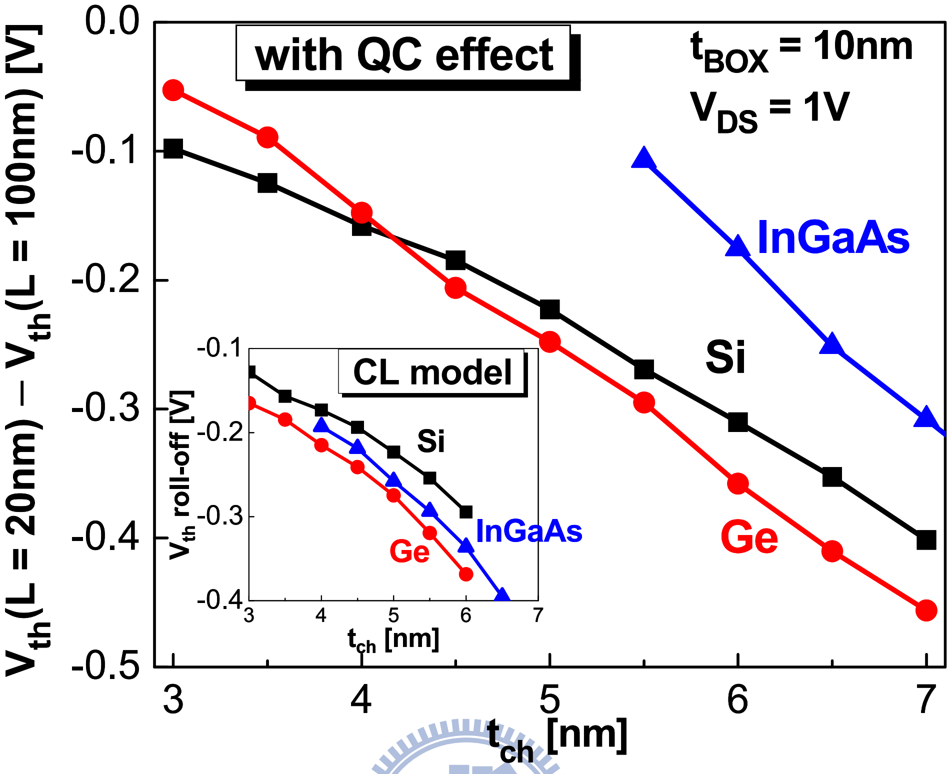

Figure 4-5 V_{th} roll-off comparison between Si, Ge, and InGaAs UTB devices considering QC effect. The inset shows the comparison result using the classical model.

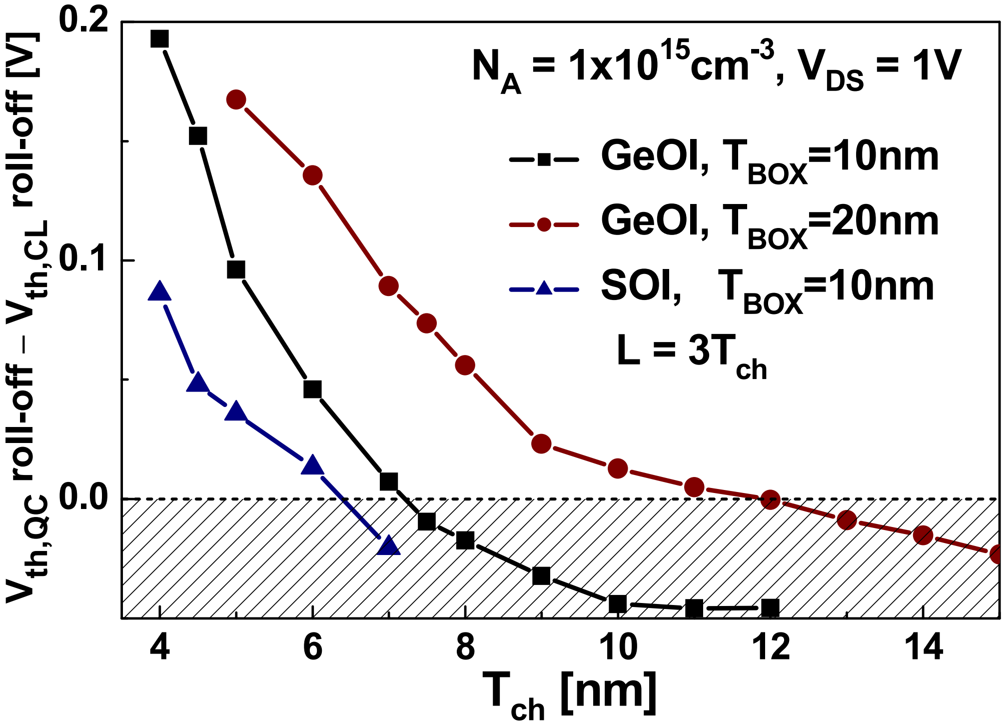

Figure 4-6 The difference in V_{th} roll-off between the QC and CL models depends on T_{BOX} and channel material. The filled region denotes that the QC effect enhances the V_{th} roll-off, while the blank region denotes that the QC effect suppresses the V_{th} roll-off.

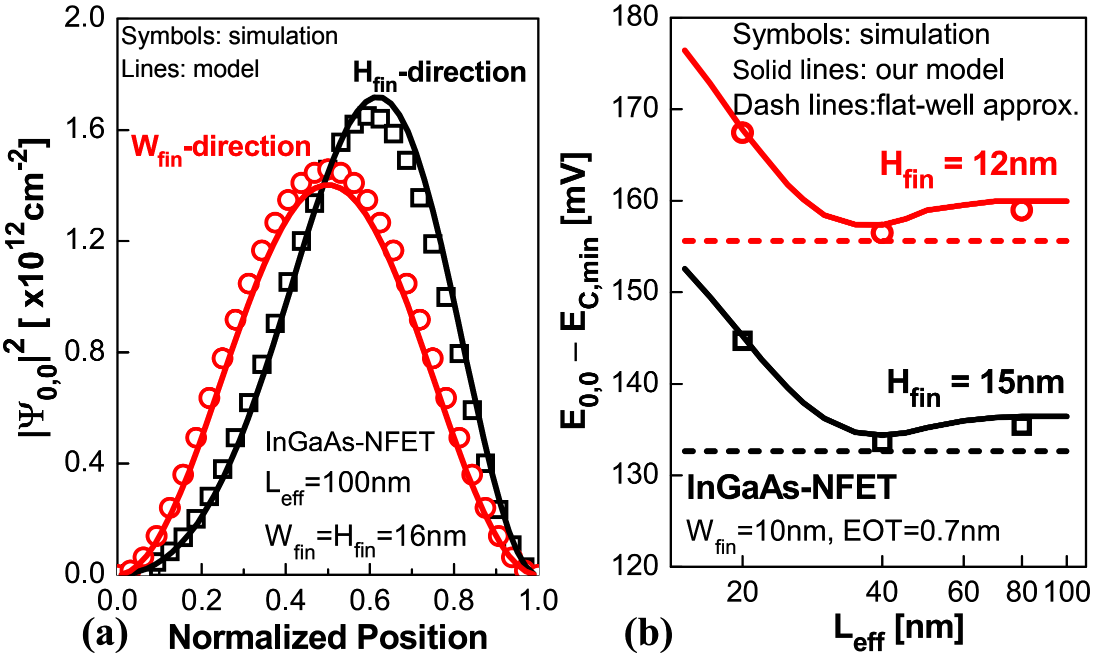

Figure 4-7 (a) Comparison of spatial distributions of $|\Psi_{0,0}|^2$ along the W_{fin} and H_{fin} directions for long-channel InGaAs multi-gate MOSFETs. (b) Channel length dependence of $E_{0,0}$ with various H_{fin} showing the accuracy of our model.

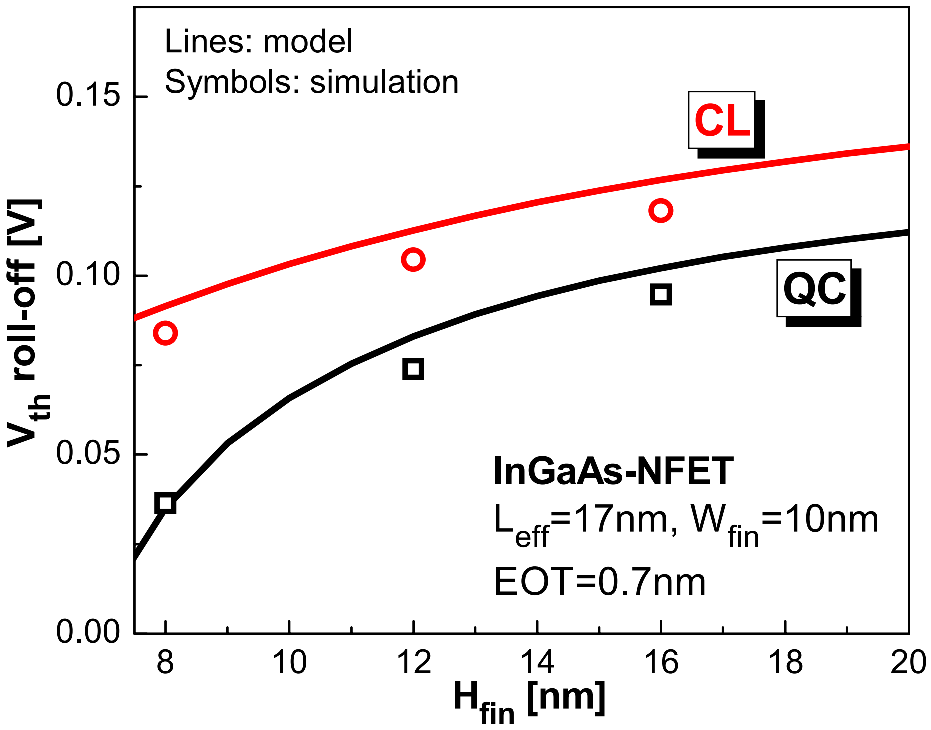

Figure 4-8 Comparison of the V_{th} roll-off vs. H_{fin} characteristic predicted by classical (CL) and quantum-confinement (QC) models for InGaAs multi-gate MOSFETs.

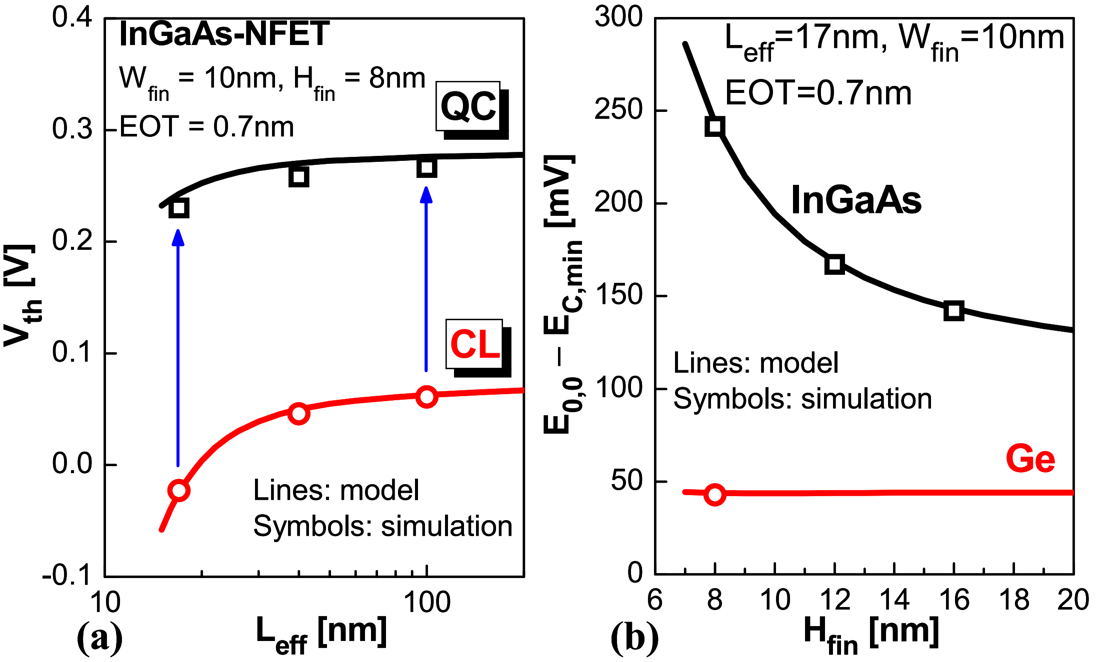

Figure 4-9 (a) Comparison of the V_{th} roll-off characteristics predicted by the CL model and the QC model for InGaAs multi-gate MOSFETs. (b) The $E_{0,0}$ of InGaAs multi-gate devices can be sensitively modulated by H_{fin} scaling. The $E_{0,0}$ of Ge multi-gate devices with (100) surface orientation are also shown.

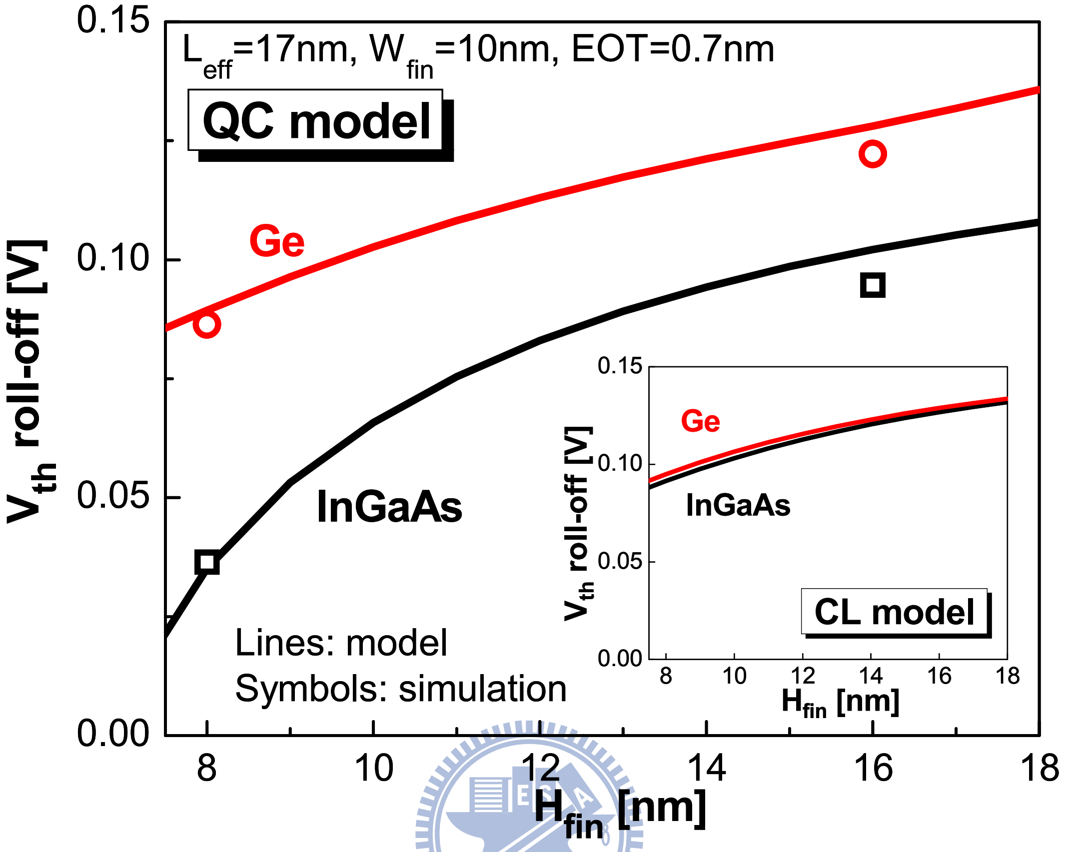

Figure 4-10 Comparison of the V_{th} roll-off vs. H_{fin} characteristic between InGaAs and Ge multi-gate MOSFETs considering the 2-D QC effect. The inset shows the comparison result by the CL model.

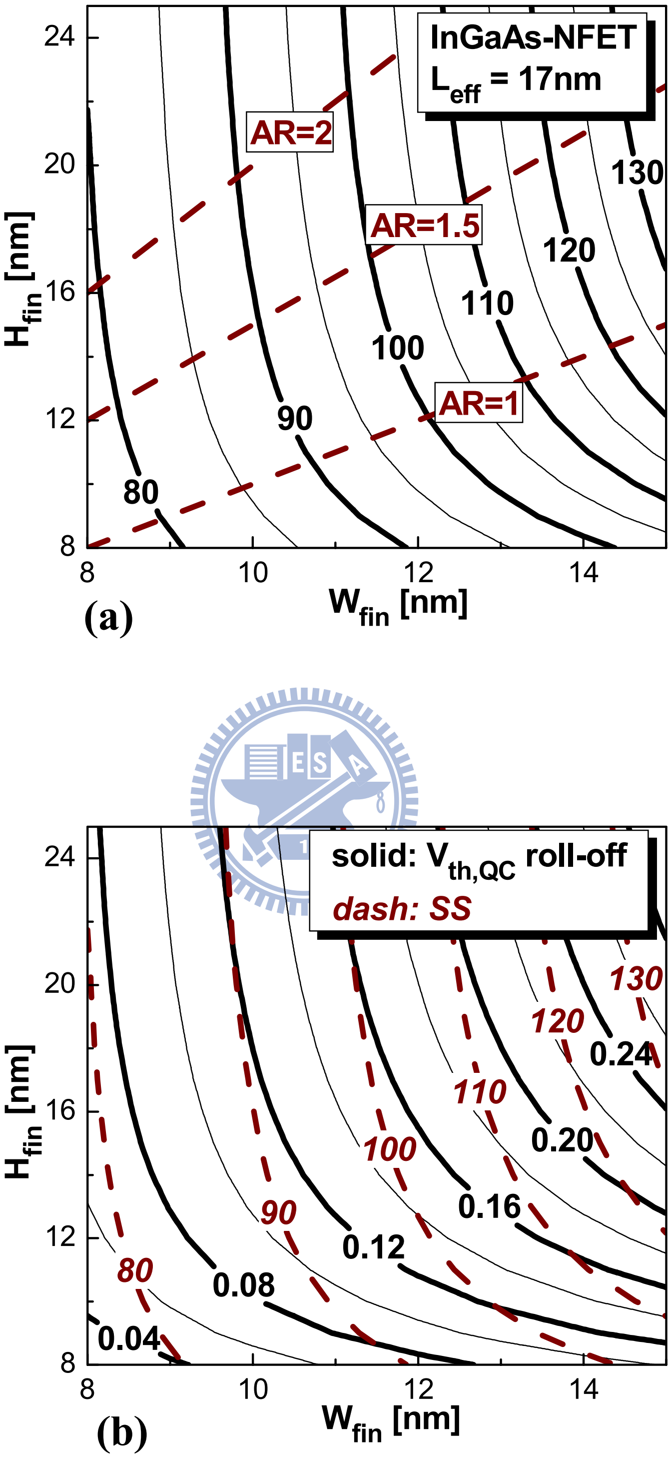

Figure 4-11 (a) Equi-SS contours, and (b) comparison of contours for $V_{th,QC}$ roll-off (solid line) and SS showing the design space of the multi-gate InGaAs NFET.

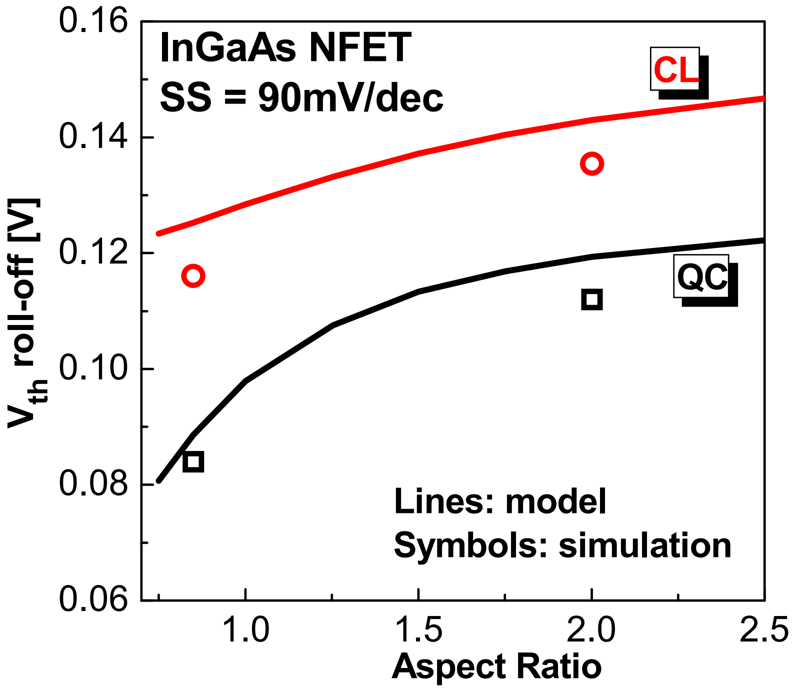

Figure 4-12 AR dependences of V_{th} roll-off for InGaAs-NFET with SS=90mV/dec.

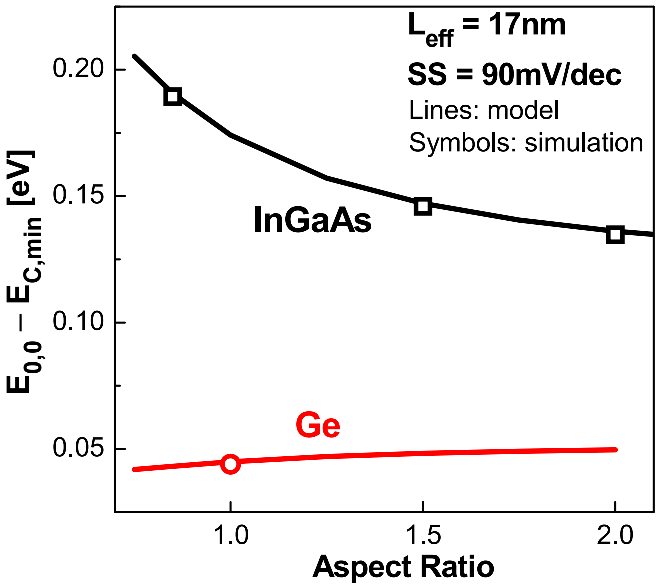

Figure 4-13 The $E_{0,0}$ of InGaAs multi-gate devices can be modulated by AR. The $E_{0,0}$ of Ge multi-gate devices with (100) surface orientation are also shown.

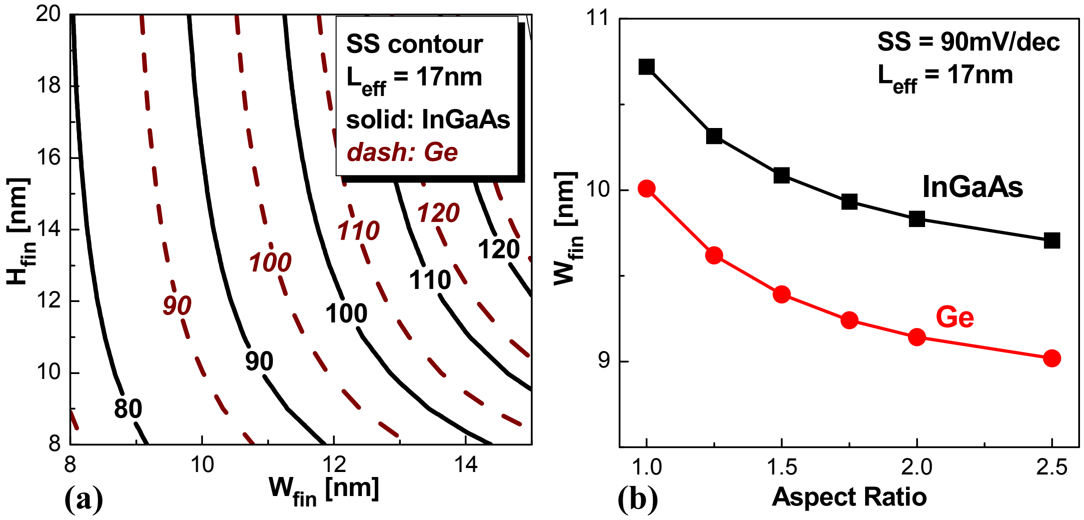

Figure 4-14 (a) Comparison of Equi-SS contours for Ge and InGaAs NFETs. (b) AR dependences of the W_{fin} needed to maintain SS=90mV/dec for Ge and InGaAs NFETs with L_{eff}=17nm.

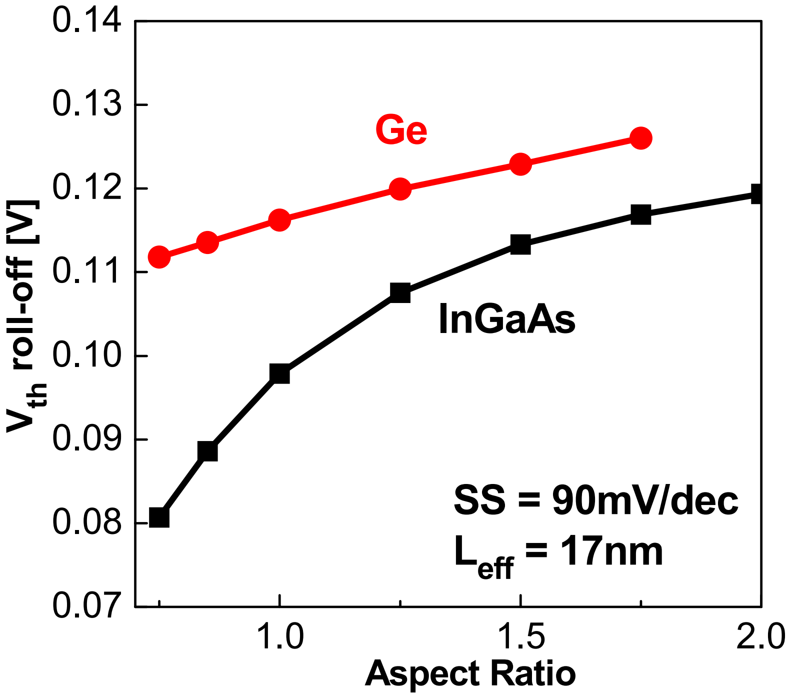

Figure 4-15 AR dependences of $V_{th,QC}$ roll-off for Ge and InGaAs NFETs with SS=90mV/dec.

Chapter 5
Modeling of Quantum Dark Space and Random Dopant Fluctuation for Advanced Ge/Si Bulk MOSFETs

5.1 Introduction

As the high-k/metal-gate stack is introduced to continue the scaling of equivalent oxide thickness (EOT), high mobility channel materials such as Ge have been proposed to compensate for the mobility loss due to the high-k gate stack [1], [2]. However, larger "dark space" [3], [4] due to quantum confinement is one major concern for Ge devices because it may significantly increase the overall electrical EOT (EOT_e) in the subthreshold region, and degrade the device electrostatic integrity. Since the quantum-confinement effect pushes the carriers away from the interface, the quantum "dark space" can be viewed as the distance from the interface to the centroid of the carrier layer (normalized with the permittivity ratio) [3]. This dark space is critical because it may significantly increase the overall electrical EOT (EOT_e) in the subthreshold region, and degrade the device electrostatic integrity.

In additional to the dark space, the small effective mass of Ge channel and the high surface electric field will result in discrete eigen-energy and increase the effective surface potential needed for threshold condition. Thus, the V_{th} will be increased because of this additional V_{th} shift due to quantum-confinement effect. As the random dopant fluctuation (RDF) becomes crucial to the V_{th} variation for heavily-doped nanoscale MOSFETs, this V_{th} shift due to quantum-confinement effect also presents a significant fluctuation, which results in an amplification of the V_{th} variation due to RDF. Therefore, a scalable model that can predict this quantum-confinement induced amplification of V_{th} variation is needed.

In this chapter, we tackle this amplification of V_{th} variation with the dark space. The modeling of this amplification requires the modeling of the dark space. First, we derive the analytical solution of the Schrödinger equation for Ge MOSFETs with high-k dielectric [4]. We further derive closed-form ground-state eigen-energy and dark space models for Ge MOSFETs with high-k dielectric. This model gives insights to the minimization of the dark space, and can be used to predict the electrostatic integrity of advanced Ge devices. Using the dark space model, a closed-form model of the amplification factor for RDF-induced V_{th} variation can be derived.

5.2 Analytical Solution of Schrödinger Equation for High-k Dielectric MOSFET

5.2.1 Eigen-Energy (E_j)

In the past, an analytical solution of Schrödinger equation in the subthreshold region had been introduced by Stern [5], who assumed an infinite oxide barrier, i.e., the carrier wavefunction goes to zero at the oxide/semiconductor interface. For high-k dielectric MOSFETs, however, the assumption is no longer valid due to smaller barrier height of the dielectric. In this section, a physically more accurate quantum confinement model by considering correct boundary conditions across the channel/dielectric interface will be presented.

An analytical solution of the Schrödinger equation in the subthreshold region can be obtained by approximating the potential well in the channel $V_{ch}(x)$ as a triangular one $V_{ch}(x) = q \cdot F_S \cdot x$ [5] with F_S the surface electric field in the channel. Under the triangular potential well, the eigen-function for the channel carrier can be expressed as

$$\Psi_{ch} = c_1 \cdot Ai\left(k_{ch} \cdot \left(x - x_{ch}\right)\right) \qquad (5\text{-}1)$$

with $k_{ch} = (2m_{ch}qF_S / \hbar^2)^{1/3}$ and $x_{ch} = E_j/(qF_S)$ [5]. E_j is the eigen-energy, $\hbar$ is the reduced Plank constant, and m_{ch} is the effective mass of the channel carrier. $Ai(x)$ is the Airy function of the first kind.

For high-k dielectric, the barrier height (ϕ_b) is relatively small and the eigen-functions are not zero at the dielectric/channel interface (x =0). Since the potential well in the dielectric is $V_{di}(x) = (\varepsilon_{ch}/\varepsilon_{di})\cdot q\cdot F_S\cdot x+\phi_b$ with ε_{ch} and ε_{di} being dielectric constants of channel and gate dielectric, respectively, the eigen-function in the gate dielectric can be expressed as

$$\Psi_{di} = c_2 \cdot Ai\left(k_{di} \cdot \left(x - x_{di}\right)\right) + c_3 \cdot Bi\left(k_{di} \cdot \left(x - x_{di}\right)\right) \qquad (5\text{-}2)$$

with $k_{di}=(2m_{di}(\varepsilon_{ch}/\varepsilon_{di})qF_S/\hbar^2)^{1/3}$, $x_{di}=(E_j-q\phi_b)/(\varepsilon_{ch}/\varepsilon_{di}\cdot qF_S)$, and m_{di} is the effective mass in the dielectric. $Bi(x)$ is the Airy function of the second kind. Using the boundary conditions that the eigen-function as well as its first derivative divided by the carrier effective mass are continuous across the channel/dielectric interface (x = 0) and the eigen-function vanishes at the dielectric boundary (x = -T_{di} with T_{di} being the dielectric thickness), the eigen-energy E_j can be determined from

$$\left[Ai\left(-k_{ch}x_{ch}\right)\cdot Bi'\left(-k_{di}x_{di}\right)-\left(m_{di}/m_{ch}\right)\left(k_{ch}/k_{di}\right)Bi\left(-k_{di}x_{di}\right)\cdot Ai'\left(-k_{ch}x_{ch}\right)\right]\cdot Ai\left(-k_{di}\left(x_{di}+T_{di}\right)\right)=0$$

(5-3)

where $Ai'(x)$ and $Bi'(x)$ are first derivatives of $Ai(x)$ and $Bi(x)$, respectively.

A steep-retrograde doping profile [7], [8] with an intrinsic region (1×10^{15} cm^{-3}) of 10nm (x_s = 10nm) near the interface and a heavily doped substrate (N_{sub}= 5×10^{18}cm^{-3}) as the ground plane (as shown in the inset of Figure 5-1) is used to verify the Equation (5-3). Since the F_S for a steep retrograde doping profile is constant, the potential well is triangular. Figure 5-1 shows that in the subthreshold region, the eigen-energies determined by Equation (5-3) are fairly accurate as compared with the numerical simulation that self-consistently solves coupled Poisson and Schrödinger equations [9]. It can be seen that the eigen-energies are reduced due to wavefunction penetration.

From Equation (5-3), E_j can be further expressed as $E_j = E_j(\phi_b = \infty) - \Delta E_j$ with $E_j(\phi_b = \infty)$ being the eigen-energy derived by Stern (i.e., $(\hbar^2/(2m_{ch}))^{1/3}(3/2\cdot\pi\cdot(j-1/4)\cdot qF_S)^{2/3}$) [5] and ΔE_j

being the eigen-energy reduction due to wavefunction penetration. ΔE_j can be approximated by the first-order Taylor expansion of Equation (5-3) around $E_j(\phi_b = \infty)$:

$$\Delta E_j \cong \frac{qF_S}{\left(\frac{2m_{di}}{\hbar^2}\right)^{1/2}\left[\left(\frac{m_{ch}}{m_{di}}-\frac{\varepsilon_{di}}{\varepsilon_{ch}}\right)\cdot\left(q\phi_b - E_j(\phi_b=\infty)\right)^{1/2}+\left(\frac{\varepsilon_{di}}{\varepsilon_{ch}}\right)\cdot\left(q\phi_b - E_j(\phi_b=\infty)-\frac{\varepsilon_{ch}}{\varepsilon_{di}}\cdot T_{di}\cdot qF_S\right)^{1/2}\right]}$$

(5-4)

Equation (5-4) indicates that the reduction of eigen-energy (i.e., ΔE_0) due to the WP effect increases with F_S, as can be seen in Figure 5-2(a). For a given F_S near the onset of threshold, Figure 5-2(b) shows that the ΔE_0 due to the WP effect increases as the dielectric barrier height ϕ_b decreases [as indicated by Equation (5-4)], and our model agrees well with the numerical simulation. It should be noted that the calculated E_0 from our model (with WP) returns to Stern's model [5] (w/o WP) as ϕ_b approaches infinity. Figure 5-3 further compares the wavefunction profiles of the first two subbands between models and exact solution. It can be seen that as the WP effect is considered, the wavefunctions in the channel shift towards the interface and our model agrees well with the numerical simulation.

5.2.2 Carrier Centroid (X_0)

The carrier centroid can be expressed as $X_0 = (\int x\cdot\Psi_0^2(x)dx)/(\int\Psi_0^2(x)dx)$ with $\Psi_0(x)$ being the ground-state wavefunction [5]. X_0 is equal to $2E_0/(3qF_S)$ if the wavefunction vanishes at the interface [i.e, $\Psi_0(x=0) = 0$] [5]. However, for high-k dielectric devices with significant WP, a more general expression of X_0 is required. As the X_0 (and hence dark space) increases the overall EOT$_e$ and hence degrades the subthreshold swing (SS), an analytical expression for dark space can be derived from the SS. The SS is defined as $(d\log_{10}(Q_i)/dV_G)^{-1}$ with Q_i being the sheet carrier density $\int n(x)dx$, in which the electron density $n(x)$ can be determined by the eigen-energies and eigenfunctions

$$n(x)=\frac{kT}{\pi\hbar^2}\cdot\sum_{v,j}g_v\cdot m_d^v\cdot\left|\Psi_{v,j}(x)\right|^2\cdot\ln\left[1+\exp\left(-\frac{E_{C,surf}+E_{v,j}-E_F}{kT}\right)\right] \qquad (5\text{-}5)$$

where g_v is the valley degeneracy, m_d^v is the density-of-state effective mass of valley v. $E_{C,surf}$, $E_{v,j}$, and E_F are conduction band edge at the surface, j^{th} eigen-energy, and Fermi level, respectively. Figure 5-4 shows that the electron density considering WP is higher than that without WP because of the E_j reduction. The electron penetration into the dielectric region can be clearly seen using the E_j derived from Equation (5-3). In addition, it can be seen that the dark space can be reduced by the WP effect.

When the E_F is sufficiently smaller than $E_{C,surf}+E_{v,j}$ (e.g., in the subthreshold region), the Q_i is proportional to $\exp(-q(E_{C,surf}+E_{v,j}-E_F)/kT)$. Therefore, the SS can be expressed as

$$SS=\left(\frac{kT}{q}\right)\cdot\ln(10)\cdot Q_i\cdot$$
$$\left\{\frac{kT}{\pi\hbar^2}\cdot\sum_{v,j}g_v\cdot m_d^v\cdot\exp\left(-\frac{E_{C,surf}+E_{v,j}-E_F}{kT}\right)\cdot\left[1-\frac{dF_S}{dV_G}\cdot\left(\frac{\varepsilon_{ch}}{\varepsilon_{di}}\cdot T_{di}+\frac{d\left(E_{v,j}/q\right)}{dF_S}\right)\right]\right\}^{-1} \qquad (5\text{-}6)$$

Using the ground-state approximation (i.e., most carriers populate at the ground state),

$$SS\cong\left(\frac{kT}{q}\right)\cdot\ln(10)\cdot\left[1-\frac{dF_S}{dV_G}\cdot\left(\frac{\varepsilon_{ch}}{\varepsilon_{di}}\cdot T_{di}+\frac{d\left(E_0/q\right)}{dF_S}\right)\right]^{-1}$$
$$=\left(\frac{kT}{q}\right)\cdot\ln(10)\cdot\left[1-\left(\frac{\varepsilon_{ch}\cdot\left(dF_S/dV_G\right)}{\varepsilon_{di}/\left[T_{di}+\left(\varepsilon_{di}/\varepsilon_{ch}\right)\cdot d\left(E_0/q\right)/dF_S\right]}\right)\right]^{-1} \qquad (5\text{-}7)$$
$$=\left(\frac{kT}{q}\right)\cdot\ln(10)\cdot\left[1-\left(\frac{C_{total}}{C_{di,QC}}\right)\right]^{-1}=\left(\frac{kT}{q}\right)\cdot\ln(10)\cdot\left[1+\left(\frac{C_{dep}}{C_{di,QC}}\right)\right]$$

The $C_{di,QC}$ is the equivalent dielectric capacitance considering the quantum-confinement effect. Since the total charge is $\varepsilon_{ch}\cdot F_S$ by Gauss's law, the $C_{total}=\varepsilon_{ch}\cdot(dF_S/dV_G)$ is the total capacitance and is equal to $C_{di,QC}\cdot C_{dep}/(C_{di,QC}+C_{dep})$ with C_{dep} being the depletion capacitance. It can be seen that the equivalent increment of dielectric thickness due to quantum-confinement effect is $(\varepsilon_{di}/\varepsilon_{ch})\cdot[d(E_0/q)/dF_S]$, and hence the carrier centroid (X_0) due to the quantum-confinement effect can be expressed as

$$X_0 = \frac{d(E_0/q)}{dF_S} \qquad (5\text{-}8)$$

Figure 5-5 shows that, without considering WP, the $d(E_0/q)/dF_S$ expression returns to $2E_0/(3qF_S)$ because $E_0(\phi_b = \infty)$ can be approximated as $(\hbar^2/(2m_{ch}))^{1/3}(9/8\cdot\pi\cdot qF_S)^{2/3}$ [5]. When the WP effect is considered, however, the X_0 calculated by $d(E_0/q)/dF_S$ is significantly smaller than that calculated by $2E_0/(3qF_S)$. It should be noted that while E_0 can be used to assess the degree of quantum-confinement induced V_{th} shift, the E_0 sensitivity to F_S [i.e., $d(E_0/q)/dF_S$] can be used to assess the SS and therefore the device electrostatic integrity.

5.3 Closed-Form Models of Dark Space, Subthreshold Swing, and V_{th} Shift Due to Quantum-Confinement Effect

As the ground-state eigen-energy (E_0) and hence the dark space (DS) can be determined from the non-linear equation [Equation (5-3)], closed-form modeling of E_0 and DS for uniformly-doped channel will be employed in this section. Then, closed-form models of subthreshold swing and V_{th} shift due to quantum-confinement can be derived [6].

5.3.1 Dark Space & V_{th} Shift Due to Quantum-Confinement Effect

With the triangular well and infinite oxide barrier approximations, a carrier layer thickness model [$=2E_0/(3qF_S)$] for Si channel had been proposed in the past [5]. However, for Ge-channel devices with high-k gate dielectric, these approximations may result in significant error in the prediction of the dark space and eigen-energy because of the small effective mass of the channel carrier and the finite dielectric barrier height. Although the impact of finite barrier height on Si devices had been considered by empirically fitting the ground-state eigen-energy dependence on the surface electric field with numerical simulation recently [11]

[12], the fitting results were not scalable and not applicable for Ge devices.

To derive the E_0 and DS models for Ge channel with small quantization effective mass m_{ch}, a more accurate E_0-F_S relationship than the one used in [5] needs to be employed. First, for a uniformly-doped channel with doping concentration N_{ch} (negative for p-type substrate), a parabolic channel potential well $V_{ch}(x) = q\cdot[F_S\cdot x + (qN_{ch}/2\varepsilon_{ch})\cdot x^2]$ has to be used in the derivation of the ground-state eigen-energy E_0. Using the perturbation theory [13] and treating the $q\cdot(qN_{ch}/2\varepsilon_{ch})\cdot x^2$ term as a perturbation to the triangular well $V_{ch,tri}(x) = q\cdot F_S\cdot x$, E_0 can be expressed as $E_{0,tri} + q\cdot(qN_{ch}/2\varepsilon_{ch})\cdot\int x^2\cdot\Psi^2_{0,tri}(x)dx$ with $E_{0,tri}$ and $\Psi_{0,tri}(x)$ being the ground-state eigen-energy and wavefunction of the triangular well $V_{ch,tri}(x)$, respectively. It can be further shown that:

$$E_0 = E_{0,tri} + (4/15)\cdot(N_{ch}/\varepsilon_{ch})\cdot(E_{0,tri}/F_S)^2. \qquad (5\text{-}9)$$

To derive an accurate $E_{0,tri}$ for Ge devices with high-k dielectric, the wavefunction penetration effect needs to be considered. Equation (5-1) indicates that the wavefunction (and hence the carrier distribution) will be shifted toward the interface by $x_{ch}(\phi_b{=}\infty) - x_{ch}(\phi_b)$ $[=\Delta E_{0,tri}/(qF_S)]$, which is responsible for the X_0 reduction $X_0(\phi_b{=}\infty) - X_0(\phi_b)$ $[=d(\Delta E_{0,tri}/q)/dF_S]$. Hence, $d\Delta E_{0,tri}/dF_S \cong \Delta E_{0,tri}/F_S$. In other words, $\Delta E_{0,tri} \cong \alpha\cdot F_S$ with α being a coefficient independent of F_S.

The coefficient α can be determined by Equation (5-4). When the F_S of Equation (5-4) approaches zero, we can derive the dependences of $\Delta E_{0,tri}$ on m_{ch}, m_{di}, and ϕ_b, and then the α can be obtained as

$$\alpha = q\cdot\frac{\hbar}{\sqrt{2}}\cdot\left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}}\cdot\frac{1}{m_{ch}}\right). \qquad (5\text{-}10)$$

Therefore, $E_{0,tri}$ can be expressed as

$$E_{0,tri} = \left(\frac{\hbar^2}{2m_{ch}}\right)^{1/3} \cdot \left(\frac{9}{8}\pi \cdot qF_S\right)^{2/3} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}}\right) \cdot F_S \qquad (5\text{-}11)$$

Substituting Equation (5-11) into Equation (5-9), we can obtain a closed-form model for E_0:

$$\begin{aligned} E_0 = {} & \left(\frac{\hbar^2}{2m_{ch}}\right)^{1/3} \cdot \left(\frac{9}{8}\pi \cdot qF_S\right)^{2/3} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}}\right) \cdot F_S \\ & + \frac{4}{15} \cdot \frac{N_{ch}}{\varepsilon_{ch}} \cdot \left[\left(\frac{\hbar^2}{2m_{ch}F_S}\right)^{1/3} \cdot \left(\frac{9}{8}\pi \cdot q\right)^{2/3} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}}\right)\right]^2 \end{aligned} \qquad (5\text{-}12)$$

It can be seen from Equation (5-12) that E_0 is not exactly proportional to $(F_S)^{\lambda}$ [10]. This explains why in [11] λ has to be treated as a fitting parameter as the relation $E_0 \propto (F_S)^{\lambda}$ was used. In addition, although the λ had been empirically derived by introducing several fitting parameters to consider the ϕ_b and N_{ch} dependences [12], the m_{ch} and m_{di} dependences were not considered. Therefore, the fitting parameters used in [12] cannot be employed for devices with different channel and dielectric materials.

As $X_0 = d(\Delta E_0/q)/dF_S$, we can obtain a closed-form model for carrier centroid X_0:

$$\begin{aligned} X_0 = {} & \left[\frac{2}{3}\left(\frac{\hbar^2}{2m_{ch}qF_S}\right)^{1/3} \cdot \left(\frac{9}{8}\pi\right)^{2/3} - \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}}\right)\right] \cdot \\ & \left\{1 + \frac{8}{15}\frac{N_{ch}}{\varepsilon_{ch}}\left[\left(\frac{\hbar^2}{2m_{ch}F_S{}^4}\right)^{1/3} \cdot \left(\frac{9}{8}\pi \cdot q\right)^{2/3} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}}\right) \cdot \frac{1}{F_S}\right]\right\} \\ & - \frac{8}{15}\frac{N_{ch}}{\varepsilon_{ch}}\frac{1}{qF_S{}^3} \cdot \left[\left(\frac{\hbar^2}{2m_{ch}}\right)^{1/3} \cdot \left(\frac{9}{8}\pi \cdot qF_S\right)^{2/3} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}}\right) \cdot F_S\right]^2 \end{aligned} \qquad (5\text{-}13)$$

After normalized with the permittivity ratio, the dark space DS can be determined by $X_0/(\varepsilon_{ch}/\varepsilon_{ox})$. Figure 5-6 summarizes the derivation procedures of the closed-form model for dark space.

As the quantum-confinement effect increases the effective surface potential needed for threshold condition, this quantum-confinement induced surface potential shift ($\Delta\varphi_S{}^{QC}$) [14] is

$$\Delta\varphi_S^{\mathrm{QC}} = E_0/q - (kT/q)\cdot\ln(g_v\cdot q m_d F_S/(\pi\hbar^2 N_C)) \qquad (5\text{-}14)$$

where N_C is the effective density of state for the conduction band. With $\Delta\varphi_S^{\mathrm{QC}}$, the QC-induced $\mathrm{V_{th}}$ shift ($\Delta\mathrm{V_{th}}^{\mathrm{QC}}$) can then be derived by $m\cdot\Delta\varphi_S^{\mathrm{QC}}$ with $m = 1 + (\varepsilon_{ch}/\varepsilon_{ox})\cdot(\mathrm{EOT+DS})/W_{dep}$ with W_{dep} being the maximum depletion width. With Equations (5-12), (5-13), and (5-14), closed-form models for $\Delta\varphi_S^{\mathrm{QC}}$ and $\Delta\mathrm{V_{th}}^{\mathrm{QC}}$ can be derived.

5.3.2 Verification with TCAD Simulation

To verify our closed-form models, we have performed the TCAD simulation that numerically solves the self-consistent solution of coupled Poisson and Schrödinger equations [9]. For a given F_S near the onset of threshold, Figure 5-7 shows that the E_0 for Ge-(100) and Si-(100) devices decrease with the barrier height ϕ_b because of the wavefunction penetration (WP) effect, and our model agrees well with the TCAD simulation. In addition, the E_0 reduction for Ge-(100) is more significant than Si-(100) because Ge-(100) possesses smaller m_{ch} and hence larger α [Equation (5-10)]. Figure 5-8 shows that for Ge-(100) device with high-k dielectric and uniformly-doped profile, the E_0 is reduced after considering the WP effect and the parabolic well. Moreover, our model shows accurate F_S dependence of E_0, which is crucial to the DS modeling. Figure 5-9(a) indicates that when the WP effect is not considered, the X_0 of Ge-(100) is significantly larger than that of Si-(100). When the WP effect is considered, however, the discrepancy of X_0 for Ge-(100) and Si-(100) is substantially reduced because of the more significant reduction of X_0 for Ge-(100). After normalized with the permittivity ratio, Figure 5-9(b) shows that the discrepancy of DS for Ge-(100) and Si-(100) will be further reduced because of the higher permittivity for Ge channel. The discrepancy of DS becomes smaller than 1Å for the F_S near the onset of threshold. Figure 5-10 shows that the DS depends on the surface orientation because of the different quantization effective mass m_{ch}. Since the DS increases with decreasing m_{ch}, the DS of

Ge-(100) surface is larger than the Ge-(110) and (111) counterparts. This is contrary to the Si devices that the DS of (100)-surface is smaller than the (110) and (111) counterparts. Figure 5-11(a) shows that the E_0 increases with decreasing m_{ch}, and the E_0 of Ge-(100) surface is larger than the Ge-(110) and (111) counterparts. This is contrary to the Si devices that the E_0 of (100)-surface is smaller than the (110) and (111) counterparts. Since the g_v and m_d also contribute to the $\Delta \mathrm{V_{th}}^{\mathrm{QC}}$ [Equation (5-14)], Figure 5-11(b) shows that Ge-(100) and (110) devices exhibit similar $\Delta \mathrm{V_{th}}^{\mathrm{QC}}$. For Si devices, the $\Delta \mathrm{V_{th}}^{\mathrm{QC}}$ of (110) and (111) are similar. The DS and $\Delta \varphi_S{}^{\mathrm{QC}}$ also depend on the material of gate dielectric because the properties of gate dielectric such as ϕ_b and m_{di} will determine the degree of the WP effect. Figure 5-12 shows that among the three high-k dielectrics, HfO_2 possesses smaller DS and $\Delta \varphi_S{}^{\mathrm{QC}}$ than Al_2O_3 and La_2O_3.

Since the F_S is related to the N_{ch} and can be modulated by the substrate bias (V_{sub}), the DS and $\Delta \mathrm{V_{th}}^{\mathrm{QC}}$ also depends on N_{ch} and V_{sub}. As the F_S near the onset of threshold is $[2qN_{ch}\cdot(2\varphi_B - V_{sub})/\varepsilon_{ch}]^{1/2}$ ($\varphi_B = (kT/q)\cdot\ln(N_{ch}/n_i)$ with n_i the intrinsic carrier concentration), the F_S increases with N_{ch} and reverse V_{sub}. Figure 5-13(a) shows that the DS near the onset of threshold decreases with increasing N_{ch} because the DS decreases with increasing F_S (Figure 5-9). On the contrary, Figure 5-13(b) shows that the $\Delta \mathrm{V_{th}}^{\mathrm{QC}}$ increases with the N_{ch} of uniformly-doped profile because the E_0 increases with F_S. In addition, the $\Delta \mathrm{V_{th}}^{\mathrm{QC}}$ increases with EOT because the m factor increases with EOT. Figure 5-14(a) indicates that applying the reverse V_{sub} will reduce the DS because of the larger F_S. In addition, it can be seen that the Ge-(100) surface exhibits higher DS sensitivity to V_{sub} than the Ge-(110) and (111) counterparts. On the contrary, Figure 5-14(b) indicates that applying the reverse V_{sub} will increase the $\Delta \mathrm{V_{th}}^{\mathrm{QC}}$ because of the larger F_S. In addition, the Ge-(100) and (110) surface exhibit larger $\Delta \mathrm{V_{th}}^{\mathrm{QC}}$ sensitivity to V_{sub} than the Ge-(111) counterpart.

In additional to the uniform doping profile, our model is also applicable for devices with a steep retrograde doping profile [4]. For the steep retrograde doping profile with an intrinsic region near the interface (inset of Figure 5-1), the F_S is constant and the potential well is triangular. Therefore, the $E_{0,tri}$ in Equation (5-11) can be applied to the ground-state eigen-energy for the steep retrograde profile. The $X_{0,tri}$ can be derived by $d(E_{0,tri}/q)/dF_S$:

$$X_{0,tri}=\left[\frac{2}{3}\left(\frac{\hbar^2}{2m_{ch}}\right)^{1/3}\cdot\left(\frac{9}{8}\pi\cdot q\right)^{2/3}\cdot F_S{}^{-1/3}-q\cdot\frac{\hbar}{\sqrt{2}}\cdot\left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}}\cdot\frac{1}{m_{ch}}\right)\right] \qquad (5\text{-}15)$$

The DS for the steep retrograde profile can be determined by $X_{0,tri}/\ (\varepsilon_{ch}/\varepsilon_{ox})$. Figure 5-15(a) shows that for a given heavily-doped substrate doping (N_{sub}=5×10^{18}cm^{-3}), the DS decreases with the intrinsic region depth x_s. This is because the F_S near the onset of threshold increases with decreasing x_s. Thus, Figure 5-15(b) shows that for devices with steep retrograde doping profile, the $\Delta V_{th}{}^{QC}$ increases with the intrinsic region depth x_s. As the uniformly-doped channel is similar to the steep retrograde profile with $x_s = 0$, it can be seen from Figure 5-15(a) that the DS of the uniformly-doped profile is smaller than that of the steep retrograde profile. On the contrary, it can also be seen from Figure 5-15(b) that the $\Delta V_{th}{}^{QC}$ of the uniformly-doped profile is larger than that of the steep retrograde profile.

5.3.3 Subthreshold Swing

With the closed-form DS model, we can assess the SS of Ge devices with high-k dielectric by incorporating EOT$_e$ = EOT + DS in the SS model [2], [3], [17]. In this paper, we use the reported analytical SS model for short-channel bulk devices [17]:

$$SS=\frac{kT}{q}\ln(10)\cdot\left(1-\frac{EOT_e}{\varepsilon_{ox}}\cdot\left(-\frac{qN_{ch}\Delta W_{dep}}{\phi_f}+\frac{2\varepsilon_{ch}X_j}{L_{eff}{}^2}\cdot\frac{\Delta\nu}{\phi_f}\right)\right) \qquad (5\text{-}16)$$

where L_{eff} and X_j are the effective channel length and junction depth of source/drain, respectively. The definitions of ΔW_{dep}, $\Delta\nu$, and ϕ_f can be referred to [17]. Figure 5-16(a) shows that for long-channel Ge NFETs, the calculated SS of Ge-(100) is larger than the Ge-(110) and

(111) counterparts, as predicted by the DS in Figure 5-10. Moreover, the reduction in SS for Ge-(100) due to the WP effect is more significant than the Si-(100) counterpart. Figure 5-16(b) further shows that this reduction in SS for Ge devices due to the WP effect increases for short-channel devices.

For Ge bulk MOSFETs, only L-valley is considered in our calculation. The relative importance of other conduction band bottoms such as Γ-valley and X-valley will be discussed in the Appendix 2.

5.4 Quantum-Confinement Induced Amplification of V_{th} Variation

Random V_{th} variation is a serious problem for nanoscale MOSFETs. Whether the introduction of Ge channel will fundamentally impact the V_{th} variation is an important question. Due to random dopant fluctuation (RDF), the ground-state eigen-energy of Ge devices presents a significant fluctuation, which results in an amplification of the V_{th} variation. In this section, we present a closed-form model for the quantum-confinement induced amplification factor (AF_{QC}) in the standard variation of V_{th} (σV_{th}). In addition, we propose that a scalable quantum-mechanical σV_{th} model can be obtained through the classical Takeuchi model [18], [19] multiplied by AF_{QC}.

5.4.1 Modeling of the Amplification Factor (AF_{QC})

In addition to the conduction band edge (E_C) fluctuation (i.e., surface potential fluctuation), the RDF also results in significant ground-state eigen-energy fluctuations. Figure 5-17 shows that the spatial fluctuation of ground-state eigen-energy due to RDF is larger than that of E_C. While the classical-V_{th} ($V_{th,CL}$) variation due to RDF results from the E_C variation, the larger ground-state eigen-energy fluctuation will cause more serious $V_{th,QC}$ variation. Figure 5-18 shows that the dispersion of $V_{th,QC}$ is closely correlated to the dispersion of $V_{th,CL}$.

Therefore, the standard derivation of $V_{th,QC}$ ($\sigma V_{th,QC}$) can be modeled as the product of $\sigma V_{th,CL}$ and the slope $dV_{th,QC}/dV_{th,CL}$. The slope $dV_{th,QC}/dV_{th,CL}$ can be viewed as an amplification factor (AF_{QC}) due to quantum confinement. Therefore, modeling the AF_{QC} is crucial to the prediction of $V_{th,QC}$ variation for Ge MOSFETs.

As the $V_{th,QC}$ is $V_{th,CL}$ plus the QC-induced V_{th} shift ΔV_{th}^{QC}, the $AF_{QC}(=dV_{th,QC}/dV_{th,CL})$ for RDF can be expressed as

$$AF_{QC} = 1 + \frac{d\Delta V_{th}^{QC}}{dF_S} \cdot \frac{dF_S}{dN_{ch}} \cdot \left(\frac{dV_{th,CL}}{dN_{ch}} \right)^{-1} \qquad (5\text{-}17)$$

Since Figure 5-13(b) has qualitatively demonstrated the impact of RDF on $V_{th,QC}$, we can further demonstrate the ΔV_{th}^{QC} dependence on $V_{th,CL}$ from Figure 5-13(b), as shown in Figure 5-19. It can be seen that the ΔV_{th}^{QC} shows linear dependence on $V_{th,CL}$, and the slope $d\Delta V_{th}^{QC}/dV_{th,CL}$ is ($AF_{QC} - 1$). In addition, Figure 5-19 indicates that the AF_{QC} depends on the EOT. Using derived E_0, dark space, and ΔV_{th}^{QC} models in Section 5-3, our closed-form model for AF_{QC} [model (1)] can be expressed as the products of the following three equations:

$$\left. \frac{d\left(\Delta V_{th}^{QC}\right)}{dF_S} \right|_{V_{th,CL}} = m \cdot \left(\frac{d\left(E_0/q\right)}{dF_S} - \frac{kT}{qF_S} \right)$$
$$= \left(1 + \frac{\left(\varepsilon_{ch}/\varepsilon_{ox}\right) \cdot \left(EOT + DS\right)}{W_{dep}} \right) \cdot \left(DS - \frac{kT}{\left(\varepsilon_{ch}/\varepsilon_{ox}\right) \cdot qF_S} \right) \cdot \left(\frac{\varepsilon_{ch}}{\varepsilon_{ox}} \right) \qquad (5\text{-}18a)$$

$$\left. \frac{dF_S}{dN_{ch}} \right|_{V_{th,CL}} = \left(\varphi_B + \frac{V_{sub}}{2} + \frac{kT}{q} \right) \cdot \sqrt{\frac{q}{\varepsilon_{ch} \cdot N_{ch} \cdot \left(\varphi_B + V_{sub}/2\right)}} \qquad (5\text{-}18b)$$

$$\frac{dV_{th,CL}}{dN_{ch}} = \frac{kT}{q} \cdot \frac{1}{N_{ch}} + \frac{EOT}{\varepsilon_{ox}} \cdot \left(\varphi_B + \frac{V_{sub}}{2} + \frac{kT}{q} \right) \cdot \sqrt{\frac{q\varepsilon_{ch}}{N_{ch}\left(\varphi_B + V_{sub}/2\right)}} \qquad (5\text{-}18c)$$

where $F_S|_{V_{th,CL}} = (q \cdot N_{ch} \cdot W_{dep}/\varepsilon_{ch})$ and $\varphi_B = (kT/q) \cdot \ln(N_{ch}/n_i)$.

In this study, we also compare the model (1) with a different AF_{QC} model based on the Takeuchi model [18], [19], in which the $\sigma V_{th} = B_{VT} \cdot [T_{inv} \cdot (V_{th} + V_0)/(W \cdot L)]^{1/2}$ with T_{inv} being the electrical EOT, $V_0 = -(V_{fb}+2\varphi_B)$, and B_{VT} being a constant. Since the AF_{QC} can be determined by the ratio $\sigma V_{th,QC}/\sigma V_{th,CL}$ (for $\sigma V_{th,CL}$, T_{inv}=EOT and $V_{th}=V_{th,CL}$; for $\sigma V_{th,QC}$, T_{inv}=EOT+DS and $V_{th}=V_{th,QC}$), the AF_{QC} from Takeuchi model is [model (2)]:

$$AF_{QC} = \left(\frac{EOT+DS}{EOT}\right)^{1/2} \cdot \left(\frac{V_{th,QC}+V_0}{V_{th,CL}+V_0}\right)^{1/2} \qquad (5\text{-}19)$$

5.4.2 Amplification of V_{th} Variation for Ge MOSFET with High-k Dielectric

Figure 5-20 shows that with EOT downscaling, both the AF_{QC} and the AF_{QC} sensitivity to EOT increase. In addition, as model (1) shows consistent AF_{QC} with the TCAD simulation, model (2) overestimates the AF_{QC}, and the discrepancy increases with EOT downscaling. Therefore, model (1) is a more scalable AF_{QC} model. Figure 5-21 indicates that the AF_{QC} decreases with increasing temperature, and model (1) shows higher sensitivity to temperature, which is consistent with TCAD simulation. Since the dark space (and hence AF_{QC}) depends on the dielectric material (Figure 5-12), Figure 5-22 shows that for a given EOT, the AF_{QC} for HfO_2 is smaller because of the smaller dark space. Figure 5-23 shows that the AF_{QC} decreases with reverse substrate bias V_{sub}, which is consistent with the V_{sub} dependence of dark space (Figure 5-14).

Figure 5-24 demonstrates that, after multiplied by the AF_{QC}, the $\sigma V_{th,QC}$ due to RDF can be predicted based on the $\sigma V_{th,CL}$. The $\sigma V_{th,CL}$ can be derived either from the atomistic simulation [20], [22] or the analytical model [18], [19]. For example, based on the $A_{VT,CL}$ (the slope of $\sigma V_{th,CL}$ for various device geometry in the Pelgrom plot [23]) derived from the atomistic simulation, we can calculate the $A_{VT,QC}$ by ($AF_{QC} \cdot A_{VT,CL}$). Figure 5-25 shows that the $\sigma V_{th,QC}$ predicted by the AF_{QC} is consistent with the atomistic simulations that solves the time-consuming exact Schrödinger equation. Therefore, the AF_{QC} approach can significantly reduce the computational time for atomistic simulations.

More importantly, a scalable $\sigma V_{th,QC}$ model can be obtained using our closed-form AF_{QC} combined with the classical Takeuchi model (T_{inv}=EOT and $V_{th}=V_{th,CL}$):

$$\sigma V_{th,QC} = AF_{QC} \cdot B_{VT} \cdot \sqrt{\frac{EOT \cdot \left(V_{th,CL} + V_0\right)}{WL}} \qquad (5\text{-}20)$$

As the $\sigma V_{th,CL}$ depends on EOT with the power equal to 1, Figure 5-26 shows that the power dependence of $\sigma V_{th,QC}$ on EOT decreases because of the impact of AF_{QC}. Moreover, the $\sigma V_{th,QC}$ predicted by model (2) exhibits a much less sensitivity to EOT scaling because it overestimates the AF_{QC} (Figure 5-20). In addition, Figure 5-27(a)-(c) comprehensively compares the sensitivity of the model-predicted $\sigma V_{th,QC}$ and $\sigma V_{th,CL}$ due to RDF for Ge MOSFETs. Contrary to the classical model, Figure 5-28(a) and (b) show that our model can predict the discrepancy of σV_{th} for various surface orientations and gate dielectric materials, respectively.

Since the dopant position fluctuation is not considered in the classical Takeuchi model [18], only the dopant number fluctuation is included in Equation (5-20). For heavily-doped bulk MOSFETs, the dopant number fluctuation may dominate the overall RDF because the amount of dopants in the channel is quite high (e.g., ~80 dopants in a volume = $(25\text{nm})^3$ channel with $N_{ch} = 5\times10^{18}\text{cm}^{-3}$).

5.5 Summary

In this chapter, we have provided closed-form models of “dark space” and ground-state eigen-energy for Ge MOSFETs with high-k gate dielectric. These models show accurate dependences on barrier height, surface electric field, and quantization effective mass of channel and gate dielectric. Our models predict that as the dark space decreases with reverse substrate bias and increasing channel doping, the quantum-confinement induced V_{th} shift shows the opposite dependences with substrate bias and channel doping. Our model can also be used for devices with the steep retrograde doping profile. This physically accurate dark space model will be crucial to the prediction of the subthreshold swing and quantum-confinement induced V_{th} shift of advanced Ge devices.

Using the closed-form dark space model, we have provided a closed-form model for the quantum-confinement induced amplification factor (AF_{QC}) in σV_{th} due to random dopant fluctuation. Therefore, a scalable quantum-mechanical σV_{th} model can be obtained through the classical model multiplied by AF_{QC}. Using our model, various factors (e.g., EOT, temperature, etc.) that may modulate/reduce the impact of RDF on Ge MOSFETs can be accurately assessed.

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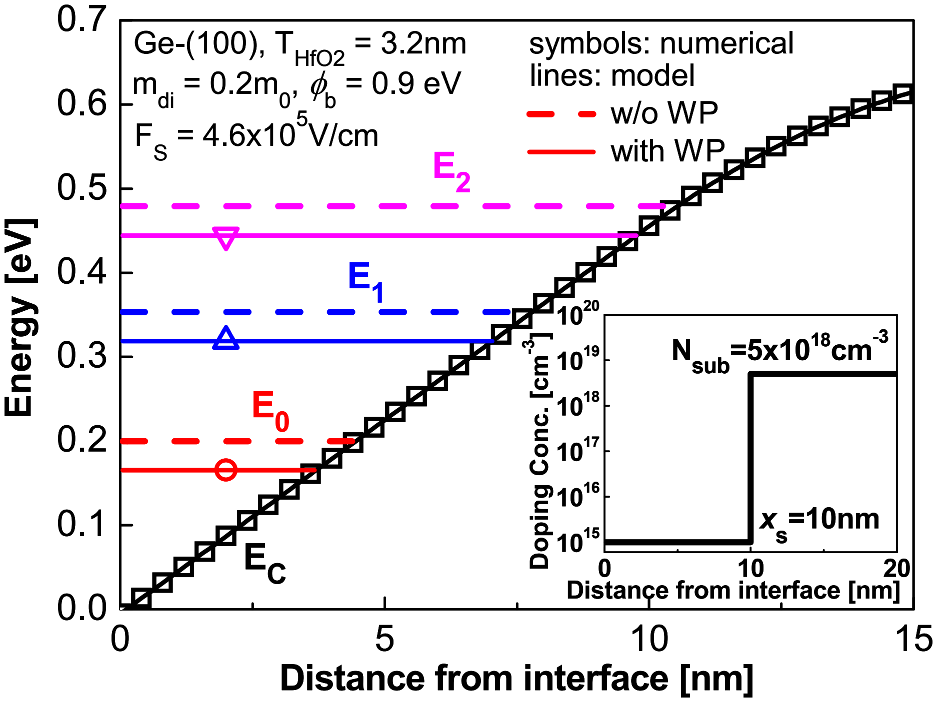

Figure 5-1 E_C and the first three subband eigen-energies for Ge-(100) NFET with steep retrograde doping profile. The eigen-energies with and without considering the WP effect are compared with the numerical simulation. (Inset) The steep retrograde doping profile used in this study.

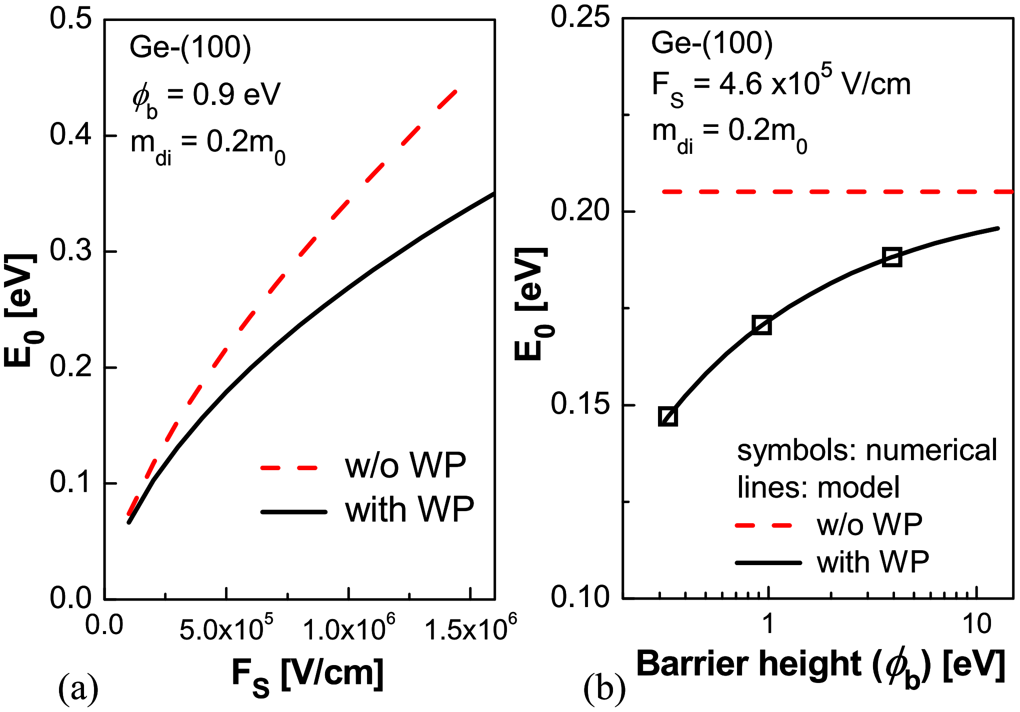

Figure 5-2 (a) Comparison of surface electric field dependences of E_0 of Ge-(100) surface calculated with and without WP. (b) Comparison of barrier height dependences of E_0 of Ge-(100) surface calculated with and without WP.

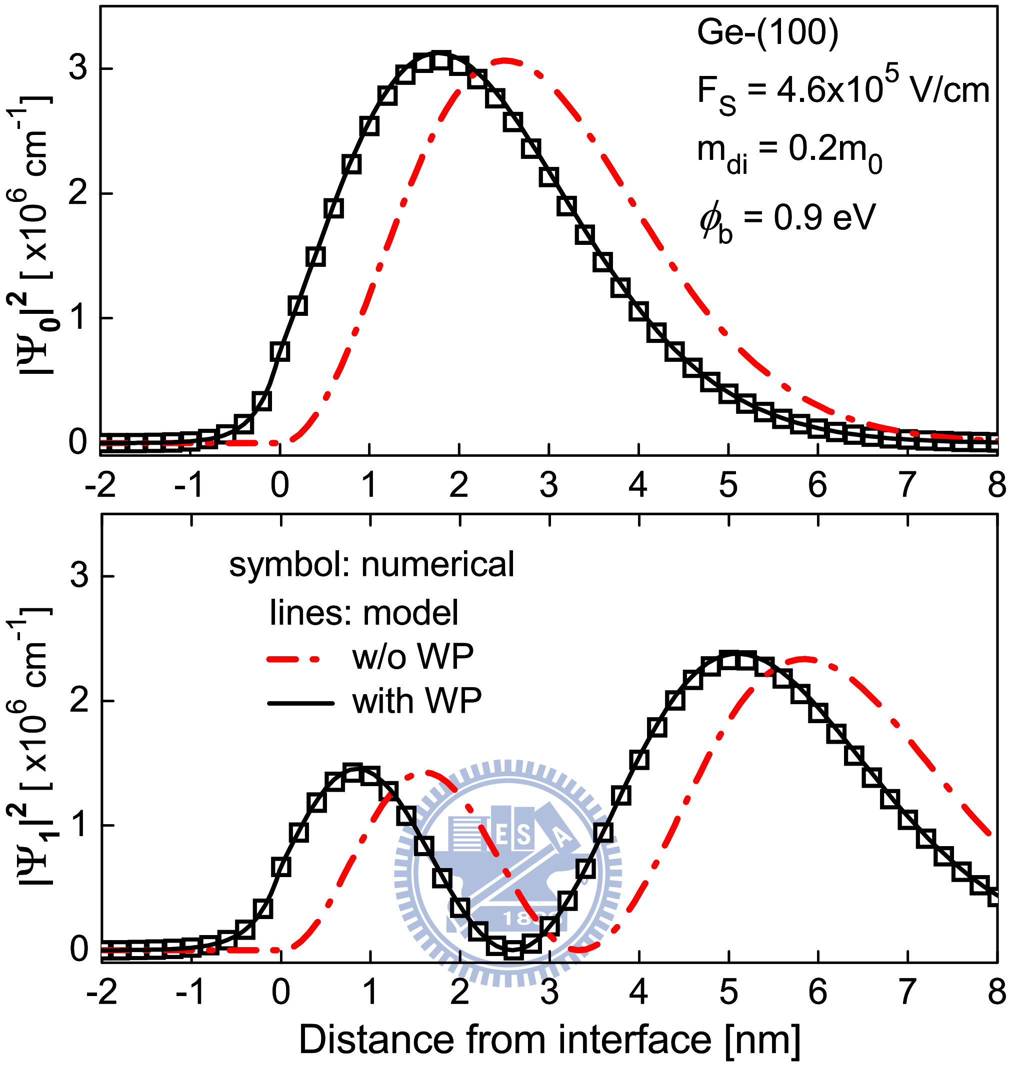

Figure 5-3 Wavefunction spread of the first two subbands for Ge-(100) surface calculated with and without WP verified with numerical simulations.

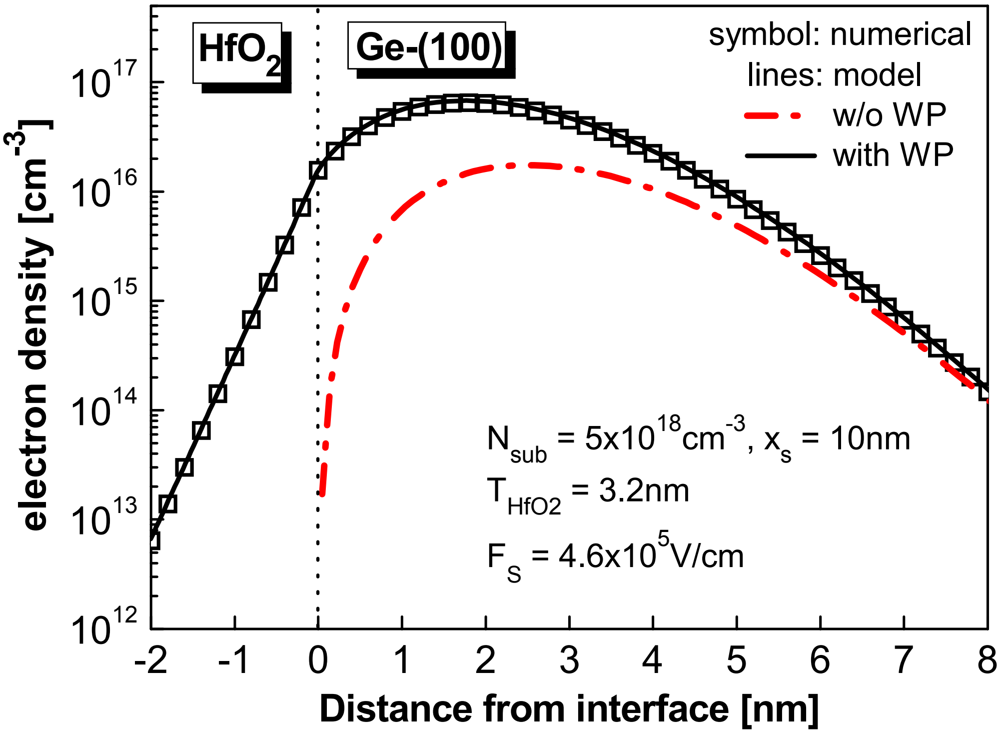

Figure 5-4 Comparison of electron density profiles calculated from models with and without WP. The ϕ_b and m_{di} used for HfO_2 in this study are 0.9eV and $0.2m_0$ [15], respectively.

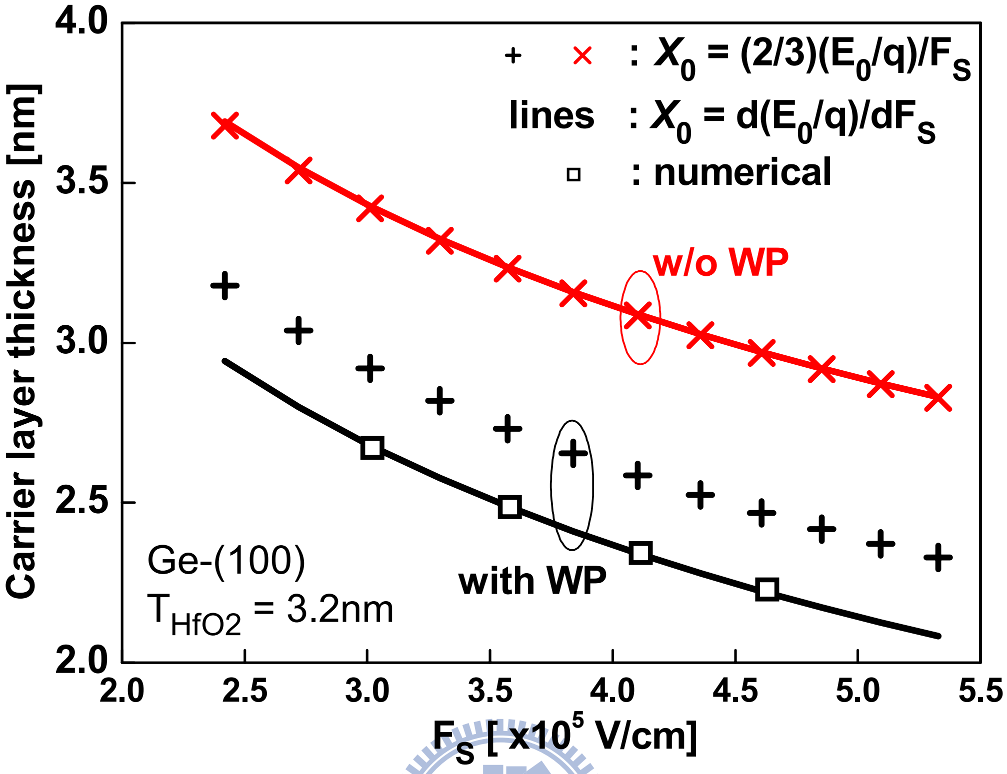

Figure 5-5 Comparison of the two expressions of carrier layer thickness (X_0) due to the QC effect. The X_0 from numerical simulation is calculated by $\int x \cdot \Psi_0^2(x)dx)/(\int \Psi_0^2(x)dx$.

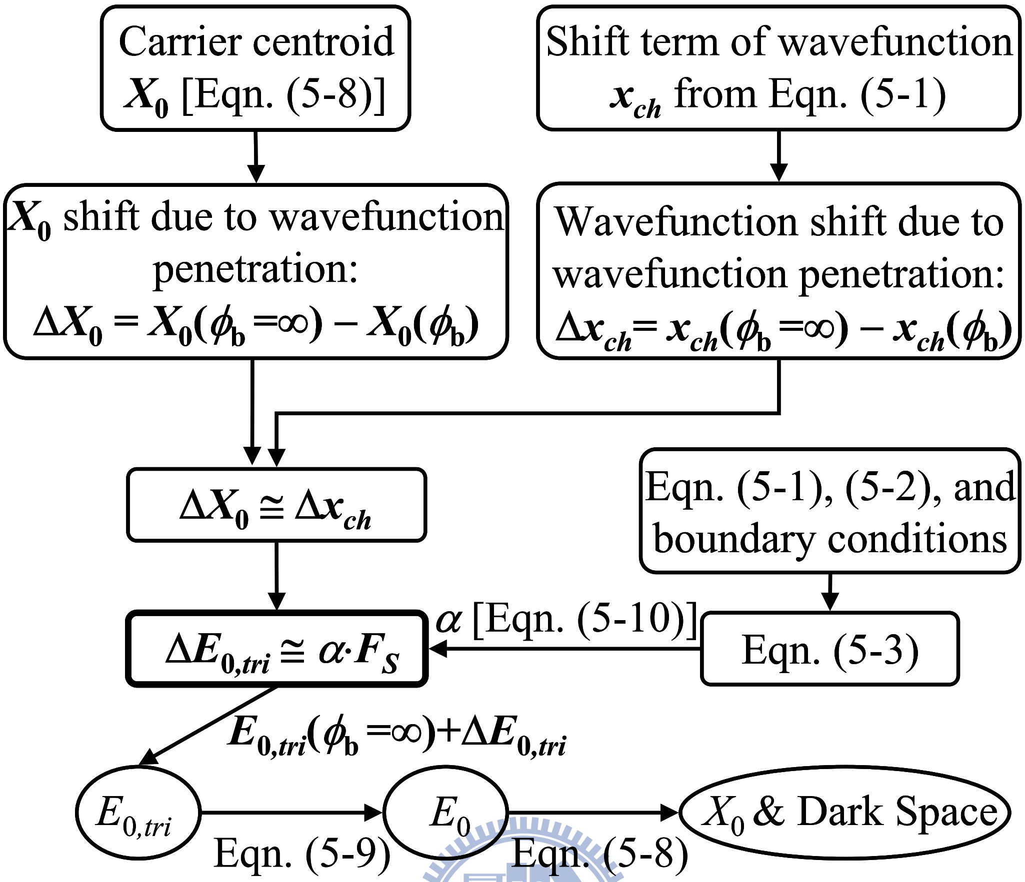

Figure 5-6 Flowchart demonstrating the derivation of the closed-form model for dark space considering the parabolic well and the wavefunction penetration effect.

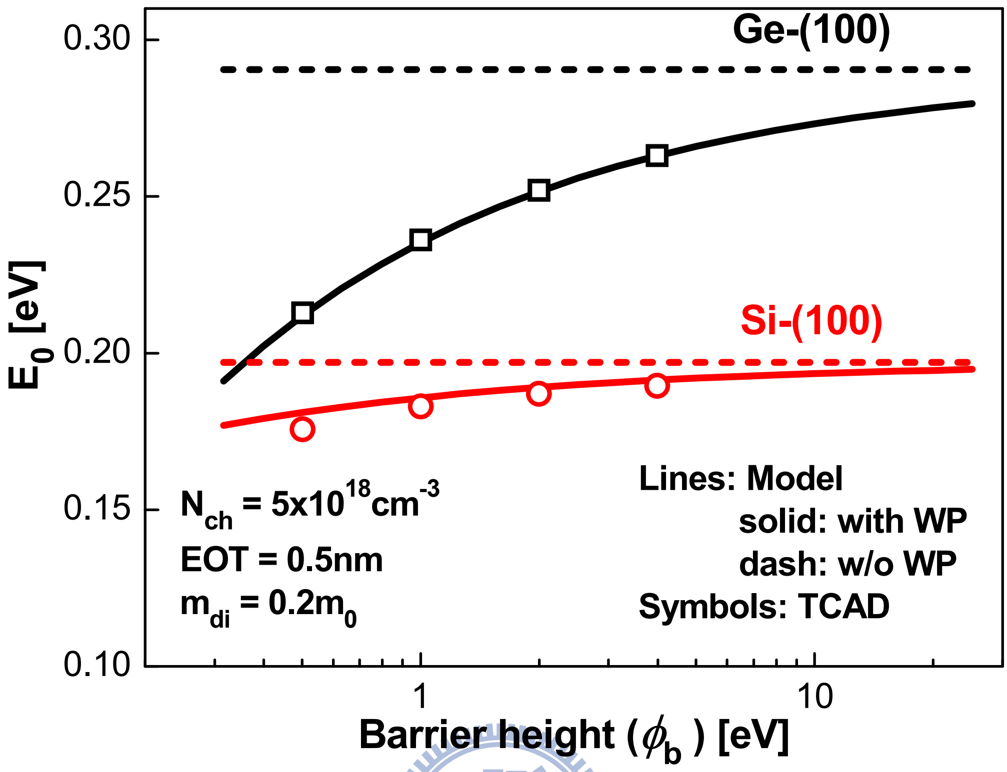

Figure 5-7 Barrier height dependences of E_0 for Si-(100) and Ge-(100) surfaces with and without considering the wavefunction penetration (WP) effect.

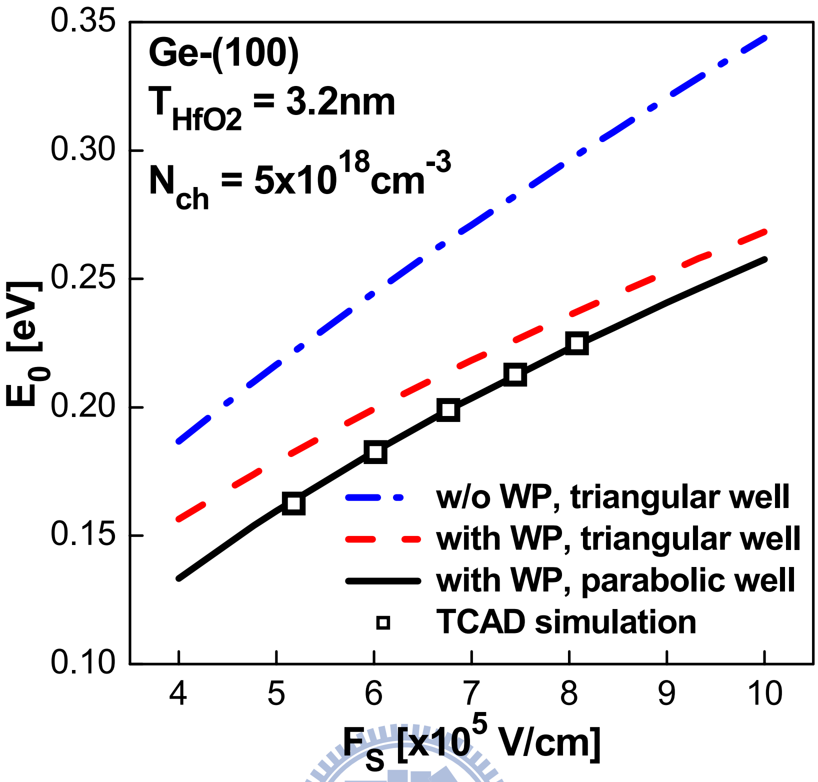

Figure 5-8 E_0 dependence on surface electric field for Ge-(100) device with high-k dielectric. It can be seen that the wavefunction penetration (WP) and parabolic well reduce the E_0.

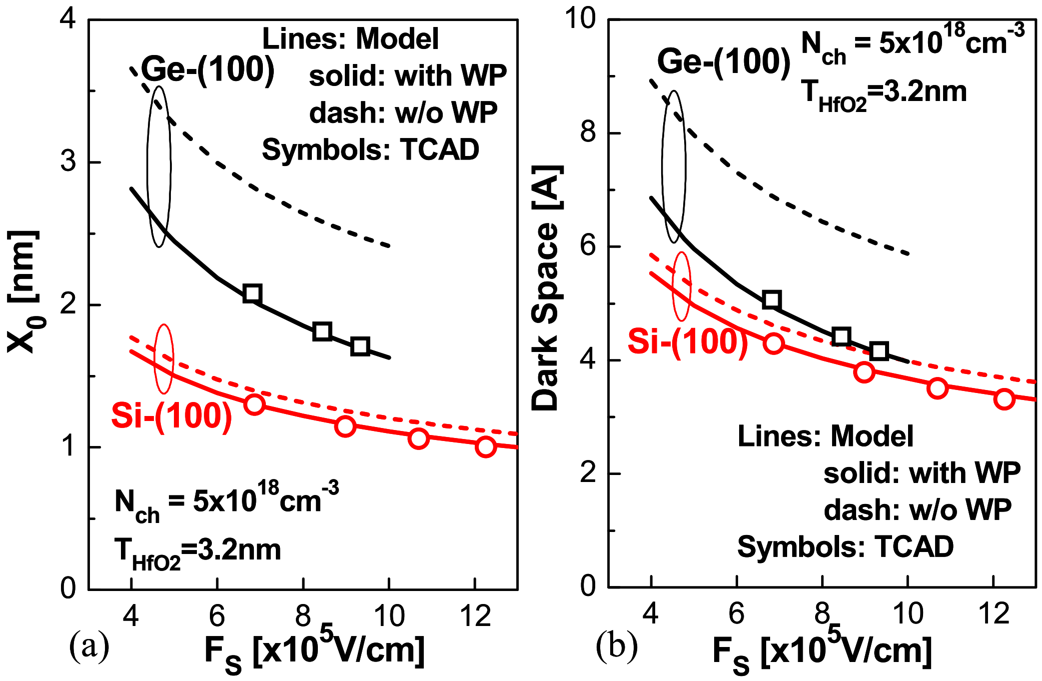

Figure 5-9 (a) Comparison of X_0 for Si-(100) and Ge-(100) surfaces with and without considering the WP effect. The ϕ_b and m_{di} used for HfO$_2$ are 0.9eV and 0.2m_0 [15], respectively. (b) The DS is directly derived by the results from (a) divided by (ε_{ch} / ε_{ox}).

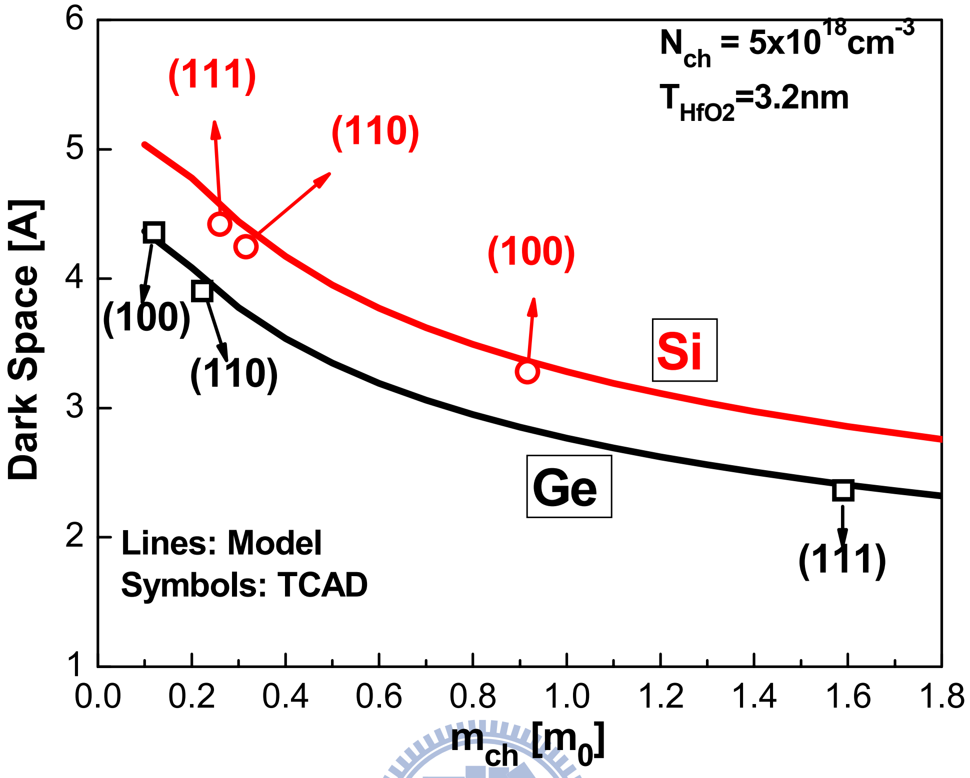

Figure 5-10 Impact of channel quantization effective mass and surface orientation on the DS of Si and Ge devices. The curve for Ge is below that of Si because of the higher $(\varepsilon_{ch} / \varepsilon_{ox})$ ratio for Ge. For Ge NFET, the m_{ch} for (100), (110), and (111) surfaces are $0.12m_0$, $0.223m_0$, and $1.59m_0$, respectively [16]. For Si NFET, the m_{ch} for (100), (110), and (111) surfaces are $0.916m_0$, $0.316m_0$, and $0.26m_0$, respectively [16].

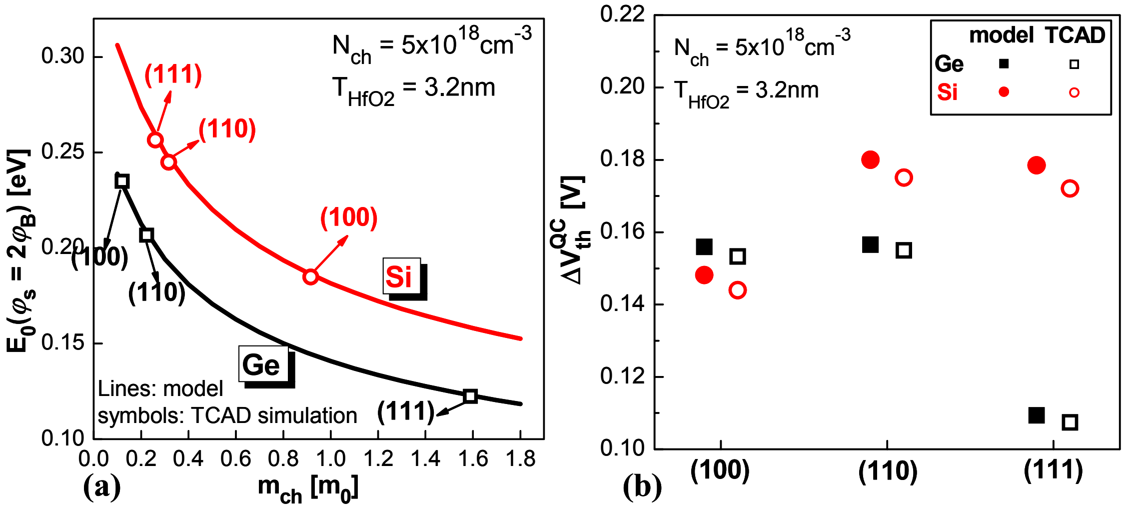

Figure 5-11 (a) Impact of channel quantization effective mass and surface orientation on the E_0 at the onset of threshold for Si and Ge devices. The curve for Ge is below that of Si because of the larger permittivity and hence smaller F_S at onset of threshold for Ge. (b) Comparison of ΔV_{th}^{QC} for Si and Ge devices with various surface orientations.

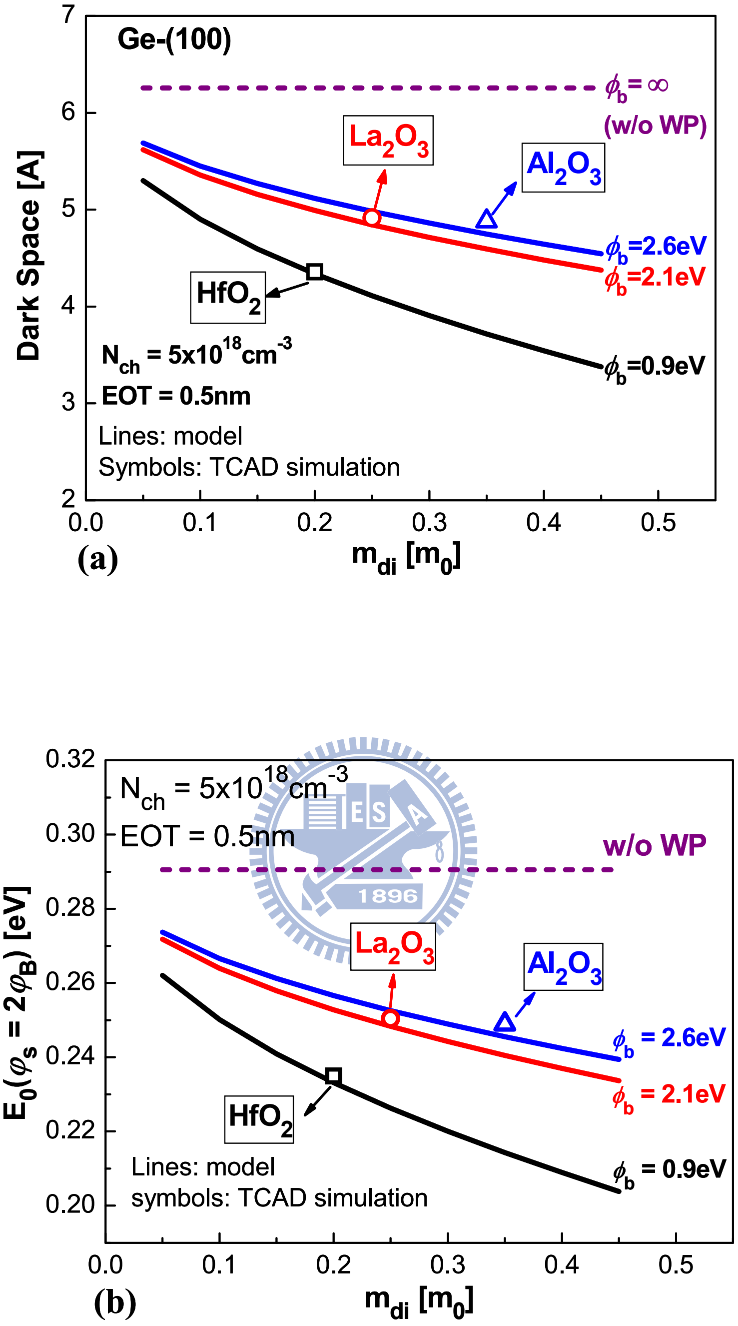

Figure 5-12 Impact of gate-dielectric material on the (a) DS and (b) E_0 of the Ge-(100) device. The ϕ_b used for La$_2$O$_3$ and Al$_2$O$_3$ are 2.1eV and 2.6eV, respectively. The m_{di} used for La$_2$O$_3$ and Al$_2$O$_3$ are 0.25m_0 and 0.35m_0, respectively [15].

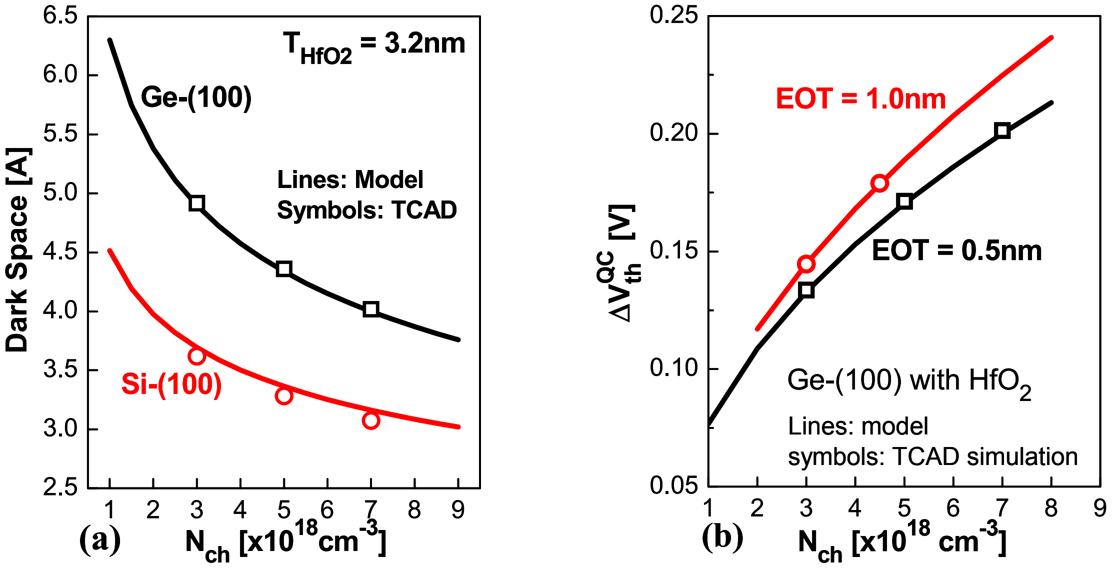

Figure 5-13 (a) Channel doping dependences of DS for Si-(100) and Ge-(100) surfaces. (b) Channel doping dependence of ΔV_{th}^{QC} for uniformly-doped Ge-(100) device with EOT = 0.5nm and 1nm.

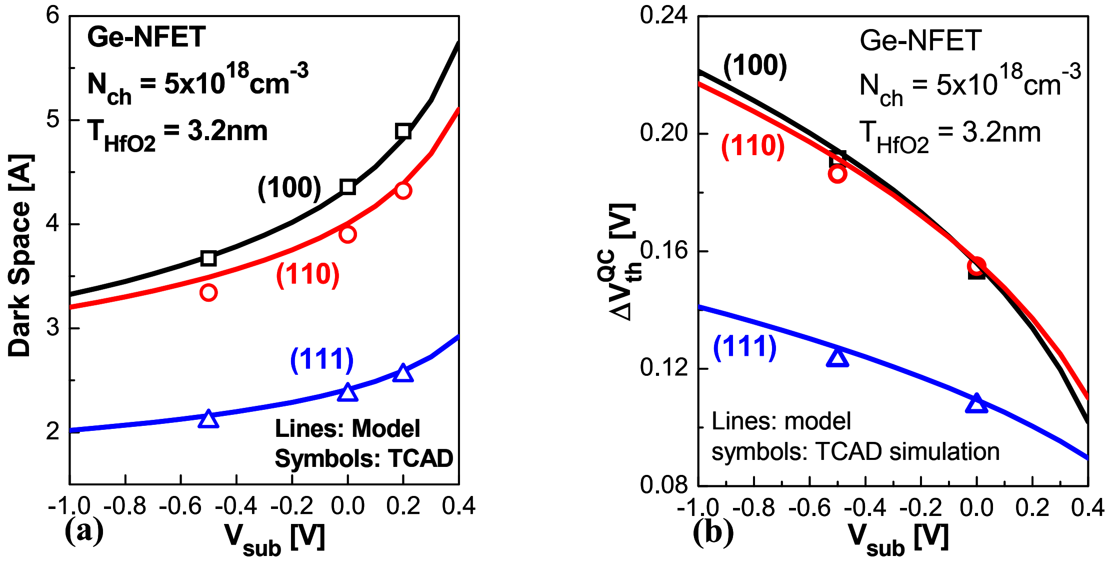

Figure 5-14 Substrate bias dependences of (a) DS and (b) ΔV_{th}^{QC} for Ge NFET with various surface orientations.

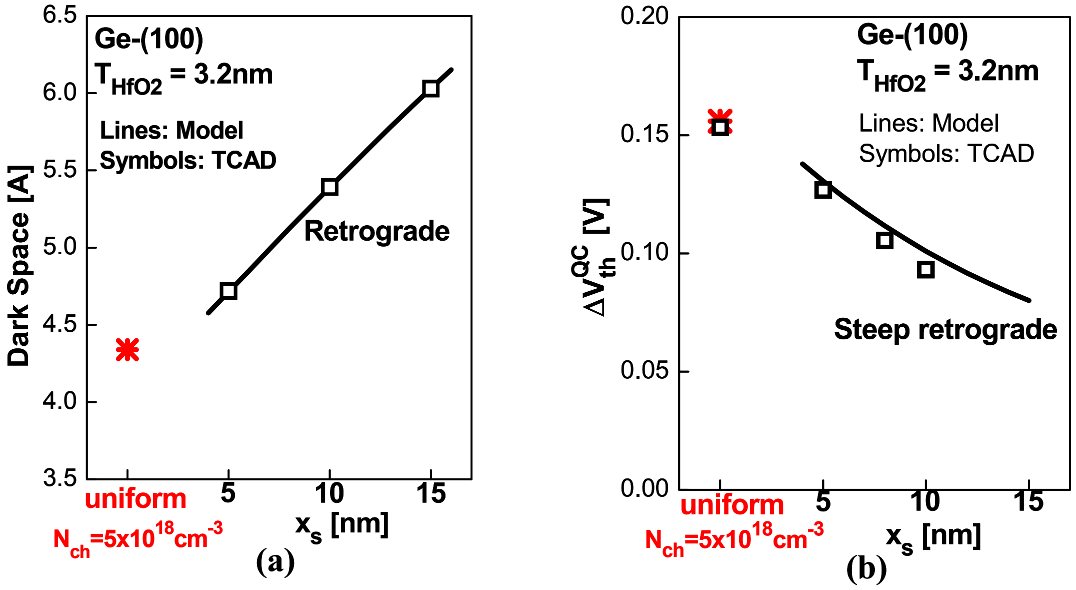

Figure 5-15 Comparison of (a) DS and (b) ΔV_{th}^{QC} for the steep retrograde doping profile with various intrinsic region depth x_s and the uniform doping profile.

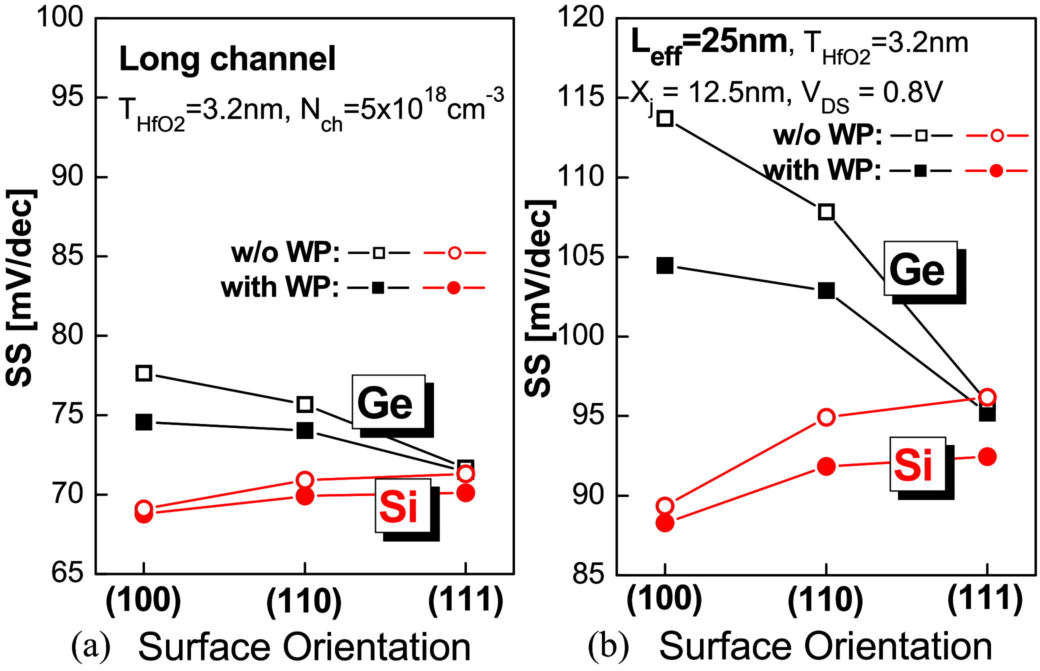

Figure 5-16 (a) Comparison of the long-channel SS for Ge-NFET and Si-NFET with various orientations. (b) Comparison of the short-channel (L_{eff}=25nm) SS for Ge-NFET and Si-NFET with various orientations.

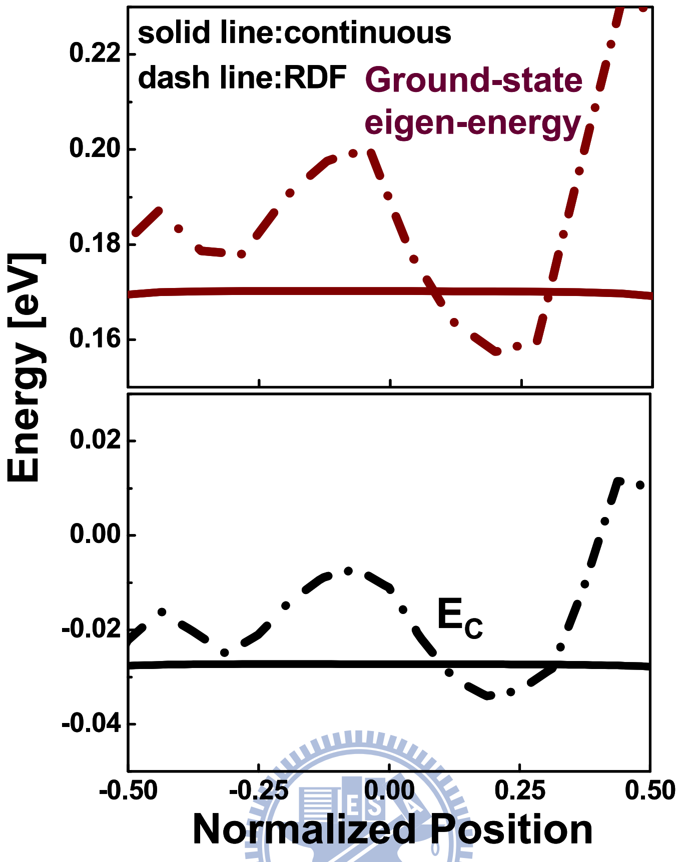

Figure 5-17 RDF-induced spatial fluctuations in E_C and ground-state eigen-energy. The atomistic RDF simulation is performed by considering the long-range part of the atomistic Coulomb potential for each randomly-placed impurity charge [20]. The quantum-confinement (QC) effect is simulated by solving the exact 1-D Schrödinger equation [21].

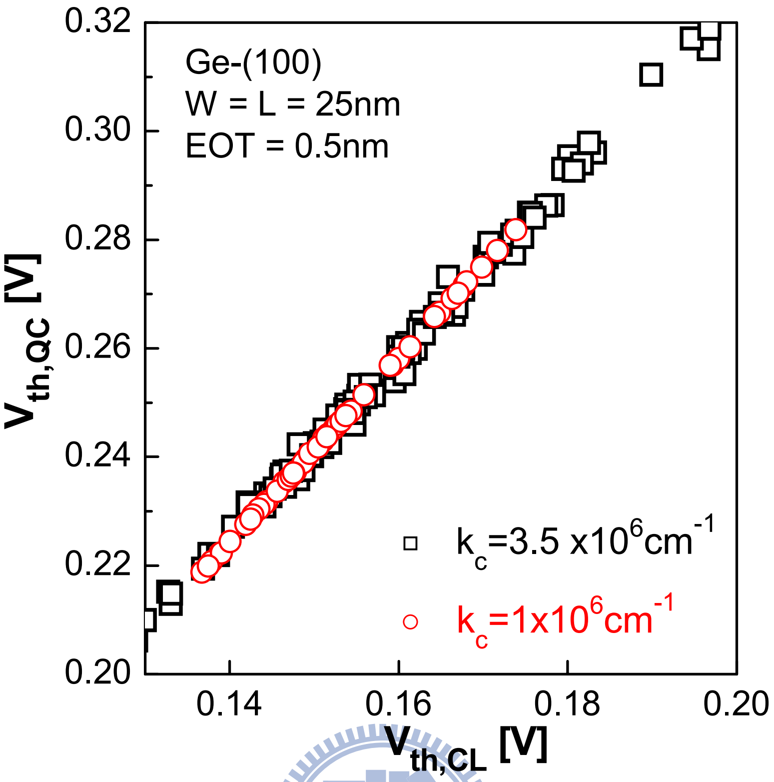

Figure 5-18 The $V_{th,QC}$ dispersion is closely related to the $V_{th,CL}$ dispersion. It can be seen that the slope $dV_{th,QC}/dV_{th,CL}$ is not sensitive to the inverse of the screening length (k_c) used in the long-range RDF simulation [20].

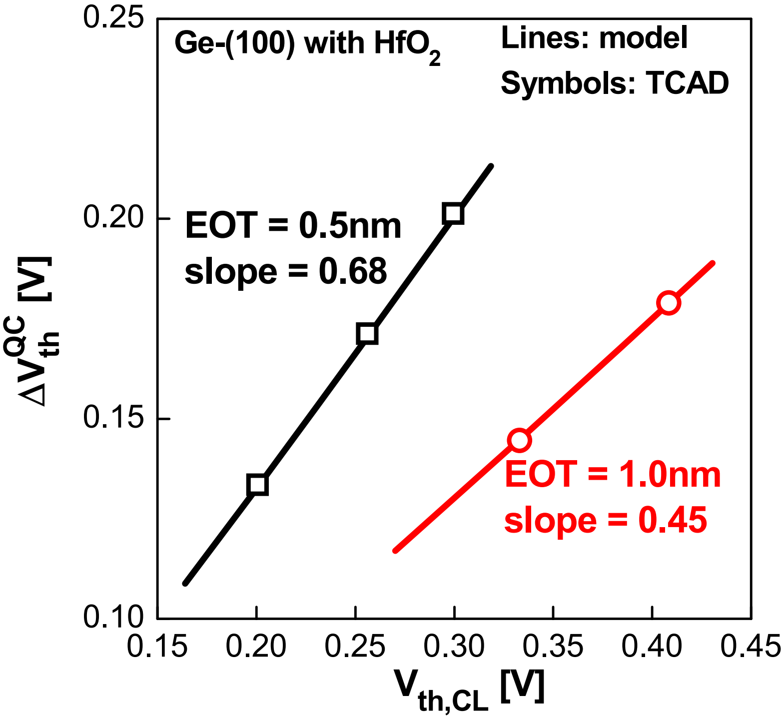

Figure 5-19 The ΔV_{th}^{QC} vs. $V_{th,CL}$ plot for Ge devices with various EOT. The various $V_{th,CL}$ values are due to the change of doping concentration.

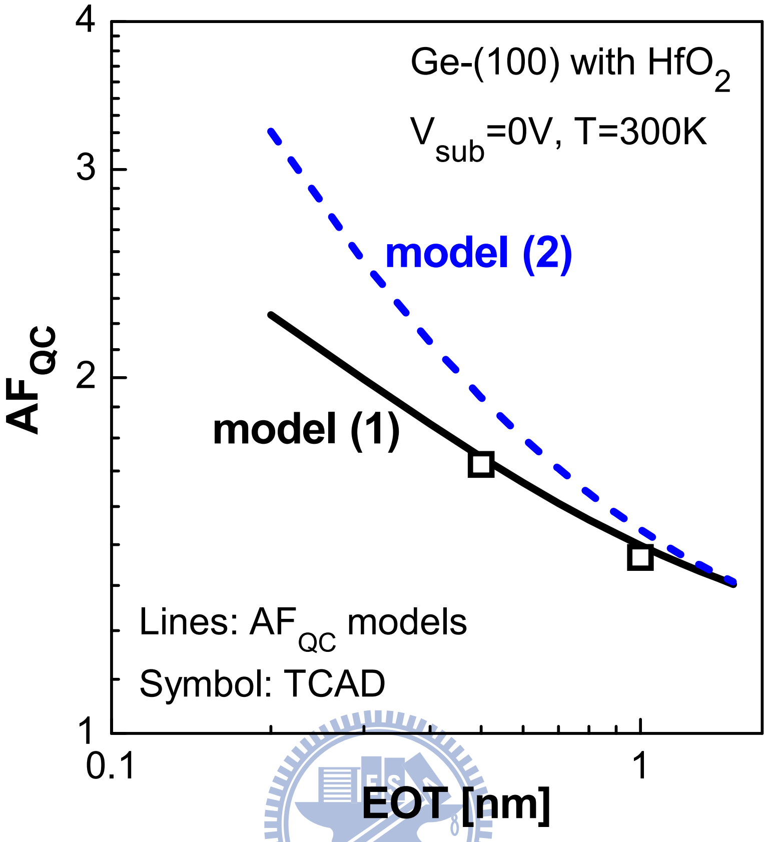

Figure 5-20 As compared with model (2), our model shows more accurate EOT dependence in AF_{QC}.

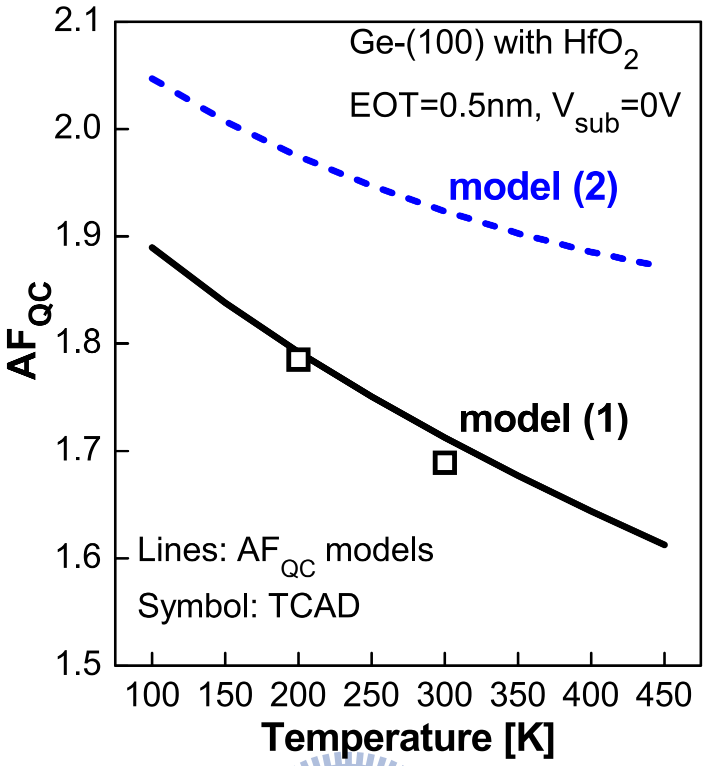

Figure 5-21 As compared with model (2), our model shows more accurate temperature dependence in AF$_{QC}$.

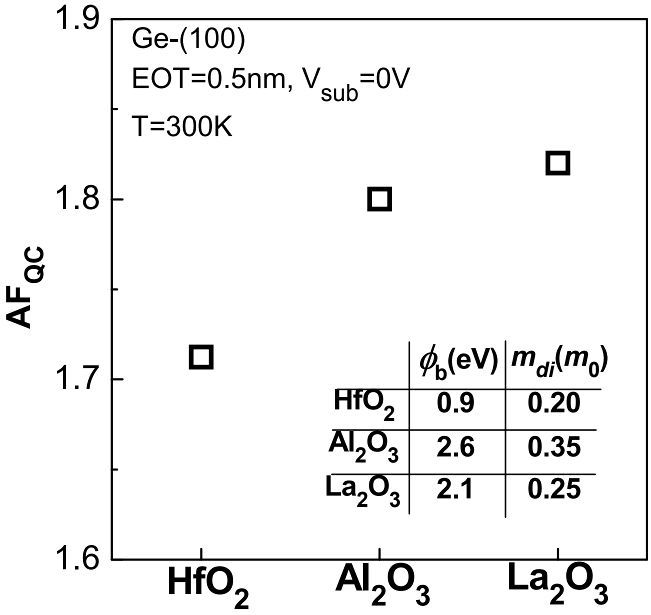

Figure 5-22 The dark space and hence AF$_{QC}$ depend on the dielectric material because of the wavefunction penetration effect.

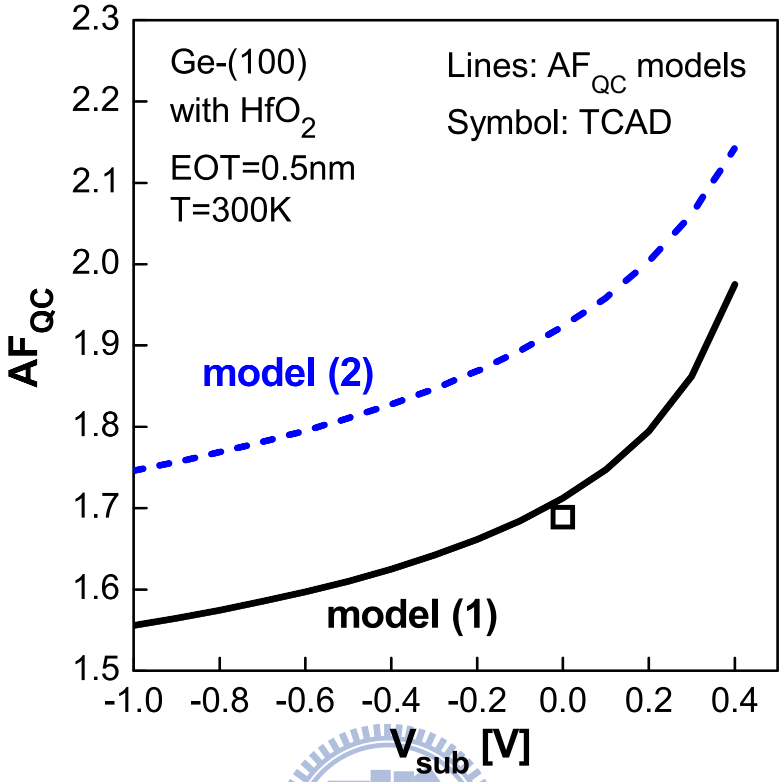

Figure 5-23 The substrate bias dependence of the AF$_{QC}$ is consistent with the dark space [Figure 5-14(a)].

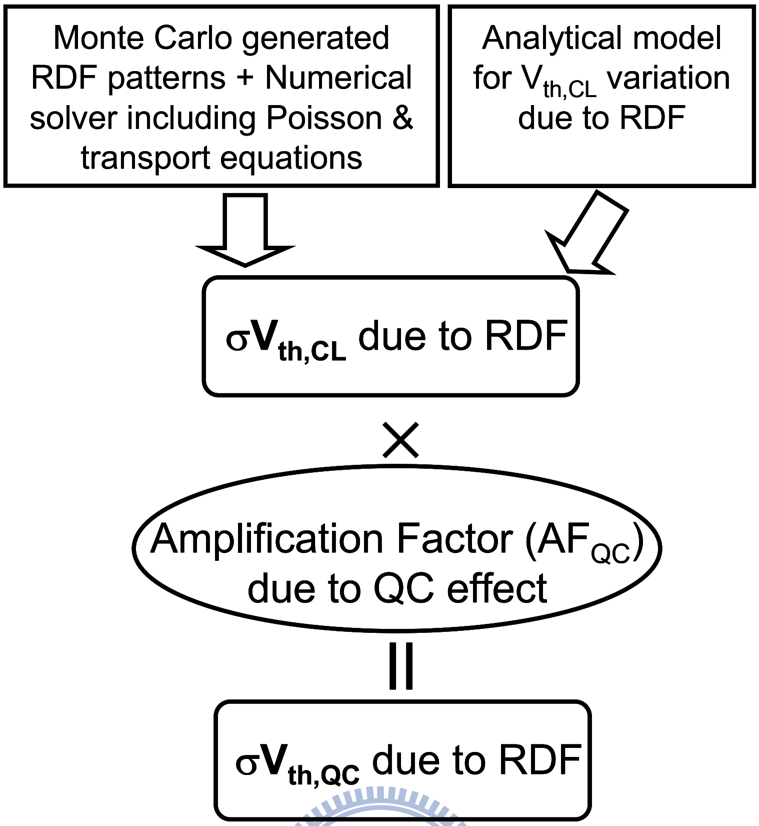

Figure 5-24 Flow chart demonstrating the AF_{QC} approach to assess the $\sigma V_{th,QC}$ due to RDF.

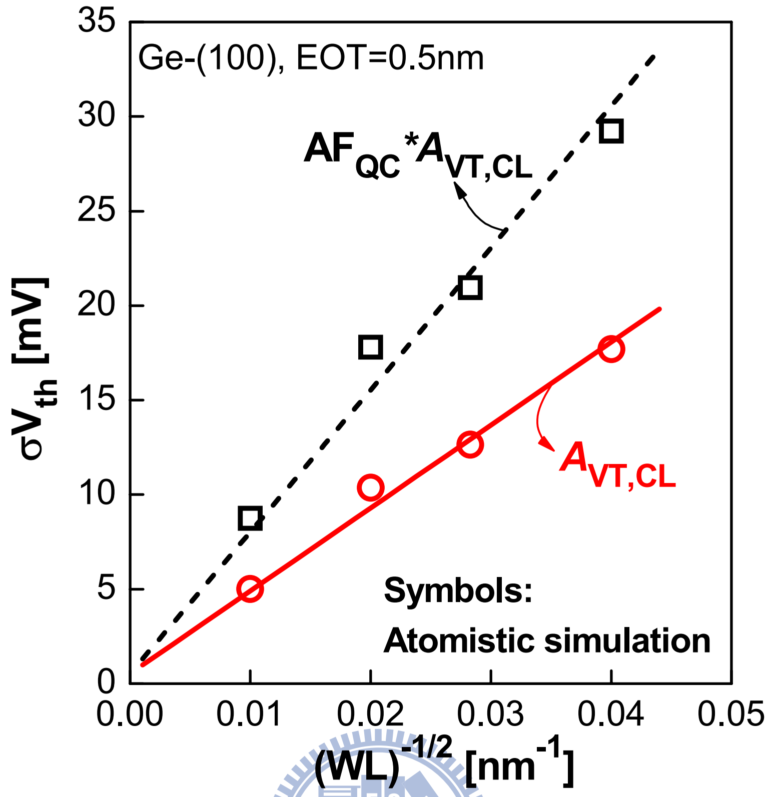

Figure 5-25 The AF_{QC} approach can predict the A_{VT} considering the QC effect through the classical A_{VT} ($A_{VT,CL}$).

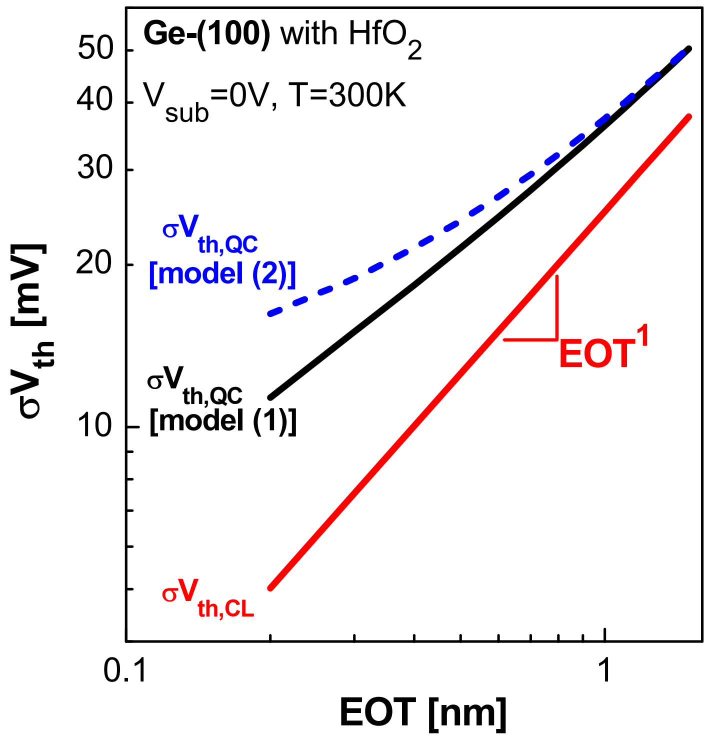

Figure 5-26 The $\sigma V_{th,QC}$ model based on the AF_{QC} approach can demonstrate the fundamental impact of QC effect with EOT downscaling. W = L = 25nm is used in the calculation.

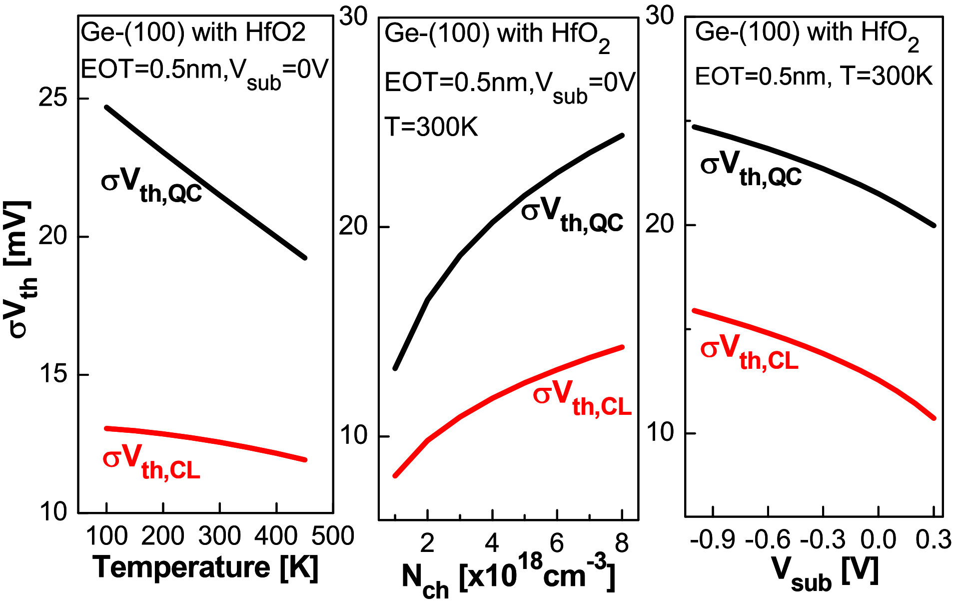

Figure 5-27 Sensitivity of σV_{th} to (a) temperature, (b) channel doping, and (c) substrate bias.

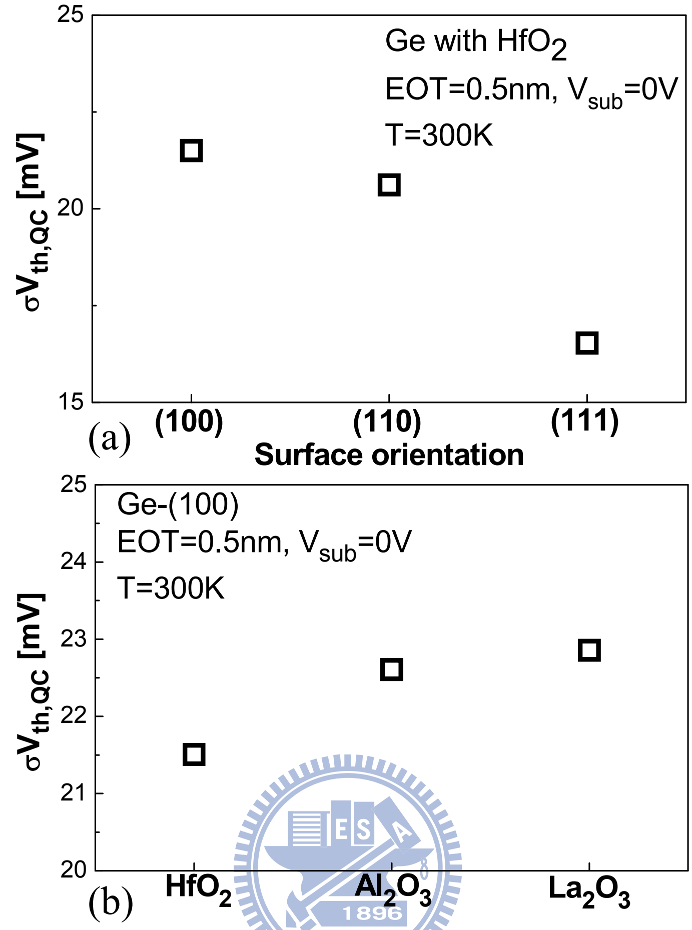

Figure 5-28 Because of the dark space due to QC effect, the $\sigma V_{th,QC}$ depends on the surface orientation and gate dielectric material.

Chapter 6
Switching Time Variations for FinFET and Bulk MOSFETs

6.1 Introduction

With MOSFET scaling, the impact of random dopant fluctuation (RDF) and line edge roughness (LER) on the threshold voltage (V_{th}) variation of nanoscale transistors is growing and being extensively examined [1]-[3]. For example, Asenov *et al.* [2] has shown that as gate dimensions for bulk MOSFETs are reduced, the V_{th} fluctuations increase and are comparable in magnitude to those caused by RDF. Roy et al. [3] has concluded that the V_{th} variation due to RDF would dominate the behavior of the bulk MOSFETs if the LER can meet the prescription of the International Technology Roadmap for Semiconductor (ITRS) [4].

Due to its better gate control, FinFET structure is an important candidate for CMOS scaling. The channel doping of FinFET can be reduced because the short channel effect can be suppressed by the geometry control. The channel RDF in FinFET is not as significant as that in bulk MOSFETs because the lightly doped channel is usually used in FinFET. Thus, the geometry variation becomes the main variation source for FinFET. Brown *et al.* [5] has concluded that LER is the major contributor to parameter fluctuations in sub-10nm FinFET. Baravelli *et al.* [6] has investigated the gate-LER and fin-LER for FinFET. They have demonstrated that for lightly doped FinFET, the V_{th} variation due to fin-LER is larger than that due to gate-LER.

For logic circuits, however, the variation of signal switching time (ST) due to RDF and LER is particularly important. Whether there is any gap between V_{th} and switching time variations merits investigation. The switching time variations for bulk MOSFETs have been investigated using the mixed-mode transient simulation [7], [8]. These studies all demonstrated that the drive current variation caused by RDF results in the intrinsic switching speed variation for bulk MOSFETs. However, how the geometry variation such as LER affects the switching time variation of FinFET has not been reported. Specifically, the impacts of gate-LER and fin-LER on the switching time variations of lightly-doped FinFET are crucial to the logic circuit using FinFET structures. In this chapter, we investigate the switching time variation for bulk MOSFETs [9] and FinFET [10] using the approach of effective drive current in CMOS inverters [11].

6.2 Switching Time Variation Decoupling Using the Effective Drive Current Approach

We decouple the switching time (ST) variation into transition charge (ΔQ) variation and effective drive current (I_{eff}) variation. The ST can be defined as ΔQ / I_{eff} [12], where ΔQ is the transition charge between logic "ON" and "OFF" states. The ΔQ for an NFET can be calculated by Q_n ($V_{GS} = V_{DD}$, $V_{DS} = 0$ V) − Q_n ($V_{GS} = 0$V, $V_{DS} = V_{DD}$) [12]. The I_{eff} for an NFET can be approximated as [I_{DS} ($V_{GS} = V_{DD}$, $V_{DS} = 0.5V_{DD}$) + I_{DS} ($V_{GS} = 0.5V_{DD}$, $V_{DS} = V_{DD}$)] / 2 [11]. Therefore, in contrast to the time-consuming mixed-mode transient simulation [7], [8], only DC simulation for a single device is needed to derive ΔQ and I_{eff}. More importantly, the effective drive current approach may provide physical insights in the assessment of switching time variations.

Since ST = ΔQ / I_{eff}, the ST fluctuation stems from the fluctuations of ΔQ and I_{eff}:

$$ST + \delta ST = \frac{\Delta Q + \delta \Delta Q}{I_{eff} + \delta I_{eff}} \cong \frac{\Delta Q}{I_{eff}} \cdot \left(1 + \frac{\delta \Delta Q}{\Delta Q}\right) \cdot \left(1 - \frac{\delta I_{eff}}{I_{eff}}\right) \cong ST \cdot \left(1 + \frac{\delta \Delta Q}{\Delta Q} - \frac{\delta I_{eff}}{I_{eff}}\right) \qquad (6\text{-}1)$$

where the fluctuation δ is small as compared with its nominal value. Therefore,

$$\frac{\delta ST}{ST} \cong \frac{\delta \Delta Q}{\Delta Q} - \frac{\delta I_{eff}}{I_{eff}} \qquad (6\text{-}2)$$

We assume that the devices with 1σ value of ST (μST + σST) are just the same devices that correspond to 1σ values of ΔQ (μΔQ + σΔQ) and I_{eff} ($\mu I_{eff} + \sigma I_{eff}$), where μ and σ are the mean and the standard deviation of the parameter, respectively. Similarly, the devices with the μ value of ST also correspond to the μ values of ΔQ and I_{eff}. The normalized standard deviation of ST (σST / μST) can thus be approximated as $\sigma ST/\mu ST \cong \sigma\Delta Q/\mu\Delta Q - \sigma I_{eff}/\mu I_{eff}$. It should be noted that the standard deviations (σST, σΔQ and σI_{eff}) are considered as signed numbers, which means they can be either positive or negative values. Practically, the standard deviations derived from the statistical experiments are always positive. Therefore, we take the absolute value:

$$\left|\frac{\sigma ST}{\mu ST}\right| \cong \left|\frac{\sigma \Delta Q}{\mu \Delta Q} - \frac{\sigma I_{eff}}{\mu I_{eff}}\right| = \left|\frac{\sigma I_{eff}}{\mu I_{eff}} - \frac{\sigma \Delta Q}{\mu \Delta Q}\right| \qquad (6\text{-}3)$$

The right-hand-side (RHS) of Equation (6-3) equals to $|\sigma I_{eff} / \mu I_{eff}| - |\sigma\Delta Q / \mu\Delta Q|$ if the σΔQ and σI_{eff} have the same sign (i.e., ΔQ and I_{eff} are positively correlated). On the contrary, the RHS of Equation (6-3) equals to $|\sigma I_{eff} / \mu I_{eff}| + |\sigma\Delta Q / \mu\Delta Q|$ if the σΔQ and σI_{eff} have the opposite sign (i.e., ΔQ and I_{eff} are negatively correlated).

6.3 Switching Time Variations for Bulk MOSFET

The device parameters of bulk MOSFETs used in the simulation is effective gate length (L_{eff}) =25nm, channel width (W) = 25nm, oxide thickness (t_{ox}) = 0.8nm, source/drain junction depth (X_j) = 12.5nm, channel doping (N_{ch}) = 4.8×10^{18} cm^{-3}, and supply voltage (V_{DD}) = 0.8V. To assess the RDF in bulk MOSFETs, we have carried out the atomistic device simulation using the Monte Carlo approach to generate the dopants in the channel [1]. To avoid the charge trapping in the sharp Coulomb potential well and hence the mesh size dependences of the simulation results, we have employed the density gradient method in our atomistic simulation [3]. The boundary condition at the Si/SiO$_2$ interface for the density gradient method is that the carrier density changes continuously across the interface, i.e., the continuity of the wavefunctions across the interface [13]. Figure 6-1(a) shows one of the 150 samples in our atomistic simulation. To assess the LER, the line edge patterns were derived using the Fourier synthesis approach similar to the one in [2], and then the Monte Carlo simulation was performed. The parameters used in the LER simulation is the root-mean-square (rms) amplitude $\Delta = 1$nm [4] and the correlation length $\Lambda = 30$nm. Figure 6-1(b) shows one of the 150 samples in our simulation. In this study, we use the drift-diffusion equation as the transport model. Velocity saturation model is used to assess the on-current under the high drain field.

Figure 6-2(a) compares the saturation threshold voltage ($V_{th,sat}$) distributions due to RDF and LER for bulk MOSFETs. Figure 6-2(b) compares the ST distributions due to RDF and LER. It can be seen that the standard deviation of $V_{th,sat}$ ($\sigma V_{th,sat}$) due to RDF is larger than that due to LER. Nevertheless, Figure 6-2(b) shows that the standard deviation of ST (σST) due to LER is comparable with that due to RDF. In other words, the relative importance of LER for ST variation increases as compared with that for $V_{th,sat}$ variation. This can be explained by Figure 6-3, which shows the $|\sigma ST/\mu ST|$, $|\sigma \Delta Q/\mu \Delta Q|$, and $|\sigma I_{eff}/\mu I_{eff}|$ caused by RDF and LER. It can be seen that the $|\sigma ST/\mu ST|$ due to RDF is roughly equal to $|\sigma I_{eff}/\mu I_{eff}| - |\sigma \Delta Q/\mu \Delta Q|$. However, the $|\sigma ST / \mu ST|$ due to LER is roughly equal to $|\sigma I_{eff} / \mu I_{eff}| + |\sigma \Delta Q / \mu \Delta Q|$.

The results in Figure 6-3 can be explained as follows. The impact of RDF on MOSFETs stems from the variation of the effective channel doping ($N_{ch,eff}$). For devices with smaller $N_{ch,eff}$, the V_{th} is smaller and hence I_{eff} and ΔQ are larger because they are roughly proportional to ($V_{GS}-V_{th}$). Thus, I_{eff} and ΔQ are positively correlated [Figure 6-4(a)] and $|\sigma ST / \mu ST|$ is roughly equal to $|\sigma I_{eff}/\mu I_{eff}| - |\sigma \Delta Q/\mu \Delta Q|$ because the quantities of $\sigma \Delta Q$ and σI_{eff} have the same sign. In other words, the impacts of RDF on ΔQ and I_{eff} are mutually canceled and

$|\sigma ST / \mu ST|$ is reduced.

The impact of LER on MOSFETs results from the variation of the effective channel length (L_{eff}). For devices with shorter L_{eff}, the V_{th} is smaller because of the short channel effect and hence the I_{eff} is larger. As for ΔQ, devices with shorter L_{eff} possess smaller ΔQ because ΔQ is proportional to the gate area ($W \times L_{eff}$). Thus, I_{eff} and ΔQ are negatively correlated [Figure 6-4(b)]. Therefore, $|\sigma ST / \mu ST|$ is roughly equal to $|\sigma\Delta Q / \mu\Delta Q| + |\sigma I_{eff} / \mu I_{eff}|$ because the quantities of $\sigma\Delta Q$ and σI_{eff} have the opposite sign. In other words, the $|\sigma ST / \mu ST|$ is larger than either $|\sigma\Delta Q / \mu\Delta Q|$ or $|\sigma I_{eff} / \mu I_{eff}|$.

6.4 Switching Time Variations for FinFET

The device parameters of FinFET used in the simulation is L_{eff} =25nm, fin-width (W_{fin}) = 15nm, fin-height (H_{fin}) = 30nm, t_{ox} = 0.8nm, channel doping (N_{ch}) = 1×10^{15} cm^{-3}, and V_{DD} = 0.8V. The impact of RDF in the channel is not significant to FinFET with undoped channel. Due to the vertical channel configuration, the LER due to fin patterning for FinFET structure includes gate-LER and fin-LER [6]. The parameters used for the fin-LER and gate-LER simulations are the Δ = 1.5nm [6] and the Λ = 20nm [2]. Figure 6-5(a) shows the nominal FinFET structure with aspect ratio = 2. Figure 6-5(b) and 6-5(c) show one of the samples in gate-LER and fin-LER simulations, respectively. We use the drift-diffusion equation as the transport model. Velocity saturation model is used to assess the on-current under the high drain field.

Figure 6-6(a) compares the impacts of gate-LER and fin-LER on $V_{th,sat}$ variations of FinFET. It can be seen that the standard deviation of $V_{th,sat}$ ($\sigma V_{th,sat}$) due to fin-LER is larger than that due to gate-LER. This comparison result for $V_{th,sat}$ variation in FinFET is consistent with [6]. Nevertheless, Figure 6-6(b) shows that the standard deviation of ST (σST) due to gate-LER is larger than that due to fin-LER. In other words, the relative importance of gate-LER for switching time variation is larger as compared with that for $V_{th,sat}$ variation (Figure 6-7). Figure 6-8 shows the $|\sigma ST / \mu ST|$, $|\sigma I_{eff} / \mu I_{eff}|$, and $|\sigma \Delta Q / \mu \Delta Q|$ caused by gate-LER and fin-LER. The $|\sigma ST / \mu ST|$ due to gate-LER is roughly equal to the $|\sigma I_{eff} / \mu I_{eff}| + |\sigma \Delta Q / \mu \Delta Q|$. However, the $|\sigma ST / \mu ST|$ due to fin-LER is roughly equal to $|\sigma I_{eff} / \mu I_{eff}| - |\sigma \Delta Q / \mu \Delta Q|$. Thus, the different trend of gate-LER and fin-LER can be explained by the opposite correlation of I_{eff} and ΔQ for gate-LER and fin-LER.

The impact of gate-LER on FinFET results from the variation of the effective channel length (L_{eff}). For devices with shorter L_{eff}, the V_{th} is smaller because of the short channel effect and hence the I_{eff} is larger. As for ΔQ, devices with shorter L_{eff} possess smaller ΔQ because ΔQ is proportional to the gate area ($W_{total} \times L_{eff}$ with W_{total} the total effective width for FinFET). Thus, I_{eff} and ΔQ are negatively correlated as shown in Figure 6-9(a). Therefore, $|\sigma ST / \mu ST|$ is roughly equal to the sum of $|\sigma I_{eff} / \mu I_{eff}|$ and $|\sigma \Delta Q / \mu \Delta Q|$. In other words, the $|\sigma ST / \mu ST|$ is larger than either $|\sigma I_{eff} / \mu I_{eff}|$ or $|\sigma \Delta Q / \mu \Delta Q|$.

The impact of fin-LER on FinFET stems from the variation of the effective fin width (W_{fin}). For lightly-doped devices with smaller W_{fin}, the V_{th} is larger because of the suppression of short channel effects [14] and hence the I_{eff} is smaller. As for ΔQ, devices with smaller W_{fin} possess smaller ΔQ because ΔQ is proportional to the gate area. Thus, the I_{eff} and ΔQ are positively correlated as shown in Figure 6-9(b). Therefore, $|\sigma ST / \mu ST|$ is roughly equal to the difference between $|\sigma I_{eff} / \mu I_{eff}|$ and $|\sigma \Delta Q / \mu \Delta Q|$. In other words, the impacts of fin-LER on I_{eff} and ΔQ are mutually canceled and $|\sigma ST / \mu ST|$ is reduced.

In the derivation of Equation (6-3), we have assumed that devices with 1σ (or μ) value of ST are those correspond to 1σ (or μ) value of ΔQ and I_{eff}. However, if the distributions of I_{eff} and ΔQ are not highly correlated (i.e., the correlation coefficient is not close to +1 or -1), some error may be introduced in (4). It can be seen in Figure 6-9 that the correlation coefficients between I_{eff} and ΔQ due to gate-LER (-0.44) and fin-LER (0.82) are not very close to ±1. Therefore, in Figure 6-8, the $|\sigma ST / \mu ST|$ is not exactly equal to the sum or the difference of $|\sigma I_{eff} / \mu I_{eff}|$ and $|\sigma \Delta Q / \mu \Delta Q|$. Although Equation (6-3) is not quantitatively very accurate in Figure 6-8, it can still provide simple and physical relationship between the ST variation and the I_{eff} and ΔQ variations.

6.5 Summary

In this chapter, we investigate the impact of RDF and LER on the switching time variations of bulk MOSFETs and FinFET using the effective drive current approach that decouples the switching time variation into ΔQ and I_{eff} variations. Our results indicate that for bulk MOSFETs, although the RDF has been recognized as the main variation source to V_{th} variation, the relative importance of LER increases as the switching time variation is considered. This is because I_{eff} and ΔQ variations due to RDF are mutually canceled and the switching time variation caused by RDF is reduced, while I_{eff} and ΔQ variations due to LER increase the switching time variation caused by LER. As for lightly-doped FinFET, although the impact of fin-LER is more crucial to V_{th} variation, the relative importance of gate-LER increases as the switching time variation is considered.

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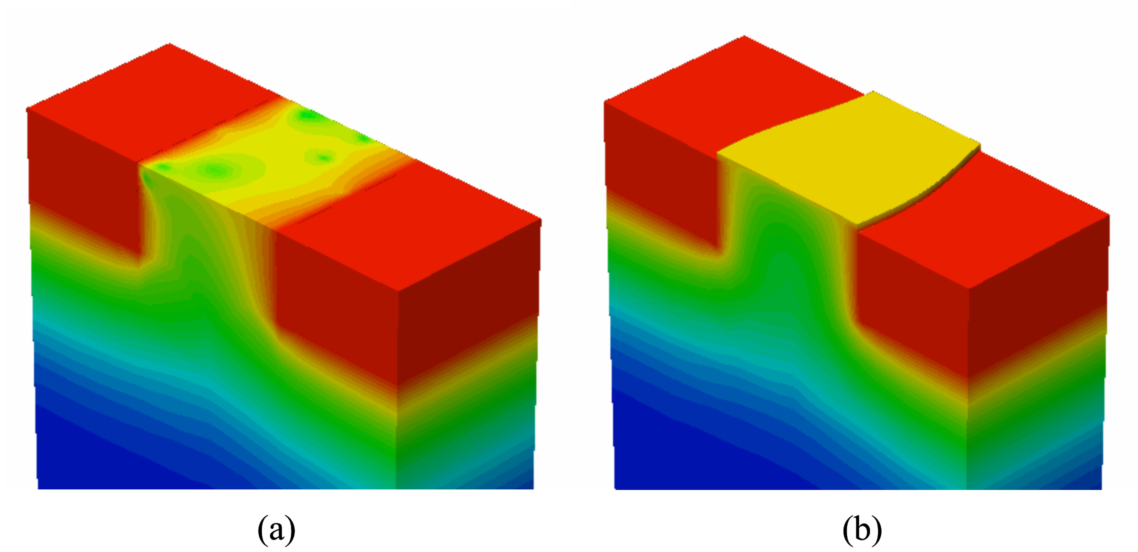

(a)
(b)

Figure 6-1 The simulated bulk MOSFETs in this study. (a) One of the samples with RDF and (b) one of the samples with LER.

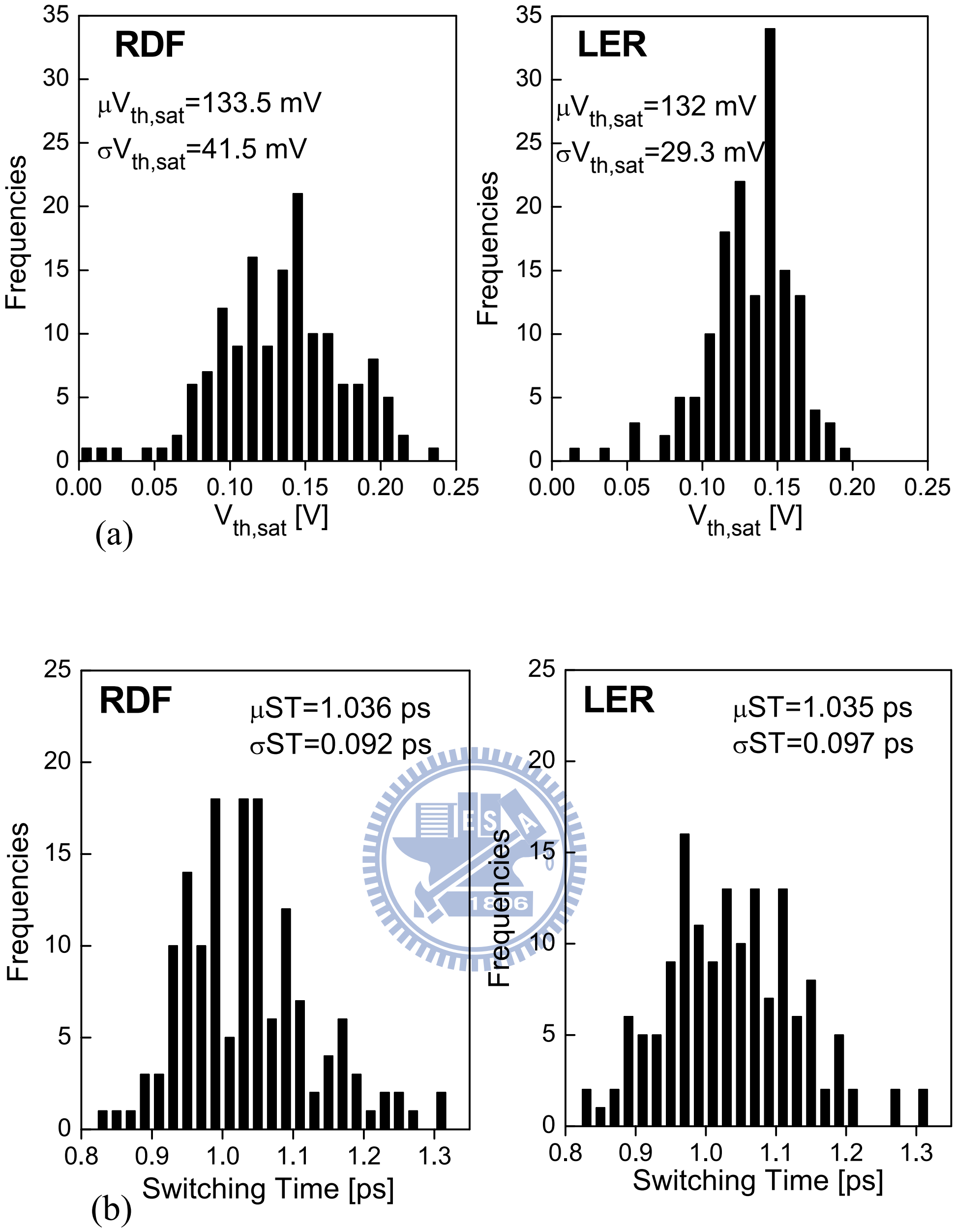


Figure 6-2 (a) $V_{th,sat}$ distribution of 150 samples due to RDF and LER. (b) ST distribution of 150 samples due to RDF and LER.

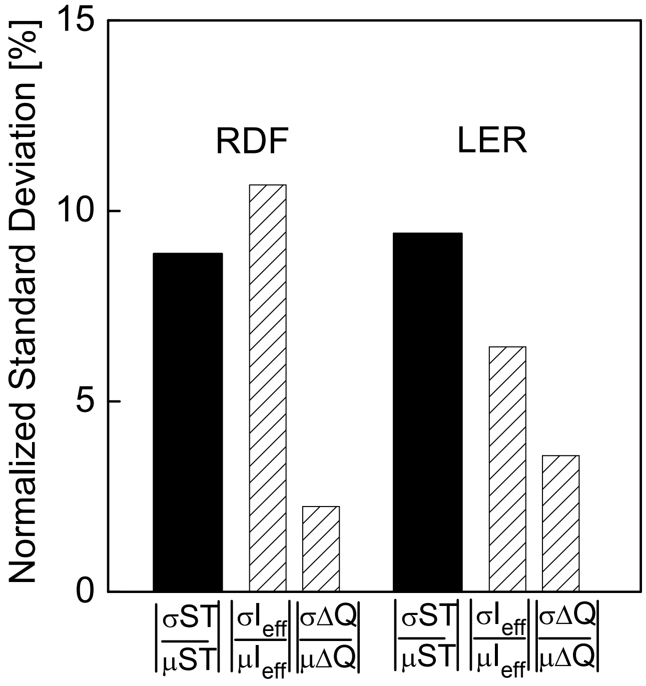


Figure 6-3 The normalized standard deviations of ST, I_{eff} and ΔQ due to RDF and LER.

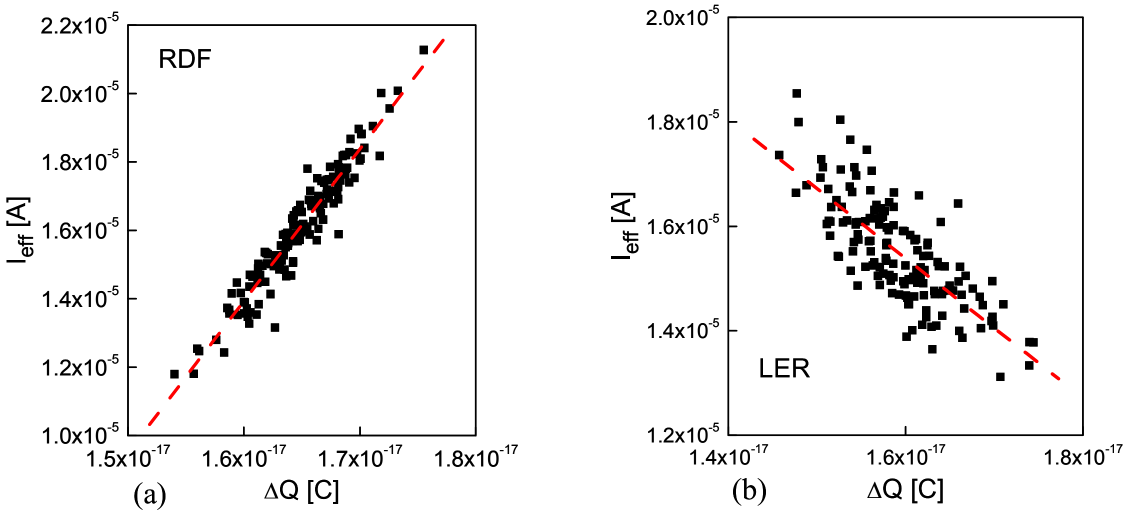
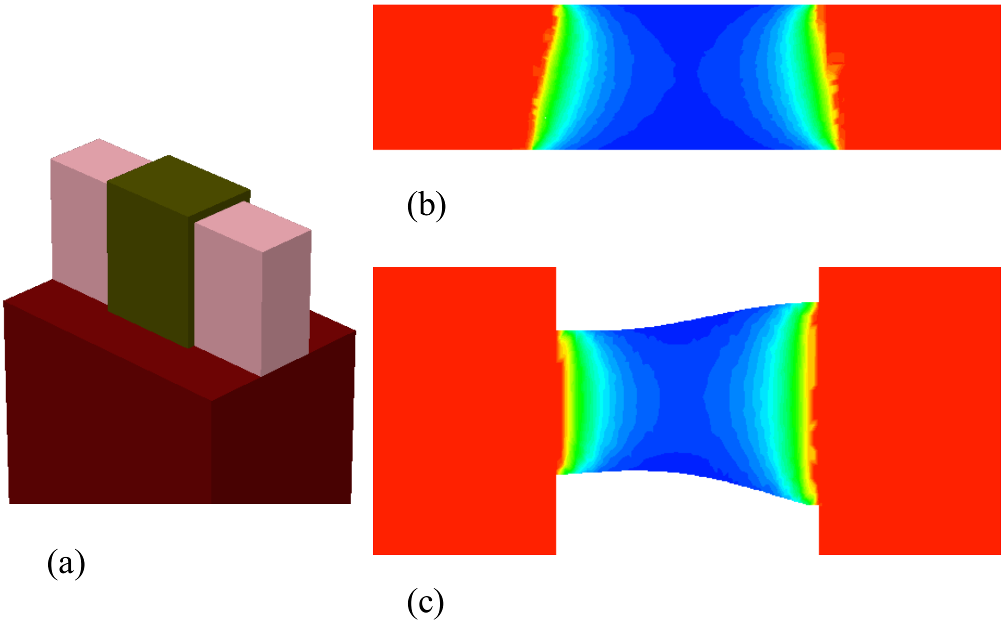


Figure 6-4 The correlations of I_{eff} distribution and ΔQ distribution for MOSFETs with (a) RDF and (b) LER.

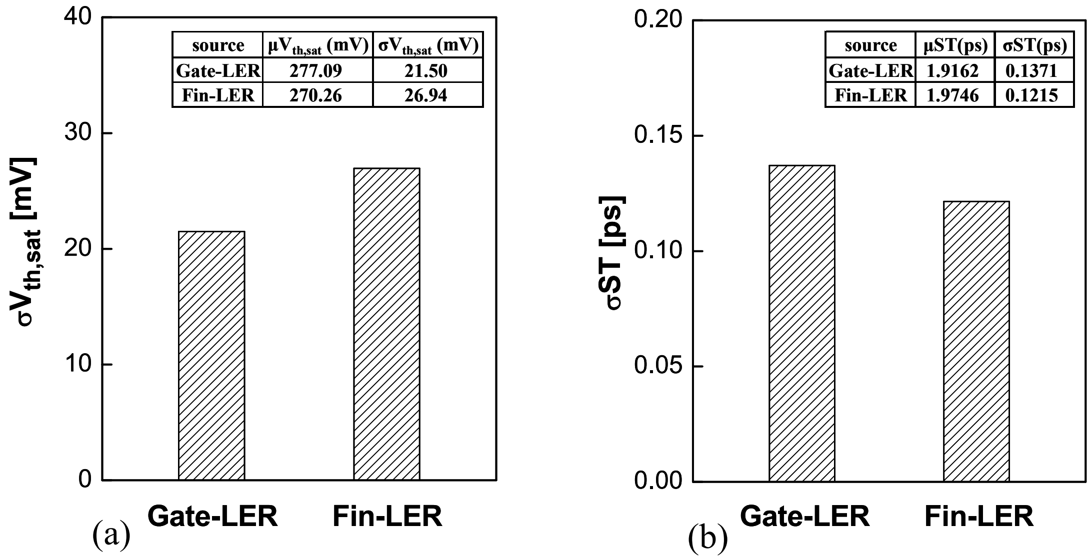


(a)

(b)

(c)

Figure 6-5 (a) The nominal FinFET structure with aspect ratio = 2. (b) One of the samples with gate-LER. (c) One of the samples with fin-LER.



source	μV$_{th,sat}$ (mV)	σV$_{th,sat}$ (mV)
Gate-LER	277.09	21.50
Fin-LER	270.26	26.94

source	μST(ps)	σST(ps)
Gate-LER	1.9162	0.1371
Fin-LER	1.9746	0.1215

Figure 6-6 (a) Comparison of the standard deviations of $V_{th,sat}$ due to gate- and fin-LER in FinFET. (b) Comparison of the standard deviations of ST due to gate- and fin-LER in FinFET.

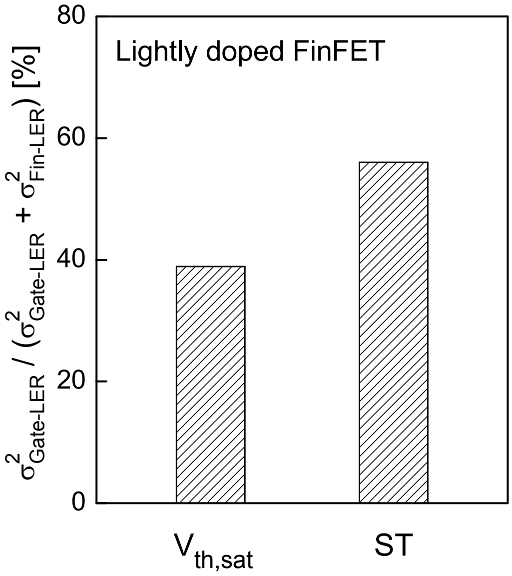


Figure 6-7 The relative importance of $V_{th,sat}$ and ST variation caused by gate-LER for FinFET. Assume that gate-LER and fin-LER are independent variation sources.

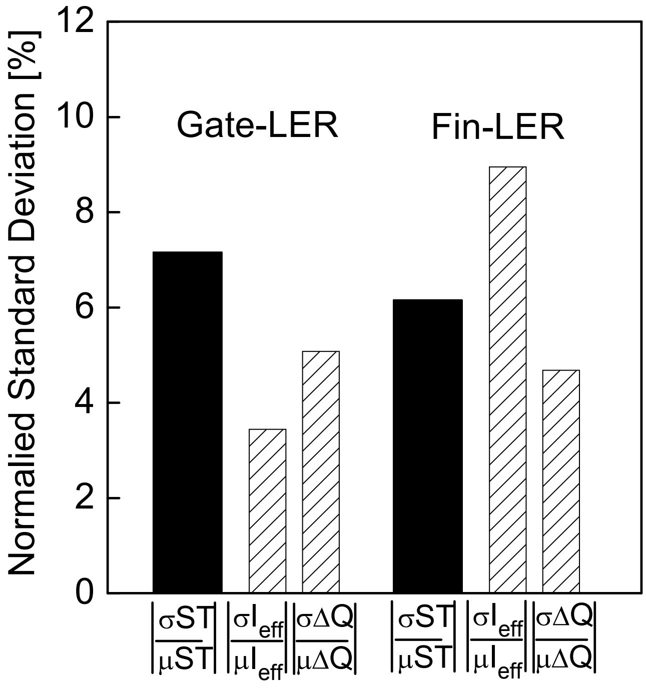
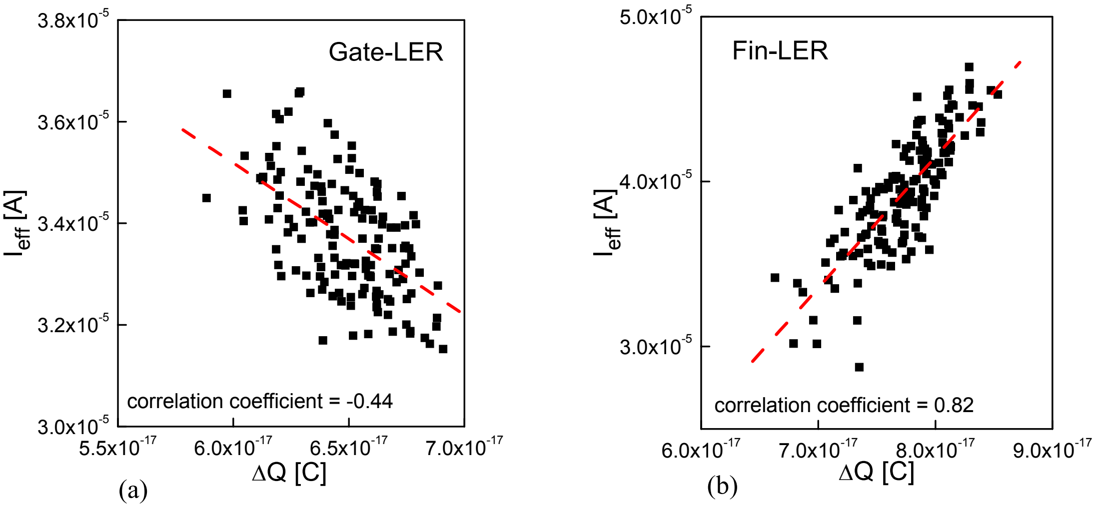


Figure 6-8 The normalized standard deviations of ST, I_{eff} and ΔQ due to gate-LER and fin-LER in FinFET.



(a)

(b)

Figure 6-9 The correlations of I_{eff} distribution and ΔQ distribution for FinFET with (a) gate-LER and (b) fin-LER.

Chapter 7
Conclusion

With MOSFET scaling, the impacts of process variations and random dopant fluctuation are main chanllenges for nano-CMOS device design. Based on the analytical solutions of Poisson and Schrödinger equation, we have established a theoretical framework to investigate the device scalability and sensitivity to process variations by tackling the electrostatic integrity and the impacts of quantum-confinement effect. This theoretical framework includes advanced device structures such as multi-gate, and GAA and UTB devices, and can be applied to devices with high mobility channel materials.

From the prospective of electrostatic integrity, we have compared the sensitivity of V_{th} to process variations for multi-gate devices with various aspect ratio (AR) and GAA device using analytical solutions of 3-D Poisson's equation [1], [2]. Our study indicates that lightly doped GAA device shows the smallest V_{th} variation caused by process variation and dopant number fluctuation. For heavily doped devices, dopant number fluctuation may dominate the overall V_{th} variation. The V_{th} dispersion of GAA device may therefore be larger than that of multi-gate MOSFETs because of its larger surface-to-volume ratio. We have also analyzed the impact of AR on the V_{th} dispersion due to dopant number fluctuation for multi-gate MOSFETs [3]. For heavily doped channel, Quasi-planar device shows smaller V_{th} dispersion because of its larger channel volume. The V_{th} dispersion due to random dopant fluctuation may still be significant in the lightly doped channel, especially for Tri-gate and Quasi-planar devices because of the larger V_{th} sensitivity to the channel doping.

Using the derived analytical solutions of Schrödinger equation for short-channel devices, we have investigated the impact of quantum-confinement effect on the sensitivity of V_{th} to process variations [4], [5]. Our theoretical models consider the parabolic potential well due to short-channel effects and therefore can be used to assess the quantum-confinement effect in short-channel devices [4], [6]. Our study indicates that, for ultra-scaled FinFET and GAA devices, the importance of channel thickness variation increases due to the quantum-confinement effect. For FinFET, the Si-(100) and Ge-(111) surfaces show lower V_{th} sensitivity to the t_{ch} variation as compared with other orientations. On the contrary, the quantum-confinement effect reduces the V_{th} sensitivity to the L_{eff} variation, and Si-(111) and Ge-(100) surfaces show lower V_{th} sensitivity as compared with other orientations. As the V_{th} sensitivity to t_{ch} for short-channel device is determined by the short-channel effect and the quantum-confinement effect, the t_{ch} of GAA MOSFETs can be optimized to reduce the V_{th} variation [6].

Using the derived analytical solutions of Schrödinger equation, we have investigated the impact of quantum-confinement on the short-channel effect of UTB [7] and multi-gate MOSFETs. When the t_{ch} is smaller than critical thickness, the quantum-confinement effect may decrease the V_{th} roll-off of GeOI MOSFETs. Thus, Ge devices may exhibit better V_{th} roll-off than the Si counterpart because of more significant quantum confinement. For multi-gate structure, by exploring the quantum-confinement effect along the H_{fin} direction, the V_{th} roll-off of InGaAs devices can be suppressed and become smaller than the Ge counterpart. This 2-D quantum-confinement effect is also crucial to the scalability of multi-gate device. By exploring a wide design space with various AR, our study indicates that for a given subthreshold swing, Tri-gate (AR=1) with significant 2-D confinement effect exhibits better V_{th} roll-off than FinFET (AR>1).

For planar bulk structure, we have provided closed-form models of quantum "dark space" [8], [9] and ground-state eigen-energy for Ge and Si MOSFETs with high-k gate dielectric. These models show accurate dependences on barrier height, surface electric field, and quantization effective mass of channel and gate dielectric. Our models predict that as the dark space decreases with reverse substrate bias and increasing channel doping, the quantum-confinement induced V_{th} shift shows the opposite dependences with substrate bias and channel doping. Our model can also be used for devices with the steep retrograde doping profile. This physically accurate dark space model will be crucial to the prediction of the subthreshold swing and quantum-confinement induced V_{th} shift of advanced Ge devices. Using the closed-form dark space model, we have provided a closed-form model for the quantum-confinement induced amplification factor (AF_{QC}) in σV_{th} due to random dopant fluctuation. Therefore, a scalable quantum-mechanical σV_{th} model can be obtained through the classical model multiplied by AF_{QC}. Using our model, various factors such as EOT and temperature that may modulate/reduce the impact of RDF on Ge MOSFETs can be accurately assessed.

The impact of RDF and LER on the switching time variations of bulk MOSFETs and FinFET have been assessed using the effective drive current approach that decouples the switching time variation into transition charge (ΔQ) and effective drive current (I_{eff}) variations [10], [11]. Our results indicate that for bulk MOSFETs, although the RDF has been recognized as the main variation source to V_{th} variation, the relative importance of LER increases as the switching time variation is considered. This is because I_{eff} and ΔQ variations due to RDF are mutually canceled and the switching time variation caused by RDF is reduced, while I_{eff} and ΔQ variations due to LER increase the switching time variation caused by LER. As for lightly-doped FinFET, although the impact of fin-LER is more crucial to V_{th} variation, the relative importance of gate-LER increases as the switching time variation is considered.

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Appendix 1

Effective Masses for Si, Ge and InGaAs

We have employed the effective mass approximation [1], [2] to deal with the Schödinger equation in this dissertation. The effective mass approximation assumes parabolic energy dispersion, which is valid for the bottom of the energy bands. Although the effective mass approximation may exhibit deviations from the actual band structure, it has been shown that for Si and Ge devices with t_{ch} down to 2nm, the ground-state eigen-energies calculated by the effective mass approximation are fairly consistent with those calculated by the full-band quantization approach [3].

The constant-energy ellipses of Si and Ge materials possess anisotropic effective masses such as the transverse effective mass (m_t) and the longitudinal effective mass (m_l). Thus, both the quantization effective mass (m_x) and the density-of-state effective mass (m_d) show surface-orientation dependences. Stern [1] had derived the effective masses of Si and Ge with various surface orientations, as listed in Table A1-1. The m_x is the effective mass perpendicular to the surface. For the 1-D quantum-confinement (such as bulk MOSFETs, FinFETs, and UTB devices), the m_d is $(m_1 \cdot m_2)^{1/2}$ [1] where m_1 and m_2 are the effective masses of the two directions parallel to the surface. By substituting the parameters m_t and m_l for Si and Ge into Table A1-1, we can derive the m_x and m_d values shown in Table 3-1. For the material with isotropic effective mass (such as InGaAs), the m_x and m_d are the same. The m_{ch} in Chapter 5 denotes the quantization effective mass in the channel, and hence is identical to the m_x in Table 3-1.

In Section 4.3, both m_x (quantization effective mass along the W_{fin} direction) and m_z (quantization effective mass along the H_{fin} direction) are needed to determine the eigen-energies of 2-D quantum-confinement in multi-gate devices. For $In_{0.53}Ga_{0.47}As$ with isotropic effective mass, $m_x = m_z = 0.04m_0$ [5], [6] is used in our calculation.

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Table A1-1 Effective masses for Si and Ge with various surface orientations [1]. For Si and Ge, the principle effective masses in the ellipsoids are two identical mt and one ml. For Si, m_t = 0.191m_0 and m_l = 0.916m_0. For Ge, m_t = 0.082m_0, m_l = 1.59m_0 for L-valley, m_t = m_l = 0.04m_0 for Γ valley, and m_t = 0.20m_0, m_l = 0.90m_0 for X-valley [4]. For $In_{0.53}Ga_{0.47}As$, m_t = m_l = 0.04m_0 [5], [6].

Surface orientation	**Si**			
	m_x	m_1	m_2	**degeneracy**
(100)	m_l	m_t	m_t	2
	m_t	m_l	m_t	4
(110)	$(2m_tm_l)/(m_t + m_l)$	m_t	$(m_t + m_l)/2$	4
	m_t	m_t	m_l	2
(111)	$(3m_tm_l)/(m_t + 2m_l)$	m_t	$(m_t + 2m_l)/3$	6

Surface orientation	**Ge**			
	m_x	m_1	m_2	**degeneracy**
(100)	$(3m_tm_l)/(m_t + 2m_l)$	m_t	$(m_t + 2m_l)/3$	4
(110)	$(3m_tm_l)/(m_t + 2m_l)$	m_t	$(m_t + 2m_l)/3$	2
	m_t	m_t	m_l	2
(111)	m_l	m_t	m_t	1
	$(9m_tm_l)/(m_t + 8m_l)$	m_t	$(m_t + 8m_l)/9$	3

Appendix 2

Γ-Valley and X-Valley in Ge Devices

For the Ge devices, only L-valley is considered in this dissertation because other conduction band bottoms such as Γ-valley and X-valley have energy offsets of 0.135eV and 0.173eV, respectively, higher than the L-valley [1]. The relative importance of Γ- and X-valley may increase when the E_0 of Γ- and X-valley plus the energy offset get close to the E_0 of L-valley (energy offset = 0). Figure A2-1 compares the E_0's plus the energy offsets for L-valley, Γ-valley and X-valley in heavily-doped Ge bulk MOSFETs. As the F_S increases, although the X-valley of the Ge (100)-surface possesses larger m_x ($0.27m_0$) than that of the L-valley ($m_x = 0.12m_0$) [1], their difference in E_0 is not significant. This is because under the "electrical confinement," the E_0 is weakly dependent on m_x [see Equation (5-12)]. Using Equation (5-12), Figure A2-1 shows that the difference in the minimum energy between L- and X-valley is still larger than $5kT$ under the F_S near the onset of threshold. Therefore, the impact of X-valley is negligible in the subthreshold region for heavily-doped Ge bulk MOSFETs. As to the Γ-valley, its impact is even smaller than the X-valley because of the small m_x ($0.062m_0$ [1]).

Figure A2-2(a) compares the E_0's plus the energy offsets for L-valley, Γ-valley and X-valley in lightly-doped FinFET. It can be seen that as the t_{ch} down-scales, the E_0 of Γ-valley is considerably smaller than that of L-valley. Thus, the difference in the minimum energy between L- and X-valley is not as significant as that in the heavily-doped bulk devices. This is because under the "structural confinement," the E_0 is (to the first order) inversely proportional to m_x. Figure A2-2(a) shows that the difference in the minimum energy between L- and X-valley is $2.5kT$ when t_{ch} = 4nm. Figure A2-2(b) demonstrates the ratio of the sheet electron density (Q_i) in Γ-valley and X-valley with respect to that in L-valley. It can be seen that the relative importance of Γ-valley decreases with t_{ch} because of the smaller m_x and hence larger E_0. On the contrary, the relative importance of X-valley increases with decreasing t_{ch} because of the larger m_x and hence smaller E_0. When t_{ch} = 4nm, the electrons in the X-valley achieve 10% of those in the L-valley.

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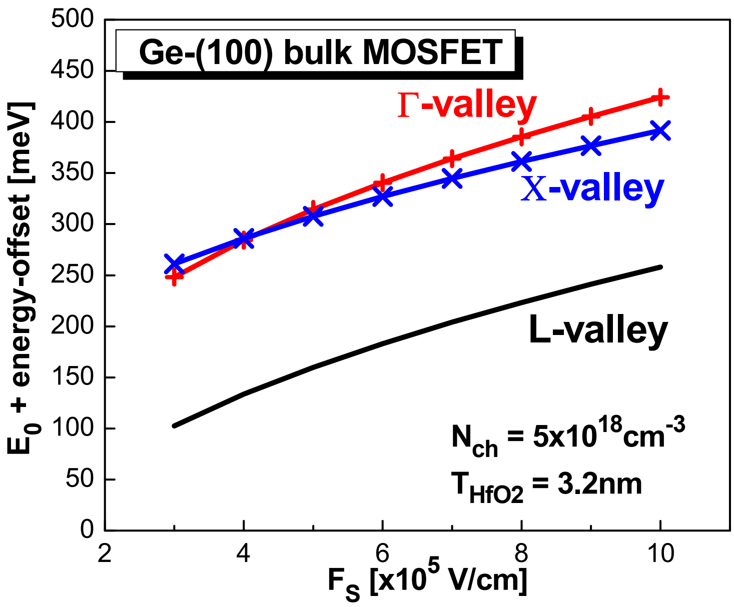

Figure A2-1 Comparison of F_S dependences of E_0's plus the energy offsets for L-valley, Γ-valley and X-valley in heavily-doped Ge bulk MOSFETs.

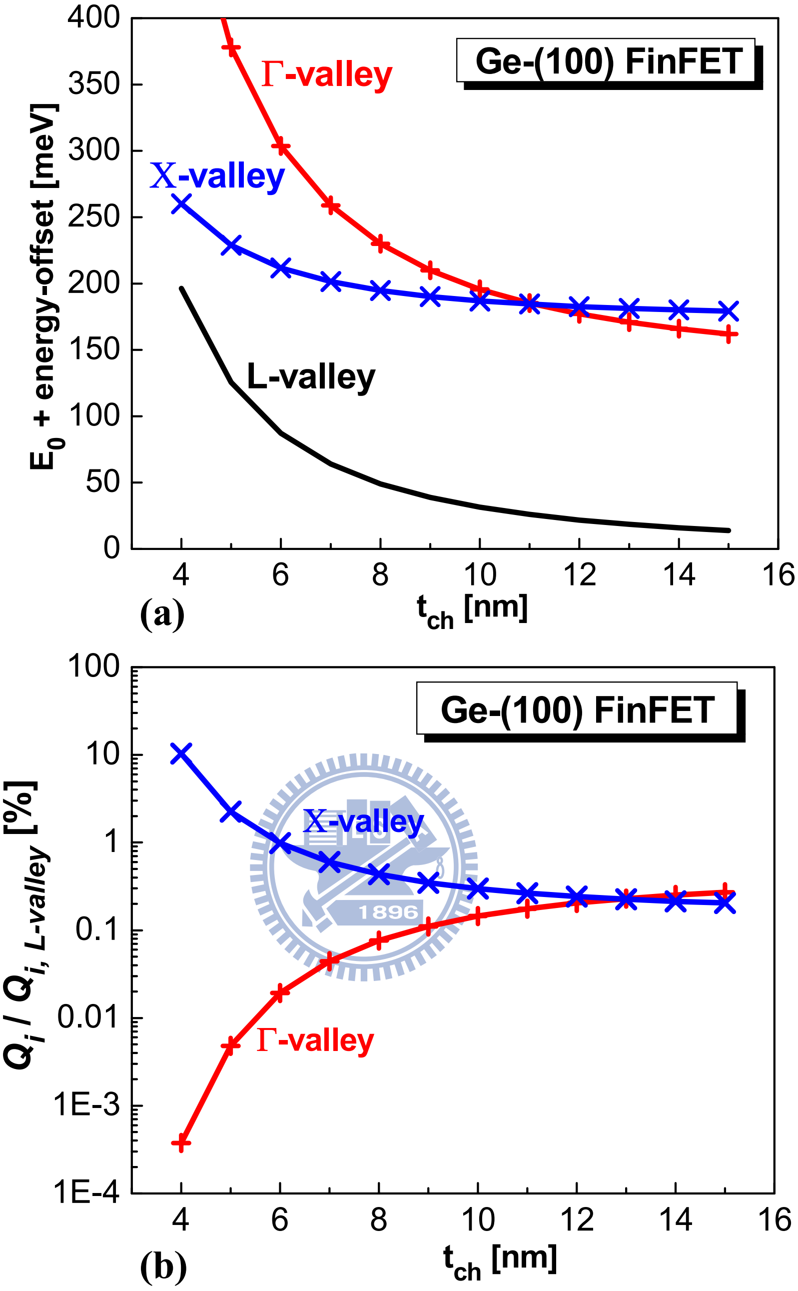

Figure A2-2 (a) Comparison of t_{ch} dependences of E_0's plus the energy offsets for L-valley, Γ-valley and X-valley in lightly-doped Ge FinFET. (b) Comparison of the ratio of the Q_i for Γ-valley and X-valley with respect to that for L-valley in lightly-doped Ge FinFET.

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Publication List

Journal Papers:

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