國立交通大學

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碩士論文

應用於液晶顯示器背光之發光二極體驅動與均流控制電路之設計

The Design of a LED Driver with Current Balance Control Circuit for the Backlight of LCD Display

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中華民國九十七年十月

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摘　要

由於發光二極體各項應用起飛，包括大型看板、車用發光二極體與背光源使用逐年提高，照明商機逐漸提高。特別是在 NB 面板方面，就光源成本來看，雖然發光二極體約為 CCFL 的 2.5 倍，總成本約高出 70%，但採用發光二極體背光源優點為: 省電，將提升 NB 約 40~60 分鐘使用時間 ； 輕薄，背光模組約可節省一半厚度 ； 重量較輕 ； 色彩飽和度較佳。

液晶顯示技術往液晶電視快速發展的契機受限於數位顯示技術發展，而在液晶電視尺寸大型化後，必須在成本上降低，才能夠與傳統電視以及電漿電視相競爭。並且，液晶顯示技術本身為一種非自發光型的顯示技術，需依賴著背光源才能夠把影像顯示出來，在面板的應用上，背光源通常需要大量的發光二極體來提供光源，因此若能有效率佳且負載能力好之驅動電路則將可降低系統成本。

本篇論文中提出應用於液晶顯示器背光之發光二極體驅動與均流控制電路之設計，其輸入電壓為 12V，而輸出電壓為 40V。其中回授控制電路以脈波寬度調變之方式實現，並擁有根據發光二極體順向電壓改變的回授機制，使此電路能夠提供更高的可靠度，供發光二極體作為背光源使用。另外由於考量發光二極體作為背光源所需要的電流匹配度，均流控制電路也一併於本論文中提出。本論文之設計使用 VIS 0.5um 嵌入高壓 5V/40V 2P3M CMOS 製程技術進模擬與製作。

The Design of a LED Driver with Current Balance Control Circuit for the Backlight of LCD Display

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Abstract

The commercial possibilities of the LED are increasing gradually since the applications of light-emitting diode are more and more prevalent in large scanning boards, vehicle-used light-emitting systems and backlighting-used display systems. Considering the cost of light source in the panel of notebook computer, the cost of light-emitting diode is 2.5 times than that of the cold cathode fluorescent lamp (CCFL). That is, it costs more than 70% of the original design. However, there are some important advantages by means of LED as a backlight module. Especially, energy saving improves the battery lifetime longer than 40% of the original design by means of CFFL backlight module. The LED backlight module can reduce the thickness of panel module. Thus, the weight is light and the color saturation is better than before. The impeding of liquid crystal display technique expending to the liquid crystal television is the developing of the digital display technique. After scaling up the size of the liquid crystal television, it should lower the cost to compete with the conventional television and plasma television. Besides, the liquid crystal display is a non-self-luminous technique and thus it leans on the backlight source to display the image. In the applications of the LCD panel, the backlight source usually needs large amount of light-emitting diodes to provide enough brightness. Therefore, if the driver circuit has high efficiency and good driving capability, the cost of the LED system can be reduced.

This thesis proposes a LED driver with current Balance control circuit for the backlight of LCD display. This driver circuit design was simulated and fabricated in VIS 0.5μm embedded high voltage 5V/40V CMOS technology. The input voltage is 12V and the output voltage is 40V. The boost voltage regulator uses a pulse width modulation (PWM) and a reference tracking circuit according to the variation of forward voltage of LEDs. The advantage of the proposed method is to offer high reliability to the LED backlight system.

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站在巨人的肩上遠眺，我發現，這所有的感動將匯集成助力，期望某一天，
我得以輕舞飛揚，抓住夢想。

邱佳麟
2008.11.06

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Chapter 1

Introduction

1.1. Background

In the past, the back light module of liquid crystal display (LCD) was mainly consisted of cold cathode fluorescent lamp (CCFL). However the CCFL does not have a good color space and its lifetime is just about 15000~50000 hours. Furthermore, there are some environmental issues in CCFL backlighting because it has hazardous material inside the lamp [1] [2] [3]. For the reasons, technology has been going through a transition which LED substitutes for CCFL as LCD backlight material. Furthermore, the red, green and blue (RGB) LEDs produce a color spectrum that is larger than not only the NTSC color space but also CCFL [4]. Due to the advances in the technology of LED, the benefits for LED backlight has become evident.

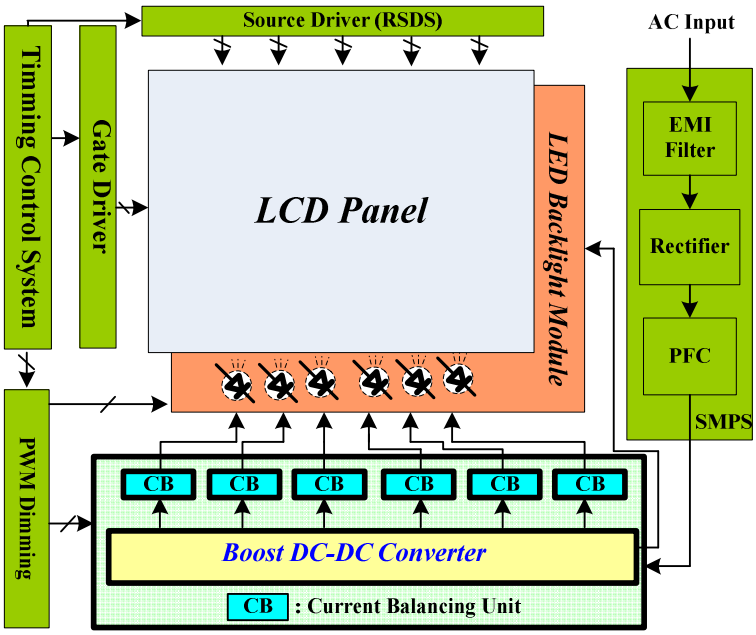


Fig. 1. LED backlight driving block diagram

The common LED backlight structure is usually like Fig. 1. It is composed of two parts. Firstly, boost DC/DC converter is to offer a sufficient voltage to overcome the LED forward voltage. Secondly, current balance unit is to regulate the current flow through each LED string and also have PWM dimming circuit to change the illumination through averaging the driving current. The current regulator also includes a minimum voltage detector and open loop detector for boost converter to dynamically regulate the output voltage, thus it can reduce unnecessary power loss.

1.2. The Basic Concepts of Current Regulators

The LED I-V curve is shown in Fig. 2. [5]. The forward voltage variation of LEDs is expected. LED can be manufactured with smaller mismatch, but it will increase the cost. Beside, the forward voltage also varies with temperature and time. In order to get high quality image for LCD TV, it is impossible to change the backlight brightness through forward voltage. In other words, the luminance is proportional to the level of driving current. The higher driving current will cause the higher brightness. As a result, by using the current to dimming the LEDs can prevent the variation of forward voltage and increase the brightness uniformity of LED backlight. Therefore, a high quality image of LCD TV can be obtained.

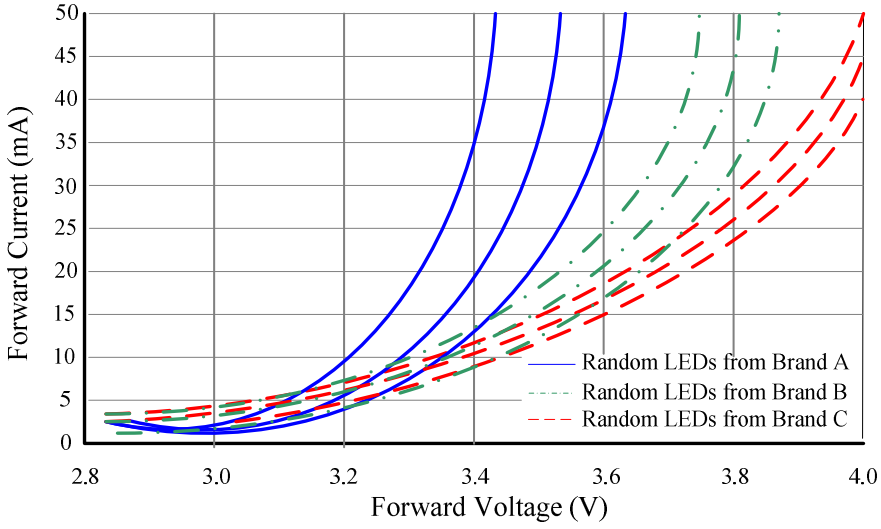


Fig. 2. I-V curve characteristic of LED

The most common method to drive LED current is shown in Fig. 3. A simple current regulator is implemented for LED strings. This circuit includes operational amplifier, a reference voltage, V_{REF}, and the external resistor, R_{EXT}. The LED current can be determined by the external resistor. It uses the constant-current source to regulate LED strings [6] [7]. The constant-current source eliminates LED current changes due to variations in forward voltage. The constant-current source produces the constant LED brightness and strings uniformly. In this configuration LEDs can be connected in series and parallel to keep an identical current flowing in each LED, due to the LED current I_{LED1}~ I_{LEDn} are produced by the value, V_{REF} /R_{EXT}. Therefore, if the external resistances are matched, this circuit can increase the current matching ability between channels.

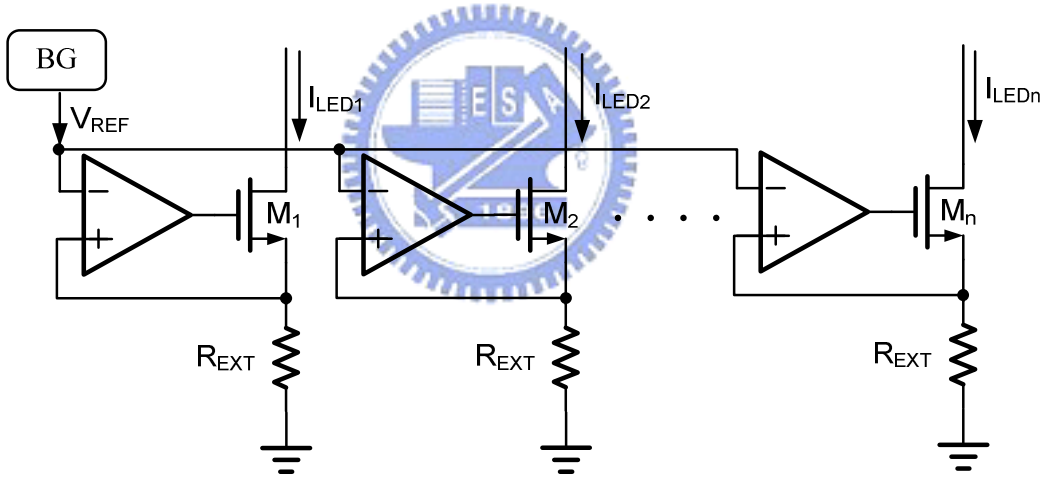


Fig. 3. A simplified current regulator for LED driver.

Another important issue is LED dimming control. LED dimming control is needed in many applications. In application of LCD backlighting, dimming provides brightness and contrast adjustment. In general, two types of dimming methods can be achieved, analog and pulse width modulation (PWM) [4]. In analog dimming, the changing of LED's forward current can change the brightness. For example, if an LED is at full brightness with 20 mA of forward current, then 50% of the brightness is achieved by applying 50% of the maximum current to the LED. However, the drawback with analog dimming is that changes in forward

current cause LED's color shift. This color shift may become unacceptable in displays requiring a true color representation. On the other hands, PWM dimming is achieved by applying full current to the LED at a modulated duty cycle. The LED brightness is controlled by adjusting the relative duty cycle. For example, 50% brightness level is achieved by turning the LED on time at full current for 50% of each period. The advantage of PWM dimming is that the forward current is always constant, so we just have to decide the maximum current for all the LED strings. Instead of analog dimming, by using this method, LED color does not vary with brightness. In order to keep the human eyes from seeing the LED turn on and off, the switching speed must be above 100 Hz. Therefore, the proposed method also includes the PWM dimming control circuit to maintain the benefits of PWM dimming. In order to eliminate the inrush current occurred at the instance of string turn on, we also proposed a delay method to reduce it. By using the delay method, the on time of all the strings will be split into several parts. In other words, turning on the strings gradually can reduce the charge current at the moment. The proposed circuit not only balances the current for LED strings but also is suitable for PWM dimming control.

1.3. Voltage Regulators Classifications

General power supply circuits can be classified into three kinds of regulator, such as linear regulators, switched capacitor circuits, and switching regulators. The technologies will be briefly introduced and described as following subsections. Furthermore, we will make a comparison for why we choose boost converter as the power supply unit of LED driver. The considerations of voltage regulators include low quiescent current consumption, low noise, high conversion efficiency, low cost, and so on.

1.3.1. Linear Regulator

The linear regulators use a pass element between input supply voltage and regulative

output voltage. The basic architecture of linear regulator is presented in Fig. 4 [8]. The low dropout voltage regulator provides a regulative voltage between input and output is about 100mv to 400mV. The linear regulator includes an error amplifier to reflect the output and input difference, a power MOSFET to supply the load current, and the resistive feedback network to sensing the output voltage variation. Due to the control circuit of LDO is the simplest one, so the chip size is smaller than other regulators. Furthermore, LDO circuit have no inductors, it can not only reduces the PCB space but also saves the cost.

Besides, it is more suitable to operate at the light-load condition than to operate in the heavy load. The other benefits of linear regulator are low noise and no output ripple. It's because that it just uses resistive feedback and error amplifier to build the feedback network but not switching signal based. In conclusion, the linear regulator can be used for analog and RF circuit application. The conversion ratio of the LDO is step-down only because of without storage element. The load ability becomes the direct ratio to the size of power MOSFET. Finally, the efficiency of LDO is proportional to output voltage, so the lower drop out voltage between input and output, the higher efficiency will be arrived.

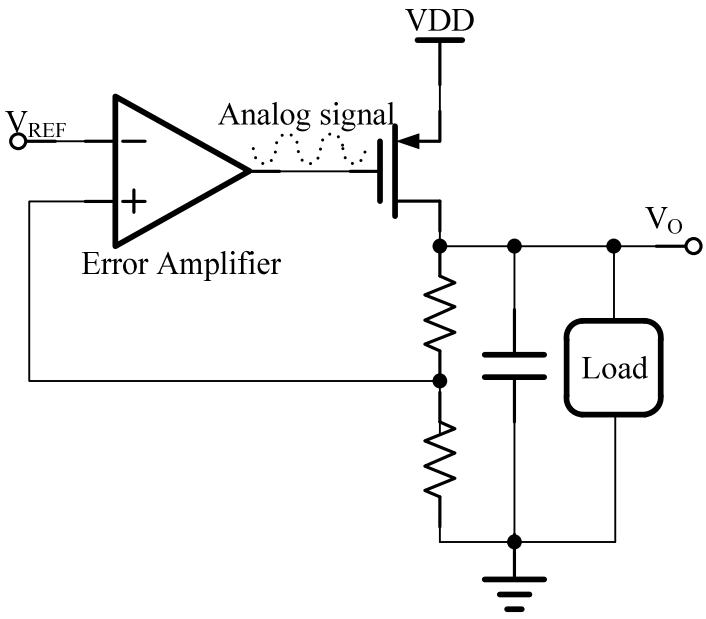


Fig. 4. The basic structure of linear regulator.

1.3.2. Switching capacitor Voltage regulator

The basic architecture of two-phase switching capacitor voltage doubler is shown in Fig. 5 [9]. The basic structure consists of capacitors and switches and it is also known as charge pump. The switching capacitor voltage doubler can generate a dc voltage higher or lower than the supply voltage or inverting voltage to the supply voltage. The operation principle is described briefly as follow: In the first interval of switching period, clock *CK1* is high and *CK2* is low. The switch, *SW1* and *SW2*, turning on and the switch, *SW3* and *SW4*, turning off. The capacitor, *C1* is being charged to the supply voltage *VDD*. In the second interval of switching period, clock *CK1* is low and *CK2* is high. The switch, *SW1* and *SW2*, turning off and the switch, *SW3* and *SW4*, turning on. The capacitor, *C1* is being charged to twice of the supply voltage *VDD*.

In order to maintain the output voltage, there are many ways to modulate the output voltage of the switched capacitor circuit to the desired value. To regulate the output voltage by a control circuit and an error amplifier is the most straightforward method. The error amplifier senses the variations of output voltage, and the control circuit controls switches, *SW1~SW4*, from the signal of error amplifier to regulate output voltage to the stable value.

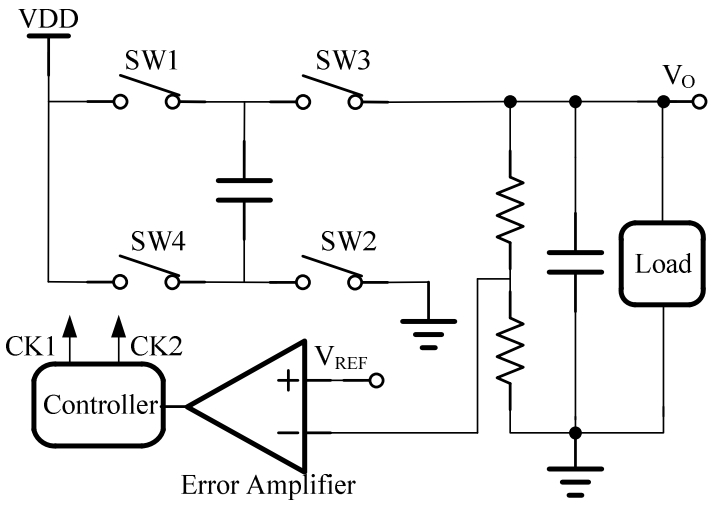


Fig. 5. The basic structure of switching capacitor voltage doubler

The efficiency of switching capacitor voltage regulator is poor at heavy load condition because the load ability depends on the output capacitor. As a result, the larger output capacitor can increase the load ability. However, when the output voltage is a multiple of input voltage, it will have the best efficiency above 90%.

1.3.3. Switching Regulator

The switching regulator includes the boost converter, the buck converter, and the buck-boost converter. The buck-boost converter combines the step-up mode and step-down mode. The conversion ratio of buck-boost converter is depending on the switching duty cycle. They are widely used in power supply design Fig. 6 [10] shows the basic architecture of switching regulator which is a boost converter. The switching regulator consists of power MOSFET, diode and resistor to feedback the output voltage variance. The error amplifier is utilized to reflect the output error and generate the error signal. The comparator is utilized to compare the error signal and the ramp signal to generate duty cycle depends on the error between output voltage and reference voltage. Therefore, controller will control the timing of switches. Driver is utilized to drive the huge power MOSFET so that it can regulate output voltage to expectative level.

The operation principle can be described as follow: In the first interval of switching period, the switch is closed and the input delivers the energy to the inductor. In the second interval of switching period, the switch is opened and the energy of the inductor delivers from the Schottky diode to output. By through this operation cycle by cycle, the circuit can provide the step-up voltage to the output. Besides, the output voltage is dominated by the reference voltage (V_{REF}) and the feedback resistances. The buck converter is achieved by changing the positions of the inductor, switch, and Schottky diode.

Because of the switching operation, noise and EMI are critical issues for the output voltage in switching regulator design. The efficiency of switching regulator is good in heavy

load, but poor in light load. The detail description of the switching regulator will be introduced in chapter 2.

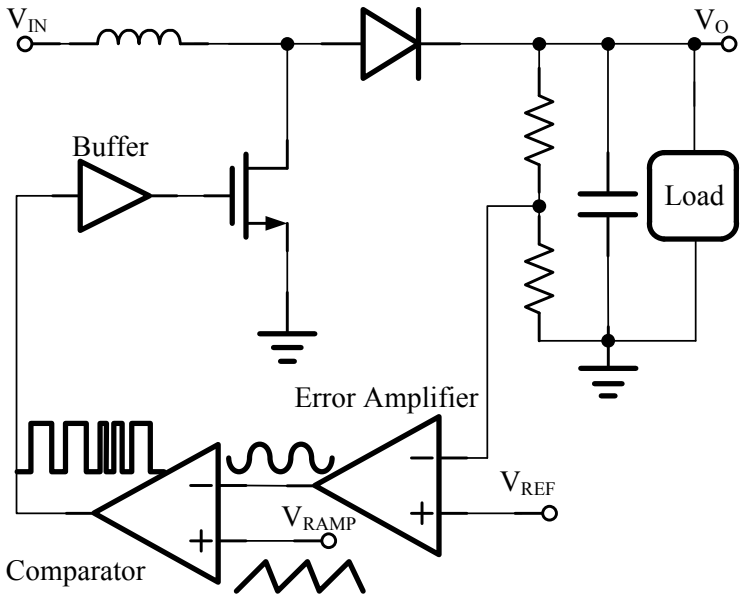


Fig. 6. The basic architecture of switching regulator.

1.3.4. Comparison of voltage regulators

In this section, we list the advantages and disadvantages of the three kinds of voltage regulator, shown in TABLE I [11].

TABLE I

Comparison of voltage regulators

	Linear regulator	**Switching capacitor Voltage regulator**	**Switching Regulator**
Regulation Mode	Buck	Buck/Boost/Inverter	Buck/Boost/Buck-Boost/ Inverter
Cost	Low	Medium	Highest
Complexity	Low	Medium	Highest
Output ripple	Lowest	Medium	Medium
Footprint area	smallest	Medium	largest
Load ability	Medium	Low	Highest
Efficiency	Low	Medium	Highest

According to the table, we can realize that not only charge pump but also boost converter can boost the input voltage to higher than output voltage. However, in the application of high

brightness and large number LED driver, high power characteristics should be concerned. Based on the consideration of the higher efficiency, smaller power consumption, wilder output range for more LEDs in series and stronger loading capacity for more strings connect in parallel. Boost converter is more suitable than charge pump to be a power supply in LED backlight application.

1.4. Motivation

Due to the advances in the technology of LED, the benefits for LED backlight has become evidently. Therefore, this thesis is focus on the entire LED driving circuit for high brightness LED or R, G, B LED backlight system.

For LED backlight in LCD TV application, LED driving circuit have two topics. Firstly, boost converter is to offer sufficient voltage to overcome the LED forward voltage. And offer a high load current ability, high efficiency for the LEDs in series and parallel. Secondly, current regulator is to regulate the current flow through each LED string and have PWM dimming circuit to adjust the illumination through averaging the driving current. This thesis proposes a new kind of LED driver to fit the application of LED backlight system.

1.5. Thesis Organization

This thesis is organized as follows. The basic current mode DC-DC converter is introduced in Chapter 2. The design and implementation for proposed LED driver are described in chapter 3. Chapter 4 shows the system implementations and simulation results based on the proposed technique. Finally, the conclusions and future works are presented in Chapter 5.

Chapter 2

Basic concepts of Switching Regulator

2.1. Basic Switching Regulator Topologies

The basic topology [10] and modulation technology of switching regulators will be introduced in this section. There are three basic switching regulators as shown in Fig. 7 to Fig. 9. They are the buck, boost, and buck-boost converter respectively. These converters consist of storage element, such as inductor and capacitor to store and deliver energy to regulate the output voltage. The power MOSFET is controlled by the control signal and the duty ratio is depends on the error between output voltage and reference voltage.

The fundamental operations of the three kinds of regulator are described as follow. In Fig.7, it shows the basic structure of a buck converter. The buck converter can generate output voltage smaller than its' input voltage. Due to the property of conversion ratio it is also called a step down converter.

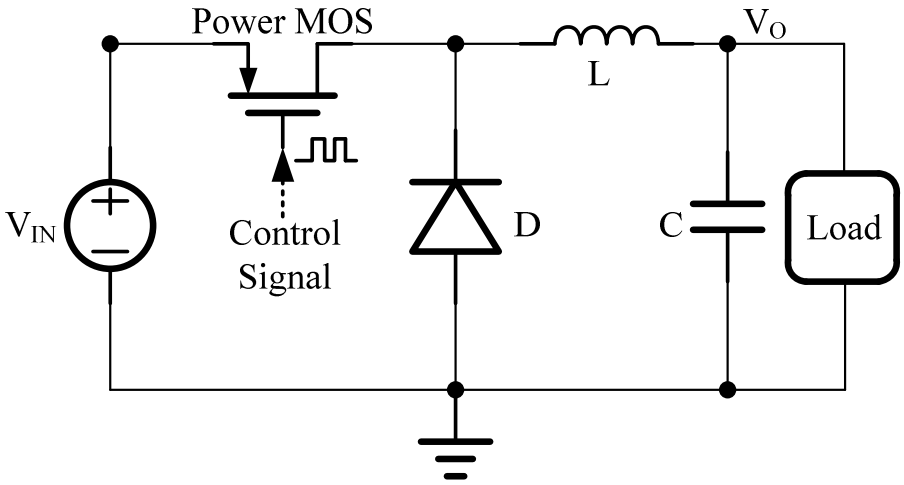


Fig. 7. The basic structure of buck converter

Fig. 8 shows the basic structure of a boost converter. The boost converter can generate output voltage larger than its' input voltage. Due to the property of conversion ratio it is also

called a step up converter.

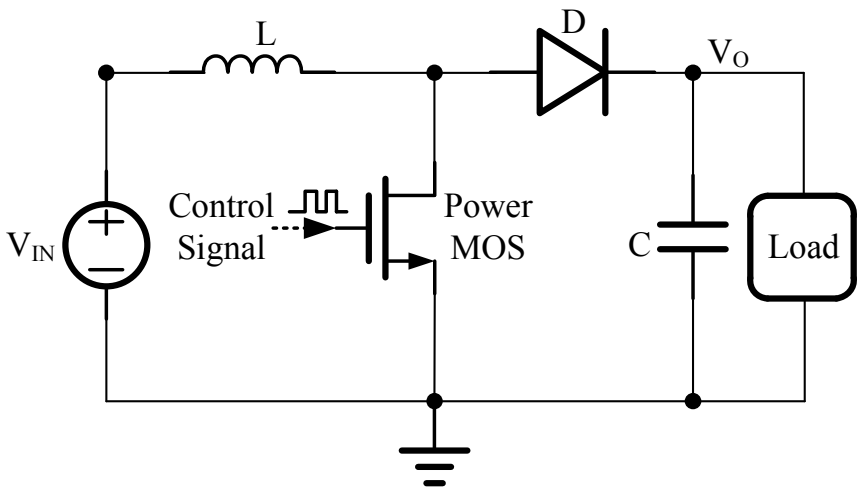


Fig. 8. The basic structure of boost converter.

Fig. 9 shows the basic structure of a buck-boost converter. The buck-boost converter has both the characteristic of buck and boost converter. Thus, it is also called a step up-down converter.

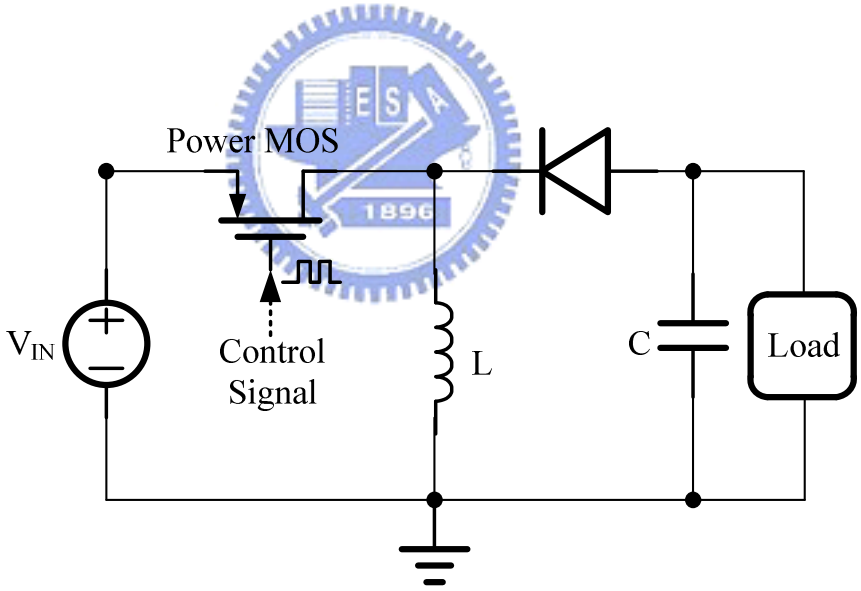


Fig. 9. The basic structure of buck-boost converter.

2.2. Modulation Technologies

There are two mainly kinds of modulation technologies in switching regulator. Firstly, PWM (Pulse Width Modulation) modulates the switching signal by a fixed switching frequency. Secondly, PFM (Pulse Frequency Modulation) uses a hysteretsis window to generate a switching signal. Both of the technologies modulate the on and off time of switches

to control the energy transfer to output.

2.2.1. Pulse Width Modulation (PWM)

In PWM control, the switching regulators are regulated by PWM signal with a constant switching frequency as shown in Fig. 10 [10]. The duty ratio is decided according to the control signal and ramp signal. When the ramp signal is smaller than the control signal, PWM signal is high and vice versa. Therefore, the duty ratio of PWM signal depends on the trend of the control voltage and regulates the output voltage to the expectative level. However, PWM modulation has poor light-load efficiencies because of higher switching losses.

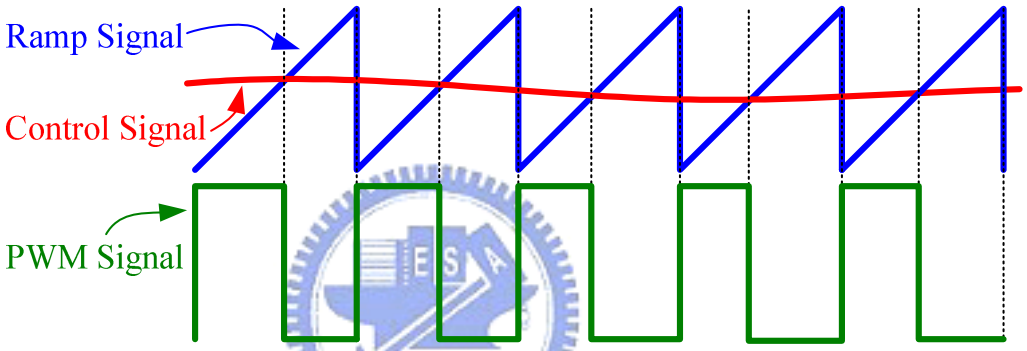


Fig. 10. Pulse-width modulation Signal.

2.2.2. Pulse Frequency Modulation (PFM)

In PFM control, it is uses a hystersis window to generate the switching signal as shown in Fig. 11 [12]. In other words, it controls the switch of switching regulator by an alternative frequency. In Fig. 11 the PFM signal will be generated when the output voltage is smaller than lower threshold voltage of the hystersis window. The PFM signals are strings of pulse with fixed frequency to regulate the output voltage. The PFM pulse will stop when the output voltage reaches to the upper threshold of hystersis window. By using this modulation technology, there is more efficient at light loads because the switching frequency and associated switching losses are scaled down with load current.

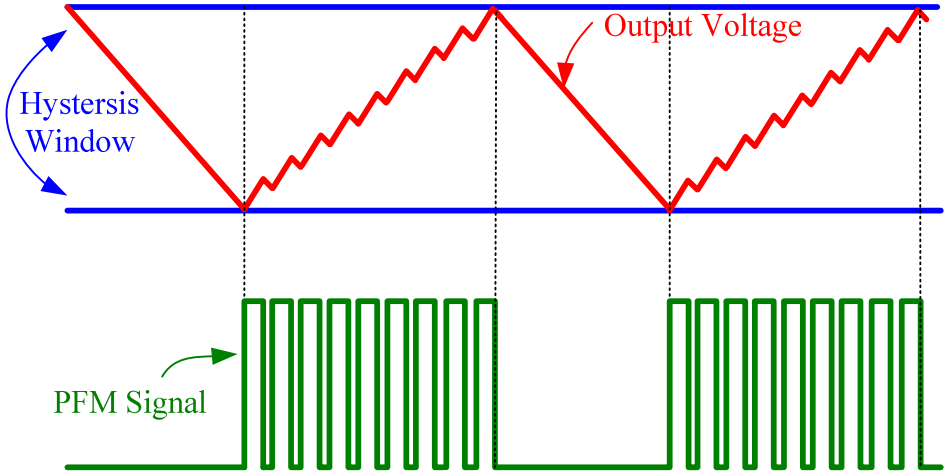


Fig. 11. Pulse-frequency modulation Signal.

2.3. Analysis of current mode Boost Switching regulator

In current mode control technique the output voltage of converter is not only controlled by the voltage feedback loop but also the peak transistor switch current. The duty cycle of power transistor is controlled by voltage loop, inductor current of converter, capacitor voltages and power input voltage.

2.3.1. The Operation Theorem of Current Mode Control

The block diagram of current mode boost converter is shown in Fig. 12. There are two operation modes for switching converter, which are voltage mode and current mode.

In voltage mode controlling, the converter only uses a voltage feedback loop to regulate the output voltage. The duty ratio of pulse-width modulation is produced by output signal of error amplifier and the original ramp signal.

In current mode controlling, it includes both voltage and current loop. The advantages of current mode are simpler dynamics and wide-bandwidth. The inductor and capacitor of power stage offer only one low frequency pole. Otherwise, current mode control should use the current sensing information during the normal operation to obtain simpler dynamics.

In Fig. 12 the PWM signal is generated by clock generator with a pulse of small duty ratio. The output of the SR latch should be set to high when the output signal of clock generator is high. In this state, the power MOSFET is turned on and diode off. The inductor current increases with a positive slope which depends on the input voltage and the value of inductor. The artificial ramp is added to the current sensing signal to avoid unstable problem when duty ratio is larger than 0.5. The error signal, the sum of ramp and current sensing are compared by the analog comparator. When the sum of ramp and current sensing is larger than error signal, the output of comparator is high to reset the SR latch. Besides, it can turn off the power MOSFET. Therefore, the duty cycle of power MOSFET is controlled by feedback voltage and inductor current.

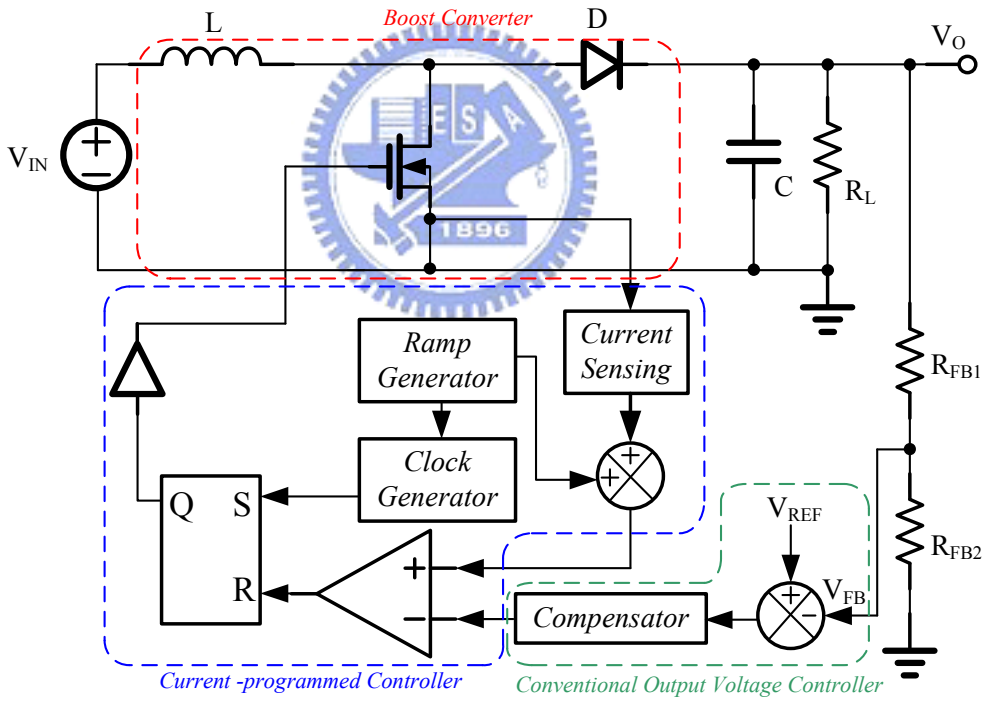


Fig. 12. Diagram of current mode boost converter.

2.3.2. Oscillation for D>0.5

The current mode controller is unstable when the steady-state duty cycle is larger than 0.5. The reasons of oscillation caused by D>0.5 is described as follow.

In current mode controlling, the inductor current changes with the rising and falling slopes for boost converter are as:

$$m_1 = \frac{V_{in}}{L}, -m_2 = \frac{V_{in} - V_{out}}{L} \tag{1}$$

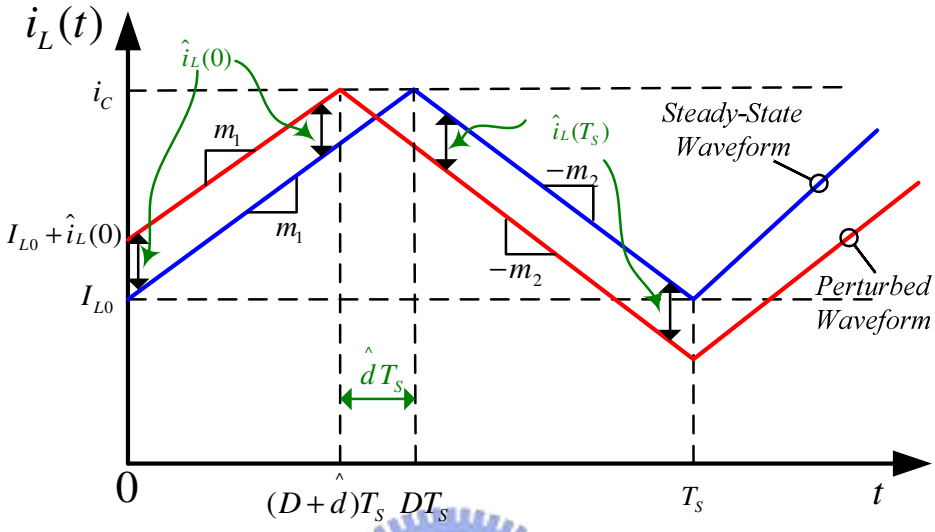


Fig. 13. Perturbed inductor current waveform

Fig. 13 [10] [13] shows the inductor current waveform without artificial ramp compensation in steady-state. The value $\hat{i}_L(0)$ is the perturbation inductor current. From Fig. 14 we can use the slop and interval length to derive $\hat{i}_L(0)$ and $\hat{i}_L(T_S)$. The value of $\hat{i}_L(0)$ and $\hat{i}_L(T_S)$ is shown in equation (2) and (3) respectively.

$$\hat{i}_L(0) = -m_1 \hat{d} T_S \tag{2}$$

$$\hat{i}_L(T_S) = m_2 \hat{d} T_S \tag{3}$$

In order to realize the relationship between slope and duty ratio, we consider the steady state inductor current without perturbing in first and second intervals. In first interval the inductor current is shown as equation (4).

$$i_L(dT_S) = i_C = i_L(0) + m_1 dT_S \tag{4}$$

When it operates in the second interval, inductor current is shown in equation (5).

$$i_L(T_S) = i_L(dT_S) - m_2 d'T_S = [i_L(0) + m_1 dT_S] - m_2 d'T_S \tag{5}$$

Because of $i_L(0) = i_L(T_S)$, $d = D$, $m_1 = M_1$, and $m_2 = M_2$ in steady state, the relationship between slope and duty ratio can be derived as equation (6).

$$0 = M_1 DT_S - M_2 D'T_S, \ \frac{M_2}{M_1} = \frac{D}{D'} \tag{6}$$

By combining equation (2), (3) and (6) the change in inductor current perturbation over one switching period can be obtained in equation (7).

$$\hat{i}_L(T_S) = \hat{i}_L(0)\left(-\frac{D}{D'}\right) \tag{7}$$

By the same analysis the changes in inductor current perturbation over two switching period can be derived.

$$\hat{i}_L(2T_S) = \hat{i}_L(T_S)\left(-\frac{D}{D'}\right) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^2 \tag{8}$$

Therefore, the perturbation becomes as equation (9) after n switching period.

$$\hat{i}_L(nT_S) = \hat{i}_L((n-1)T_S)\left(-\frac{D}{D'}\right) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^n \tag{9}$$

In equation (9), the inductor current magnitude is tending down over several switching period when the duty cycle is smaller than 0.5. The inductor current is stable in this condition. Reversely, instability occurs when duty cycle is larger than 0.5. In briefly, in order to let the perturbation $\hat{i}_L(nT_S)$ tends to zero, the value of –D/D' should has magnitude less than one or D<0.5. Reversely, the perturbation $\hat{i}_L(nT_S)$ becomes large as the magnitude of the value –D/D' has larger than one or D>0.5. Therefore, we can derive the equation as (10) and (11).

$$\left|\hat{i}_L(nT_S)\right| \to 0,\ when \left|-\frac{D}{D'}\right| < 1 \tag{10}$$

$$\left|\hat{i}_L(nT_S)\right| \to \infty,\ when \left|-\frac{D}{D'}\right| > 1 \tag{11}$$

The inductor current waveform in stable and unstable situation without compensation ramp is shown in Fig. 14. Therefore, current mode controller adds an artificial ramp and inductor current to avoid the unstable problem.

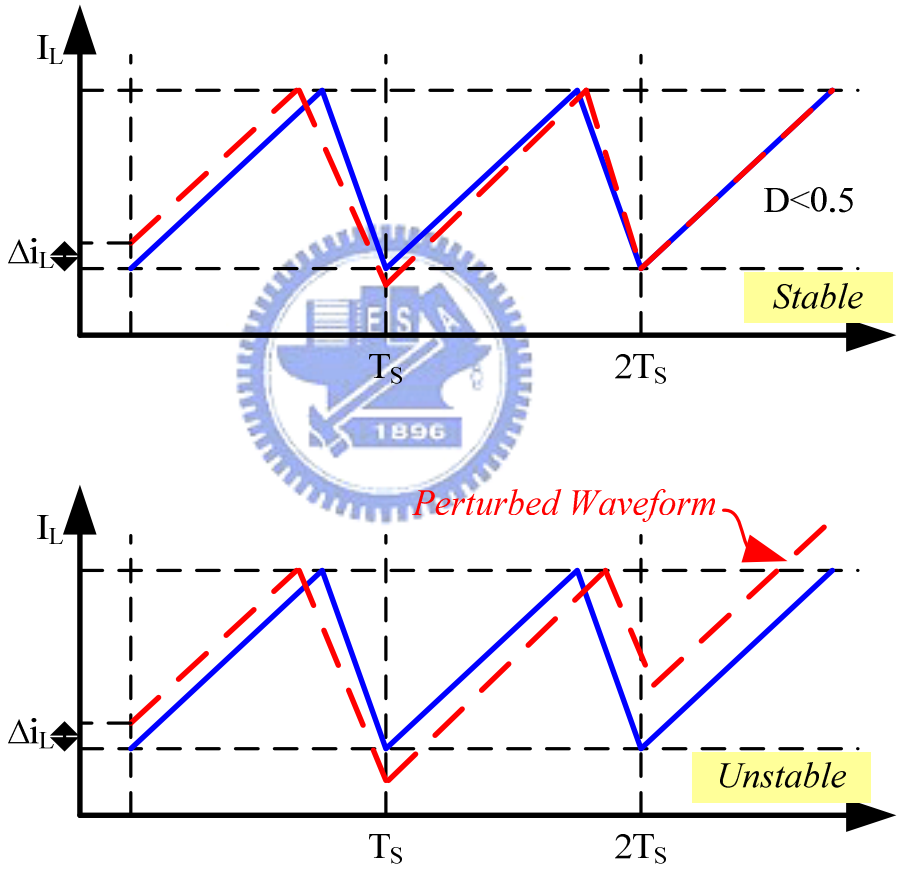


Fig. 14. Inductor waveform in stable and unstable situation without compensation ramp.

2.3.3. Ramp Compensation

The sub-harmonic oscillation is a well-known problem of current-mode converter. It is independent on the converter topology. In Fig. 15 [10] [14], the artificial ramp generator is

added to the switching current sensing loop to avoid unstable oscillation. The compensated ramp can reduce the gain of the inner current sensing loop to prevent the oscillation problem of the current mode converter.

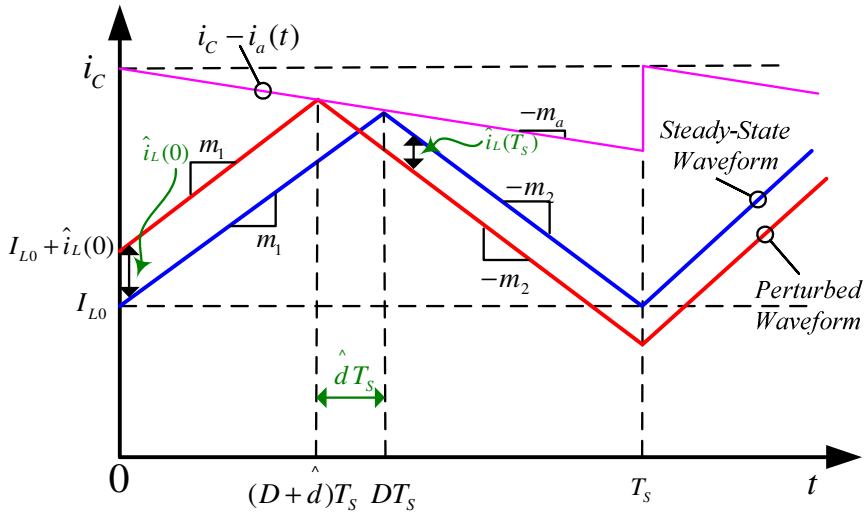


Fig. 15. Perturbed inductor current waveform with ramp compensation

From Fig. 15, the perturbations $\hat{i}_L(0)$ and $\hat{i}_L(T_S)$ can be derived as equation (12) and (13).

$$\hat{i}_L(0) = -m_1 \hat{d} T_S - m_a \hat{d} T_S \tag{12}$$

$$\hat{i}_L(T_S) = -m_2 \hat{d} T_S + m_a \hat{d} T_S \tag{13}$$

By combining equation (12) and (13) the change in inductor current perturbation over one switching period with ramp compensation can be obtained in equation (14).

$$\hat{i}_L(T_S) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) \tag{14}$$

From equation (14), the change in inductor current perturbation over several switching periods as:

$$\hat{i}_L(nT_S) = ((n-1)T_S)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n = \hat{i}_L(0)\alpha^n \tag{15}$$

In equation (15), when the value n trends to infinite the perturbation $\hat{i}_L(T_S)$ becomes to zero just as the characteristic value α has magnitude less than one. Reversely, the perturbation $\hat{i}_L(T_S)$ becomes infinite when the characteristic value α has magnitude greater than one. Therefore, we can derive the equation as (16).

$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a},\ \left|\hat{i}_L(nT_S)\right| \rightarrow \begin{cases} 0 & when\ |\alpha| < 1 \\ \infty & when\ |\alpha| > 1 \end{cases} \tag{16}$$

Thus, the common choice of the slope m_a of compensation ramp is as shown in equation (17). Furthermore, the slope of compensation ramp should be larger than the slope of second subinterval period, as shown in equation (18). By the condition of equation (18) can make $\hat{i}_L(T_S)$ trends to zero for any $\hat{i}_L(0)$. It also lets current-mode controlled DC-DC boost converter stable for all possible duty cycle.

$$m_a = \frac{1}{2} m_2 \tag{17}$$

$$m_a \geq \frac{1}{2} m_2 \tag{18}$$

2.3.4. Continuous Conduction Mode (CCM)

In the CCM operation the inductor current has a minimum level above zero and operates continuously. Therefore, there are only two subintervals for switching converter in CCM operation [10]. The two equivalent circuits of first and second subintervals are as shown in Fig. 16.

Fig. 16 (a) shows the first subinterval operation in CCM. When converter operating in first subinterval the low side NMOS turns on and inductor current increasing. During this subinterval the inductor voltage and capacitor current can be derived as equation (19) and (20).

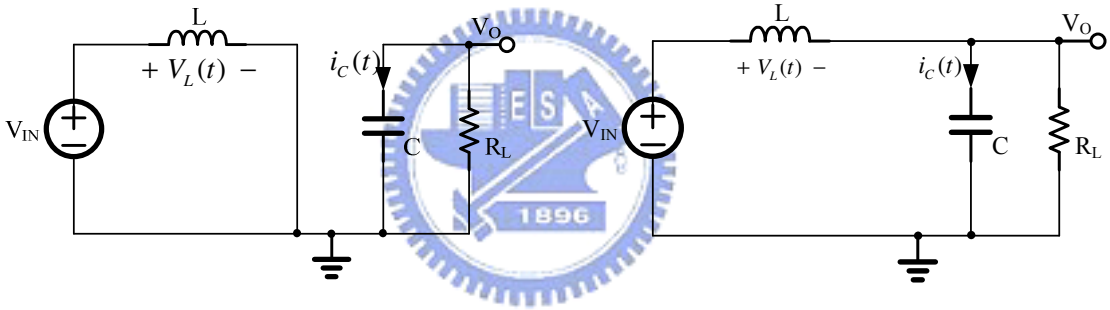
$$v_L(t) = L\frac{di_L}{dt} = V_{in} \tag{19}$$

$$i_C(t) = C\frac{dv_C}{dt} = \frac{-V_{out}}{R} \tag{20}$$

Fig. 16 (b) shows the second subinterval operation in CCM. When converter operates in first subinterval the high side PMOS turns on and inductor current delivering to output. During this subinterval the inductor voltage and capacitor current can be derived as equation (21) and (22).

$$v_L(t) = L\frac{di_L}{dt} = V_{in} - V_{out} \tag{21}$$

$$i_C(t) = C\frac{dv_C}{dt} = i_L - \frac{V_{out}}{R} \tag{22}$$



(a) (b)

Fig. 16. (a) Equivalent circuits of the first subinterval in CCM. (b) Equivalent circuits of the second subinterval in CCM

By inductor voltage second balance, equation (23) can be derived. The output voltage increases when D rises. In the ideal case, the conversion ratio tends to infinity when D trends to 1.

$$V_{in}\cdot DT_s + (V_{in} - V_{out})\cdot(1-D)T_s = 0\ ,\quad \frac{V_{out}}{V_{in}} = \frac{1}{D'} = \frac{1}{1-D} \tag{23}$$

By capacitor charge balance, the steady-state current in the switching converter can be calculated as shown in equation (24).

$$\left(\frac{-V_{out}}{R}\right)\cdot DT_S+\left(i_L-\frac{V_{out}}{R}\right)(1-D)\cdot T_S=0\ ,\quad i_L=\frac{V_{out}}{D'R}=\frac{V_{in}}{D'^2R} \tag{24}$$

The inductor current in equation (24) is equal to the input current of converter. Its' magnitude is greater than the load current. By combining the equation (19) and (20) the inductor current ripple and output voltage ripple can be calculated as equation (25) and (26) respectively:

$$\Delta i_L=\frac{V_{in}}{2L}\cdot DT_S \tag{25}$$

$$\Delta v=\frac{V}{2RC}\cdot DT_S \tag{26}$$

2.3.5. Discontinuous Conduction Mode (DCM)

In the DCM operation, the inductor current has a minimum level equal to zero. Therefore, the operation region will be defined as three subintervals for switching converter in DCM operation [10]. However, the first and second subinterval are as the same as CCM operation. Thus, the equivalent circuit in Fig. 17 has just shows the third subinterval. In the third subinterval the power MOSFET and diode are both turn off, the energy store in output capacitor to discharge to load. Owing to the three subintervals in the DCM operation, one switching cycle has divided into three parts, D_1T_S, D_2T_S and D_3T_S. The operation waveform of boost converter is shown in Fig. 18.

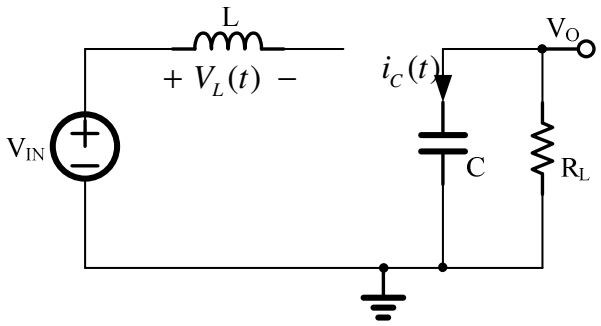


Fig. 17. Equivalent circuits of the third subinterval in DCM

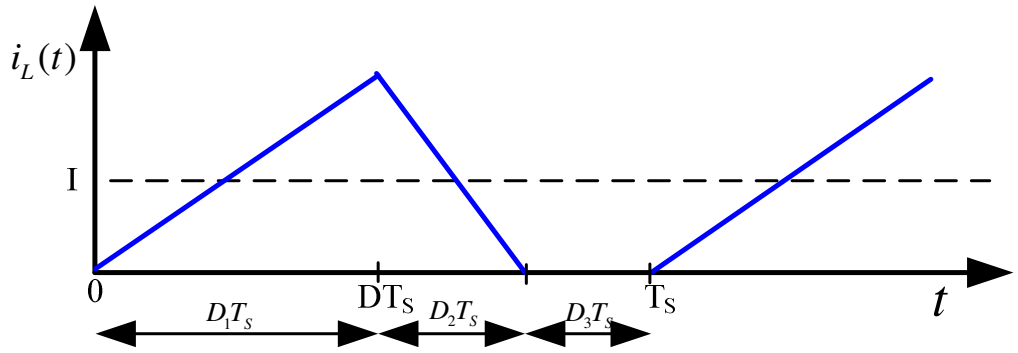


Fig. 18. Operation waveform of boost converter in DCM.

In the DCM operation, the inductor voltage, capacitor current of first and second subintervals are the same as equation (19) (20) (21) (22). The relative equations of the third subinterval are shown in equation (27) and (28).

$$v_L = 0 \tag{27}$$

$$i_C = -\frac{V_{out}}{R},\ i_L = 0 \tag{28}$$

By inductor voltage second balance, equation (29) can be derived. The conversion ratio is relative to the duty ratio of the first and second subintervals.

$$V_{in} \cdot D_1T_s + (V_{in} - V_{out}) \cdot D_2T_s + 0 \cdot D_3T_S = 0\ ,\ \frac{V_{out}}{V_{in}} = \frac{D_1 + D_2}{D_2} \tag{29}$$

By capacitor charge balance, the steady-state current in the switching converter can be calculated as shown in equation (30).

$$I_{out} = \frac{V}{R} = \frac{1}{T_S} \cdot \left[\frac{1}{2} \left(\frac{V_{in}}{L} D_1T_S \right) \cdot D_2T_S \right] = \frac{V_{in}D_1D_2T_S}{2L} \tag{30}$$

By replacing equation (29) into (30) the output voltage can be obtained as:

$$\frac{V_{out}}{V_{in}} = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2}\ ,\ where\ K = \frac{2 \cdot L}{RT_S} \tag{31}$$

As mentioned in 2.3.4 the conversion ratio in CCM operation only depends on input

voltage and duty cycle. However, in DCM operation the voltage conversion ratio depends on the inductor, load resistance, switching frequency and input voltage.

2.3.6. Current Mode Controller Model

In order to have accurate model of current mode controller for DC-DC converter, the analysis is combined with the controller small signal model [15] [16] [17] [18]. For CCM operation, the relationship between control signal and inductor current are illustrated in Fig. 19, where m_1 and m_2 are the slope of inductor current, m_a is the slope of compensation ramp.

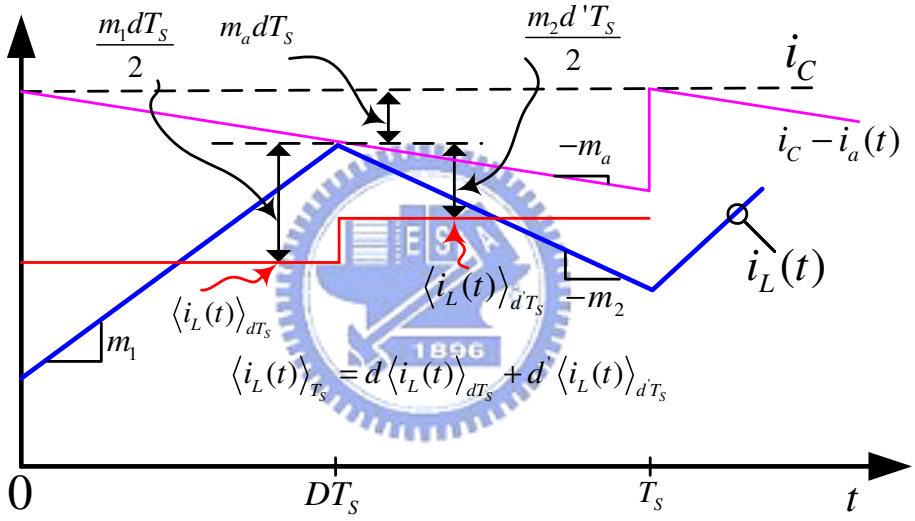


Fig. 19. The relationship between the average inductor current and control voltage

From Fig. 19 the average inductor current can be expressed as equation (32)

$$\left\langle i_L(t)\right\rangle_{T_S} = \left\langle i_C(t)\right\rangle_{T_S} - m_a dT_S - m_1 \frac{d^2 T_S}{2} - m_2 \frac{(d')^2 T_S}{2} \tag{32}$$

Where the slope m_1 and m_2 are shown in equation (33)

$$\hat{m}_1 = \frac{\hat{V}_{in}}{L}, \hat{m}_2 = \frac{\hat{V}_{out} - \hat{V}_{in}}{L} \tag{33}$$

Therefore, solution for $\hat{d}(t)$ yields:

$$\hat{d}(t)=\frac{1}{M_a T_s}\left[\hat{i}_C(t)-\hat{i}_L(t)-\left[\frac{2D-1}{2L}T_S\right]\hat{v}_{in}(t)-\left[\frac{D'^2 T_S}{2L}\right]\hat{v}(t)\right] \tag{34}$$

Finally, to make $\hat{d}(t)$ as a function of $\hat{i}_C(t), \hat{i}_L(t), \hat{v}_{in}(t)$ and $\hat{v}(t)$, equation (34) can be rewritten as equation (35). Where the parameters F_m, F_g, F_v are as the function in equation (36).

$$\hat{d}(t)=F_m\left[\hat{i}_C(t)-\hat{i}_L(t)-F_g\hat{v}_{in}(t)-F_v\hat{v}(t)\right] \tag{35}$$

$$F_m=\frac{1}{M_a T_s}, F_g=\frac{2D-1}{2L}T_S, F_v=\frac{D'^2 T_S}{2L} \tag{36}$$

By combining the controller block and power stage small signal model the model of current mode dc-dc boost converter can be obtained, as shown in Fig. 19.

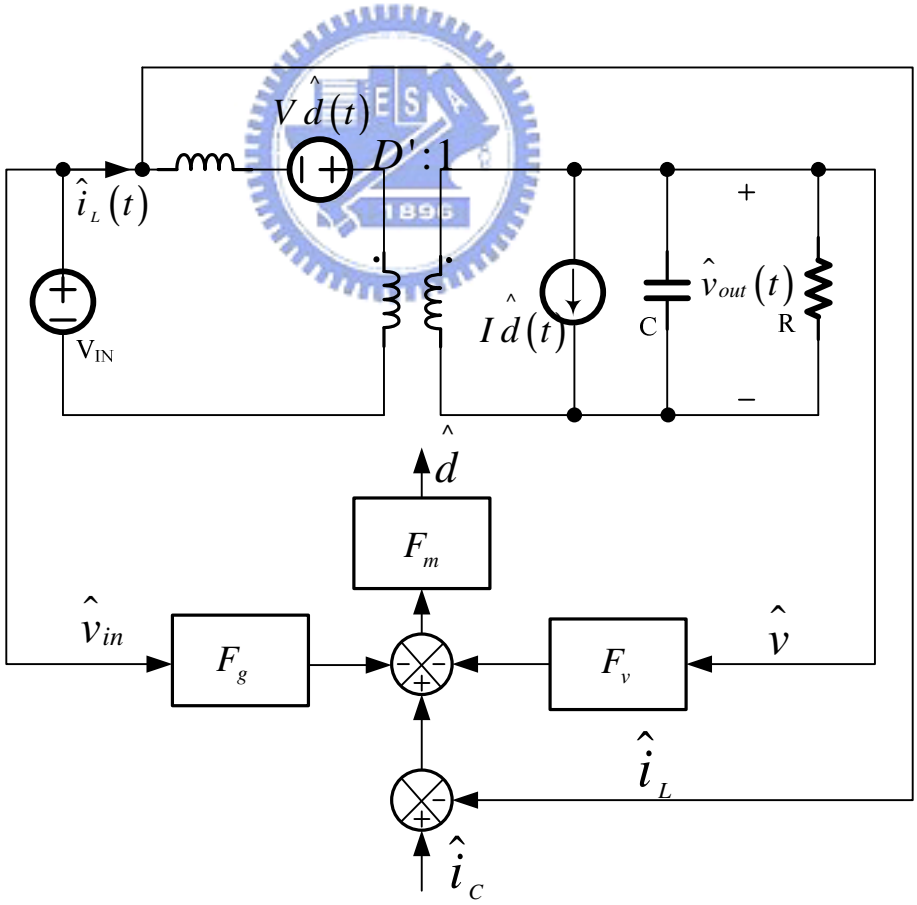


Fig. 20. Small signal model of current mode dc-dc boost converter

From Fig. 20 the transfer function of current mode dc-dc boost converter can be derived as follow. The control-to-output and line-to-output transfer functions are shown in equation (37) (41), respectively.

Control-to-output transfer function:

$$G_{vc} = \frac{\hat{v}_{out}}{\hat{i}_c} = G_{c0} \frac{\left(1 - s\frac{L}{(D')^2 R}\right)}{1 + s(\frac{1}{Q_C \omega_C}) + s^2(\frac{1}{\omega_C})^2} \tag{37}$$

Where

$$G_{c0} = \frac{V_{out}}{D'} \frac{F_m}{1 + \frac{2F_m V_{out}}{(D')^2 R} + \frac{F_m F_v V_{out}}{D'}} \tag{38}$$

$$\omega_C = \frac{D'}{\sqrt{LC}} \sqrt{1 + \frac{2F_m V_{out}}{(D')^2 R} + \frac{F_m F_v V_{out}}{D'}} \tag{39}$$

$$Q_C = RD' \sqrt{\frac{C}{L}} \frac{\sqrt{1 + \frac{2F_m V_{out}}{D'^2 R} + \frac{F_m F_v V_{out}}{D'}}}{\left(1 + RC\frac{F_m V_{out}}{L} - \frac{F_m F_v V_{out}}{D'}\right)} \tag{40}$$

Line-to-output transfer function:

$$G_{vg} = \frac{\hat{v}_{out}}{\hat{v}_{in}} = G_{c0} \frac{\left(1 + \frac{s}{\omega_{gz}}\right)}{1 + s\left(\frac{1}{Q_C \omega_C}\right) + s^2\left(\frac{1}{\omega_C}\right)^2} \tag{41}$$

Where

$$G_{c0} = \frac{1 - F_m F_g V_{out} + \frac{F_m V_{out}}{(D')^2 R}}{D'} \frac{}{1 + \frac{2F_m V_{out}}{(D')^2 R} + \frac{F_m F_v V_{out}}{D'}} \tag{42}$$

$$\omega_C = \frac{D'}{\sqrt{LC}} \sqrt{1 + \frac{2F_m V_{out}}{(D')^2 R} + \frac{F_m F_v V_{out}}{D'}} \tag{43}$$

$$\omega_{gz} = \frac{(D')^3 R}{L} \frac{\left(1 - F_m F_g V_{out} + \frac{F_m V_{out}}{(D')^2 R}\right)}{F_m F_g V_{out}} \tag{44}$$

$$Q_C = D' R \sqrt{\frac{C}{L}} \frac{\sqrt{1 + \frac{2F_m V_{out}}{(D')^2 R} + \frac{F_m F_v V_{out}}{D'}}}{\left(1 + RC\frac{F_m V_{out}}{L} - \frac{F_m F_v V_{out}}{D'}\right)} \tag{45}$$

Based on the above analytic the current mode dc-dc boost converter can be constructed and designed.

2.4. Compensator Design for DC-DC Converter

In general, the feedback loop of converter always comprises error amplifier. However, the error amplifier without compensating causes the stability problem to make this system unstable. In order to solve the stability problem, a compensator for current mode boost converter is needed. Therefore, a pole zero cancellation technique is used. The compensation network comprises one resistance and one capacitor to generate one pole and one zero [10] [19].

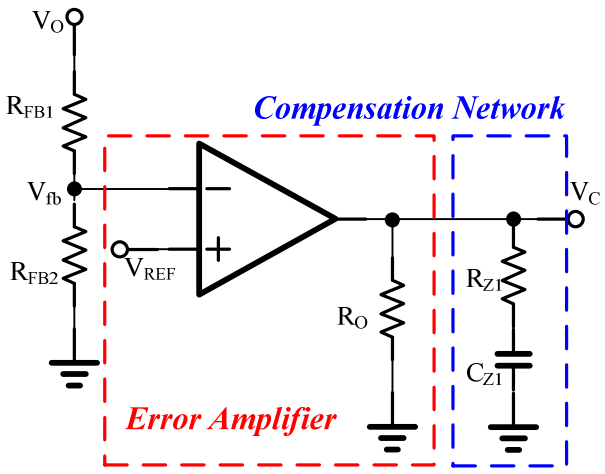


Fig. 21.The compensator of current dc-dc converter

The compensation theorem is as follow. The relationship between feedback signal V_{fb} and error amplifier output V_C of transfer function is shown as equation (46)

$$\frac{V_O}{V_{fb}} = g_m \cdot [R_O // (R_{Z1} + \frac{1}{sC_{Z1}})] = g_m \cdot R_O \cdot \frac{(1 + s \cdot C_{Z1} \cdot R_{Z1})}{(1 + s \cdot C_{Z1} \cdot R_O)} \quad ,if \ R_O >> R_{Z1} \tag{46}$$

Where g_m is the transconductance and *Ro* is the output resistance of the error amplifier. Therefore, the pole and zero contributed by the compensation network are as follow.

$$zero : s_Z = \frac{1}{C_{Z1} \cdot R_{Z1}}, \ \ pole : s_p = \frac{1}{C_{Z1} \cdot R_O} \tag{47}$$

In this kind of compensation technique the pole which is smaller than the system pole and becomes the dominate pole to make sure the stability of the system. Furthermore, the unit gain frequency of the loop is determined by the compensation resistance. Thus, the frequency response of the system can be improved by choosing an optimal compensation resistance.

Chapter 3

LED Driver with Current Mode DC-DC Converter

3.1. The Proposed LED Driver with Current-Mode Boost Converter

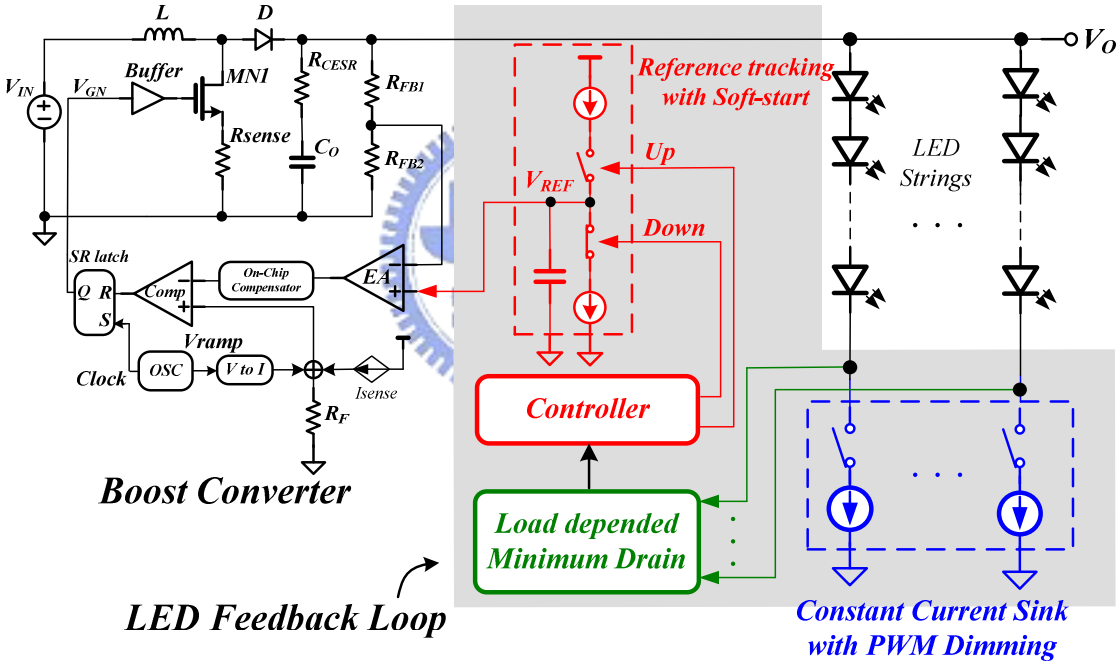


Fig. 22.The proposed LED driver with current-mode boost converter

Fig. 22 illustrates the proposed LED driving circuit with current-mode dc-dc boost converter which can drive up to 11x6 white LEDs. This white LED array has 6 chains which consists of 11 series LEDs. Besides, it has six precision current sink channels, up to 30mA per channel. The driving circuit includes four parts as shown in Fig. 22. There are current-mode boost converter, reference tracking circuit, PWM dimming with constant current sink and load

dependent minimum drain circuit.

The power stage includes an internal power NMOS to charge a 10μH inductor L and the inductor current is discharged by an external Schottky diode to a 4.7μH filtering capacitor, C. The internal resistor R_{sense} is utilized to sense the inductor current by current sensing technique. The feedback resistances R_{FB1} and R_{FB2} are utilized to scale down the output voltage to compare with the reference voltage V_{REF} before feeding into the comparator. Then the comparator compares the output signal of error amplifier and sums up ramp signal and current sensing signal. The output signal of comparator is utilized to decide the duty cycle of the PWM signal.

3.1.1. The Design Theorem

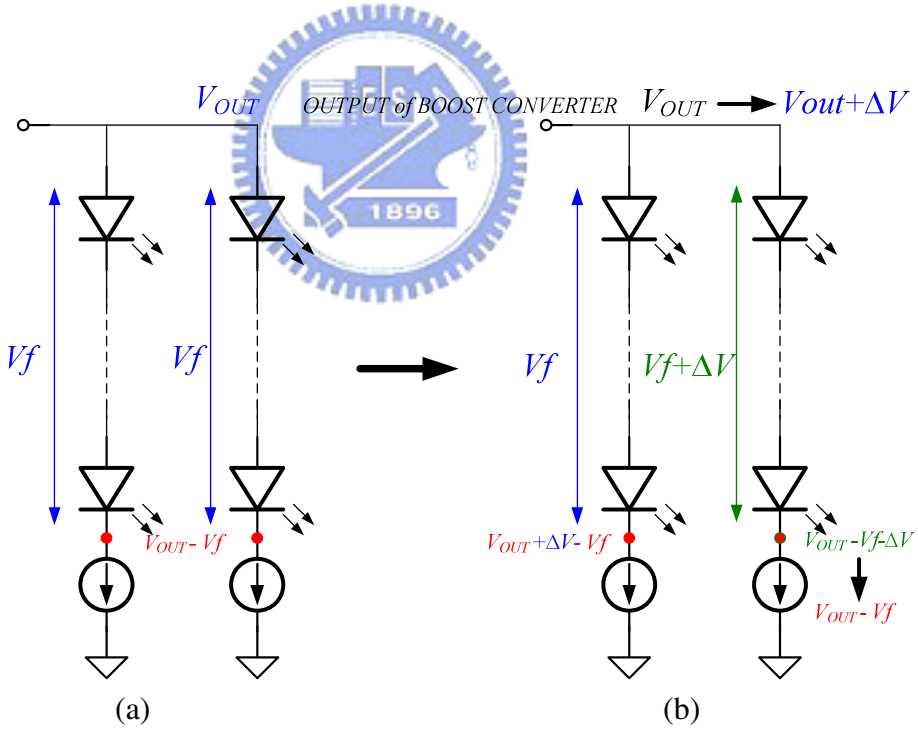


Fig. 23. (a) Case I: Two LED strings having the same forward voltage. (b) Case II: Two LED strings having different forward voltage.

The most important issue in design of a LED driving circuit is forward voltage variation, which will be unreliable when temperature and time vary. Although we can choose similar

LED of forward voltage manually, the cost is too expensive. Moreover, in order to get sufficient luminance, the backlight requires many LEDs to be connected in series and needs a constant current supply to maintain stable light illumination [20] [21] [22]. Therefore, to supply a sufficient voltage lager than the forward voltage of LEDs is needed and important. Fig. 23 shows two different cases of forward voltage. In Fig. 23 (a), if the forward voltages of two LED strings are the same and sufficient high, the output voltage level of boost converter is enough equals to *Vout*. Consider the forward voltage of one of the strings increases ΔV when the other stays in constant. If the output voltage of boost converter still maintain at *Vout* and the head room of constant current sink might be compressed. Therefore, the output voltage of boost converter should be rose up equal to the variation on the forward voltage of LEDs. In other words, if forward voltage of LED increases the amount of ΔV, the output of boost converter should also raise the amount of ΔV. Therefore, the constant current sink circuit has the head room equal to *Vout* –*Vf* as the forward voltage of LEDs changing before.

By the analysis above, a LED driver should have a feedback loop according to the head room of constant current sink circuit to regulate the output voltage to a sufficient level.

Although the higher head room can contribute a more accurate current for LEDs, it will cause dispensable power dissipation. Therefore, the head room of the constant current sink circuit should be keep at the minimum value to prevent unnecessary power loss on it.

The detail description will be introduced in following sections.

3.1.2. Operation Principle of Soft-Start and Reference Tracking

The operation principle of soft-start and reference tracking circuit can be divided into two parts as shown in Fig. 24. At the first stage, the reference voltage level can rise gradually [23] by only executes the charging action. At the second stage, the adjusting of reference

voltage only depends on the channel voltage drop. If the head room of constant current sink circuit is too small the reference tracking circuit will execute up tracking and via versa.

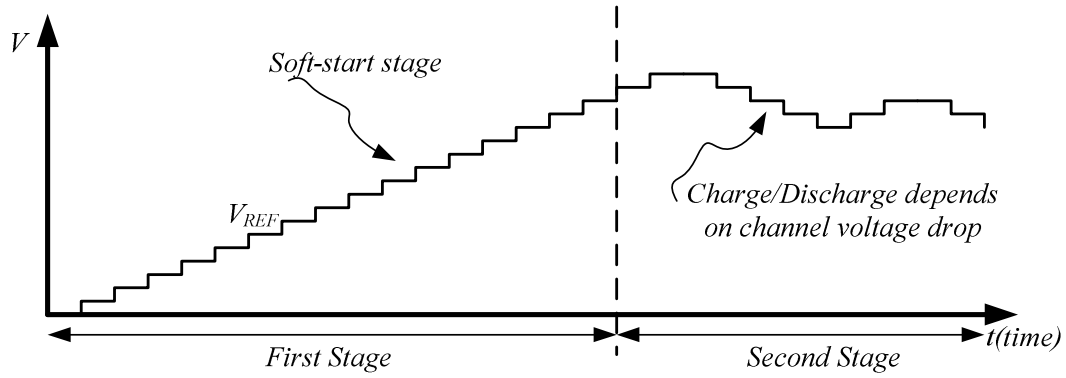
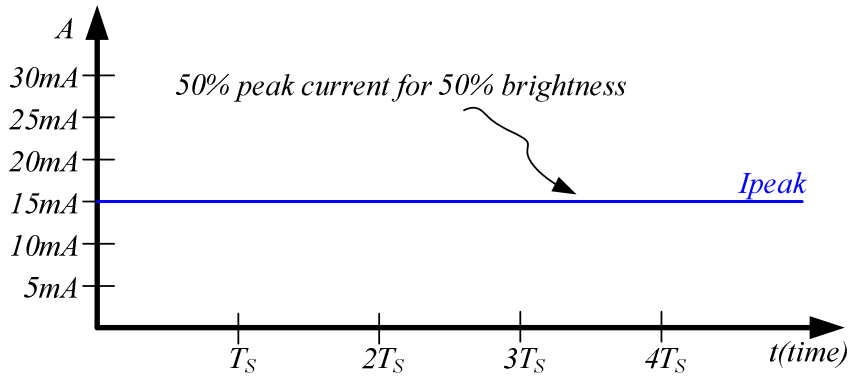


Fig. 24.The proposed LED driver with current-mode boost converter

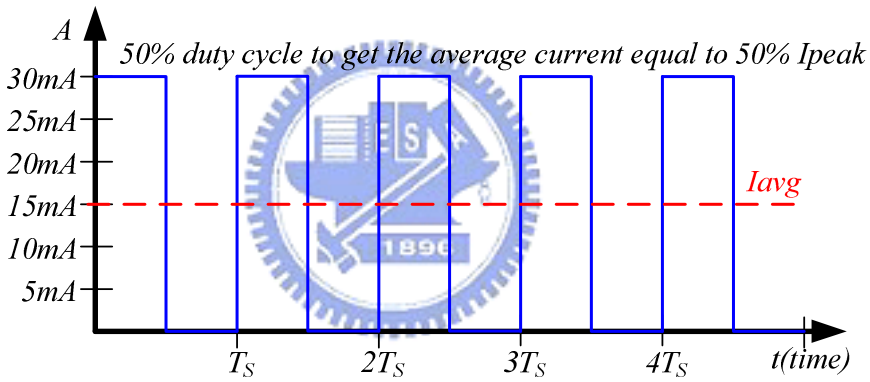
3.1.3. PWM Dimming Consideration

Consider the PWM dimming and constant current sink circuit in Fig. 25 [4]. Owing to the current matching is the most important issue for LED strings as a backlight system. The constant current sink circuit to ensure the current matching is needed. Otherwise, High-quality, full-color video requires hundreds or thousands of gray levels from 0% to 100%. Therefore, the adjustment of gray level can always achieved by the dimming method. As mentioned before, the dimming method can be divided into two types, analog and digital dimming. The LED current and brightness which adjusted by changing the forward voltage of LED is called analog dimming. On the other hands, PWM dimming is achieved by applying full current to the LED and adjusted by modulating duty cycle. In analog dimming, if an LED is at full brightness with 30 mA of forward current, then 50% of the brightness is achieved by applying 50% of the maximum current to the LED. In digital dimming, the 50% brightness is controlled by adjusting the relative duty cycle for 50% of each period. Both of these two methods are illustrated in Fig. 25. Thus, the average current in PWM dimming can be written as equation (48). The parameter D represents the duty cycle of the PWM dimming signal.

$$I_{avg} = I_{peak} \times D \tag{48}$$



(a)



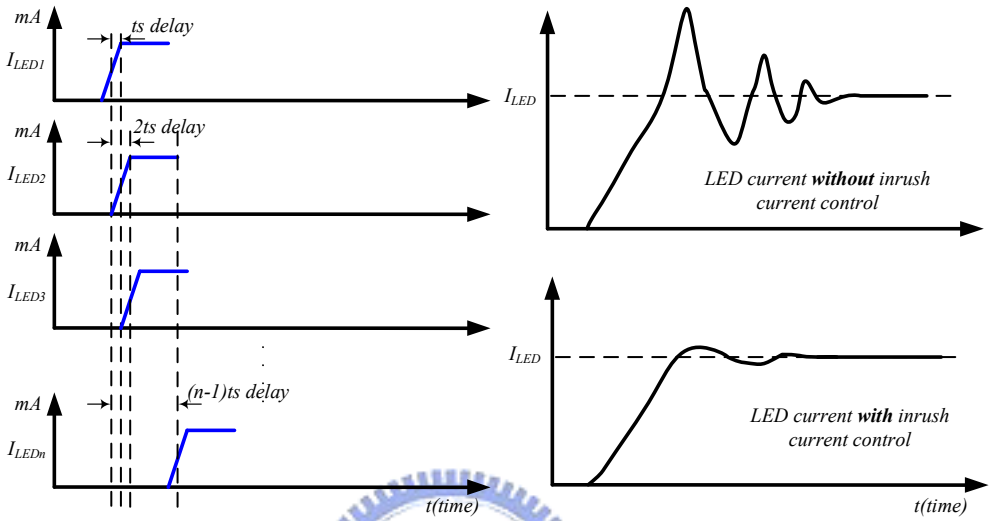
(b)

Fig. 25. (a) Analog dimming for LED current. (b) Digital dimming for LED current.

The differences between the analog dimming and digital dimming are as follow. Because of the brightness control method of analog dimming which will cause the color shift with changes in forward voltage. However, the forward current of LED is always constant in PWM dimming, so color of LED does not vary with brightness. The switching frequency of PWM dimming must be above 100 Hz to avoid the human eyes seeing the LED turned on and off.

The other important issue for PWM dimming is inrush current. Turning on all LED strings simultaneously requires a large current and caused inrush current with relative large

spike to the purpose current value. Therefore, a delay method is needed to solve the problem of inrush current. The delay method which uses the time delay to turn on the LED strings gradually. Therefore, the inrush current can be improved as shown in Fig. 26 [4].



(a) (b)

Fig. 26. (a) Inrush current control method. (b) The LED current with and without inrush control method

3.1.4. Load Dependent Minimum Drain with Constant Current Sink

The load dependent minimum drain circuit is utilized to determine minimum drain voltage according to the situation of the current through LED stings as shown in Fig. 27. The main idea is to save unnecessary power loss in the constant current sink circuit.

In Fig. 27, it shows that in different current condition the head room of constant current sink circuit will be claimed to different voltage level. For example, when LED current is 20mA and 30mA, the head room of constant current sink circuit equals to 0.7V and 0.9V respectively.

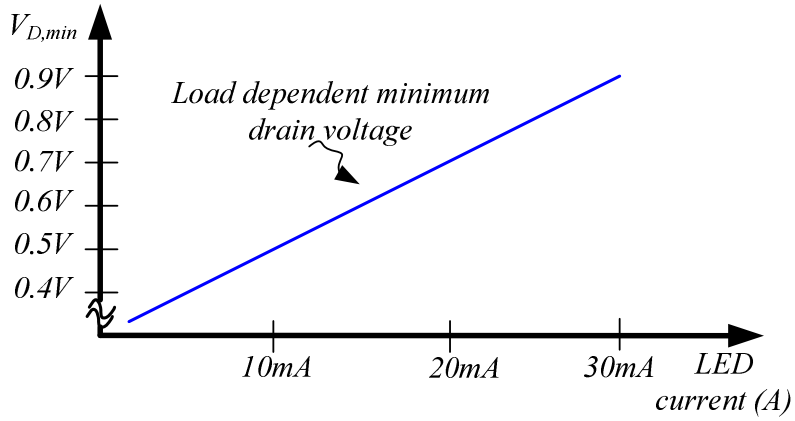


Fig. 27.The proposed LED driver with current-mode boost converter

3.2. The Proposed Soft-Start and Reference Tracking Implementation and Simulation Result

The proposed soft-start and reference tracking circuit is shown in Fig. 28. The voltage level of reference to do up and down tracking is achieved by the charge and discharge path. The charge and discharge action can be divided into two parts and controlled by the signal of soft-start or not.

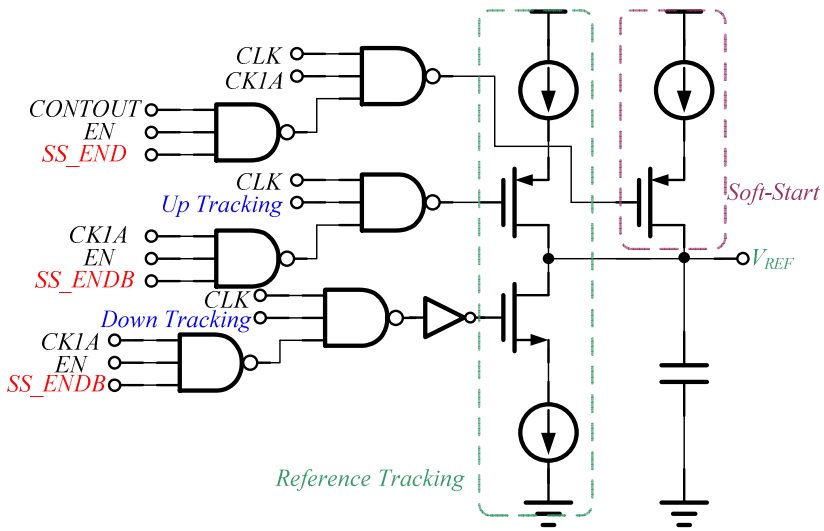


Fig. 28.The proposed LED driver with current-mode boost converter

The soft-start part operates just when the signal *SS_END* and *SS_ENB* equals to digital

VDD and digital *GND* respectively. At the same time, the reference tracking part is in the idle mode. The clock signals *CLK*, *CLK1A*, *COUTOUT* are several kind of period to determine the charged and discharged operation duration. Therefore, the operation of this circuit can be summarized in TABLE II. The internal blocks of this circuit will be introduced in the following sections.

TABLE II

State table of soft-start and reference tracking circuit

Signal	Operation
SS_END=1 , SS_END=0	Soft-Start
SS_END=0 , SS_END=1	Referencing Tracking
COUNTOUT is utilized to setup the step of soft start	

3.2.1. Detection Clock Generator

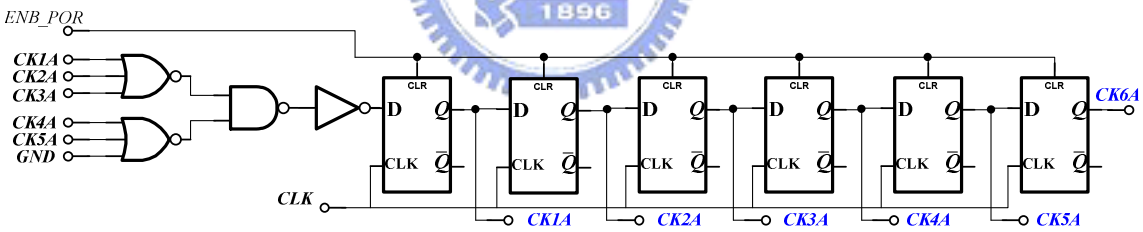


Fig. 29.The one period detection clock generator circuit

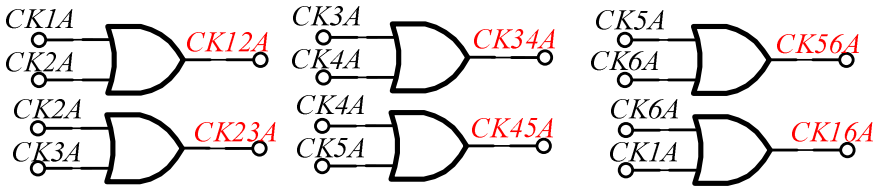


Fig. 30.The two periods detection clock generator circuit

The clock generator circuit is utilized to generate the clock for detection of the voltage drop on the constant current circuit. Due to the PWM dimming signal for each channel has a

short time delay, that's the reason why this kind of clock is needed. Therefore, the detecting action can not do at the same time.

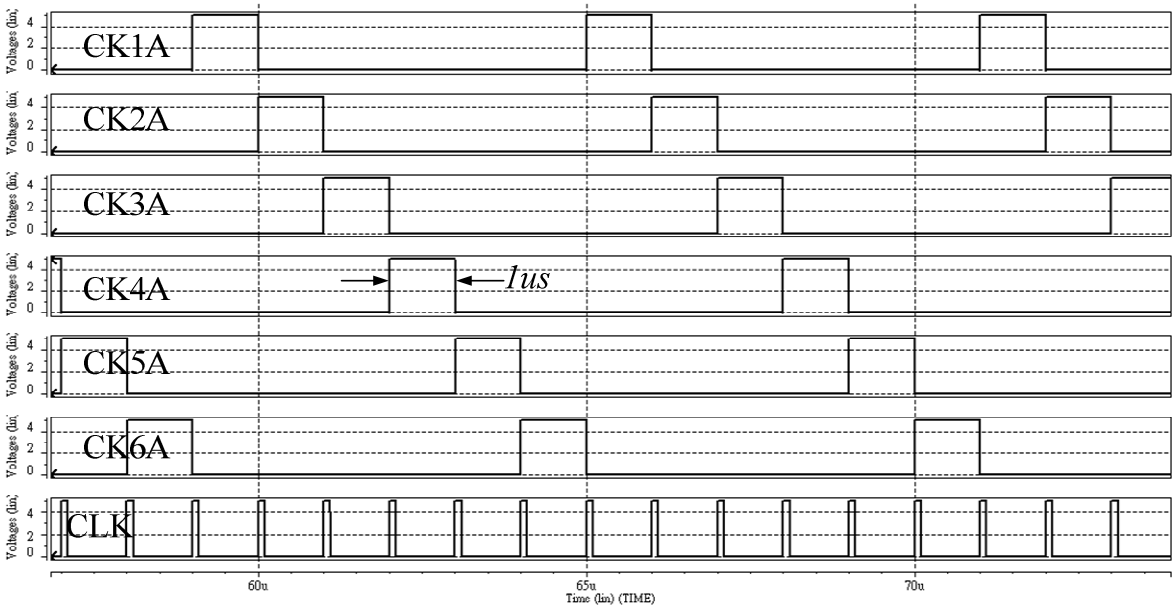


Fig. 31.The simulation result of CK1A ~ CK6A

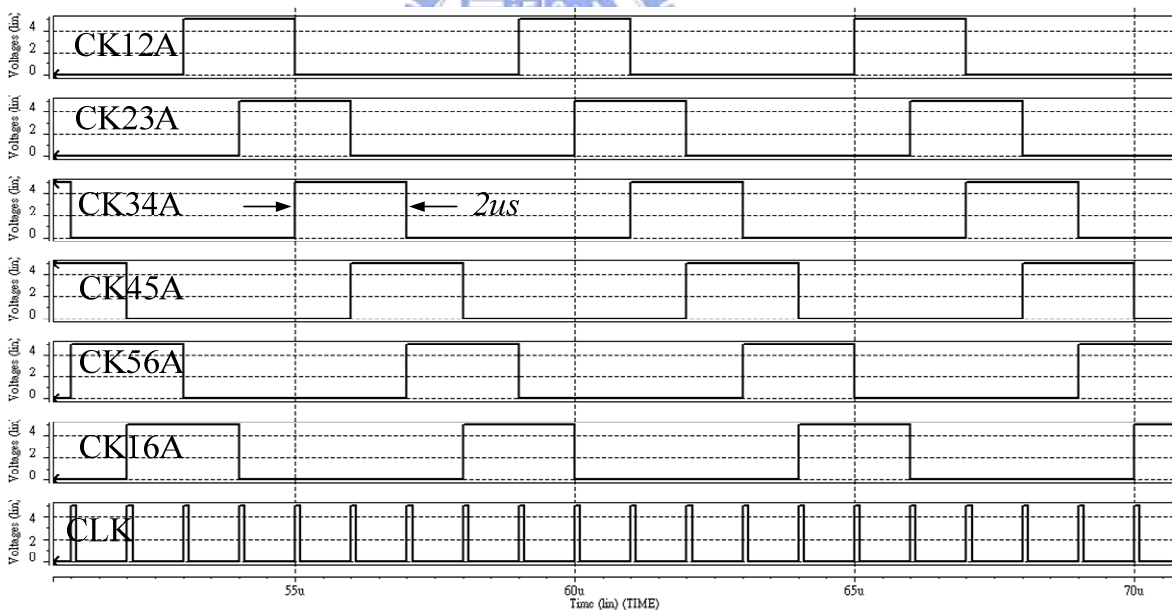


Fig. 32.The simulation result of CK12A ~ CK16A

The clocks *CK1A* to *CK6A* are signals with 6us period and sixth of one duty cycle. The circuit implementation is shown in Fig. 29. The clocks *CK12A* to *CK16A* are signals with 6us period and third of one duty cycle. The circuit implementation is shown in Fig. 30. Both of

the circuits in Fig. 29 and Fig. 30 are utilized to generate six phase shift clocks to do voltage detection for all the channels. Thus, the simulation results are shown in Fig. 31 and Fig. 32, respectively.

3.2.2. Voltage Drop on Constant Current Sink Detection Circuit

The voltage drop detection circuit for one of the LED strings is shown in Fig. 33. This circuit is utilized to detect the voltage drop on the constant current sink and delivers the signals to reference tracking circuit to do up or down tracking. The reference voltage V_H and V_L are the expectative window for the voltage drop on the constant current sink circuit. The voltage drop on the constant current sink circuit will be called V_{CH} following. The comparator is utilized to compare V_{CH} which is higher or lower than the reference voltage V_H and V_L respectively. The clock signals *CK12A*, *CK2A*, *CK4A* are generated by detection clock generator. The pin *S1* is utilized to set the detection action should be enabled or disabled. The pin PWM1 is the PWM dimming of the first LED string.

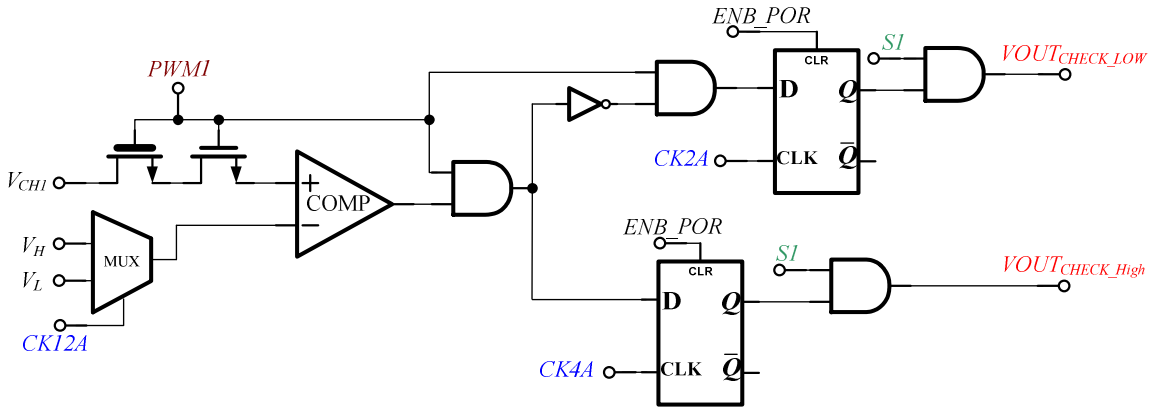


Fig. 33.Voltage drop on constant current sink detection circuit

The operation principle of this circuit is described as follow:

The compare operation will do low reference level check first. When the *CK12A* is at

digital *VDD*, the multiplexer will select the voltage V_L to the negative input terminal of the comparator. Therefore, the comparator compares the V_{CH} and V_L to produce a digital signal output and latch it by the D type flip-flop. The compared result latched by D type flip-flop will be delivered to the output when the clock *CK2A* at digital *GND* transforms into digital *VDD*. Thus, the signal $VOUT_{CHECK\_LOW}$ is formed.

Consider to the signal *CK12A* translates to digital *GND*; the multiplexer will select voltage V_H to the negative input terminal of the comparator. Then the output of comparator will be generated according to the voltage level of V_{CH} and V_H. The output signal generated by the comparator is also latched in the D type flip-flop and waits for the *CK4A*. When *CK4A* is at digital *VDD* the data which latched in D type flip-flop will be delivered to output. Thus, the signal $VOUT_{CHECK\_HIGH}$ is formed.

Summing up the statements mentioned before, this detection circuit will be used in every channel. All of the detection circuits will produce the signals $VOUT_{CHECK\_LOW}$ and $VOUT_{CHECK\_HIGH}$ to reference tracking circuit to do up or down tracking. And the simulation result is shown in Fig. 34.

The simulation results are shown in Fig. 34 (a) and (b). In Fig. 34 (a), it shows the detection clock for first sting. In Fig. 34 (b), it shows the reference voltage of the comparator, the output voltage of the comparator, the test signal as the voltage drop on the constant current sink, the detection results $VOUT_{CHECK\_HIGH}$ and $VOUT_{CHECK\_LOW}$. Note that the voltage levels of V_H and V_L is 1.1V and 0.9V, respectively.

The simulation results can be divided into three regions. There are the times before 30u seconds, 30u seconds to 60u seconds and after 60u seconds.

In the first region, the voltage V_{CH} is set between V_H and V_L. This V_{CH} level is in the purposed voltage window and the reference tracking circuit will stay in the idle mode.

In the second region, the voltage V_{CH} is set to be higher than the upper bound V_H. This V_{CH} level is over the purposed voltage window. And if the V_{CH} of six LED strings are exceed

the upper bound, the reference tracking unit will do down tracking to scale down the reference voltage.

In the third region, the voltage V_{CH} is set to 0, which is smaller than both V_H and V_L. This V_{CH} level is under the purposed voltage window. Therefore, this detection circuit should generate the signal for reference tracking circuit to do up tracking.

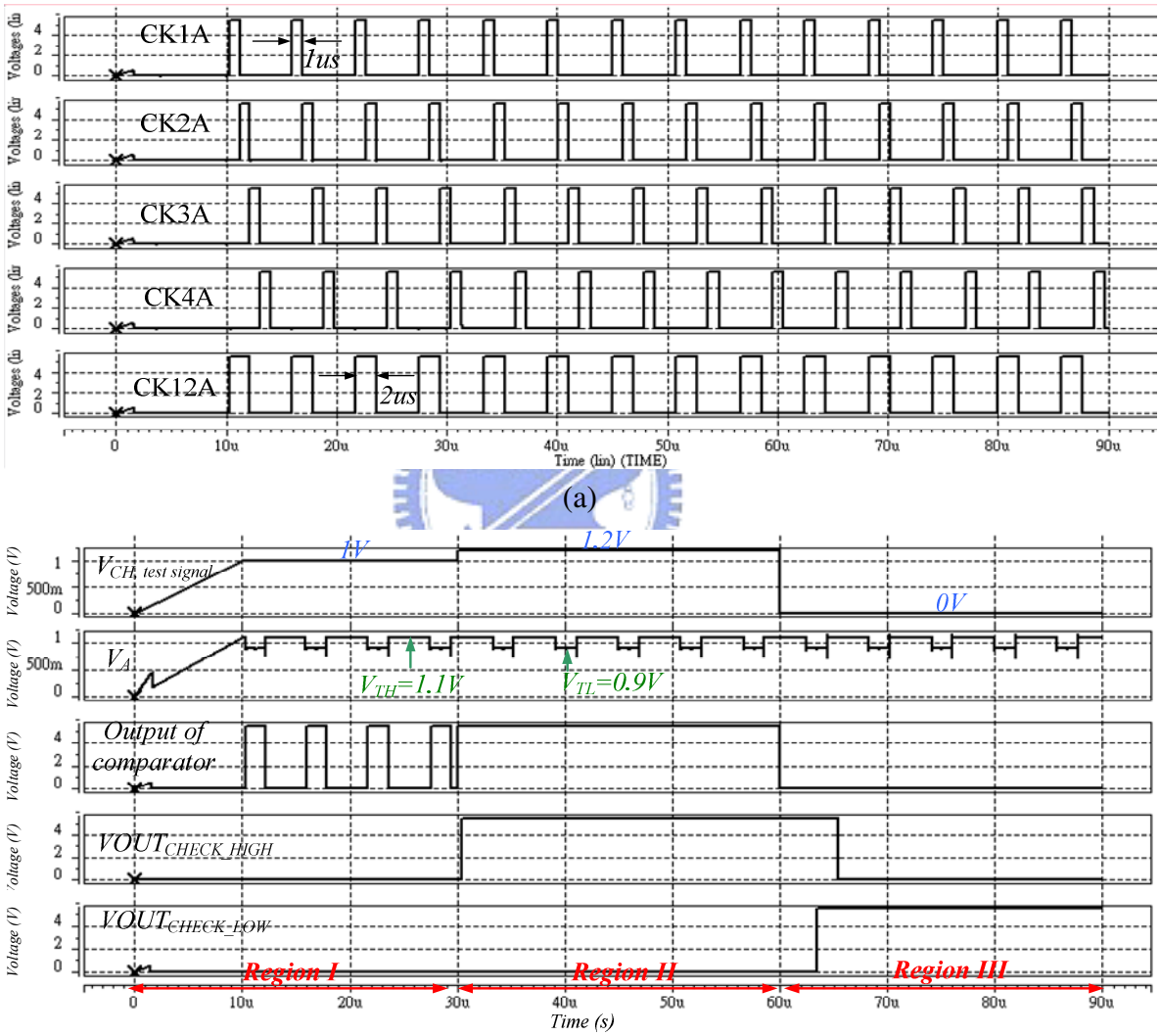


Fig. 34.(a) Detection signal for the first LED sting (b)Output signals of the detection circuit

In a brief conclusion, the entire signal states mentioned above are list in TABLE III. TABLE III shows the relationship between input and output signals.

TABLE III

The relationship between input and output signals

V_{CH}	$VOUT_{CHECK\_HIGH}$	$VOUT_{CHECK\_LOW}$	Reference Tracking
$V_L < V_{CH} < V_H$	0	0	idle
$V_H < V_{CH}$	1	0	Down tracking
$V_{CH} < V_L$	0	1	Up tracking

3.2.3. Reference Tracking Circuit

Fig. 35 shows the reference tracking decision circuit to adjust the reference voltage level according to the voltage drop on the constant current sink unit.

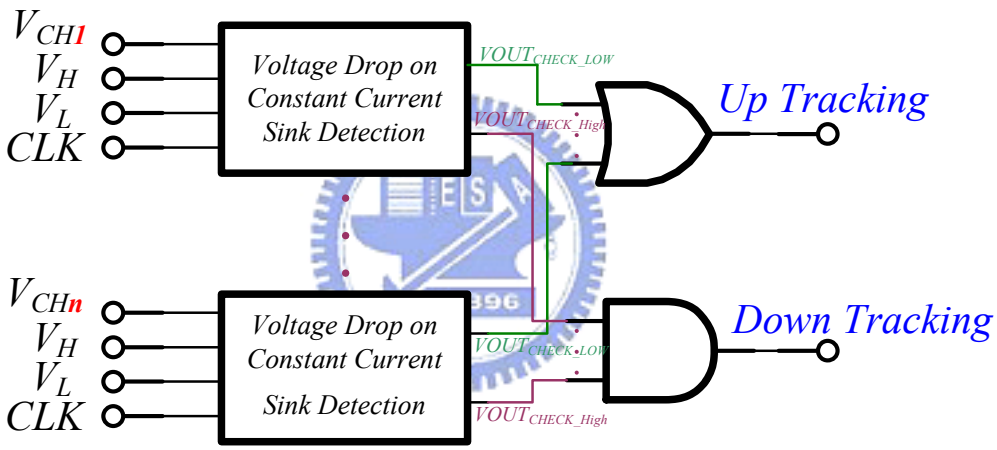


Fig. 35.Voltage drop on constant current sink detection circuit

In Fig. 35, the left side signals are the same as defined in section3.2.2. The *CLK* signal includes *CK12A*, *CK2A* and *CK4A*. The up and down tracking will be generated by copy the voltage drop on the constant current sink detection cell. However, the condition of up and down tracking is a little different. For up tracking it is triggered by one of the $VOUT_{CHECK\_LOW}$ equals to digital *VDD*. If one of the head rooms of constant current sink circuit has been suppressed, it means that the forward voltage of LED of the corresponding string is too large. And the output voltage of boost converter should be rose up rapidly to offer a sufficient driving voltage to all the LED strings. After increasing the output voltage of boost converter,

the LED string can operate normally again. For down tracking, it will execute when all of the $VOUT_{CHECK\_HIGH}$ equals to digital *VDD*. It is because that all the voltage drops on the constant current sink circuit is enough and unnecessary. The higher voltage drop on the constant current sink circuit will cause a dispensable power loss. However, before executing the down tracking action, it should make sure that all the head room of constant current sink circuits are high enough. Therefore, the down tracking can be done. The operations can be summarized in TABLE IV.

TABLE IV
The operations of reference tracking

One of $VOUT_{CHECK\_LOW}$ = 1	Up tracking =1	To charge to capacitor of reference
All of $VOUT_{CHECK\_HIGH}$ = 1	Down tracking =1	To discharge to capacitor of reference

3.2.4. Soft-Start End-Point Detection

The soft-start end-point detection is important for the switching of soft-start and reference tracking. This circuit is utilized to detect the reference voltage to determine when the soft-start duration should be finished. The circuit is composed as shown in Fig. 36.

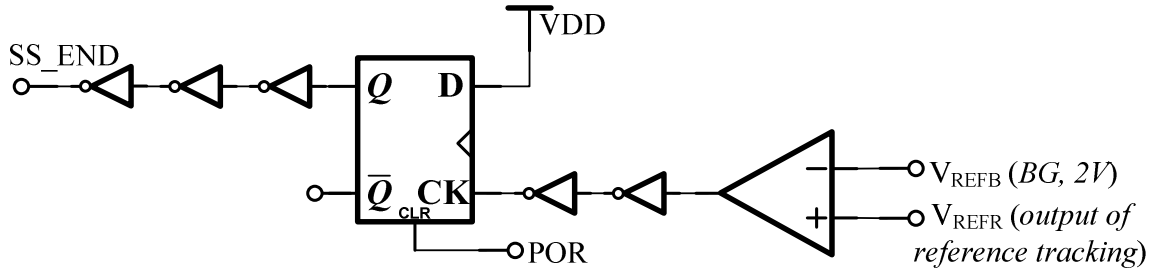


Fig. 36.Soft-start end-point detection

The operation principle can be stated as follow:

During the power on stage the signal *POR* is at digital *VDD* to clear the D type flip flop

and *SS_END* equals to digital *VDD*. When the signal *SS_END* is at digital *VDD*, the reference tracking circuit do up tracking for soft-start. After the power on stage the flip flop will be triggered by the state of V_{REFB} and V_{REFR}. The signals V_{REFB}, V_{REFR} are the output of bandgap and reference tracking circuit respectively. At the soft-start stage the voltage V_{REFR} will be rose gradually. The target of the end-point of soft-start is when the reference voltage attains to 2V. And through the virtual ground characteristic of the input terminal of error amplifier, we can regulate the output voltage of boost converter by reference voltage level. In order to make the feedback voltage equals to 2V as the output of boost converter reached to 40V, it can be achieved by selecting the appropriate feedback voltage. Therefore, the end-point of soft-start is decided when the output of reference tracking circuit arrives to 2V. And the output of comparator changes to digital *VDD* to trigger the D type flip flop. The output of D type flip flop rises from digital *GND* to *VDD* and *SS_END* equals to digital *GND*. Thus, the reference tracking circuit executes both up and down tracking again.

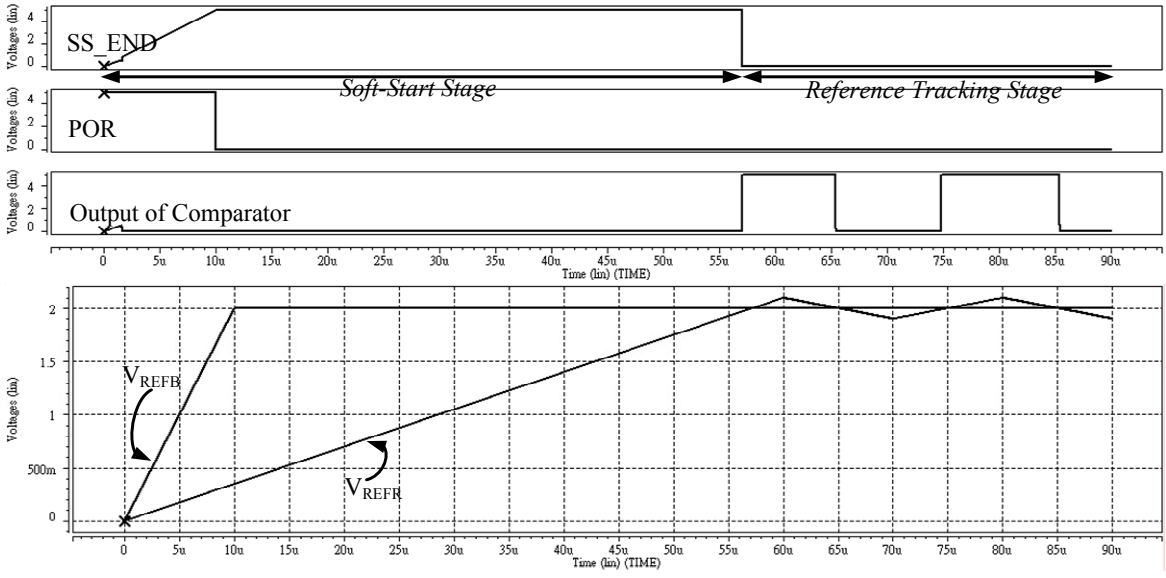


Fig. 37.The simulation result of soft-start end-point detection

Fig. 37 shows the simulation result of soft-start end-point detection circuit. From the simulation result we can realize that after the soft-start stage the output of D type flip flop will

be latched regardless of the variation of V_{REFR}. Therefore, the soft-start will not do again to avoid a wrong action.

3.3. Load Dependent Minimum Drain Circuit

For a LED driver, current matching is an important issue. In order to regulate the current of each string the constant current sink circuit is needed. However, the head room of constant current sink circuit is a key point for design. In conventional design, the head room of constant current sink circuit is claimed and fixed for different LED current applications [24]. However, over large head room of constant sink circuit will cause unnecessary power loss and poor efficiency. Inversely, over small head room will result in an incorrect current through LED string. Therefore, an appropriate head room of constant current sink circuit for different current application is significant. In this thesis, we proposed a load dependent minimum drain method to adjust the head room automatically.

3.3.1. Constant Current Sink Current

Fig. 38 [25] [26] shows the constant current sink circuit to regulate the LED currents. The external resistance R_{ext} is an off-chip element to determine the LED current. The practical current through LEDs is the current I_{ref} amplified by the current mirror. The LED current can be written as equation (49) where the parameters N and K are the proportional current of the current mirrors. And the operational amplifiers in this circuit are utilized to claim the V_{DS} voltage drops on the current mirror to get a precise mirror current.

$$I_{LED} = I_{REF} \times N \times K \tag{49}$$

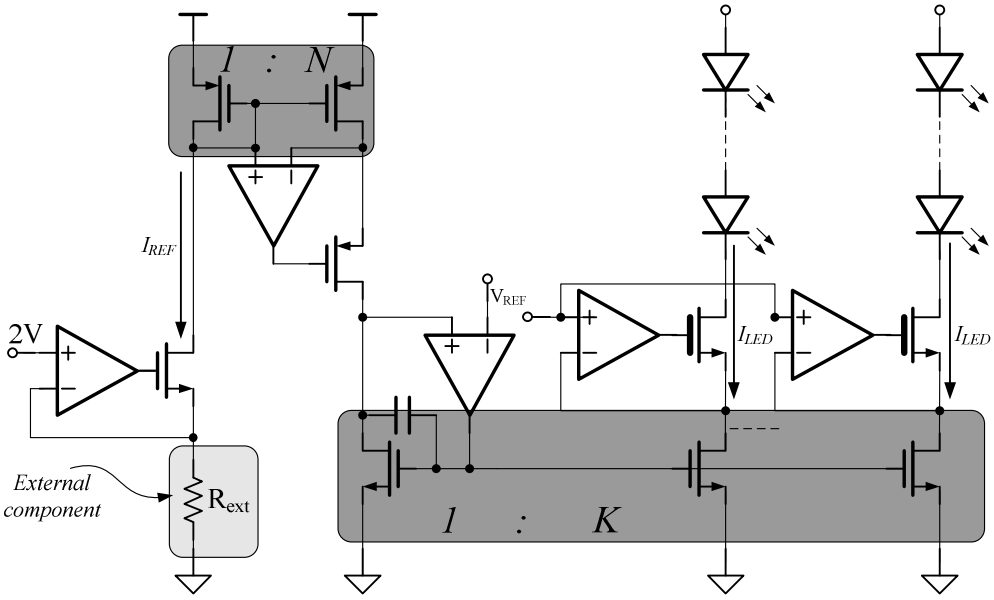


Fig. 38. Constant current sink circuit

3.3.2. Load Dependent Minimum Drain Circuit

The head room of constant current sink circuit is an important issue for design. In conventional design, the head room of constant current sink circuit is claimed and fixed for different LED current applications. For example, if the minimum head room is fixed at 0.9V for 10mA, 20mA, 30mA current of LED strings and the power loss on the constant current sink are 9mW, 18mW and 27mW per strings respectively.

From the I-V characteristic of MOSFET we can know that, for a small current application the gate-source voltage is relative low and the drain-source voltage can be scaled down, too. Therefore, this thesis proposed a load dependent technique to save unnecessary power loss on the constant current sink circuit.

In Fig. 41, there are two added parts to do voltage adjustment for the constant current sink circuit. Both of the added circuits modulate the voltage by current sensing method. The current mirror NMOS (called low-side NMOS) can be observed that the gate-source voltage has a 0.1V variation with per-10mA current change. Therefore, the first current sensing loop for V_{DS} will generate 0.3V, 0.4V, 0.5V voltage level for 10mA, 20mA and 30mA current

conditions. The second current sensing loop is to do the same operation as the first loop. Due to the adjustment of voltage V_{TL} includes both the low-side and cascade NMOS, thus the scale is two times of V_{DS}. Therefore, for 10mA, 20mA, 30mA current conditions the corresponding voltage level of V_{TL} are 0.5V, 0.7V and 0.9V respectively. The voltage level V_{TH} is as the upper bound of the voltage drop on the constant current sink circuit. It is 0.2V higher than the lower bound V_{TL}. By these two voltage levels the range of the voltage drop on constant current sink circuit can be determined. And the voltages V_{TH} and V_{TL} form the window for the detection circuit in 3.2.2.

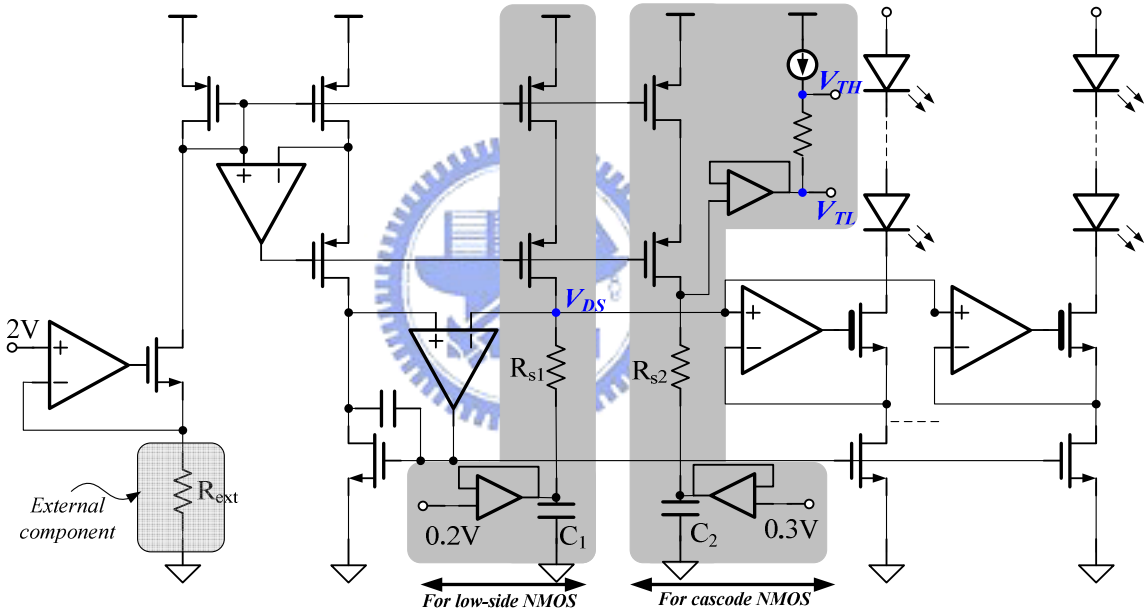


Fig. 39. Constant current sink circuit with load dependent minimum drain technique

The comparisons of power consumption of constant sink circuit with and without load depend adjustment circuit are shown in TABLE V, TABLE VI respectively. Considering the condition of 20mA LED current, the power difference is 4mW for each sting. Therefore, if there are six strings parallel at once, 24mW power loss can be saved. In conclusion, by using a load dependent V_{DS} circuit can help saving the power loss in low current application.

TABLE V

The constant current sink circuit without load depend minimum drain circuit

Current	V_{DS}	Power Consumption
I_{LED}=10mA	$V_{CH,MIN}$ = 0.9V	9mW
I_{LED}=20mA	$V_{CH,MIN}$ = 0.9V	18mW
I_{LED}=30mA	$V_{CH,MIN}$ = 0.9V	27mW

TABLE VI

The constant current sink circuit with load depend minimum drain circuit

Current	V_{DS}	Power Consumption
I_{LED}=10mA	$V_{CH,MIN}$ = 0.5V	5mW
I_{LED}=20mA	$V_{CH,MIN}$ = 0.7V	14mW
I_{LED}=30mA	$V_{CH,MIN}$ = 0.9V	27mW

Chapter 4

The system implementations and simulation results

In this chapter, the simulation results and detail description of each sub-circuit mentioned in Chapter 3 are presented. The Simulation conditions for each circuit are shown in TABLE VII.

TABLE VII
The conditions of simulations

Power supply of control circuit				
4.5		5		5.5
Temperature Range				
-20 ~ 120				
Process Corner				
TT	FF	SF	SS	FS

4.1. Bandgap Reference and Bias Circuit

The bandgap reference [27] circuit is important in integrated circuit to generate a fixed voltage level, V_{REF}. The reference voltage which generated by bandgap reference circuit is independent of power supply V_{DD}, process variations and temperature.

The bandgap voltage reference involves the bandgap core circuit, bias circuit, trimming circuit and startup circuit, which are shown in Fig. 41. The core circuit is composed of current generator and operational amplifier. The current is generated by the bipolar Q_1, Q_2, and the resistance R_1, R_2, and R_3. The reference voltage can be obtained as equation (50), where the base-emitter voltage of bipolar transistor is a negative temperature coefficient (TC) and V_T is the positive TC. The zero TC for voltage reference V_{REF} can be obtained by selecting the

appropriate resistors R_1, R_2, R_{trim} and the ratio of bipolar Q_1, Q_2.

$$V_{REF} = \left[\frac{V_T \ln(n)}{R_1} + \frac{V_{EB,Q1}}{R_2} \right] \times R_{trim} \tag{50}$$

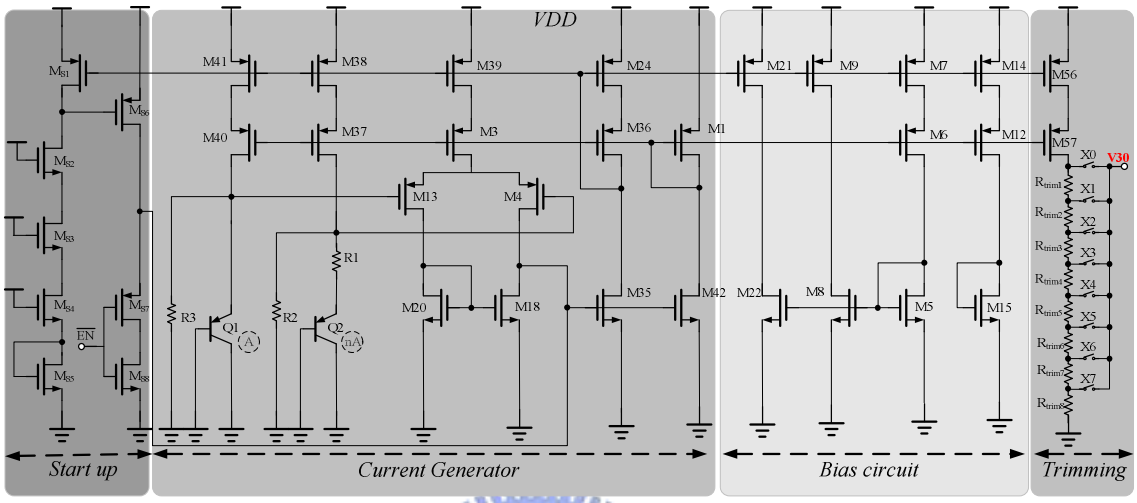


Fig. 40. The circuit structure of bandgap reference

The power on sequence of the proposed start up circuit is describe as follow. When the circuit is at enable state $EN = 1$, $\overline{EN} = 0$, the MOSFET M_{S6} pulls the gate voltage of NMOS, M_{35} and M_{42}, to a relative high level. Therefore, the gate voltage of PMOS will be pull to a relative low level to avoid an incorrect steady state. After the start up operation, M_{S1} turns off. And the gate voltage of M_{S1} returns to the regular level.

The bias circuit in Fig. 40 is to generate the bias voltage level for other sub-circuits such as comparators, operational amplifiers and so on.

The trimming resistance R_{trim} is utilized to modify the voltage V_{REF} for attaining the precise voltage level under the variations from the process. The control signals X_0 ~ X_8 are digital codes to adjust the voltage V_{REF}. Therefore, by setting the switch X_4 on and others off to get the voltage V_{REF} to expectative level in simulation, the best trimming range can be obtained.

The simulation results are shown in Fig. 41. The typical reference voltage is 3.0V and the

ranges of supply voltage are 4.5V ~ 5.5V. The temperature coefficient (TC) under all corner and supply voltages can be calculated as.

$$TC = \frac{\frac{\partial V_{REF}}{V_{REF}}}{\partial T} \times 10^6 = \frac{\frac{8mV}{3.0V}}{140°} \times 10^6 = 18.1 ppm/°C \quad (51)$$

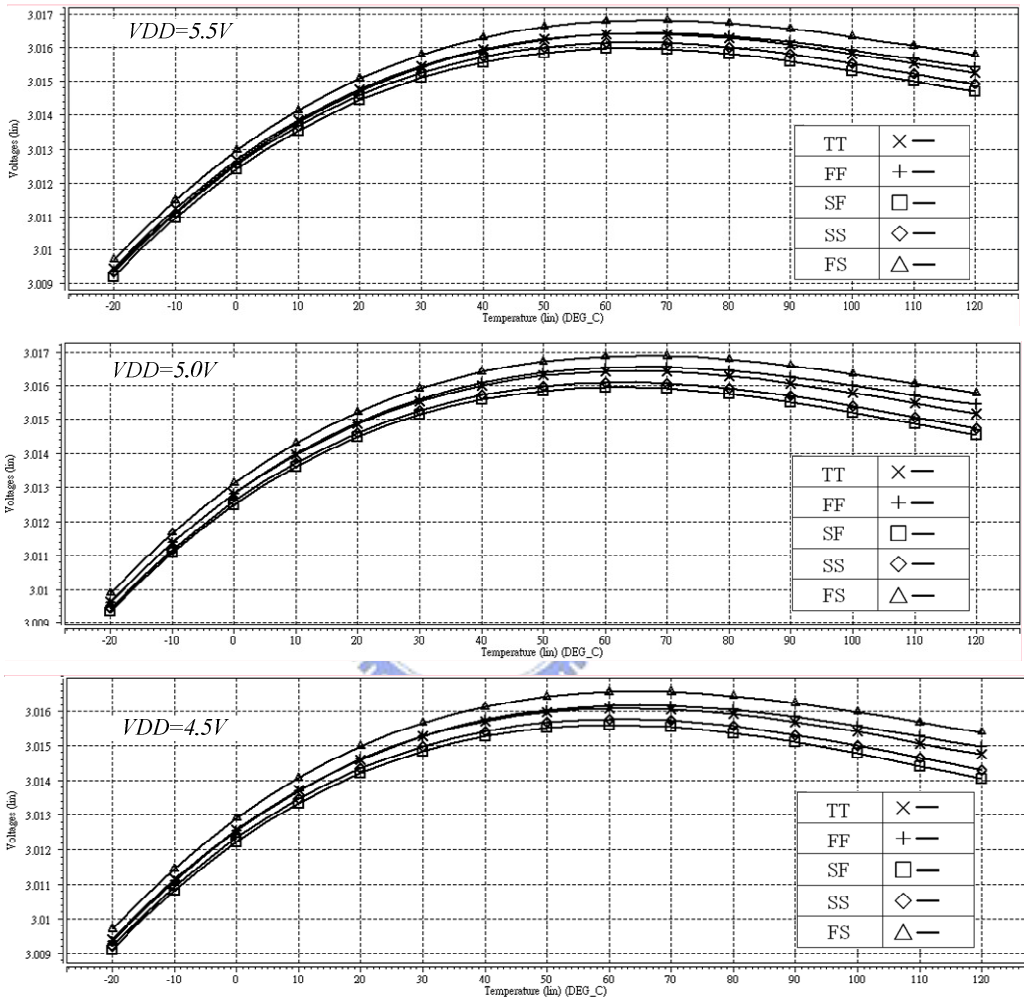


Fig. 41. The simulations for the bandgap voltage reference circuit that varies supply voltage, operating temperature and process variation.

4.2. Ramp and Clock Generator

The ramp and clock generator is utilized to offer the one-shot clock and artificial ramp. The simulation result of one-shot clock and the compensated ramp are shown in Fig. 42. The one-shot clock is the switching frequency of the converter. The ramp signal is to avoid

oscillation of the current mode DC-DC converter when the duty cycle larger than 50%.

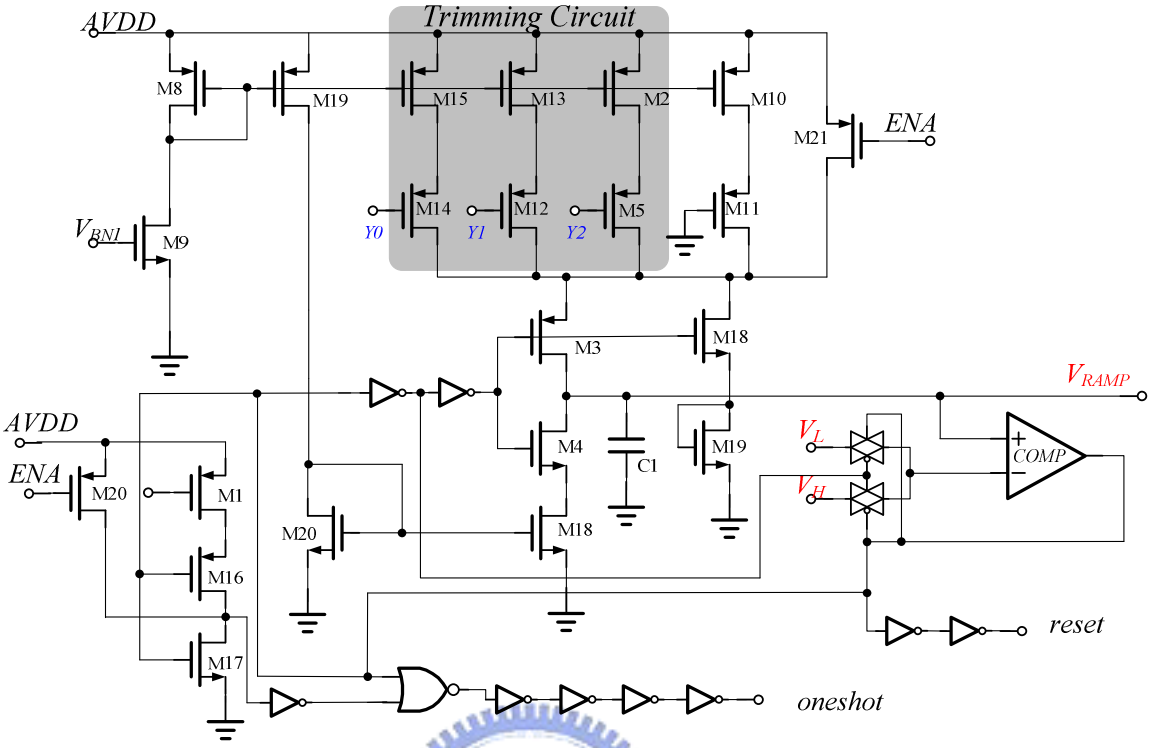


Fig. 42. The circuit structure of ramp and clock generator.

The operation principle can be described as follow:

When the output of comparator is pulled low, the reference voltage of comparator equals to V_H. The switch transistor M_3 is turned on and the switch transistor M_4 is turned off. Therefore, the capacitor is charged by the designed current to generate the rising up signal.

When the voltage of the capacitor reaches to the upper bound voltage V_H, the output of the comparator is pulled high to turn off the switch M_3 and turn on the switch M_4. The reference voltage of the comparator is returns to V_L. Therefore, the capacitor is discharged by the designed current through M_4, M_{18} to generate the falling down signal. The signal *reset, oneshot* are pulled to high and low respectively.

During the discharge state, the output of comparator is pulled low when the voltage of capacitor fall to the lower bound V_L. The signal *reset, oneshot* are pulled to low and high respectively. Therefore, the ramp and clock signal can be formed by repeat above operation.

As mentioned above, the *oneshot* clock is provided when the output of comparator is

pulled high. Owing to the *oneshot* clock should be designed as small as possible; the percentage of the period is 10% normally. However, the rising slop of the ramp signal must be corresponding to the compensation principle. In conclusion, the compensation slope is determined by equation (52), where m_a is the slope of ramp current, m_2 is the down-slope of sensed inductor current.

$$m_a \geq \frac{1}{2} \times m_2$$
$$\frac{V_H - V_L}{0.9 \times T_S} \geq \frac{1}{2} \times \left(\frac{V_{OUT,MAX} - V_{IN,\min}}{L} \right) \times R_{SENSE} \quad (52)$$

The boundary voltage V_H and V_L are designed as 3V and 1.2V. Furthermore, the charging current I is 6.5 uA and the capacitor C_1 is 2.8pF. The simulation result of the ramp signal is shown in Fig. 43.

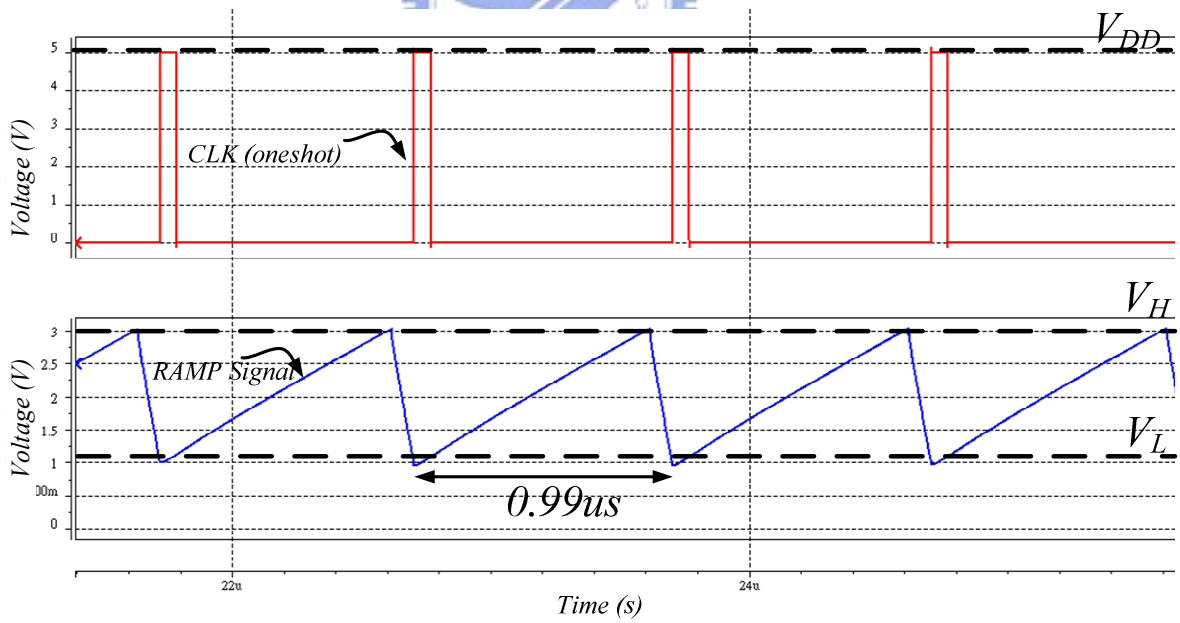


Fig. 43. The simulation result of the ramp and clock generator.

4.3. Voltage to Current Converter

In current-mode converters, the compensation ramp needs to add with the sensing current

signal to avoid sub-harmonic oscillation. However, it is difficult to add the signals in voltage domain and accurately. Therefore, a voltage to current converter is needed and shown in Fig. 44 [14]. Then the ramp signal and sensing signal can be converted into currents and add by passing through the same resistor.

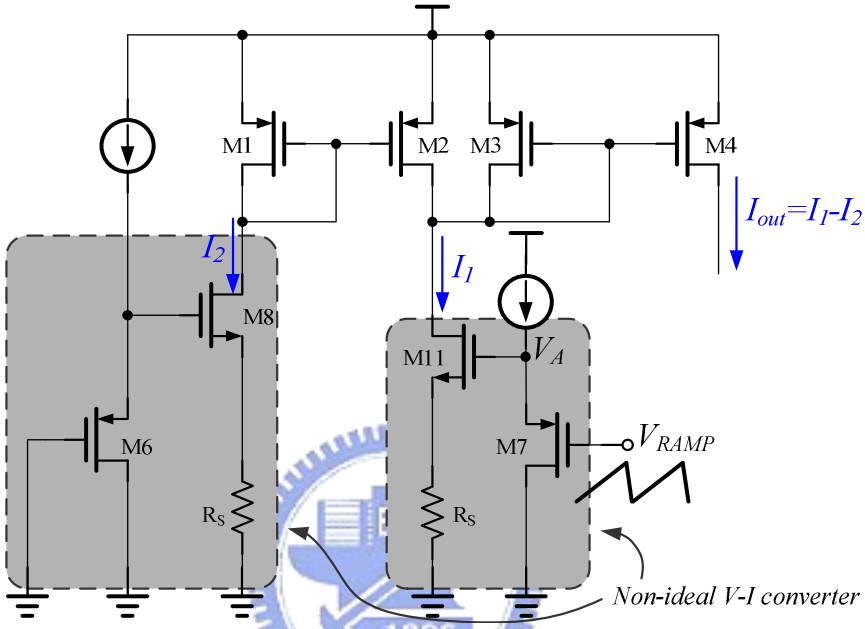


Fig. 44. Voltage to current converter.

The circuit consists of two identical non-ideal V-I converter. The reasons for using two identical parts will be described as follow. The current I_1 can be derived in equation (53).

$$V_A = V_{RAMPI} + V_{SG7}$$
$$G_{m11} = \frac{I_1}{V_A} = \frac{g_{m11}V_{gs11}}{V_{gs11} + I_1 R_S} = \frac{g_{m11}}{1 + g_{m11}R_S} \approx \frac{1}{R_S} \tag{53}$$
$$I_1 = V_A \times G_{m11} = \frac{V_{RAMP} + V_{SG7}}{R_S} = \frac{V_{RAMP}}{R_S} + \frac{V_{SG7}}{R_S}$$

Owing to the extra term of V_{GS}, the identical non-ideal converter is needed to eliminate it. Therefore, the current I_2 can be derived as

$$I_2 = \frac{V_{SG6}}{R_S} \tag{54}$$

By combining the equations (53) and (54), the unwanted term can be eliminated. The total current I_{out} is as follow, the simulation result is shown in Fig. 45.

$$I_{out} = I_1 - I_2 = \left(\frac{V_{RAMP}}{R_S} + \frac{V_{SG7}}{R_S} \right) - \frac{V_{SG6}}{R_S} = \frac{V_{RAMP}}{R_S} \propto V_{RAMP} \tag{55}$$

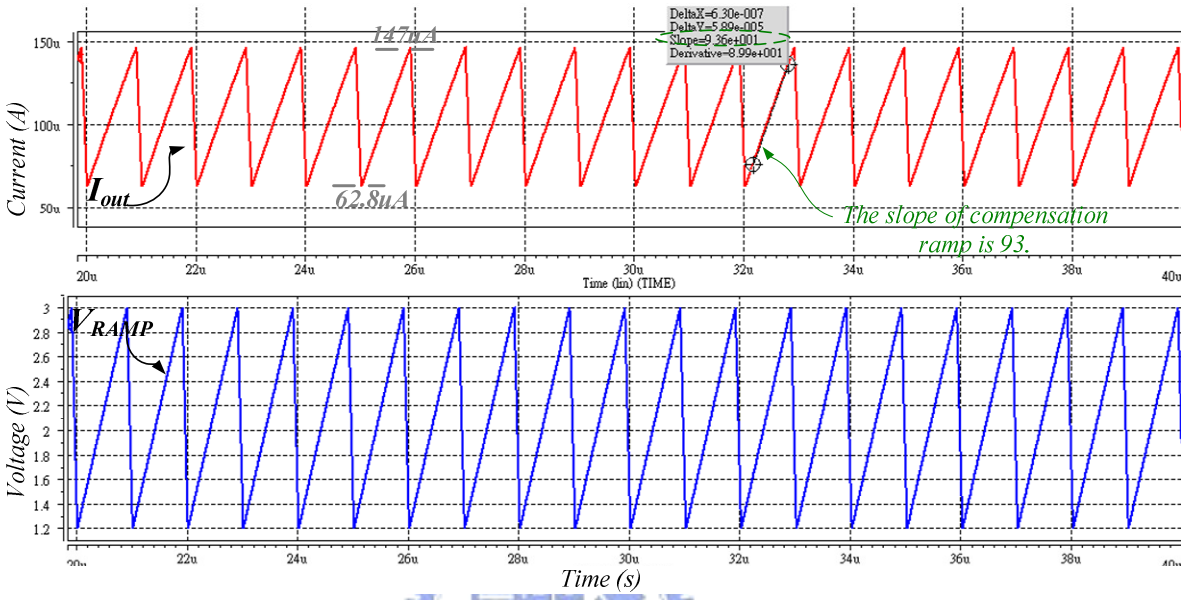


Fig. 45. Simulation result of voltage to current converter.

4.4. Error Amplifier

The error amplifier is utilized to amplify the error of feedback and reference voltage. The error amplifier is as the operational transconductance amplifier (OTA).The high current driving ability is the characteristic of OTA. Therefore, the OTA is suitable for the boost converter with large compensate capacitor. The circuit structure of the operational transconductance amplifier is shown in Fig. 46. The transistors M_{B1}-M_{B10} produce the biasing current to bias the error amplifier. The transistors M_{P3} and M_{P4} form the input differential pair with cascode-mirror loads that are constructed by the transistors M_{N1}-M_{N8} and M_{P5}-M_{P8}.

The simulation result of the operational transconductance amplifier is shown in Fig. 47. The dc gain of the error amplifier in this design is about 60dB for all corners. The unity gain frequency is 2.27MHz and the phase margin is 88° with capacitive load 10pF.

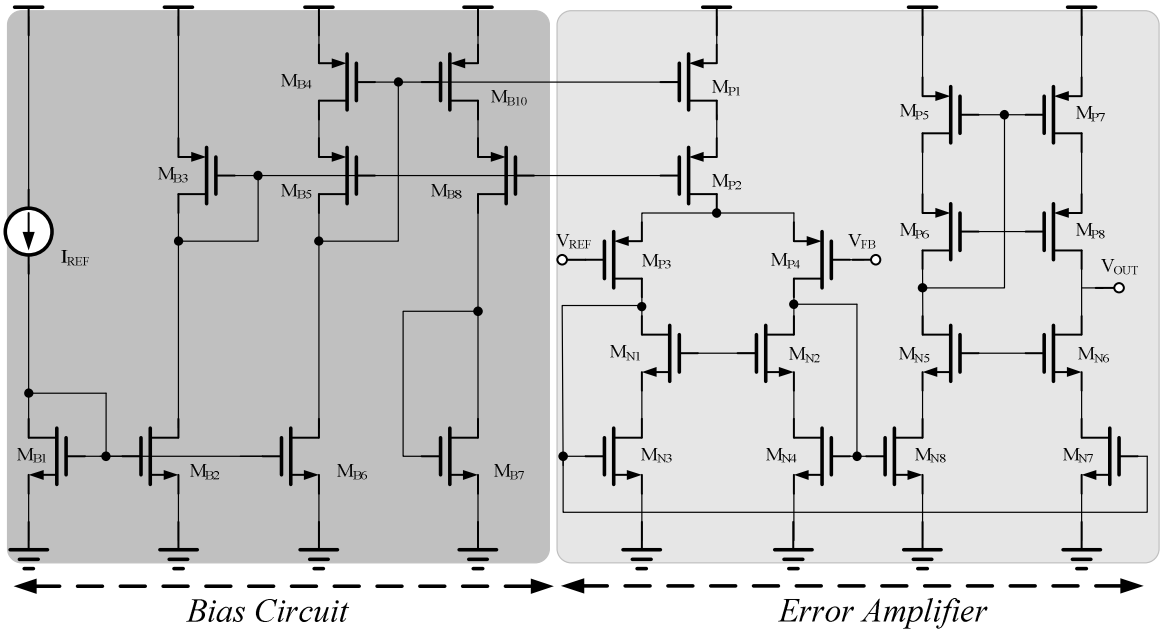


Fig. 46. The circuit structure of error amplifier.

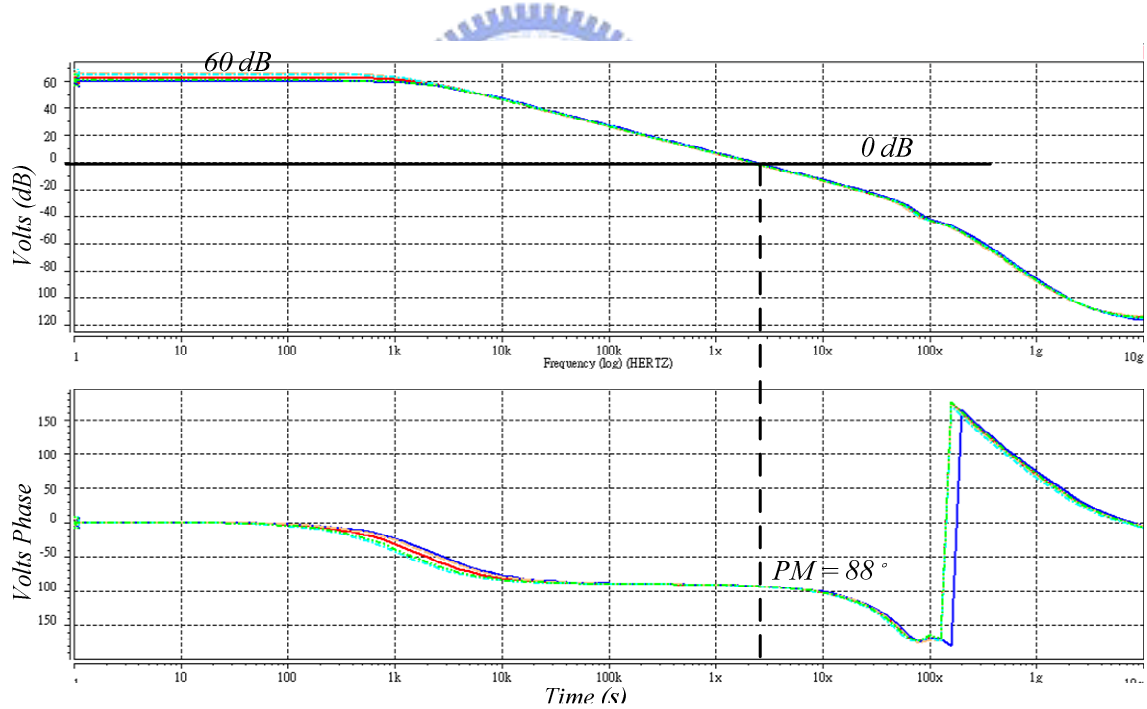


Fig. 47. The simulation result of error amplifier.

4.5. Level Shift Buffer

Owing to the power MOSFET of the boost converter is NMOS and it is a high voltage device with large V_{th}. The efficiency of switching converter is relative with the on-resistance

of the switching power MOSFET. Therefore, the smaller on-resistance of power NMOS for better efficiency of voltage regulator is needed. In conclusion, the level shift circuit is needed for boost converter to convert the control signal from the lower supply voltage DV_{DD} to the higher input voltage V_{IN}. The circuit structure of level shift is shown in Fig. 48 [28]. The transistors M_{P1}-M_{P2} and M_{N1}-M_{N2} are as the buffer stage between V_{IN} to level shift. The transistors M_{P3}, M_{N3}, M_{PLS1}-M_{PLS2} and M_{NLS1}-M_{NLS2} forms the level shift coil circuit. The transistors M_{PH1}-M_{PH5} and M_{NH1}-M_{NH5} are utilized to offer a high driving ability for the large power MOSFET.

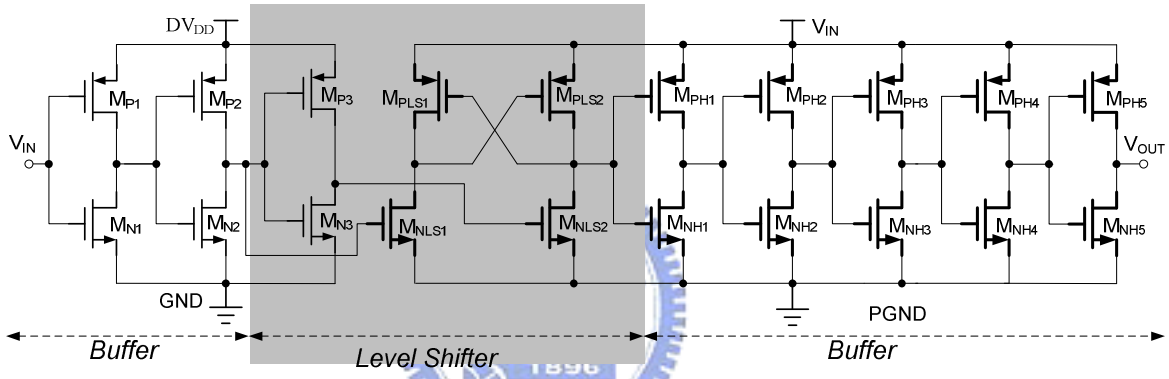


Fig. 48. Level shift buffer.

The simulation of level shift circuit is shown in Fig. 49, in which the rise time delay is 14.9 nano-seconds.

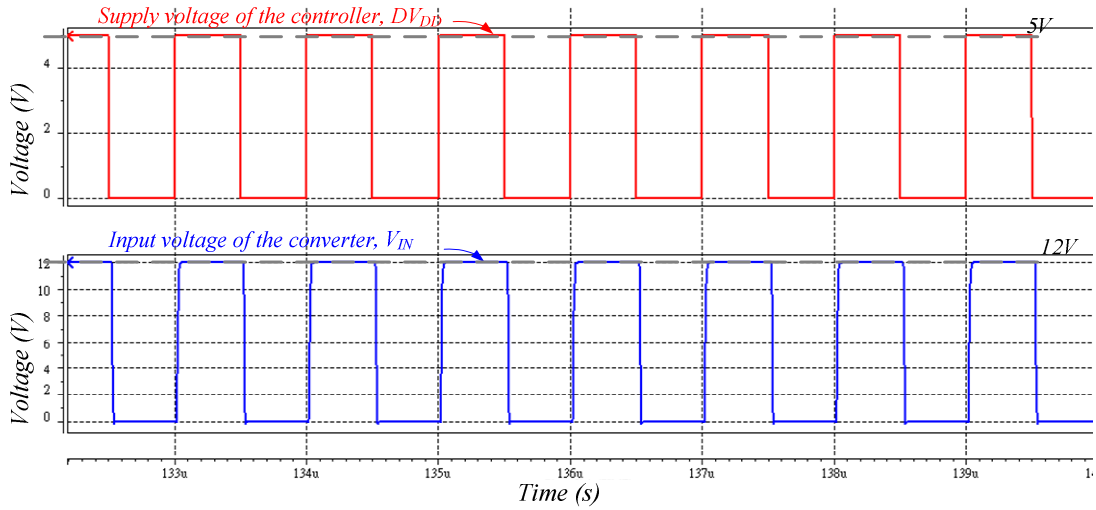


Fig. 49. The simulation result of level shift buffer.

4.6. Compensator Design

In order to allow an optimization loop dynamics of the switching converter, the design of compensator is important [19]. The current-mode boost converter produces an undesirable right-half plane (RHP) zero in the regulation feedback loop. Therefore, it requires compensation network to the regulator such that the crossover frequency occurs below the frequency of the RHP zero.

The right-half plane zero and one dominant pole of the conventional current-mode boost converter are determined by the following equation, where f_{domp} is the system dominant pole, $f_{Z(RHP)}$ is the right-half plane zero.

$$f_{domp} = \frac{2 \times I_{LOAD}}{2\pi \times V_{OUT} \times C_{OUT}} \quad , f_{Z(RHP)} = (1-D)^2 \times \frac{R_{LOAD}}{2\pi \times L} \tag{56}$$

In order to stabilize the regulator, the regulator crossover frequency should be less than or equal to one-fifth of the right-half plane zero and less than or equal to one-fifteenth of the switching frequency. However in heavy load condition, the frequency of RHP zero will be most close to low frequency position. Therefore, the compensator design should be considered in heavy load condition.

For the proposed boost converter, the pole and the RHP zero in the heavy load condition can be calculated as 338Hz and 900 kHz dividedly.

4.6.1. The concept of compensation resistance

Owing to the frequency response of the boost converter will be unstable without compensation. Therefore, the compensation resistance and capacitor is added to create the new dominate pole and the LHP zero to increase the stability.

The close loop gain of the switching converter can be written as:

$$A_L = \frac{V_{FB}}{V_{OUT}} \times (1-D) \times G_{M,EA} \times \left|Z_{comp}\right| \times \frac{1}{n \times R_{CS}} \times \left|Z_{OUT}\right| \quad (57)$$

Where A_L is the close loop gain, $G_{M,EA}$ is the error amplifier transconductance gain, Z_{COMP} is the impedance of the series compensation RC network, n is the current sense amplifier gain, R_{CS} is the current-sense resistance, and Z_{OUT} is the impedance of the load and output capacitor.

Due to the compensation impedance Z_{COMP} is dominated by the resistor and the output impedance Z_{OUT} is dominated by the impedance of the output capacitor at crossover frequency. Therefore, for solving the crossover frequency, the equation (57) is simplified as follow.

$$A_L = \frac{V_{FB}}{V_{OUT}} \times (1-D) \times G_{M,EA} \times \left|Z_{comp}\right| \times \frac{1}{n \times R_{CS}} \times \left|Z_{OUT}\right| = 1 \quad (58)$$

The compensation resistance R_{COMP} can be written as:

$$R_{comp} = \frac{2\pi \times f_c \times C_{OUT} \times n \times R_{CS} \times V_{OUT}}{V_{FB} \times (1-D) \times g_m} \quad (59)$$

The right-half plane zero of this work at maximum output current equals to 200mA is 900 kHz. The value of one-fifth of the right-half plane zero is 180 kHz and the value less than or equal to one-fifteenth of the switching frequency is 66 kHz. Thus, the crossover frequency of the converter f_c is selecting at 60 kHz. Therefore, by replacing the design values into equation (59) the compensation resistance R_{COMP} can be determined as 700 KΩ.

4.6.2. The concept of compensation capacitor

Owing to the compensation pole is determined by the compensation capacitor and the output resistance of the error amplifier. However, the output resistance of the error amplifier is usually much larger than the compensation resistance. Thus, the compensation pole must become the dominant pole of the converter.

Due to the compensation zero is dominated by the compensation capacitor. In order to make the system be stable, the compensation zero is select to be twice or triple frequency of the initial converter pole in the heavy load. Therefore, the compensation zero is set to be 1 kHz and the compensation capacitor can be determined by equation (60) and it is 16pF.

$$C_{comp} = \frac{2}{\pi \times f_c \times R_{COMP}} \tag{60}$$

Moreover, the compensation pole is 50 Hz to become the dominant pole of the system. Therefore, the phase margin of the converter is near 90^0 according to this design even if the proposed boost converter operating in the light load condition.

4.7. Soft-Start Simulation

The simulation result of the proposed soft-start technique for the designed boost converter is shown in Fig. 50. The operation principle had been mentioned in 3.1.2 and 3.2.4. In Fig. 50, the soft-start signal is controlled by the signal, *SS_END*. When the signal is at logic "1", the reference voltage, V_{REF}, will be charge gradually until 2V. Therefore, the reference voltage will be rose slowly during soft-start operation period.

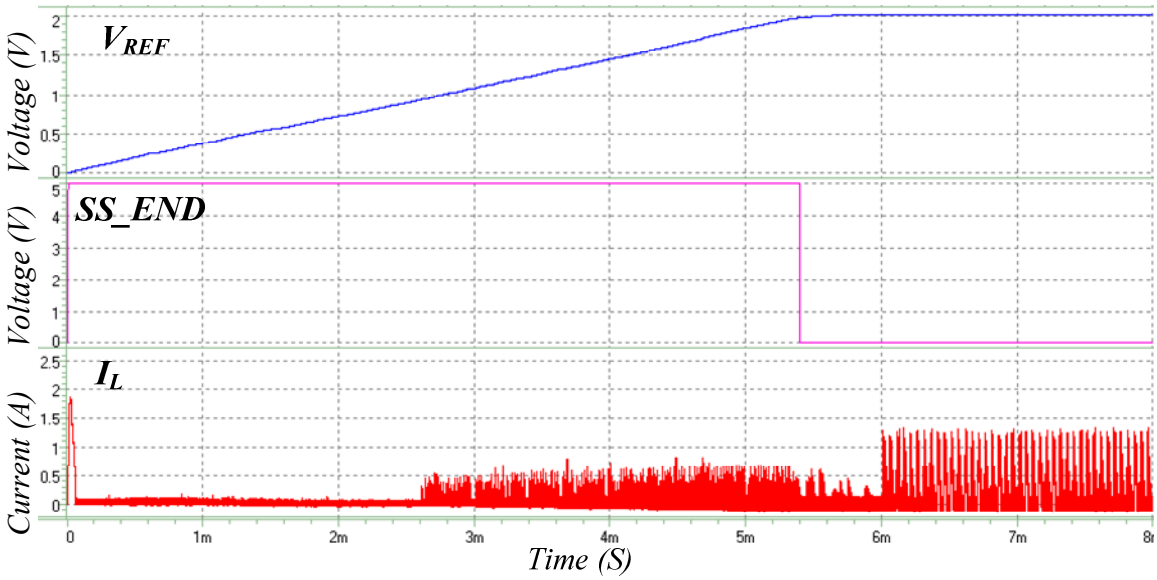


Fig. 50. Soft-start waveform.

4.8. Whole Chip Simulation

The whole chip simulation results of the designed LED driving circuit are shown in Fig. 52 to Fig. 59. In Fig. 52, it shows the relationship between output voltage and inductor current of the LED driving circuit. The output voltage of the boost converter (V_{out}) is tends to about 40V at steady state to offer a sufficient voltage to overcome the forward voltage of LEDs. In Fig. 52, the voltage drop of each LED string (V_{CH}) will be detected while the PWM dimming signal is at logic "1". And the head room of constant current sink circuit can be corrected into the load dependent window which mentioned in 3.3.2.

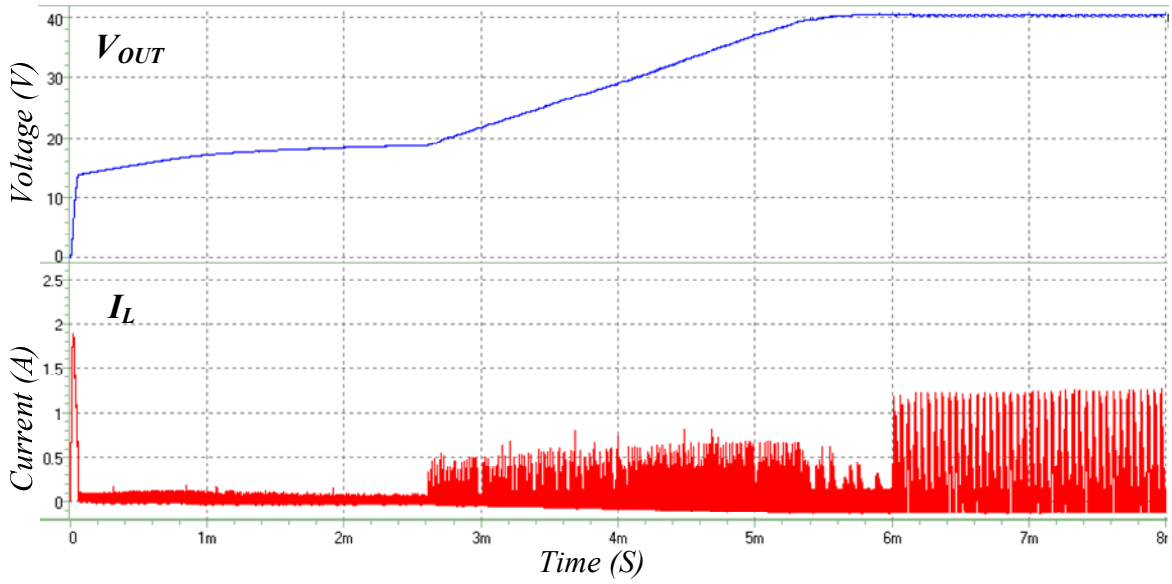


Fig. 51. The waveform of V_{OUT} and I_L with PWM dimming.

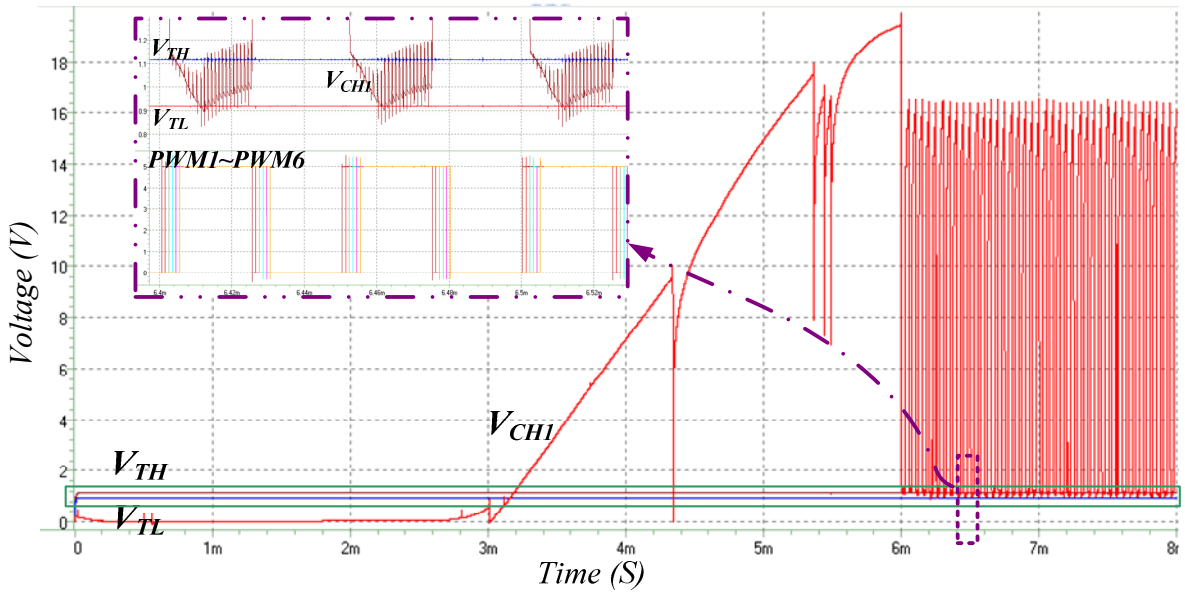


Fig. 52. The waveform of V_{CH}, V_{TH}, and V_{TL} with PWM dimming.

In Fig. 53, it shows the LED current of each string under PWM dimming frequency which is 20kHz. Owing to obtain 30mA current for each string the external resistor should be set to 67KΩ. During the on time of each sting, the current of LEDs are as the value what we defined.

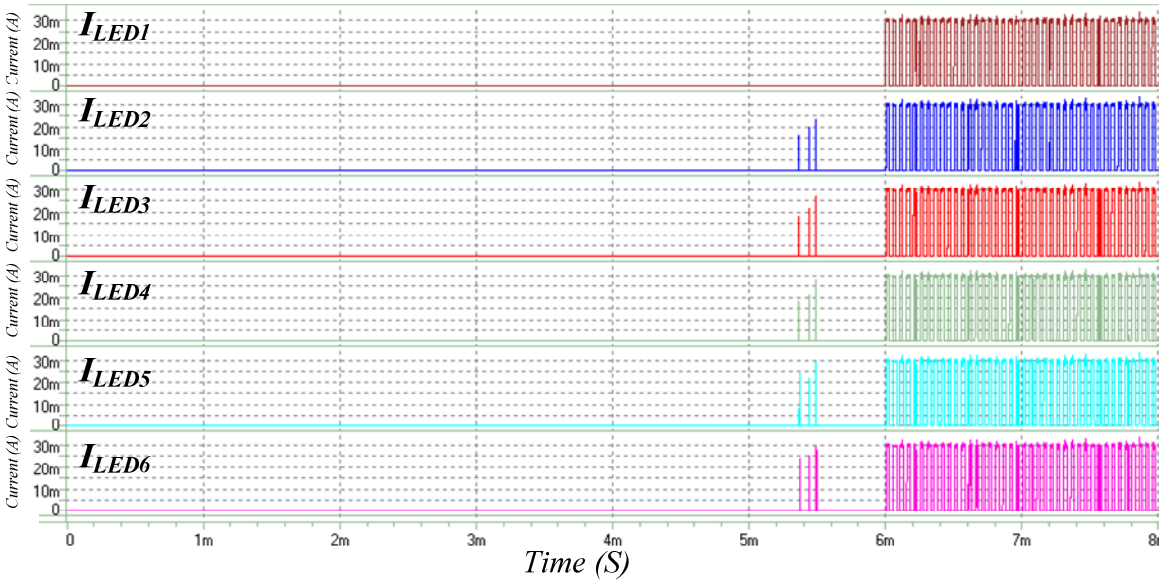


Fig. 53. The LED current with PWM dimming.

In Fig. 56, it shows the zoom in result of the 6.68ms to 6.87ms of Fig. 55. It can realize that the LED current of each string under PWM dimming in steady state.

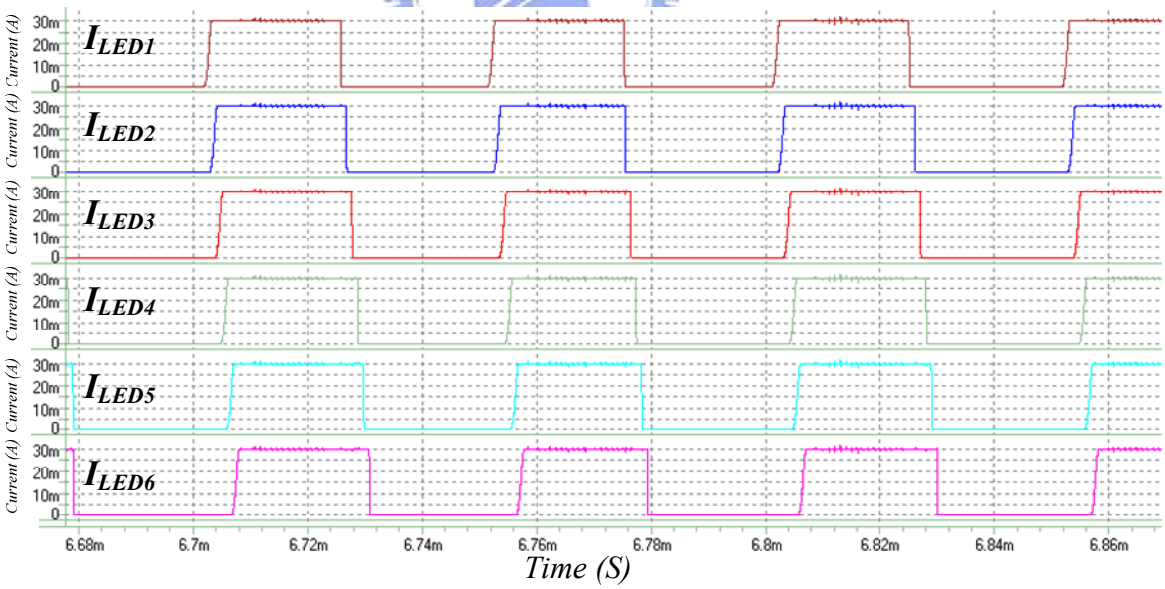


Fig. 54. The LED current with PWM dimming.

In Fig. 55 it shows the output of boost converter, LED current of 1st string and inductor current without PWM dimming. The output voltage of boost converter is at 40V. The LED current is 30mA per string by an external resistor which is 67kΩ.

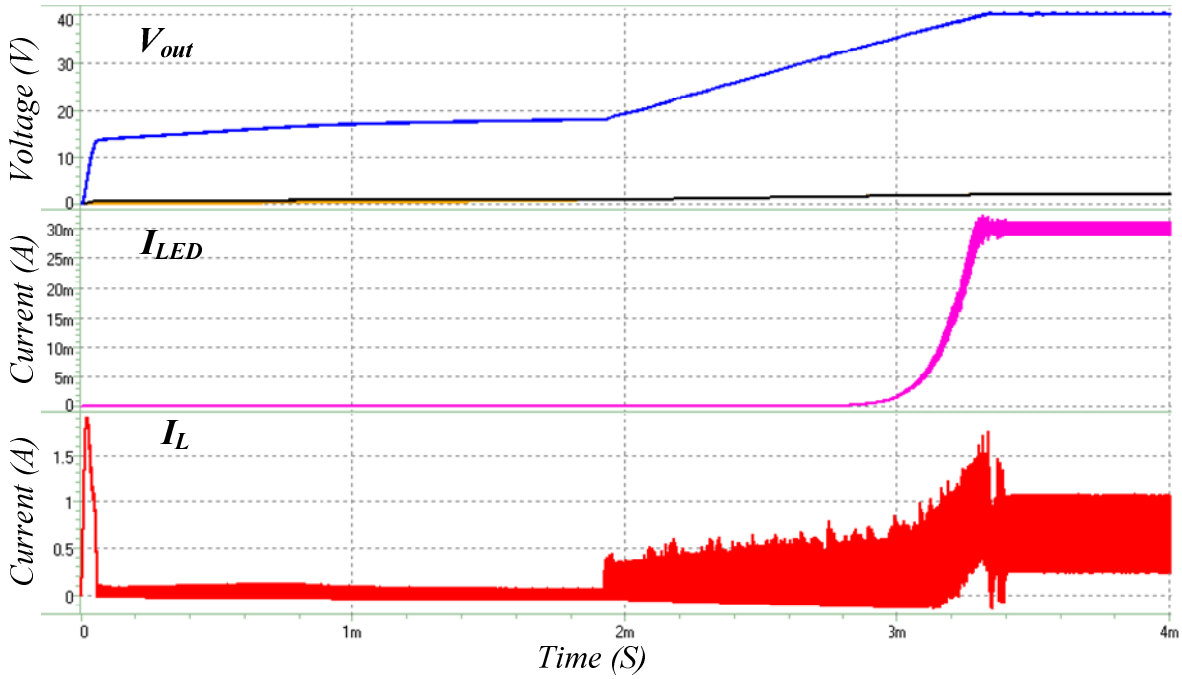


Fig. 55. The output of boost, LED current and inductor current without PWM dimming.

In Fig. 56, it shows the zoom in result of the 3.71ms to 3.8ms of Fig. 55. It can realize that the output of boost converter, LED current of 1st string and inductor current without PWM dimming are stable in steady state.

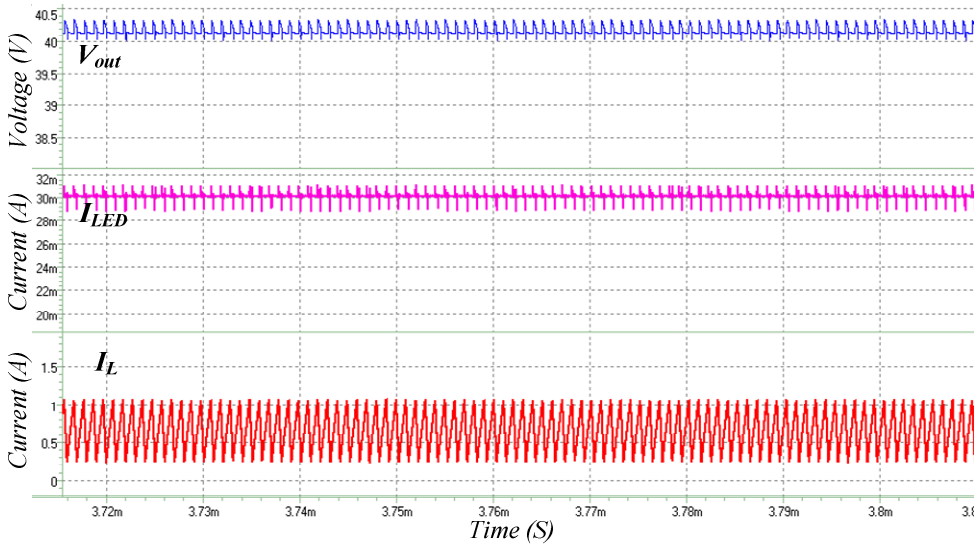


Fig. 56. Zoom in for 3.71ms to 3.8ms of Fig.53.

In Fig. 57, it shows the simulation results of V_{TH}, V_{TL}, V_{CH} and V_{REF}. The voltage levels

V_{TH} and V_{TL} are load dependent signal. In LED current of 30mA condition, the voltage level of V_{TH}, V_{TL} are 1.1V and 0.9V respectively. From the simulation result, it can realize that the minimum drain voltage, V_{CH}, has been corrected to the expectative window.

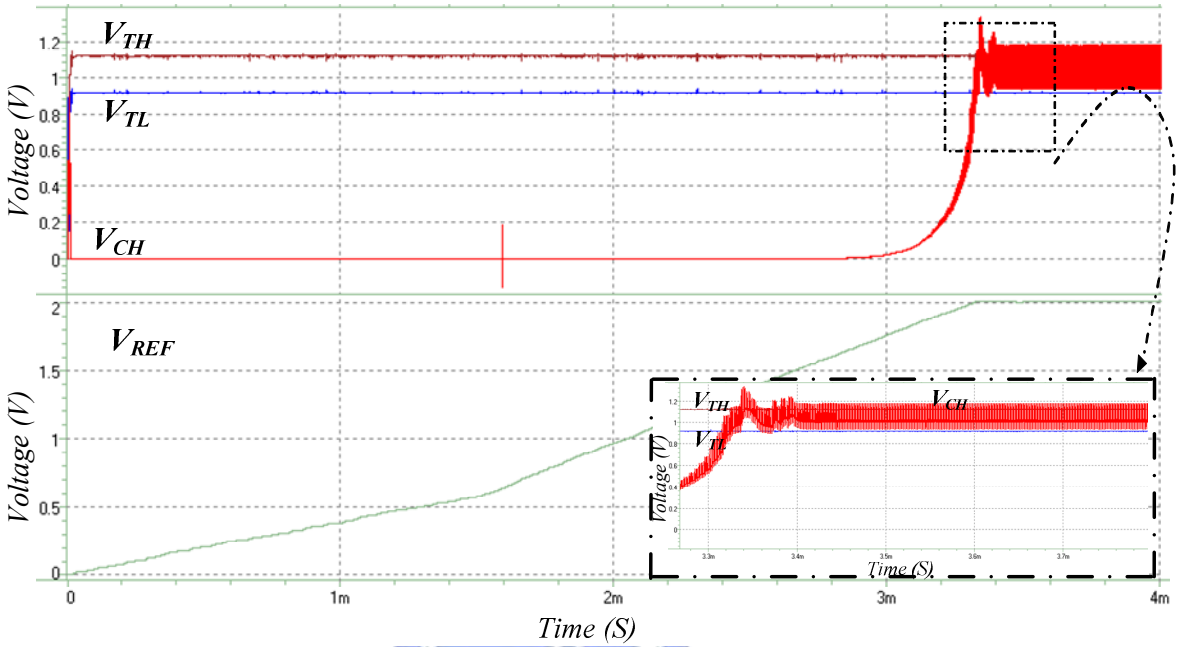


Fig. 57. Simulation results of V_{TH}, V_{TL}, V_{CH} and V_{REF}.

4.9. Load regulation, Line regulation

The performance of the proposed current mode boost converter, load regulation and line regulation will be shown as follow. The simulation results are shown that discuss the load regulation, line regulation respectively.

4.9.1. Line Regulation

The simulation result of line regulation is shown in Fig. 58. The supply voltage variance between 11V and 13V and the normal supply voltage is 12V. The line regulation is 18mV/V for 12V to 11V and 11V to 12V conditions of the design converter. The line regulation is 13mV/V for 12V to 13V and 13V to 12V conditions of the design converter. The line transition response time is 80 us and 70us for 11V to 12V and 12V to 13V conditions

respectively.

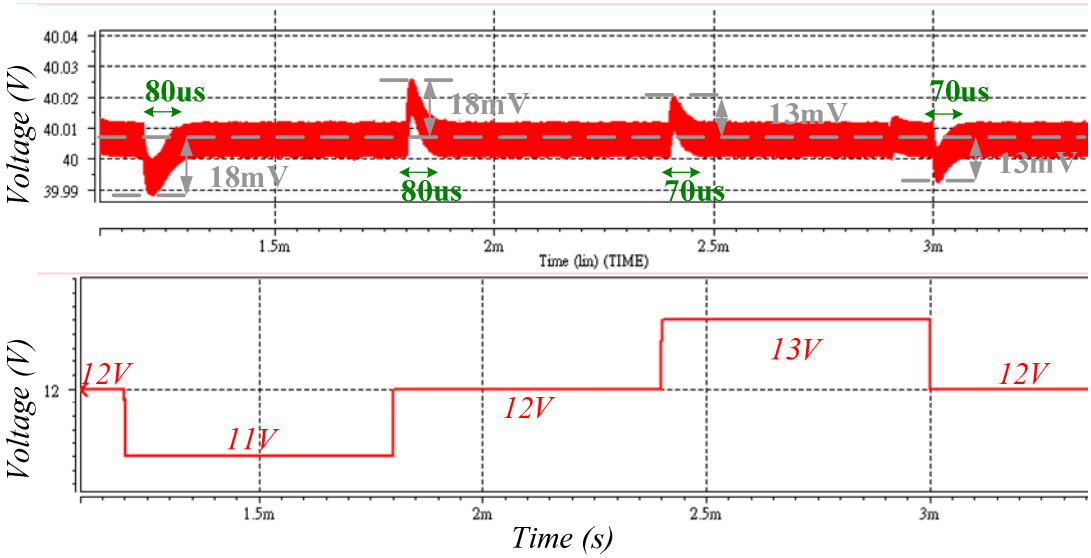


Fig. 58. Line regulation waveform.

4.9.2. Load Regulation

The load regulation of the design converter is shown in Fig. 59.

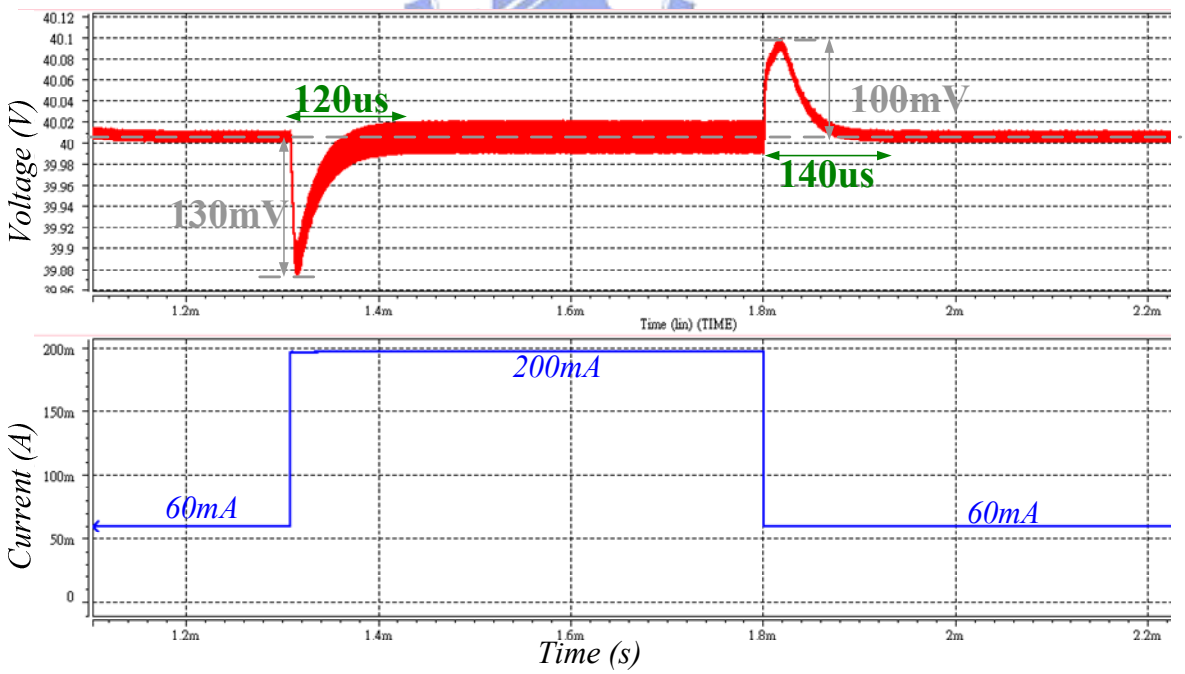


Fig. 59. Load regulation waveform.

The load condition transforms minimal load condition 60mA into maximal load condition 200mA. Therefore, the load regulation is 0.928mV/mA. The recovery time of the load transitions for heavy load to light load, light load to heavy load are 100us and 116us respectively. The recovery time for each condition is very close because the phase margin and the crossover frequency are almost the same for the different load conditions.

4.10. Die photograph

The proposed LED driving circuit with constant current sink circuit is implemented by the VIS CMOS 0.5 um process. The die photograph is shown in Fig. 60.

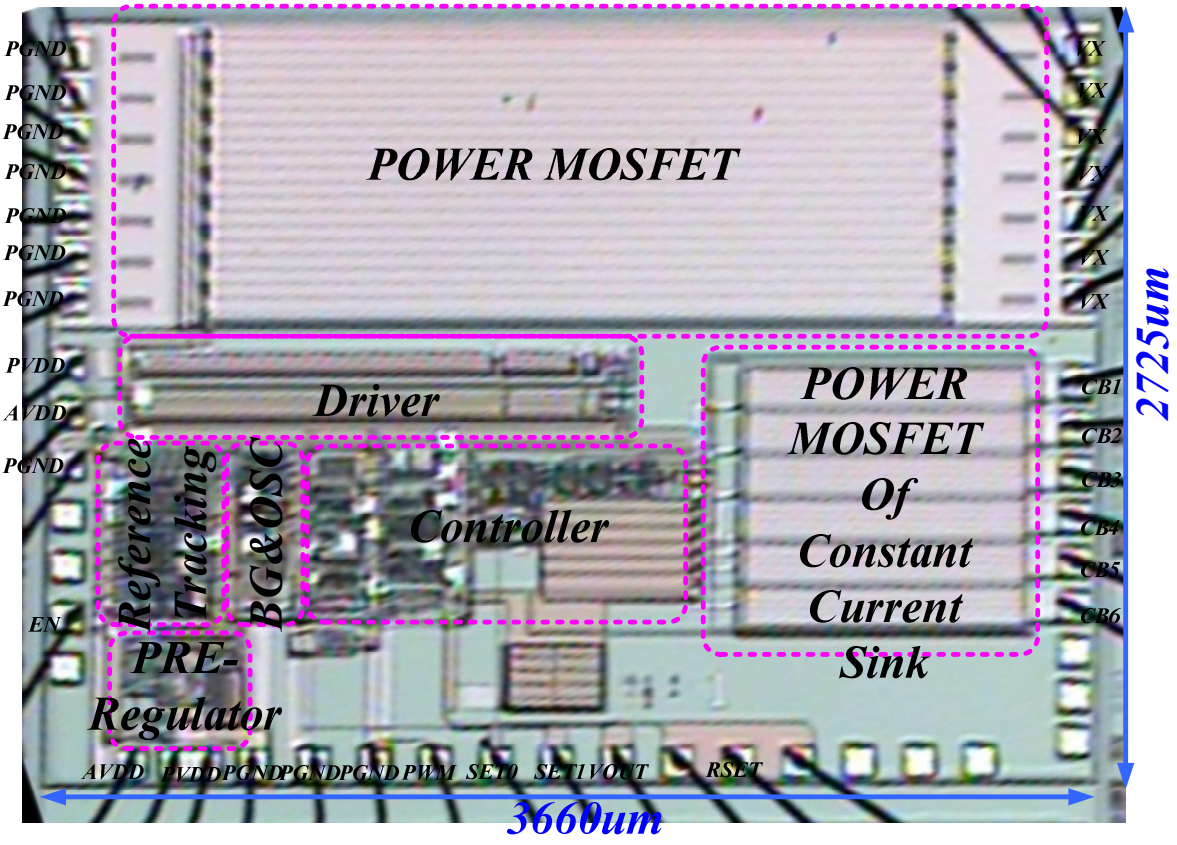


Fig. 60. The die photograph.

The chip size of the designed driving circuit is 3660 um * 2725 um. The power MOSFET must be large enough to reduce the on-resistance and endure the large inductor

current during heavy load condition. Another power MOSFET is for the LED strings to regulate the LED currents. In order to minimize the voltage drop on the constant current sink circuit and sustain the LED current, the power MOSFET should be large enough to reduce the gate-source voltage, V_{GS}. The sub-circuits are divided into four parts, such as reference tracking circuit, bandgap and oscillator circuit, controller and pre-regulator. The functions of each block are as mentioned in previous sections. The controller comprises ramp generator, voltage to current converter, current sensing, error amplifier, on-chip compensator and constant current sink unit.

Chapter 5

Conclusions, Experiment Results and Future work

5.1. Conclusions

The proposed circuit is a WLED backlight driver with an integrated 40V HV process to drive up to total 66 white LEDs. The regulator provides six-channel precise control of LED current with boost converter topologies.The circuit is simulated and fabricated by VIS 0.5um 2P3M 5V/5V and 40V/40V CMOS technology. The chip size is about 3.6 x 2.7 mm^2.

The output voltage of the boost converter can be reached to around 40V. The power stage is designed by asynchronous rectification with an off-chip Schottky diode. The on-chip soft start technique can prevent the using of a large off-chip capacitor. The proposed soft-start technique is implemented by the digital circuits as mentioned in Chapter 3.

The constant current sink circuit is designed with a load dependent minimum drain circuit. It is utilized to determine minimum drain voltage according to the situation of the current through LED stings. Through a load dependent minimum drain circuit can save unnecessary power loss at the constant current sink circuit.

The propose boost converter runs from an internally generated clock. The brightness of the LED strings is controlled by an external low frequency PWM control via the PWM pin. The normal operation temperature range is over -20℃ to 120℃.

In conclusions, the proposed driving circuit is suitable for the application such as display backlighting, LCD monitor, Notebook displays and LED accent lighting.

5.2. Measurement Module

The measurement module of the propose chip is as shown in Fig. 61. The proposed circuit and external elements are illustrated together to show the entire testing method. There are some key points should be concerned: The output capacitor should use low ESR capacitor to reduce the output voltage ripple. The low DCR inductor on the DC-DC converter is better to minimize switching current ripple and increase efficiency. The selection of Schottky diode should be fast switching and low forward-voltage to minimize power loss.

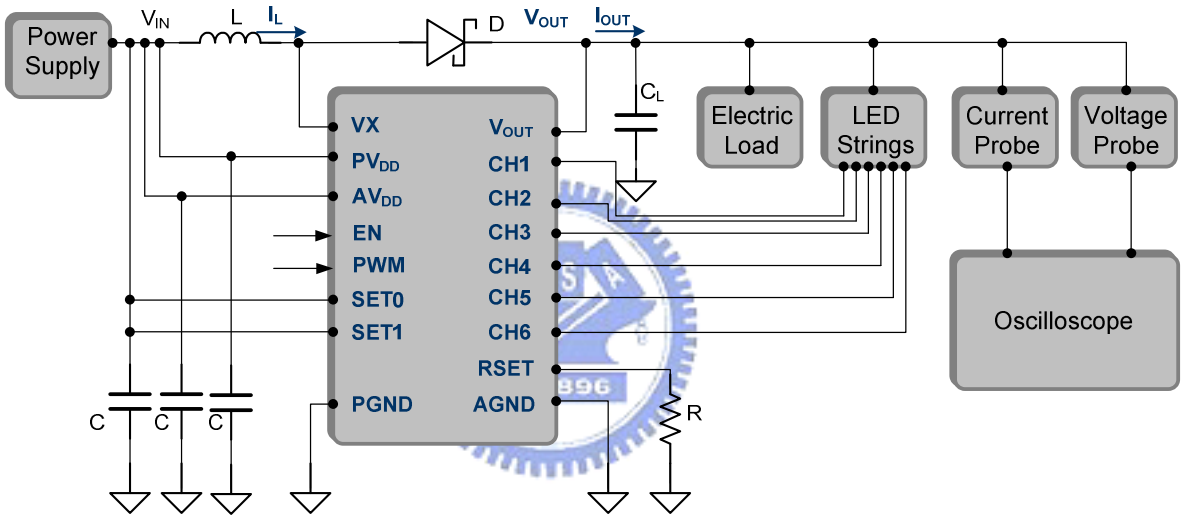


Fig. 61. The measurement module.

The power supply is utilized to offer the request voltage level. The electric load is as total LED string current and for load regulation measurement. The oscilloscope is to show the output voltage and output current waveform respectively.

5.3. Future Work

In this thesis, the proposed circuit only operates in PWM mode. The efficiency of converter is relative poor at light loads. Therefore, by means of the hybrid PFM/PWM operation the efficiency over a wide load range may be raised quite substantially. Furthermore,

the constant current sinking circuit is composed of a cascode structure in this thesis. However, a cascode structure suffers from a poor efficiency due to its' large voltage headroom. Therefore, the improvement of a better constant current sinking circuit is important in the future to enhance the efficiency. Finally, the fault detection is a critical issue in design of LED driver in order to enhance the reliability of the LED backlight system. Thus, the fault detection circuit such as open-loop, short circuit, over voltage, and over temperature should be added to the LED backlight system in the future.

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