使用 i 射線步進機的雙重圖形曝光技術以及其應用在元件製作之研究

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摘要

在本論文中，我們發展出一種新穎的技術可利用 i 射線(i-line)光學步進機來製作次世代小於 100 奈米的閘極圖形，並應用其來製作元件。這技術包含了兩次光學微影以及後續製程。因為它不會受到如同一般製程中的繞射效應，其複雜製程帶來的好處是突破一般 i 射線光學微影方法的解析度極限(~0.3μm)。這技術的解析度在本論文中已被證實可進展到約 80 奈米左右。數種非對稱源極/汲極元件在本論文中也用此技術來製作與分析，如穿隧式場效電晶體(TFET)以及非對稱式沿展之 N 型場效電晶體。

A Study on Double Patterning Technique with i-line Stepper and Its Application to Device Fabrication

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ABSTRACT

In this thesis, we have developed a novel double patterning technique utilizing an i-line stepper for the formation of sub-100nm gate patterns and implemented this technique to the fabrication of devices. This technique consists of 2-step lithography and following etch process to form the gate patterns. Reward for the complicated process steps is the shrinkage of resulted patterns beyond the resolution limit of the conventional i-line lithographic method (~0.3μm), since this technique doesn't suffer the diffraction effect encountered in conventional process. Resolution capability of this technique has been confirmed to improve at least to 80nm in this thesis. Several types of devices with asymmetrical source/drain structure, such as tunneling field-effect transistors (TFETs) and n-MOSFETs with asymmetric extensions, were fabricated with this technique and characterized in this thesis.

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謝瑞桀

誌於新竹交通大學

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Chapter 1
Introduction

1-1 General Background and Motivation

The invention of transistor has dramatically changed our life. Due to its relatively low cost, it widely replaces traditional mechanical devices in many fields, such as switch, amplifier, signal modulation and so on. For decades, the semiconductor industry has made huge success through various ways, but the most important one is device shrinking. According to Moore's Law [1], the number of devices on an integrated circuit (IC) doubles every 2 years, this trend has been confirmed through the scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) in the past few decades, therefore performance and density grow as the shrinking progresses.

To keep pace with Moore's Law, it requires innovation to overcome several fundamental physical barriers lying ahead, and the first of all is to extend the photolithography limit. According to the Rayleigh's theory [2], the resolution of a lithography system can be expressed as

$$R = \frac{k1\lambda}{NA} \quad \ldots\ldots(1\text{-}1),$$

where k1 is a system constant, λ is the wavelength of incident light, and NA is numerical aperture. From the equation, it's clear that the shorter wavelength we use, the higher resolution we get. Thereby the light source in the evolution of exposure tools has been changed from G-line (436nm), I-line (365nm), to excimer laser. Advanced lithography systems, such as e-beam and ion-beam, have also been proposed and adopted. But shortening the wavelength is not always useful. Conventional SiO_2 mask used in photolithography system would strongly absorb the light with wavelength shorter than 180 nm [2]. Besides, although e-beam & ion-beam lithography systems are capable of achieving fine resolution, they are not suitable for mass production due to the poor throughput of the direct patterning process. Back to Eq. 1-1, λ and NA are both natural characters of a stepper, changing these two factors implies a huge modification of the entire lithography system, the process may be costly. As a result, modern lithographic equipment for generating nano-scale patterns like 193 nm stepper is extremely expensive and usually not affordable for the laboratories in universities.

Examining what really limits resolution, Fig. 1.1 illustrates the collapse of the photoresist (PR) pattern. To expose a narrow line between two adjacent patterns, two open windows are designed in the mask as shown in the figure. During exposure,

incident photo-waves pass through the two windows, diffract and make constructive interference in the masked regions. Since the exposure light intensity is proportional to the square of wave amplitude, the PR underneath the fine line pattern of the mask may get exposed as the line width is sufficiently narrow to render a high light intensity. In order to solve this problem, in this work we develop a novel double patterning technique which uses a conventional I-line stepper to generate sub-100nm PR patterns and intend to use it to fabricate nano-scale MOS devices. As shown in Fig. 1.2, it consists of two times of lithographic and subsequent etching steps. First, we use mask 1 to define the left edge of a pattern. After the subsequent etching step, we use mask 2 to define the right edge of the pattern. Simply because the two edges are not defined at the same time, double patterning technique would not suffer from the aforementioned diffraction effect, thus a higher resolution can be achieved. The penalty is the additional mask and the process cost. However, the extra mask also provides more flexibility in device application than conventional process. For example, we may take advantage of such flexibility to fabricate devices having asymmetric source/drain structure, such as tunneling field effect transistors (TFETs), and MOSFETs with asymmetric S/D extensions.

1-2 Tunneling FET (TFET)

The suppression of short channel effects (SCE) is one of the most important requirements that come up with shrinking, because it determines the basic field effect properties of a transistor. While the channel length is decreased to an extent comparable to the depletion width of the source/drain junctions, the drain voltage would affect the carrier transport, leading to V_{th} roll-off, drain induced barrier lowing (DIBL), and bulk punch-through, thus the gate loses its controllability over carrier conduction. For conventional transistors the subthreshold swing (SS) and maximum depletion width of the channel, *Wdm*, are expressed as follows:

$$SS \approx \ln 10 \frac{kT}{q}\left(1+\frac{C_d+C_{it}}{C_{ox}}\right) \quad \text{.....(1-2),}$$

$$Wdm = \sqrt{\frac{2\varepsilon_s(2\varphi b - Vbs)}{qNa}} \quad \text{.....(1-3),}$$

Where q is the electronic charge, k is the Boltzmann's constant, T is absolute temperature, C_d is the depletion capacitance, C_{it} is the capacitance of the interface states, C_{ox} is the oxide capacitance, ε_s is the silicon permittivity, φb is the Fermi potential with respect to the midgap, Vbs is the substrate bias, and *Na* is the substrate doping concentration. As indicated in Eqs. 1-2, 1-3 and Fig. 1-3, an increase in channel doping could reduce the depletion width and increase C_d, it is therefore a trade-off between SCE immunity and SS. To untie this Gordian Knot, it needs a new

device with different transport and operation mechanisms.

The concept of TFET was brought out around 1990 and called surface tunneling transistor at that time [3]~[5]. As its original name, TFET makes use of band-to-band tunneling (BTBT) as carrier injection mechanism. Basically, the device is a gated P-I-N diode under reverse bias, as shown in Fig. 1.4. For a TFET in off-state, the tunneling barrier between source and drain (or channel) is very wide, preventing the occurrence of tunneling. Thus, in principle only an extremely low current dominated by the reversed-biased leakage current of the P-I-N diode exists in the off-state. While the applied gate voltage is sufficiently high the energy band near the surface in the channel region is significantly lifted or lowered, resulting in the formation of a tunnel point adjacent to the source or drain. At this point the tunneling width is narrow and the tunnel probability becomes high. The polarity of gate voltage decides the location of the tunneling junction (near source or drain). This makes TFET an ambipolar conduction device. (see Fig. 1.5(b)). The conduction mechanism relies on the tunneling barrier width rather than the formation of an inversion channel, therefore it does not experience the same physical limitation in MOSFET. According to Eq. 1-4 given below [6], there are two terms that should be increased to reduce SS:

$$SS = \ln 10 \left[\frac{1}{V_{eff}} \times \frac{dV_{eff}}{dV_{GS}} + \frac{\xi + b}{\xi^2} \times \frac{d\xi}{dV_{GS}}\right]^{-1} \quad \text{.....(1-4).}$$

In the equation the first term describes how the gate-to-source voltage (Vgs) controls the tunnel-junction bias (Veff) and suggests the use of ultra-thin body and high-*k* dielectric would help. The second term stipulates the relationship between Vgs and tunnel junction electric field, it's a complex coupled term that doesn't provide a single way to improve device performance.

To view SS from a different perspective, as pointed out previously [7]~[9], the SS of a TFET is also expressed as in Eq.1-5:

$$SS = \frac{V_{GS}^2}{2V_{GS} + B_{kane} W_g^{3/2} / D} \quad \text{……(1-5)}$$

where Wg is the tunneling barrier width, D is a function of structural parameters and Vds, and B_{kane} is in general a function of carrier effective mass but assumed constant here. This equation indicates SS have strong dependence on Vgs but weak dependence on Wg, implying that SS could ideally reduce to zero as Vgs goes to zero. Equation 1-5 confirms TFET's sub-60mV/dec SS character, as have also been demonstrated in related simulation results [6][10], making sure that TFET is a strong candidate for next generation device to replace MOSFET.

Although the basic idea of TFET seems so easy to implement, however, most related papers are still limited to device simulation or theory development [11]~[15], and only few experimental reports [16][17] support the potential of such kind of

device. It was not until 2007 [18] that the first silicon- based TFET with SS below 60mV/dec was achieved by mesa structure. The main obstacle of TFET is the low on-current, which is at most only one-tenth of a MOSFET's at 90 nm node. One of the reasons results from the difficulty of precise control of source/drain doping profile. It needs junction concentration > 10^{19} cm^{-3} for significant BTBT to occur. Without abrupt source/drain junction, the tunneling width would become long. According to Eq. 1-6 [7] given below, an increase in tunneling width makes exponential decrease in conduction current.

$$I_{DS} = A_{kane} D^2 W_g^{-1/2} V_{GS}^2 e^{-(B_{kane} W_g^{3/2})/(V_{GS} D)} \quad \ldots\ldots (1\text{-}6)$$

Also the effective tunneling area is a concern. The schemes shown in Fig. 1.5 represent an ideal case near the surface region, while the band in deeper region may not be so sensitive to gate voltage, thus there would be not enough tunneling area to gain higher conduction current. In addition, the rather large bandgap of Si also limits the performance of TFET built in Si-based materials.

To solve these problems, beside abrupt junction engineering, many modified TFET structures are proposed. Tunnel Source(PNPN) n-MOSFET [19]& Green Transistor [20] are promising to solve the problems mentioned above. Recently a Si TFET with 42 mV/dec was reported [21], these showed the competitiveness of the TFETs.

1-3 N-channel MOSFETs with asymmetrical S/D extensions

Device designer should consider not only electrical behavior but also reliability. Among various reliability issues, hot carrier effect (HCE) is one of the most critical problems [22][23]. As described in [24] ~ [26] and illustrated in Fig. 1.6, as the gate voltage is higher than threshold voltage, an inversion layer is formed in the channel. When the device is operated in the saturation region with a high drain bias, pinch-off of the inversion layer occurs near the drain side, and most voltage drops across this region between the pinch-off point and the drain junction, wherein a high electric field is resulted. The carriers drifting from source to drain could gain significant energy from such high field, and portions of them would become hot carriers. Hot carriers may generate electron-hole pairs via impact ionization. These generated carriers produce a high substrate current which may turn on the parasitic bipolar device, leading to snapback breakdown [27]. Moreover, parts of the hot carriers could surmount the energy barrier at Si/dielectric interface and inject into the gate dielectric, leading to the generation of oxide trapped charges and interface states, and deteriorating electrical characteristics of an MOSFET. According to the mechanisms mentioned above, the location of damaged region is close to the drain side [28]. For devices with continuous scaling, the HCE damaged region progressively occupies a

large ratio of the channel region. More serious HCE degradation is thus expected in smaller transistors. The lightly doped drain (LDD) structure [29]-[31] has been widely evaluated and implemented to solve these issues. It's a structure with a narrow, self-aligned n^- region between deep source/drain and channel. LDD could reduce HCE by spreading the high field at drain pinch-off region into n^- region.

However, with the scaling to sub-0.18 micron node and beyond, the reduced drain voltage results in much reduced HCE, and it becomes not necessary to employ LDD. Substituting for HCE, SCE and parasitic resistance raise represent more important concerns in future scaling. It needs a shallow junction to suppress SCE but a high doping concentration ($> 10^{20}$ cm^{-3}) to reduce parasitic resistance. Combining the two approaches, shallow source/drain extensions have been adopted in modern nano-CMOS manufacturing (Fig. 1.7). The shape and structure of shallow source/drain extension are almost the same as the LDD structure except a very high doping concentration is adopted in lieu of the n^- region in the LDD, thus it could easily be implemented in conventional device fabrication. Depending on what kind of properties we desire on the devices, optimization of source/drain extensions is the key to achieve the target.[32]~[34]

The asymmetric-extensions MOSFET comes into our notice. Reviewing HCE

mechanism mentioned above, LDD is only needed on the drain side, the use of lightly doped source with higher resistance comes from the simplicity and economical consideration of self-aligned process. Optimization of the source and drain extensions separately in principle should benefit the device performance. Most reported asymmetric MOSFETs made by standard process have their own issues. As illustrated in Fig. 1.8, the asymmetric LDD structure is made by using additional implantation masks or shift of gate mask, followed by formation of selective oxide deposition [35][36]. The scaling capability of the above process is still limited by the lithographic requirement. Even worse, it experiences an alignment problem obviously, making the scaling an issue. The self-aligned asymmetric structure (SAAS) [37] was proposed to solve the aforementioned problem. The effective channel length of transistors with SAAS is down to 100nm in that report. However, the necessary use of H_3PO_4 is a issue. We thought the selectivity of H_3PO_4 would damage the gate oxide, the yield of the transistors with SAAS would not be good. Implementation of tilt implant in [38] made it difficult to identify how the source and drain extensions affect SCE. With the help of double patterning technique, we could easily fabricate optimized S/D extensions in asymmetric MOSFET without aforementioned issues, the resolution could increase without degradation of the yield. This would help clarify what roles the source and drain extensions act in affecting the device performance.

[39]

1-4 Thesis Organization

This thesis is divided into four chapters. Introduction in Chapter 1 is already given above. In Chapter 2, we describe experimental design, device fabrication, and measurement setup. The electrical behavior of devices are presented and discussed in Chapter 3. Finally we sum up the results and propose some future works in Chapter 4.

Chapter 2
Device Structure and Process Flow

All device fabrications mentioned in this chapter were carried out at the National Nano Device Laboratories (NDL).

2-5 Feasibility of Double Patterning Technique

To realize the ideas mentioned in Chapter1, it's necessary to ensure the feasibility of Double Patterning Technique. For all lithographic steps, we used an i-line stepper (Canon FPA-3000i5+) to generate the photoresist (PR) patterns. Fig. 2.1 is the design of the 2-step gate masks that we used in this thesis. We used scanning electronic microscope (SEM), in-line SEM, and focused ion beam (FIB) SEM to check the structure formed by Double Patterning Technique. Fig. 2.2 and Fig. 2.3 are top view photos taken from our first test run. The practical gate length didn't fit well our designed values because of too much exposure dose we used at that time. After fine tuning the conditions, Figs. 2.4 and 2.5 show that Double Patterning Technique did work with the optimized stepper parameters. It also demonstrated the capability of

this approach to shrink the gate length beyond the resolution limit of single patterning technique (~0.3 μm) with conventional i-line steppers. However, in Fig. 2.6 we can see a rather thick white line along the right gate edge in the SEM pictures taken on some of the prepared samples. These white lines are believed to be due to the tapering of the sidewall, and can be improved by adjusting the plasma etching condition. Except this etching issue, the gate length is almost the same as the design set. These results confirm the feasibility of Double Patterning Technique for fabrication of devices with much reduced feature size. However, Double Patterning Technique is still limited by the overlay accuracy of the stepper. In this study the shortest gate length achieved was 42 nm (Fig. 2.7) with designed length of 30 nm. Actually, most lines designed below 80 nm are out of control and not easy to reproduce, and the practical length falls in the range between 60 and 70 nm (Fig. 2.9). According to Table1 (Specifications of the employed Stepper. Data are courtesy of NDL), the observed results look reasonable, since the overlay accuracy is larger than 45 nm. From the above results, we believe that the double-patterning of an i-line stepper should be a reliable approach for generating 80 nm gate length.

2-6Fabrication of TFETs

The purpose of this experiment is to confirm the feasibility of Double Patterning Technique for TFET fabrications, and to distinguish how p-type source concentration affects the characteristics of TFETs. We first fabricated single-crystal TFETs on single 6-inch (100) p-type wafers with resistivity of 15~25 Ω-cm, and the wafer thickness is 660-690 μm. The process flow is illustaretd in Fig. 2.10. Standard local oxidation of silicon (LOCOS) process with channel stop implant (BF_2^+ at 120 kev and $4x10^{13}$ cm^{-2}) was used for device isolation. Note that the active regions did not receive anti-punchthrough or threshold voltage (Vth) adjustment implant. After RCA clean, 2.5 nm N_2O thermal gate oxide and 100nm in-situ n-doped poly-Si were formed by vertical furnaces. After double patterning gate 1 lithography, and subsequent etching, n-type drain formation was performed with As^+ implantation at 10 keV and $5x10^{14}$ cm^{-2}. Next, double patterning was performed for gate 2 definition. A BF_2 implantation with split conditions shown in Table 2 was then used to form the p-type source. Afterwards, substrate contacts were formed by etching through the isolation oxide and then implanting the substrate windows with BF_2^+ at 40 keV with a dosage of 5e15 cm^{-2}. A 1000 ℃ spike rapid thermal anneal (Spike RTA) was subsequently applied for dopant activation in nitrogen ambient by a Korona RTP 800 system. Afterwards, standard back-end process was carried out. All wafers were then capped with a 500

nm TEOS passivation layer by plasma enhanced chemical vapor deposition (PECVD) system. After contact hole etching, 600 nm Al-Si-Cu deposition and patterning were performed. Finally, an H_2-sinter at 400 ℃ for 30 min was performed to mend the dangling bonds and to reduce interface state density at gate oxide/Si interface.

We've also fabricated and characterized poly-Si TFETs based on the double patterning process. The process flow is illustrated in Fig. 2.11. Firstly a 200 nm wet-oxide was grown on all wafers followed by low pressure chemical vapor deposition (LPCVD) of 50 nm intrinsic amorphous Si. After solid phase crystallization (SPC) performed at 600 ℃ for 24 hr, the crystallized poly-Si was patterned to form the active regions. Then a 16 nm LPCVD TEOS oxide, a 150 nm in-situ n-doped poly-Si, and a 50 nm LPCVD TEOS oxide were deposited sequentially to serve as gate oxide, gate electrode, and hard mask, respectively. The following process steps were varied to fabricate different types of devices, namely, conventional TFTs, TFETs, as shown in the Fig. 2.10. For TFTs, the S/D regions were implanted together after 2-step gate definition process. For TFETs, it was basically the same process flow as that for single crystal TFETs described in Fig. 2.10. Table 3 summaries the implantation conditions for the two kinds of devices. Dopant activation of aforementioned device was carried out in nitrogen ambient at 900 ℃ for 30 sec. Subsequent passivation oxide and metallization were the same as that described for

TFET on Si wafers.

2-7Fabrication of N-channel MOSFETs with Asymmetric Extensions

All theses devices were fabricated on single 6-inch (100) p-type wafers with resistivity of 15~25 Ω-cm. The process flow is illustrated in Fig. 2.13. First the p-typed well was formed by BF_2^+ implantation at 70 keV and 1e13 cm^{-2}. Well drive-in was carried out at 1100 ℃ for 12 hr. Then standard LOCOS process with channel stop implant (BF_2^+ at 120 keV and $4x10^{13}$ cm^{-2}) was used for device isolation. Vth adjustment and anti-punchthrough implantation steps were done by implanting BF_2^+ (40 keV, 1e13 cm^{-2}) and B^+ (35 kev, 5e12 cm^{-2}), respectively. After RCA clean, a 3.7 nm N_2O thermal gate oxide and a 150 nm in-situ n-doped poly-Si were formed by vertical furnaces. Asymmetric extensions were then formed separately after gate 1 and gate 2 definitions. For control samples with symmetric S/D extensions, the implantation was done together after 2 step gate definition. The implantation conditions of aforementioned devices are shown in Table 4. After 80 nm LPCVD TEOS spacer formation, deep S/D was implanted with As^+ at 25 keV and 3e15 cm^{-2}. Then substrate contacts were formed by etching through the isolation oxide and then

implanting the substrate windows with BF_2^+ at 40 keV with dosage of 5e15 cm^{-2}. Dopant activation of was carried out by RTA at 1000 ℃ for 30 sec in an N_2 atmosphere. Afterwards, dielectric passivation and metallization steps were the same as those described in the former section were performed.

2-8Measurement Setup

In this study the electrical characteristics of the fabricated devices were all evaluated by a measurement system regulated by a personal computer. The system consists of an HP-4156A parameter analyzer for I-V measurement, an HP 4284A LCR meter for C-V measurement, an Agilent-E5250A switch, an Agilent-8110A pulse generator, and a temperature-regulated hot chuck. Interactive Characterization Software (ICS) is used to setup all the measurement conditions.

Table 1 Specifications of Canon FPA-3000i5+ Stepper.

Resolution	0.35 micron (dense lines)
NA	0.63 – 0.45 (automatically variable)
Reticle Size	5-inch
Reduction Ratio	5:1
Field Size	20 mm x 20 mm
Overlay Accuracy	Mean + 3 sigma ≦ 45 nm
Throughput	100 wph (200 mm)

Table 2 Split conditions for p-type implant condition of the single-crystal TFET.

P –type source BF_2^+ , 10 keV	2e14 cm^{-2}
	4e14 cm^{-2}
	6e14 cm^{-2}
	8e14 cm^{-2}
	1e15 cm^{-2}

Table 3 Split conditions for poly-Si thin film devices.

TFT	BF_2^+ 5e15 cm^{-2} , 40 keV

TFET	Drain: As^+ 5e15 cm^{-2} ,40 keV
	Source: BF_2^+ 5e15 cm^{-2} , 40 keV

Table 4 Split conditions for n-MOSFETs with asymmetric extensions.

Symmetric Extension As^+	1e15cm^{-2}, 15 keV

Asymmetric S/D Extensions As^+	
Source Extension	1e15 cm^{-2}, 20 keV
Drain Extension	1e14 cm^{-2}, 10 keV
	1e15 cm^{-2}, 10 keV

Chapter 3
Results and Discussion

3-1 Issues of Double Patterning Technique

Although we have confirmed the feasibility of double patterning technique in Chapter 2, there are some issues encountered in our process, and most of them arise from the 2-step etching. The actual gate length was extracted by the top-view images taken by in-line SEM. As shown in Fig. 3.1, the fluctuation (1-σ standard deviation) is about 30 nm, which is too high for the fabrication of nanoscale devices. Another issue illustrated in Fig. 3.2 coming from the mask design is probably the most critical problem encountered in this work. For conventional process, the gate definition only needs one etching step and the etching process could stop automatically with the aid of end-point detection (EPD) technique. It should be noted that the EPD requests a large etch area for sufficient optical signal collection, and the conventional process usually meets the requirement. For double patterning technique, although the area of the poly-Si film to be etched is the same as that of conventional process, most of them is removed during the first etch step and only a tiny portion left for etching in the second etch step, as shown in Fig. 3-2. Therefore the EDP signal is too weak to be detected. As a result time-mode was performed for the second etch step, and potential

issue related to the control of etch process may occur. This indeed happens! Fig. 3.3 represents a fabricated MOSFET showing a damaged drain region. Electrical characteristics of the damaged MOSFETs are shown in Fig. 3.4. The device with long channel (Lg = 5 μm) shows degraded current drive implying a high series resistance, while the short-channel one (Lg=0.5 μm) exhibits high gate leakage. All these phenomena are believed to be related to the formation of "cliff" circled in Fig. 3-3. With zero-angle implant, portions of the sidewall of the "cliff" cannot receive the implant and a considerable resistance is thus introduced, leading to the degradation in drain current. Moreover, the edge of gate oxide near the drain side may also be damaged during etching, resulting in the high leakage issue in short-channel devices, as shown in Fig. 3-4(b). Fig. 3.5(a) ~(d) are the SEM images showing the situation at the twos sides of patterned gates with different gate length. As can be seen in the figures, the necking phenomenon, i.e., shrinkage of gate dimension, occurs near the edge between active region and the LOCOS. This would further make the effective gate length differ from the gate length extracted by SEM images. It was not easy to find the necking from the PR patterns generated before the 2 step etching (Fig. 3.6 (a)). From the PR patterns generated with conventional single patterning process shown in Fig. 3.6(b), it clearly indicates the necking comes from the narrowing of PR pattern located in the regions close to the boundaries between LOCOS and the active

region. Such necking phenomenon is presumably related to the non-planar topography of the LOCOS structure.

3-2Electrical Characteristics of TFETs

The dependence of Id on channel length is quite different between conventional MOSFETs and TFETs. For the latter devices, Equation 1.6 shows the current is independent of channel length, although in a related simulation study [40], the results pointed out the conduction current would drop slightly due to the higher resistance of longer channel. Fig. 3-7 and 3-8 show and compare such channel-length dependences of the two kinds of devices built on bulk Si and poly-Si, respectively. For all the measurements on the TFETs, we define the n^+ region as drain and the p^+ region as source. As can be seen in those figures, for both n-channel MOSFETs and p-channel TFTs, Id strongly depends on the gate length. Such dependence is especially true for the MOSFETs shown in Fig. 3-7(a), in which severe short-channel effects as evidenced by the significant increase in the subthreshold leakage is observed. On the other hand, the characteristics of the TFET devices, either built on bulk-Si or poly-Si, essentially show little dependence on the channel length. In Fig. 3-8(b), poly-Si TFETs show a little Id drop with increasing Lg at high positive Vg. Beside the reason

of channel resistance mentioned above, we thought it might also be related to the nature of poly-Si. Although tunneling is independent of channel length, but the tunneling carriers would be retarded by defects contained in the channel. This effect has less influence on holes due to higher effective mass, so as represented in Fig. 3.8(b), it shows little length dependence only in positive Vg region.

Fig. 3.9 and 3.10 show the output characteristic curves of single crystal TFETs with gate length of 0.2 μm and 1 μm, respectively. When Vds is negative, the PIN diode is under forward bias and the gate voltage doesn't have any controlability in modulating the drain current. Therefore TFETs are operated at Vds > 0V. In the figures the drain current is not zero at zero drain bias. This is caused by the existence of gate leakage current due to the etch-induced recess issue mentioned in last section. Moreover, it's also noticeable that the conduction current isn't competitive with the MOSFETs. This might be related to the weak field strength at the tunneling junction which can be optimized with further optimization in structural parameters, such as the oxide thickness and channel thickness [9][10]. Another major factor is the small effective area of the tunneling junction which is located very close to the channel/oxide interface. New structures have been proposed for addressing such issue. [19][20].

As illustrated in Fig. 3.11, we set the gate floating and applied voltage at the source side to distinguish the relationship between channel conductance and channel length. For those TFETs with designed gate length shorter than 0.1μm, all the characteristics behave like a leaky PN junction, which implies that there is negligible intrinsic region under gate. Therefore 0.1 μm is a critical length for our devices and thermal budget of the fabrication should be re-examined to improve the device performance. The shortest gate length of TFETs with reproducible characteristics is 0.2 μm. The transfer curves of a TFET with gate length of 0.2 μm are shown in Fig. 3.12. Note the device was fabricated later than those discussed in Fig. 3.9, and the gate leakage is about 10^{-13} A. In the figure Vds is fixed at -1.25 V, and the drain bias is increased from -0.25 V to 0.75 V with step of 0.25 V. We can see in the figure that these transfer curves are parallel and shift with respect to the adjacent ones by 0.25 V, consistent with the trend reported by Wang et al. [17]. The min SS denotes the minimum value of SS in the entire substhreshold region, the avg SS denotes the average value of SS in the range of drain current between 10^{-11} A and 10^{-9} A. In the figure the lowest min SS and ave SS are 231 mV/dec and 367 mV/dec, respectively.

Next we shift our attention to the poly-Si TFET devices. With the same procedure carried out in Fig. 3.11, the shortest devices available for characterization are with Lg of 0.5 micron. This is attributed to the high diffusivity of the dpaonts in

the poly-Si. Fig. 3.13 and 3.14 are the output characteristics of a poly-Si TFET with gate length of 1 μm under p- and n-channel modes of operation. The higher Id with positive Vg represents the difference of effective mass between electrons and holes. The transfer curves of the device are shown in Fig. 3.15. It clearly shows the ambipolar conduction characteristics of TFETs. Note that we define the current at Vg = 0V as the off-current and the one at Vg = 6V as the on-current for NTFETs. At Vds = 2V, the min SS is 698 mV/dec, avg SS is 1070 mV/dec, and on/off ratio is about 10^5.

3-3 Electrical Characteristics of N-channel MOSFETs with Asymmetric Extensions

Fig. 3.16 shows the cross-sectional view of a 0.3 μm MOSFET, showing an ultra-shallow trench in the drain region. The region indicated by the arrow corresponds to the damaged region caused by etch, as identified in Fig. 3.5. Such unexpected damage encountered has resulted in impact on the fabricated NMOSFETs, and some of the results are presented and discussed below.

For the measurements discussed below, forward mode and reverse mode represent that a positive bias is applied to the nominal drain and source, respectively, while the other terminal is grounded. Three types of devices fabricated with

double-patterning process and denoted as Types A, B, and C were characterized in this thesis. Type A is the nominal symmetric MOSFETs having both extensions formed by implantation at 1e15 cm^{-2} and 15 keV. Type B and Type C are asymmetric MOSFETs with same source extensions formed by implantation at 1e15 cm^{-2} and 20 keV, but different drain extensions which are implanted with 1e15 cm^{-2} and 1e14 cm^{-2}, respectively, both at 10 keV. Fig. 3.17 shows the low-frequency CV curves of the three types of devices. As can be seen in the figures, the three curves coincide well, indicating the devices have the same oxide thickness and flat-band voltage. The effective oxide thickness is 4.4 nm as estimated from the inversion capacitance.

Fig. 3.18 shows the output characteristics of a symmetrical MOSFET fabricated with conventional single-patterning process. Without the etch-induced damage in the drain side as that encountered in double-patterning process, the Id-Vd curves measured under forward mode coincide with those of the reverse mode. However, the drain current is rather low while no saturation behavior is observed as both gate voltage and drain voltage are high, similar to that observed in Schottky barrier MOSFETs [44]. One reasonable reason is the deficient carrier concentration in the source/drain. The 1000 ℃ spike anneal used for post-implant seems not sufficient for dopant activation.

The equivalent circuit of the MOEFET considering the parasitic source and drain resistances is illustrated in Fig. 3.19 [41][42]. As these parasitic resistances are taking into account, the actual gate voltage used to modulate the device under forward mode, defined as Vgs` in Fig. 3.19(a), equals to Vgs minus the voltage drop across the source resistance. Similarly, the effective drain voltage, defined as Vd`s`, equals to Vds minus the voltage drop across the source and drain resistances. For reverse mode of operation, the situation is shown in Fig. 19(b). In Fig. 3.18, since the device has symmetrical S/D, the forward and reverse modes have the same characteristics.

However, Fig. 3.20 shows quite different trends observed on the three types of devices fabricated with double patterning process. As can be seen in the figures, both Type-A and Type-C devices show higher current drive when operated under forward mode of operation with a high gate bias, while for the Type-B device, the two modes exhibit comparable I-V characteristics. Among these devices, it seems only the trend of Type-C device is expected owing to its asymmetrical S/D extension described above. In this regard, the etch-induced recess in drain region shown in Fig. 3.16 should be taken into account. In Type-A device, the etch-induced recess may increase the parasitic drain resistance, making the two operation modes asymmetrical. However, the reason why the two modes look symmetrical remains unclear, and needs further effort to clarify.

The Vth roll-off characteristics are presented in Fig. 3.21, Vth is extracted by maximum conductance method at Vds = 0.1V. As can be seen in the figures, the asymmetric splits (B and C) indeed show less Vth roll-off than the nominal symmetrical one, thanks to the use of a shallower drain extension. The improvement in the immunity to the short-channel effects is further evidenced with the results of DIBL characterization shown in Fig. 3.22.

Chapter 4
Conclusion and Future Work

In this thesis, we have confirmed the feasibility of double patterning for pushing the resolution limit of photolithographic tools and the implementation to device fabrication. With an i-line stepper, the capability of forming 80 nm line patterns was demonstrated in this thesis, which is far beyond the resolution limit of conventional i-line process (~0.3 μm).

Moreover, with the aid of this technique, various devices with asymmetrical source/drain structure were fabricated and characterized in this thesis. TFETs with on/off ratio of around 4~5 orders in magnitude was achieved, and the minimum SS was about 230~260 mV/dec. N-channel MOSFETs with asymmetrical S/D were also fabricated. Owing to the insufficient dopant activation, the device performance is poor. Furthermore, the etch-induced recess phenomenon was observed in the drain region of the fabricated devices, which was induced in the second gate etching step.

Although the preliminary results obtained in this work demonstrated that the double patterning technique is promising for practical device fabrication, some issues remained to be solved in the future. For TFET, the formation of abrupt junction

profile is essential. The spike RTA employed in this work seems not appropriate for this purpose. In the future, solid-phase epitaxial re-growth (SPER) [45] can be adopted to improve the device performance. The insufficient conduction current could be overcame by the use of high-k dielectric and new structure. The Green Transistors are also taken into account, Fig. 4.1 show the cross sectional view of a Green Transistor.

The poor characteristics of the asymmetric extensions nMOSFETs fabricated in this work is obviously related to the inappropriate anneal condition as well as the etch-induced damage issue of double patterning technique. Optimization of the S/D implant conditions and the post anneal conditions must be done to improve the device performance. For the latter issue, re-design of the mask layouts to promote the end point signals of the second step should be helpful for improving the control of etch process.

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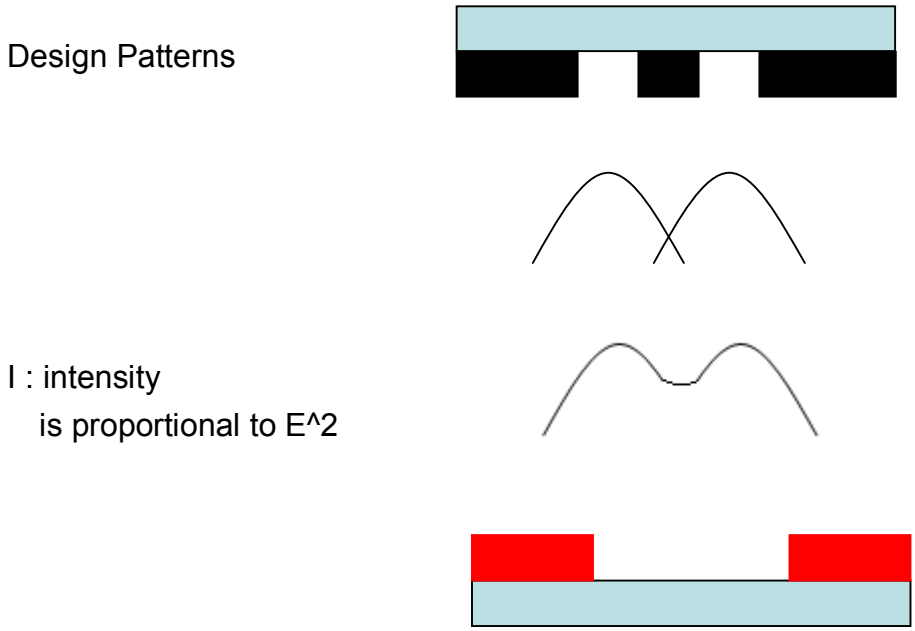


Fig. 1.1 Collapse of PR patterns due to diffraction effect.

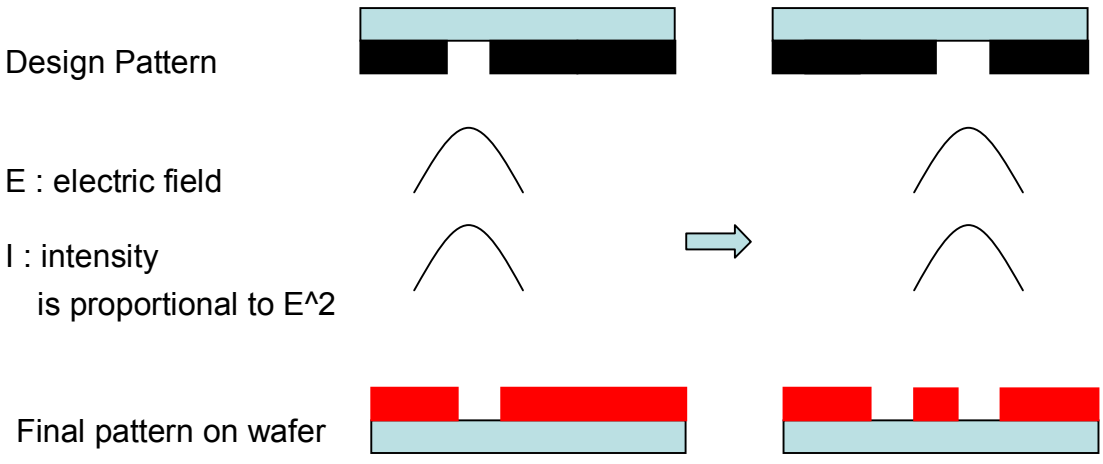


Fig. 1.2 Working principle of double patterning technology.

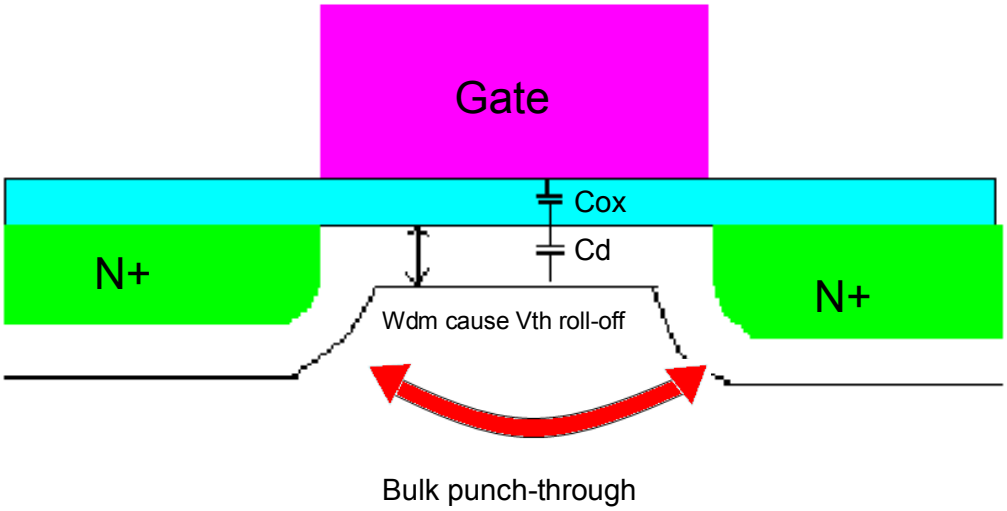


Fig. 1.3 Illustration of the depletion regions and capacitance components inside a planar MOSFET.

TFET

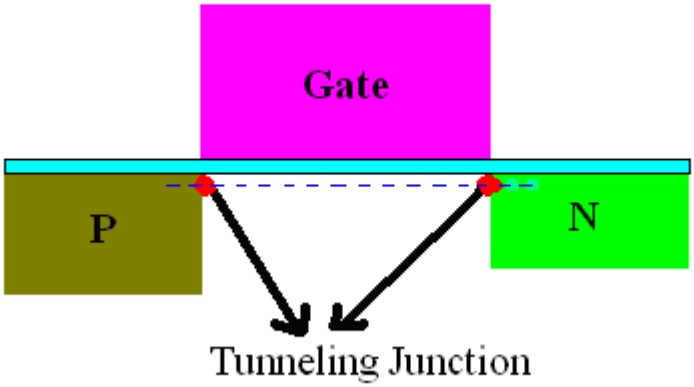


Fig. 1.4 Schematic TFET structure.

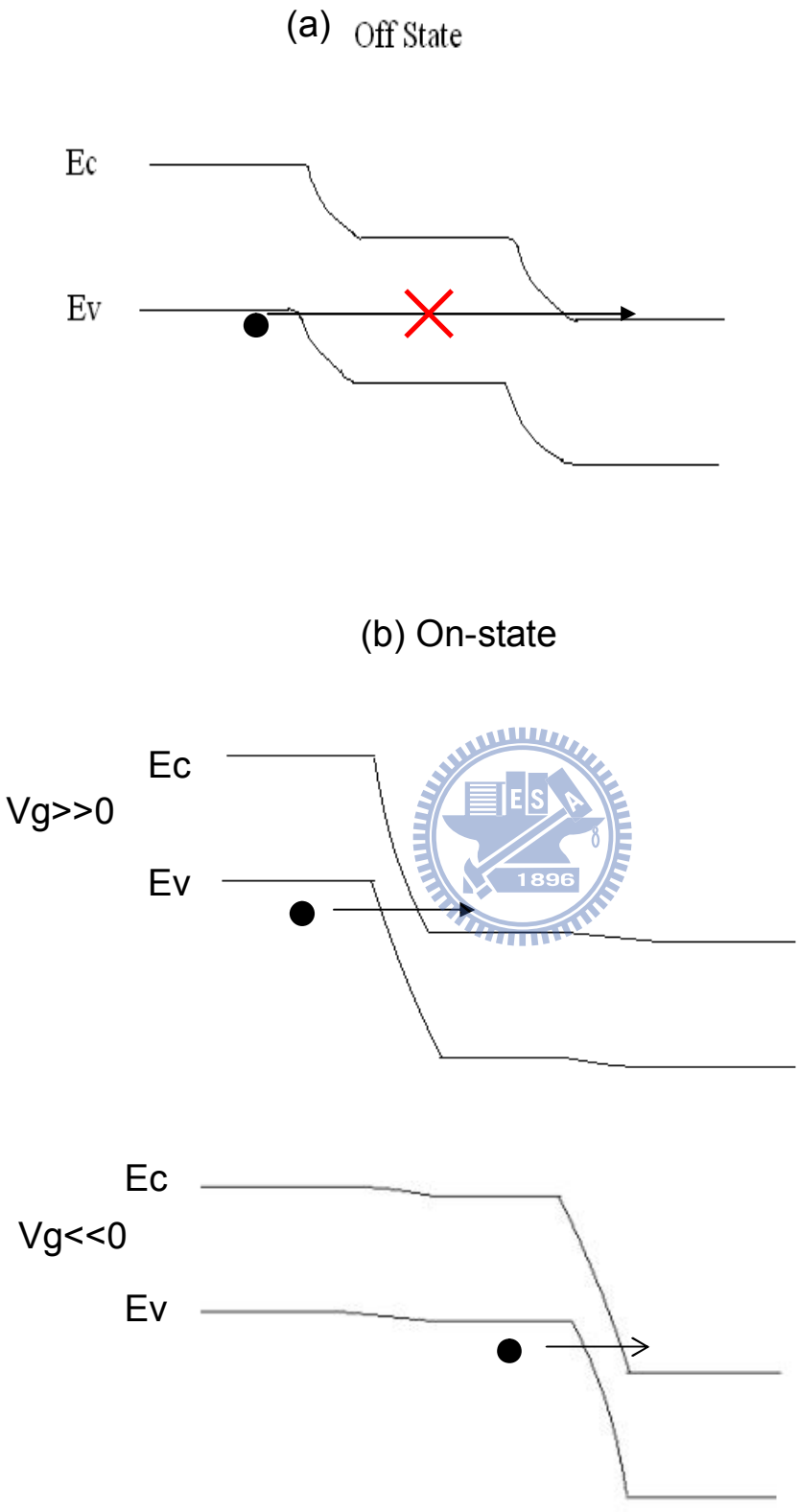


Fig. 1.5 Energy band diagram along the dash line in Fig. 1.4 for TFET in (a) off and (b) on state.

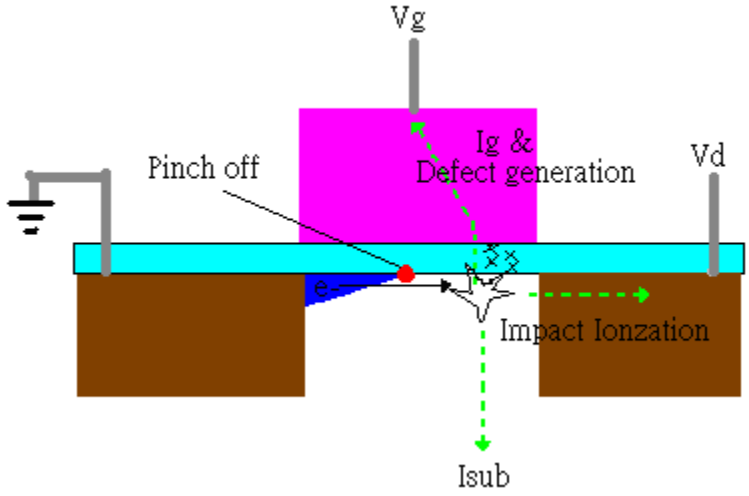


Fig 1.6 Hot carrier effect diagram.

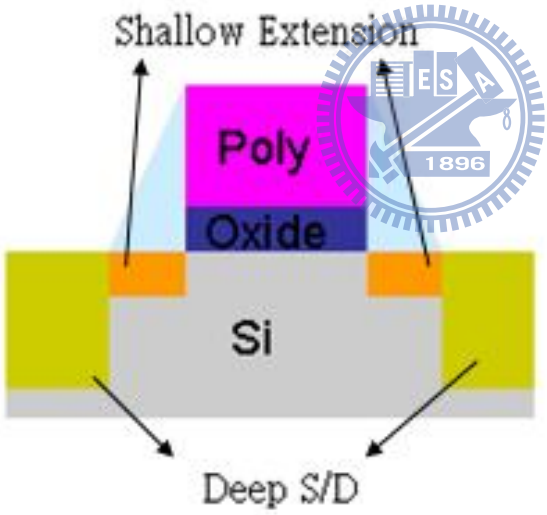


Fig. 1.7 MOSFET with source/Drain extensions.

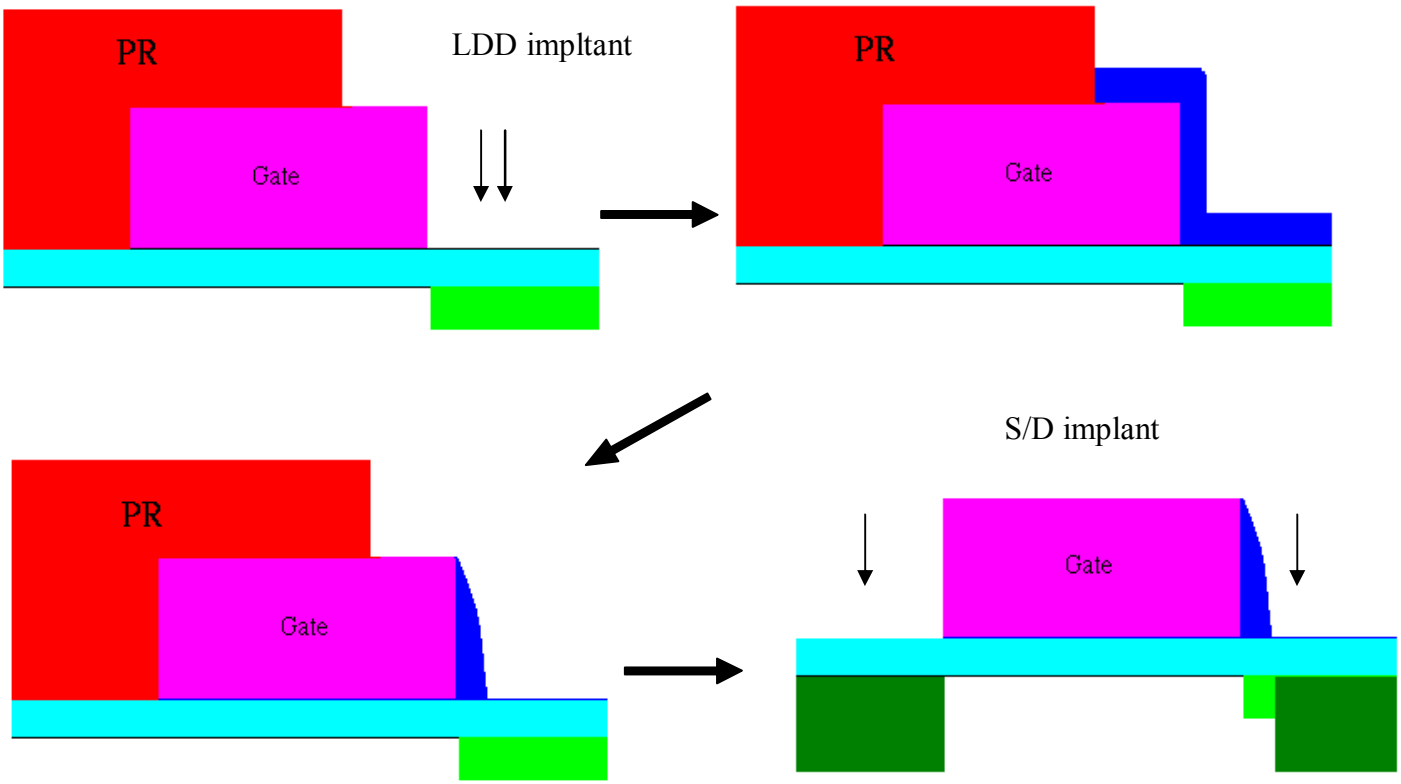


Fig. 1.8 Conventional process flow of the MOSFETs with asymmetric extensions.

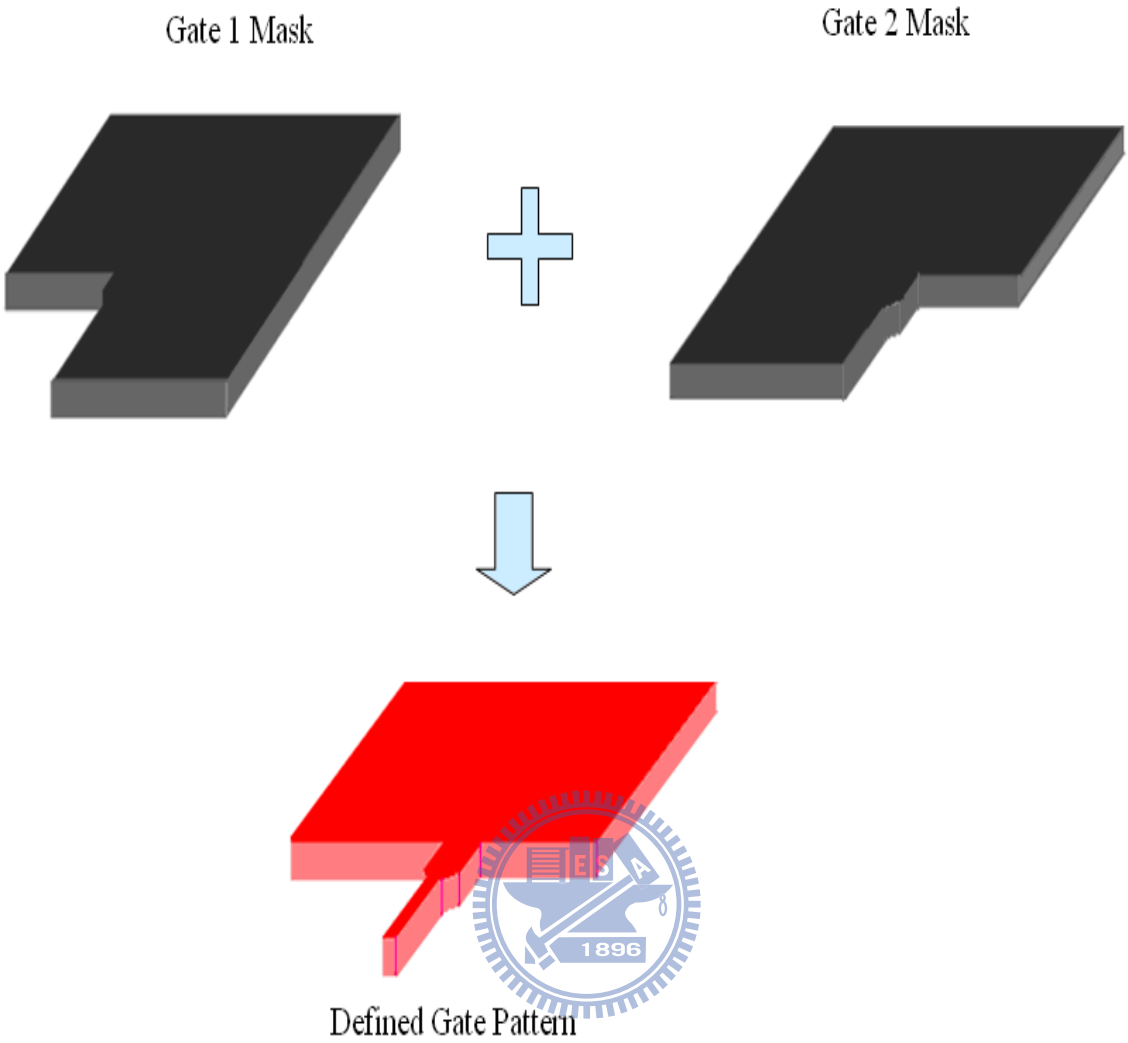


Fig. 2.1 Schematic of the Double Patterning technique. The gate pattern formed on the substrate is defined by the overlap region of the two designed masks.

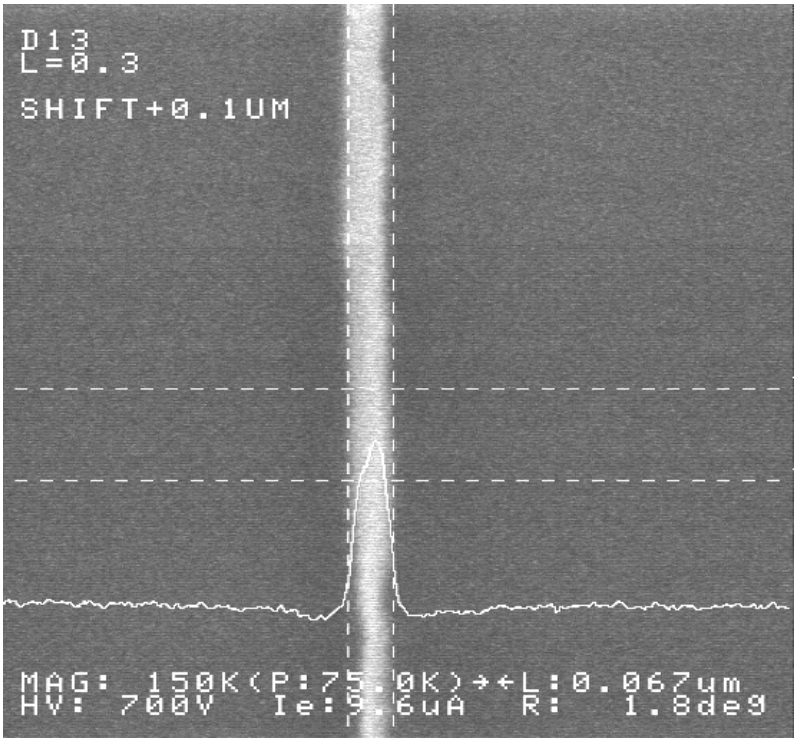


Fig. 2.2 Top view of a pattern with nominal gate length of 0.3 μm. Practical gate length was measured to be 67 nm

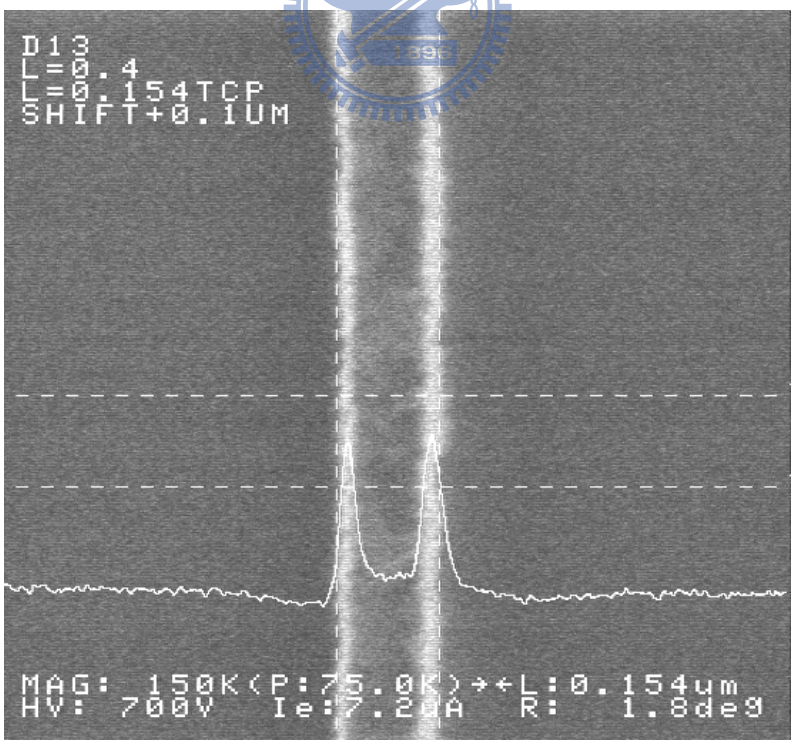


Fig. 2.3 Top view of a pattern with nominal gate length of 0.4 μm. Practical gate length was measured to be 0.154 μm.

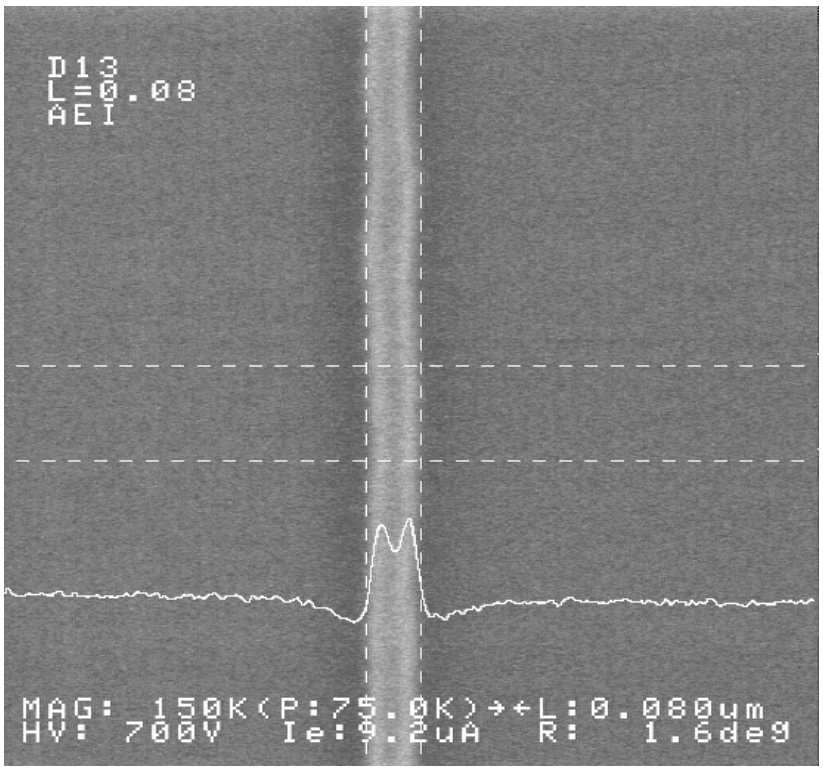


Fig. 2.4 Top view of a pattern with gate length of 80 nm. Practical gate length was measured to be close to the designed value.

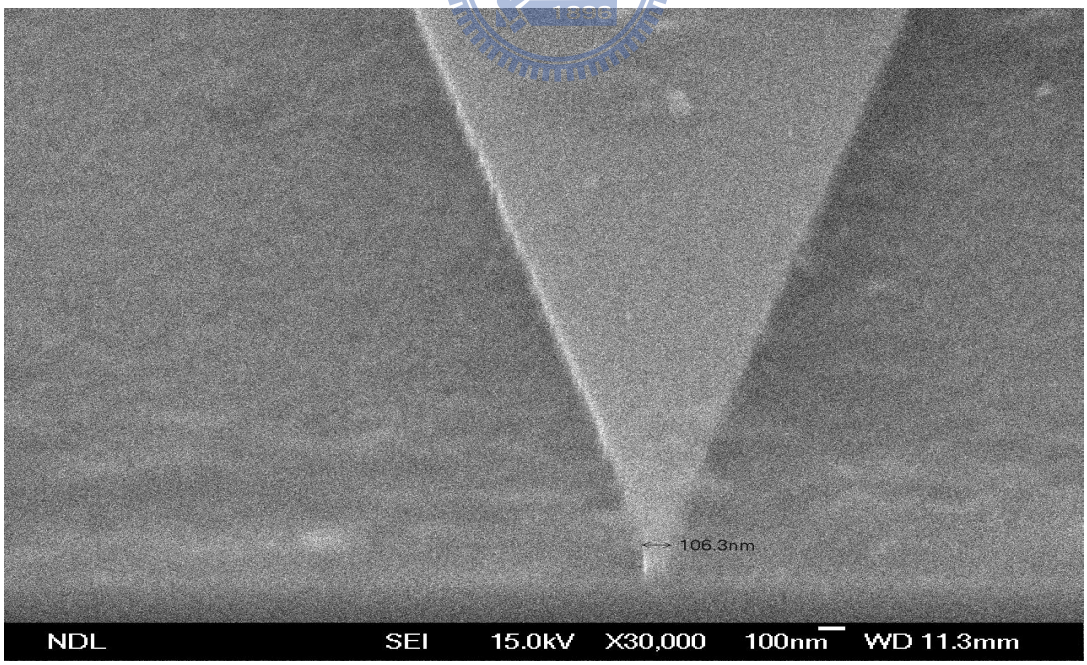
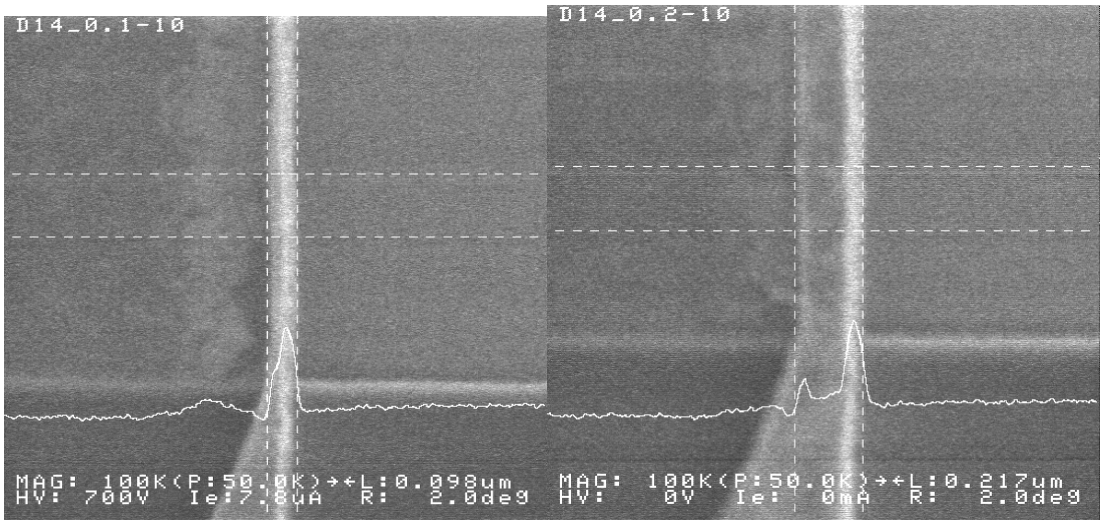
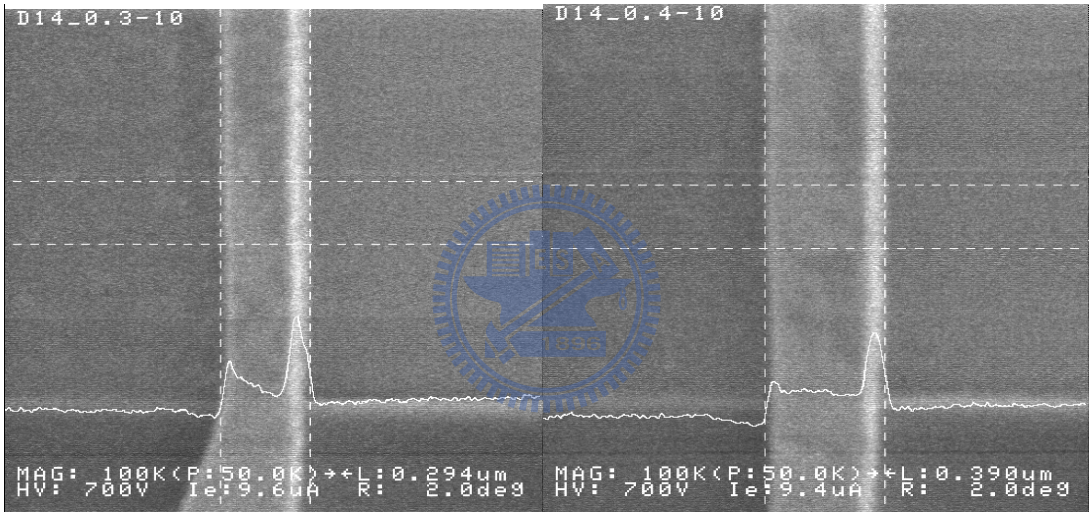


Fig 2.5 Top view of a poly-Si gate formed by double patterning technique.



a) b)



c) d)

Fig. 2.6 Top-view SEM images of poly-Si gates with designed length of (a) 0.1μm, (b) 0.2 μm, (c) 0.3 μm, and (d) 0.4 μm.

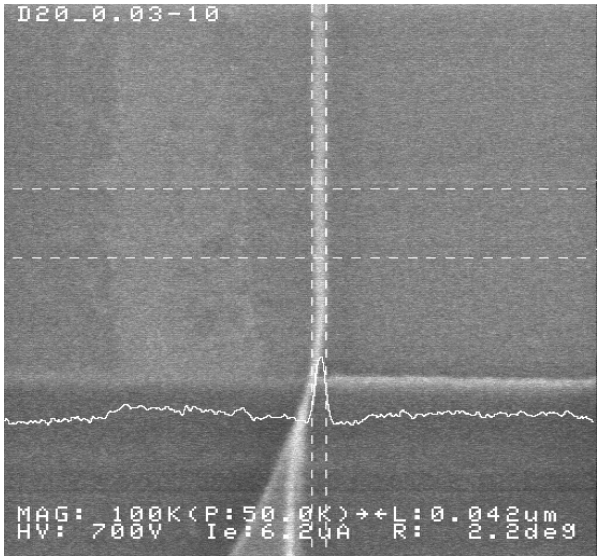
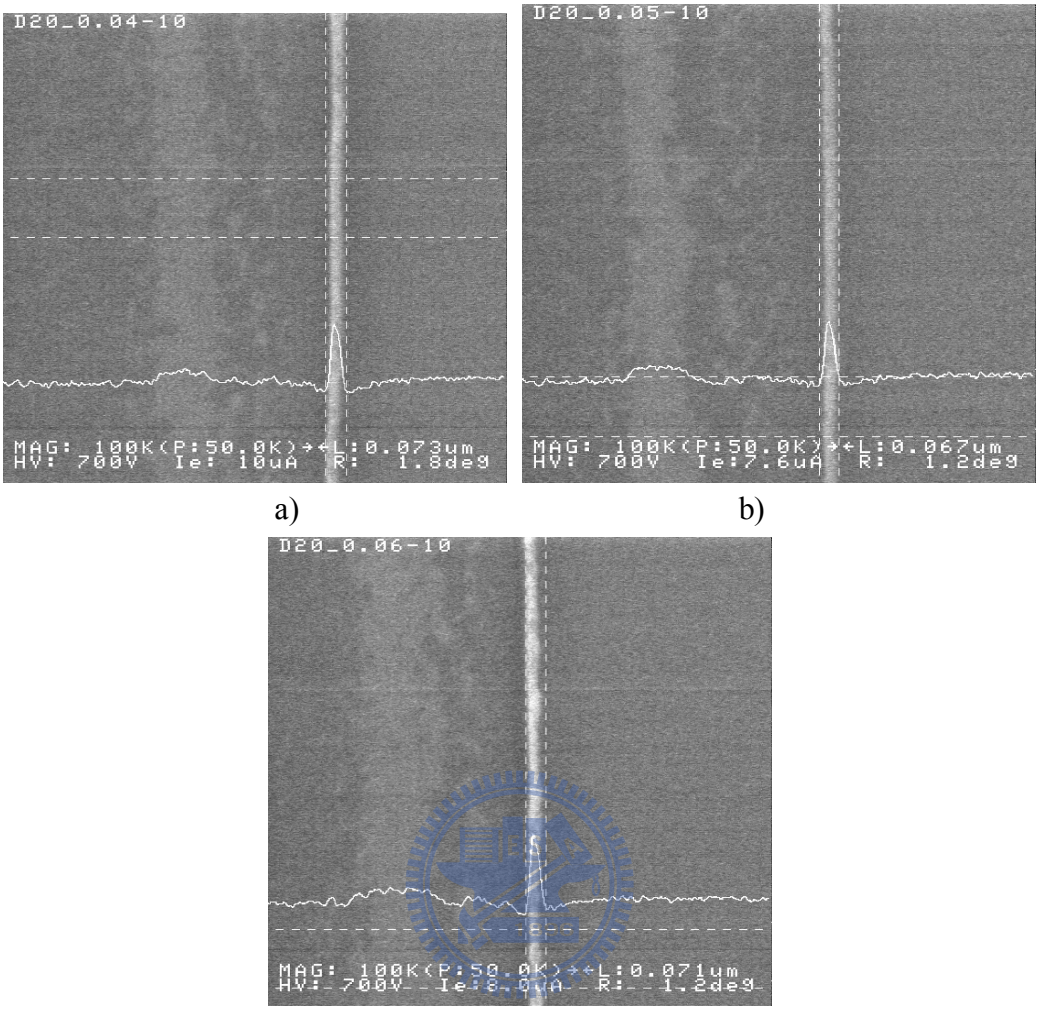


Fig. 2.7 Top view SEM image of a poly-Si gate with designed length of 30 nm.



a) b)

c)

Fig. 2.8 Top-view SEM images of poly-Si with designed length of (a) 40 nm, (b) 50 nm, and (c) 60 nm.

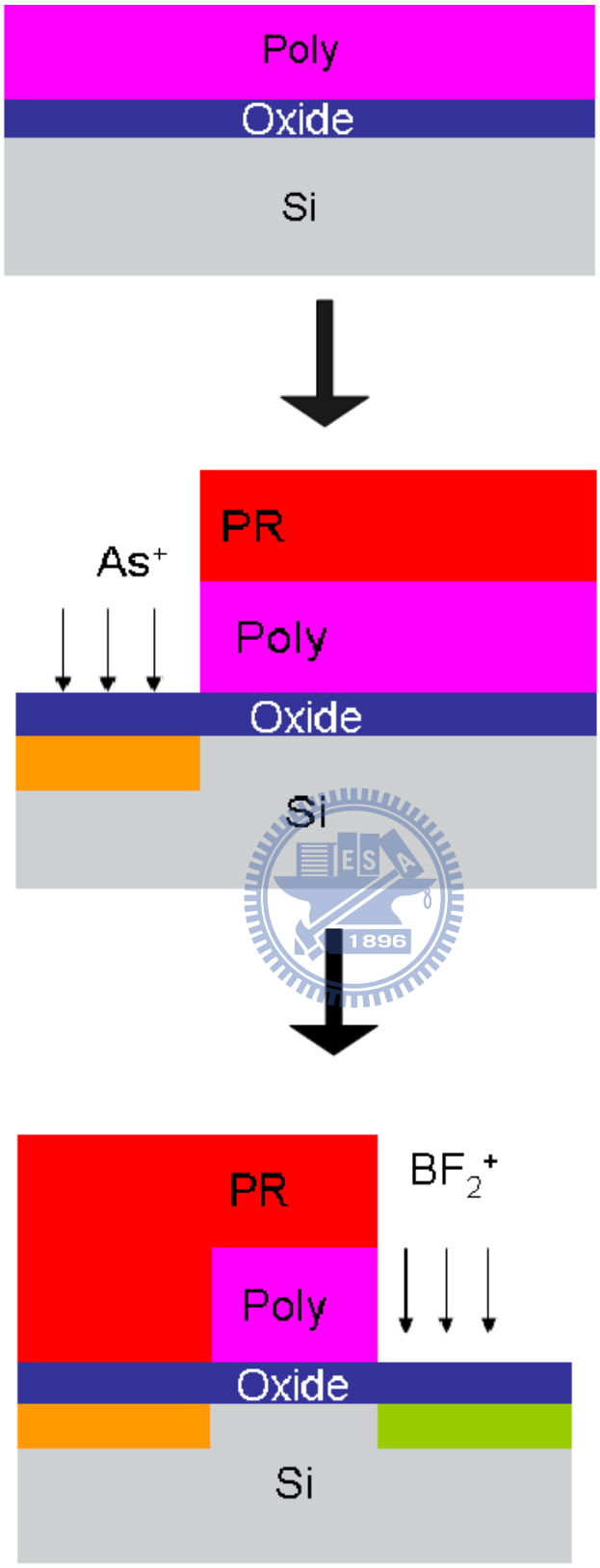


Fig. 2.9 Process flow of the TFETs fabricated on Si wafers.

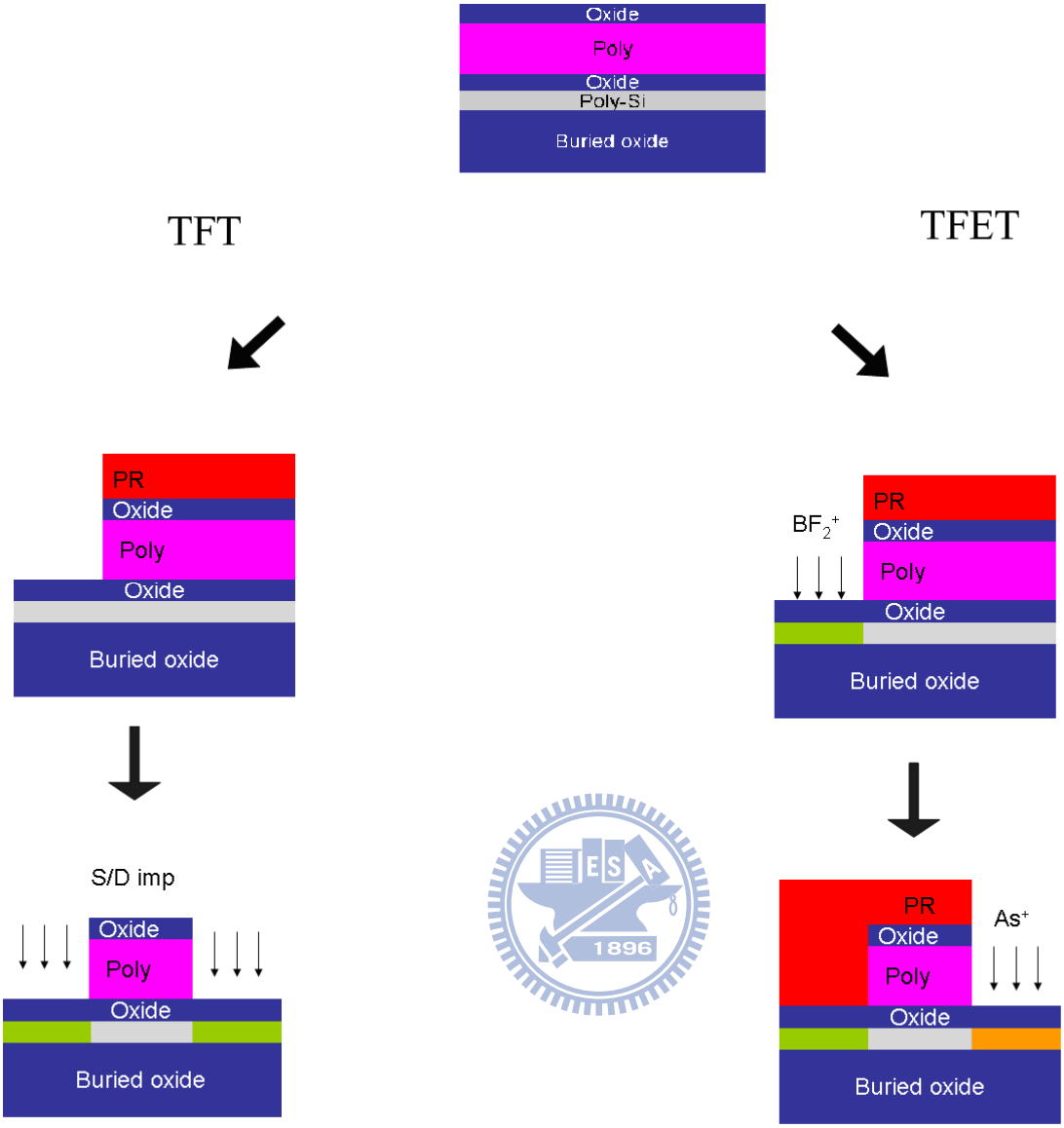


Fig. 2.10 Process flows for fabrication of different types of poly-Si devices.

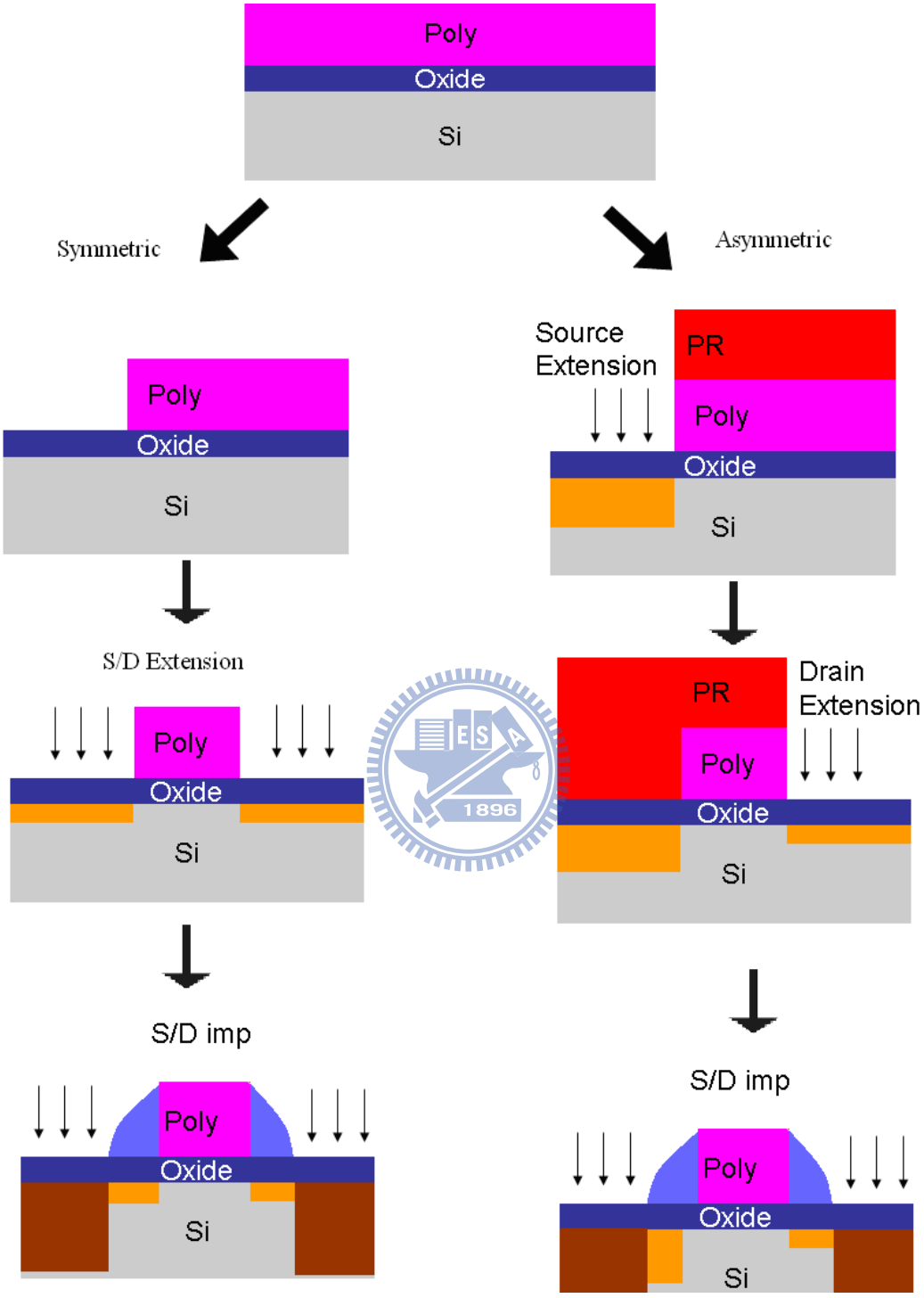


Fig. 2.11 Process flow of N-MOSFETs with asymmetric extensions.

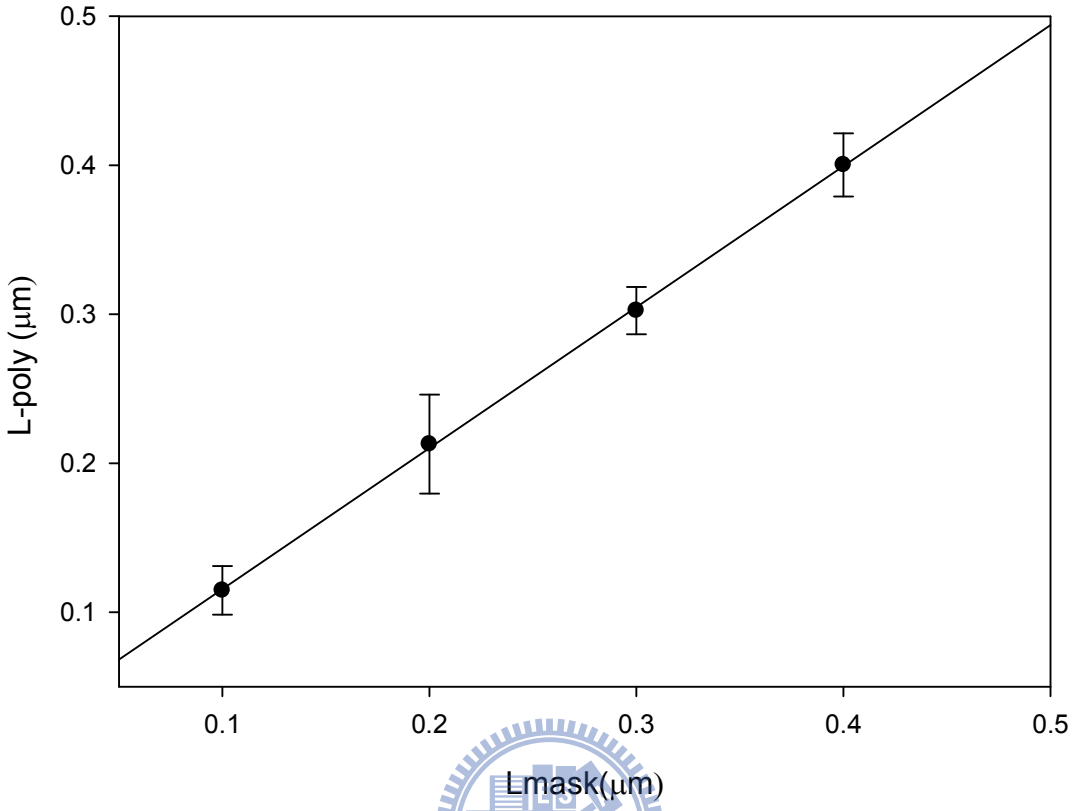


Fig. 3.1 Actual gate length extracted by top view SEM images as a function of the designed gate length. The error bar indicates the standard deviation (1σ) of the measured data.

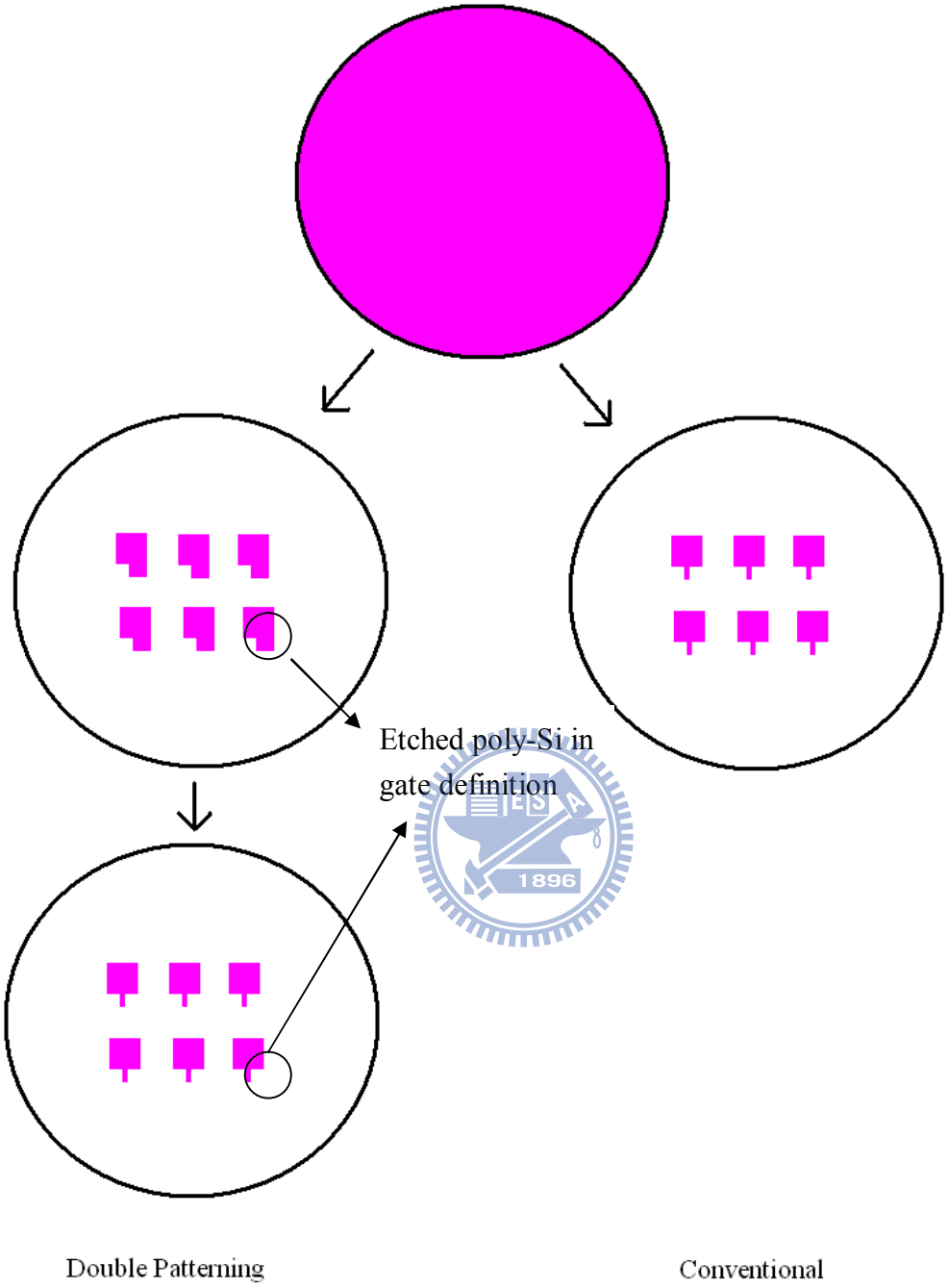


Fig. 3.2 Diagrams of gate patterns remaining on the wafer after specific steps.

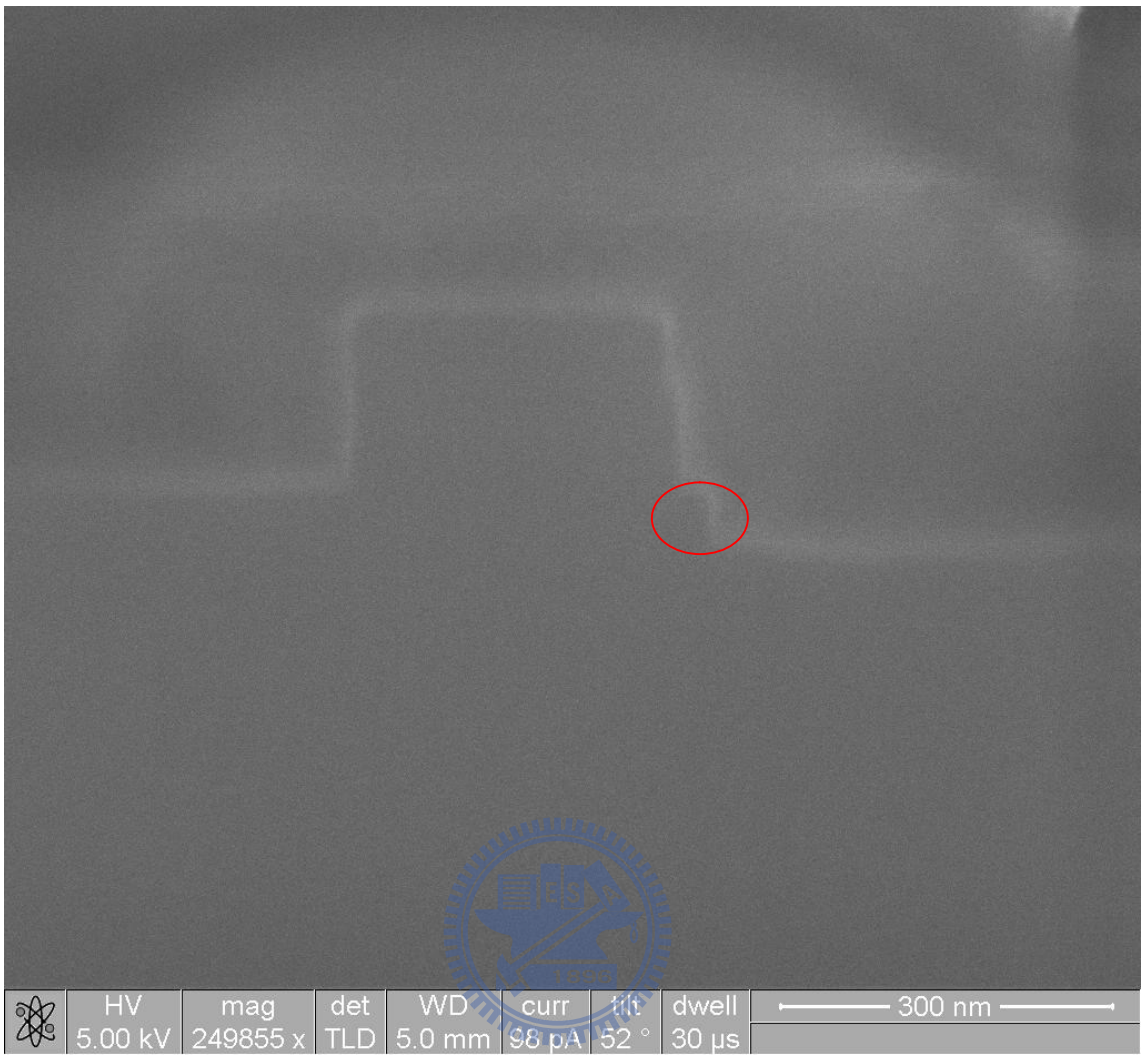
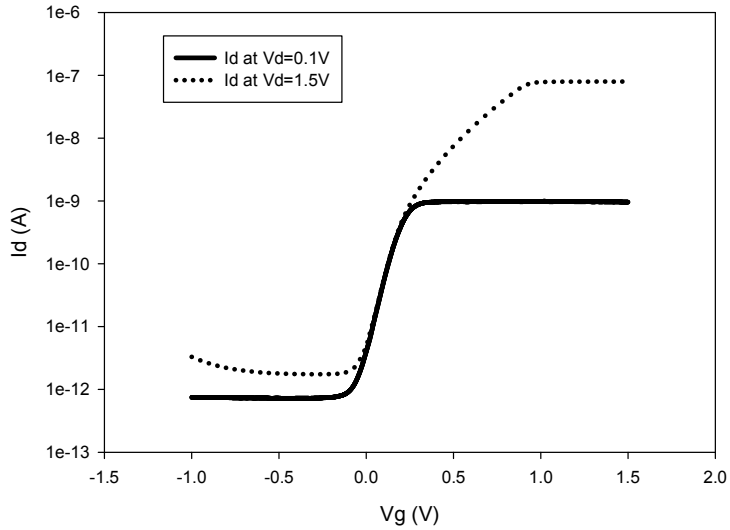
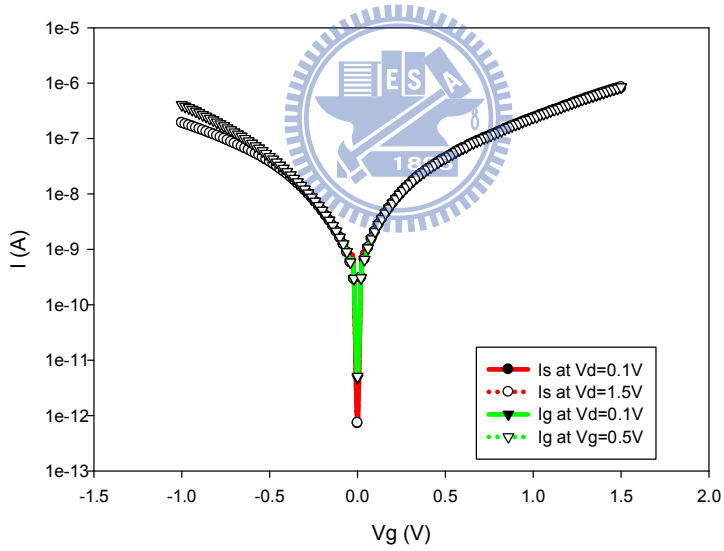


Fig. 3.3 Cross sectional view of a fabricated MOSFET showing the damaged drain region caused by the second etch step.



a)



b)

Fig. 3.4 Id-Vg curves of damaged MOSFETs with gate width of 10 μm. (a) Lg = 5 μm (b) Lg = 0.5 μm

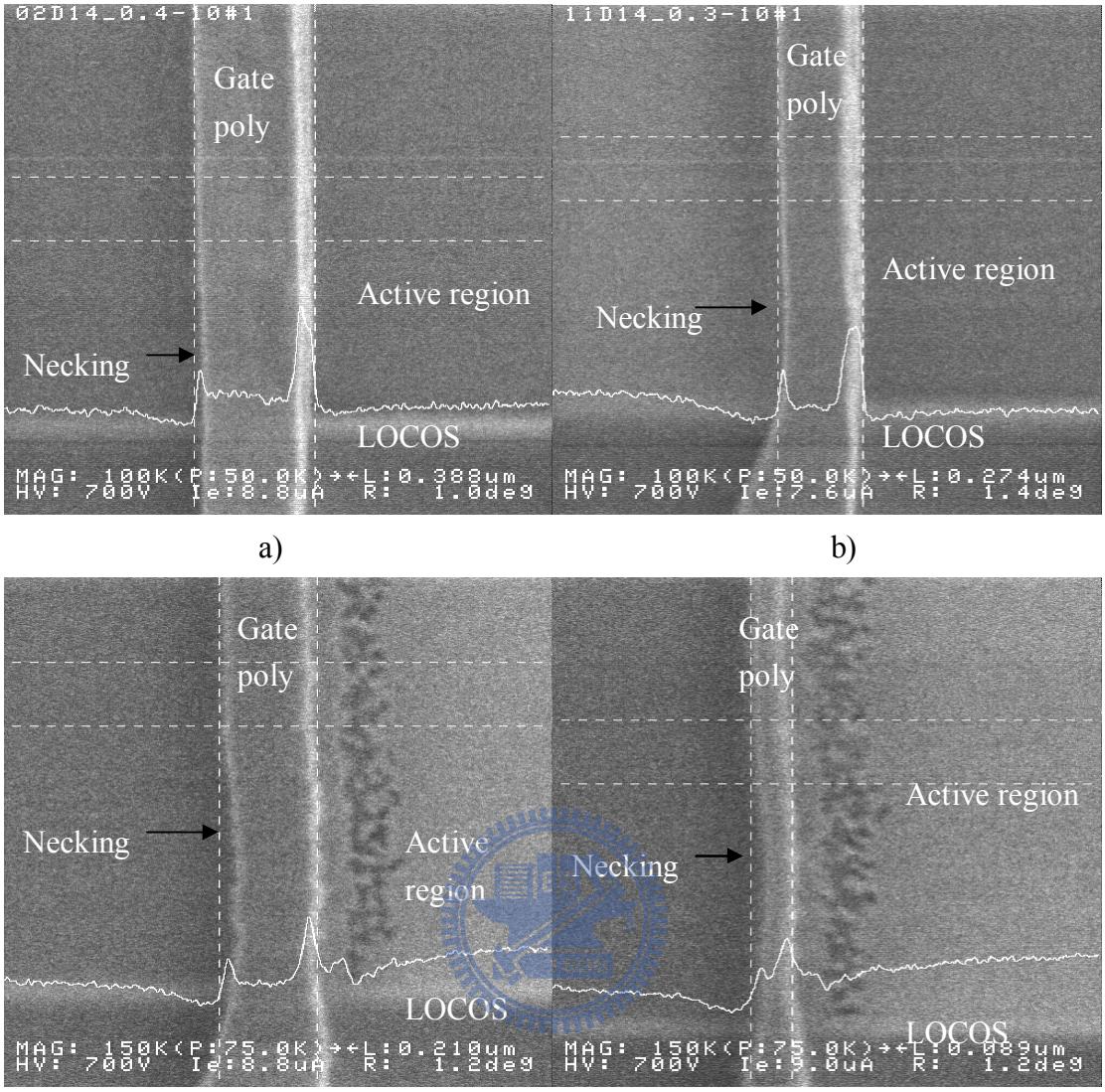
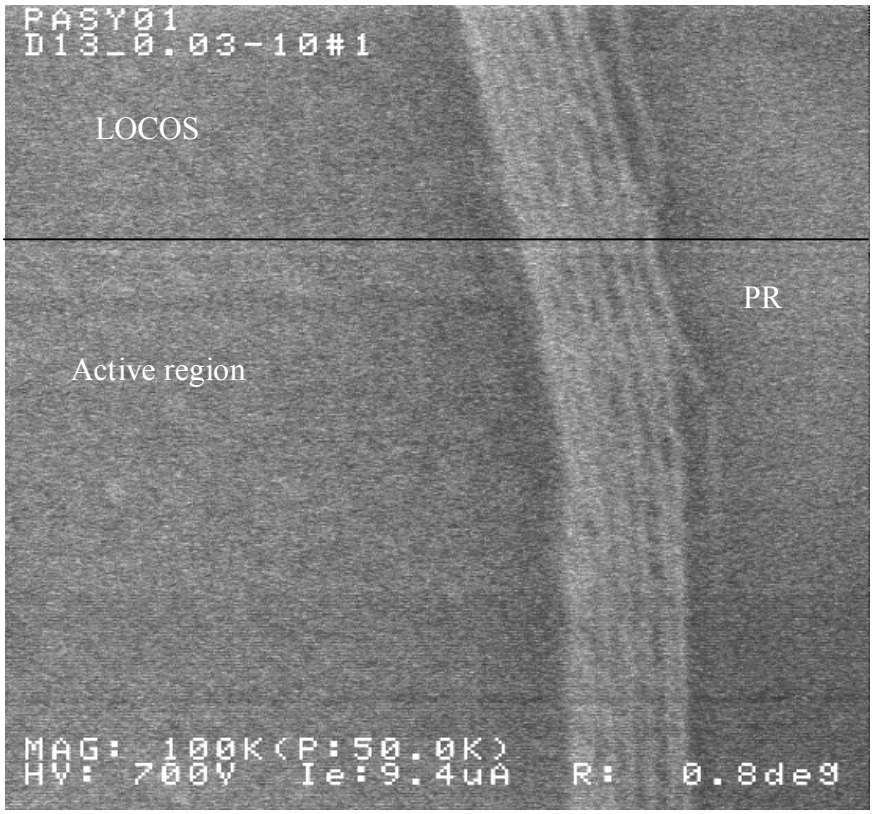
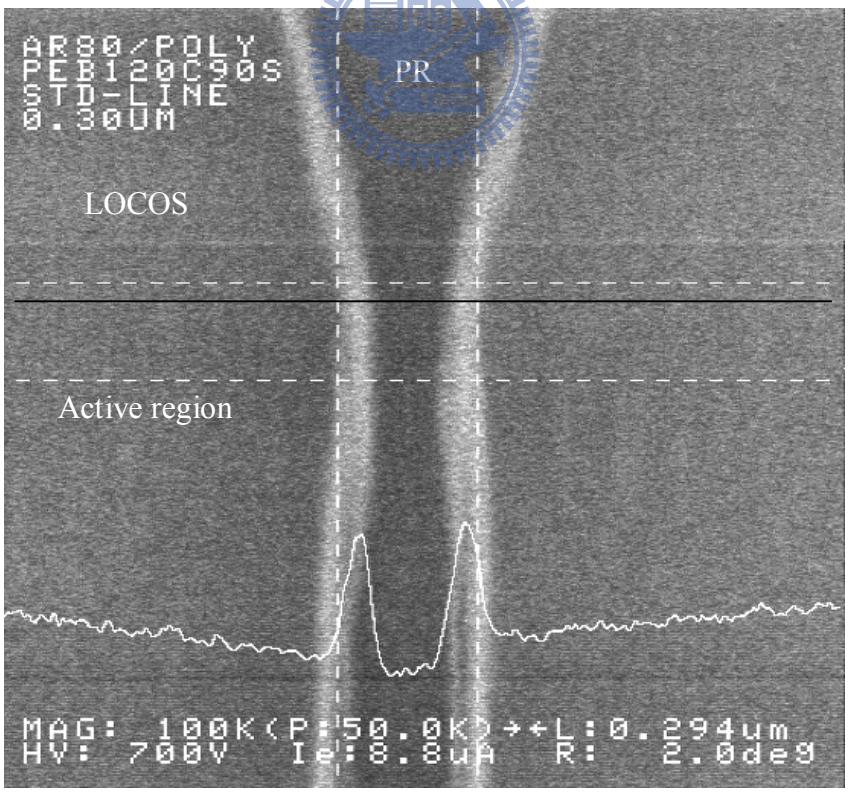


Fig. 3.5 SEM images showing etch-induced recess in the drain side induced during the second etch step with gate length of (a) 0.4 μm, (b) 0.3 μm, (c) 0.2 μm, and (d) 0.1 μm.

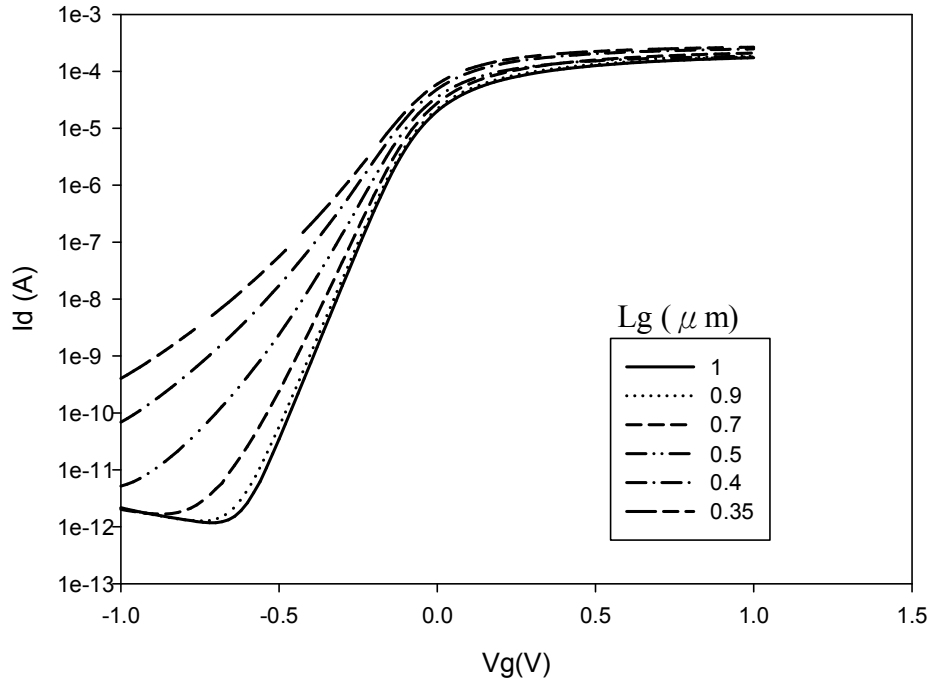


a)



b)

Fig. 3.6 PR patterns after (a) gate 1 lithographic step in double patterning and (b) single patterning process.



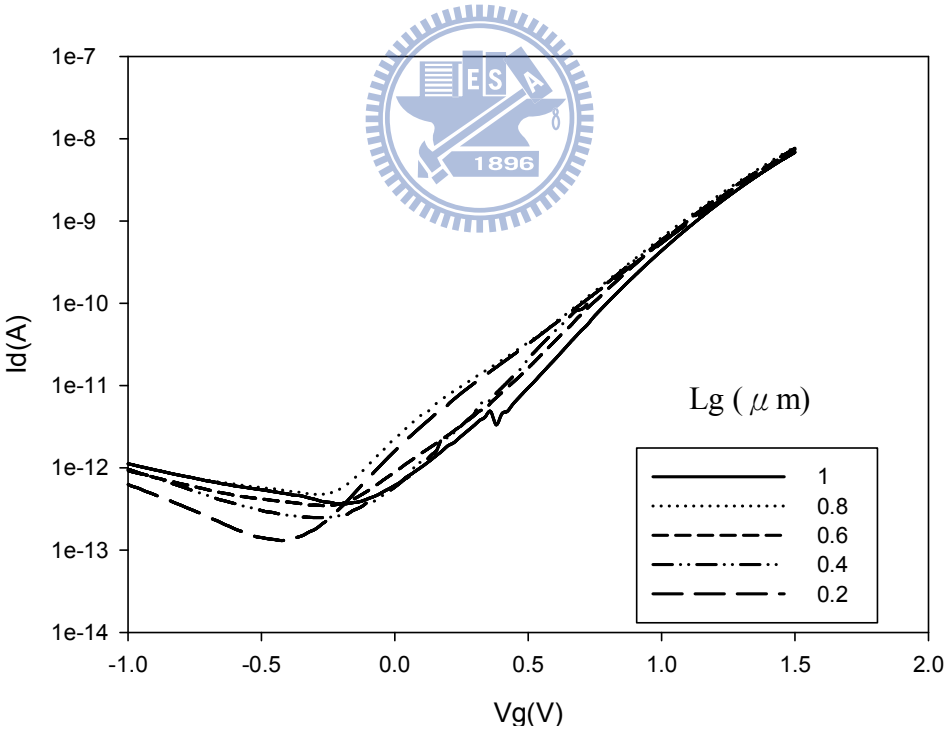
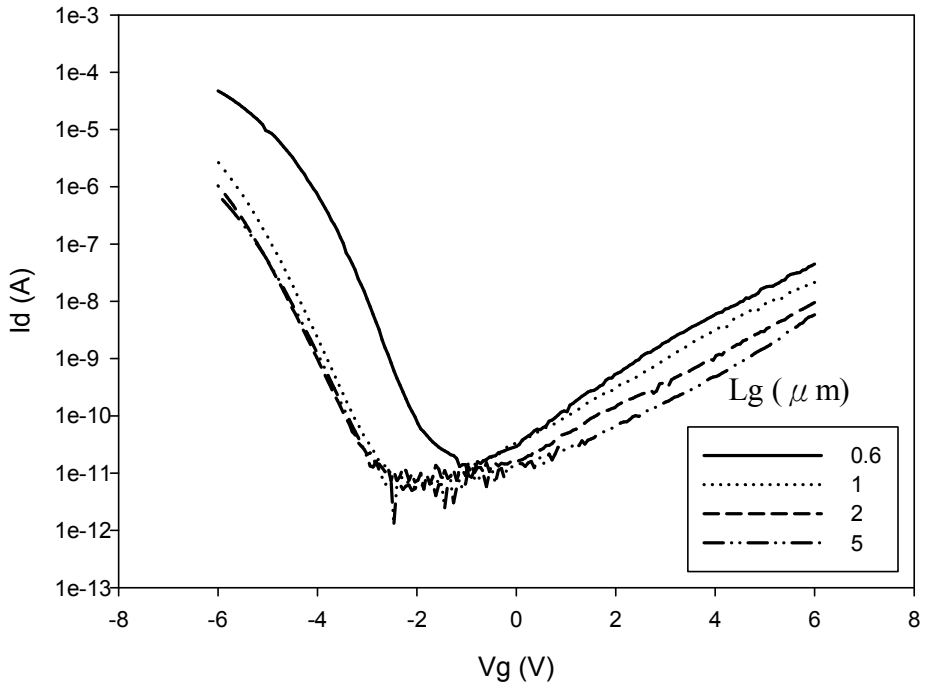
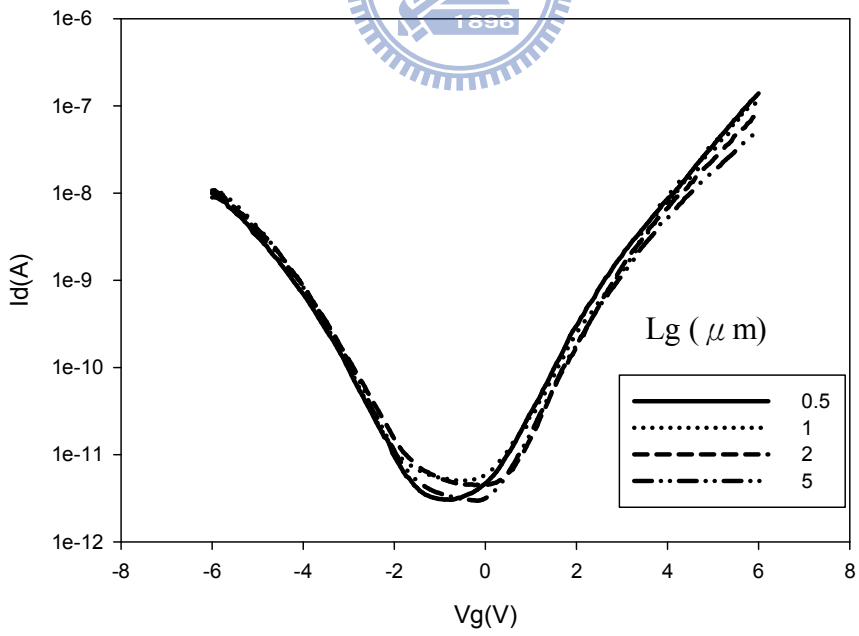


Fig. 3.7 Length dependence of transfer characteristics of devices built on bulk-Si with gate width of 10 μm. (a) MOSFETs biased at Vd = 1 V and Vs = 0V. (b) TFETs biased at Vd = 0.5V and Vs = -0.5V.

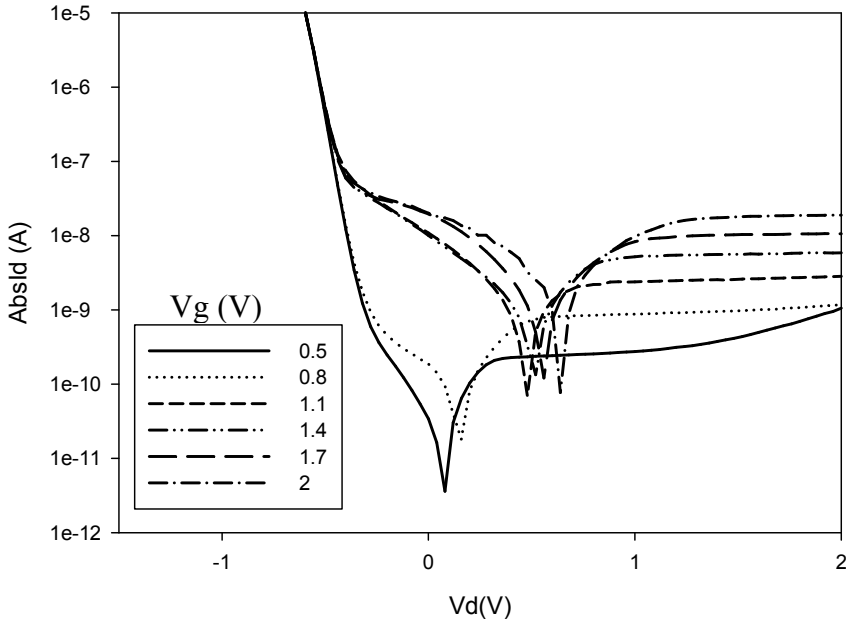


a)

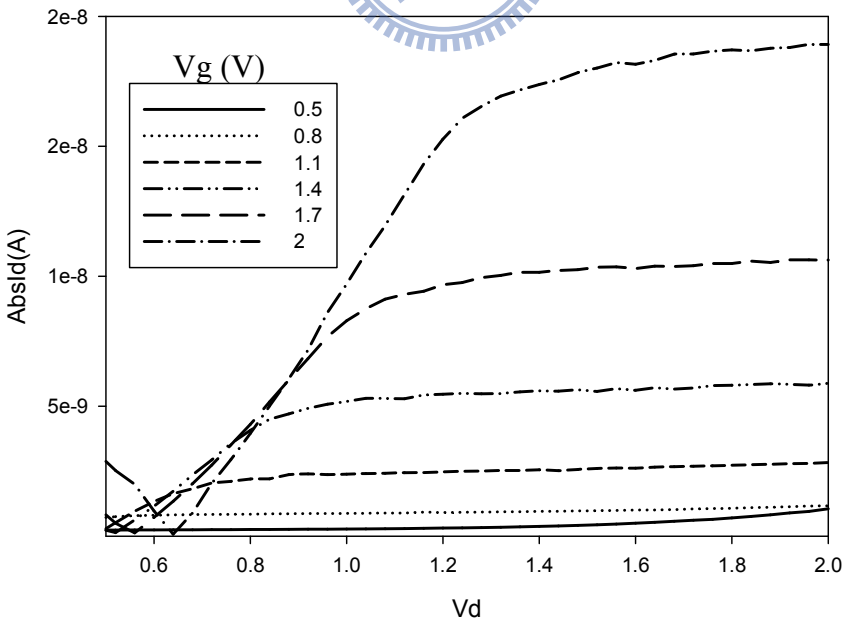


b)

Fig. 3.8 Length dependence of transfer characteristics of devices built on poly-Si substrate. (a) p-channel TFT biased at Vds = -2V. (b) TFETs biased at Vds = 2V.

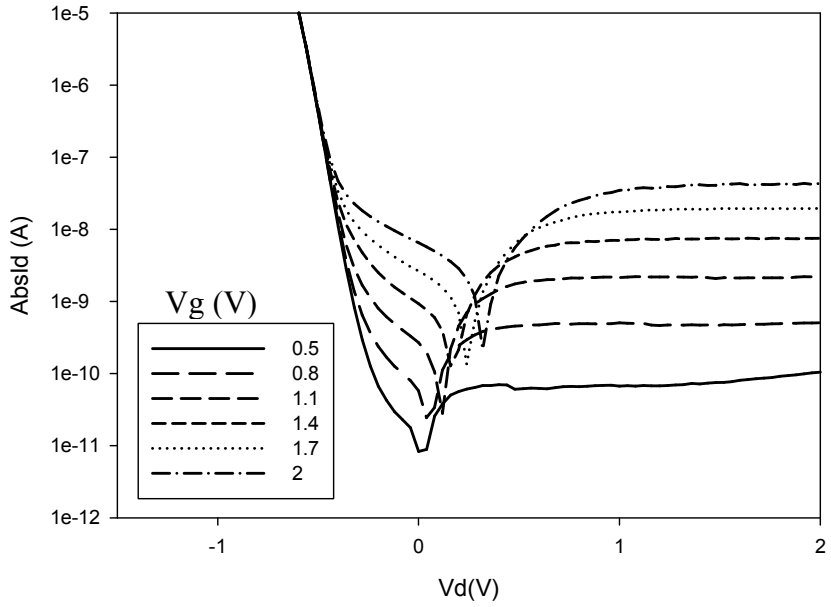


a)

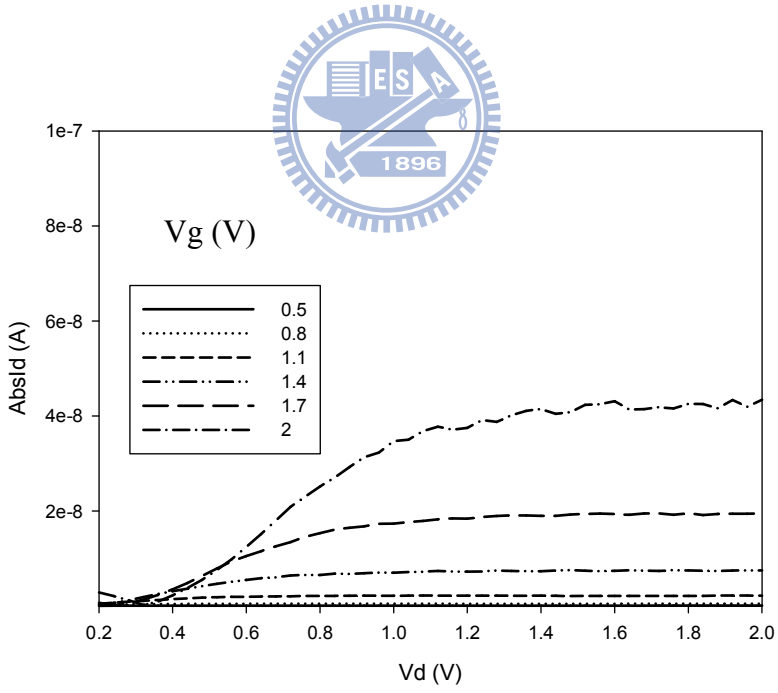


b)

Fig. 3.9 Output characteristics of a c-Si TFET with Id expressed in (a) log scale and (b) linear scale. Channel length/width =0.2 μm /10 μm.



a)



b)

Fig. 3.10 Output characteristics of a c-Si TFET with Id expressed in (a) log scale and (b) linear scale. Channel length/width =1 μm /10 μm.

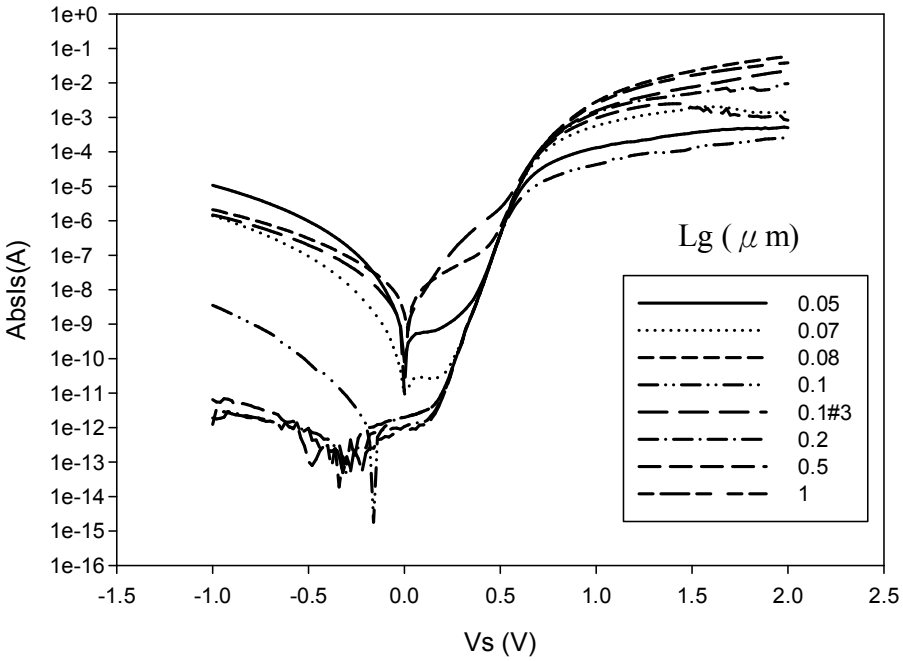


Fig. 3.11 Characteristics of the PIN diodes with different gated length. The gate is floating during measurements.

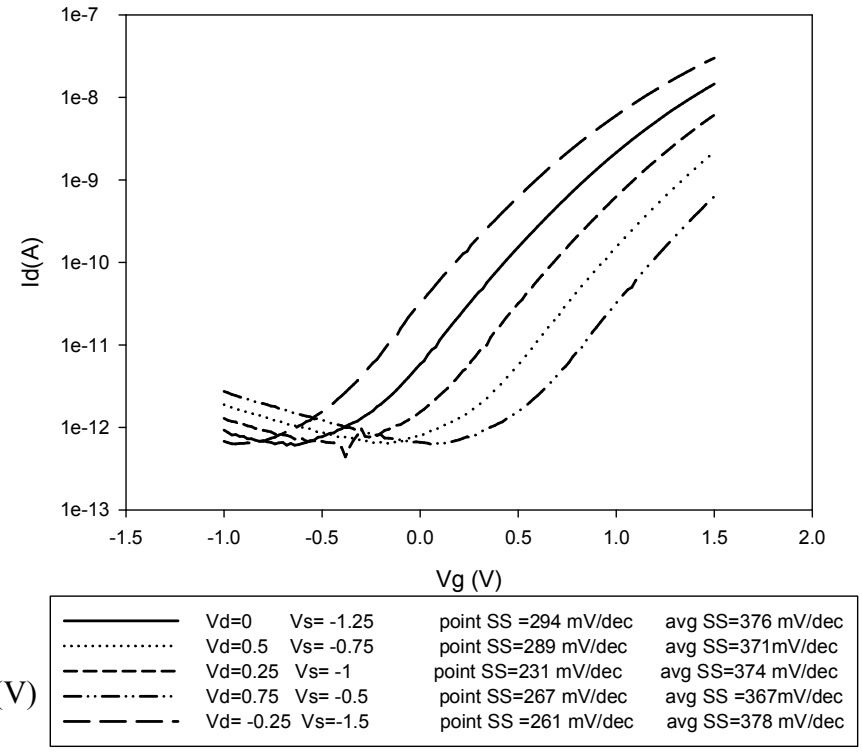
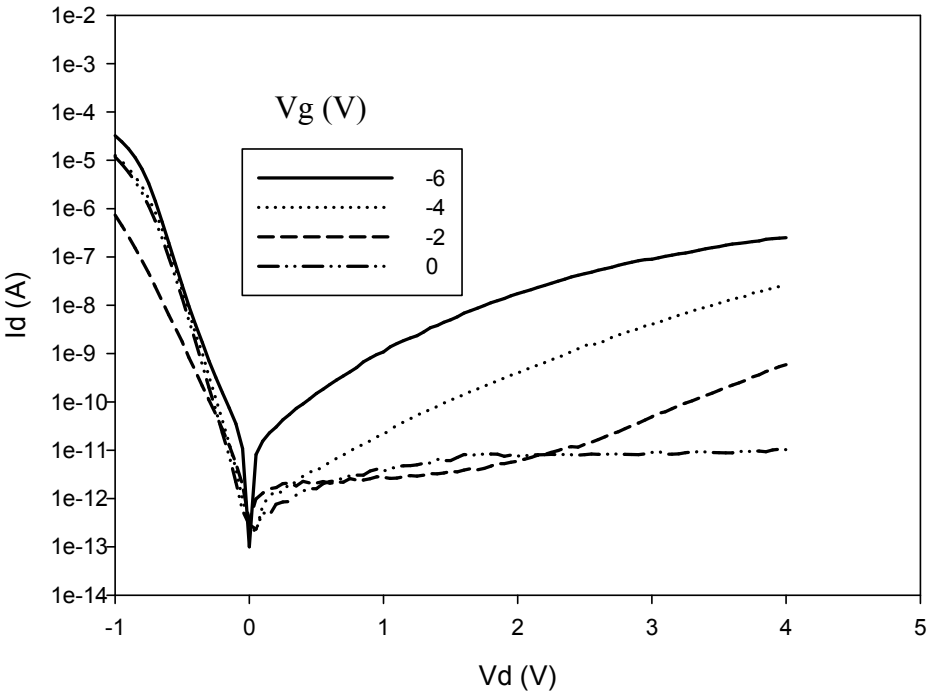
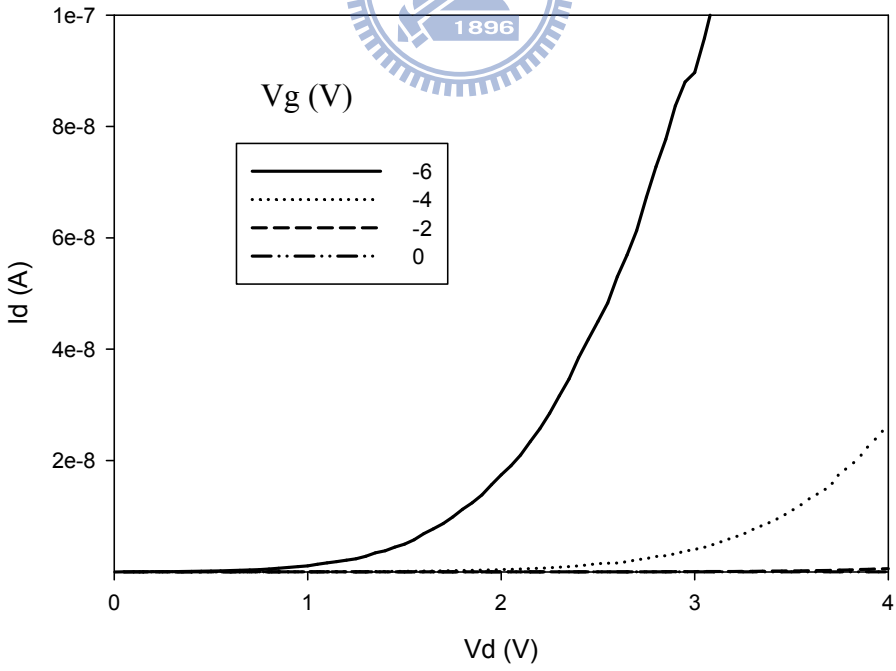


Fig. 3.12 Transfer characteristics of a c-Si TFET with constant Vds (1.25V) but different S/D bias. Channel length/ channel width =0.2 μm/10 μm.

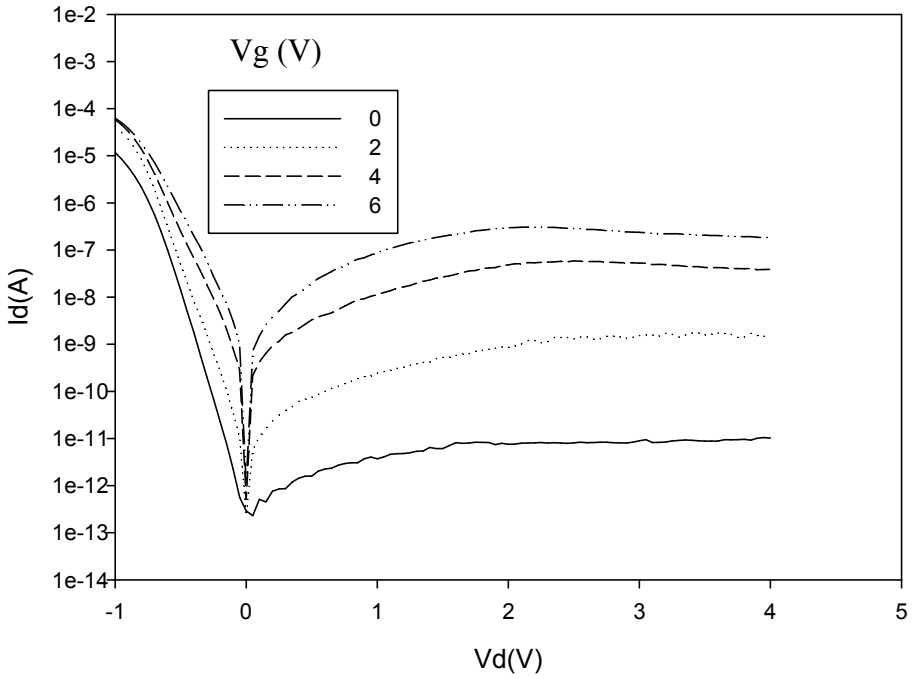


a)

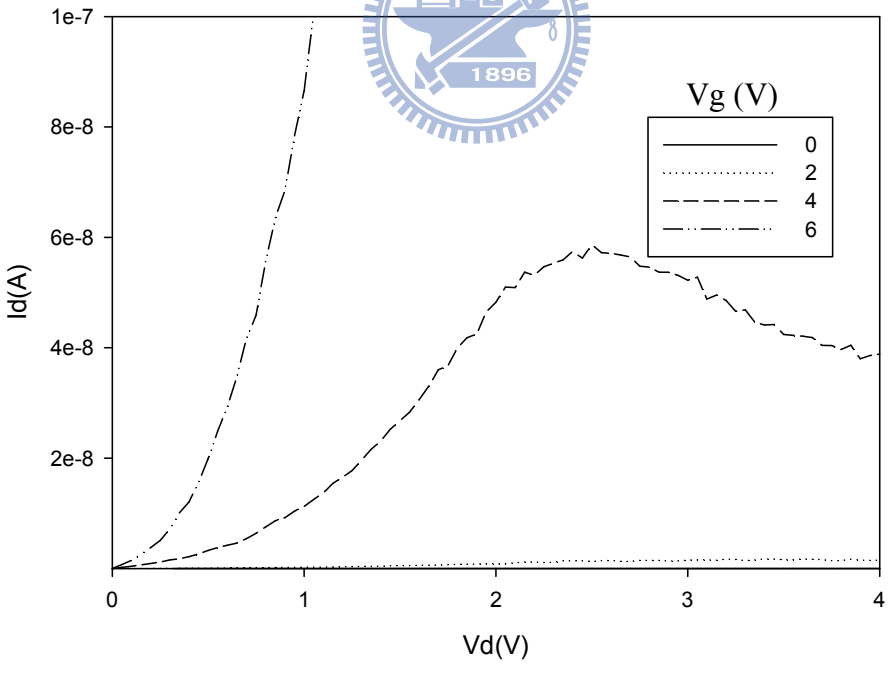


b)

Fig. 3.13 Output characteristics of a poly-Si TFET expressed in (a)log-Id scale (b) linear-Id scale. The post-S/D anneal was conducted at 900℃ for 30 sec. Channel length/width/thickness =1 μm/10 μm/50 nm.



a)



b)

Fig. 3.14 Output characteristics of a poly-Si TFET expressed in (a) log-Id scale (b) linear-Id scale. The post-S/D anneal was conducted at 900℃ for 30 sec. Channel length/width/thickness =1 μm/10 μm/50 nm.

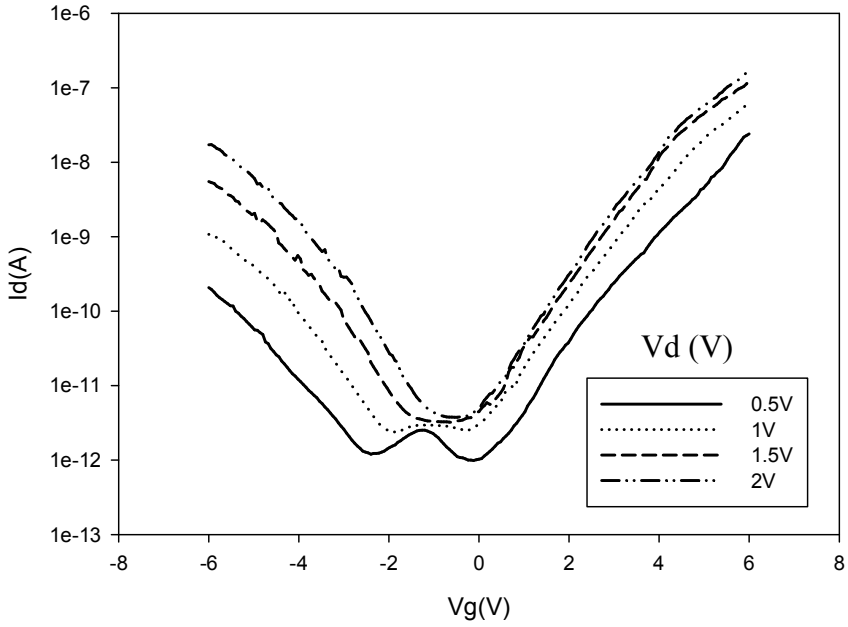


Fig. 3.15 Transfer characteristics of a poly-Si TFET. Channel length/channel width/channel thickness =1 μm/10 μm/50 nm.

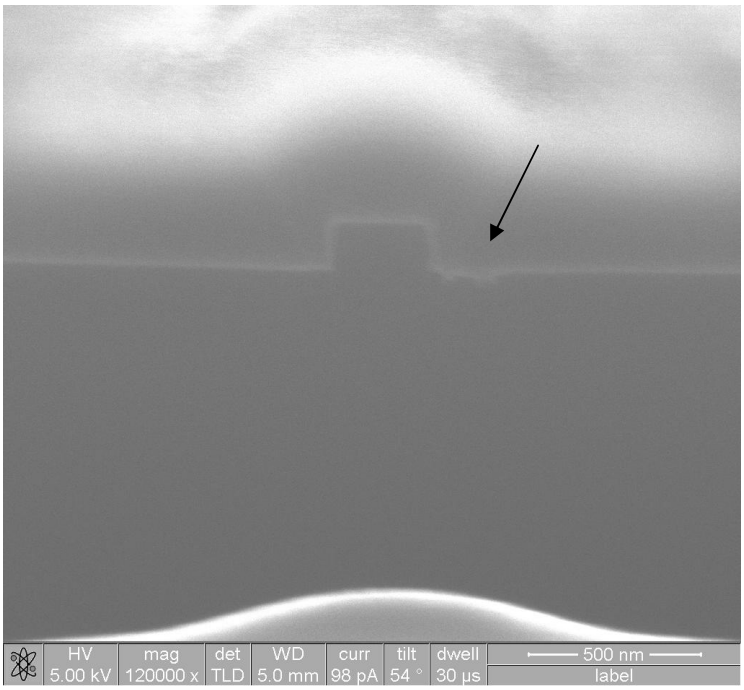


Fig. 3.16 Cross-sectional view of a 0.3 µm MOSFET showing an etch-induced recess in the drain region.

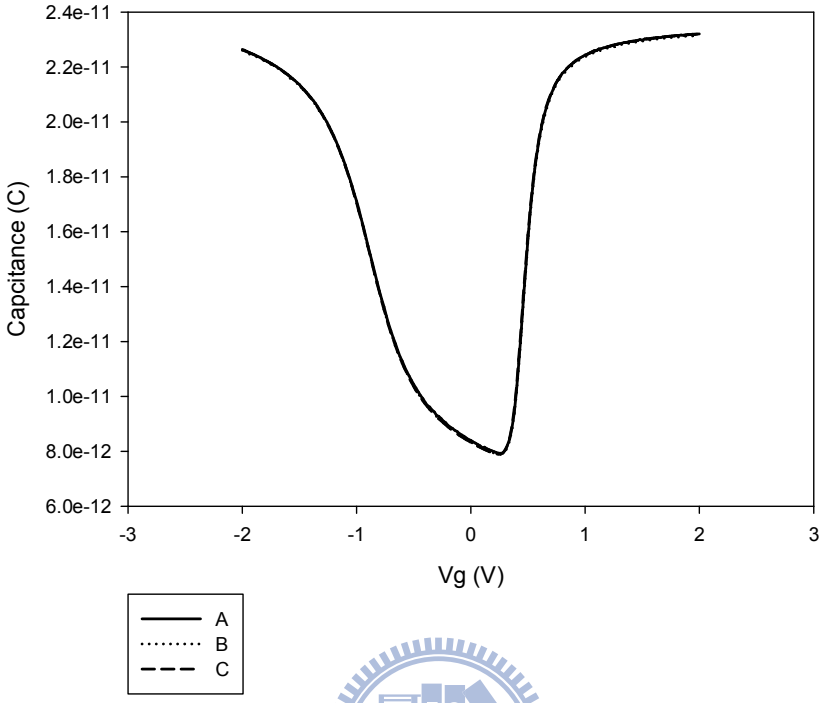


Fig. 3.17 The CV-curves of the three types of devices fabricated with double patterning process. Channel length/width =50 μm /50 μm. The measurement frequency is 100 kHz.

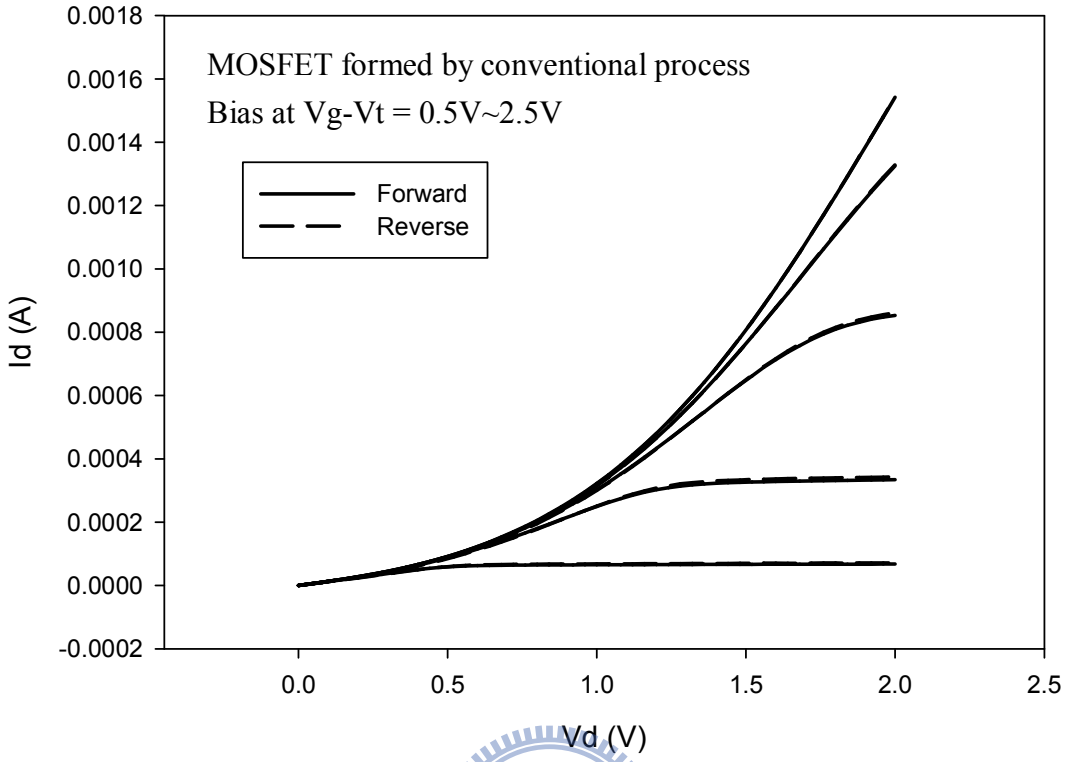


Fig. 3.18 The output characteristics of a symmetric MOSFET formed by conventional process. Channel length/width =0.4 μm /10 μm.

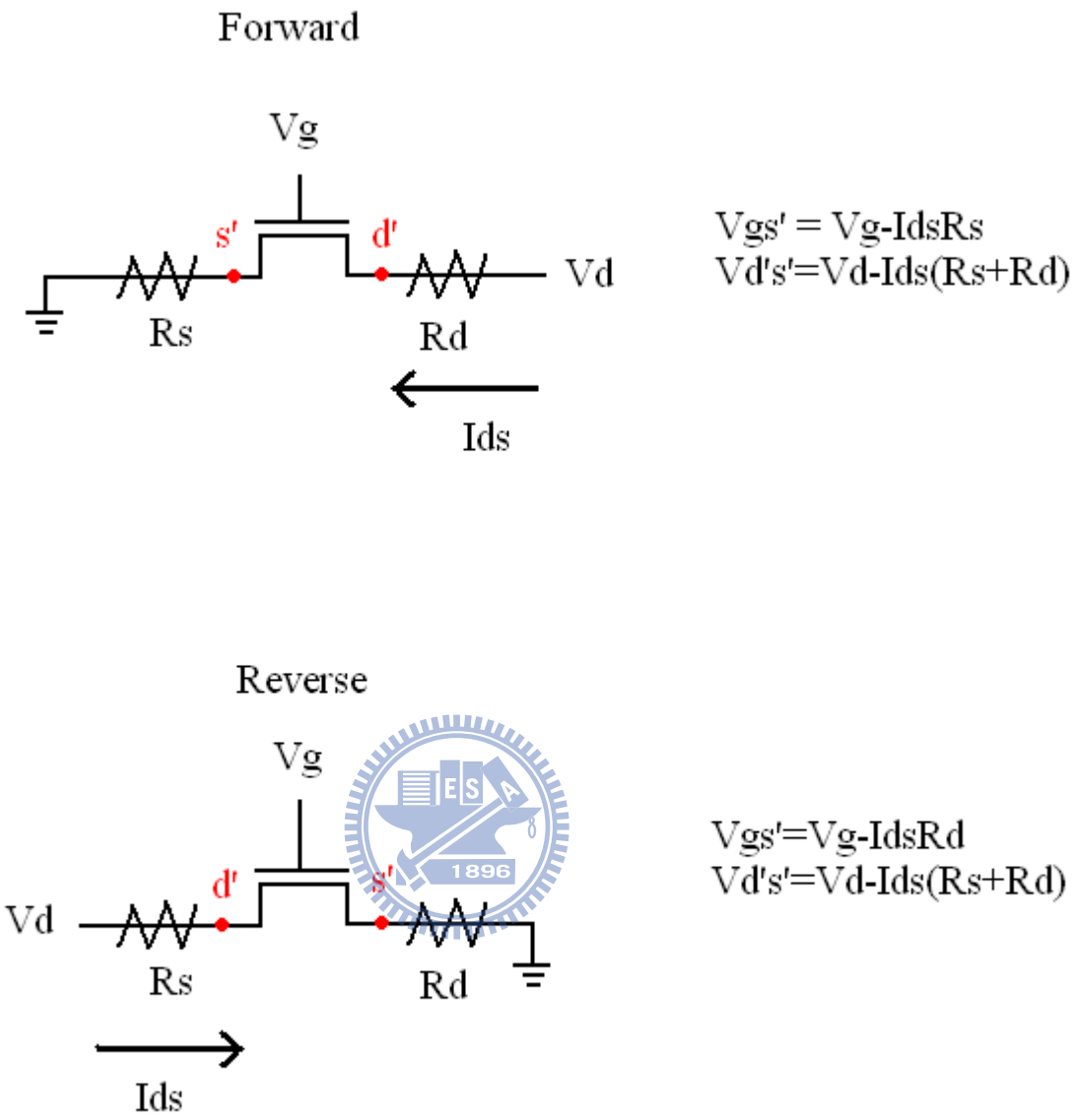
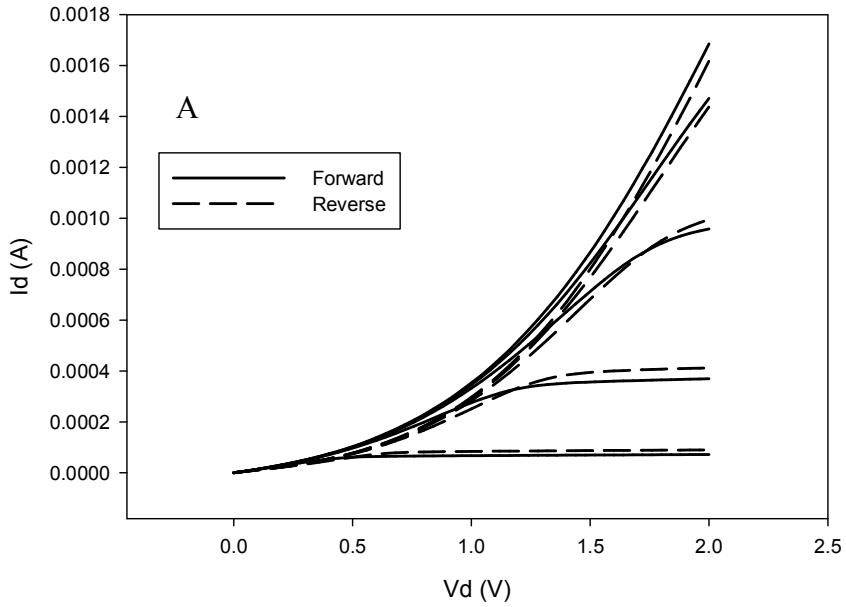
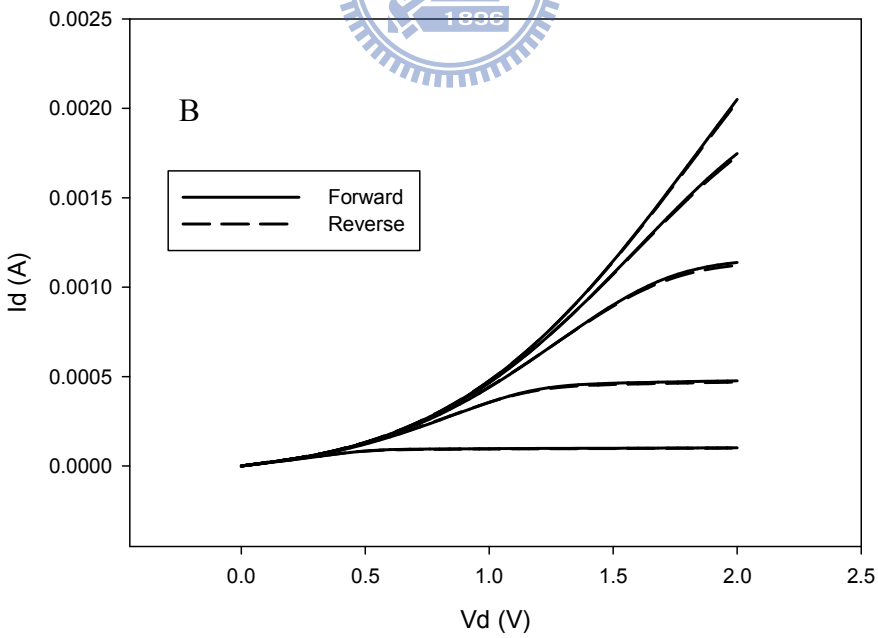


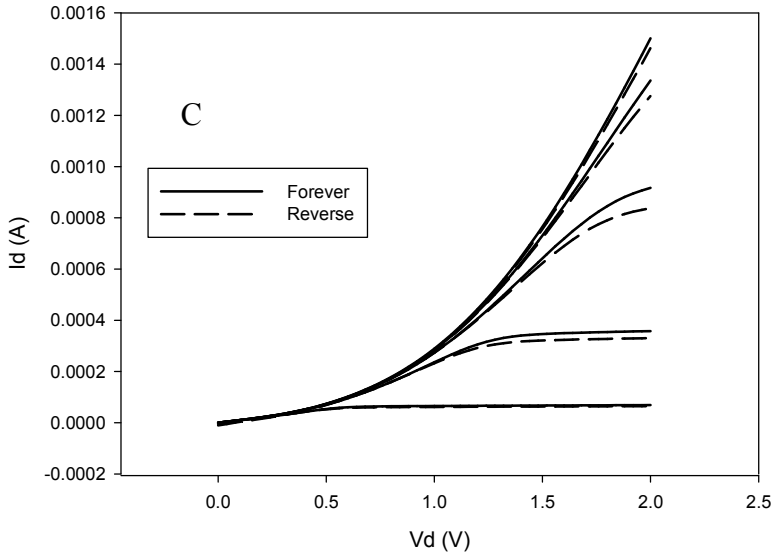
Fig. 3.19 Equivalent circuit diagrams considering the parasitic resistances under forward and reverse modes of operation.


A
Forward
Reverse
Id (A)
Vd (V)
0.0018
0.0016
0.0014
0.0012
0.0010
0.0008
0.0006
0.0004
0.0002
0.0000
0.0
0.5
1.0
1.5
2.0
2.5

a)


B
Forward
Reverse
Id (A)
Vd (V)
0.0025
0.0020
0.0015
0.0010
0.0005
0.0000
0.0
0.5
1.0
1.5
2.0
2.5

b)



c)

Fig. 3.20 The output characteristics of MOSFETs fabricated with double patterning technique. Channel length/width =0.4 μm /10 μm. (a) Device A. (b) Device B. (c) Device C.

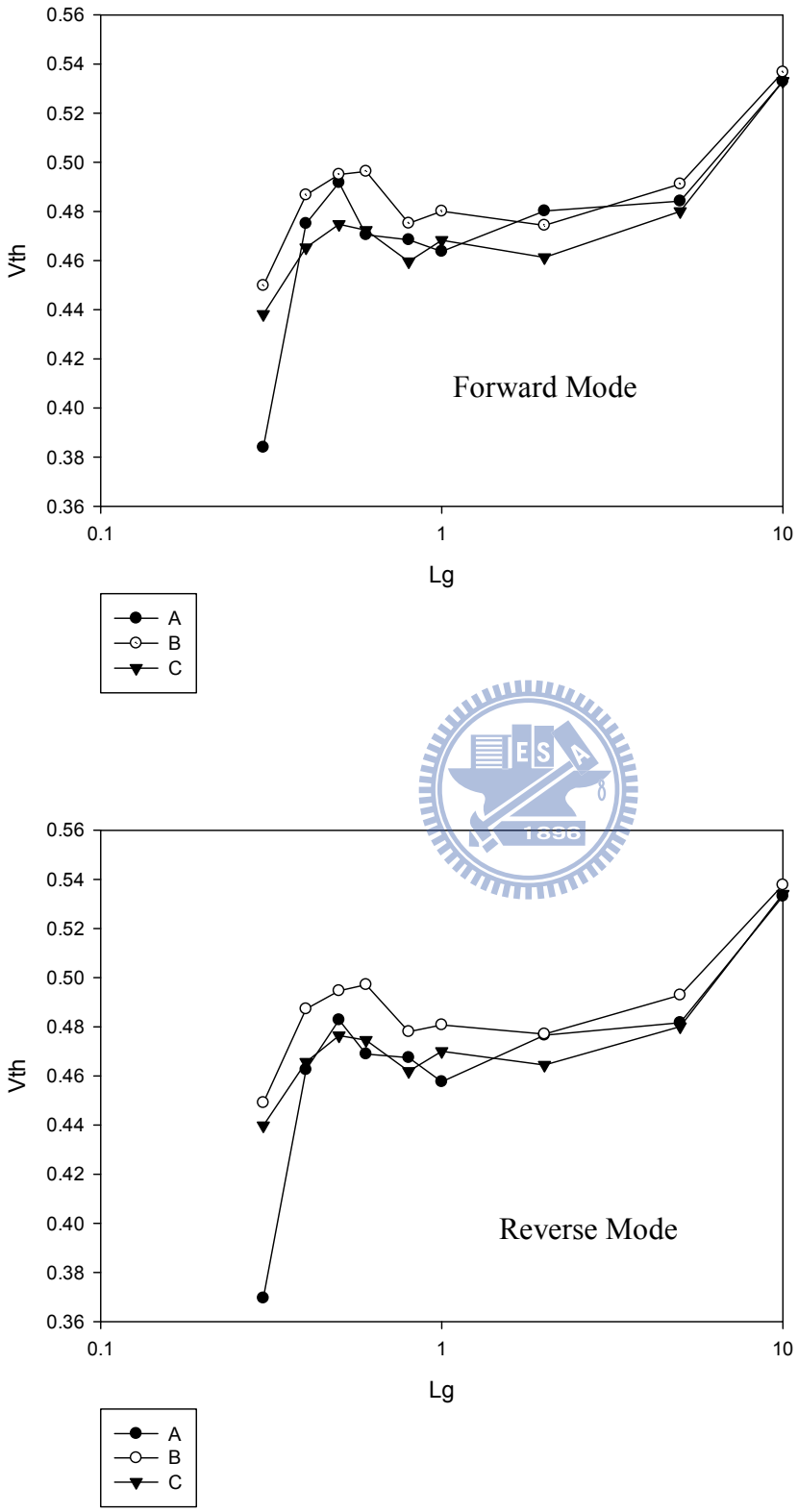


Fig. 3.21 Vth roll-off characteristics of the three types of devices.

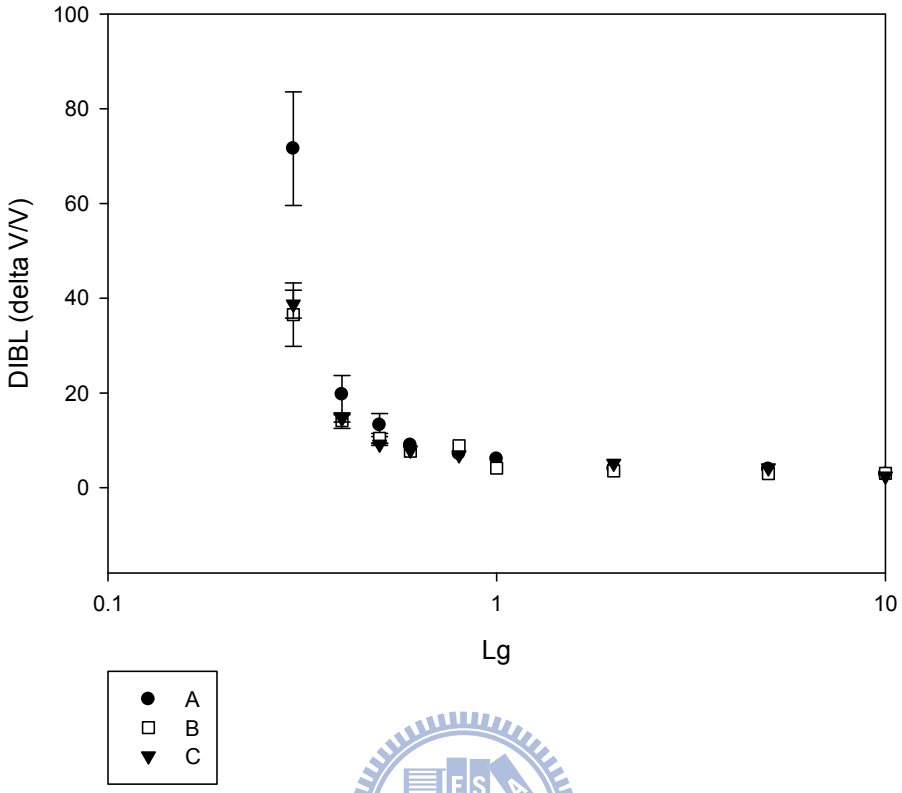


Fig. 3.22 DIBL characteristics of the three types of devices.

Fig. 4.1 Cross sectional view of a Green Transistor

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碩士論文題目：

使用 I 射線步進機的雙重圖形曝光技術以及其應用在元件製作之研究

A Study on Double Patterning Technique with i-line Stepper and Its Application to Device Fabrication