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High Breakdown P-Channel InSb MOSFET

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P-channel InSb MOSFET is fabricated by anodic oxidation and SiO evaporation for the MOS gate structure and by Cd diffusion for the source and drain. A breakdown voltage exceeding 11 V is obtained in the drain junction, which renders the drain current saturation fully observable. An on-off ratio of 10^4 in the drain current is also obtained, indicating that the present InSb MOSFET is useful for a good switching operation.

KEYWORDS: InSb p-n junction, MOSFET

InSb p-n junction diodes have been shown to be excellent photodiodes in the spectral range of 3-5 μm.[1,2] It is also known that InSb has a very high electron mobility and a high saturation velocity. These intrinsic properties make InSb an attractive material for the application to high-speed MOSFET devices. Furthermore, the monolithic approach to infrared imaging by the integration of MOSFET with photodiodes on InSb becomes highly desirable if considerations such as readout noise and switching speed are taken.[3] Though the photodiodes are reported to have excellent properties, the characteristics of fabricated InSb MOSFETs are still not satisfactory enough to be used in the monolithic approach. Shappir, Margalit and Kidron[4] had successfully fabricated an InSb p-channel MOS transistor with the source and drain defined by mesa etching in a Cd diffused p layer and the gate formed by evaporation of chromium and gold on top of a SiO_2 layer. However, a large drain current due to tunneling at the surface of the p^+ drain region under the overlapping gate caused the subthreshold characteristics to be insufficient for the switching operation. Fujisada[3] fabricated a planar-type p-channel InSb MAOSFET by anodic oxidation and sputtering for the MAOS gate, and Be ion implantation for the source and drain. An excellent on-off ratio of the order of 10^5 was obtained in the drain current. However, the device showed a maximum voltage of only -2 V, which was not large enough to observe complete saturation of the drain current. This imposed a limit on the FET, and efficiency operation in the saturation region was impossible. In order to have good subthreshold characteristics and high drain junction breakdown voltage, suppression of the tunnel current at the surface along with a high-quality InSb p-n junction is required.

In this letter, we report a p-channel MOSFET fabricated by a two-temperature-zone Cd diffusion for the source and drain on $(\bar{1}\bar{1}\bar{1})$-oriented n-type InSb with a carrier concentration of 1×10^{14} cm^{-3} at 77 K. The two-temperatur-zone diffusion technique was described in a previous publication.[5] The diffusion was carried out with the Cd source at 380°C and InSb substrate at 440°C. Since the diffusion was carried out with separate Cd source and InSb substrate temperatures, it is believed that, while still being able to maintain the substrate surface morphology, the carrier concentration at the surface of the p^+ drain region can be increased sufficiently to protect against the formation of a field-induced junction due to band bending. This advantage provided by the two-temperature diffusion technique is crucial for the preparation of high-quality InSb FET since the field-induced junction formed under the gate overlapping the reverse biased drain junction is known to usually be the origin of the surface tunnel current and the cause of early drain junction breakdown.[6] The source and drain regions were then defined by etching through the diffused p-layer forming a mesa structure. The wafer was then anodized in 0.1 N KOH solution by a Keithley 220 current source at a current density of 7×10^{-4} A/cm^2 for 5 minutes. The resulting anodized oxide had a thickness of roughly 700 Å. After the anodic oxidation, a SiO layer with a thickness of 1500 Å was evaporated onto the surface; then the contact windows were etched by a plasma etcher, followed by Cr–Au evaporation. Figure 1 shows a cross-sectional view of the InSb MOSFET used in this study. The channel length and width were 50 μm and 200 μm, respectively. All the *I-V* characteristics were measured in the dark at 77 K with the source of the FET connected to the ground.

Shown in Fig. 2 are the drain current-drain voltage characteristics for different gate voltages. The device clearly displays typical MOS characteristics in the ohmic

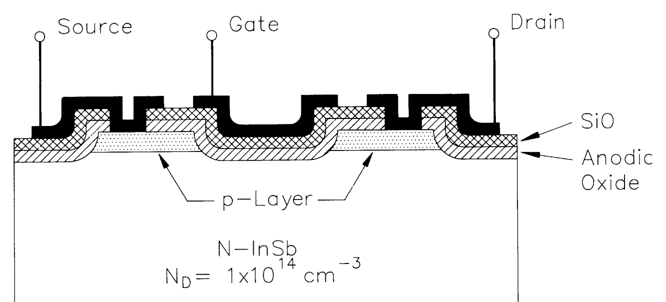

Fig. 1. Cross-section view of InSb MOSFET used in this work.

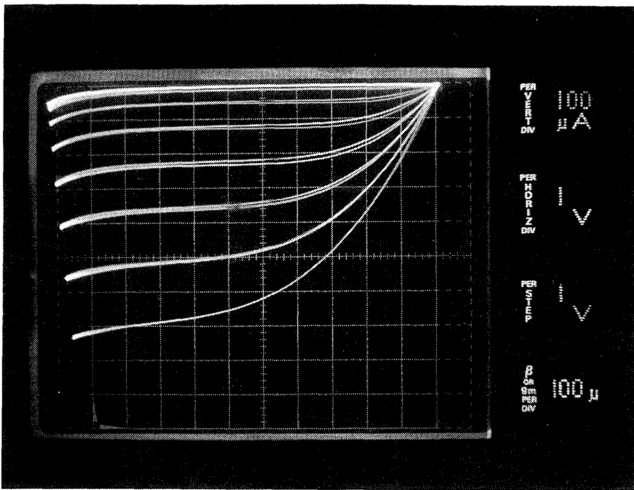

Fig. 2. Drain current-Drain voltage characteristics as a function of gate voltage. Horizontal: 1 V/div. Vertical: 100 μA./div. Gate Voltage: 10 steps with 1 V increments.

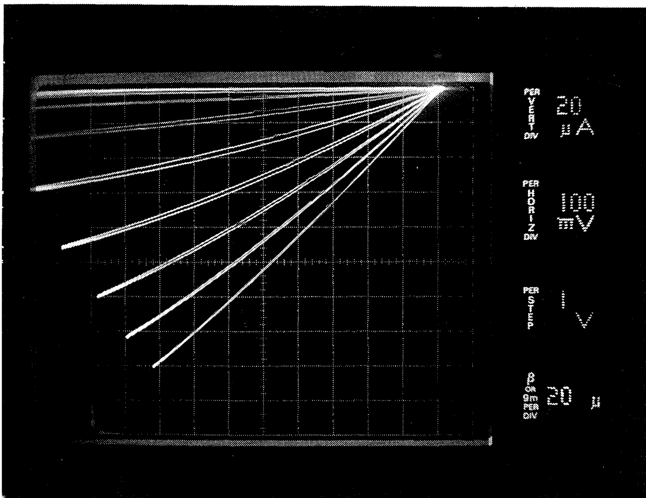

Fig. 3. Drain current-drain voltage in the ohmic region. Horizontal: 100 mV/div. Vertical: 20 μA/div. Gate voltage: 10 steps with 1 V increments.

and saturation regions. The high breakdown voltage (exceeding 11 V) enables clear observation of the saturation region, which was not observed in the device reported previously by Fujisada.[3]

The *I-V* characteristics in the ohmic region are shown in Fig. 3. The drain current in this region versus gate voltage for $V_{DS}=500$ mV, as taken from Fig. 3, is plotted in Fig. 4. The data fit the well-known approximate relation,

$$I_D=(w/L)C_{ox}\mu V_D(V_G-V_T),$$

where *w* and *L* are the length and width of the channel, respectively, C_{ox} is the gate oxide capacitance per unit area, and V_T is the threshold voltage. From the slope of the straight line and its intersection with the abscissa, the surface hole mobility μ_p and threshold voltage are determined to be 320 cm^2/V·s and 4.2 V, respectively. It is also observed from Fig. 2 that the drain current begins to

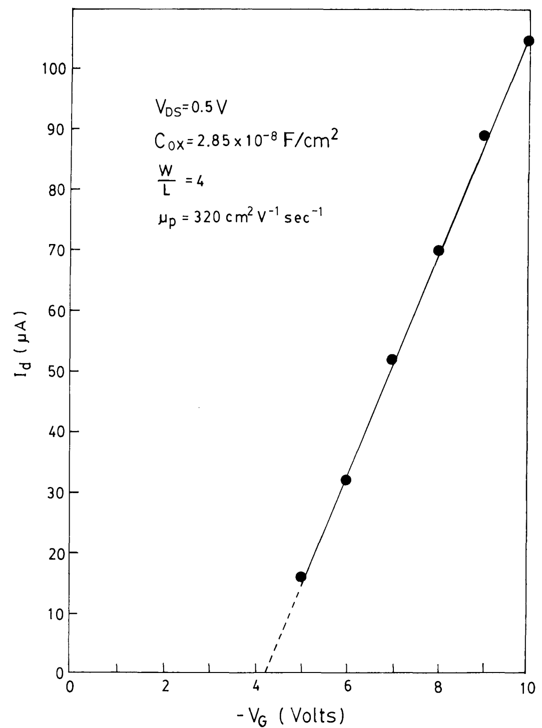

Fig. 4. Drain current plotted against gate voltage for $V_{DS}=500$ mV.

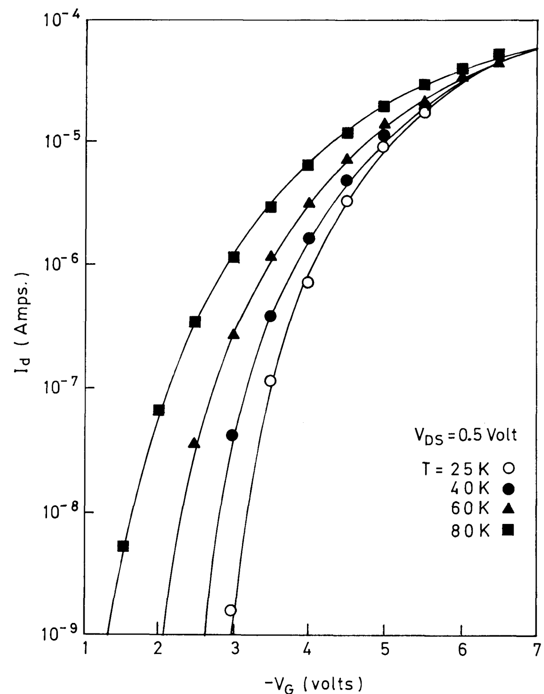

Fig. 5. Transfer characteristics of InSb MOSFET with temperature as a parameter.

saturate at a drain voltage $V_{D_{sat}}=V_G-V_T$, which also agrees well with the MOS transition theory. The threshold voltage was found to depend on the history of the gate voltage application, as has been reported by Fujisada.[3] This is understandable because the well-known hysteresis effect is usually present in such MOS structures.

Shown in Fig. 5 are the *I-V* characteristics for $V_{DS}=500$ mV in the subthreshold region at four different temperatures $T=25$, 40, 60, 80 K. For voltages below the threshold, the drain current depends roughly exponentially on the gate voltage. Since leakage current due to tunneling at the surface of the p^+ drain region under the gate is known to increase sharply with the decrease of the gate voltage,[7] the present MOS transistor clearly showed no indication of such a large leakage current. The subthreshold swing, defined usually as the gate voltage swing required to reduce the current by one order, can be calculated from Fig. 5. The subthreshold swing at 80 K determined from the current varied from 10^{-6} to 10^{-8} amps was roughly 600 mV/order. This value is to be compared with that of roughly 700 mV/order calculated from the reported data of Fujisada.[3] Also noted in Fig. 5 is that the subthreshold swing is reduced to 400 mV/order as the temperature is decreased to 25 K. This improvement is expected, but does not agree exactly with the predicted kT/q dependence.[8] An on-off ratio of the order of 10^4 was obtained in the drain current. This is comparable to that reported by Fujisada.[3]

In conclusion, we have fabricated a p-channel InSb MOSFET with high breakdown voltage and good subthreshold behavior. Breakdown voltage exceeding 11 V was observed, which rendered the drain current saturation region fully observable. An on-off ratio of 10^4, comparable to that of devices reported previously, is also realized. It is believed that such a high-quality MOSFET was made possible by using the so called two-temperature-zone Cd diffusion technique. The problems of threshold voltage shift and low channel mobility are still present. An oxide deposition process, such as LTCVD, with the vapor etch technique may be the solution to these problems.

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