國立交通大學

電控工程研究所

碩士論文

模組化在單迴路積分三角類比數位轉換器中積分器充放電雜訊與諧波失真模型

Modeling Settling Noises and Distortions for Single-Loop Sigma-Delta Modulators

研究生：謝武璋

指導教授：陳福川 教授

中華民國九十八年九月

模組化在單迴路積分三角類比數位轉換器中積分器充放電雜訊與諧波失真模型

Modeling Settling Noises and Distortions for Single-Loop Sigma-Delta Modulators

研 究 生：謝武璋　　Student：Wu-Chang Hsieh
指導教授：陳福川　　Advisor：Fu-Chuang Chen

國 立 交 通 大 學
電 控 工 程 研 究 所
碩 士 論 文

A Thesis
Submitted to Department of Electrical and Control Engineering
College of Electrical Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Master
In

Electrical and Control Engineering

September 2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年九月

模組化在單迴路積分三角類比數位轉換器中積分器充放電雜訊與諧波失真模型

研究生：謝武璋　　指導教授：陳福川 教授

國立交通大學

電控工程研究所

摘要

交換式電容積分器已經被廣泛的應用在積分三角轉換器的領域中,且由於積分器中電容不完全的充放電轉換特性(積分器充放電問題),使得此積分器充放電問題與其效能有著高度的相關性。因此,在現今已發表出之積分三角轉換器中,積分器充放電問題是一個很艱難且棘手的設計課題。而因爲積分器充放電問題的高複雜性,相關的誤差和失真的解析模型實際上是不存在的。此篇論文的目地在於利用了非線性擬合方法和輸出端頻譜預測技術來探討單迴路積分三角轉換器的積分器充放電問題。經由上面的分析,我們可以獲得積分器充放電問題誤差和失真的封閉解,且此封閉解可以經由積分三角轉換器中的系統參數所組成的函式呈獻出來。我們同時利用了行爲層的模擬以及電晶體層次的電路模擬來驗證此解析模型的正確與精確性。由上面的驗證結果顯示出此兩種模擬結果與我們的解析模型有著相當合適的一致性。

Modeling Settling Noises and Distortions for Single-Loop Sigma-Delta Modulators

Student：Wu-Chang Hsieh　　Advisor：Dr. Fu-Chuang Chen

Institute of Electrical and Control Engineering

Nation Chiao Tung University

ABSTRACT

Switch-capacitor (SC) integrators have been widely used in sigma-delta modulators (ΣΔ Ms) and the performances of SC integrators depend highly on their incomplete charge-transfer (settling problem) behavior. Therefore, the settling problem is a crucial design concern in well-published switch-capacitor ΣΔ Ms. Due to the complexity of settling problem, analytic models for related noises and distortions are virtually non-existent. The aim of this paper attempts to explore the settling problems on single-loop ΣΔ Ms by employing nonlinear fitting methods and output spectrum prediction techniques. Closed forms of settling error and settling distortion models are acquired, and are represented as functions of ΣΔ modulator system parameters. Both behavior simulations and transistor-level-circuit simulations are employed to verify these analytical models. The results of above validation showed an appropriate level of consistence between the two simulations and our analytical models.

Acknowledgment

此篇論文的完成首先要感謝陳福川教授在我兩年的碩士班過程中指導我在研究以及學術上的想法,讓我能夠獲得老師在學術上的經驗以自我成長。其次要感謝畢業的黃俊傑學長在我有所疑問時的輔助以及幫忙,讓我能達到事半功倍的研究效果。同時要感謝畢業的王文佑以及沈柏年學長在同實驗室相處期間的一切幫助,還有 608 lab 的同學謝智隆、黃瑞祺以及學弟歐嘉昌、盛子恩和我在研究上的互相交流、討論。

感謝我的父母、雅如姐姐和其餘長輩們在我求學期間的一切支持與鼓勵、怡人姐姐以及順欽姐夫在生活上的照顧。也謝謝子誠、瑋琳、柏元、柏勛、立杰這群朋友帶給我在學校生活之外的成長與歡樂。最後感謝我最愛的女朋友,遠在 Loughborough University 的怡今(princess of smile)一路給我心靈上以及情感上的陪伴,讓我能順利渡過這兩年碩士生活。

Contents

Lists of Tables

Lists of Figures

List of Symbols

Symbols

V_{LSB}	Quantizer step size
V_{OS}	Maximum output swing of op-amp
OSR	OverSampling Ratio
n	Order of the Sigma-Delta modulator
B	Number of bits in the quantizer
f_S	Sampling Frequency
f_B	Signal Bandwidth
V_{ref}	Reference Voltage of the quantizer
A_0	Finite Gain of OTA
f_{in}	Frequency of the input signal
ϕ_i	ith phase of a nonoverlap clock
A_{in}	Amplitude of input signal
$\sigma_{jit.}$	standard deviation of clock jitter
C_S	Sampling capacitor
C_I	Integrating capacitor
C_L	Load capacitor of OTA
C_{Logic}	The loading capacitors of CMOS logic gates
C_{gate}	The gate capacitances of all CMOS transmission gates
C_{OX}	The capacitance per unit area of the gate oxide
V_S	Input signal plus feedback DAC signal
τ_1	Time constant of input branch
σ_{VS}	Standard deviation of V_S
τ_2	Time constant of integrator output settling
a_i	gain coefficient of i th integrator

η	percentage of the bottom plate parasitic
T	Absolute temperature
R	Switch ON resistance
N	quantizer levels
gm1	Amplifier transconductance
Pr()	Probability of some condition
$\sigma_{cap.}$	Mismatch of unit capacitance
k	Boltzmann's constant (1.38×10^{-23}) J/K
α	OTA noise factor
$Erf[]$	Error Function
I_{OTA}	Total current of the OTA
I_B	Bias current of each transistor of the input differential pair of OTA
k_{OTA}	The ratio of the total current of the OTA to this bias current
f_{cl2}	The *GBW* of the OTA
V_{reff}	The overdrive voltage of the transistor of the input differential pair of OTA
k_{Cs}	The ratio between the summation capacitance of C_S in all stages and the one in the first stage
ε_0	The permittivity of free space
N_S	The number of the CMOS transmission gate in $\Sigma\Delta$ modulator

1.Introduction

1.1 Current Status and Background

Sigma-delta modulators(ΣΔ Ms) are widely employed in many modern applications such as telecommunications, multimedia, sensors-interface and precision measurement systems, especially used for implementation of analog-to-digital converters(ADCs) with high-resolution and low-power [1-10]. Compared to the traditional converters, ΣΔ modulators have achieved the most attraction recently in data converter systems due to their noise shaping and oversampling behavior that lead them to superior linearity and accuracy, simple realization, low sensitivity to circuit imperfection [11], and are more suitable for the implementation of A/D interfaces in modern standard CMOS technologies [12].

ΣΔ modulators can be implemented either with continuous-time(CT) or switched-capacitor (SC) approach. The most popular approach is based on a sampled-data solution with SC integrators implementation. Its incomplete charge transfer and the characteristics of the operational amplifiers decline drastically the performance of ΣΔ modulators. As the clock frequency increases in ΣΔ modulators to cope with wideband applications, SC integrators defective settling problem become the bottle neck in present designs. Due to the complexity of settling problem, analytic models for related noises and distortions are virtually non-existent. Transient charge transfer in SC integrators and proposed several time-domain-based behavioral descriptions have been studied by former authors[13-16], which can be used in behavior simulations. Behavioral simulations are time-consuming, unobvious, and difficult to observe settling affection in entire modulators from other nonlinearities. In addition, analytical efforts have been actually seen before. In [17-19], a thorough transient analysis for the charge-transfer error was carried out by assuming linear feedback. However, their results cannot be directly applied due to the highly nonlinear

feedback inherent in the $\Sigma\Delta$ modulators. In [20-21], the distortion due to operational transconductance amplifier (OTA) dynamics has been analyzed and modeled. It uses power expansion and nonlinear fitting to obtain analytical model to represent harmonic distortion of single bit modulator as a function of the slew-rate (SR), gain-bandwidth (GBW), and nonlinear DC gain. Unfortunately, the author provides little or no insight on how oversampling-ratio (OSR) can be influenced the system performance, and the settling noise model was not discussed. It is coarsely assumed in [22] that the settling noise is white noise contribution and the associated power spectral density (PSD) is constant in the sampling interval, but this assumption is divergent in comparison to the realistic phenomenon.

1.2 Motivation and Aims

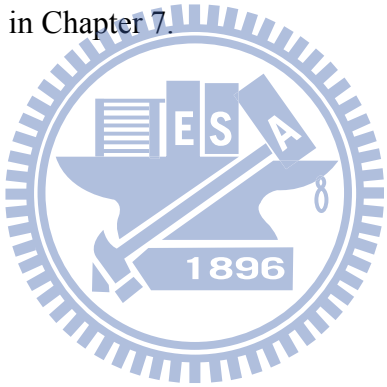
ΣΔ modulators are extremely nonlinear sampled-data circuits, and hence, the designing of ΣΔ modulators would be a predictably tough task. As several studies have suggested the one of the best way of designing ΣΔ modulators is achieved by using the so-called behavioral simulation technique [23-24]. In this approach the modulator is separated into a set of sub-blocks. These blocks are described by equations that express their outputs in terms of their inputs and their internal related parameters. Thus, the accuracy of simulation depends on how closely those equations describe the actual behavior of each building block. From the technique discussed above, the ΣΔ modulator implementation based on numerical optimization [21,25-26] is previously reported, which are based on an iterative optimization process in which the synthesis problem is formulated as a cost function, and requires many computation until best performance is achieved. If the best performance achieved still cannot meet the design specification, this strategy can provide helpful clue about the dominating nonlinearity. In contrast, design and optimization based on analytical noise and distortion models can be a more efficient and dependable approach [27, 28], as long as all of the important noise and distortion models are available. There have been a number of literatures that many noise and distortion models have derived for ΣΔ modulators, but analytical model for switched-capacitor(SC) integrators settling noise model is never seen in the literatures, and it seems premature to discuss the settling distortion model without specifying the effect of quantizer bit number. For these reasons, the major goal of this paper is to provide the settling noise model and to supplement the finding of the earlier settling distortion model.

The settling problems of the SC integrators are mainly caused by non-idealities of OTA such as finite dc gain, finite GBW, and SR limitations. Our following works show that these non-idealities will alter the ideal SC integrators transfer function and

cause the nonlinear transfer characteristics, which not only cause signal distortions, but also reflect high-frequency noises into base band. In light of these concerns, the purpose of our study is to obtain closed-form of settling error and settling distortion analytical models by using nonlinear fitting methods and output spectrum prediction techniques. These analytical models are represented as functions of ΣΔ modulator system parameters. Both behavior simulations and HSPICE circuits are employed to verify these analytical models, and the results show that our analytical models are sufficiently accurate.

1.3 Organization

This paper is organized as follows. In Chapter 2, the basic architectures and knowledge of ΣΔ modulators are introduced. In Chapter 3, the motivation of ΣΔ modulators settling problem and characteristics of the SC integrator input end are discussed. In Chapter 4, the formulation of analytical settling noise power model for first, second and high order ΣΔ modulators are presented with several analytical discussions. In Chapter 5, we derive the settling distortion model, and discuss the effects between the system parameters with settling distortion. In Chapter 6, the behavior simulations and HSPICE-circuit simulations are used to validate our model. Moreover, we propose several analytical discussions. Finally, we summarize some conclusions and discussions in Chapter 7.



2.
Architectures of ΣΔ Modulators

This section we introduce basic architectures of ΣΔ modulators. In our paper, we will focus on the single-loop module for ΣΔ modulators. First, second, and high order single-loop ΣΔ modulators will be discussed. In order to understand the system performance merits used to specify the behavior of ΣΔ modulators, several specifications concerning the performance have been discussed [28], and we incorporate it finally.

2.1 First-Order Sigma-Delta Modulator

Fig. 2.1. shows a standard architecture of first order sigma-delta modulator. Here, H(z) is $\frac{Z^{-1}}{1-Z^{-1}}$; Analyze transfer function H(z) from time-domain, it indicates that output signal m(t) is obtained by adding the delayed input signal n(t-1) and the delayed output signal m(t-1), so we can express a complete first-order ΣΔ modulator as Fig. 2.1.

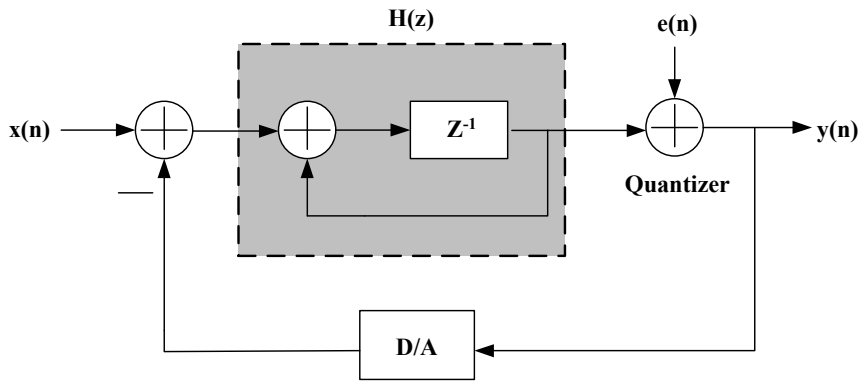


Fig. 2.1 First-order ΣΔ modulator

H(z) in Fig. 2.1 is indicated the effects of delay and accumulation, this is equivalent with an integrator in circuit design, so the three circuits components of ΣΔ

modulator are integrator, quantizer and DAC in the feedback path. A first order ΣΔ modulator's output can represent as

$$Y(z)=z^{-1}X(z)+(1-z^{-1})E(z) \qquad (2.1)$$

From (2.1) we can find the signal transfer function is as a delay function, and noise transfer function is as a high pass filter, moves the noise to high frequency. In order to derive PSNR(Peak Signal-to-Noise Ratio) of first order ΣΔ modulator, we must get the magnitude of $N_{TF}(z)$ and $S_{TF}(z)$ in the frequency domain, so we substitute z with $e^{j2\pi \cdot f/f_s}$, and get $|S_{TF}(f)|$ and $|N_{TF}(f)|$ respectively as:

$$|S_{TF}(f)| = |z^{-1}| = |e^{-j2\pi \cdot f/f_s}| = 1 \qquad (2.2)$$

$$N_{TF}(f) = 1 - e^{-j2\pi \cdot f/f_s} = \sin(\frac{\pi f}{f_s}) \times 2j \times e^{-j\pi \cdot f/f_s}$$

$$\Rightarrow \quad |N_{TF}(f)| = 2 \cdot \sin(\frac{\pi f}{f_s}) \qquad (2.3)$$

So the quantization noise in base band $\pm f_B$ can obtain (2.3)

$$P_Q = \int_{-f_B}^{f_B} S_e^{\,2}(f) \cdot |N_{TF}(f)|^2 df = \int_{-f_B}^{f_B} \frac{V_{LSB}^{\,2}}{12 \cdot f_s} \cdot \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 \cdot df \qquad (2.4)$$

Because that f_B is much lower than f_s, so $\sin(\pi f/f_s)$ is approximate equal to $(\pi f/f_s)$, and P_Q is as

$$P_Q = \frac{V_{LSB}^{\,2}\pi^2}{36} \cdot (\frac{1}{OSR})^3 = \frac{FS^2 \cdot \pi^2}{36 \cdot 2^{2B} \cdot OSR^3} \qquad (2.5)$$

Assume that input signal is sinusoidal, expressed as $V_{in}(t) = A \sin\omega t$, so the input signal power $V_{in(rms)}^{\,2}$ is as (2.6). In (2.6), we define the amplitude of input signal is the full scale of reference voltage

$$V_{in(rms)}^{\,2} = \frac{1}{T}\int_{-T/2}^{T/2} (A \cdot \sin\omega t)^2 \cdot dt = \frac{A^2}{2} = \frac{(2A)^2}{8} = \frac{FS^2}{8} \qquad (2.6)$$

From (2.5) and (2.6), if we have the maximum signal power, then PSNR is as (2.7)

$$PSNR = 10\log(\frac{P_{signal}}{P_Q}) = 10\log(\frac{3}{2}2^{2B}) + 10\log[\frac{3}{\pi^2}(OSR)^3]$$

$$= 6.02B + 1.76 - 5.17 + 30\log(OSR) \quad (2.7)$$

From (2.7), we find that each octave of OSR, PSNR will increase 9dB, increase 1.5 bit in resolution. Compare (2.7) with A/D converter only has oversampling effect; we can find that 1st order noise shaping increases the performance of ΣΔ modulator.

2.2 Single-Loop Second-Order Sigma-Delta Modulator

When the discrete time filter H(z) in Fig. 2.1 is replaced by two cascade integrator, then it is a second order ΣΔ modulator, output of the first integrator is only connecting with the input of the second integrator, it is shown in Fig. 2.2

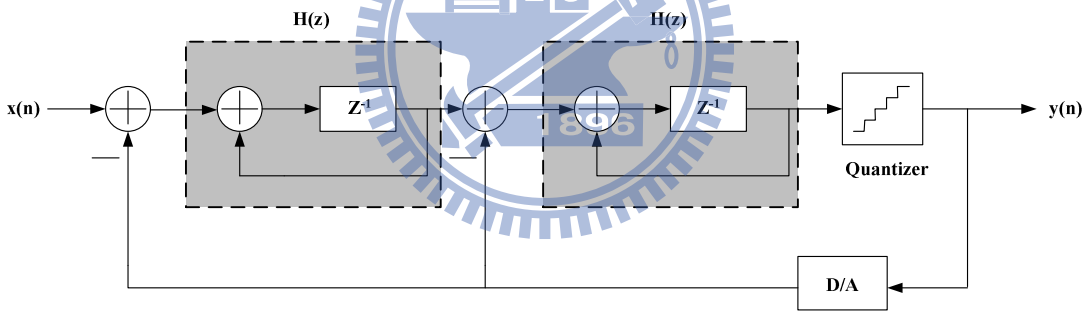


Fig. 2.2 Single loop second order ΣΔ modulator

Then the output of it can easily be derived as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z) \quad (2.8)$$

where S_{TF} and N_{TF} is as

$$S_{TF}(z) = z^{-2} \quad (2.9)$$

$$N_{TF}(z) = (1- z^{-1})^2 \quad (2.10)$$

Using the same method in (2.3) (2.4), we can obtain

$$|S_{TF}(f)| = 1 \quad (2.11)$$

$$\left|N_{TF}(f)\right| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \qquad (2.12)$$

$$P_Q = \frac{V_{LSB}{}^2 \cdot \pi^4}{60 \cdot OSR^5} = \frac{FS^2 \cdot \pi^4}{2^{2B} \cdot 60 \cdot OSR^5} \qquad (2.13)$$

So finally, PSNR of the second order ΣΔ modulator is as

$$PSNR = 10\log\left(\frac{P_{signal}}{P_Q}\right) = 10\log\left(\frac{3}{2}2^{2B}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

$$= 6.02B + 1.76 - 12.9 + 50\log(OSR) \qquad (2.14)$$

In the single loop second order architecture, each octave of OSR can increase PSNR by 15 dB, it is equivalent to 2.5 bit in resolution. If we compare (2.12), (2.3) with $\left|NTF(f)\right|=1$ that without noise shaping, as Fig. 2.3, we can find that in our needed signal bandwidth, the quantization noise is highest when $\left|NTF(f)\right|=1$, and that with second order noise shaping is smallest among this figure.

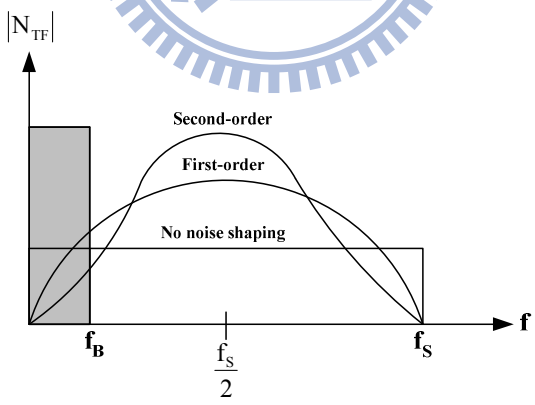


Fig. 2.3 Comparison of noise shaping techniques

2.3 Single-Loop High Order Sigma-Delta Modulator

The simplest way to extend a ΣΔ modulator towards an arbitrary *L*th-order filtering consists of including *L* integrators before the quantizer. Extending the second order ΣΔ modulator in Fig. 2.2, the architecture in Fig. 2.4 can be obtained, which is a single loop high order ΣΔ modulator, its output would yield

$$Y(z) = z^{-L}X(z) + (1-z^{-1})^{L}E(z) \qquad (2.15)$$

Here L is order, from the derivation in Section 2.1 and Section 2.2 we can get the quantization noise P_Q in signal bandwidth is as

$$P_Q = \frac{V_{LSB}^{2}}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot \left(\frac{1}{OSR}\right)^{2L+1} \qquad (2.16)$$

and its PSNR is

$$PSNR = 6.02B + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \qquad (2.17)$$

In the application of high order ΣΔ modulator, (6L+3) dB increases in SNR when OSR is octave, so PSNR can be raised by increasing the order of the system, especially at large oversampling ratio. But sometimes in high order architecture, the performance will be worse than result predicted by (2.14), because of the stability problem, it will make less effective noise shaping function, so the quantization noise will not be suppressed completely.

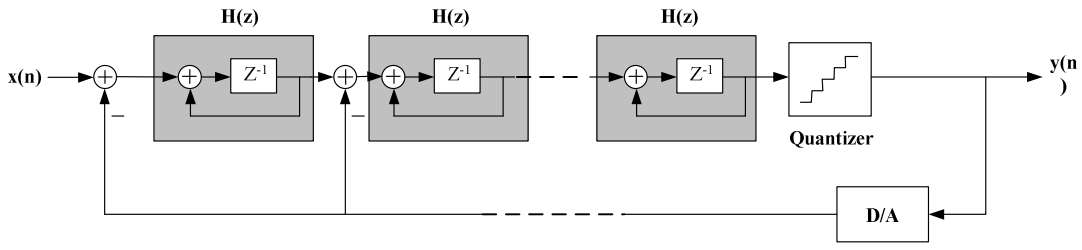


Fig 2.4 Single-loop high order ΣΔ modulator

2.4 Quantizer Nonlinearity Of Sigma-Delta Modulator

In this section, we supplement some notion about the quantizer. The quantization operation is inherently nonlinear because the quantizer error is determined from the quantizer input signal. For convenience, we usually model the quantizer as a linear model and approximate the quantization noise as a white noise. This approximation is made when the quantization error has the following properties, which we refer to collectively as the "input-independent additive white noise approximation" [11]:

Property 1. ε_n is statistically independent of the input signal or ε_n is uncorrelated with the input signal.

Property 2. ε_n is uniformly distributed in $[-\Delta/2, \Delta/2]$.

Property 3. ε_n is an independent identically distributed (i.i.d.) sequence or ε_n has a flat power spectral density.

where ε_n is the error sequence and Δ is the distance between output levels. Therefore, the quantization error from $\Sigma\Delta$ modulators is typically not white. For dc inputs, the quantization noise spectrum consists of discrete spectral lines, called idle channel tones or pattern noise. For ac inputs, the quantization noise spectrum comprises all harmonics of system input frequency and amplitude as one might expect with a nonlinear device [29]. One can view this effect as a time-domain distortion and therefore argue that the converter actually has less resolution than rms measurements. In fact, the decorrelation between the quantization error ε_n and the input signal increases with the modulator order. This, together with circuit noise acting as a dithering signal in practical implementations, greatly helps to palliate the coloration of quantization error ε_n, the dithering method have been discussed in [11], and we will

use it in the latter chapter.

2.5 Performance for a ΣΔ Modulator

We collect several performance indices which often used to specify the behavior of ΣΔ modulator.

- **Signal to Noise Ratio:** The SNR of a data converter is the ratio of the signal power to the noise power, measured at the output of the converter for a certain input amplitude. The maximum SNR that a converter can achieve is called the peak SNR.
- **Signal to Noise and Distortion Ratio:** The SNDR of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for a certain input amplitude. The maximum SNDR that a converter can achieve is called the peak SNDR.
- **Dynamic Range at the input:** The DRi is the ratio between the power of the largest input signal that can be applied without significantly degrading the performance of the converter, and the power of the smallest detectable input signal. The level of significantly degrading the performance is defined as the point where the SNDR is 6 dB bellow the peak SNDR. The smallest detectable input signal is determined by the noise floor of the converter.
- **Dynamic Range at the output:** The dynamic range can also be considered at the output of the converter. The ratio between maximum and minimum output power is the dynamic range at the output DR_o, which is exactly equal to peak SNR.
- **Effective Number of Bits:** ENOB gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This numbers also includes the distortion components and can be calculated as:

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \tag{2.18}$$

- **Overload Level:** OL is defined as the relative input amplitude where the SNDR is decreased by 6dB compared to peak SNDR

Typically, these specifications are reported using plots like Fig. 2.5. This figure shows the SNR and SNDR of the ΣΔ converter versus the amplitude of the sinusoidal wave applied to the input of the converter. For small input levels, the distortion components are submerged in the noise floor of the converter. Consequently, the SNDR and SNR curves coincide for small input levels. When the input level increases, the distortion components start to degrade the modulator performance. Therefore, the SNDR will be smaller than the SNR for large input signals. Note that these specifications are dependent on the frequency of the input signal and the clock frequency of the converter. Fig. 2.5 also shows that SNDR curves drop very fast once the overload point is achieved. This is due to the overloading effect of the quantizer which results in instabilities.

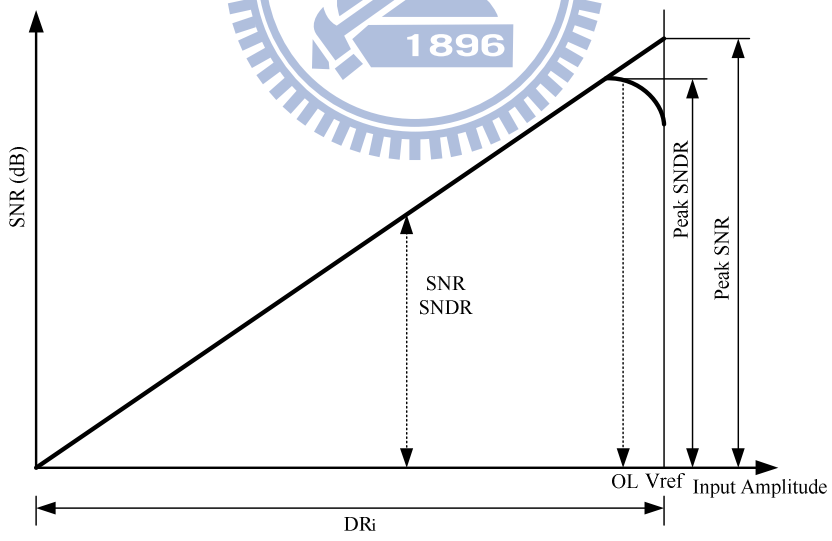


Fig. 2.5 Performance characteristic of a ΣΔ converter

3.
Investigation of $\Sigma-\Delta$ Modulators Settling Problems

In practice, dynamic limitations in switched-capacitor integrators, basically due to the finite GBW and SR of the amplifiers, induce non-linear behavior in the charge transfer. The impact of the associated output settling problem on the modulator performance will be higher, the higher the sampling frequency. In order to understand why there is such serious, it is necessary to examine the evolution of the notion of settling problem. Previous papers have mentioned the settling problem [15,30]. Therefore, in this section, we firstly clearly define the settling error in switched-capacitor integrators. Due to the input of SC integrator, called V_S, dramatically affect the SC integrator performance, so we examine the properties of V_S later. We focus on second order module, and the procedure of first, high order module will be similar. Since the settling problem at later stages are less influential due to noise shaping, so we only consider the settling problem of first stage integrator. Fig. 3.1 indicates a standard architecture of second order sigma-delta modulators. As stated before, where H(Z) = $\frac{Z^{-1}}{1-Z^{-1}}$ is the transfer function of switched-capacitor integrator, a1=0.5 and a2=2 are used for stability of entire modulator. The Fig. 3.2 shows a typical scheme of switched capacitors integrators with DAC branches. Here, C_μ is the unit capacitor whose capacitance value is $C_s/2^B$.

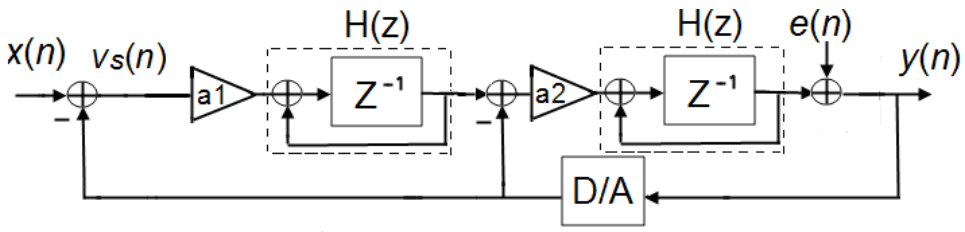


Fig. 3.1. Single loop second order ΣΔ modulator

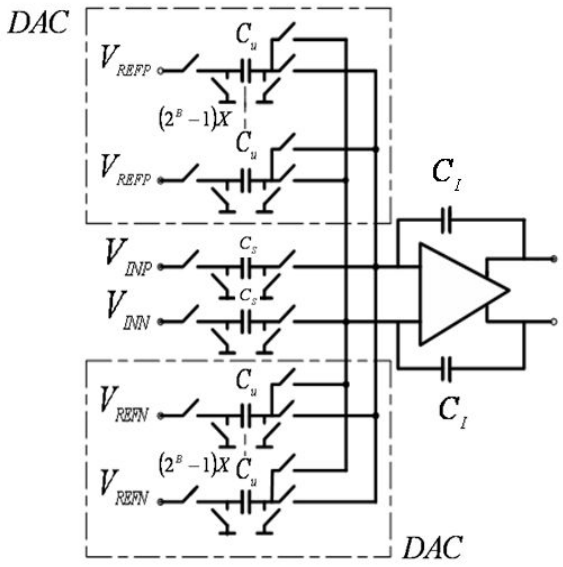


Fig. 3.2. A typical SC integrator with DAC branches

3.1 **Settling Noise of Sampling Phase and Integration Phase**

Sampling and integration phase will be analyzed separately. Fig. 3.3 illustrates sampling and integration phase of SC integrators with the MOS switched on-resistance *R* and the transconductance of OTA, *gm1*. Let the output parasitic capacitor be $C_L \cong \eta \cdot C_I$, where η is the percentage of bottom plate parasitic, assumed to be 20%[31]. In Fig. 3.3(a), the voltage V_S represents the difference between the sinusoid input signal and the feedback signal from DAC:

$$V_S(z) = X(z) - Y(z) \tag{3.1}$$

As stated before, in a second-order ΣΔ modulator, modulator output signal $Y(z)$ is the time delay version of $X(z)$ plus high-pass filtered (noise shaped) quantization noise $(1-z^{-1})^2 E(z)$. Therefore,

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2 E(z) \tag{3.2}$$

Combining（3.1）and（3.2）, $V_S(z)$ can be written as

$$V_S(z) = X(z)\left[1 - z^{-2}\right] - (1 - z^{-1})^2 E(z) \tag{3.3}$$

It is sampled by C_s, so C_s is charged in the half clock period $T/2$ to the voltage V_{CS}:

$$V_{CS} = V_S \cdot [1 - \exp(-\frac{T}{2 \cdot \tau_1})] \tag{3.4}$$

where $\tau_1 = R_s \cdot C_s$ is the time constant of the sampling phase in the input branch. So the setting error during the sampling phase is:

$$\varepsilon_1 = V_S \cdot \exp(-\frac{T}{2 \cdot \tau_1}) \tag{3.5}$$

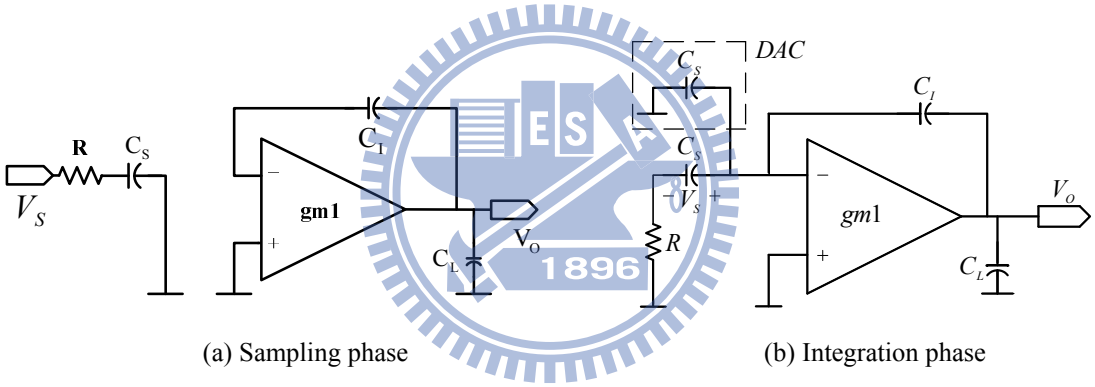


Fig. 3.3 Switched capacitor integrator diagrams

Next, we consider the integration phase shown in Fig. 3.3(b), where the 2^B unit capacitors are combined into C_s, and the 2^B DAC switches are neglected. The charge stored in sampling capacitor will be added to the integration capacitor and this charge current is supplied by OTA. So when the slew rate and gain bandwidth are not large enough, the settling error ε_2 will become nonlinear. According to absolute value of V_S, three types of settling conditions will happen in the integrator output during integration phase, and the corresponding voltage errors ε_2 of these three conditions are [15]:

1. Linear settling: When the initial change rate of the integrator output voltage (V_o) is smaller than the OTA slew rate (SR).

$$\varepsilon_2 = a_1 \cdot V_S \cdot \exp(-\frac{T}{2 \cdot \tau_2}),$$

when $0 < |V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2$ (3.6)

2. Partial slewing: The initial change rate of V_o is larger than SR, but it gradually decreases until it is below the slew rate.

$$\varepsilon_2 = SR \cdot \tau_2 \cdot \mathrm{sgn}(V_S) \cdot \exp(\frac{a_1 \cdot |V_S|}{SR \cdot \tau_2} - \frac{T}{2\tau_2} - 1),$$

when $\frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S| < (\frac{T}{2} + \tau_2)\frac{SR}{a_1}$ (3.7)

3. Fully slewing: The initial change rate of V_o is larger than SR, and it maintains above SR in the $T/2$ interval.

$$\varepsilon_2 = a_1 \cdot V_S - SR \cdot \mathrm{sgn}(V_S) \cdot \frac{T}{2}$$

when $|V_S| > \frac{SR}{a_1}(\frac{T}{2} + \tau_2)$ (3.8)

where SR is the slew rate of OTA, and $\tau_2 = \frac{1 + 2\pi \cdot GBW \cdot R \cdot Cs}{2\pi \cdot GBW}$ [30] is the time constant in the integration phase, with GBW being the equivalent gain bandwidth in the integration phase. The capacitor loading in OTA output during this phase is heavier than in the sampling phase, and is [28]

$$C_{L2} = 2C_S + C_L \cdot \frac{C_I + (2C_S)}{C_I} \quad (3.9)$$

The GBW is given by

$$GBW = \frac{gm1}{C_{L2} \cdot 2\pi} \quad (3.10)$$

3.2 **Properties of** V_S

In this section, we separately discuss the time-domain and frequency-domain properties of V_S to find out the time-domain probability distribution and the P.S.D of V_S. These properties will be used to do nonlinear fitting and spectrum construction of settling noise in next chapter.

Firstly, we need to find the V_S time-domain statistical property. Simulations results (using SIMULINK) on a second-order ΣΔ modulator with $a_1 = 0.5$, $a_2 = 2$, 10-level quantization, reference voltage $V_{ref} = 1$, and a full scale sinusoidal input signal, are shown in Fig. 3.4. The result is close to a Gaussian distribution. Therefore, we assume V_S is Gaussian distributed with a zero mean. The standard deviations σ_{VS} of V_S under different quantizer levels are tabulated in Table 3.1. We observed that when the quantizer level N increases, σ_{VS} decreases. From this table, the relation between standard deviation σ_{VS} and quantizer levels 2^B can be approximated by

$$2^B \cdot \sigma_{VS} \approx 1.4 \cdot |V_{ref}| \qquad (3.11)$$

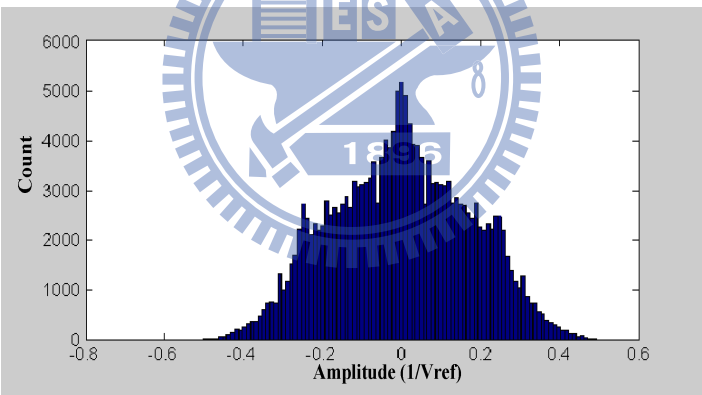


Fig. 3.4. Simulated results of V_S distribution

TABLE 3.1

Standard deviations of V_S (2nd-order) vs. different quantizer bit numbers

Std. deviation (σ_{VS})	Variance	Quantizer level (N)	Bit number (B)
0.711	0.506	2	1
0.455	0.207	3	1.585
0.282	0.080	5	2.322
0.206	0.042	7	2.808
0.155	0.024	9	3.17
0.136	0.018	11	3.46
0.048	0.002	31	4.95

Next, we must determine the P.S.D of V_S. An expression for V_S has been given in (3.3)

$$V_S(z) = X(z)\left[1 - z^{-2}\right] - (1 - z^{-1})^2 E(z)$$

The PSD of V_S of second order $\Sigma\Delta$ modulator which simulates with OSR = 16, SR = $60 V/\mu s$, GBW = 130M, and a 100kHz sinusoidal input signal is plotted in Fig. 3.5. In order to calculate the PSD of V_S, we separately discuss the part of $E(z)$ and $X(z)$. We firstly ignore $X(z)$ in (3.3) and express V_S as

$$V_S(z) = (1 - z^{-1})^2 E(z) \tag{3.12}$$

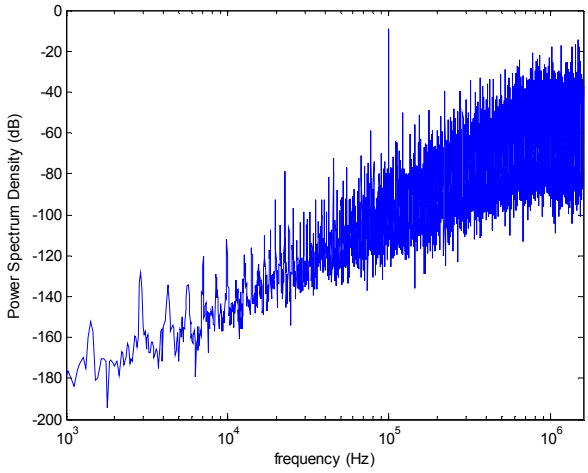


Fig. 3.5. PSD of V_S

Then the magnitude of $E(z)$ must be determine. The range of quantization error is limited in $\pm V_{LSB}/2$, and we assume the probability density function of quantization error is uniformly distributed between $\pm V_{LSB}/2$ and its mean is zero. From this assumption, the total quantization noise power can be calculated as

$$e_q^2 = \frac{V_{LSB}^2}{12} \tag{3.13}$$

$$V_{LSB} = \frac{FS}{2^B} \tag{3.14}$$

FS=Full scale = $V_{ref+} - V_{ref-}$ B：Quantization bit number

Since all the noise power of quantization error is folded into the frequency band $-f_s/2 \sim f_s/2$ and power spectral density is white, we can easily get the height of power spectral density of quantization noise.

$$h_e = \frac{V_{LSB}}{\sqrt{12 f_s}} \tag{3.15}$$

Then we substitute z with $e^{j2\pi f/f_s}$ in (3.12) and magnitude of V_S can be defined as

$$|V_s(f)| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \cdot \frac{FS}{2^B \sqrt{12 f_s}} \tag{3.16}$$

So the relationship between the magnitude of V_S and the bits number translates to a gain. Fig. 3.6 shows that the shape of V_S is not related to bits which can only affect the level of quantization noise floor.

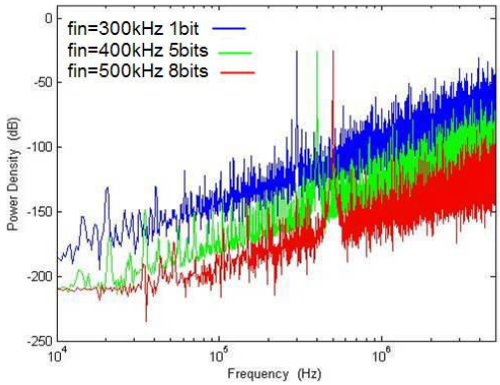


Fig. 3.6. Simulated results of V_S with A_{VS} = 0.5, OSR = 16, and different Bits

Then we consider the part of $X(z)$ and ignore the $E(z)$ in (3.3) to express V_S as

$$V_S(z) = (1 - z^{-2})X(z) \tag{3.17}$$

Take the inverse z-transform to （3.17）

$$V_S(t) = x(t) - x(t-2T)u(t-2T)$$

$$= A_{in}\sin(\omega t) - A_{in}\sin(\omega(t-2T))\cdot u(t-2T) \tag{3.18}$$

Then, the amplitude of V_S can be obtained as

$$A_{VS} = V_S(2T) = x(2T) = A_{in}\sin(\omega \cdot 2T) \cong 2A_{in}\cdot\omega\cdot T \tag{3.19}$$

Note that A_{VS} is not related to quantizer bit number B. The result has been verified by behavior simulation under different B values, as shown in Fig. 3.6.

The analytic procedure of first, and high order single-loop modulators will be similar to above discussion. We just show the results of it in Table 3.2. , Table 3.2. :

TABLE 3.2
Standard deviations of V_S (1st-order) vs. different quantizer bit numbers

Std. deviation (σ_{VS})	Variance	Quantizer level (N)	Bit number (B)
0.331	0.110	2	1
0.254	0.065	3	1.585
0.176	0.031	5	2.322
0.129	0.017	7	2.808
0.091	0.008	9	3.17
0.066	0.004	11	3.46
0.026	0.0006	31	4.95

TABLE 3.3

Standard deviations of V_S (3rd-order) vs. different quantizer bit numbers

Std. deviation (σ_{VS})	Variance	Quantizer level (N)	Bit number (B)
1.305	1.703	2	1
0.864	0.746	3	1.585
0.520	0.270	5	2.322
0.369	0.136	7	2.808
0.287	0.082	9	3.17
0.235	0.055	11	3.46
0.085	0.007	31	4.95

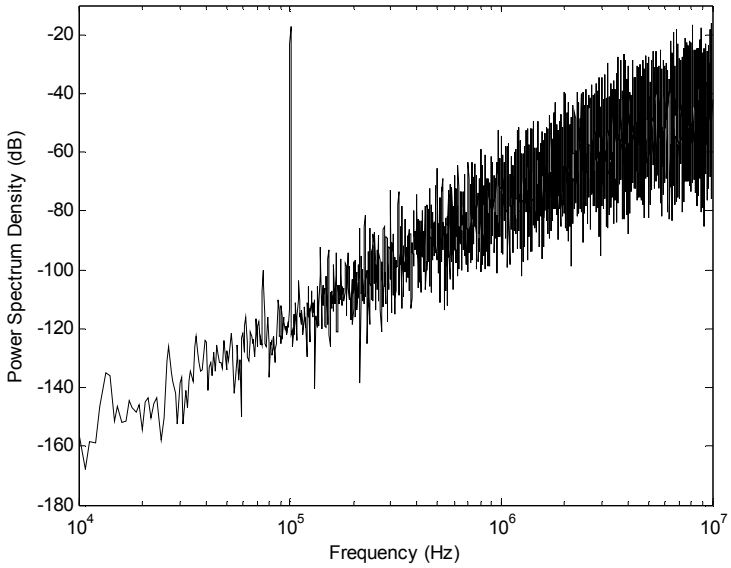
From these tables, the relation between standard deviation σ_{VS} and quantizer levels 2^B can be approximated by

$$2^B \cdot \sigma_{vs} \approx 0.8 \cdot |V_{ref}| \quad \text{(1st-order)} \qquad (3.20)$$

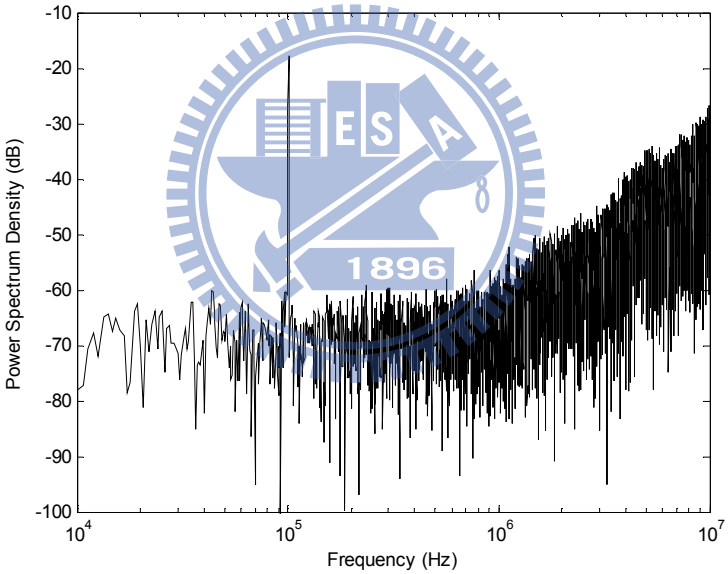
$$2^B \cdot \sigma_{vs} \approx 2.6 \cdot |V_{ref}| \quad \text{(3rd-order)} \qquad (3.21)$$

4.
Derivation of Sigma-Delta Modulator Settling Noise Power Model

The purpose of this section is to derive the analytical ΣΔ modulator output models of settling noises and express in noise power form. This derivation is divided into sampling phase and integration phase. Most of the complexity appears in integration phase. Non-idealities in OTA can cause nonlinear transfer characteristics, which can increase the noise power within base band. These nonlinearities are approximated by a nonlinear fitting which takes into account the time-domain distribution of SC integrator input V_S described in (3.11). Then circular convolution is employed to synthesize the PSD of settling noises at ΣΔ modulator output, using the height of PSD of noise part of V_S given in (3.16). Our results will quantitatively explain how these OTA transfer nonlinearities can reflect high-frequency noises into base band, this phenomenon is demonstrated in Fig. 4.1, Fig. 4.1(a) show the output PSD of an ideal ΣΔ modulator without nonlinear settling problem. When *SR* and *GBW* of OTA are not large enough, nonlinear effects will become obvious and it can reflect high-frequency noises into base band, resulting in a large and flat noise floor in base band as is shown in Fig. 4.1(b). Due to the derivations of first and high order ΣΔ modulator will be similar as second order, we abbreviate it and discuss valuable insights of first and high order finally in comparison with second order.



(a) SR=100 *V/us,* GBW=100 *MHz*



(b) SR=30 *V/us,* GBW=55 *MHz*

Fig. 4.1 Settling noise of integration phase under different *SR* and *GBW* values

4.1 Settling Errors of Sampling Phase

From (3.5) and (3.16), we can obtain the sampling-phase settling noise power at $\Sigma\Delta$ modulator output by integrating the PSD of sampling-phase settling noise, i.e. $\varepsilon_1^2(f)$, over the base band:

$$P_{\varepsilon_1} = \int_{-f_B}^{f_B} S_e^{\,2}(f)\left|N_{TF}(f)\right|^2 df$$
$$= \int_{-f_B}^{f_B} \frac{V_{LSB}^{\,2}}{12 f_s}\left[4\sin^2\left(\frac{\pi f}{f_s}\right)\times \exp\left(-\frac{T_s}{2\tau_1}\right)\right]^2 df \qquad (4.1)$$

4.2 Settling Errors of Integration Phase

As was mentioned above chapter, there are three settling conditions depending on the absolute value of V_S. The full slewing case is not considered here because it is not significant. Note that V_S at end of each integration interval can be written as

$$V_S(T) = \begin{cases} a_1 V_S(1-\beta) \;; & |V_S| \le V_L \\ a_1 V_S\left(1-\frac{V_L}{|V_S|}\beta e^{-1} e^{|V_S|/V_L}\right) \;; & |V_S| > V_L \end{cases} \qquad (4.2)$$

where $\beta = \exp(-T_s/2\tau_2)$ and $V_L = SR\tau_2/a_1$

From（4.2）,the settling error of integration phase can be calculated as following expression, and we draw it in Fig. 4.2:

$$\varepsilon_2(V_S) = \begin{cases} a_1 V_S \beta \;; & |V_S| \le V_L \\ a_1 \,\mathrm{sgn}(V_S) V_L \beta e^{-1} e^{|V_S|/V_L} \;; & |V_S| > V_L \end{cases} \qquad (4.3)$$

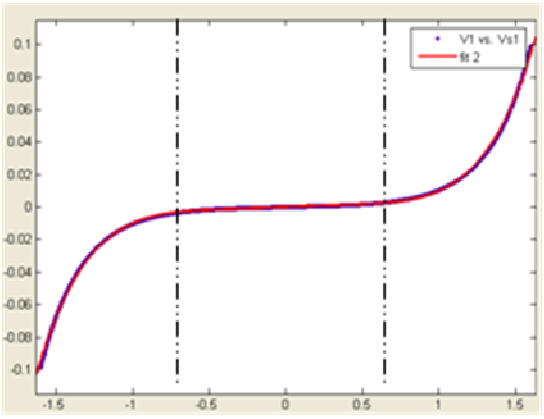


Fig. 4.2 nonlinear transfer function of (4.3)

To approximate (4.3), we apply least square method and neglect the even terms by

reasons of symmetry of Fig. 4.2. Then (4.3) can be approximated by

$$p_i(V_S) = a_1(\boldsymbol{\alpha}_1 V_S + \boldsymbol{\alpha}_3 {V_S}^3 + \boldsymbol{\alpha}_5 {V_S}^5) \tag{4.4}$$

The $p_i(V_S)$ should be fitted through all the points in 0~V_H, where V_H is defined as the maximum value of V_S, so that the sum of the squares of the distances of those points from the $p_i(V_S)$ is minimum. The sum of the squares is

$$q = \int_0^{V_H} [\varepsilon_2(V_S) - p(V_S)]^2 dV_S$$

$$= \int_0^{V_H} [\varepsilon_2(V_S) - a_1\alpha_1 V_S - a_1\alpha_3 {V_S}^3 - a_1\alpha_5 {V_S}^5]^2 dV_S \tag{4.5}$$

With the method above, the coefficients in (4.5) for q to be minimum can be the solution of follow equations.

$$\begin{cases} \frac{\partial}{\partial \alpha_1}[\int_0^{V_H} [\varepsilon_2(V_S) - p(V_S)]^2 dV_S] = 0 \\ \frac{\partial}{\partial \alpha_3}[\int_0^{V_H} [\varepsilon_2(V_S) - p(V_S)]^2 dV_S] = 0 \\ \frac{\partial}{\partial \alpha_5}[\int_0^{V_H} [\varepsilon_2(V_S) - p(V_S)]^2 dV_S] = 0 \end{cases} \tag{4.6}$$

Note that the distribution of V_S in (4.6) is assumed to be uniform over 0~V_H. This may lead to a bad estimation of settling noise, especially in the case of small V_L. As mentioned before chapter, the distribution of V_S have been defined as Gaussian distribution with standard deviation $\boldsymbol{\sigma}_{V_S} \approx 1.4 \cdot |V_{ref}| / 2^B$ (second-order). There, the probability density function (PDF) of V_S is

$$f(V_s) = \frac{1}{\sqrt{2\pi}\boldsymbol{\sigma}_{V_S}} \exp(-\frac{{V_S}^2}{2{\boldsymbol{\sigma}_{V_S}}^2}) \tag{4.7}$$

Nevertheless, since the integral interval is 0~V_H, the PDF of V_S should be modified as

$$f(V_s)=\frac{1}{\int_0^{V_H}\frac{1}{\sqrt{2\pi}\sigma_{V_S}}\exp(-\frac{{V_S}^2}{2{\sigma_{V_S}}^2})dV_S}\frac{1}{\sqrt{2\pi}\sigma_{V_S}}\exp(-\frac{{V_S}^2}{2{\sigma_{V_S}}^2}) \tag{4.8}$$

Then (4.8) is normalized and weighting function can be expressed as

$$W(V_S)=\frac{V_H}{\int_0^{V_H}\frac{1}{\sqrt{2\pi}\sigma_{V_S}}\exp(-\frac{{V_S}^2}{2{\sigma_{V_S}}^2})dV_S}\frac{1}{\sqrt{2\pi}\sigma_{V_S}}\exp(-\frac{{V_S}^2}{2{\sigma_{V_S}}^2}) \tag{4.9}$$

Taking into account the PDF of V_S in any specific interval, then (4.6) is revised as:

$$\begin{cases}\frac{\partial}{\partial\alpha_1}[\int_0^{V_H}[\varepsilon_2(V_S)-p(V_S)]^2\cdot W(V_S)dV_S]=0\\ \frac{\partial}{\partial\alpha_3}[\int_0^{V_H}[\varepsilon_2(V_S)-p(V_S)]^2\cdot W(V_S)dV_S]=0\\ \frac{\partial}{\partial\alpha_5}[\int_0^{V_H}[\varepsilon_2(V_S)-p(V_S)]^2\cdot W(V_S)dV_S]=0\end{cases} \tag{4.10}$$

$$\Rightarrow\begin{cases}\frac{\partial}{\partial\alpha_1}\left[\int_0^{V_H}\left[\varepsilon_2(V_S)-a_1\alpha_1V_S-a_1\alpha_3{V_S}^3-a_1\alpha_5{V_S}^5\right]\times W(V_S)dV_S\right]=0\\ \frac{\partial}{\partial\alpha_3}\left[\int_0^{V_H}\left[\varepsilon_2(V_S)-a_1\alpha_1V_S-a_1\alpha_3{V_S}^3-a_1\alpha_5{V_S}^5\right]\times W(V_S)dV_S\right]=0\\ \frac{\partial}{\partial\alpha_5}\left[\int_0^{V_H}\left[\varepsilon_2(V_S)-a_1\alpha_1V_S-a_1\alpha_3{V_S}^3-a_1\alpha_5{V_S}^5\right]\times W(V_S)dV_S\right]=0\end{cases}$$

$$\Rightarrow\begin{cases}\int_0^{V_H}\left[\varepsilon_2(V_S)-a_1\alpha_1V_S-a_1\alpha_3{V_S}^3-a_1\alpha_5{V_S}^5\right]\times(-2a_1V_SW(V_S))dV_S=0\\ \int_0^{V_H}\left[\varepsilon_2(V_S)-a_1\alpha_1V_S-a_1\alpha_3{V_S}^3-a_1\alpha_5{V_S}^5\right]\times(-2a_1{V_S}^3W(V_S))dV_S=0\\ \int_0^{V_H}\left[\varepsilon_2(V_S)-a_1\alpha_1V_S-a_1\alpha_3{V_S}^3-a_1\alpha_5{V_S}^5\right]\times(-2a_1{V_S}^5W(V_S))dV_S=0\end{cases}$$

$$\Rightarrow \begin{cases} \int_0^{V_H} \left[a_1\alpha_1 V_S + a_1\alpha_3 {V_S}^3 + a_1\alpha_5 {V_S}^5\right] \times (V_S W(V_S))dV_S = \int_0^{V_H} \varepsilon_2 V_S W(V_S)dV_S \\ \int_0^{V_H} \left[a_1\alpha_1 V_S + a_1\alpha_3 {V_S}^3 + a_1\alpha_5 {V_S}^5\right] \times ({V_S}^3 W(V_S))dV_S = \int_0^{V_H} \varepsilon_2 {V_S}^3 W(V_S)dV_S \\ \int_0^{V_H} \left[a_1\alpha_1 V_S + a_1\alpha_3 {V_S}^3 + a_1\alpha_5 {V_S}^5\right] \times ({V_S}^5 W(V_S))dV_S = \int_0^{V_H} \varepsilon_2 {V_S}^5 W(V_S)dV_S \end{cases}$$

$$\Rightarrow \begin{cases} \int_0^{V_H} \left[\alpha_1 {V_S}^2 + \alpha_3 {V_S}^4 + \alpha_5 {V_S}^6\right] \times W(V_S)dV_S \\ \qquad = \int_0^{V_L} \beta {V_S}^2 W(V_S)dV_S + \int_{V_L}^{V_H} V_L \beta e^{-1} e^{|V_S|/V_L} V_S W(V_S)dV_S \\ \int_0^{V_H} \left[\alpha_1 {V_S}^4 + \alpha_3 {V_S}^6 + \alpha_5 {V_S}^8\right] \times W(V_S)dV_S \\ \qquad = \int_0^{V_L} \beta {V_S}^4 W(V_S)dV_S + \int_{V_L}^{V_H} V_L \beta e^{-1} e^{|V_S|/V_L} {V_S}^3 W(V_S)dV_S \\ \int_0^{V_H} \left[\alpha_1 {V_S}^6 + \alpha_3 {V_S}^8 + \alpha_5 {V_S}^{10}\right] \times W(V_S)dV_S \\ \qquad = \int_0^{V_L} \beta {V_S}^6 W(V_S)dV_S + \int_{V_L}^{V_H} V_L \beta e^{-1} e^{|V_S|/V_L} {V_S}^5 W(V_S)dV_S \end{cases}$$

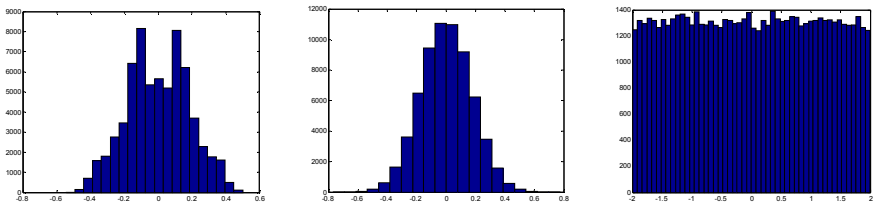
Then the values of the coefficients computed to be:

$$\begin{bmatrix} \alpha_1 \\ \alpha_3 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} \int_0^{V_H} W(V_S){V_S}^2 & \int_0^{V_H} W(V_S){V_S}^4 & \int_0^{V_H} W(V_S){V_S}^6 \\ \int_0^{V_H} W(V_S){V_S}^4 & \int_0^{V_H} W(V_S){V_S}^6 & \int_0^{V_H} W(V_S){V_S}^8 \\ \int_0^{V_H} W(V_S){V_S}^6 & \int_0^{V_H} W(V_S){V_S}^8 & \int_0^{V_H} W(V_S){V_S}^{10} \end{bmatrix}^{-1} \times$$

$$\begin{bmatrix} \int_0^{V_L} W(V_S)\beta {V_S}^2 dV_S + \int_{V_L}^{V_H} W(V_S)V_L \beta e^{-1} e^{|V_S|/V_L} V_S dV_S \\ \int_0^{V_L} W(V_S)\beta {V_S}^4 dV_S + \int_{V_L}^{V_H} W(V_S)V_L \beta e^{-1} e^{|V_S|/V_L} {V_S}^3 dV_S \\ \int_0^{V_L} W(V_S)\beta {V_S}^6 dV_S + \int_{V_L}^{V_H} W(V_S)V_L \beta e^{-1} e^{|V_S|/V_L} {V_S}^5 dV_S \end{bmatrix} \qquad (4.11)$$

In order to validate (4.11), we apply least square to the V_S in three cases. In case one, behavior simulation was carried. In case two, equation (4.11) is used. In case three, the weighting function $W(V_S)$ is not considered. The parameters used in case one are B = 3-bits, OSR = 120, $SR = 40 V/\mu s$, and GBW = 100MHz. Fig 4.3 and Table 4.1.

show the V_S and coefficients obtained in three cases. The case applying Gaussian distribution shows a good fit when compared to the one by simulation. In Fig 4.4, the fitting results in three cases are illustrated, and the case with Gaussian distribution is closer to the simulated one than another case. Note that the V_L in this case is 0.1681 and the probability of nonlinear operation is respectively 0.35, 0.34, and 0.9 in three cases. This result shows that applying Gaussian distribution to V_S plays a crucial role in calculating settling noise.



(a) Behavioral model (b) With Gaussian distribution (c) No Gaussian distribution

Fig. 4.3. Distribution of V_S obtained in three different cases

TABLE 4.1

Coefficients obtained in three different cases

	Behavioral model	With Gaussian distribution	No Gaussian distribution
α_1	0.958	0.94	835.67
α_3	1.239	1.609	-1532.7
α_5	19.677	16.357	567.25

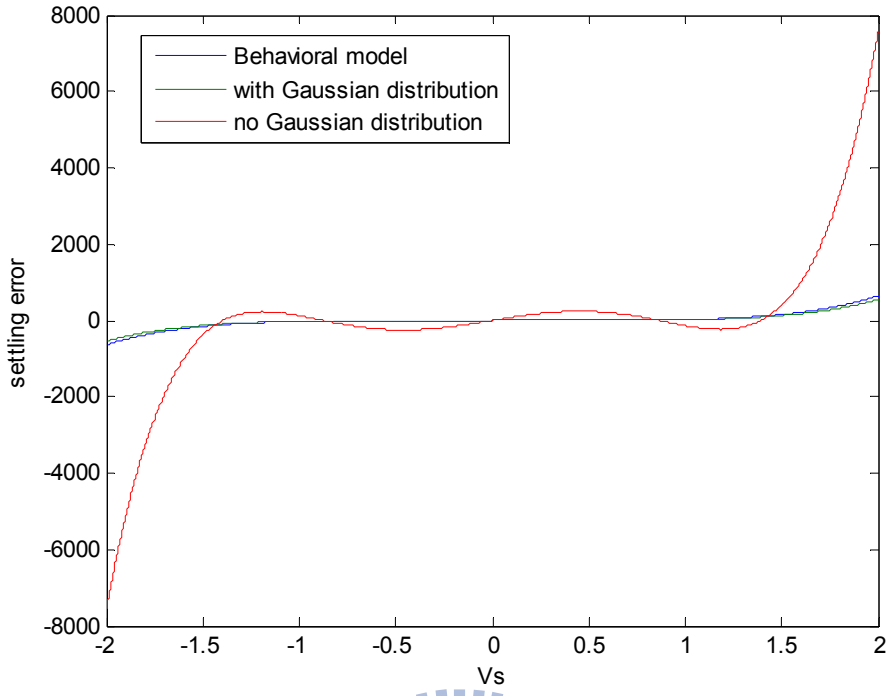


Fig. 4.4. Settling error versus V_S in three different cases

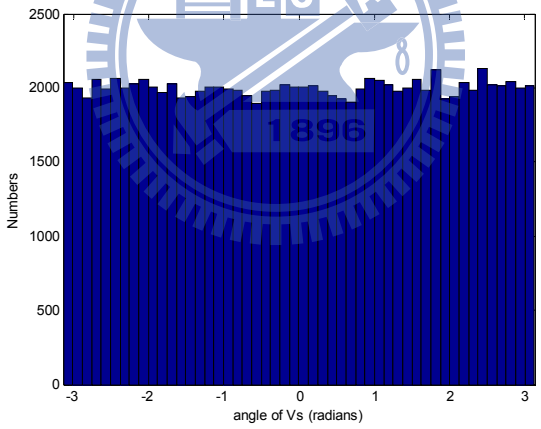


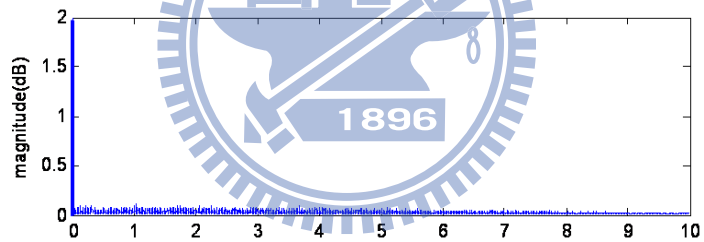
Fig. 4.5. The distribution of angle of V_S

With coefficients α_1, α_3 and α_5 in (4.4), the next step for calculating settling noise power is to determinate the PSD of $V_S{}^3$ by using the PSD of V_S. From (3.16), the height of the power spectral density of V_S can be expressed as

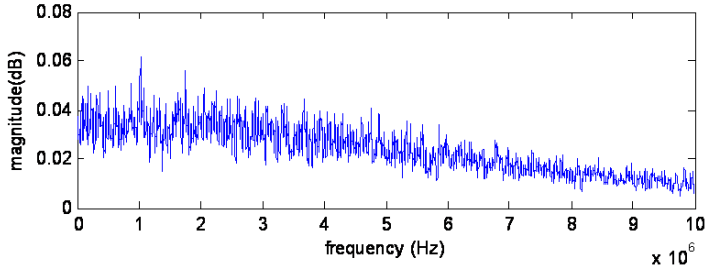
$$h_e(f) = \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin\left(\frac{\pi f}{f_s}\right) \right]^2 \times e^{i\theta(f)} \tag{4.12}$$

where θ represents the angle of h_e at a particular frequency f. In previous chapter, the angle of PSD of V_S is not considered. However, the angle of PSD of V_S should be included in the computation of the PSD of ${V_S}^3$ and ${V_S}^5$ so that correct results can be obtained. In Fig. 4.5, simulation result shows that the angle of V_S is close to a uniform distribution. Therefore, θ is considerably assumed to be an arbitrary value in $0 \sim 2\pi$. To find out the PSD of ${V_S}^3$, we firstly try to generate the PSD of square of V_S as shown in Fig. 4.6. The discussion is divided into when $f = 0$ and when $f \neq 0$. When $f = 0$, $h_{e2}(0)$ means sum of square of V_S in time domain. From Parseval's theorem, we get

$$h_{e2}(0) = \sum {V_S}^2[n] = \frac{1}{f_s}\int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \left\{ \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi f}{f_s}) \right]^{-2} \right\}^2 df \tag{4.13}$$



(a) Included f = 0



(b) Not included f = 0

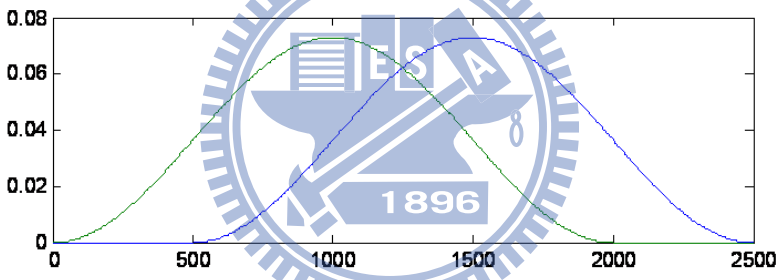
Fig. 4.6 Height of PSD of square of V_S

When $f \neq 0$, by applying circular convolution, we can express the height of PSD of square of V_S as

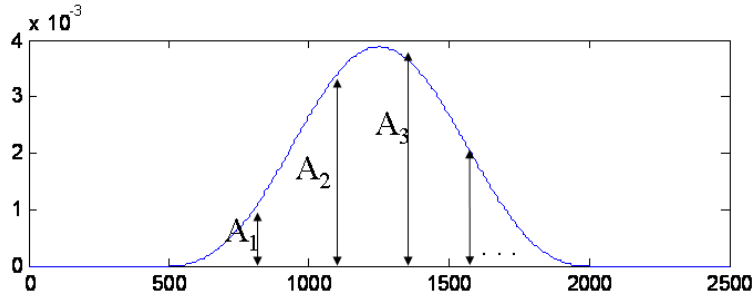
$$h_{e2}(f) = h_e(f) \otimes h_e(f)$$
$$= \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi\theta}{f_s}) \right]^2 \times e^{i\theta(f)} \otimes \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi\theta}{f_s}) \right]^2 \times e^{i\theta(f)}$$
$$= \frac{1}{f_s} \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi f_1}{f_s}) \right]^2 \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi(f - f_1)}{f_s}) \right]^2 \times e^{i\theta(f_1)} \times e^{i\theta(f - f_1)} df_1$$

(4.14)

Then it become clear that we cannot correctly compute the magnitude of h_{e2} without taking into account the angle of h_e. To demonstrate this idea, the integration of the convolution can be emulated as summing together arbitrarily large number of complex numbers $A_1, A_2, A_3 \ldots$ as is illustrated in Fig. 4.7.



(a) A result of convolution



(b) Sum of overlap part of (a)

Fig. 4.7 Integration of the convolution

Since all of these complex numbers have different angles, we cannot simply add together their magnitudes, which would be the case if the angle of h_e is not included

in the convolution. Fortunately, because θ is arbitrary, the angles of A_1, A_2, A_3… are also arbitrary. Therefore, the magnitude of sum of A_1, A_2, A_3… can be expressed as

$$\left|A_1 e^{i\alpha} + A_2 e^{i\beta} + A_3 e^{i\gamma} + \ldots\right|$$

$$= \left| A_1(\cos(\alpha) + i\sin(\alpha)) + A_2(\cos(\beta) + i\sin(\beta)) + A_3(\cos(\gamma) + i\sin(\gamma)) + \ldots \right|$$

$$= \left[A_1^{\,2} + A_2^{\,2} + A_3^{\,2} + \ldots + A_1 A_2 \cos(\alpha - \beta) + A_2 A_3 \cos(\beta - \gamma) + A_1 A_3 \cos(\gamma - \alpha) + \ldots\right]^{0.5} \quad (4.15)$$

Because α, β, and γ are arbitrary between 0~2π, the mean of cosine function is zero and then the expected value of (4.15) results as

$$\sqrt{A_1^{\,2} + A_2^{\,2} + A_3^{\,2} + \ldots} \quad (4.16)$$

Then the expected value of the height of spectral density of square of V_S can be defined as

$$E\{h_{e2}(f)\} = \frac{1}{f_S}\frac{4V_{LSB}^2}{3f_S}\left[\int_{-\frac{f_S}{2}}^{\frac{f_S}{2}} \sin^4\left(\frac{\pi f_1}{f_S}\right)\sin^4\left(\frac{\pi(f - f_1)}{f_S}\right)df_1\right]^{0.5} \quad (4.17)$$

Fig 4.8 compares the expected value of (4.17) and behavior model simulation with f_S = 20MHz, Bit = 1.

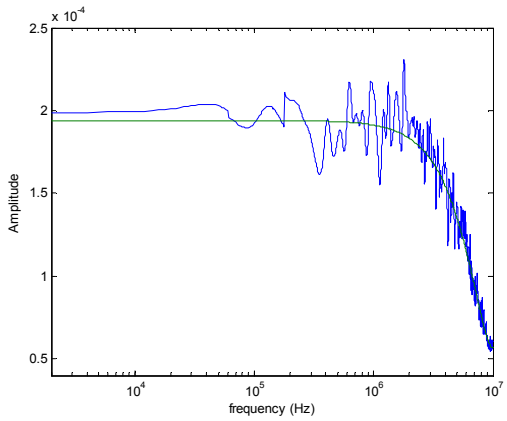


Fig. 4.8 Comparison of the expected value of (4.17) with the behavior simulation result

Then we can follow the above technique to obtain expected value of $V_S{}^3$ and $V_S{}^5$

$$h_{e3}(f) = h_e(f) \otimes h_{e2}(f)$$
$$h_{e5}(f) = h_{e2}(f) \otimes h_{e3}(f)$$

$$E\{h_{e3}(f)\} \cong \frac{1}{2^{3B}} \left\{ \begin{array}{l} 2.49\sqrt{f_S}\sin^2(\frac{\pi f}{f_S}) + \\ \frac{0.182}{f_S}\sqrt{\left[173 - 136\cos^2(\frac{\pi f}{f_S}) + 8\cos^4(\frac{\pi f}{f_S})\right]} \end{array} \right\}$$

$$E\{h_{e5}(f)\} \cong \frac{0.0396 f_S}{2^{5B}} \left[\begin{array}{l} 9.2 + 16.97\cos^2(\frac{\pi f}{f_S})\sin^2(\frac{\pi f}{f_S}) \\ +18.11\cos^2(\frac{\pi f}{f_S}) + 55.6\sin^2(\frac{\pi f}{f_S}) \\ +3.23\cos^4(\frac{\pi f}{f_S}) + 15.8\sin^4(\frac{\pi f}{f_S}) \end{array} \right]^{0.5} \quad (4.18)$$

Fig. 4.9 and Fig. 4.10 respectively compare the expected values of $V_S{}^3$ and $V_S{}^5$ with corresponding simulation results. Then the expected value of the height of spectral density of settling noise of integration phase can be defined as

$$E\{h(f)\} = \alpha_1 E\{h_{e1}(f)\} + \alpha_3 E\{h_{e3}(f)\} + \alpha_5 E\{h_{e5}(f)\} \quad (4.19)$$

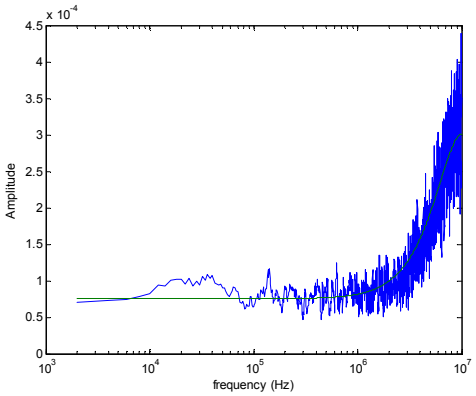


Fig. 4.9 Comparison of the expected value of $V_S{}^3$ with the behavior simulation result

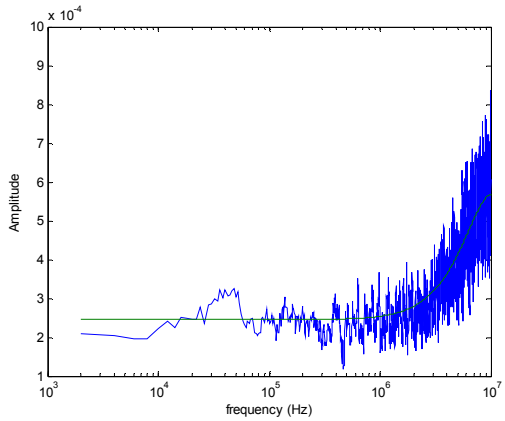


Fig. 4.10 Comparison of the expected value of $V_S{}^5$ with the behavior simulation result

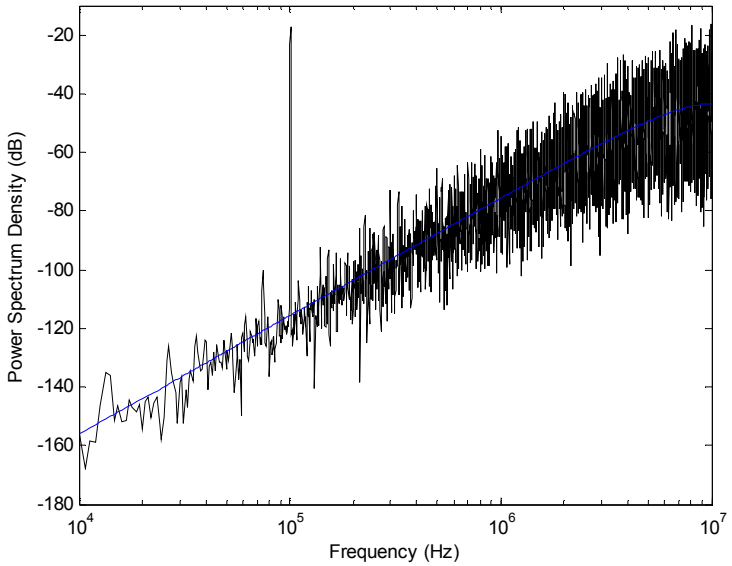
So the settling noise in base band $\pm f_B$ of integration phase can be obtained by integrating (4.19) as

$$P_{\varepsilon 2} = \int_{-f_B}^{f_B} (\alpha_1 E\{h_{e1}(f)\} + \alpha_3 E\{h_{e3}(f)\} + \alpha_5 E\{h_{e5}(f)\})^2 df \quad (4.20)$$

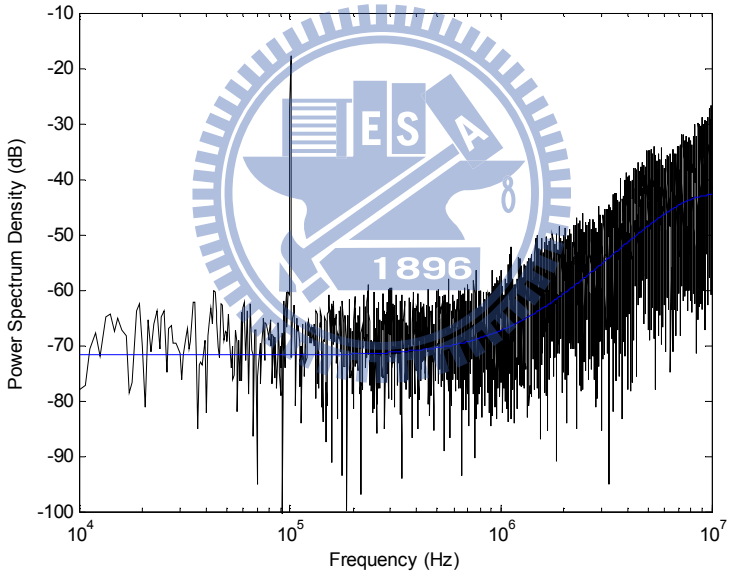
Then the total settling noise power can be computed as

$$P_\varepsilon = P_{\varepsilon 1} + P_{\varepsilon 2} \quad (4.21)$$

In order to demonstrate our analytical models, we use our model to predict the system behaviors shown in Fig. 4.1, and the results are provided in Fig. 4.11. These result show our models are very accurate. Notice that α_3 and α_5 are 8.9725×10^{-8} and 5.1274×10^{-7} in Fig. 4.11 (a), and are 0.04887 and 0.06023 in Fig. 4.11 (b). These values mean that too serious nonlinearity may result in larger α_3 and α_5, and we can find out from (4.19) that larger α_3 and α_5 would arise affection of $V_S{}^3$ and $V_S{}^5$, and more high frequency noise will be reflected into base band.



(a) SR=100 *V/us*, GBW=100 *MHz*



(b) SR=30 *V/us*, GBW=55 *MHz*

Fig. 4.11 Settling noise of integration phase under different *SR* and *GBW* values

Note the low frequency regions of $V_S{}^3$ and $V_S{}^5$ in Fig. 4.9 and Fig. 4.10 are absolutely flat, and this means that the in band noise power will increase if the α_3 and α_5 in (4.11) increase. Therefore, the nonlinearity of settling will make an amount increase on noise power. It is worth noting that settling noise is highly dependent on the high frequency noise. Due to the noise shaping nature, the high

frequency amplitude of V_S is great and will lead to large settling noise. In order to provide insight on how settling noise is related to α_3 and α_5, we show behavior simulation with OSR = 100 , f_{in} = 100kHz, GBW = 80MHz, and for several different SR. The result is listed in Table 4.2. It is clear from Table 4.2 that when SR decreases, nonlinear effect would increase, resulting in much larger α_3 and α_5. Accordingly, settling noise increases significantly.

TABLE 4.2

The effect of SR on settling noise

SR $(V/\mu s)$	$\lvert\alpha_3\rvert$	$\lvert\alpha_5\rvert$	***Settling noise (dB)***
40	2.4523×10^{-3}	2.8582×10^{-3}	**-69.967**
60	4.5034×10^{-5}	8.0204×10^{-5}	**-83.272**
80	2.0764×10^{-6}	1.1864×10^{-5}	**-92.784**
100	8.5082×10^{-7}	3.466×10^{-6}	**-100.851**

As we indicated in the above definitions of second order, we could extend such methodology easily for first, high order module. It must further be noted that we pointed out in the previous chapter, the quantizer nonlinearity will result in the presence of idle tones and pattern noise in the modulator output spectrum, these effects will lead to imperfect curve fitting in comparison to modulator output spectrum, especially in first order module. Therefore, a possible solution to this problem is to include, usually at the quantizer input, a non-periodic signal as pseudo-random noise. With this technique, called dithering [11], it is possible to partially decorrelate the quantization error and the input, and yield the good fitting result. Since the fitting procedures are certain similarities between second order and first, high order module, we omit the discussion and show the fitting result of first,

high order modulator output spectrum in Fig. 4.12, Fig. 4.13. Furthermore, we derive the expected value of the height of spectral density of $V_S{}^2$, $V_S{}^3$ and $V_S{}^5$ in (4.22-23).

$$E\{h_{e2}(f)\} = \frac{1}{f_S}\frac{V_{LSB}^2}{3f_S}\left[\int_{-\frac{f_S}{2}}^{\frac{f_S}{2}} \sin^2(\frac{\pi f_1}{f_S})\sin^2(\frac{\pi(f-f_1)}{f_S})df_1\right]^{0.5} \quad \text{(First Order)}$$

$$E\{h_{e3}(f)\} \cong \frac{\sqrt{f_S}}{2^{3B}}\left\{0.415\sin(\frac{\pi f}{f_S}) + \sqrt{0.165 - 0.066\cos^2(\frac{\pi f}{f_S})}\right\} \quad \text{(First Order)}$$

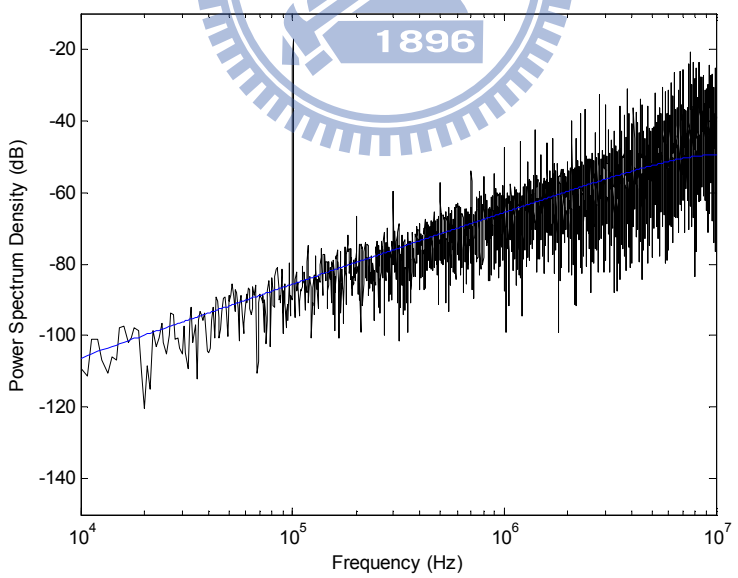
$$E\{h_{e5}(f)\} \cong \frac{0.0396 f_S}{2^{5B}}\left[\begin{array}{l} 1.93 + 2.24\cos(\frac{\pi f}{f_S})\sin(\frac{\pi f}{f_S}) \\ +1.39\cos^2(\frac{\pi f}{f_S}) + 2.46\sin^2(\frac{\pi f}{f_S}) \end{array}\right]^{0.5} \quad \text{(First Order)} \qquad (4.22)$$

$$E\{h_{e2}(f)\} = \frac{1}{f_S}\frac{16V_{LSB}^2}{3f_S}\left[\int_{-\frac{f_S}{2}}^{\frac{f_S}{2}} \sin^6(\frac{\pi f_1}{f_S})\sin^6(\frac{\pi(f-f_1)}{f_S})df_1\right]^{0.5} \quad \text{(Third Order)}$$

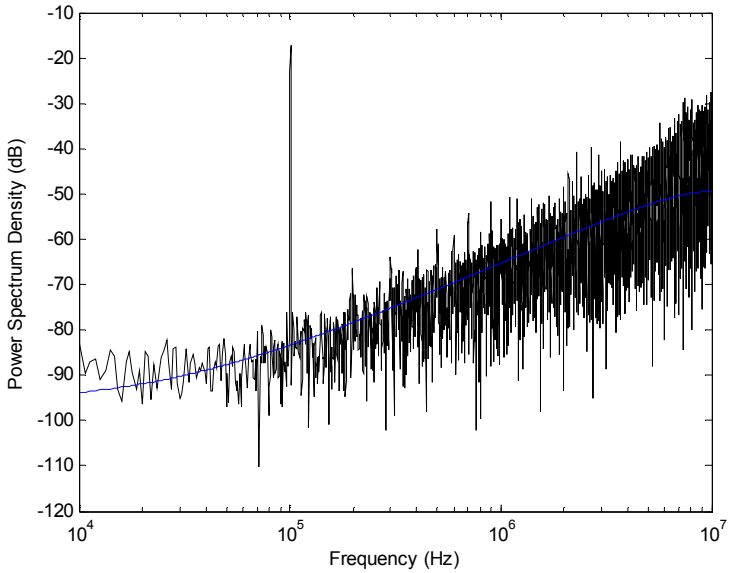
$$E\{h_{e3}(f)\} \cong \frac{\sqrt{f_S}}{2^{3B}}\left\{\begin{array}{l} 16.592\sin^3(\frac{\pi f}{f_S}) + \\ \sqrt{\begin{array}{l} 253.474 - 283.656\cos^2(\frac{\pi f}{f_S}) \\ +59.295\cos^4(\frac{\pi f}{f_S}) - 1.068\cos^6(\frac{\pi f}{f_S}) \end{array}} \end{array}\right\} \quad \text{(Third Order)}$$

$$E\{h_{e5}(f)\} \cong \frac{0.0396 f_S}{2^{5B}} \left[\begin{array}{l} 19300 + 33800\cos^4(\frac{\pi f}{f_S})\sin^2(\frac{\pi f}{f_S}) \\ + 64000\cos^2(\frac{\pi f}{f_S})\sin^4(\frac{\pi f}{f_S}) + 296000\cos^2(\frac{\pi f}{f_S})\sin^2(\frac{\pi f}{f_S}) \\ + 51600\cos^4(\frac{\pi f}{f_S}) + 266000\sin^2(\frac{\pi f}{f_S}) \\ + 76300\cos^2(\frac{\pi f}{f_S}) + 37100\sin^6(\frac{\pi f}{f_S}) \\ + 4740\cos^6(\frac{\pi f}{f_S}) + 309000\sin^4(\frac{\pi f}{f_S}) \\ + 117000\cos^3(\frac{\pi f}{f_S})\sin(\frac{\pi f}{f_S}) + 45900\cos^3(\frac{\pi f}{f_S})\sin^3(\frac{\pi f}{f_S}) \\ + 55000\cos(\frac{\pi f}{f_S})\sin^5(\frac{\pi f}{f_S}) + 9450\cos^5(\frac{\pi f}{f_S})\sin(\frac{\pi f}{f_S}) \\ + 341000\cos(\frac{\pi f}{f_S})\sin^3(\frac{\pi f}{f_S}) + 172000\cos(\frac{\pi f}{f_S})\sin(\frac{\pi f}{f_S}) \end{array} \right]^{0.5}$$

(Third Order) (4.23)

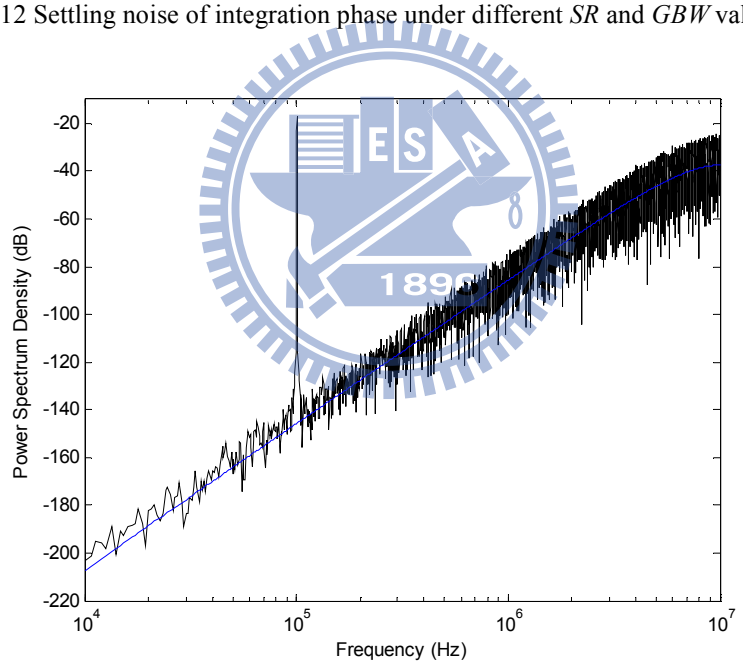


(a) SR=200 *V/us*, GBW=200 *MHz*

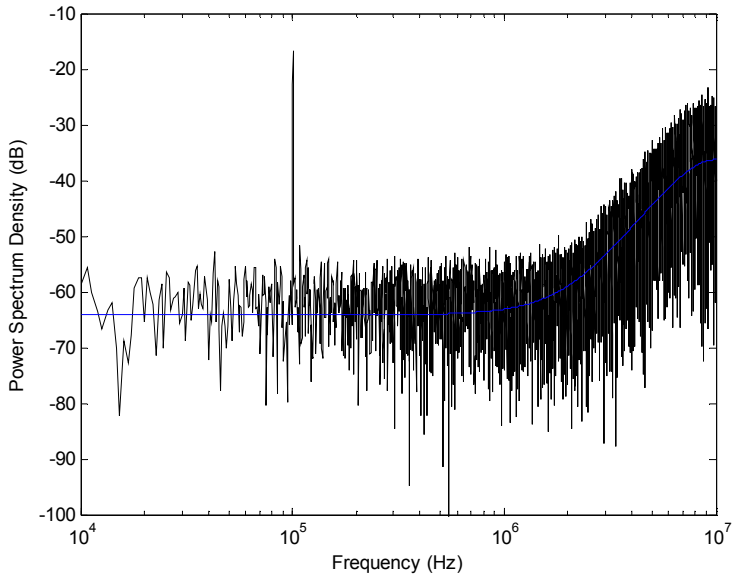


(b) SR=60 *V/us*, GBW=70 *MHz*

Fig. 4.12 Settling noise of integration phase under different *SR* and *GBW* values (first-order)



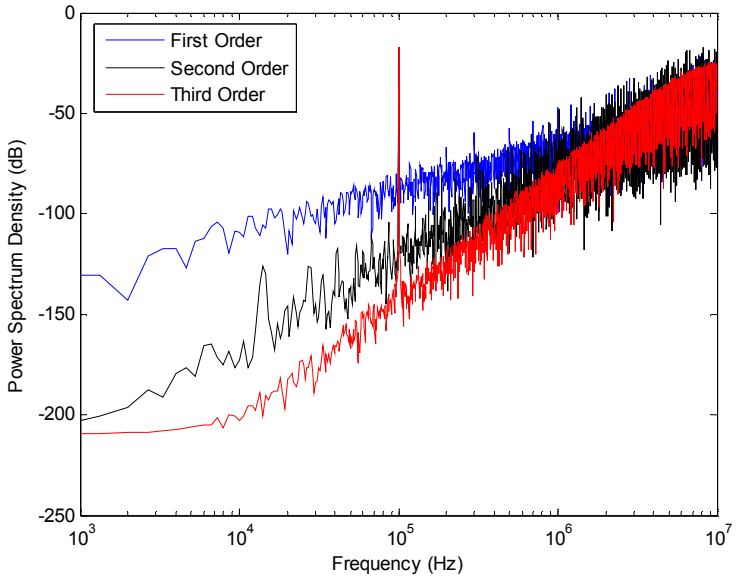
(a) SR=200 *V/us*, GBW=200 *MHz*



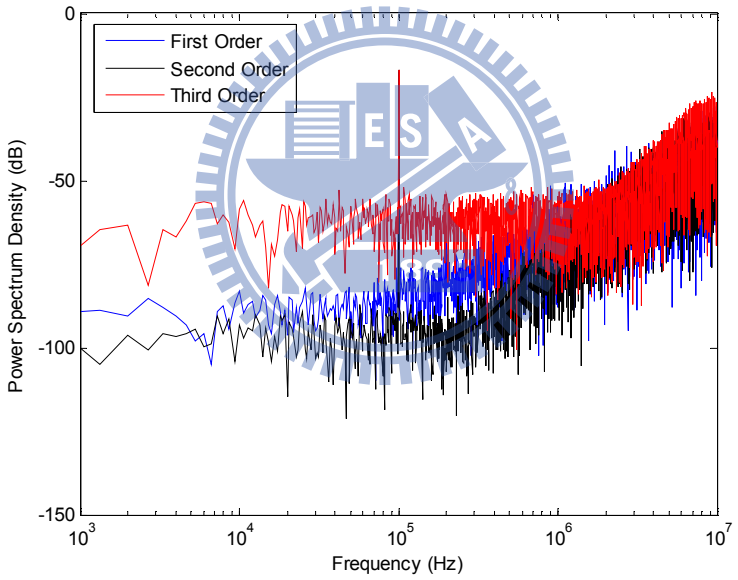
(b) SR=60 *V/us,* GBW=70 *MHz*

Fig. 4.13 Settling noise of integration phase under different *SR* and *GBW* values (third-order)

In general, the higher-order ΣΔ modulator are found to offer improved performance, but when SR and GBW of OTA are not large enough, the performance of the higher-order ΣΔ modulator may be worse than the lower-order ΣΔ modulator. Our model is used to show this phenomenon in Fig. 4.14. Typical ideal output PSD for three modulators are shown in Fig. 4.14 (a), we can find out that second, third-order PSD higher at high frequency and lower at low frequency than first-order PSD. However, when SR and GBW of OTA decrease, nonlinear effect becomes significant. Since second, third-order ΣΔ modulator have much larger noise power at high frequency, a large quantity of high frequency noise would be reflected into base-band, resulting in approximate settling noise power in the base-band for second-order ΣΔ modulator , and even excess settling noise power for third-order one. Fig. 4.14 (b) illustrating a typical such situation.



(a) SR=200 *V/us,* GBW=200 *MHz*



(b) SR=60 *V/us,* GBW=70 *MHz*

Fig. 4.14 Comparison of settling noise of first, second and third order ΣΔ modulators

It is worth noting that the previous literatures have been discussed as OSR increases, the settling noise power will rise dramatically and degrade the performance of ΣΔ modulator. Therefore, first order module might be a more efficient architecture than second and high order module. Our model can be applied to compute the minimum *SR* and *GBW* required so that the second or high order settling noise

power would not exceed the first order quantization noise power P_Q. That is, only when *SR* and *GBW* are larger than the required minimum values, then it is justified to employ second or high order modulator in stead of first order one. The results are summarized in Table 4.3. Table 4.3 indicates that as OSR increases, the bigger SR and GBW of second or high order modulator are needed to cope with the settling noise power.

TABLE 4.3

MINIMUM SR AND GBW REQUIRED W. R. T. OSR

OSR	$\mathbf{P_Q}$ of Fist Order ΣΔ modulator (dB)	Second Order ***SR*** ($V/\mu s$)	Second Order ***GBW*** **(MHz)**	Third Order ***SR*** ($V/\mu s$)	Third Order ***GBW*** **(MHz)**
16	−41.744	≥ 6	≥ 5	≥ 12	≥ 10
32	−50.775	≥ 12	≥ 12	≥ 24	≥ 30
64	−59.805	≥ 25	≥ 33	≥ 52	≥ 55
80	−62.713	≥ 35	≥ 45	≥ 64	≥ 74
100	−65.620	≥ 46	≥ 53	≥ 85	≥ 100
120	−67.995	≥ 51	≥ 65	≥ 98	≥ 119
160	−71.744	≥ 71	≥ 90	≥ 135	≥ 150

5.

Derivation of Sigma-Delta Modulators Settling Distortion

Settling problem will produce not only the in-band noises but also the distortions in the ΣΔ modulator output spectrum, called settling distortions. These distortions introduced by an SC integrator are mainly due to voltage-dependent behavior of capacitors and switches, and nonlinearities associated to the gain of the amplifier as well as its settling behavior that we have been discussed in chapter 3. In this chapter, we analyze incomplete charge transfer in an SC integrator to obtain analytical models to represent harmonic distortion as function of SR, GBW of OTA. On the other hand, the nonlinearities in the front-end integrator are considered only due to it directly affecting the overall modulator linearity. When referred to the modulator input, nonlinear effects in the remaining integrators will be attenuated by the gain of the integrators.

The effect of the SR and GBW are related to each other, and may be interpreted as a nonlinear gain. Consider the SC integrator operates in the integration phase. As mentioned around (3.6), (3.7) in chapter 3, the evolutions of the output node during the n-th integration period are given by

1. Linear settling: $|V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2$:

$$V_O(t) = V_O(nT-T) + a_1 \cdot V_S \cdot (1 - e^{\frac{-(t-nT+\frac{T}{2})}{\tau_2}}), nT - \frac{T}{2} < t < nT \qquad (5.1)$$

2. Partial slewing: $\frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S|$:

$$V_O(t) = V_O(nT-T) + SR \cdot (t_O - nT + \frac{T}{2}) \cdot \mathrm{sgn}(V_S) +$$

$$\left[a_1 V_S - SR\cdot(t_O - nT + \frac{T}{2})\cdot \mathrm{sgn}(V_S)\right](1-e^{\frac{-(t-(t_O-nT+\frac{T}{2}))}{\tau_2}}), t > t_O \tag{5.2}$$

Where t_O is the time instant when integrator operates in partial slewing case and slope of output becomes less than SR, which result

$$t_O = \frac{a_1|V_S|}{SR} - \tau_2 \tag{5.3}$$

Note that (5.1) and (5.2) at end of each integration interval can be rewritten as

$$\begin{aligned} V_O(nT) &= V_O(nT-T) + a_1 V_S(1-e^{-(\frac{T}{2\tau_2}+1)}\cdot e) \\ &= V_O(nT-T) + a_1 V_S(1-\gamma\cdot e), |V_S| \le V_L \end{aligned} \tag{5.4}$$

$$V_O(nT) = V_O(nT-T) + a_1 V_S\left[1 - \frac{V_L}{|V_S|}\cdot\gamma\cdot e^{\frac{|V_S|}{V_L}}\right], |V_S| > V_L \tag{5.5}$$

Where $\gamma = e^{-(\frac{T}{2\tau_2}+1)}$; $V_L = \dfrac{SR\tau_2}{a_1}$

Let $$g_i(V_S) = \begin{cases} a_1(1-\gamma\cdot e) \ ; & |V_S| \le V_L \\ a_1\left(1 - \dfrac{V_L}{|V_S|}\gamma\cdot e^{|V_S|/V_L}\right) ; & |V_S| > V_L \end{cases} \tag{5.6}$$

Which is the integrator gain, and we show a plot of the expression (5.6) in Fig. 5.1. It is worth noting that distortions are produced at the modulator output when OPAs operate in the partial slewing region, because we can find in that region, the integrator gain is a function of integrator input V_S.

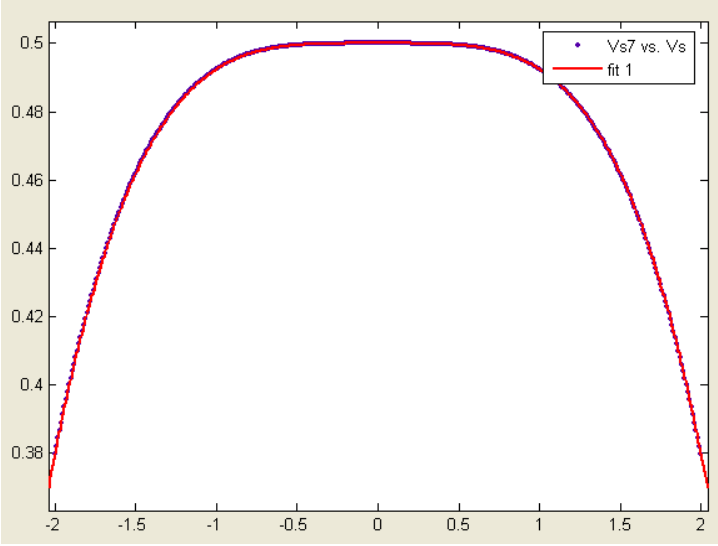


Fig. 5.1 nonlinear transfer function of (5.6)

The curve fitting technique applied in chapter 4 will be used again to acquire analytical model of settling distortion. From (5.4), (5.5) and (5.6), we rewrite the equation of front-end integrator output as

$$V_O(nT)=V_O(nT-T)+g_i(V_S)\cdot V_S \tag{5.7}$$

And (5.7) can be described with the following form

$$V_O(nT)=V_O(nT-T)+\alpha_1\cdot V_S+\alpha_2\cdot V_S^2+\alpha_3\cdot V_S^3+\alpha_4\cdot V_S^4+\alpha_5\cdot V_S^5\ldots \tag{5.8}$$

From Fig. 3.1, we obtain intuitively that $V_S = X - Y\cdot V_{ref}$, where X, Y and V_{ref} are input, output and reference voltage of modulator in Fig. 3.1. From [32], it indicates the coefficients of nonlinear DC transfer characteristic of ΣΔ modulator contain enough information to calculate the harmonic distortions when a realistic input signal is applied. Therefore our immediate work is to obtain the nonlinear DC transfer characteristic from the input X to output Y. In order to determine the nonlinear DC transfer characteristic, we use a DC input signal X is applied to the modulator input, and consider 1-bit quantizer case, we can find out the signal Y will be either one or minus one. Let us denote the probability that Y equals one with the symbol "P", then the probability that Y equals minus one is "$1-P$", and since for a stable modulator [33] , the output of the first integrator cannot grow without limit, the average increment of V_O has to equal zero, this means that

$$\begin{aligned} &P\cdot\left\{\begin{aligned}&\alpha_1\cdot(X-V_{ref})+\alpha_2\cdot(X-V_{ref})^2+\alpha_3\cdot(X-V_{ref})^3\\&+\alpha_4\cdot(X-V_{ref})^4+\alpha_5\cdot(X-V_{ref})^5\end{aligned}\right\}+\\ &(1-P)\cdot\left\{\begin{aligned}&\alpha_1\cdot(X+V_{ref})+\alpha_2\cdot(X+V_{ref})^2+\alpha_3\cdot(X+V_{ref})^3\\&+\alpha_4\cdot(X+V_{ref})^4+\alpha_5\cdot(X+V_{ref})^5\end{aligned}\right\}=0\end{aligned} \tag{5.9}$$

Then

$$P=\frac{\alpha_1\cdot(X+V_{ref})+\alpha_2\cdot(X+V_{ref})^2+\alpha_3\cdot(X+V_{ref})^3+\alpha_4\cdot(X+V_{ref})^4+\alpha_5\cdot(X+V_{ref})^5}{2\alpha_1V_{ref}+4\alpha_2V_{ref}X+6\alpha_3V_{ref}X^2+2\alpha_3V_{ref}^3+8\alpha_4V_{ref}^3X+8\alpha_4V_{ref}X^3+2\alpha_5V_{ref}^5+10\alpha_5V_{ref}X^4+20\alpha_5V_{ref}^3X^2} \tag{5.10}$$

From (5.10), the expected value of Y is given by

$$E\{Y\} = P\cdot 1 + (1-P)\cdot(-1)$$
$$= 2\cdot P - 1$$
$$= \frac{2\cdot\{\alpha_1\cdot(X+V_{ref}) + \alpha_2\cdot(X+V_{ref})^2 + \alpha_3\cdot(X+V_{ref})^3 + \alpha_4\cdot(X+V_{ref})^4 + \alpha_5\cdot(X+V_{ref})^5\}}{2\alpha_1 V_{ref} + 4\alpha_2 V_{ref} X + 6\alpha_3 V_{ref} X^2 + 2\alpha_3 {V_{ref}}^3 + 8\alpha_4 {V_{ref}}^3 X + 8\alpha_4 V_{ref} X^3 + 2\alpha_5 {V_{ref}}^5 + 10\alpha_5 V_{ref} X^4 + 20\alpha_5 {V_{ref}}^3 X^2} - 1$$

$$= \frac{2\alpha_2 {V_{ref}}^2 + 2\alpha_4 {V_{ref}}^4}{2\alpha_1 V_{ref} + 2\alpha_3 {V_{ref}}^3 + 2\alpha_5 {V_{ref}}^5} + \frac{2\alpha_1}{2\alpha_1 V_{ref} + 2\alpha_3 {V_{ref}}^3 + 2\alpha_5 {V_{ref}}^5} X$$
$$+ \frac{4\alpha_2}{2\alpha_1 V_{ref} + 2\alpha_3 {V_{ref}}^3 + 2\alpha_5 {V_{ref}}^5}\frac{X^2}{2!} + \frac{12\alpha_3}{2\alpha_1 V_{ref} + 2\alpha_3 {V_{ref}}^3 + 2\alpha_5 {V_{ref}}^5}\frac{X^3}{3!}$$
$$+ \frac{48\alpha_4}{2\alpha_1 V_{ref} + 2\alpha_3 {V_{ref}}^3 + 2\alpha_5 {V_{ref}}^5}\frac{X^4}{4!} + \frac{240\alpha_5}{2\alpha_1 V_{ref} + 2\alpha_3 {V_{ref}}^3 + 2\alpha_5 {V_{ref}}^5}\frac{X^5}{5!} + \ldots$$

$$= \alpha_0^* + \alpha_1^* X + \alpha_2^* X^2 + \alpha_3^* X^3 + \alpha_4^* X^4 + \alpha_5^* X^5 \ldots \quad (5.11)$$

Where $\alpha_0^*, \alpha_1^*, \alpha_2^*, \alpha_3^*, \alpha_4^*, \alpha_5^* \ldots$ represent the coefficients of nonlinear DC transfer characteristic. Therefore, we use these coefficients and let modulator input $X = A_{in}\cos(\omega_O t)$, from [32], the modulator output will be given by

$$Y = \sum_K \frac{|\alpha_K^*|}{2^{K-1}} \cdot {A_{in}}^K \cos(K\omega_O t + \varphi_K) \quad (5.12)$$

And the K-th harmonic distortion is obtained as

$$HD_K = \frac{1}{2^{K-1}} \frac{|\alpha_K^*|}{|\alpha_1^*|} {A_{in}}^{K-1} \quad (5.13)$$

We turn now to the equation (5.8), it is of paramount importance how α_1, α_2, α_3, α_4, $\alpha_5 \ldots$ could be obtained. This problem can be solved with curve fitting method as was mentioned earlier. Notice that the V_S is defined as a sinusoidal input in this section, so the noise part of V_S is ignored. In order to approximate (5.6), we apply least square method again and neglect the odd terms by reasons of even-function characteristic of Fig. 5.1. Then (5.6) can be approximated by

$$p_i(V_S) = a_1(\alpha_1 + \alpha_3 {V_S}^2 + \alpha_5 {V_S}^4) \quad (5.14)$$

The $p_i(V_S)$ should be fitted through all the points in 0~V_H, where V_H is defined as A_{VS}, and have been discussed in (3.19), so that the sum of the squares of the distances of those points from the $p_i(V_S)$ is minimum. Since the input signal is sinusoid and is uniformly distributed in - A_{VS} ~ A_{VS}, the weighting function is not needed here. Therefore, the sum of the squares is

$$q = \int_0^{V_H} [g_i(V_S) - p_i(V_S)]^2 dV_S$$

$$= \int_0^{V_H} \left[g_i(V_S) - a_1\alpha_1 - a_1\alpha_3 {V_S}^2 - a_1\alpha_5 {V_S}^4 \right]^2 dV_S \tag{5.15}$$

With the method above, the coefficients in (5.15) for q to be minimum can be the solution of follow equations.

$$\begin{cases} \frac{\partial}{\partial \alpha_1}[\int_0^{V_H} [g_i(V_S) - p_i(V_S)]^2 dV_S] = 0 \\ \frac{\partial}{\partial \alpha_3}[\int_0^{V_H} [g_i(V_S) - p_i(V_S)]^2 dV_S] = 0 \\ \frac{\partial}{\partial \alpha_5}[\int_0^{V_H} [g_i(V_S) - p_i(V_S)]^2 dV_S] = 0 \end{cases} \tag{5.16}$$

$$\Rightarrow \begin{cases} \frac{\partial}{\partial \alpha_1}\left[\left[g_i(V_S) - a_1\alpha_1 - a_1\alpha_3 {V_S}^2 - a_1\alpha_5 {V_S}^4 \right]^2 dV_S\right] = 0 \\ \frac{\partial}{\partial \alpha_3}\left[\left[g_i(V_S) - a_1\alpha_1 - a_1\alpha_3 {V_S}^2 - a_1\alpha_5 {V_S}^4 \right]^2 dV_S\right] = 0 \\ \frac{\partial}{\partial \alpha_5}\left[\left[g_i(V_S) - a_1\alpha_1 - a_1\alpha_3 {V_S}^2 - a_1\alpha_5 {V_S}^4 \right]^2 dV_S\right] = 0 \end{cases}$$

$$\Rightarrow \begin{cases} \int_0^{V_H} \left[g_i(V_S) - a_1\alpha_1 - a_1\alpha_3 {V_S}^2 - a_1\alpha_5 {V_S}^4 \right] \times (-2a_1) dV_S = 0 \\ \int_0^{V_H} \left[g_i(V_S) - a_1\alpha_1 - a_1\alpha_3 {V_S}^2 - a_1\alpha_5 {V_S}^4 \right] \times (-2a_1 {V_S}^2) dV_S = 0 \\ \int_0^{V_H} \left[g_i(V_S) - a_1\alpha_1 - a_1\alpha_3 {V_S}^2 - a_1\alpha_5 {V_S}^4 \right] \times (-2a_1 {V_S}^4) dV_S = 0 \end{cases}$$

$$\Rightarrow \begin{cases} \int_0^{V_H} \left[a_1\alpha_1 + a_1\alpha_3 {V_S}^2 + a_1\alpha_5 {V_S}^4\right] dV_S = \int_0^{V_H} g_i(V_S)\, dV_S \\ \int_0^{V_H} \left[a_1\alpha_1 + a_1\alpha_3 {V_S}^2 + a_1\alpha_5 {V_S}^4\right] \cdot {V_S}^2\, dV_S = \int_0^{V_H} g_i(V_S) {V_S}^2\, dV_S \\ \int_0^{V_H} \left[a_1\alpha_1 + a_1\alpha_3 {V_S}^2 + a_1\alpha_5 {V_S}^4\right] \cdot {V_S}^4\, dV_S = \int_0^{V_H} g_i(V_S) {V_S}^4\, dV_S \end{cases}$$

$$\Rightarrow \begin{cases} \int_0^{V_H} a_1 \left[\alpha_1 V_S + \alpha_3 {V_S}^2 + \alpha_5 {V_S}^4\right] dV_S \\ \qquad = \int_0^{V_L} a_1 (1 - \gamma e)\, dV_S + \int_{V_L}^{V_H} a_1 \left(1 - \frac{V_L}{|V_S|} \gamma e^{|V_S|/V_L}\right) dV_S \\ \int_0^{V_H} a_1 \left[\alpha_1 {V_S}^2 + \alpha_3 {V_S}^4 + \alpha_5 {V_S}^6\right] dV_S \\ \qquad = \int_0^{V_L} a_1 (1 - \gamma e) {V_S}^2\, dV_S + \int_{V_L}^{V_H} a_1 \left(1 - \frac{V_L}{|V_S|} \gamma e^{|V_S|/V_L}\right) {V_S}^2\, dV_S \\ \int_0^{V_H} a_1 \left[\alpha_1 {V_S}^4 + \alpha_3 {V_S}^6 + \alpha_5 {V_S}^8\right] dV_S \\ \qquad = \int_0^{V_L} a_1 (1 - \gamma e) {V_S}^4\, dV_S + \int_{V_L}^{V_H} a_1 \left(1 - \frac{V_L}{|V_S|} \gamma e^{|V_S|/V_L}\right) {V_S}^4\, dV_S \end{cases}$$

Then the coefficients were expressed as

$$\begin{bmatrix} \alpha_1 \\ \alpha_3 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} \frac{225}{64 \cdot {V_H}} & \frac{-525}{32 \cdot {V_H}^3} & \frac{945}{64 \cdot {V_H}^5} \\ \frac{-525}{32 \cdot {V_H}^3} & \frac{2205}{16 \cdot {V_H}^5} & \frac{-4725}{32 \cdot {V_H}^7} \\ \frac{945}{64 \cdot {V_H}^5} & \frac{-4725}{32 \cdot {V_H}^7} & \frac{11025}{64 \cdot {V_H}^9} \end{bmatrix} \begin{bmatrix} \int_0^{V_L} (1 - \gamma e)\, dV_S + \int_{V_L}^{V_H} (1 - \frac{V_L}{|V_S|} \gamma e^{|V_S|/V_L})\, dV_S \\ \int_0^{V_L} (1 - \gamma e) \cdot {V_S}^2\, dV_S + \int_{V_L}^{V_H} (1 - \frac{V_L}{|V_S|} \gamma e^{|V_S|/V_L}) {V_S}^2\, dV_S \\ \int_0^{V_L} (1 - \gamma e) \cdot {V_S}^4\, dV_S + \int_{V_L}^{V_H} (1 - \frac{V_L}{|V_S|} \gamma e^{|V_S|/V_L}) {V_S}^4\, dV_S \end{bmatrix} \tag{5.17}$$

Applying (5.11), (5.12), (5.13) and (5.17), the third and fifth settling distortions at the modulator output are

$$HD3 = \frac{\frac{\left|\alpha_3^*\right|}{2^{3-1}} A_{in}^{\ 3}}{\frac{\left|\alpha_1^*\right|}{2^{1-1}} A_{in}} = \frac{\frac{A_{in}^{\ 3}}{2^{3-1}} \left| \frac{12\alpha_3}{(2\alpha_1 V_{ref} + 2\alpha_3 V_{ref}^{\ 3} + 2\alpha_5 V_{ref}^{\ 5}) \cdot 3!} \right|}{\frac{A_{in}}{2^{1-1}} \left| \frac{2\alpha_1}{(2\alpha_1 V_{ref} + 2\alpha_3 V_{ref}^{\ 3} + 2\alpha_5 V_{ref}^{\ 5})} \right|} = \frac{|\alpha_3|}{4|\alpha_1|} A_{in}^{\ 2} \tag{5.18}$$

$$HD5 = \frac{\frac{\left|\alpha_5^*\right|}{2^{5-1}} A_{in}^{\ 5}}{\frac{\left|\alpha_1^*\right|}{2^{1-1}} A_{in}} = \frac{\frac{A_{in}^{\ 5}}{2^{5-1}} \left| \frac{240\alpha_5}{(2\alpha_1 V_{ref} + 2\alpha_3 V_{ref}^{\ 3} + 2\alpha_5 V_{ref}^{\ 5}) \cdot 5!} \right|}{\frac{A_{in}}{2^{1-1}} \left| \frac{2\alpha_1}{(2\alpha_1 V_{ref} + 2\alpha_3 V_{ref}^{\ 3} + 2\alpha_5 V_{ref}^{\ 5})} \right|} = \frac{|\alpha_5|}{16|\alpha_1|} A_{in}^{\ 4} \tag{5.19}$$

It must be noted that the validation of the (5.17) is $V_L < V_H$, otherwise, the settling behavior will operates linearly and has no distortion at output node.

In order to verify the result in (5.18), (5.19), we use MATLAB-SIMULINK to construct a second-order ΣΔ modulator with a multi-bit quantizer. The behavioral settling model in [15] is employed. We assume that $SR = 50 V/\mu s$, GBW = 70MHz, R = 300 Ω, OSR = 100, f_B = 100KHz and C_s = 2pF, and a 100KHz sinusoidal input signal is used. After performing FFT to the output data of the ΣΔ modulator, we obtain the simulated PSD which is shown in Fig. 5.2. It shows that HD3 is -79.69dB and HD5 is -82.51dB. The theoretical harmonic powers calculated from (5.18), (5.19) are HD3 = -80.64dB and HD5 = -83.7dB. These simulated and theoretical results are very close, and these values confirm that our settling distortion model is reasonably accurate.

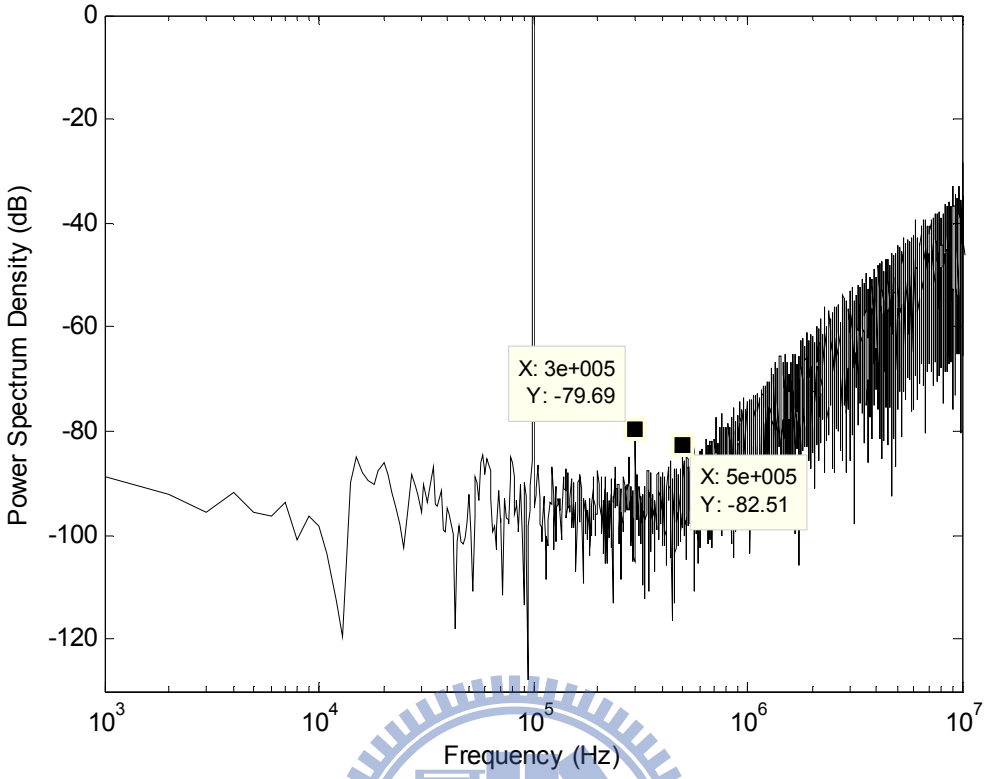


Fig. 5.2 Output spectrum of a second-order $\Sigma\Delta$ modulator with settling harmonic distortion

In order to provide insight on how settling distortions are related to circuit and system parameters, we further analyze the 3rd and 5th harmonic powers as follows:

$$HD3_{Settling}\ (\text{dB}) = 20\log\ (\frac{1}{\sqrt{2}}\frac{|\alpha_3|}{4|\alpha_1|}A_{in}{}^2)$$

$$HD5_{Settling}\ (\text{dB}) = 20\log\ (\frac{1}{\sqrt{2}}\frac{|\alpha_5|}{16|\alpha_1|}A_{in}{}^4) \qquad (5.20)$$

The（5.20）appears that α_1, α_3 and α_5 are functions of T, GBW, R, C_S and SR. Furthermore, due to these non-idealities of OTA such as GBW, and SR limitations will be dramatically affect the harmonic distortions, we put more emphasis on relationships between SR, GBW and the settling distortion. Fig 5.3 shows SR versus HD3 with GBW=65MHz, R = 300Ω, OSR = 100, f_B= 100 KHz and C_s = 2pF, and a 100 KHz sinusoidal input signal. Similarly, Fig. 5.4 shows GBW versus HD3 with SR=60 V/us. These simulated and theoretical results are very close, and these values

confirm that our settling distortion model is reasonably accurate.

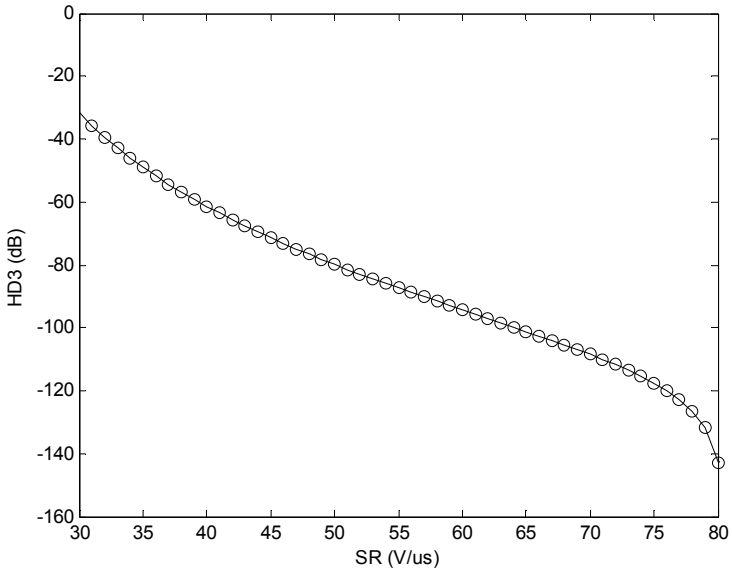


Fig. 5.3 SR versus HD3

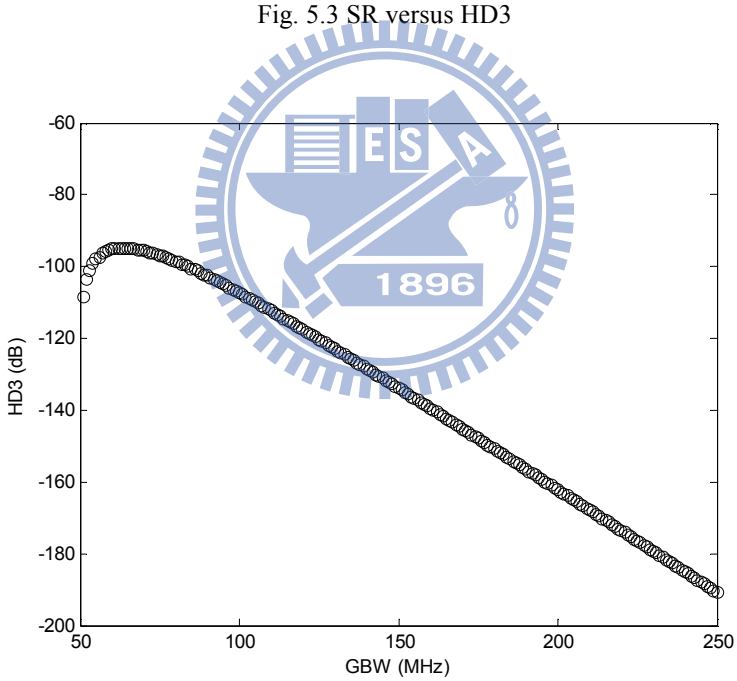


Fig. 5.4 GBW versus HD3

In general, harmonic distortion less than -110dB can be ignored because it is below the noise floor of modulator output spectrum. From（5.20）, Fig. 5.3 and Fig. 5.4, we can obtain the minimum required *SR* and *GBW* w. r. t. the specific *OSR*. The results are summarized in Table 5.1. It is clear from Table 5.1 that as *OSR* increase, *SR* increase dramatically so that the effect of settling distortion can be contained.

TABLE 5.1

Minimum SR and GBW required w. r. t. OSR

OSR	***SR*** $(V/\mu s)$	***GBW*** **(MHz)**
10	≥ 7	≥ 10
20	≥ 13	≥ 16
32	≥ 23	≥ 20
64	≥ 36	≥ 29
80	≥ 50	≥ 40
100	≥ 66	≥ 53
120	≥ 78	≥ 68
140	≥ 85	≥ 72

6.
Simulation Results and Validation

In this chapter, we demonstrate the validation of our models that have been introduced in the previous chapter. The second-order single-loop modulator in Fig. 3.1 is used in order to evaluate the proposed models. We use the HSIPCE simulation as shown in Fig. 6.1 and Fig. 6.2, and the related parameters were: f_B= 100 KHz, OSR = 100, C_S = 2pf, C_i = 4pf, and a 100 KHz sinusoidal input signal. Additional parameters are used in the simulation of Fig. 6.3 are listed in Table 6.1. Fig. 6.3 shows the settling noise and distortion obtained by proposed model and simulated output by transistor-level and behavior model. The theoretical noise power by previous model is obtained by adding the previous settling noise power to the theoretical quantization noise power. The output shows a good agreement between the transistor-level modeled and presented modeled modulator.

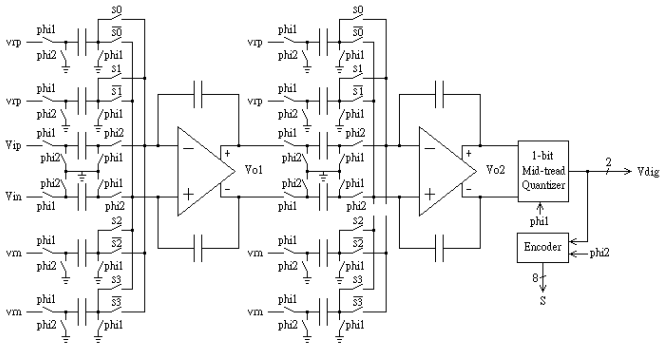


Fig. 6.1 Circuit-level schematic of spice simulation

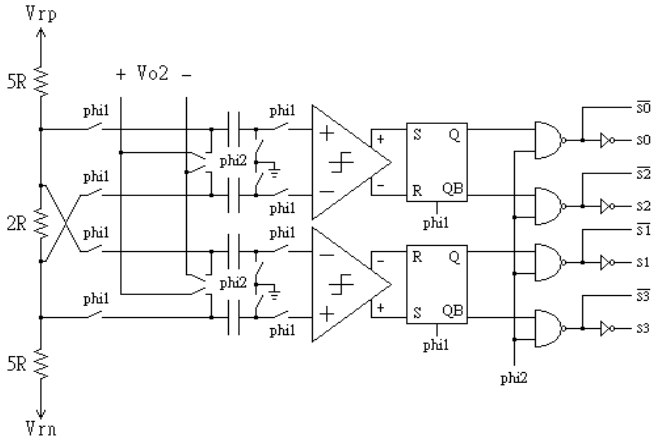
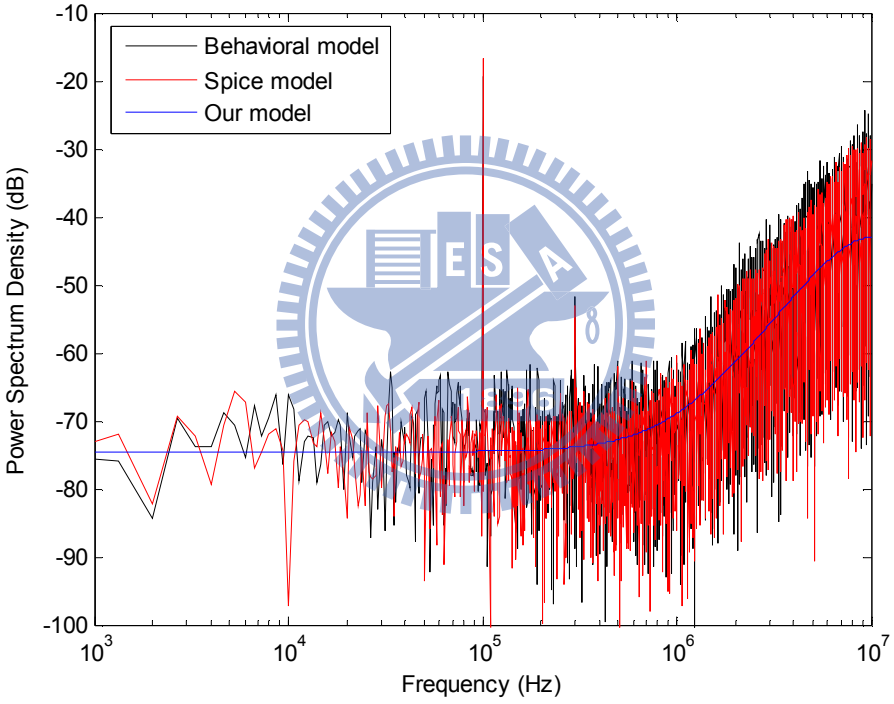
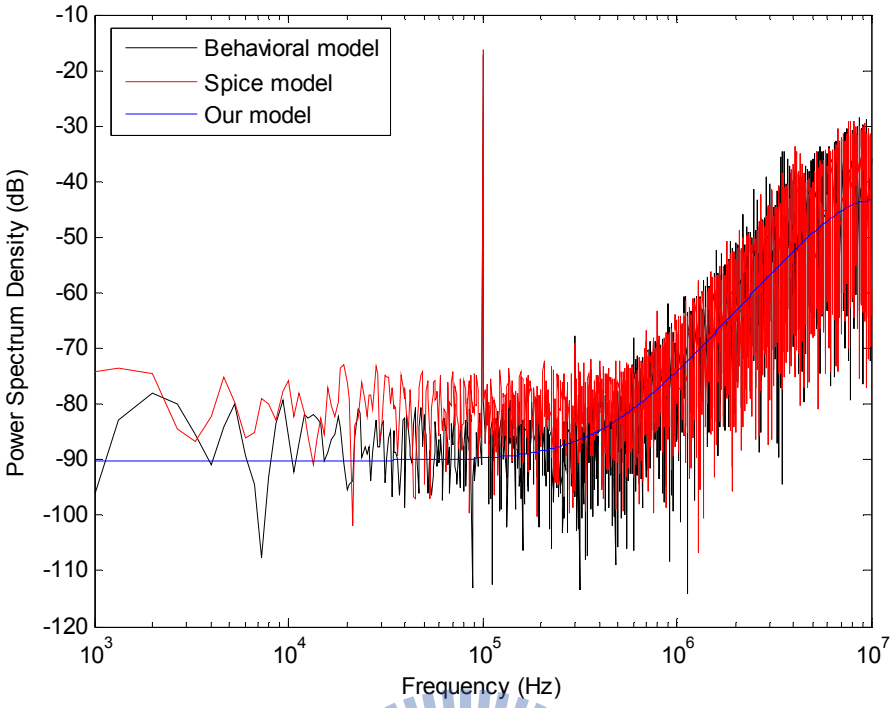


Fig. 6.2 Quantizer of spice simulation



(a)



(b)

Fig. 6.3 Comparison of our theoretical result with transistor-level and behavior simulation result

TABLE 6.1

SIMULATION PARAMETERS IN FIG. 6.3

Parameters	**Fig. 6.3 (a)**	**Fig. 6.3 (b)**
SR $(V/\mu s)$	40	50
GBW **(MHz)**	65	70
P_n **(dB)**	Behavior: -48.433 (dB) Spice: -50.935(dB) Analytic: -52.757 (dB)	Behavior: -63.439(dB) Spice: -58.862(dB) Analytic: -66.227(dB)
HD3$_{amplitude}$ (dB)	Behavior: -51.82 (dB) Spice: -53.09 (dB) Analytic: -53.713 (dB)	Behavior: -67.72(dB) Spice: -68.95(dB) Analytic: -69.676(dB)

As we indicated in the above chapter, the ratio of the signal power to the power of the noise and the distortion components (SNDR) plays a large role in design of $\Sigma\Delta$ modulators. Therefore, it is worth to find the domination between the power of the noise and the distortion. We show the result in Fig. 6.4, and we can observe that the noise energy is dominant over the energy of the distortion. These results are entirely consistent with the previous study [7].

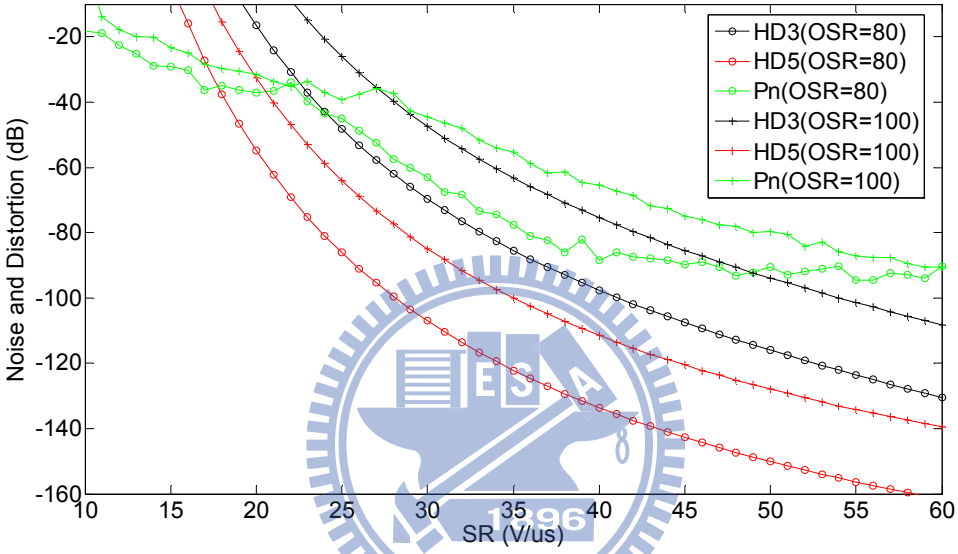


Fig. 6.4 SR versus HD3, HD5 and Noise

Notice that increasing *SR* and *GBW* will reduce nonlinearities of settling problem and increase *SNDR*, but will also increase analog power consumption and the design challenges. On the other hand, multi-bit quantizer can reduce the slew rate requirement, since a multi-bit structure makes the output feedback signal closer to the input signal.

7.
Conclusions and Discussions

While considerable attention has been paid in the past to research issues related to the settling problem of ΣΔ ADCs, a literature on issues of the analytical model of settling noise of ΣΔ ADCs has never derived in the literature, and designer only implemented through time-domain behavior simulations due to its complex dynamic behavior. In this paper, we express an analytical model with nonlinear slewing behavior to adequately estimate the ΣΔ ADCs in-band noise power as a function of ΣΔ modulator system parameters, and add more insights to supplement the findings of the settling distortion model that have been presented in [20-21]. Once the system parameters such as OSR, GBW, and SR are known, the models give the expect value of PSD, and predict the powers of harmonics. Both behavior simulations and HSPICE circuits are employed to verify these analytical models, and the results show that our analytical models are sufficiently accurate. Measurement results suggest that for low order ΣΔ ADCs with high OSR and low Bit-number the settling problem will be bigger than other nonlinearities and becomes the dominant nonlinearities.

References

[1] J. Candy, "A Use of Double Integration in Sigma Delta Modulation," *Communications, IEEE Transactions on [legacy, pre - 1988],* vol. 33, pp. 249-258, 1985.

[2] B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," *Solid-State Circuits, IEEE Journal of,* vol. 26, pp. 618-627, 1991.

[3] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *Solid-State Circuits, IEEE Journal of,* vol. 23, pp. 1298-1308, 1988.

[4] B. DelSignore, D. Kerth, N. Sooch, and E. Swanson, "A monolithic 20 b delta-sigma A/D converter," in *Solid-State Circuits Conference, 1990. Digest of Technical Papers. 37th ISSCC., 1990 IEEE International*, 1990, pp. 170-171, 293.

[5] J. Grilo, I. Galton, K. Wang, and R. G. Montemayor, "A 12-mW ADC delta-sigma modulator with 80 dB of dynamic range integrated in a single-chip Bluetooth transceiver," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 271-278, 2002.

[6] B. J. Farahani and M. Ismail, "Adaptive Sigma Delta ADC for WiMAX fixed point wireless applications," *Circuits and Systems, 2005. 48th Midwest Symposium on,* pp. 692-695, 2005.

[7] R. Gaggl, A. Wiesbauer, G. Fritz, C. Schranz, and P. Pessl, "A 85-dB dynamic range multibit delta-sigma ADC for ADSL-CO applications in 0.18-/spl mu/m CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 1105-1114, 2003.

[8] R. del Rio, J. M. de la Rosa, B. Perez-Verdu, M. Delgado-Restituto, R. Dominguez-Castro, F. Medeiro, and A. Rodriguez-Vazquez, "Highly linear 2.5-V CMOS /spl Sigma//spl Delta/ modulator for ADSL+," *Circuits and Systems I: Regular Papers, IEEE Transactions on [Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on],* vol. 51, pp. 47-62, 2004.

[9] F. Maloberti, P. Estrada, P. Malcovati, and A. Valero, "Validation of data converter specifications with behavioral modeling specifications," Measurement, Elsevier, vol. 31, pp. 231-245, 2002.

[10] H. Zare-Hoseini, I. Kale, and O. Shoaei, "Modeling of Switched-Capacitor Delta-Sigma Modulators in Simulink," IEEE Transactions on Instrumentation and Measurement, vol. 54 ,no. 4, pp. 1646-1654, Aug. 2005.

[11] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma data converters: theory, design, and simulation*: New York: IEEE Press: Wiley-Interscience, 1997.

[12] E. Dallago, P. Malcovati, D. Miatton, T. Ungaretti and G. Venchi, "Analysis of sigma

-delta converters for MEMS sensors using power supply voltage as reference", IEE Proc. Circ. Dev. And Syst., vol. 53, no. 5, pp. 473-479, Oct. 2006.

[13] J. Ruiz-Amaya et al.: "High-level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time ΣΔ Modulators Using SIMULINK-Based Time-Domain Behavioral Models", *IEEE Trans. on Circuits and Systems-I: Regular Papers,* pp. 1795-1810, September 2005.

[14] G. Suarez, M. Jimenez, and F. O. Fernandez, "Behavioral Modeling of Switched Capacitor Integrators with Application to ΣΔ Modulators," in *Circuits and Systems, 2006. MWSCAS '06. 49th IEEE International Midwest Symposium on*, 2006, pp. 709-713.

[15] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on],* vol. 50, pp. 352-364, 2003.

[16] G. Suarez, M. Jimenez, and F. O. Fernandez, "Behavioral Modeling Methods for Switched-Capacitor Σ∆ Modulators," *Circuits and Systems I: Regular Papers, IEEE Transactions on [Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on],* vol. 54, pp. 1236-1244, 2007.

[17] W. M. C. Sansen, H. Qiuting, and K. A. I. Halonen, "Transient analysis of charge-transfer in SC filters-gain error and distortion," *Solid-State Circuits, IEEE Journal of,* vol. 22, pp. 268-276, 1987.

[18] K. L. Lee and R. G. Mayer, "Low-distortion switched-capacitor filter design techniques," *Solid-State Circuits, IEEE Journal of,* vol. 20, pp. 1103-1113, 1985.

[19] J. C. Candy and G. C. Temes, "Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation," *IEEE, New York,* 1992.

[20] F. Medeiro, B. Perez-Verdu, A. Rodriguez-Vazquez, and J. L. Huertas, "Modeling opamp-induced harmonic distortion for switched-capacitor ΣΔ modulator design," in *Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on*, 1994, pp. 445-448 vol.5.

[21] F. Medeiro, A. Perez-Verdu, and A. Rodriguez-Vazquez, *Top-Down Design of High-Performance Sigma-Delta Modulators*: Kluwer Academic Publishers, 1999.

[22] V. M. F. Dias, "A Design Environment for Switched-Capacitor Noise-Shaping A/D Converters", *Ph. D. Dissertation,* Universita' Degli Studi di Pavia, 1991.

[23] C. H. Wolff and L. Carley. "Simulation of Δ – Σ modulators using behavioral models," in *Proc. IEEE Int. Symp. Circuits Syst.,* 1990, pp. 376-379.

[24] V. Liberali, V. F. Dias, M. Ciapponi, and F. Maloberti, "TOSCA: a simulator for switched-capacitor noise-shaping A/D converters," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.,* vol. 12, no. 9, pp. 1376-1386, Sep. 1993.

[25] S. Loeda, H. M. Reekie, and B. Mulgrew, "On the design of high-performance wide-band continuous-time sigma-delta converters using numerical optimization," *Circuits and Systems I: Regular Papers, IEEE Transactions on [Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on],* vol. 53, pp. 802-810, 2006.

[26] O. Bajdechi and J. H. Huijsing, *Systematic Design Of Sigma-delta Analog-to-digital Converters*: Springer, 2004.

[27] G. I. Bourdopoulos, *Delta-SIGMA Modulators: Modeling, Design and Applications*: Imperial College Press, 2003.

[28] Y. Geerts, M. Steyaert, and W. M. C. Sansen, *Design of Multi-Bit Delta-SIGMA A/D Converters*: Kluwer Academic Publishers, 2002.

[29] R. M. Gray, "Quantization noise spectra," *IEEE Trans. Inform. Theory,* vol. 36, pp. 1220-1244, Nov. 1990.

[30] R. Rio Fernandez, F. Medeiro, B. Perez Verdu, J. M. Rosa Utrera, and A. Rodriguez Vazquez, "CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom: Error Analysis and Practical Design," 2008.

[31] S. Rabii and B. A. Wooley, *The design of low-voltage, low-power sigma-delta modulators*: Kluwer Academic Publishers Norwell, MA, USA, 1998.

[32] F. OP'T Eynde and W. Sansen: "*Analog Interfaces for Digital Signal Processing Systems*", Kluwer 1993.

[33] R.Schreier and G. Temes. "*Understanding Delta-Sigma Data Converters*" New York: Wiley/IEEE Press, 2005.