國 立 交 通 大 學

電信工程研究所

碩 士 論 文

一個時脈為 320MHz 訊號頻寬 10MHz 之十二位元

CMOS 連續時間積分三角調變器

A 320 MHz CMOS Continuous-Time Sigma-Delta Modulator

with 10 MHz Bandwidth and 12-bit Resolution

研究生：洪國哲

指導教授：闕河鳴　博士

中　華　民　國　九　十　九　年　一　月

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A Thesis

Submitted to Institute of Communications Engineering

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Communication Engineering

January 2010

Hsinchu, Taiwan

中 華 民 國 九 十 九 年 一 月

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摘要

使用超取樣技巧的積分三角類比數位轉換器由於具有高動態範圍以及低功率消耗的優點，它被廣泛地使用在特別應用的積體電路之上。由於先進製程技術的進步以及結合連續時間類比濾波器的技巧，連續時間積分三角類比數位轉換器的使用近幾年來越來越受到歡迎。因為使用了非取樣式的迴路濾波器，連續時間積分三角類比數位轉換器是可以同時達到高解析度以及 10MHz 以上的訊號頻寬需求，因此能成為一種在功率消耗以及面積使用上都更有效率的類比數位轉換器。

本論文提出一個頻寬為 10MHz 的寬頻連續時間積分三角調變器，並使用台積電的 0.18 微米製程實現。為了達到所需要的規格，所提出的調變器包含了一個三階主動式電阻電容積分器以及操作頻率為 320MHz 之 4 位元量化器。為了降低時脈抖動的敏感度，使用了不歸零式的數位類比轉換器脈衝整形來做實現。回授路徑的時間延遲被設定為半個取樣頻率週期並使用數位式微分器來補償。本論文所提出的積分三角類比數位轉換調變器在 10MHz 訊號頻寬的操作之下可以達到 74dB 以上之訊號雜訊比，功率消耗在 1.8V 之供應電壓之下為 36mW。這樣的規格是可以被使用於生醫影像處理以及無線通訊的應用之上。

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Abstract

Over-sampling ΣΔ ADCs are widely used in application-specific ICs due to their high dynamic range and low power consumption. Thanks to the advance CMOS processes and continuous-time (CT) analog filter technique, the popularity of CT ΣΔ ADCs has been growing recently. Due to the non-sampling loop filter, it is feasible to build high-resolution CT ΣΔ ADCs with a bandwidth up to MHz at the same time, leading to more power- and area-efficient ADCs.

In this thesis, a wide-bandwidth low-power CT ΣΔ modulator with 10 MHz signal bandwidth is implemented in TSMC 0.18 μm CMOS process. To realize such application scenario, the proposed CTSDM comprises a third-order active-RC loop filter and a 4-bit internal quantizer operating at 320 MHz clock frequency. To reduced clock jitter sensitivity, non-return-to-zero (NRZ) DAC pulse shaping is used. The excess loop delay is set to half the sampling period of the quantizer and the excess loop delay compensation is achieved by the discrete-time derivator structure. The proposed CTSDM achieves above 74 dB SNDR (12 ENOB) over a 10 MHz signal band. The power dissipation is 36 mW from a 1.8 V supply and the energy per conversion is 235 fJ from post-layout simulation. The proposed circuitry can be utilized in low-power medical imaging and modern wireless communications.

Acknowledgements

本篇碩士論文能夠順利完成，首先要感謝的是我的指導教授闕河鳴博士；在碩士班的日子裡，闕老師給予我許多研究上寶貴的建議，讓我在遇到問題時能夠找到解決的方法並且突破瓶頸。除了專業知識的指導以外，老師平日特別注重學生獨立思考、分析問題的能力，以及口語表達和思路上面的邏輯性，對於我在研究以及論文的完成上有很大的幫助。

此外，也感謝實驗室的佐昇、嘉儀、順華、江俊、信太、俊誼、秉勳、凱迪、明君學長和春慧學姊在研究以及日常生活上對我的照顧與指導；也謝謝是瑜、鎮宇、鼎國、燦杰同學、登政學弟及筱筑助理在我的課業及生活上的陪伴與幫忙；也謝謝文仲、維盈學弟及鄭錡、舜婷學妹的支持與鼓勵。另外還要特別謝謝仿生中心的林俐如博士和勝豪學長，在我研究遇到困難時能夠給予適當的建議和討論讓我能夠有所突破。有了各位的陪伴，才能讓我在這兩年半的日子裡有如此快樂且充實的研究生活。

最後我要感謝我的父母，讓我在經濟上沒有後顧之憂，能夠全心在學業上的完成。也謝謝所有關心我的家人與朋友，謝謝大家的愛護跟幫忙，讓我能順利的完成學業。

洪國哲

January, 2010 於新竹

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Chapter 1

Introduction

1.1 Introduction of High Speed ADC

For modern wireless communications and medical imaging applications, a high-performance analog-to-digital converter (ADC) is the core building block of analog front-ends. Such system-on-chip (SoC) applications are often accompanied by digital-signal-processing (DSP), which requires an implementation in deep-submicron technology. As the interface between analog and digital data, ADCs must provide higher dynamic range (DR) for the increasing system performance. In addition, ADCs with increasing bandwidth (BW) and resolution are required to support new standard and higher data rates of wireless communications. For example, WiFi and WiMAX standards require that data are transferred in a channel bandwidth above 5 MHz and 10-bit resolution; commercial image sensors need ADCs with above 8-bit resolution and a few 10 MHz clock frequency. Typically, subranging or pipelined ADCs are employed for these applications. However, the linearity of pipelined ADC is limited by the finite opamp gain especially in low voltage process [35]. To compensate these non-idealities, digital calibration [31][32][35] and additional high gain opamp structure must be used to achieve the resolution higher than 10 bits. Thus, the power consumption and chip area will increase largely. Thus, it is less efficient to achieve high resolution with pipelined architecture.

Over-sampling ΣΔ ADCs are widely used in application-specific ICs due to their high dynamic range and low power consumption. Traditionally, discrete-time (DT) ΣΔ ADCs, implemented in switched-capacitor (SC) technique, are suitable for low-bandwidth (less than a few MHz) and high-resolution (above 14-bit) applications. Thanks to the advance CMOS processes and continuous-time (CT) analog filter technique, the popularity of CT ΣΔ ADCs has been growing recently. More discussions about the possibility of building a high speed and high resolution CT ΣΔ ADC for those applications are presented. In [1], the feedback delay problems of CT ΣΔ ADCs were compensated by an additional feedback signal path, and high-resolution performance was achieved by multi-bit quantization; [3] employed multi-stage low-order modulators for stable system and high bandwidth realization; a design-optimized methodology for CT ΣΔ modulator was proposed in [6], resulted in very low power consumption in even high speed operation.

The comparison of recent researches in CTSD- and pipelined ADC is shown in Table 1.1, and the figure of merit (FOM) is calculated according to Eq. 1.1. Assuming that the power consumption of decimator is the same as that of modulator in CTSD-ADC, and we can find out that CTSD-ADCs can achieve better performance than pipelined architecture.

Table 1.1 Comparison of CTSD- and pipelined ADC

	Tech (nm)	VDD (V)	Conversion Rate (MHz)	SNDR (dB)	ENOB (bit)	Power (mW)	FOM	FOM_1	FOM_2 (Normalized)
[31] 2004 JSSC	350	3.3	20	70.8	11.47	254	4477	4477	1184
[32] ISSCC	180	1.8	20	74	12	233	2844	2844	2844
[33] 2005 JSSC	180	1.8	20	64.2	10.40	22	814	814	814
[34] 2006 TCASI	350	1.5	20.48	56.0	9.01	19.5	1847	1847	489
[35] 2009 JSSC	350	3.3	20	70.2	11.37	231	4364	4364	1154
[1] 2004 JSSC	500	3.3	2.2	83	13.50	62	2433	4866	631
[3] 2004 JSSC	180	1.8	20	63	10.17	122	5295	10590	10590
[5] 2006 JSSC	130	1.2	40	74	12.00	20	122	244	468
[6] 2007 TCASI*	180	1.8	20	66	10.67	7.5	230	460	460
[8] 2007 CICC	180	1.8	50	52	8.35	18	1103	2206	2206
[9] 2008 ISSCC	180	1.8	20	82	13.33	100	486	972	972

$$FOM = \frac{Power}{(2^{ENOB} \cdot 2 \cdot BW)} = \frac{Power}{(2^{ENOB} \cdot f_S)} (fJ / conversion) \qquad (1.1)$$

1.2 Motivation

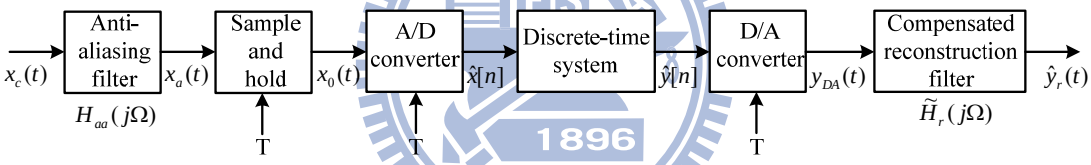


Fig. 1.1 Digital signal processing of analog signals

Fig. 1.1 demonstrates the traditional Nyquist-rate ADCs operation in a DSP system. Compared with Nyquist-rate ADC, over-sampling ΣΔ ADC trades digital signal processing complexity for relaxed requirements on the analog components, so the advance digital CMOS process can be fully utilized. Moreover, CT ΣΔ ADCs exhibit an inherent anti-alias filter function, thus the power-hungry high performance anti-alias filters can be avoided, resulting a low-power DSP system implementation. These unique features are important for mobile applications such as wireless communications or instrument, since these are battery powered and limited in available space. Due to the non-sampling loop filter, it is feasible to build high-resolution CT ΣΔ ADCs with a BW up to MHz at the same time, leading to more

power- and area-efficient ADCs. Thanks to the achievable increasing bandwidth and resolution at low power consumption, the popularity of CT ΣΔ ADCs has been growing.

Table 1.2 compares DT- and CT ΣΔ ADCs, and we can find out that: First, the inherent anti-aliasing characteristics of CT ΣΔ ADCs avoid using a power-hungry front-end filter, hence reduce the power consumption of the whole system. Second, the bandwidth requirement of operational amplifiers in CT filter is much lower than that in DT ones, so CT ΣΔ ADCs can apply for high speed operation easily, and provide high DR as well; but for the CT filters which employ absolute value of passive device to map the filter coefficients, the matching of device element (resistor and capacitor) could be a large uncertainty. Otherwise, more accurate and low-jitter sampling clock is required for CT ΣΔ ADCs driving, or the whole system may be unstable and the operation will be failed.

Table 1.2 Comparison of DT- and CT-ΣΔ ADCs

	DT ΣΔ ADCs	CT ΣΔ ADCs
Input signal	Sampled signal	Continuous signal
Signal BW	~a few 10 KHz	~a few 10 MHz
OSR	Relatively high	Relatively low
Loop filter type	Switched-capacitor	CT loop-filter
Settling requirement	Critical	Relaxed
Sampling frequency	<100-150 MHz	>400 MHz
Anti-aliasing	Need extra filter	Inherent filter
Coefficients mismatch	Very good (0.1%)	Worse (30%)
Clock jitter sensitivity	Low	High

Generally, ΣΔ ADCs are composed of front-end analog modulator and back-end digital decimator (Fig. 1.2(a)). According to multi-channel real-time bio-signals monitoring system (Fig. 1.3) requirements, the thesis proposes a CMOS CT ΣΔ modulator (CTSDM) with 10 MHz signal bandwidth and 12 effective number of bit (ENOB). By combining the over-sampling technique and blackened signal processing, a single SDM is utilized to sample 1024 signals from an electrode array with the signal bandwidth of 9 KHz for high frequency EEG detections. The target performance also promotes CT ΣΔ ADCs as alternative to other types of ADCs for wireless communications and medical imaging requirements. For the higher requirements of next generation applications in the future, the possibility of building CT ΣΔ ADCs will arise more by applying modern CMOS technology and new circuit technique (Fig. 1.2(b)).

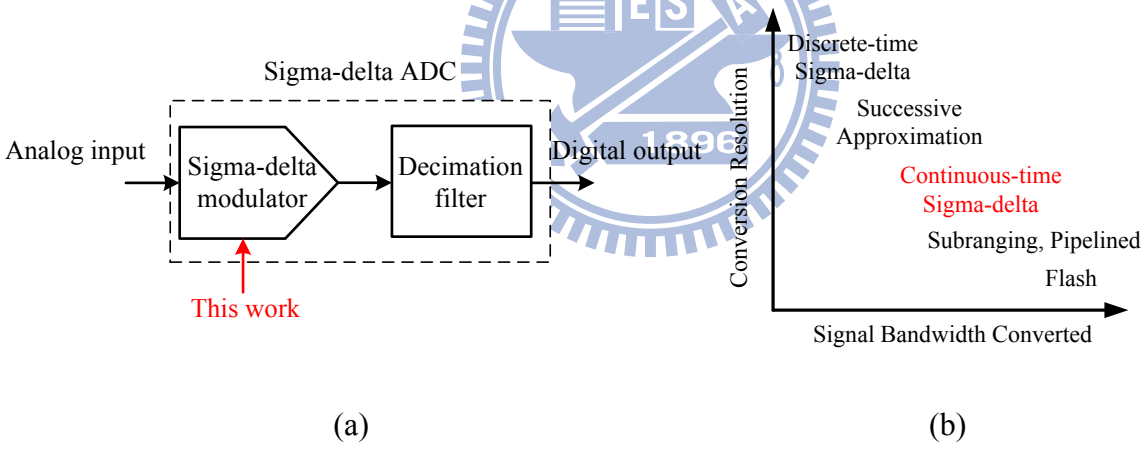


Fig. 1.2 (a) Sigma-delta ADC block diagram (b) Bandwidth resolution tradeoffs

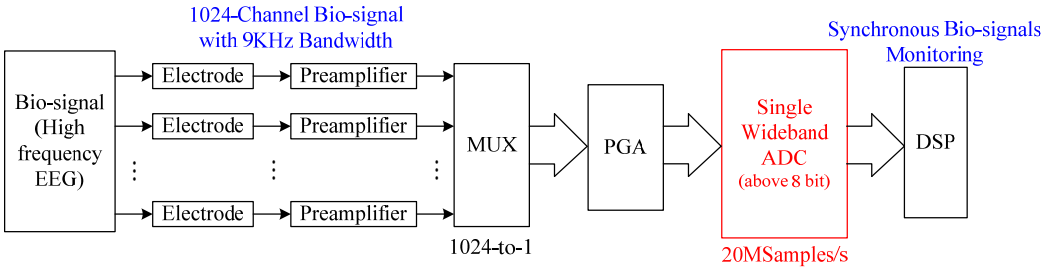


Fig. 1.3 Multi-channel real-time bio-signals monitoring system

1.3 Thesis Organization

This thesis covers theoretical analysis of CTSDM and practical circuit design implementation. After introducing the fundamentals of ΣΔ modulator, the design challenge of CTSDM is discussed. According to the target specifications of the CTSDM, the design procedure from system level to transistor level is detailed. The transistor level simulation and prototype chip measurement are also presented. The thesis is organized as following:

Chapter 1 consists of simple introduction and motivation of this thesis.

Chapter 2 is an overview of general ΣΔ modulator. The fundamental of A/D conversion is introduced briefly, such as sampling and quantization. The principles of oversampling and noise shaping are also described. Furthermore, advance techniques such as multi-stage or multi-bit ΣΔ modulator are introduced, which can achieve higher resolution. Finally, the basic CTSDM architecture is introduced, and the inherent anti-alias filter function is also discussed.

In Chapter 3, some main design issues of CTSDM are considered. Here discusses the non-idealities of CT integrator, including finite gain and unity gain bandwidth of the amplifier. The variation of filter time constant is also covered. After them, the excess loop delay problem is introduced, and some solution of prior work is described. The clock jitter effect is presented finally, which may cause the degradation of the resolution of whole modulator.

Chapter 4 proposes the system level design procedure. Due to the CMOS process limitations and reliability, the system level parameters must be designed carefully. For such a high speed applications, appropriate modulator architecture is very important.

Considering the practical circuit implementation, the loop filter coefficients must be modified form ideal value. The system simulation result of overall modulator is presented in the last part.

In Chapter 5, practical circuit design and implementation is introduced. Some non-idealities of practical circuit implementation are considered. The building block designs of proposed CTSDM are detailed. Finally, the transistor level simulation of CTSDM is presented.

Chapter 6 covers the test environment and the experimental result. Chapter 7 concludes the thesis and discusses some future work.

Chapter 2

Fundamentals of ΣΔ Modulator

In this chapter, the basic concepts of ADC are introduced, including sampling and quantization. Then the fundamentals of ΣΔ ADCs are illustrated, the over-sampling and noise-shaping techniques are described. Above introduction about general ΣΔ A/D conversion is based on [21]. For high speed applications, multi-stage or multi-bit modulator architecture is often used to achieve higher SNR. Finally, the CTSDM topology is introduced. The inherent anti-aliasing filtering effect of CTSDM is presented by an example.

2.1 Sampling and Quantization

Analog to digital conversion is described in terms of two main operations: sampling in time domain, and quantization in signal amplitude. In the sampling process, a analog continuous-time signal is sampled at a unit time interval, T_S, resulting the discrete sampled signal, which can be represented as $x[n] = x(nT_S)$. The effect of sampling process in the frequency domain is to create periodically repeated versions of the signal spectrum at multiples of the sampling frequency $f_S = 1/T_S$, which can be written in Eq. 2.1:

$$X_S(f) = \frac{1}{T_S}\sum_{k=-\infty}^{\infty} X(f - kf_S) \tag{2.1}$$

Assuming the sampling frequency is twice the signal bandwidth, as shown in Fig. 2.1, then the repeated signal spectrum will not overlap in frequency domain exactly, and this signal can be perfectly reconstructed back to continuous time. In other words, a signal with bandwidth f_B must be sampled at a rate greater than twice the bandwidth, $f_S \geq 2f_B$, which is known as Nyquist rate theorem.

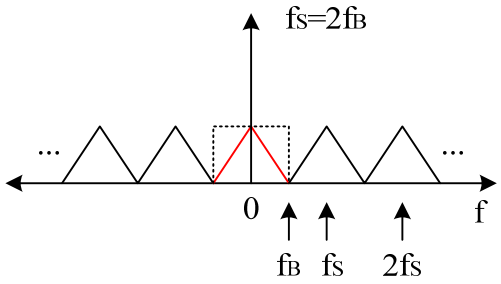


Fig. 2.1 Nyquist rate sampling

But in the real world, an analog signal is not so ideal that contains only one pure frequency. There is always some residual signal energy above the desired frequency results in aliasing if twice the signal bandwidth is used as the sampling rate. In order to avoid this problem, an anti-aliasing filter is often used to ensure that the signal is indeed band limited to half the sampling frequency. However, the analog anti-aliasing filter preceding the sampler must have very sharp cutoff frequency characteristic, which is very power- and area- hungry.

Once sampled, the signal must be quantized to a finite set of output values, and the quantized output amplitudes are usually represented by a digital code word composed of a finite number of bits. In Fig. 2.2, a 1-bit ADC example is shown. If the input signal (x axis value) is greater than 0, than it is quantized to output level V (y axis value), which is mapped to digital code "1." On the other hand, the ADC output will be -V if the input is smaller than 0, and the mapping digital code is "0."

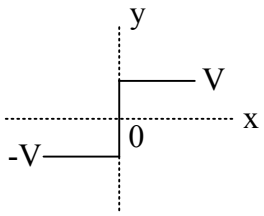


Fig. 2.2 1-bit quantization

For the tractable analysis of the ADC, the behavior of quantization can be modeled as a linear noise source. Here defines the least significant bit (LSB) of an ADC with Q quantization levels is equivalent to $\Delta = 2V/(Q-1)$. The quantization error can be represented as an additional noise source, and the output of ADC is shown as:

$$y[n] = x[n] + e[n] \tag{2.2}$$

The linear model is shown as Fig. 2.3. The magnitude of quantization error $e[n]$ does not exceed half a LSB, provided that $|x[n]| \le V + \Delta/2$, or the ADC will be overloaded.

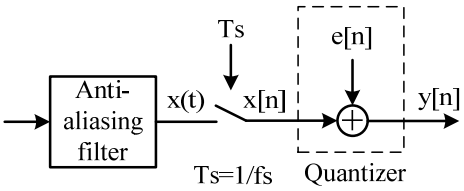


Fig. 2.3 Block diagram and model of a conventional ADC

In general, the quantization error is a white noise process. Consider an N bit ADC with $Q = 2^N$ quantization levels, i.e., with $\Delta = 2V/(Q-1) = 2V/(2^N - 1)$. For a zero mean $e[n]$, its variance σ_e^2 or power is:

$$\sigma_e^2 = \frac{\Delta^2}{12} = \left(\frac{2V}{2^N - 1}\right)^2 \approx \left(\frac{2V}{2^N}\right)^2 / 12 \tag{2.3}$$

If the signal is treated as a zero mean random process and its power is σ_x^2, then the signal to quantization noise ratio is:

$$SNR = 10\log(\frac{\sigma_x^2}{\sigma_e^2}) = 10\log(\frac{\sigma_x^2}{V^2}) + 4.77 + 6.02N(dB) \tag{2.4}$$

Thus, for each extra bit of resolution in the ADC, there is about 6 dB improvement in the SNR. For a sinusoidal input, the dynamic range of the ADC is defined as the ratio of the signal power of a full scale sinusoid ($V^2/2$) to the signal power of a small sinusoidal input that results in a SNR of 1 (or 0 dB, $\Delta^2/12$). The dynamic range expression and the result value is:

$$(\frac{V^2}{2}/\frac{\Delta^2}{12}) \approx (\frac{V^2}{2}/\frac{(2V/2^N)^2}{12}) \tag{2.5}$$
$$DR = 6.02N + 1.76\,(dB)$$

The value of Eq. 2.5 is just the peak SNR of the ADC for a sinusoidal input, i.e., the dynamic range of the Nyquist rate ADC is the same as its peak SNR.

2.2 Oversampling

Oversampling analog-to-digital conversion is a technique that improves the resolution obtained from traditional Nyquist-rate conversion. The improvement is achieved by sampling the signal with a sampling rate which is much faster than Nyquist rate. As shown in Fig. 2.2(a), the same noise power in Nyquist rate case has been spread over a bandwidth equal to the sampling frequency, f_S, while this sampling frequency is much greater than the original signal bandwidth, f_B. Thus, only a small fraction of the total noise power falls in the range between $-f_B$ and f_B, and the out-of-band noise power can be attenuated by the back-end digital low-pass filter.

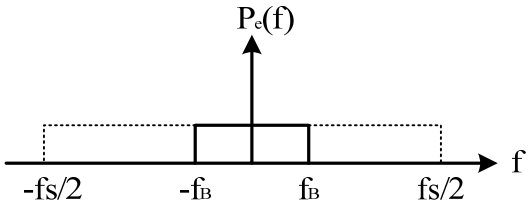


Fig. 2.4 Quantization noise power spectral density for oversampled conversion

After the digital low-pass filter, the signal will be downsampled to the Nyquist rate. The operation of digital low-pass filtering and downsampling is called decimation, and the block diagram of the oversampling ADC model can be shown as Fig. 2.5.

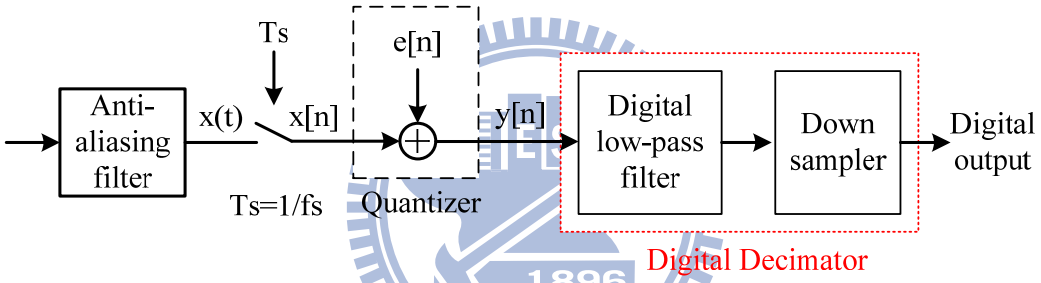


Fig. 2.5 Oversampled conversion system

Assuming that the back-end digital filter is ideal, then the in-band noise power σ_{ey}^2 of the ADC output is:

$$\sigma_{ey}^2 = \int_{-f_B}^{f_B} P_{ey}(f)df = 2\int_{0}^{f_B} P_{ey}(f)df = \int_{0}^{f_B} \frac{2\sigma_e^2}{f_S} df = \sigma_e^2\left(\frac{2f_B}{f_S}\right) \tag{2.6}$$

The maximum achievable SNR is:

$$SNR = 10\log\left(\frac{\sigma_x^2}{\sigma_{ey}^2}\right) = 10\log(\sigma_x^2) - 10\log(\sigma_{ey}^2) + 10\log\left(\frac{f_S}{2f_B}\right)(dB) \tag{2.7}$$

Here define the oversampling ratio (OSR) as $2^r = f_S/2f_B$, Eq. 2.7 can be expressed as following:

$$SNR = 10\log(\frac{\sigma_x^{\ 2}}{\sigma_{ey}^{\ 2}}) = 10\log(\sigma_x^{\ 2}) - 10\log(\sigma_{ey}^{\ 2}) + 3.01r\ (dB) \qquad (2.8)$$

From Eq. 2.8, for every doubling the oversampling ratio r, the SNR of the ADC improves by about 3 dB (0.5 bit resolution). It means that to achieve the same SNR compared with Nyquist rate ADC, the resolution of internal quantizer in oversampling ADC can be much lower than that of the overall conversion resolution, i.e., the analog circuit complexity is simplified by oversampling the signal.

In addition, due to the oversampling technique, the front-end analog anti-aliasing filter does not need a very sharp cutoff frequency. For example in Fig. 2.6, the signal is sampled at four times the signal bandwidth. Here, the anti-aliasing filter can have a transition band between f_B and $f_S/2$, while it still attenuate the out-of-band noise power very well. The design effort in analog circuit can be relaxed more.

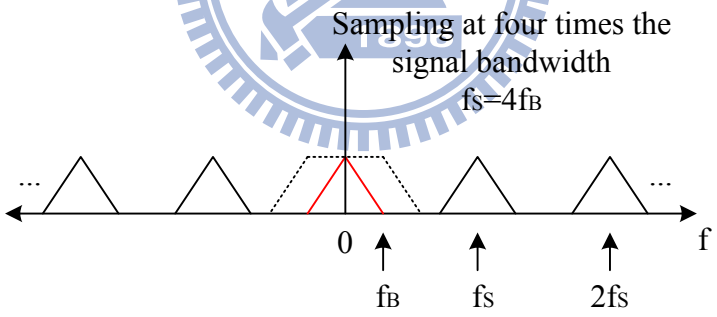


Fig. 2.6 Oversampling ADC example

2.3 Noise Shaped ΣΔ Modulator

In general, the z-domain output of an ADC can be written as:

$$Y(z) = X(z)H_x(z) + E(z)H_e(z) \qquad (2.9)$$

where H_x denotes the signal transfer function (STF) and H_e is the noise transfer

function (NTF). For oversampled ADC, H_e can be designed to be different from H_x. NTF can be modified, which attenuates the in-band noise and amplifies it outside the signal band. The technique is the so called noise shaping or modulation. Just like the oversampled ADCs, the modulator output then is low-pass filtered and finally is downsampled to the Nyquist rate. By oversampling and noise shaping, ΣΔ ADC can achieve very high resolution with relaxed analog circuit requirements, while the price of the improvement in SNR is the increased complexity of the digital hardware.

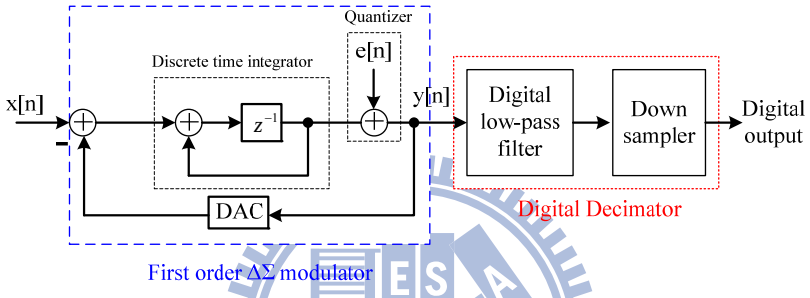


Fig. 2.7 First-order ΣΔ modulator in ADC system

Fig. 2.7 is the block diagram of a first-order ΣΔ ADC. It consists of a front-end modulator and following a digital decimator. The analog modulator covers an integrator, a quantizer and a digital-to-analog converter (DAC).If the DAC is ideal, the z-domain modulator output $Y(z)$ is given by:

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) \tag{2.10}$$

The STF is z^{-1} and the NTF is $(1\text{-}z^{-1})$ in Eq. 2.10. In ΣΔ ADCs, it is common to use 1-bit DAC and a corresponding 1-bit quantizer for the perfect linearity. And the total in-band noise power of the modulator is:

$$\sigma_{ey}{}^2 = \sigma_e{}^2 \frac{\pi^2}{3}\left(\frac{2f_B}{f_S}\right)^3 \tag{2.11}$$

The SNR in dB is:

$$SNR = 10\log(\frac{\sigma_x^{\ 2}}{\sigma_{ey}^{\ 2}}) = 10\log(\sigma_x^{\ 2}) - 10\log(\sigma_{ey}^{\ 2}) - 10\log(\frac{\pi^2}{3}) + 30\log(\frac{f_S}{2f_B})\,(dB) \quad (2.12)$$

With OSR defined as $2^r = f_S/2f_B$, we obtain:

$$SNR = 10\log(\frac{\sigma_x^{\ 2}}{\sigma_{ey}^{\ 2}}) = 10\log(\sigma_x^{\ 2}) - 10\log(\sigma_{ey}^{\ 2}) - 10\log(\frac{\pi^2}{3}) + 9.03r\,(dB) \quad (2.13)$$

From Eq. 2.13, for every doubling the oversampling ratio *r*, the SNR of the ADC improves by about 9 dB (1.5 bits resolution).

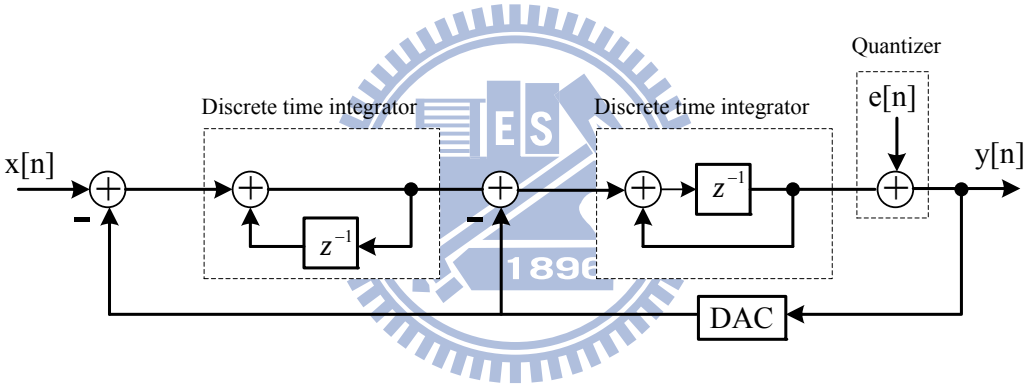


Fig. 2.8 Second-order ΣΔ modulator

Then we consider a second-order ΣΔ modulator, which is widely used in many applications. In Fig. 2.8, the modulator realizes STF is z^{-1} and NTF is $(1-z^{-1})^2$, the output *Y(z)* is:

$$Y(z) = X(z)z^{-1} + E(z)(1-z^{-1})^2 \quad (2.14)$$

Compared with first-order ΣΔ ADC, the second order NTF provides more quantization noise suppression in the signal band and pushes more this noise power to high frequency which is out of band. Again assuming that the second-order ΣΔ modulator output is filtered by an ideal low-pass filter, the in-band SNR is given that:

$$SNR = 10\log(\frac{\sigma_x^{\ 2}}{\sigma_{ey}^{\ 2}}) = 10\log(\sigma_x^{\ 2}) - 10\log(\sigma_{ey}^{\ 2}) - 10\log(\frac{\pi^2}{5}) + 50\log(\frac{f_S}{2f_B})\ (dB)$$

(2.15)

Letting $2^r = f_S/2f_B$, we obtain:

$$SNR = 10\log(\frac{\sigma_x^{\ 2}}{\sigma_{ey}^{\ 2}}) = 10\log(\sigma_x^{\ 2}) - 10\log(\sigma_{ey}^{\ 2}) - 10\log(\frac{\pi^2}{5}) + 15.05r\ (dB)$$

(2.16)

From Eq. 2.16, for every doubling the oversampling ratio r, the SNR of the ADC improves by about 15 dB (2.5 bits resolution).

Finally, we discuss a standard Lth-order ΣΔ modulator based on the extension of the first and second order ones. By realizing higher order NTF, ΣΔ modulator can push more quantization noise outside the signal band and attenuate the in band noise more, thus the higher SNR can be achieved. In other words, the same resolution can be achieved by a lower sampling rate combined with a high order ΣΔ modulator. Thus, the speed requirements on the analog hardware can be relaxed.

The Lth-order NTF is given by $(1\text{-}z^{-1})^L$, and the STF is z^{-1}. The ideal in-band SNR achieved by the Lth-order modulator is :

$$SNR = 10\log(\frac{\sigma_x^{\ 2}}{\sigma_{ey}^{\ 2}}) = 10\log(\sigma_x^{\ 2}) - 10\log(\sigma_{ey}^{\ 2}) - 10\log(\frac{\pi^{2l}}{2l+1}) + (20L+10)\log(\frac{f_S}{2f_B})\ (dB)$$

(2.17)

From Eq. 2.17, for every doubling the oversampling ratio r, the SNR of the ADC improves by about $(6L+3)$ dB (L+0.5 bits resolution). However, unlike first- and

second-order modulator, high order filter do face the stability problem. The quantizer of the modulator could overload due to the saturation of the integrator output. This is a main concern of designing high order modulator.

2.4 Multi-Stage and Multi-bit ΣΔ Modulator

From above discussion, high order ΣΔ modulator can achieve higher SNR but also suffers from stability problem. In additional to single-loop architecture, high order noise shaping can be realized by cascading independent modulator stages.

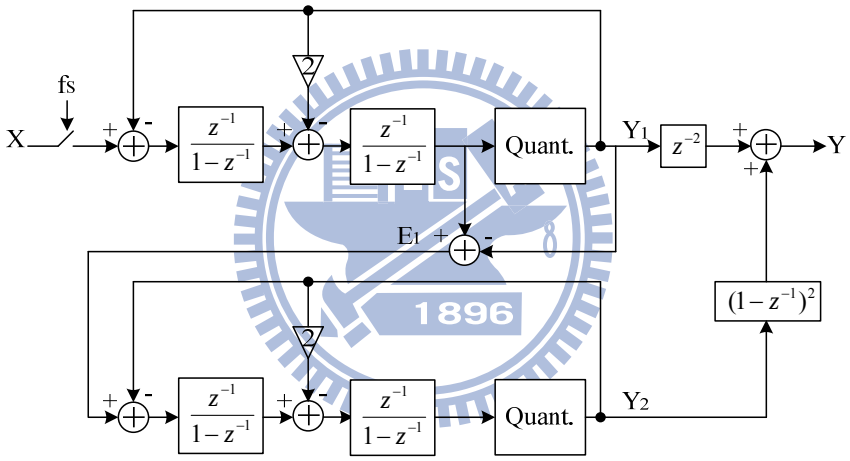


Fig. 2.9 Example of 2-2 cascaded DT ΣΔ modulator

For example in Fig. 2.9 [3], the output of the first modulator stage is connected to the second modulator input, the expression of $Y_1(z)$ and $Y_2(z)$ is:

$$\begin{aligned} Y_1(z) &= z^{-2}X(z) + E_1(z)(1-z^{-1})^2 \\ Y_2(z) &= -z^{-2}E_1(z) + E_2(z)(1-z^{-1})^2 \end{aligned} \tag{2.18}$$

To obtain the final output $Y(z)$, the $Y_1(z)$ and $Y_2(z)$ are passed through a digital delay (z^{-1}) and a digital differentiator ($1\text{-}z^{-1}$) first, then the sum result of Y_1 and Y_2 is :

$$Y(z) = z^{-4}X(z) + E_2(z)(1-z^{-1})^4 \tag{2.19}$$

Finally, the fourth-order quantization noise suppression can be achieved by cascading two single-loop second-order ΣΔ modulators. This implies that the SNR of the cascaded modulator is as high as single loop fourth-order modulator, and the system is guaranteed to be stable the same time. This is the main advantage of the cascaded (or multi-stage) ΣΔ modulator topology.

However, the cascaded structure requires perfect matching between analog and digital transfer function. Otherwise, the quantization noise of first-stage modulator can not be cancelled completely, which may cause significant degradation in overall SNR. Generally, extra calibration circuit must be designed to compensate the mismatch for avoiding this problem.

So far, aforementioned discussions focus on the ΣΔ modulators with only one-bit internal quantizer and DAC. In fact, multi-bit quantization is widely used to achieve even higher resolution. From Eq. 2.5, it is easy to see that for each additional bit used in the internal quantizer, the 6 dB improvement in SNR can be obtained. The behavior of a multi-bit ΣΔ modulator system is more closed to the linear model of quantization noise, and the stability of high order loop modulator using multi-bit quantization is more accurately predicted. Thanks to this technique, the sampling rate can be reduced while keeping the resolution the same, and the speed requirement of analog circuit is relaxed more. Nevertheless, the linearity of the multi-bit DAC in VLSI is a main issue while applying multi-bit ΣΔ modulators. To achieve sufficient linearity needed for high resolution conversion, digital dynamic element matching (DEM) or additional calibration circuits are used. Moreover, multi-bit digital output of the modulator complicates the digital low-pass filter design, and the hardware cost is increased in digital circuit.

2.5 Continuous-time ΣΔ Modulator

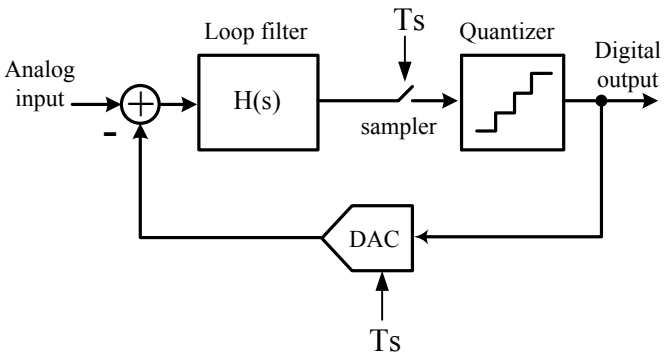


Fig. 2.10 Conventional CTSDM block diagram

Compared with discrete-time architecture incorporating switch-capacitor circuits, more ΣΔ modulator implementations employing continuous-time loop filter have been presented in recent years. A simple CTSDM block diagram is show in Fig. 2.10, which comprises a continuous-time loop filter, a quantizer and a feedback DAC. Traditionally, the maximum sampling frequency which discrete-time ΣΔ modulators can achieve is limited to the operational amplifiers (opamps) requirement. To reduce the settling error and distortion in switch-capacitor circuit, the sampling rate must be as high as five times the gain-bandwidth product (GBW) of the opamps. For CTSDM, this requirement can be relaxed. According to [16], GBW in continuous-time integrators can be as low as sampling frequency without significant degradation of SNR. In other words, CTSDM is more suitable for high speed operation compared with discrete-time one. Besides, due to the non-sampling input stage, CTSDM exhibits an inherent anti-alias filter function.

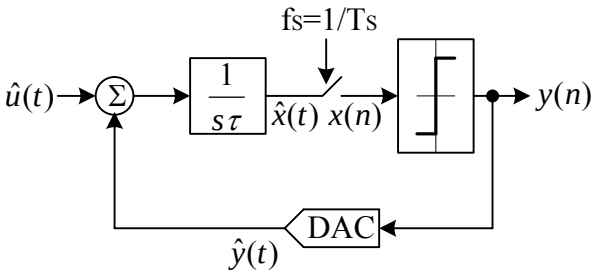


Fig. 2.11 First-order CTSDM

In Fig. 2.11, a first-order low-pass CTSDM is shown as a simple example [16]. The modulator compromises a single continuous-time integrator, a comparator (1-bit quantizer) and a corresponding 1-bit non-return-to-zero (NRZ) DAC. The quantizer input expression in time domain can be obtained:

$$x(n+1) = x(n) - \frac{T_S}{\tau} y(n) + \frac{1}{\tau}\int_{nT_S}^{(n+1)T_S} \hat{u}(t)dt \qquad (2.20)$$

The input signal $\hat{u}(t)$ will be integrated over one clock (T_S) before sampling, and the input integral can be written as:

$$\int_{nT_S}^{(n+1)T_S} \hat{u}(t)dt = \hat{u}(t) * rect(nT_S, (n+1)T_S) = \hat{U}(s) \cdot \sin c(f / f_S) \qquad (2.21)$$

Consequently, the input spectrum is multiplied by a sinc function, which has spectral nulls at frequencies $\pm \alpha f_S, \alpha \geq 1$. In CTSDM, the anti-aliasing property just arises because the sampling happens after the integrator, while the order of the anti-aliasing filter will be increased as well as that of the modulator. Therefore, a high cost analog front-end filter can be avoided in whole ADC system. Above these discussions, continuous-time ΣΔ ADC can achieve high resolution and high speed operation at the same time. Compared with pipelined or subranging type converters, this approach can be more power- and area-efficient for the equivalent SNR and bandwidth,

Chapter 3

Design Issues of CT ΣΔ Modulator

While realizing the CTSDM with practical circuits, the non-idealities of the analog blocks must be considered. These effects may influence the performance of the modulator as well as the stability of the whole system. In this chapter, the main design issues of CTSDM are discussed, covering the non-idealities in CT integrators, excess loop delay and clock jitter. Especially in high speed operations, these errors could degrade the SNR achieved by the modulator significantly. In recent years, many related discussions and compensation methods are presented.

3.1 Non-idealities of CT Integrator

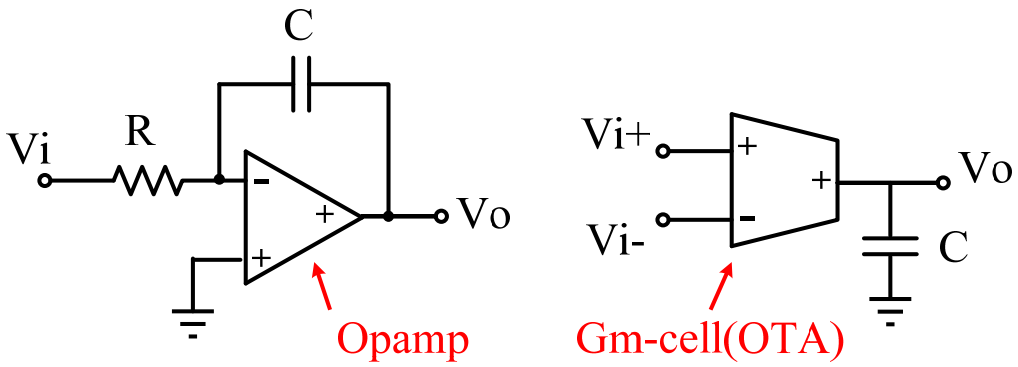


Fig. 3.1 Commonly used CT integrator

The commonly used CT integrators are active-RC integrators and Gm-C integrators, as shown in Fig. 3.1. RC integrators combine passive device with opamp

to perform closed-loop applications. The input of opamp is virtual ground and the output experience very small signal swing, resulting in very good linearity. On the contrary, Gm-C integrators operate under open-loop condition, and the linearity will be decreased due to the large swing of the input. The main advantage of Gm-C ones is the achieved bandwidth can be relative high. The power consumption will be lower than RC integrators for the same speed requirement.

When the RC integrators are employed to build CTSDM, the virtual ground provided by the closed-loop opamp applications can greatly increase the linearity of the feedback DAC whose output is connect to the input of opamp. For Gm-C integrators, the linearity of DAC will be decreased due to the large swing of the integrator output, which is directly connected with DAC output. According to the above analysis, hybrid integrators have been used for the different requirement in multi-stage loop filters [1]. Here, the active-RC integrators are preferred for its good linearity and reasonable power consumption with the target speed requirement, so only the non-idealities of the RC integrators will be discussed.

3.1.1 Leaky CT Integrator

In CTSDM, the first integrator is the most critical and main power-consuming circuit of whole system. Because any errors of this integrator will add to the modulator input directly, the performance of the ADC will be degraded seriously. Thus, its specification requirements should be considered in detail according to the trade off between distortion and power consumption.

First, the dc gain of opamp is discussed. Unlike ideal opamp which has infinite dc gain, the finite gain of real opamp will cause additional parasitic pole in CT integrators. The practical transfer function of the CT integrator due to this effect can be expressed as [13]:

$$ITF_{\varepsilon_{A_0}} = \frac{f_I A_0}{s(1+A_0)+f_I} = \frac{\alpha f_I}{s+\gamma}$$
$$\alpha = \frac{A_0}{1+A_0}, \quad \gamma = \frac{f_I}{1+A_0} \tag{3.1}$$

A_0 represents the finite dc gain of the opamp, and f_I is the inverse of the integrator time constant. α and γ represent the integrator gain error and the pole displacement. In order to minimize the degradation in SNR due to this non-ideality, the gain requirement can be obtained by computing the in-band noise effect. From [13], the critical gain of a third-order CTSDM is :

$$A_{0_{\zeta dB}} \approx \sqrt{\frac{21}{5(10^{\frac{\zeta}{10}}-1)}}\frac{OSR}{\pi} \tag{3.2}$$

ζ represents the loss of the SNR while only leakage is considered. If other distortion and noise are taken into account also, the required dc gain has to be much higher than Eq. 3.2.

3.1.2 Finite Gain Bandwidth of Opamp

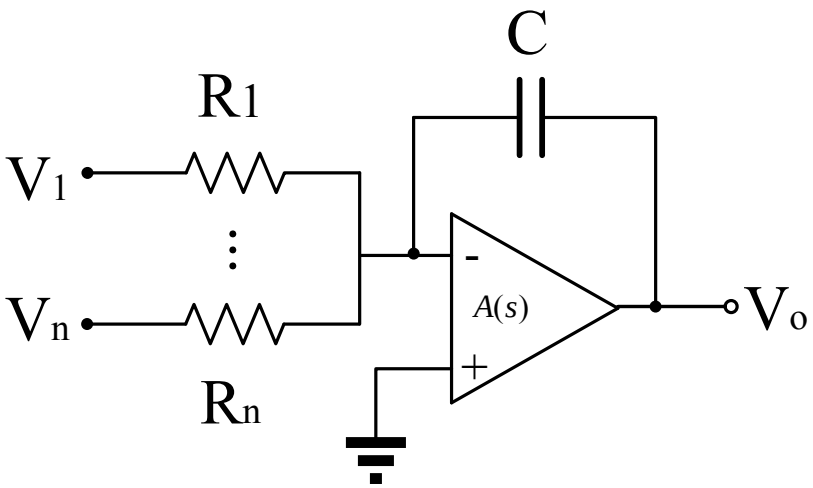


Fig. 3.2 Multi-input active-RC integrator

Fig. 3.2 shows a typical *i*th input integrator employing active-RC topology, and the transfer function of the amplifier is given by $A(s)$. Thus, one can calculate that the output of this integrator can be expressed as [17]:

$$ITF_i(s) = \frac{k_i f_I}{s(1+\frac{1}{A(s)}) + \frac{1}{A(s)}\sum_{l=1}^{N} k_l f_I} \approx \frac{k_i f_I}{s}, A(s) \to \infty \quad (3.3)$$

k_i denotes the scaling coefficient of the *i*th integrator. Compared with ideal opamps, the dc gain and the gain bandwidth product of a real opamp are finite, resulting in an additional non-dominant pole in integrators. This will degrade the loop stability of the entire modulator by pushing the poles closer to the imaginary axis. The transfer function of a real opamp comprises a finite dc gain and several poles and zeros. Taking the influence of finite gain bandwidth into account, the behavior of the simplified non-ideal amplifier can be expressed as:

$$A(s) = \frac{A_{dc}}{\frac{s}{\omega_A}+1}, \quad GBW = A_{dc}\omega_A \ [rad/s] \quad (3.4)$$

ω_A is the dominant pole of the amplifier inside the integrator, and A_{dc} represents the finite dc gain. Incorporating Eq. 3.4 into Eq. 3.3, the entire transfer function is:

$$ITF_{GBW(s)}|_i \approx \frac{k_i f_s}{s} \frac{\frac{GBW}{GBW+\sum_l |k_l f_s|}}{\frac{s}{GBW+\sum_l |k_l f_s|}+1} = \frac{k_i f_s}{s} \frac{GE_{GBW}}{\frac{s}{\omega_p}+1} \quad (3.5)$$

$$c = \frac{GBW}{2\pi f_s}$$

As a rule of thumb, c=2 is a conservative chose that performance loss is negligible and the amplifier do not waste much power at the same time. In CTSDM, some papers found that the GBW could even be as low as sampling frequency.

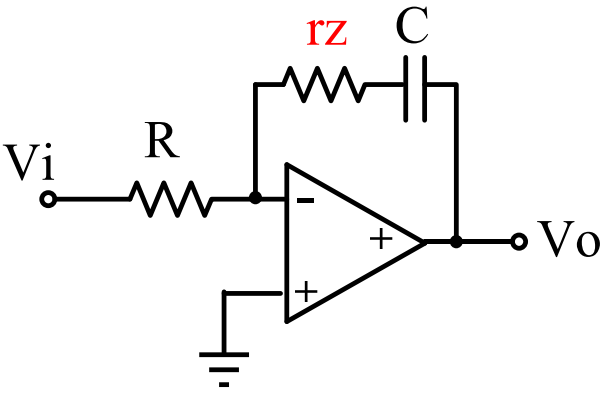


Fig. 3.3 Non-dominant pole cancellation

In order to cancel the parasitic pole, a resistor r_z can be added in front of the integration capacitor. As shown in Fig. 3.3, the value of this resistor is [26]:

$$ITF = \frac{sCr_z + 1}{sRC} \rightarrow r_z \approx \frac{1}{GBW \cdot C} \tag{3.6}$$

3.1.3 RC Time Constant Variation

Because the transfer function of CT integrators is related to the RC time constant which can vary largely due to the process variation and temperature, this non-ideality becomes a challenge in CTSDM design. In modern CMOS technology, the absolute value of resistors and capacitors can vary as large as 10-20%, thus the resulting integrator gain error could be more than 30%. For a real CT integrator, the RC time constant variation can be considered as Δ_{RC} in transfer function, which can be expressed as [17]:

$$ITF_{RC} = \frac{1}{sR_iC(1+\Delta_{RC})} = \frac{f_I}{s}\frac{k_i}{(1+\Delta_{RC})} = GE\frac{k_i f_I}{s} \tag{3.7}$$

The effect of RC time constant can be observed form system simulation incorporating Eq. 3.7 as a non-deal model. Generally, the result will be like Fig. 3.4, which is just an example diagram:

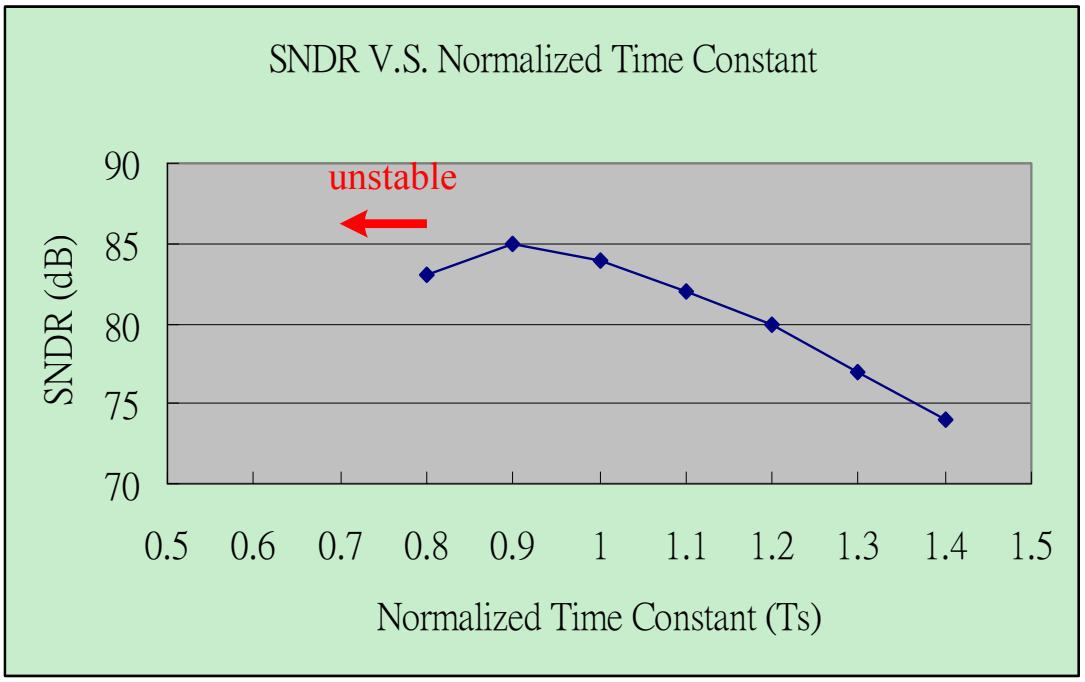


Fig. 3.4 SNDR V.S. time constant variation

The normalized RC time constant is set to be 1 in Fig. 3.4. When the RC tine constant is smaller, a better SNR can be obtained due to the higher gain of loop filter. However, the modulator could be unstable when the gain becomes too larger. On the other hand, a RC time constant is larger than 1 will lead to a more stable modulator, but the achieved SNR will decrease due to the less efficient noise shaping. To compensate this variation, a convenient method can be used by implementing the integration capacitor with tunable capacitor array [1]. As shown in Fig. 3.5, the number of digital control word bit can be designed according to the tuning accuracy requirement.

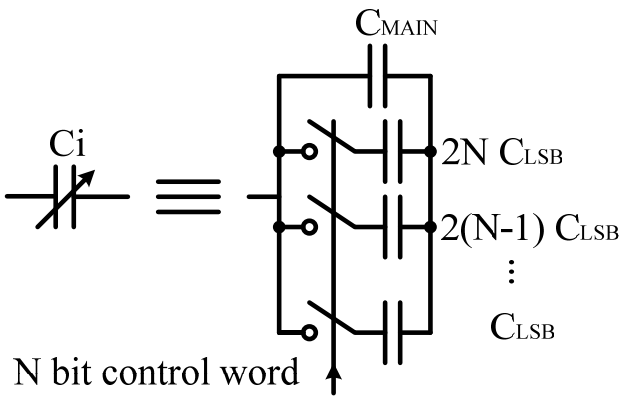


Fig. 3.5 Tunable capacitor array

3.2 Excess Loop Delay

In practical circuit implementation, the speed of transistors is infinite. It means that the delay between sampling clock and circuit output is non-zero. This delay, which is known as excess loop delay, usually consists of quantizer, DAC and loop filter delay. Sometimes, dynamic element matching technique will be employed to enhance the linearity of the multi-bit DAC. However, this extra signal processing will lead to more serious problem.

In general, there are two types of impulse response for feedback DAC output. In Fig. 3.6, return-to-zero (RZ) and non-return-to-zero (NRZ) pulse shaping including the excess loop delay (td) are shown:

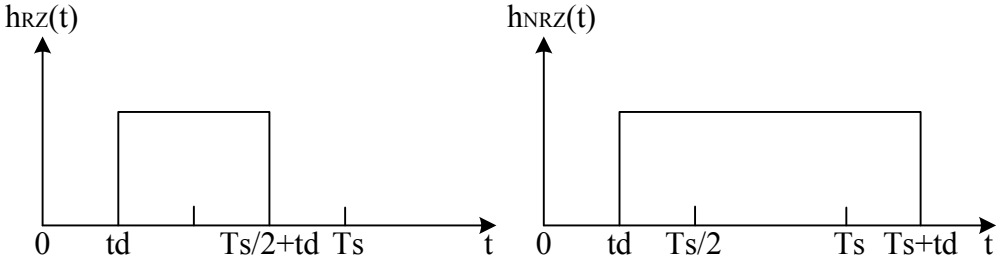


Fig. 3.6 Different types of DAC pulse shaping

From the analysis in [17], if the falling edge of DAC pulse exceeds Ts, then the order of the DT loop filter equivalent to CT one will be higher by one, and the modulator will be unstable. Moreover, excess loop delay could also degrade the effect of noise shaping as well as SNR and dynamic range of modulator. Traditionally, the RZ pulse shaping can be used to relax the excess loop delay. As shown in Fig. 3.6, if the delay is smaller than half the sampling clock period, then the falling edge of DAC pulse is indeed within the range between Ts/2 and Ts, and the order of the equivalent DT loop filter is the same as CT one. Nevertheless, for very high sampling frequency in wideband CTSDM, RZ pulse shaping is more sensitive to clock jitter than NRZ one. Recently, the common solution to the excess loop delay is to use NRZ DAC pulse incorporating an explicit full clock delay in the feedback path. Thus, the varying quantizer delay and other delays caused by digital logic circuit can be absorbed. Besides, in order to compensate the response sample in the CT loop filter, an extra feedback branch will be added directly to the quantizer input to make the impulse response of CT loop equivalent to DT one [1].

3.3 Clock Jitter Influence

In CTSDM, there are two points in Fig. 2.10 where sampling clock jitter will occur and affect the performance of the modulator. First, the sampling error due to the clock jitter in quantizer input will be suppressed due to the high gain of the noise shaping filter, hence the SNR degradation could be negligible. However, the sampling uncertainties of the feedback DAC will produce errors into the modulator input at every sampling instant. These timing errors will appear at the modulator without any attenuation, which may cause the performance degradation of the whole system directly. Thus, the DAC clock jitter is one of the most important issues that should be considered carefully while designing wideband CTSDM.

The sampling uncertainties of DAC could produce errors in the feedback pulse area. The equivalent additive errors can be expressed as [2]:

$$\Delta A[n] = (y[n] - y[n-1]) \cdot \Delta T_{DAC}[n]$$
$$e_j[n] = \frac{\Delta A[n]}{T} = (y[n] - y[n-1]) \cdot \frac{\Delta T_{DAC}[n]}{T} \quad (3.8)$$

$\Delta T_{DAC}[n]$ is the DAC sampling uncertainty and T is the ideal sampling clock period. According to [2], Eq. 3.8 can be utilized in system simulation model to observe the effect of clock jitter noise, and the requirement of the rms clock jitter can be predicted for the whole system, as shown in Fig. 3.7. In [2], the modulator remains stable without significant SNR degradation up to a rms jitter of 30ps at a nominal sampling clock of 300 MHz.

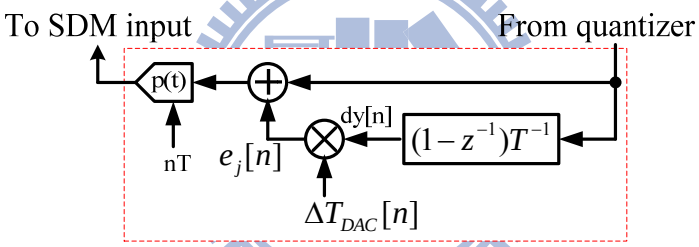


Fig. 3.7 Clock jitter model for feedback DAC

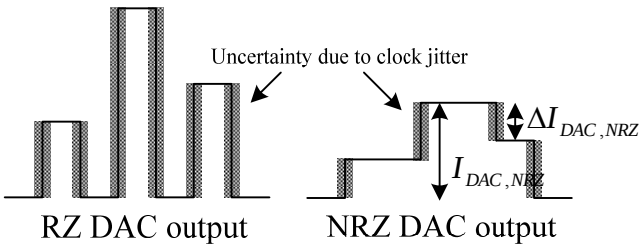


Fig. 3.8 Clock jitter in different types of DAC pulse shaping

In order to reduce the clock jitter sensitivity, multi-bit NRZ DAC pulse shaping is widely used instead of traditional RZ one. To ease the analysis of the jitter noise, one can assumes that the noise introduced by the clock jitter is a white noise spectrum.

In Fig. 3.8, the duty cycle of the RZ DAC output is half the NRZ one. To keep the same area of the output waveform, the amplitude of RZ DAC pulse is twice the NRZ DAC output. As the analysis in [1], the SNR improvement of NRZ pulse shaping over RZ pulse shaping can be derived:

$$SNR_{NRZ-RZ} = 10\log_{10}\left(\frac{8\cdot\sigma^2{}_{I_{DAC,NRZ}}}{\sigma^2{}_{\Delta I_{DAC,NRZ}}}\right) dB \tag{3.9}$$

where $\sigma^2{}_{I_{DAC,NRZ}}$ is the variance of the NRZ DAC output current, and $\sigma^2{}_{\Delta I_{DAC,NRZ}}$ is the variance of $\Delta I_{DAC,NRZ}$.

Chapter 4

System Level Design

In this chapter, the system level design of the proposed CTSDM is described in detail. The top-to-down design flow is introduced, and many system level considerations are discussed, which include the system level parameters, the architecture of the modulator, the loop filter coefficients. In the last part, the overall system simulation is shown.

4.1 System Level Parameters

As described in chapter 1, the target resolution of the proposed CTSDM is 12-bit ENOB with 10 MHz signal bandwidth. Once the specifications of the modulator are decided, the system parameters must be designed carefully to achieve these targets. The ENOB and the corresponding peak SNR (the same as dynamic range) of a SDM can be calculated by the following equation:

$$ENOB = \frac{DR - 1.76}{6.02} \tag{4.1}$$

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N - 1)^2 \times OSR^{2L+1} \tag{4.2}$$

The system parameters in Eq. 4.2 [2] include the resolution of internal quantizer (N), the loop filter order (L) and the oversampling ratio (OSR).

For the target resolution of 12-bit (peak SNR = 74 dB), it is reasonable to set an overdesign specification to 14-bit ENOB (peak SNR = 86 dB), then the decision of the above system parameters is discussed as following: first, one can start from the OSR, which is related to the operating speed of the modulator. Because the target signal bandwidth is as high as 10 MHz, taking the 0.18-μm CMOS process limit and the trade off between GBW and power consumption of opamp into account, a sampling rate of 500 MHz is a reasonable upper bound [8]. In addition, OSR is usually a power of two to simplify the back-end decimation filter design, so the OSR can be 2, 4, 8, 16 or 32 (corresponding sampling rate is 640 MHz). In [8], an OSR smaller than 10 implies that the GBW of the opamp must be high enough than the situation that OSR larger than 10 to provide the loop gain for linear operation. Based on the above discussion, an OSR of 16 (sampling rate is 320 MHz) is an appropriate choice for the modern CMOS process limitation. Second, the loop filter order can be considered for the modulator stability and design effort. A filter order larger than 3 may cause the quantizer overloaded easily and result an unstable system. Moreover, high order loop filter means that the number of the corresponding system coefficients is much more than the low order one, which may complicate the system design. Third, due to the relatively lower OSR in CTSDM than in DT one, multi-bit quantizer is commonly used to achieve the same SNR. Finally, it can be seen that a loop filter order of 3 combined with a 4-bit quantizer is a suitable solution in considering the modulator stability and the achieve performance. With OSR = 16, L = 3 and N = 4 in Eq. 4.2, the resulted peak SNR is 88.19 dB, which is larger than the target specification.

4.2 CT ΣΔ Modulator Topology

As introduced in chapter 2, the single-loop SDM is commonly used for its simple circuit design. Although cascaded or time-interleaved modulators have been presented in some early papers, additional noise cancellation filter or more chip area must be used for the practical implementation, and the circuit design becomes even more complicated. Compared with low-pass loop filter, band-pass and complex ones are employed in some specific applications ICs. But for the target signal bandwidth of 10 MHz, these topologies require much higher GBW in the amplifiers, which are not so power-efficient. So, the proposed CTSDM focuses on a single-loop, low-pass topology.

4.3 Architecture of the Loop Filter

In general, there are two types of the loop filter architectures to form the CTSDM system: cascade of integrators (CI) combined with distributed feedback (FB) or feed-forward (FF) [17].

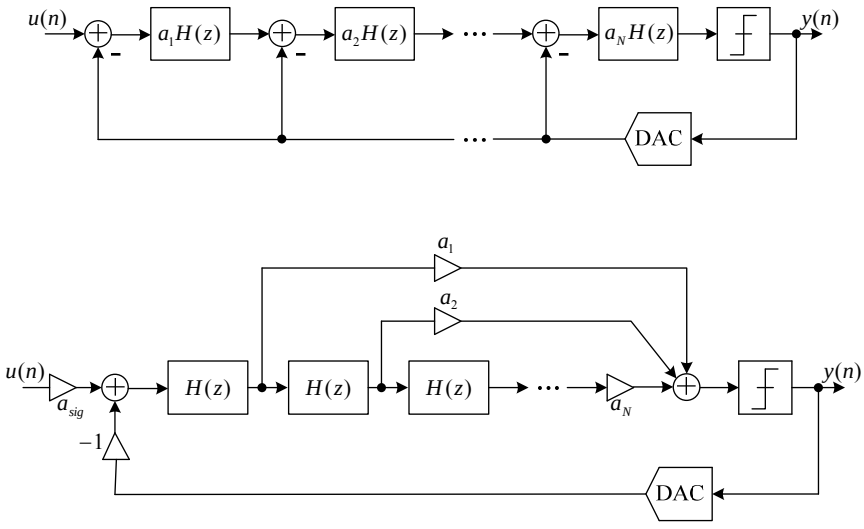


Fig. 4.1 (a) CIFB (b) CIFF

In CIFB architecture as shown in Fig. 4.1(a), the output of every integrator contains a significant amount of the input amplitude, which implies that the integrator will operate at large output swing. In order to avoid the integrator overload, the system coefficients of loop filter must be designed carefully, which are usually smaller than CIFF topology. Smaller passive device in layout means that the matching could be a problem due to process variation. In contrast, CIFF (Fig. 4.1(b)) is more suitable for low power design because of the small swing of the integrator output. But the sum of the feed-forward path could cause overload in quantizer input, a peak transient response also occurs at high frequency of the signal transfer function (STF) at the same time. Combined with above discussion, the hybrid loop filter architecture is presented in [5], which covers the advantages of both CIFB and CIFF ones, and the additional summation circuit is also avoided.

Except for the common topologies in Fig. 4.1, a local feedback loop around pairs of integrators can move the zeros of noise transfer function away from dc and spread over the signal band. Consequently, the in-band SNR will be improved. Moreover, the excess loop delay issue of the CTSDM can be compensated by an extra feedback path, so a additional branch of feedback signal is added in front of the quantizer input. The whole proposed loop filter architecture is shown as Fig. 4.2, where k1, k2 and k3 represent the integrator coefficients, k4 is the feed-forward coefficient, kz denotes the local feedback path, kb1 and kb3 are feedback path, and kd is the compensation coefficient of the excess loop delay.

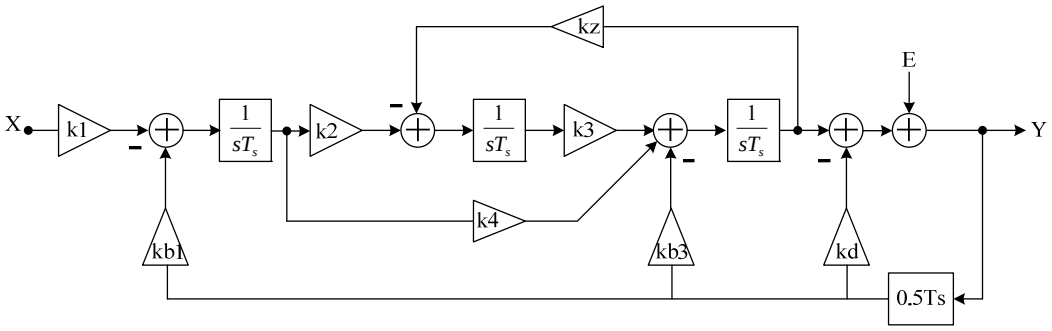


Fig. 4.2 Combination of FF and FB architecture CTSDM

4.4 Loop Filter Coefficients

According to [5], the coefficients of continuous-time loop filter can be derived by MATLAB and delta-sigma toolbox [27][28]. The overall flow is shown as Fig. 4.3: first, substitute the system level parameters into the MATLAB toolbox, then the optimized NTF can be obtained according to [28]. By using the "d2d" (discrete-to-discrete) function, an equivalent transfer function in $z^{1/2}$ is derived. The half sample delay ($z^{-1/2}$) of the quantizer can be incorporated by multiplying $H(z)$ with $z^{1/2}$. Finally, the equivalent continuous-time transfer function in s-domain can be obtained.

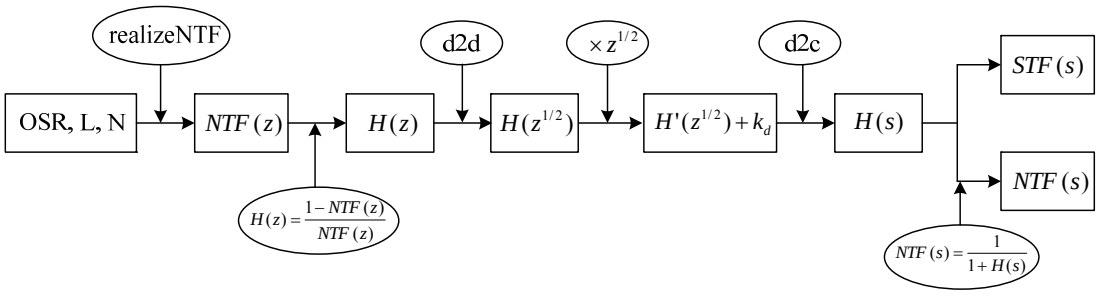


Fig. 4.3 Continuous-time NTF design flow

$$\begin{aligned}
&\mathrm{NTF} = \mathrm{synthesizeNTF}(\mathrm{order}, \mathrm{OSR}, \mathrm{zero_opt}, \mathrm{H_inf}) \\
&\quad = \mathrm{synthesizeNTF}(3,16,1,4) \\
&\Rightarrow NTF(z) = \frac{z^3 - 2.977z^2 + 2.977z - 1}{z^3 - 0.6323z^2 + 0.3002z - 0.05593} \\
&\Rightarrow NTF(s) = \frac{s^3 + 0.02401s}{s^3 + 2.321s^2 + 1.705s + 0.6147} \\
&NTF(s) = \frac{s^3 + k_z k_3 s}{s^3 + k_{b3} s^2 + (k_z k_3 + k_{b1} k_4)s + k_{b1} k_2 k_3}
\end{aligned} \tag{4.3}$$

Eq. 4.3 is the final NTF in s-domain. Combined with this equation and Fig. 4.2, the loop filter coefficients can be chosen. The coefficients considerations are following: first, if the internal integration coefficient is larger than 1, the output of integrators will saturate easily. Second, because these coefficients correspond to the equivalent R-C time constant, considering the matching in practical circuit implementation, it is better to design these coefficients in a ratio relation, so the original coefficients must be modified. The proposed loop filter coefficients for Fig. 4.2 are shown as Table 4.1.

Table 4.1 Proposed loop filter coefficients for CTSDM

(a) original (b) modified

k1	k2	k3	k4	Kz	kb1,3	kd
9/4	0.4267	0.6403	0.7471	3/80	9/4, 2.321	0.9619

(a)

k1	k2	k3	K4	Kz	kb1,3	kd
9/4	3/8	3/4	3/4	3/80	9/4	9/8

(b)

4.5 System Level Simulation

From the above discussion and design considerations, the MATLAB simulink model of whole CTSDM is shown in Fig. 4.4. Fig. 4.5 shows the system simulation result according to the designed loop filter coefficients, and the ideal peak SNR of 88.50 dB (corresponding ENOB = 14.41) is achieved by the proposed third order CTSDM with 4-bit quantizer and an OSR of 16. The amplitude of the input sin wave is 0.4, and the signal bandwidth is 3.203125 MHz. The FFT size is 4096 points.

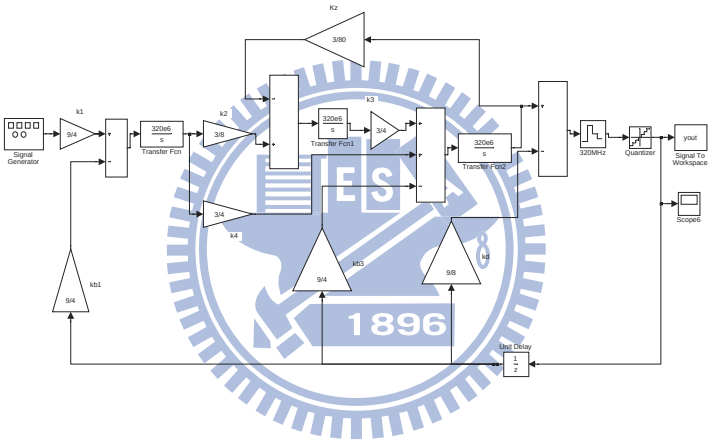


Fig. 4.4 Simulink model of the proposed CTSDM

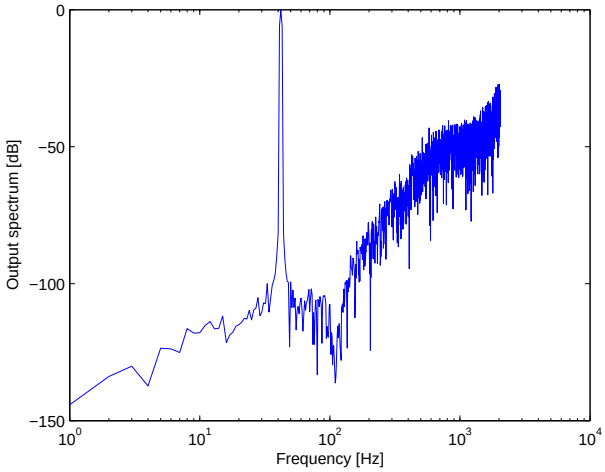


Fig. 4.5 Ideal FFT of the proposed CTSDM

Chapter 5

Circuit Design and Implementation

After system level design and considerations, the practical circuit implementation of the proposed CTSDM must be designed carefully. First, the active RC architecture is considered, and the value of the equivalent resistors and capacitors must be determined according to thermal noise consideration. Then the corresponding building blocks of CTSDM are described, such as two-stage opamp, flash ADC and the feedback current-steering DAC. Clock generator and capacitor tuning circuit are used for the improvement of the SNR. In the last part, the transistor level simulation result is shown.

5.1 Active-RC Integrator

5.1.1 Resistor and Capacitor Consideration

As introduced in Chapter 3, active RC integrator is chosen because of the high linearity and the high gain achieved by the opamp. Once the integrator topology is decided, the corresponding value of the resistors and capacitors must be designed according to thermal noise consideration. Owing to the three stages of integrator in the proposed CTSDM, the effect of induced noise and distortion form the second and third integrators are attenuated by OSR^2 and OSR^4, which are negligible. In order to minimize the influence of the circuit noise, the first stage is the critical one which

must be considered in detail. According to the thermal noise analysis [15] and the target SNR, the maximum value of the usable resistors can be derived as following: the noise source of the first stage integrator is:

$$\overline{dv_{in1}^{2}} = 8k_B TR_1 \tag{5.1}$$

where k_B is Boltzmann constant, R_1 denotes the first integration resistor and T is the absolute temperature. If the other noise of the circuit can be negligible, the total induced noise of the first stage can be expressed:

$$P_{noise} \approx 16k_B TR_1 f_B \tag{5.2}$$

where f_B is the signal bandwidth. Combined with Eq. 5.2 and the signal power of the sin wave, the signal to thermal noise ratio must be larger than the signal to quantization noise, which may not affect the performance of CTSDM. The result is shown as:

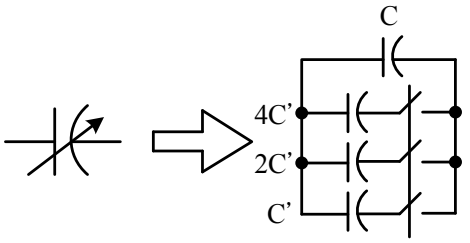
$$\begin{aligned} SNR &= \frac{S_S}{S_N} = \frac{\frac{V_{SW}^{2}}{2}}{16k_B TR_1 f_B} = \frac{V_{SW}^{2}}{32k_B TR_1 f_B} \geq 74.0dB \\ \Rightarrow R_1 &\leq \frac{V_{SW}^{2}}{32k_B Tf_B(SNR)} = 4.808k\Omega \end{aligned} \tag{5.3}$$

where V_{SW} represents the signal swing, which is 0.4 here. According to Eq. 5.3 and Table 4.1, the equivalent resistor and capacitor can be determined by $k_i / T_S = 1/RC$, where T_S is the period of sampling clock. Considering some design margin and practical implementation, the determined values are shown in Table 5.1.

Table 5.1 Resistor and capacitor value of the proposed CTSDM

R1	R2	R3	R4	Rz	C1,2,3
1.388k	8.333k	4.166k	4.166k	83.333k	1p

To compensate the RC time constant variation, the unit integration capacitor is replaced by multiple capacitor array combined with MOSFET switch. Thus, the actual integration capacitor becomes tunable and the effect of process variation can be reduced. The circuit block diagram and the tuning range are shown in Fig. 5.1. According to TSMC 0.18 μm model, the proposed tuning range is sufficient to compensate ±30% resistor variation of real implementation.



$$C_{in-use} = C + k \cdot C' \quad (k = 0 \sim 7)$$

$$C_{\max} = C + 7C' \quad C_{\min} = C$$

$$\text{tuning range}: \frac{C_{\max}}{C_{\min}} = 1 + \frac{7C'}{C}$$

$$\text{tuning accuracy}: \frac{C'}{C + 3C'}$$

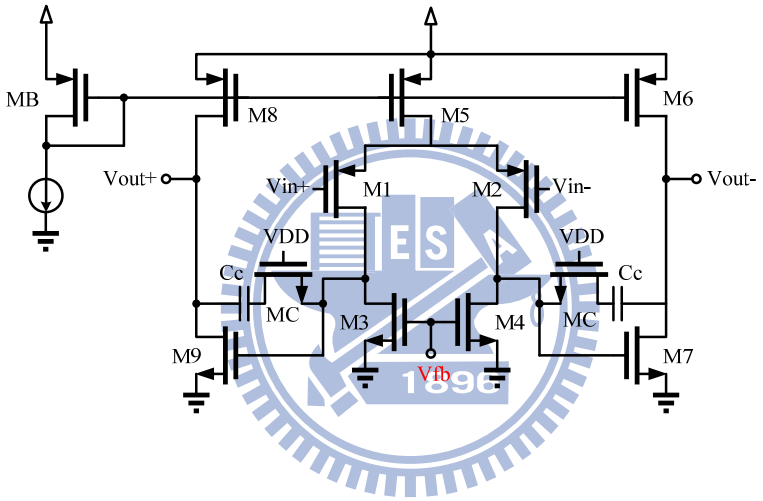
Fig. 5.1 Tunable capacitor array of the proposed CTSDM

As described in Chapter 3, an additional small resistor r_z is added in front of the integration capacitor, which can compensate the influence of the finite GBW effect.

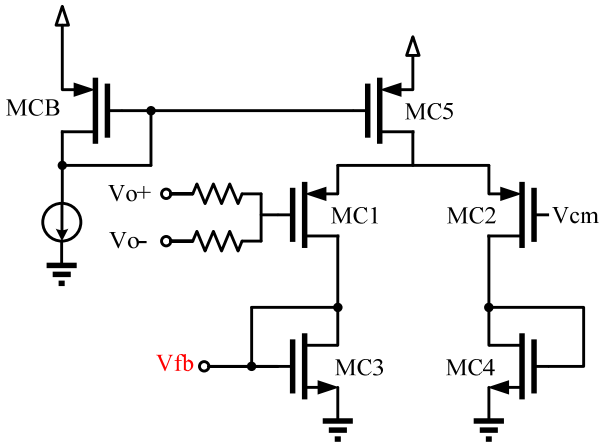
5.1.2 Two-stage Opamp

In CTSDM, the first stage integrator is the most important one because any noise and distortion in this stage is not attenuated by the loop filter, and this will cause significant degradation in SNR. For the resistive loading in continuous-time integrator, one stage opamp is not suitable due to the large output impedance. In [5], multistage opamp with nested Gm-C compensation (NGCC) is used, which can achieve very large gain (>80 dB). However, the frequency compensation of NGCC is very complex, and the multistage architecture may even waste some power consumption. From simpler design, two-stage Miller opamp structure is chosen, since it can provide high

GBW and sufficiently high dc gain, combined with a high output swing [2][8]. The sufficient speed and gain requirements are found by MATLAB analysis. The used opamp structure and the corresponding continuous time common mode feedback (CMFB) circuit are shown in Fig. 5.2. For the same slew rate requirement, the calculated power consumption of NGCC [10] is 9.72 mW, while that of two-stage opamp is 7.92 mW. In other words, assuming that the power from opamp is 60% of whole modulator, the overall power consumption can be saved by 11% while replacing NGCC with two-stage opamp.



(a)



(b)

Fig. 5.2 (a) Two-stage opamp (b) Continuous-time CMFB circuit

The specifications of the opamp are considered as following: according to Eq. 3.4 and [13], a dc gain of 30 dB is sufficient at all. Taking other noise and distortion and design margin into account, a 50 dB dc gain is a chosen, and this is also a requirement to use one-pole integrator model in system simulation [2], which is convenient to observe the non-ideality in modulator behavior. Phase margin (PM) denotes the stability and transient response of opamp, and it is not a critical concern in CTSDM, so a PM of 45° is sufficient. Refer to slew rate, [16] proposed that $SR_{\min} = 1.1\Delta / T_S$, where $\Delta = FS/(2^B - 1)$. In this work, the resulting $SR_{\min}$ is 14.08 V/μS, while the corresponding current is too small for the GBW requirement. In CTSDM, the GBW product is the main consideration, which is a trade off between performance loss and power consumption. As introduced in Chapter 1, the required GBW in DTSDM which employing switch capacitor circuit must be as high as five times the sampling frequency due to the settling limitation. In [16], the GBW could be the same as the sampling rate that the performance loss is still negligible. Here, the appropriate GBW is designed by incorporating the non-ideal model in system simulation. Using Eq. 3.5 into MATLAB simulink, the simulated SNR due to the gain error and non-dominant pole can be observed:

Table 5.2 SNDR V.S. GBW of opamp

	SNDR	ENOB
Ideal	89.35 dB	14.55
c=2	85.59 dB	13.93
c=1	84.06 dB	13.67
c=0.5	77.42 dB	12.57

where c denotes the ratio between GBW and sampling rate (in rad/s). From Table 5.2, one can find that when the GBW is reduced from c=1 to c=0.5, the SNDR is degraded about 6 dB, which is about 1-bit in ENOB. Considering the design margin due to the process corner variation, the target is set to be larger than two times the sampling frequency. The simulated frequency response of the used opamp is shown in Fig. 5.3, and the specifications are shown in Table 5.3.

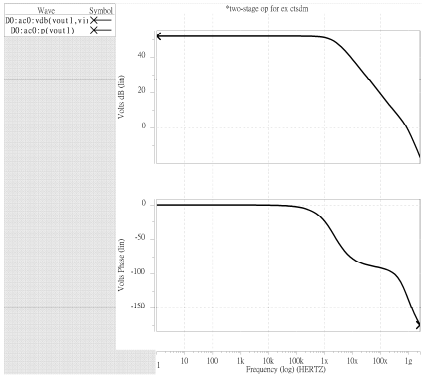


Fig. 5.3 Frequency response of the two-stage opamp

Table 5.3 Performance of the two-stage opamp

Technology/Power supply	Tsmc 0.18 μm/1.8 V
DC Gain	51.6 dB
CMRR/ PSRR	75.3 dB/71.9 dB
Phase margin	48.3°
Unity gain frequency	851 MHz (>2fs)
Slew rate	390(V/uS)
Output swing	>1.4 V
ICMR	>0.3 V
Power dissipation	8.86 mW (Opamp+CMFB+Bias)
CL	1.5 pF//4.166 kΩ//8.333 kΩ

5.2 Current-steering DAC

In high speed applications, current-steering topology is widely used for multi-bit DAC. As shown in Fig. 5.4, the output of DAC is current mod, so it is easy to connect the continuous-time loop filter without any other transform circuit. The input of the DAC is multi-bit thermometer code, while the output is fully differential current.

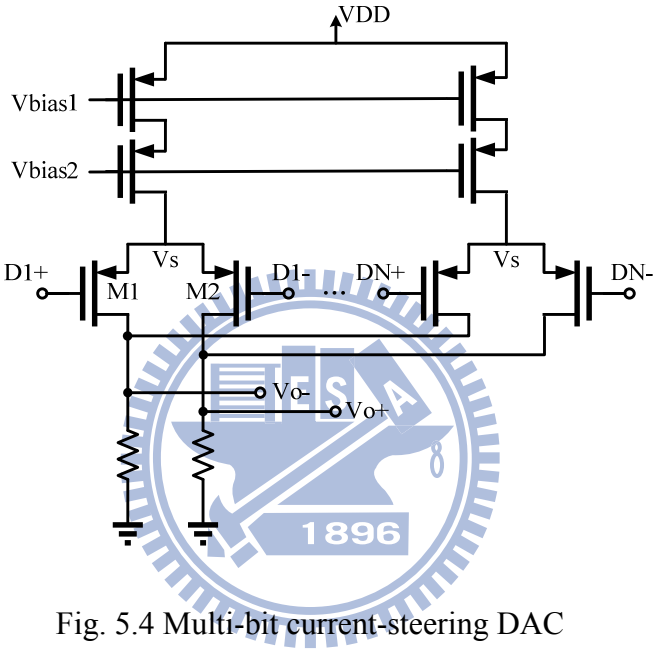


Fig. 5.4 Multi-bit current-steering DAC

The main design issue for multi-bit current steering DAC is the linearity consideration. Dynamic element matching or current calibration technique is commonly used to achieve high linearity, but extra power consumption and loop delay may occur, which is not suitable for wideband CTSDM. To achieve intrinsic high linearity, a large area device must be used for sufficient matching in circuit implementation. According to [11], the required size of the device element could be determined. Assuming a normal distribution for the unit current sources, the required accuracy of the current sources is given by:

$$\frac{\sigma(I)}{I} \leq \frac{1}{2C\sqrt{2^N}} \tag{5.4}$$

where C is equal to the inverse norm of (0.5+yield/2), and yield is the relative number of DAC with an INL<0.5 LSB. For 14 bits resolution and 99.7% INL yield requirement, $\frac{\sigma(I)}{I} \le 0.13\%$ can be found. Based on the process parameter mismatch model, an expression for $(WL)_{min}$ of the unit current source transistor can be derived:

$$(WL)_{\min} = \frac{1}{2}[A_\beta{}^2 + \frac{4A_{VT}{}^2}{(V_{GS} - V_T)^2}]/(\frac{\sigma I}{I})^2 \qquad (5.5)$$

where A_β and A_{VT} are mismatch parameters, which are defined in the mismatch statistical model provided by the foundry. For V_{VO}=0.31 V, one can obtain that $(WL)_{min}$ must be larger than 288 μm^2.

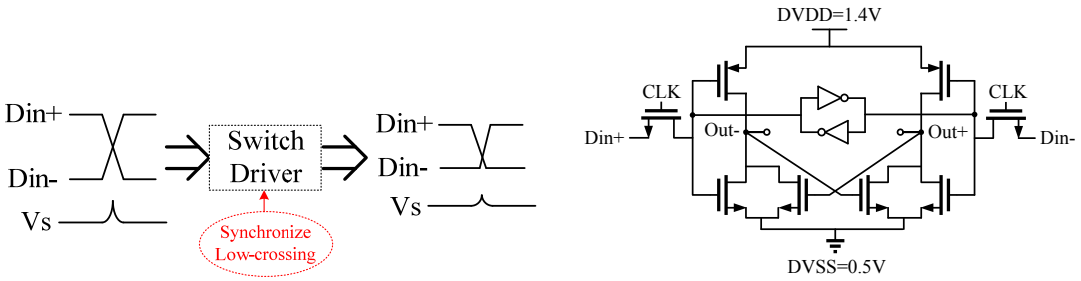
The full swing scale current of the first DAC can be determined by considering the thermal noise of M1,2 in Fig. 5.4. As mentioned in [7], the SNR requirement due to the first DAC can be expressed:

$$SNR_{DAC} = \frac{P_{signal}}{2n_{DAC}} = \frac{I_{DAC}(V_{GS} - V_T)}{32kT\gamma\Delta f} > 74dB \qquad (5.6)$$

With the target design parameters as discussed before, the I_{DAC} must be larger than 61μA.

The first feedback DAC is the most critical block in CTSDM that it is connected to the modulator input directly. Because the non-idealities and distortion of this DAC will influence whole modulator without any suppression, the linearity requirement of the first DAC must be eve higher than the resolution of whole modulator system. Except for the large size device is used, the linearity can be improved by enlarge the output impedance of the current cell, which is achieved by cascading the transistors at output node. Besides, a low-crossing point switch driver is employed in front of each current cell. This driver is composed of a latch that can change the cross point of the

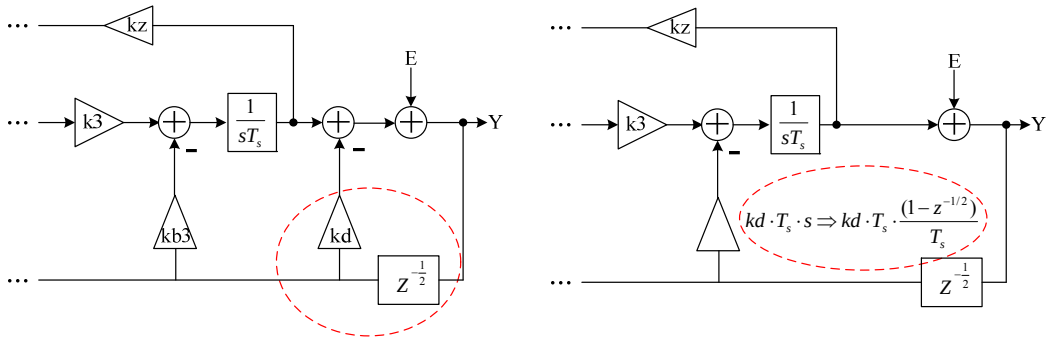
input digital signal, which make the switch transistors still saturated even the input signal is toggled. Thus, the induced glitch is increased and the linearity of the current source is improved more. The block diagram of the switch driver is shown in Fig. 5.5.



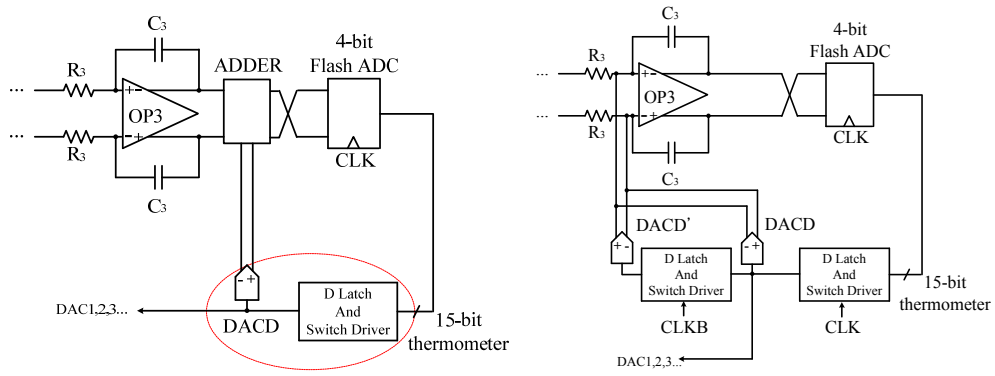
(a) (b)

Fig. 5.5 (a) Low-crossing point to reduce the glitch (b) The switch driver circuit

As described in Chapter 3, the excess loop delay could be a problem in CTSDM design. In Fig. 4.2, an additional feedback path kd is already introduced to solve this problem (Fig. 5.6(a).(c)), which implies that an extra DAC must be implemented in the feedback loop. According to [5], this path can be moved to the input of the third integrator, then the high power-consuming adder is avoided. Finally, this feedback path is realized by a third DAC, while the CT derivator is replaced by DT derivator (Fig. 5.6(b),(d)).



(a) (b)



(c) (d)

Fig. 5.6 Excess loop delay compensation by using DT derivator

In order to compensate the common mode offset in opamp virtual ground, an additional current source is added in opamp input (Fig. 5.7), where Imax is the maximum output current of the first feedback DAC.

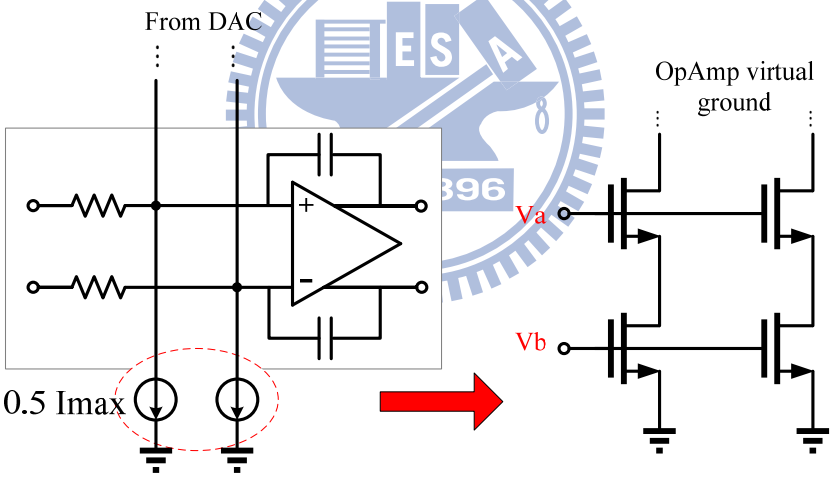


Fig. 5.7 Additional current source to compensate the common mode offset

5.3 4-bit Quantizer

Flash ADC is widely used in multi-bit quantization due to the capability of high speed operation. In Fig. 5.8, it comprises 15 dynamic comparators combined with a SR latch. In whole CTSDM system, any non-ideal effect of the quantizer is attenuated by the noise shaped loop filter, so the induced noise and distortion requirements are

relaxed. As a trade off between feed through and power consumption, the unit resistor in resistor ladder is designed to be 40 Ω.

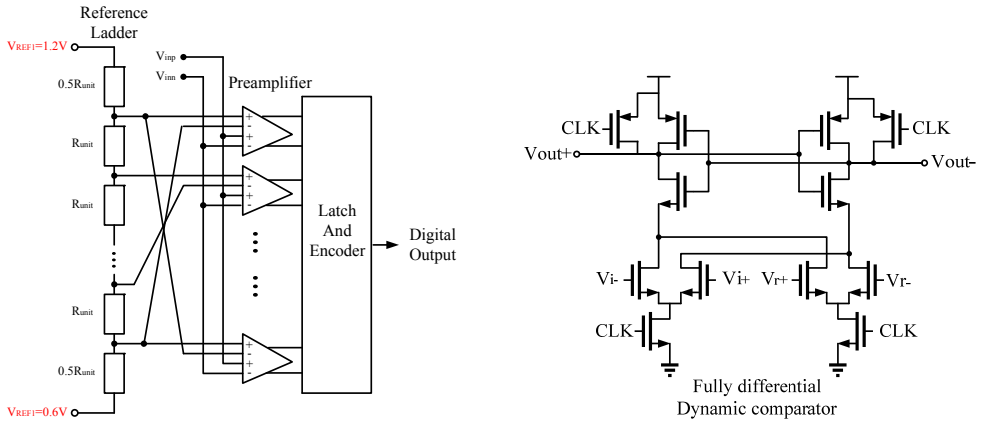


Fig. 5.8 Flash ADC and the dynamic comparator

The output of the 15 comparators is 15-bit thermometer code, which will be converted to 4-bit binary code for the modulator output. The digital encoding is implemented by the Wallace tree thermometer-to-binary converter [23], which incorporating several 1-bit full adder [24]. As shown in Fig. 5.9, to compute the sum of logic 1 in thermometer input, the binary output can be obtained easily. Although the Wallace tree structure is not the fastest operation, this encoder is the most hardware economic one.

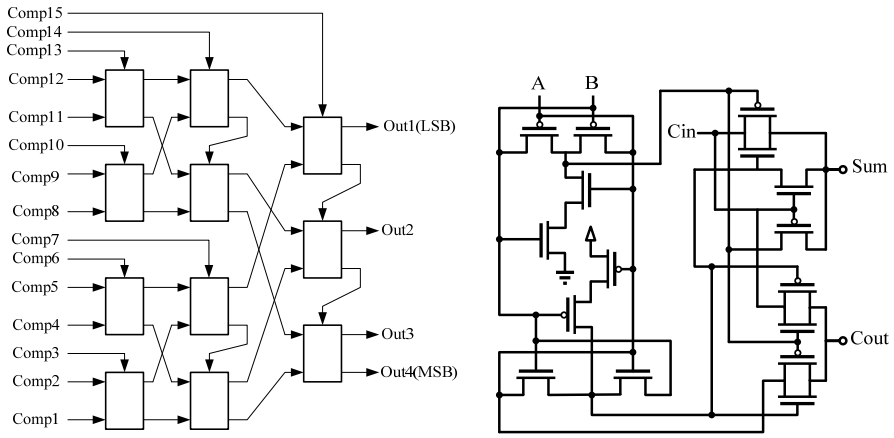


Fig. 5.9 Wallace tree converter and the 1-bit full adder

5.4 Clock Generator

Unlike the non-overlap clock in DTSDM which employing switch capacitor, the clock generator in CTSDM is simpler. In the proposed CTSDM, there are three points that the sampling clock must drive the digital circuit: flash ADC (CLK F), DAC3 (CLK L2) and DAC1,2 (CLK L1). Because of the finite speed of the transistor switching, these clock pulse edges can not be as the same as in system simulation. The delay between different clock edges must be designed carefully that it will not degrade the performance of CTSDM and even make system unstable. To compensate the delay issue, voltage control delay line has been used in some reference, but this may increase the complexity of circuit design. Here, a simple clock generator is used to provide the three different phases of clock edge (Fig. 5.10). The overall circuit level simulation result combined with this clock generator is acceptable in different corner variation, so the complicated tunable delay line is avoided.

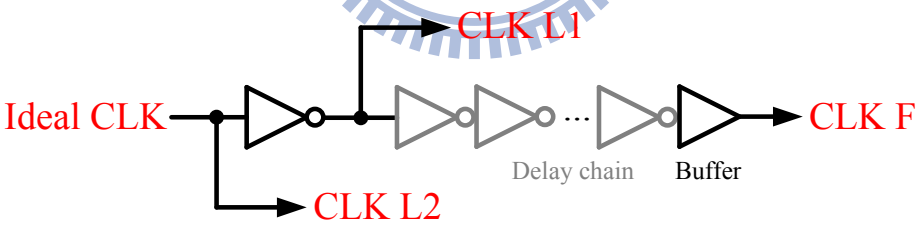


Fig. 5.10 The proposed clock generator

5.5 Transistor Level Simulation

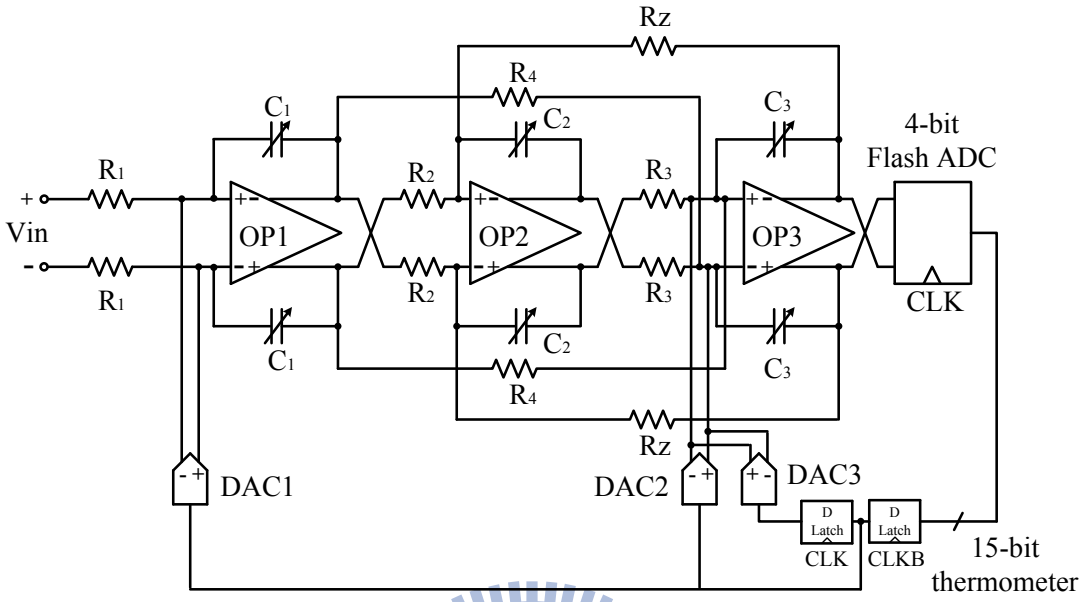
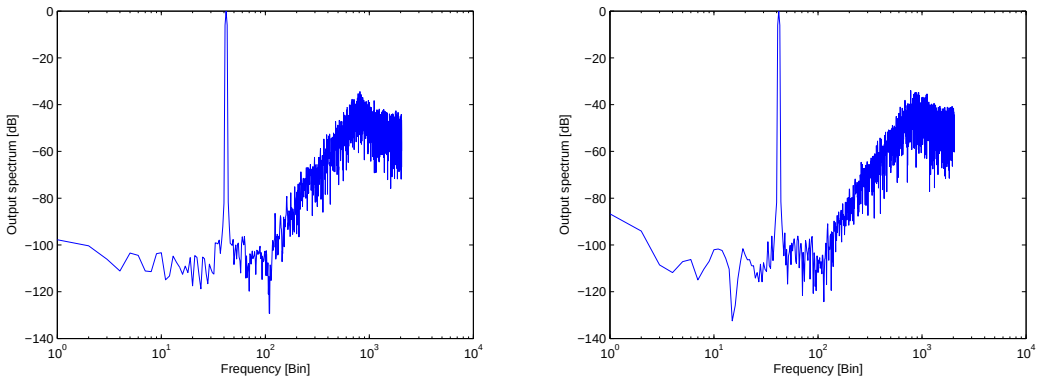
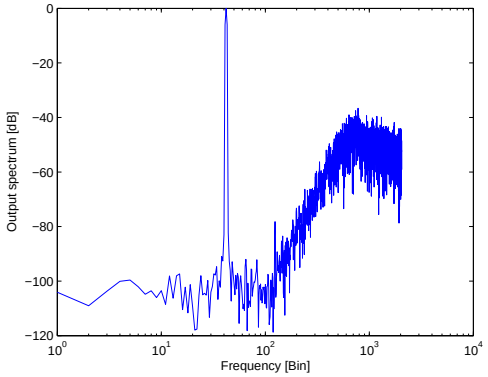


Fig. 5.11 Overall circuit implementation of the proposed CTSDM

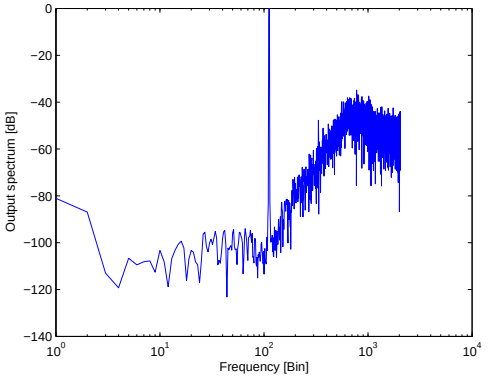
The overall circuit implementation diagram of the proposed CTSDM is shown in Fig. 5.11. The input is fully differential sin wave and the modulator output is 4-bit binary code. The transistor level simulation results are shown as following: Fig. 5.12 is the FFT for different input signal and simulation condition.



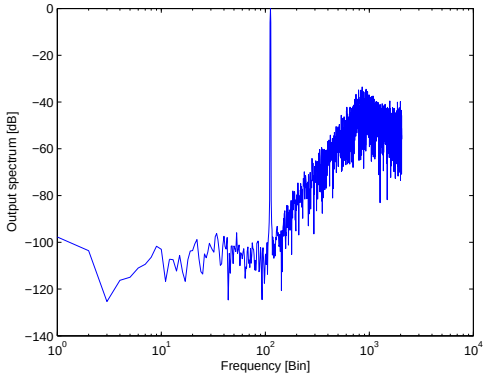
(a) Fin=3.203125 MHz TT corner 25℃ (b) Fin=3.203125 MHz FF corner 0℃



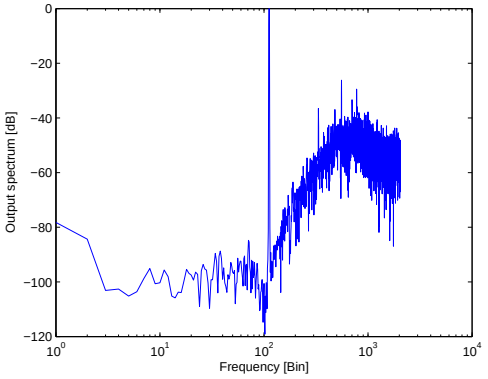
(c) Fin=3.203125 MHz SS corner 80℃



(d) Fin=8.671875 MHz TT corner 25℃



(e) Fin=8.671875 MHz FF corner 80℃



(f) Fin=8.671875 MHz SS corner 0℃

Fig. 5.12 Circuit level simulation of the proposed CTSDM

The summary of Fig. 5.12 is in Table 5.4.

Table 5.4 Summary of the circuit level simulation result

Signal Bandwidth = 10 MHz FFT points = 4096 CLK = 320 MHz					
Fin = 3.203125 MHz			Fin = 8.671875 MHz		
Corner	SNDR	ENOB	Corner	SNDR	ENOB
TT 25°	82.30 dB	13.38	TT 25°	80.72 dB	13.12
FF 0°	83.02 dB	13.50	FF 0°	83.91 dB	13.65
SS 80°	76.53 dB	12.42	SS 80°	75.37 dB	12.23

Fig. 5.13 shows the modulator input (Fin = 8.671875 MHz) and the corresponding output of the third integrator. The output is not overloaded and the system is stable.

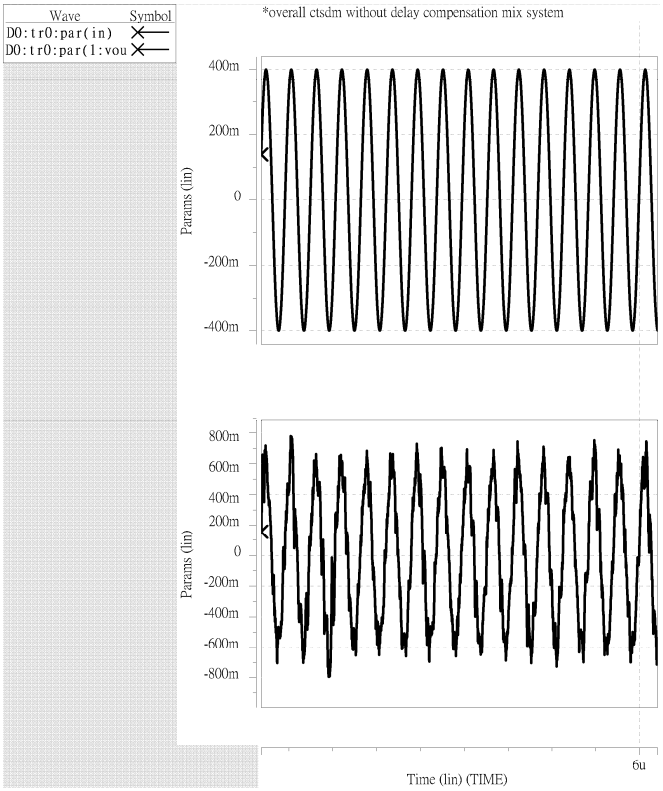


Fig. 5.13 Fully differential input signal and the third integrator output

Fig. 5.14 is the dynamic range (DR) simulation of the proposed CTSDM. The simulated DR is 87 dB, and the peak SNR is 83.25 dB while $|V_{in}/V_{ref}| = -3$ dB.

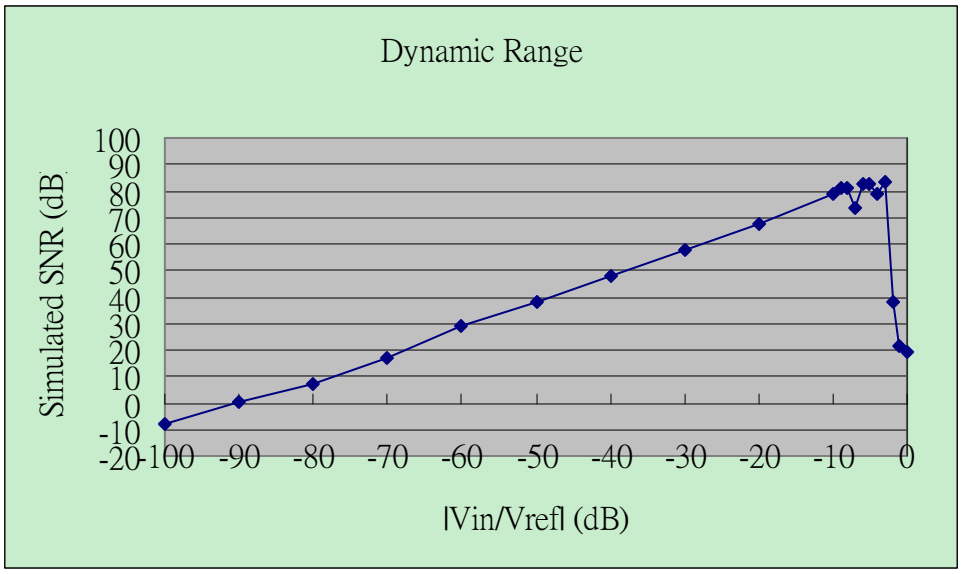


Fig. 5.14 Dynamic range of the proposed CTSDM

5.6 Layout Consideration and Post-layout Simulation

Because CTSDM is essentially a mixed-signal system, many design issues must also be considered in layout level implementation. The modulator contains continuous-time blocks such as loop filter, sampled data blocks such as the quantizer, and purely digital blocks such as latch and encoder. In order to achieve high resolution as well as high linearity, several techniques such as common-centroid layout for current source and capacitors, inter-digitation for transistors, guarding ring and shielding must be used to reduce the performance loss due to mismatch, parasitic and non-linearity.

In loop filter layout, fully symmetrical layout style is employed for the differential signal path. To improve the matching, dummy capacitors are added in MIM capacitor array to make the environments of all unit capacitors the same. Except for the tunable capacitor array to compensate the time constant variation, crossed resistors technique is also employed to reduce the mismatch of the passive device.

In circuit level design, large device size is used to improve the linearity of the current-steering DAC. While in layout level, symmetrical sequence technique [7] is employed to further reduce linear gradient errors. As illustrated in Fig. 5.15, all even-numbered current cells are placed on one side of the array center, while odd-numbered ones are placed on the other side. In the way, linear gradient errors are cancelled by every two cells located symmetrically about the center.

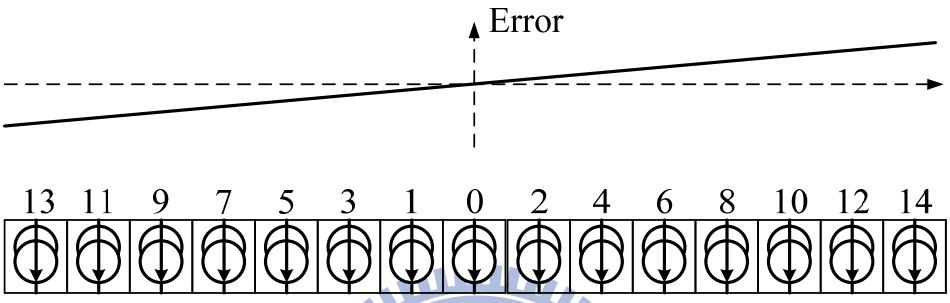


Fig. 5.15 Current-steering DAC layout with symmetrical sequence

The whole chip layout and die photo of the proposed CTSDM is shown in Fig. 5.16.

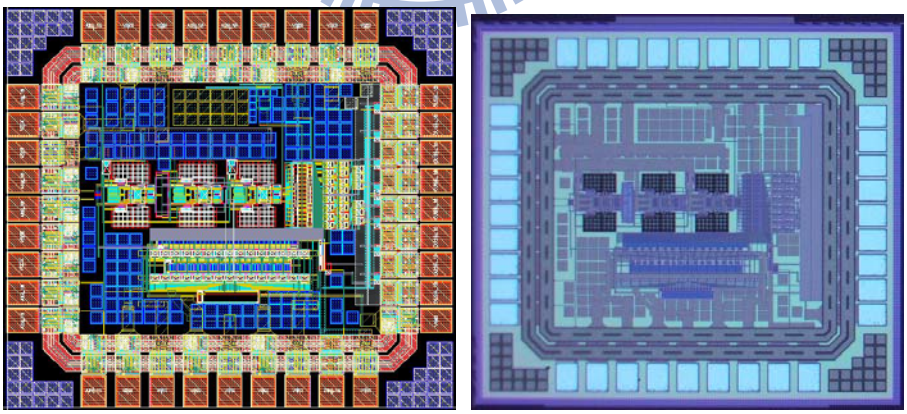
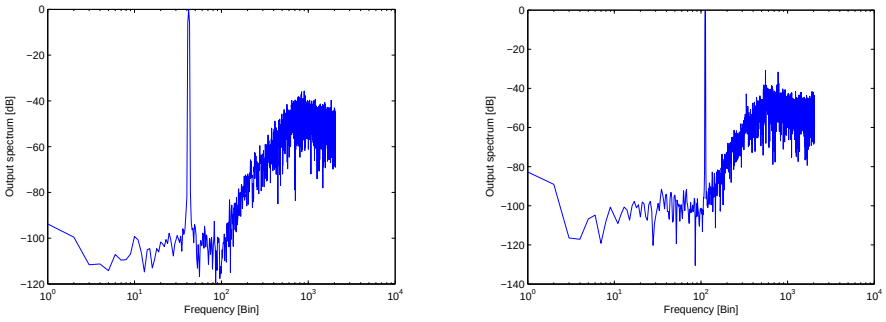


Fig. 5.16 Layout of the proposed CTSDM and chip die photo

The post-layout simulation result is shown as following: Fig. 5.17 is the FFT of the modulator output. The summary of Fig. 5.17 is shown in Table 5.5.



(a) Fin = 3.203125 MHz (b) Fin = 8.671875 MHz

Fig. 5.17 FFT of the post-layout simulation result

Table 5.5 Summary of the post-layout simulation result

Signal Bandwidth = 10 MHz FFT points = 4096 CLK = 320 MHz			
Fin = 3.203125 MHz		Fin = 8.671875 MHz	
SNDR	79.31 dB	SNDR	79.37 dB
ENOB	12.88	ENOB	12.89

The comparison of pre-layout and post-layout simulation is shown in Table 5.6.

Table 5.6 Comparison of the pre-layout and post-layout simulation result

	Pre-sim	Post-sim
Technology	TSMC 0.18 μm	
Supply voltage	1.8 V	
Signal Bandwidth	10 MHz	
Sampling frequency	320 MHz(OSR=16)	
Peak SNR	83.29 dB	80.94 dB
Peak SNDR	81.97 dB	79.31 dB
ENOB	13.32	12.88
Power consumption	36.1 mW	35.5 mW
Chip Area	0.993 × 1.113 mm^2	
Core Area	0.680 × 0.440 mm^2	

The comparison of this work and previous researches are listed in Table 5.4 with figure of merit defined as:

$$FOM = \frac{Power}{(2^{ENOB} \cdot 2 \cdot BW)} (fJ/conversion) \quad (5.7)$$

Table 5.7 Comparison of this work and previous researches

	Tech (um)	VDD (V)	Signal BW(MHz)	OSR	Peak SNR (dB)	SNDR (dB)	ENOB (bit)	Power (mW)	FOM
[1] 2004JSSC	0.5	3.3	1.1	16	84	83	13.50	62	2433
[2] 2004JSSC	0.13	1.5	15	10	64.6	63.7	10.29	65	1731
[3] 2004JSSC	0.18	1.8	20	8	63	N/A	10.17	120	2604
[5] 2006JSSC	0.13	1.2	20	16	76	74	12.00	20	122
[6] 2007TCASI	0.18	1.8	10	32	N/A	66	10.67	7.5	230
[7] 2007JSSC	0.25	2.5	2.5	12	81	80.5	13.08	50	1155
[8] 2007CICC	0.18	1.8	25	8	53	52	8.35	18	1103
[9] 2008ISSC	0.18	1.8	10	32	87	82	13.33	100	486
Pre-sim	**0.18**	**1.8**	**10**	**16**	**83.29**	**81.97**	**13.32**	**36.1**	**177**
Post-sim	**0.18**	**1.8**	**10**	**16**	**80.94**	**79.31**	**12.88**	**35.5**	**235**

From Table 5.7, we can find out that most previous papers only focus on high resolution (SNR>80 dB) or high bandwidth (BW>10 MHz) performance, while the proposed CTSDM achieves ENOB of 12 bits with 10 MHz bandwidth at the same time, and the power consumption is relative low. In FOM comparison, [6] only showed the simulation result and the architecture is simpler (1-bit quantizer). The process of [5] is more advanced than this work and the supply voltage is 1.2V. Take

the process factor into account, we can scale down the FOM of this work according to [28] with FOM'=235*(0.13/0.18)^2=123(fJ/conversion), which is almost the same as [5]. In Table 5.8 and Fig. 5.18, the comparison of CTSD- and pipelined ADC are shown. According to [15], the power consumption of decimator is relatively low compared with modulator in SD-ADC, but significant. We assume the worse case that the power consumption of decimator is the same as modulator. Nonetheless, the achieved FOMs of CTSD-ADC still show better performance compared with pipelined ADC.

Table 5.8 Comparison of CTSD- and pipelined ADC

	Tech (nm)	VDD (V)	Conversion Rate (MHz)	SNDR (dB)	ENOB (bit)	Power (mW)	FOM	FOM_1	FOM_2 (Normalized)
[31] 2004 JSSC	350	3.3	20	70.8	11.47	254	4477	4477	1184
[32] ISSCC	180	1.8	20	74	12	233	2844	2844	2844
[33] 2005 JSSC	180	1.8	20	64.2	10.4	22	814	814	814
[34] 2006 TCASI	350	1.5	20.48	56.0	9.01	19.5	1847	1847	489
[35] 2009 JSSC	350	3.3	20	70.2	11.37	231	4364	4364	1154
[1] 2004 JSSC	500	3.3	2.2	83	13.50	62	2433	4866	631
[5] 2006 JSSC	130	1.2	40	74	12.00	20	122	244	468
[6] 2007 TCASI*	180	1.8	20	66	10.67	7.5	230	460	460
Pre-sim	180	1.8	20	81.97	13.32	36.1	177	354	354
Post-sim	**180**	**1.8**	**20**	**79.31**	**12.88**	**35.5**	**235**	**470**	**470**

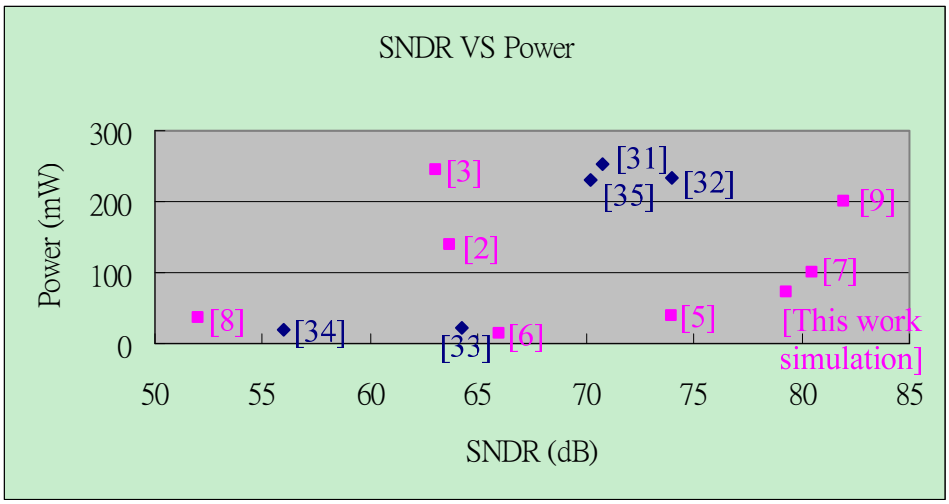


Fig. 5.18 Comparison of CTSD- and pipelined ADC

From the achieved SNR combined with wide bandwidth of the this work, we can conclude that for the high requirements of ADCs in the future, CT ΣΔADCs can be an alternative to Nyquist ADCs to achieve higher performance with lower power consumption.

Chapter 6

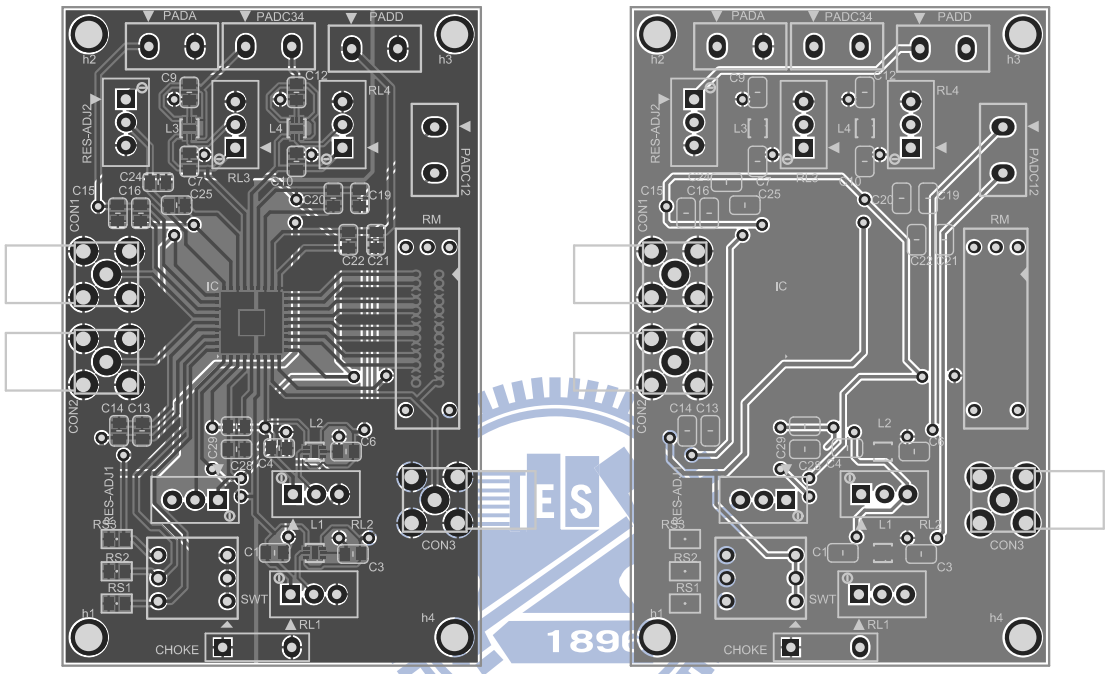
Test Setup and Experimental Results

This chapter describes the test setup and experimental results of the prototype chip. Because of the high speed operation of the proposed CTSDM, the printed circuit board (PCB) for the test chip must be designed carefully. The test environment of this work is also introduced. Finally, the measurement results and discussion are presented.

6.1 Test Board Design

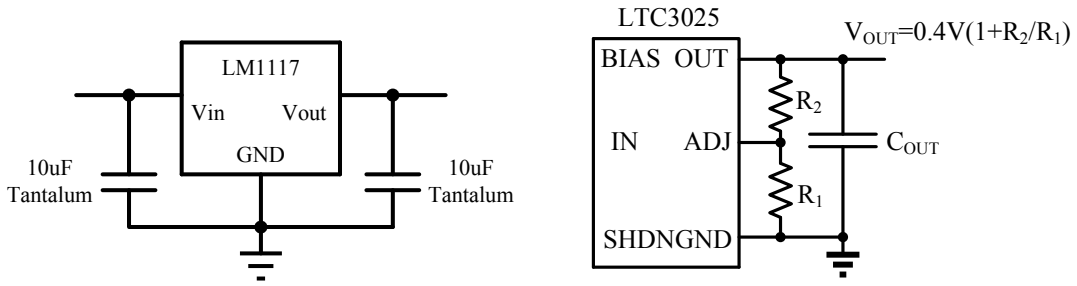
To achieve the expected performance and high speed operation of the prototype chip, the test board must be designed for many considerations. The two-layer PCB for the test chip is shown in Fig. 6.1. The top layer is used to place components such as regulators, variable resistors, capacitors and switch. The bottom layer is the ground plane. To avoid the parasitic effect of the package in high speed operation, the raw die is directly connected to PCB by bonding wires. The analog and digital powers are both provided by LM1117 fixed output regulator combined with battery series as shown in Fig. 6.2(a), and they are isolated into different partition on PCB to prevent the noise in digital circuits coupling to the analog ones through the supply paths. The output of regulator is decoupled by a 10 μF tantalum capacitor for the lower-frequency noise, and high-frequency noise are decoupled by capacitors of 0.1 μF and 0.01μF placed at each supply pin of the prototype chip. In addition to the

supply voltage of 1.8V, the reference voltage for flash ADC and digital supply voltage for DAC latches are provided by LTC3025 VLDO (very low drop-out) linear regulator as shown in Fig. 6.2(b). The power and ground traces are made as short as possible to minimize the wire resistance.



(a) (b)

Fig. 6.1 Top layer and bottom layer of the PCB



(a) (b)

Fig. 6.2 Typical application of LM1117 and LTC3025 regulator

Due to the high speed output data rate, the soft touch connectorless probe combined with retention module on PCB is used to minimize the equivalent load. The differential signal traces are routed symmetrically. The inputs of modulator and clock source are placed as close as possible to the chip. The high frequency digital traces are also as short as possible to reduce electromagnetic interference.

6.2 Test Environment Setup

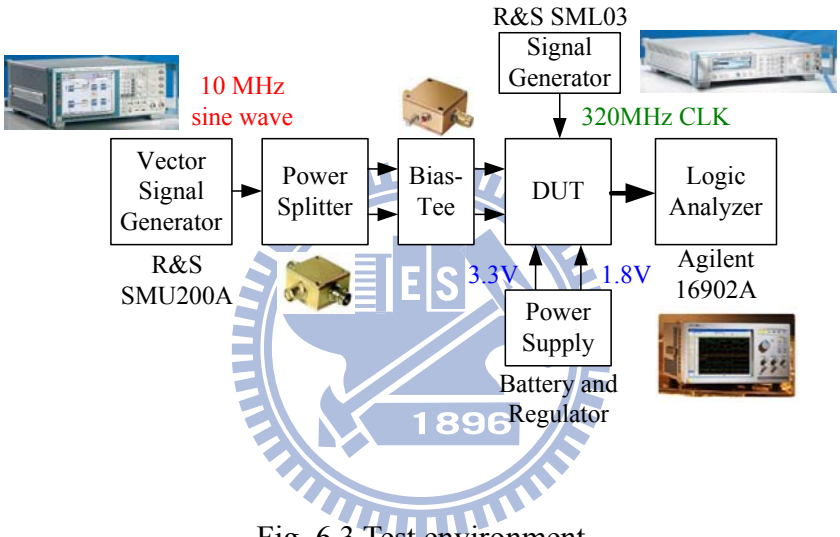
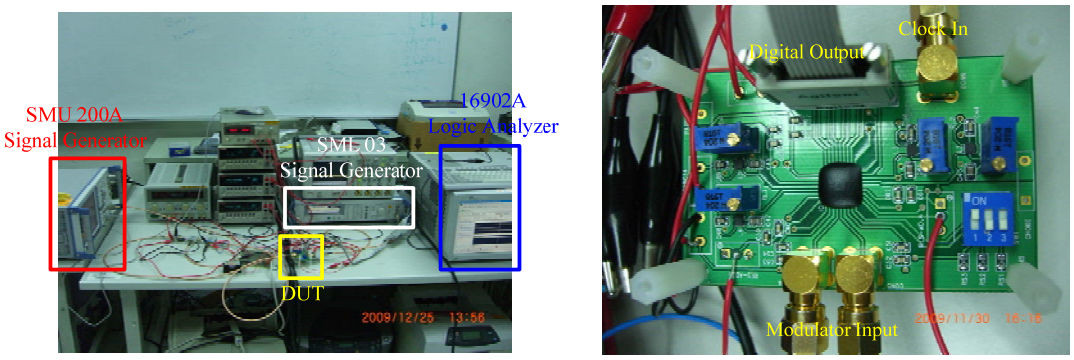


Fig. 6.3 Test environment

Fig. 6.3 is the test environment of the test chip. The input signal and 320 MHz clock of the modulator are generated by Rohde & Schwarz signal generator. The single-ended input signal is transformed into differential on by power splitter and bias-Tee, then it is fed into the chip through SMA connector on PCB. The power supply for the chip core is 1.8V, and the supply voltage of LTC3025 is 3.3V. Both these two powers are provided by LM1117 regulators. The modulator outputs are sampled by Agilent logic analyzer (LA) through retention module on PCB and connetorless probe. The acquired data in LA then transferred to the computer and analyzed by MATLAB. The test environment and PCB photo are shown in Fig. 6.4.



(a) (b)

Fig. 6.4 Test environment and PCB photo

6.3 Measurement Results

6.3.1 The Tuning Mechanism of the Proposed CTSDM

There are two ways to tune the loop filter coefficients in the proposed CTSDM: the tunable capacitor array (TCA) and the feedback current biased by external power supply as shown in Fig. 6.5. As described in Chapter 5, the TCA is controlled by a 3-bit binary code by switch on PCB to change the $C_{in\text{-}use}$ for the modulator. The C_{min} is set to be 0.6pF and C' is 0.1pF for reasonable tuning range. If there is no any process variation for the resistors and capacitors in the continuous-time loop filter, the switch code of "100" should result in the measurement result the same as the simulation one. However, the RC time constant of the practical integrators can vary by as much as more than 30% due to the PVT variation, which will greatly reduce the noise shaping effectiveness and even drive the loop filter unstable [8]. To compensate this large variation, what we can do is to tune the capacitor array and feedback bias current, in other words, to change the undesired loop filter coefficients back to the original one.

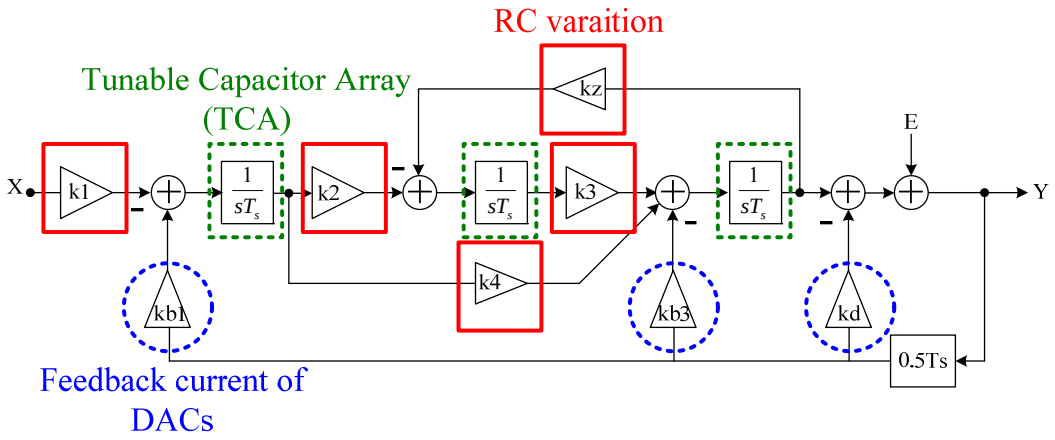


Fig. 6.5 Tuning mechanism of proposed CTSDM

As shown in Fig. 6.5, there are three sets of TCA in proposed CTSDM and they are controlled by the same binary code. In simulation level, the switch code of "100" means that the $C_{in\text{-}use}$ is 1 pF, and the ideal loop filter coefficient (k_i) can be obtained:

$$k_i f_S = \frac{1}{R_i C_i} \Rightarrow k_i = \frac{1}{f_S R_i C_i} \tag{6.1}$$

But in real implementation, the RC time constant will change greatly due to process variation as well as the loop filter coefficients. For example, if the loop filter coefficient in real implementation (k_{ir}) is larger than ideal one, which means that the real RC time constant ($R_{ir}C_{ir}$) is smaller than the ideal one, than we can increase the binary code by one bit to obtain a larger $C_{in\text{-}use}$ as well as $R_{ir}C_{ir}$. Consequently, the real RC time constant is more close to the ideal one and the system becomes more stable. On the other hand, $R_{ir}C_{ir}$ can also be smaller by decreasing the binary code of the switch if the noise shaping effectiveness is worse than ideal one due to the smaller k_{ir}.

Thanks to the TCA mechanism, the proposed CTSDM can also work with lower sampling clock if the measurement results show that the chip can not operate with such a high sampling frequency.

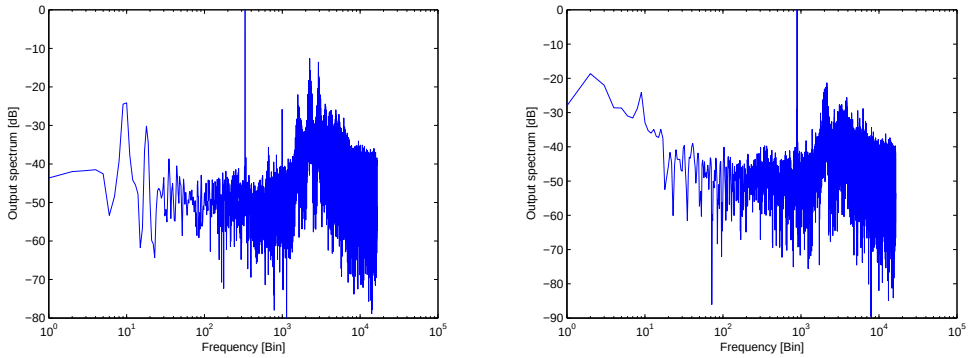
Except for the feed-forward coefficients constructed from the RC time constant, the current produced by feedback DACs represent the feedback coefficients of the loop filter. Any mismatch of feedback and feed-forward coefficients could lead to unstable system. In this work, the three bias current of the DACs are provided by a single variable resistor with external power supply voltage, so the current is tunable. In some case that the TCA can not compensate RC time constant variation effectively, the tuning of feedback current can be another solution. Here, the tuning range of the feedback current is set to be ±50% according to the TCA limitation and the normal operation of the bias circuit.

6.3.2 Measurement Results

Nine chips are test in this work. The test principle of the prototype chip is as following: first, we assume that there is no nay process variation occurred, so the switch code is set to be “100”, resulting in the bias current of feedback DACs is 30 μA. The signal amplitude of modulator input is 110 mV, the same as in simulation. If the modulator output is saturated, which means that the system is unstable, we increase the switch code to decrease the loop filter coefficient as well as more stable condition. Finally, we change the input swing to achieve better performance or more stable operation of the modulator.

The measurement results show that the prototype chip can not work correctly as simulation results. Although in some tuning case that the noise shaping can be observed in output spectrum, the noise floor is still too high, so the expected SNDR can not be achieved. The outputs of modulator are almost all saturated when the bias current of feedback DACs is 30 μA (normal condition) with switch code from “000” to 111, which means that the process variation may be larger than the tuning range we

designed. The 32768-points FFT output spectrums of the measurement results with input frequency of 3 MHz and 8 MHz are shown in Fig. 6.6, and the comparison of measurement and simulation results is shown in Table 6.1.



(a) (b)

Fig. 6.6 Output spectrum of measurement results

Table 6.1 Comparison of measurement and simulation results

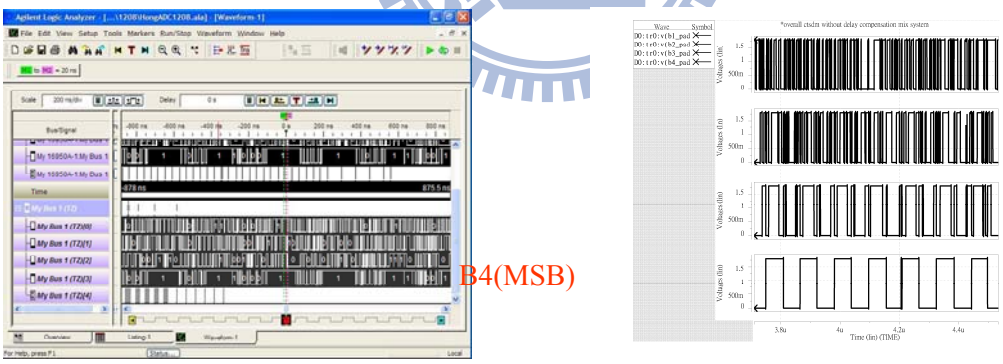
	Pre-sim	Post-sim	Measurement
Technology	TSMC 0.18 μm		
Supply voltage	1.8 V		
Signal Bandwidth	10 MHz		
Sampling frequency	320 MHz(OSR=16)		
Peak SNR	83.29dB	80.94 dB	22.55 dB
Peak SNDR	81.97dB	79.31 dB	22.38 dB
ENOB	13.32	12.88	3.43
Power consumption	36.1mW	35.5 mW	37.17 mW
Layout Area	0.993 x 1.113 mm^2		

According to the measurement compared with simulation results, the possible problems of the prototype chip are discussed in the following.

6.4 Discussion

6.4.1 The Noise Problem

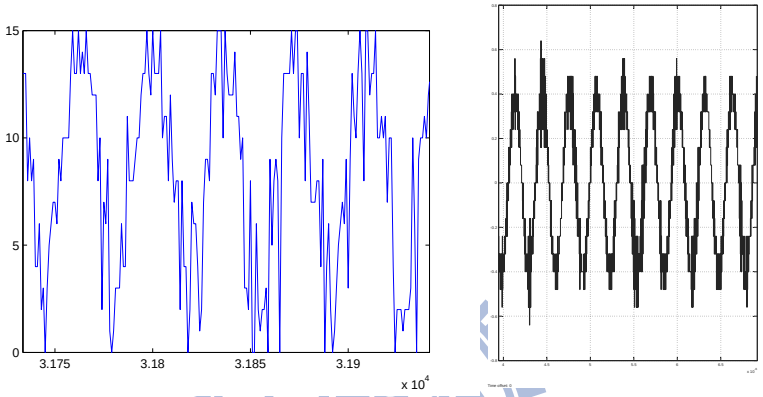
To find out the problems about the incorrect work of the prototype chip, the real waveform of digital output must be checked as well as the supply voltage for the chip powers. The 4-bit digital output can be observed through logic analyzer directly, and we can compare the waveform of these data with ideal simulation results to verify that whether the chip working is correct or not. The unsaturated 4-bit digital output of measurement is shown in Fig. 6.7(a). Compared with the output waveform of simulation in Fig. 6.7(b), it is obvious that there are too many ripples occurred in MSB (B4) of measurement results, hence the noise floor will be very high in output spectrum deservedly.



(a) (b)

Fig. 6.7 Comparison of measurement and simulation output

To ease the observation of the output data, we use MATLAB to transform the 4-bit binary code back to the corresponding analog waveform (Fig. 6.8(a)) and compare it with the ideal one in simulink simulation (Fig. 6.8(b)). As shown in Fig. 6.8(a), although it seems that the continuous-time integrators inside the chip can work and the output of the third integrator of the modulator are converted to 4-bit binary code successfully, the ripples are still too high compared with the ideal output.



(a) (b)

Fig. 6.8 Comparison of measurement and simulation output in MATLAB

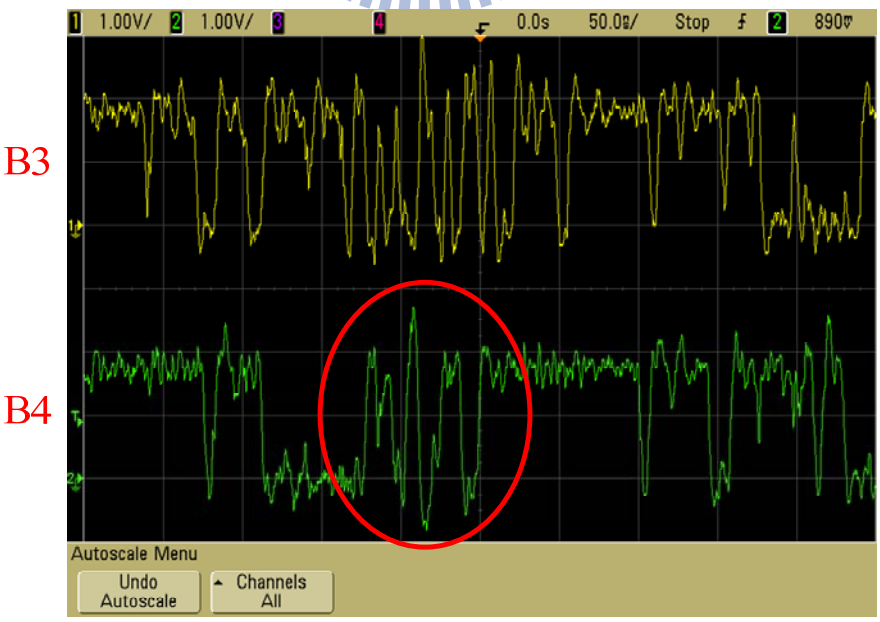


Fig. 6.9 Output waveform of digital output in oscilloscope

Moreover, by observing the waveform of the digital output on PCB through oscilloscope, as shown in Fig. 6.9, we can find out that the undesired logic 1 of MSB are also occurred. Because the waveform in oscilloscope represents the output from the chip on PCB directly, the noise problem is indeed caused by the chip itself.

As shown in Fig. 6.9, except for the large noise occurred while the digital output must be logic 0, the threshold uncertainty of logic 1 is also very large. The possible reason for this large spike is the power line noise. To check the transient response of the dc supply voltage, we use oscilloscope to observe the real waveform of the supply voltage on PCB pins similarly. As shown in Fig. 6.10, the power line noise in digital powers is very large. The amplitude of the noise is about 50 mV, and the frequency is about 320 MHz, which is the same as the sampling frequency for the chip. Due to the coupling effect, other supply voltage such as analog powers and reference voltage for internal ADC are also not clean. From the observing in oscilloscope, the amplitude of other power lines noise is almost the same. This high speed power line noise will degrade the modulator performance and even make the system unstable.

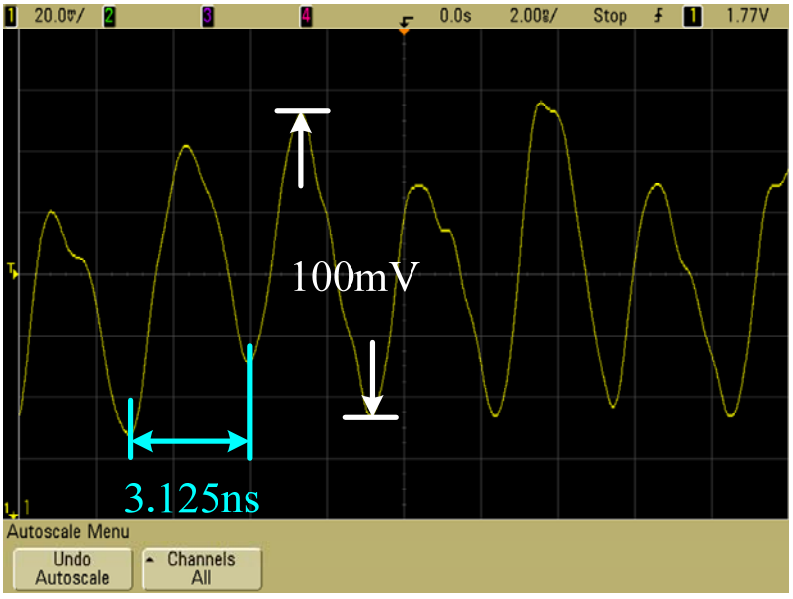


Fig. 6.10 Output waveform of digital supply voltage in oscilloscope

The cause of the power line noise and the effect resulted form these large noise are discussed as following.

6.4.2 RC Variation Consideration

The large ripples discussed in 6.4.1 can be caused by two reasons: incorrect operation of internal modulator and high speed noise coupled by power line of the output digital circuits. From the measurement results discussed in 6.3.2, we suspect that the process variation is larger than the tuning range we designed, so the original loop filter coefficients can not be obtained to achieve the ideal noise shaping effect and the modulator can not work correctly. In MATLAB, the time constant error due to the process variation can be modeled as a gain error of the integrator. By simulink model simulation, we can find out the range that the proposed CTSDM suffered from RC variation can still work correctly with TCA compensation. Here, the trend of RC variation for all integrators is set to be the same. As described in Eq. 6.1, the ideal coefficients are named by k_i. Taking the RC variation into account, the real coefficients k_{ir} are different form the ideal ones, and we can represent k_{ir} combined with k_i and a variation term, Δ_{RC}, as shown in Eq. 6.2. Finally, the TCA compensation is also considered, and the effectiveness of the compensation is denoted by Δ_{TCA}. The overall equivalent loop filter coefficients are represented by k'_{ir}, and the equation covering RC variation and TCA compensation is shown as Eq. 6.3.

$$k_{ir} = \frac{1}{f_S R_{ir} C_{ir}} = \frac{1}{f_S R_i C_i (1+\Delta_{RC})} \tag{6.2}$$

$$k'_{ir} = \frac{1}{f_S R_{ir} C'_{ir}} = \frac{1}{f_S R_i C_i (1+\Delta_{RC})(1+\Delta_{TCA})} \tag{6.3}$$

To find out the optimum tuning range for TCA, both Δ_{RC} and Δ_{TCA} are set to be in the range between -50% to +50%. The summary of MATLAB simulation results are listed in Table 6.2.

Δ_{RC} \ Δ_{TCA}	-50%	-40%	-30%	-20%	-10%	0%	+10%	+20%	+30%	+40%	+50%
-50%	X	X	X	X	X	X	X	X	X	O	O
-40%	X	X	X	X	X	X	X	X	O	O	O
-30%	X	X	X	X	X	O	O	O	O	O	O
-20%	X	X	X	X	O	O	O	O	O	O	X
-10%	X	X	X	O	O	O	O	O	O	X	X
0%	X	X	X	O	O	O	O	O	O	X	X
+10%	X	X	X	O	O	O	O	O	X	X	X
+20%	X	X	O	O	O	O	O	X	X	X	X
+30%	X	X	O	O	O	O	O	X	X	X	X
+40%	X	X	O	O	O	O	O	X	X	X	X
+50%	X	X	O	O	O	O	X	X	X	X	X

Tuning range of this work

Resistor variation according to TSMC model

Table 6.2 Summary of MATLAB simulation results with RC variation and TCA

Compared with MATLAB simulation, the proposed tuning range is indeed sufficient to cover the RC variation in TSMC process.

6.4.3 Power Supply Noise Effect

Due to the high speed operation of the digital circuits, the coupling effect must be considered. From RC-extraction of layout, the coupling capacitors between different power line buses can be found. As shown in Fig. 6.11, although the noise coupled by DVDD2 (digital powers) crossed over VREF1 and VREF2 can not be observed in post-layout simulation, the real coupling effect can be calculated and verify by adding this noise to spice simulation.

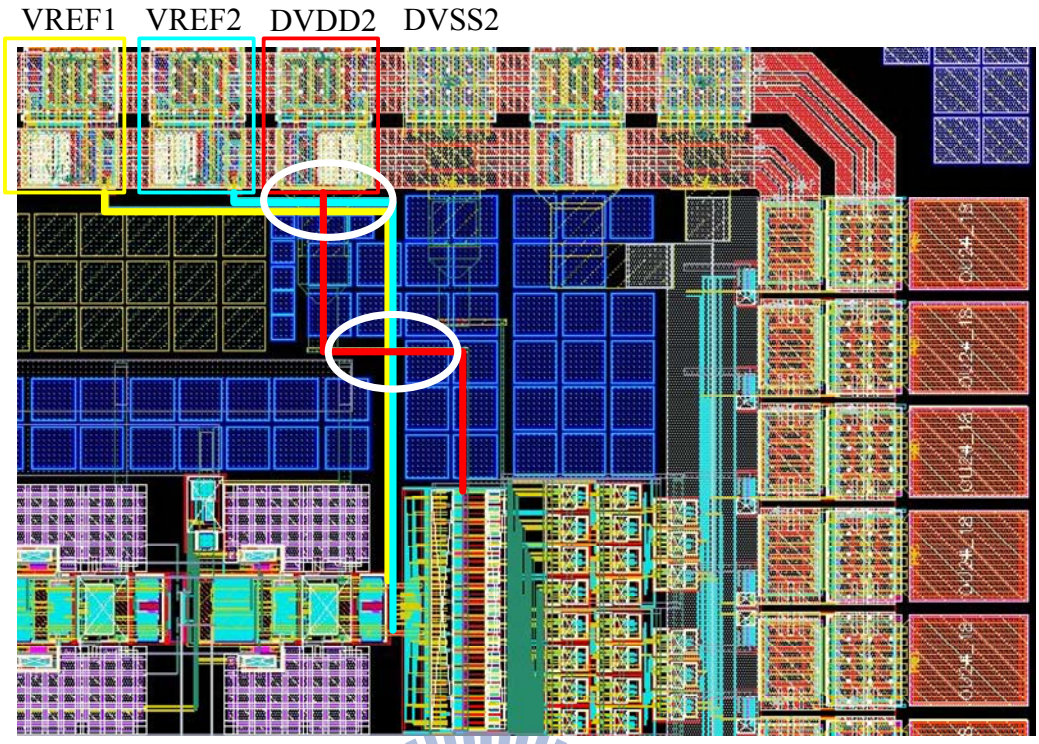
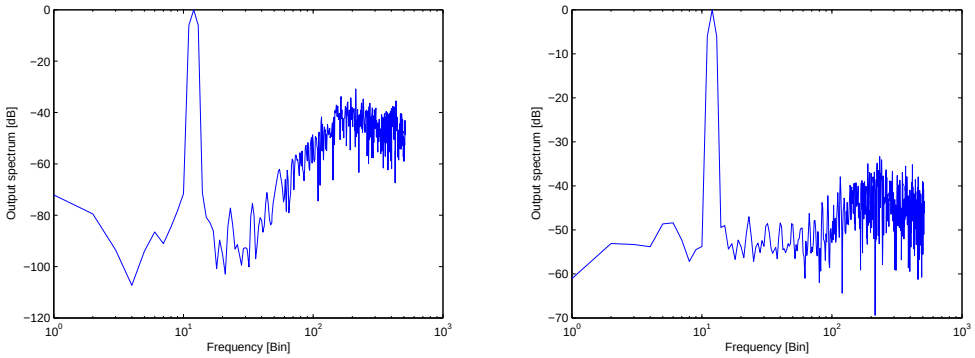


Fig. 6.11 Crossed over power line buses

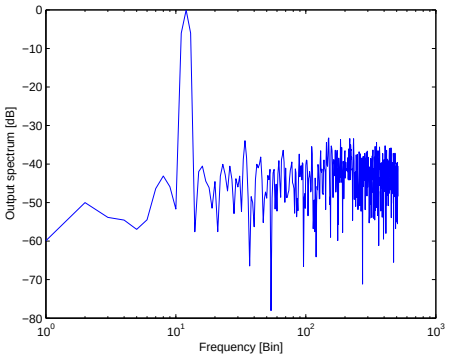
For example, the coupling capacitors (Cc) between DVDD2 and VREF1, VREF2 are 3.2 fF and 4.3 fF, respectively, while Cc between ground and VREF1, VREF2 are 0.7 fF and 0.8 fF. Assume the noise source coupled by DVDD2 is a small signal of 320 MHz frequency and 50 mV amplitude, the noise coupled to VREF1 and VREF2 can be calculated:

$$V_{Ni} = V_N(t) \times \frac{\text{Cc}}{\text{Cc} + \text{Cc}_{\text{GND}}}, V_N(t) = 50 \times 10^{-3} \sin(2\pi f_S t)$$
$$\Rightarrow V_{N1} \approx 41 \times 10^{-3} \sin(2\pi f_S t) \quad V_{N2} \approx 43 \times 10^{-3} \sin(2\pi f_S t) \tag{6.4}$$

The order of the noise amplitude is almost the same between calculation and real waveform observed in oscilloscope. The other noise coupled by DVDD2 can also be calculated in the same way. In spice simulation, we set all the noise source amplitude is the same as that of DVDD2, and the coupled effect can be observed directly.



(a) (b)



(c)

Fig. 6.12 Hspice simulation results of coupling noise effect

In pre-layout simulation, although the small signal noise is added to every power supply voltage source, the output spectrum is almost the same as the one without any noise. But in post-layout simulation which considering all the parasitic and coupling capacitors, the influence due to the large noise in power line is obvious. Fig. 6.12 is the 1024-points FFT output spectrum of post-layout simulation results with coupling noise effect. In Fig. 6.12(a), there is no any coupling noise in power lines, and the achieved SNDR is more than 74 dB (ENOB>12 bits). In Fig. 6.12(b), the digital power and reference voltage of flash ADC are added by a noise small signal source, while the noise floor of output spectrum raise largely, resulting in the degraded SNDR

of 38.54 dB (6.11 ENOB). In Fig. 6.12(c), all the power supply voltage are added with a small signal noise, and the achieved ENOB is only 4.25 bits. The noise floor (~-40dB) in Fig. 6.12(c) is almost the same as that of measurement results. From the simulation result with coupling noise, the reason why the prototype chip can not work correctly can be explained. Because of the high speed noise coupled by digital power line bus, not only the analog block can not work correctly, due to the variation of the reference voltage, the internal flash ADC can not convert the analog output of the third integrator to digital code precisely, and the linearity of feedback DAC is also decreased. Thus, the modulator becomes unstable and the SNDR degrade quickly.

6.4.4 Summary of the Problems of Proposed CTSDM

From the aforementioned discussion, the main problems of the proposed CTSDM are summarized as following:

Tuning Range Limitation

- Compared with measurement and MATLAB simulation, the proposed tuning range is sufficient to cover the RC variation in real implementation.

High speed power line coupling issue

- By observing the output data in oscilloscope, the threshold uncertainty due to noise coupled by power line and RC variation is very large.

- From spice simulation with power line noise source, the reason why the performance of the chip degrades largely can be explained.

- To ensure that the noise will not couple to each other, the power line of high speed digital circuits must be separated and shield from each other.

- Long power line bus must be avoid for high speed circuits to prevent the core blocks from voltage drops and coupled noise.

6.4.5 Discussion: FOM Improvement Can Be More

From Table 5.8, we find out that the FOM improvement from replacing NGCC opamp in [5] with two-stage topology is not obvious. The reason is the conservative design of proposed CTSDM in different integrator stages. In fact, the speed requirement of opamps can be scaled down for relaxed noise requirement of integrator stages. From MATLAB and pre-layout simulation, the SNDR loss is negligible with scaled GBW specifications in different opamp stages: $GBW_2=GBW_3=0.8GBW_1$. Thus, the power consumption of whole CTSDM can be saved by 10%, and the resulting FOM can be reduced to: 470*0.9=423 (fJ/conversion), which is the lowest one in Table 5.8.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

The proposed high-bandwidth low-power CTSDM implemented in 180 nm CMOS consumes 36 mW power dissipation and achieves a SNDR above 74 dB (ENOB>12) over 10 MHz signal bandwidth. Combined with adequate loop filter architecture and intrinsically high linearity DACs, the high speed operation is achieved. The sufficient speed and gain requirements of opamp are found by MATLAB analysis and achieved by two-stage topology, which is much simpler designed and consumes less power compared with NGCC architecture. The achieved SNR, high-bandwidth and its anti-alias performance promotes CT sigma-delta ADCs as alternative to Nyquist ADCs in deep-submicron CMOS technologies. The design is suitable for low-power wireless communications and medical imaging requirements.

7.2 Future Work

To ensure that the noise will not couple to each other, the power line of high speed digital circuits must be separated and shielded from each other. More guard ring must be used in power-sensitive blocks. Clock bus must be separated far away from other sensitive blocks and shielded. The power consumption of whole modulator can be saved more by scaling down the opamp requirements in different integrator stages. In addition, more low power technique can be utilized to achieve more power-efficient performance.

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