The Electrical Characteristics of the Amorphous Silicon Thin Film Transistors with Dual Intrinsic Layers

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ABSTRACT

The amorphous silicon thin film transistors (a-Si:H TFTs) with dual intrinsic layers, namely, a bottom a-Si:H deposited at a low deposition rate and an upper layer at a high deposition rate, were investigated to improve the manufacturing throughput. It was found that the high deposition rate for the upper layer resulted in high density of states and low mobility and high threshold voltage. Although a-Si:H TFTs with high deposition rates for the upper layer still had an I_{on}/I_{off} ratios higher than 10^6 and saturation mobility higher than 0.4 cm^2/V s, the deposition rates of 1786 and 3340 Å/min exhibited a significant current crowding and led to low mobility and on-current in the linear region. On the other hand, a-Si:H TFTs with deposition rate of 1170 Å/min for the upper layer achieved similar characteristics as those with single layer deposited at deposition rate of 482 Å/min. Furthermore, the stress stability for deposition rate of 1170 Å/min also showed a threshold voltage shift similar to that of a single-layer one. This indicated that the deposition rate of the upper layer for dual-layer a-Si:H TFTs must be properly chosen for applications in high resolution LCDs.

Introduction

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) have been widely studied for their practical applications, such as active matrix liquid crystal displays (AMLCDs) and image sensors.[1] In particular, high-performance TFTs will have an application in high-pixel-density LCDs,[2] such as for use in engineering workstations and high-definition television (HDTV).

In general, there are two types of popular structures of inverted staggered a-Si TFTs made by mass production manufacturers. One is the etched-stop structure, another is the back-channel-etched structure.[3] The major differences in these two types are the production process and the thickness of an intrinsic a-Si:H film. In the etched-stop type, there is a consecutive deposition of a gate nitride, an intrinsic a-Si:H, and then a second silicon nitride layer. The top nitride is then etched from the source/drain contact regions, before depositing the n^+ layer. The total process, including the indium-tin oxide (ITO) layer and passivation layer needs a six or more layer mask. In the back-channel-etched type, there is a consecutive deposition of a gate nitride, an intrinsic a-Si:H, and n^+ a-Si in a single growth step. The n^+ a-Si is then etched from the channel region of the transistor. The total process needs only a five-layer mask but a thicker intrinsic a-Si film is necessary. Owing to the cost-cutting demand for most display manufactures, the back-channel-etched type is relatively favorable. However, the required thicker intrinsic a-Si:H layer will encounter a challenge in the manufacturing throughput.

Therefore, in order to improve such a throughput problem, the double amorphous silicon layer of TFT was proposed. The TFTs with a dual-layer a-Si:H film, a bottom a-Si:H deposited at a low power to obtain a high quality interface layer and an upper layer deposited, named at a high power to attain the thick bulk layer, were fabricated. The deposition temperature of dual-layer a-Si:H and gate-SiN_x was kept at a constant temperature of 300°C.

The dual-layer a-Si:H TFTs were proposed by Takeuchi *et al.*[4] and Kuo.[5] Takeuchi *et al.* reported that ultrathin a-Si:H TFTs in which a 1 nm thick layer of a-Si:H deposited at 20°C followed by a 14 nm thick bulk layer deposited at 250°C exhibited a mobility two times higher than that of single-layer TFTs with the same a-Si:H thickness.[4] The throughput of this process was influenced by different deposition temperature of dual layer. Kuo reported that a deposited multilayered thin a-Si:H film of TFTs with etched-stop type affected the quality of the a-Si:H/gate SiN_x interface due to the plasma radiation damage from the high power deposition of the second a-Si:H layer. They reported that thin-multilayer a-Si:H TFT characteristics were better than a conventional single-layer a-Si:H TFT. However, the stress stability of the dual-layer a-Si:H TFT and the thicker dual-layer a-Si:H TFTs with the back channel etched structure were still not investigated. Therefore, in this paper, the dual-layer a-Si:H TFTs with back-channel-etched structure were manufactured, due to the merits as mentioned above. The effects of the deposition rate of the dual intrinsic a-Si layers were systematically investigated with respect to the single-layer a-Si TFTs deposited only with low power. Furthermore, the stability of single-layer and dual-layer a-Si:H TFTs under various bias stresses were also performed and discussed. Consequently, the a-Si:H TFTs with the optimum deposition rate of upper layer can achieve not only the manufacturing throughput but also the stability of the single-layer a-Si:H TFTs.

Experimental

The a-Si:H TFTs employed in this study have a back-channel-etched type inverted staggered structure, as shown in Fig. 1. After depositing and patterning of the chromium gate metal on the Corning 7059 glass sub-

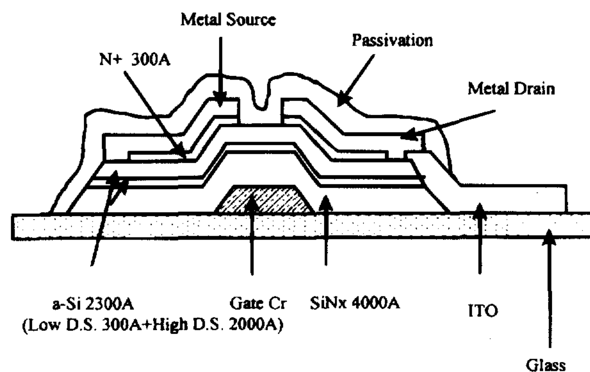

Fig. 1. A cross-sectional view of the a-Si:H TFTs with dual-layer intrinsic a-Si:H.

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strates, four layers, *i.e.*, 400 nm thick SiN_x, 30 nm thick low deposition rate a-Si:H, 200 nm thick high deposition rate a-Si:H, and 30 nm thick n^+ a-Si:H film, were deposited successively in a 13.56 MHz multichamber plasma enhanced chemical vapor deposition (PECVD) system. The flow rate ratio of NH_3 to SiH_4 was 9, resulting in a 1.84 refractive index for the gate SiN_x. For systematically investigating the electrical characteristics of the TFTs with dual intrinsic a-Si layers, the a-Si:H films were deposited with different deposition rates by changing the power density, pressure, and flow rate. Table I lists the deposition conditions of a-Si:H films with various deposition rates. The bottom layer, with a deposition rate of 482 A/min and the upper layer, with a deposition rate of 1170, 1786, or 3340 A/min were investigated. After patterning the Cr/Al source/drain electrodes, the exposed n^+ a-Si:H was removed by reactive ion etching. The channel length and width of the TFTs were 8 and 32 μm, respectively. A passivation layer was then deposited to protect the channel region. The bias stress measurements at room temperature were performed for up to 10^3 s using an HP 4156A semiconductor parameter analyzer interrupted at preselected times to measure the transfer characteristics at the drain voltage of 1 V. The threshold voltage was determined from the intercept of the transfer curves plotted on a linear scale. During the stresses, the source and drain electrodes of the TFTs were commonly grounded. To restore the initial transfer characteristics,[6-9] a-Si:H TFTs were annealed at 180°C for 30 min before each bias stress measurement. The density of states in the bulk of a-Si films with various deposition rates were measured by isothermal capacitance transient spectroscopy (ICTS).[10,11]

Results and Discussion

Figure 2 shows the transfer characteristics of the a-Si TFTs with different deposition rates of upper layers, all reflecting the I_{on}/I_{off} ratios greater than 10^6. However, they possess different threshold voltages, as shown in Fig. 3. The saturation mobility (V_d = 10 V) and liner mobility (V_d = 0.5 V) of various dual-layer a-Si TFTs are shown in Fig. 4. When the upper a-Si layer deposition rate increasing, the threshold voltage increases and the mobility decreases. It can be explained from Fig. 5, in which the bulk density of state distribution ($g(E)$) is a function of the deposition rate of upper a-Si:H films. The density of states of bulk a-Si:H film are proportional to the deposition rate, especially, much high density of states for the 3340 Å/min deposition rate. Obviously, the higher the deposition rate of upper layer, the higher the density of states. The density of states of the bulk a-Si:H film is closely related to its dangling bonds, which exist in positively, negatively, and neutral charged states.[12] Therefore, the high density of states of the bulk a-Si:H films will have a low mobility of TFTs. In Fig. 5, the position of characteristic energy E_p[11] is different for various upper-layer deposition rates. The high deposition rate of upper layer possesses the E_p position far below the conduction band E_c and toward the midgap. Thus, the high bulk density of states near the midgap effectively pins the Fermi level position to far below the conduction band[13] and yields a high threshold voltage. On the other hand, the transfer characteristics for various deposition rates of upper layer, all have an I_{on}/I_{off} ratio higher than 10^6 and saturation mobility is higher than 0.4 cm^2/V s. However, the linear mobility shown in

Table I. The deposition conditions of a-Si:H films with various deposition rates.

Deposition rate	Power density (W/cm^2)	Pressure (Torr)	SiH_4 Flow rate (sccm)	Temperature (°C)
482 Å/min	0.06	1.1	200	300
1170 Å/min	0.2	1.3	400	300
1786 Å/min	0.4	1.3	800	300
3340 Å/min	0.75	1.3	1500	300

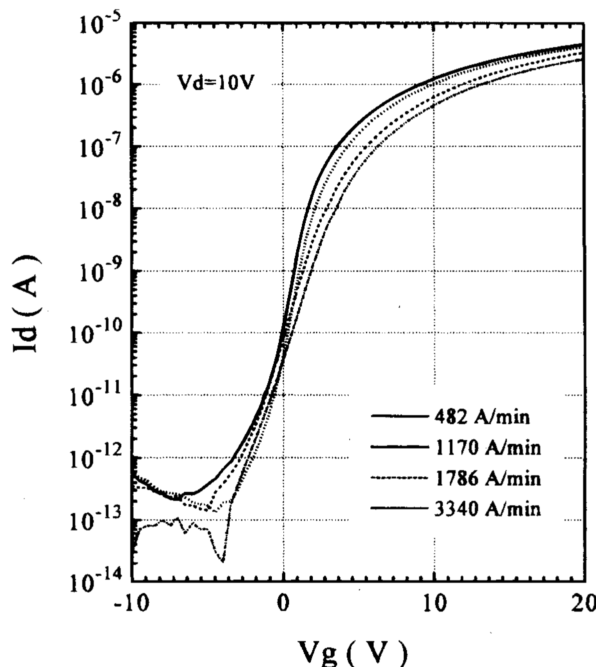

Fig. 2. Transfer characteristics of dual-layer a-Si:H TFTs with various deposition rates for the upper layer at V_d = 10 V.

Fig. 4 rapidly decreased compared to saturation mobility as the deposition rate of the upper layer increased. This indicates that the Fermi level in the subthreshold[9,14] is near the midgap and the a-Si:H film with high deposition rates possesses a high density of states near the midgap, therefore reflecting significantly degraded linear mobility.

In the active matrix liquid crystal displays, the TFT operates in the linear regime so that $V_g - V_{th} > V_d$. Therefore, it is important that an adequate "on-current" is maintained for low source-drain voltages, to enable full charging of the liquid crystal pixel to the voltage of the data signal. On the other hand, due to the pixel resolution increasing from VGA (640 × 480) and SVGA (800 × 600) to XGA (1024 × 768) and SXGA (1280 × 1024), the time of every scan-line is shortened gradually (typically, at 60 Hz frame frequency, 35 μs for VGA, and 16.4 μs for SXGA). During each gate pulse (the time of every scan-line), the TFTs must charge fully the pixel capacitance (which often includes an additional storage capacitance parallel to the

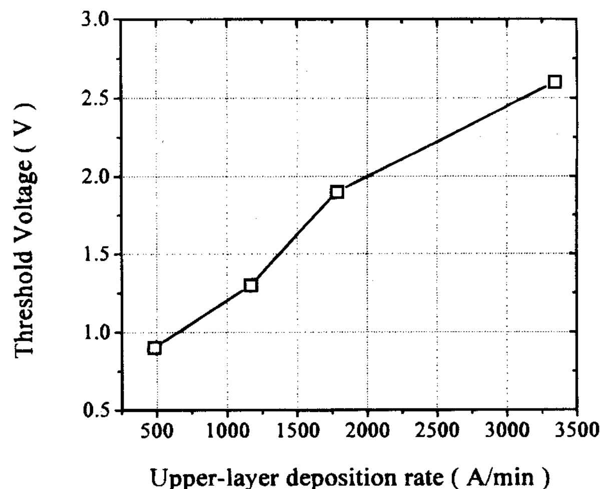

Fig. 3. The threshold voltage of dual-layer a-Si:H TFTs as a function of the deposition rate for the upper layer.

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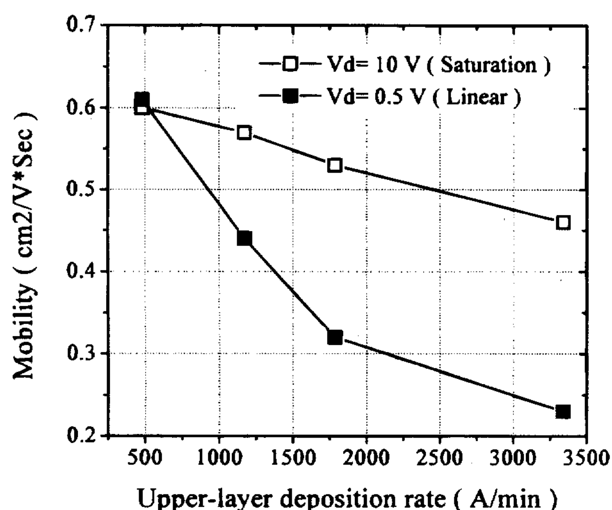

Fig. 4. The saturation mobility and linear mobility of dual-layer a-Si:H TFTs with the upper layer at different deposition rates.

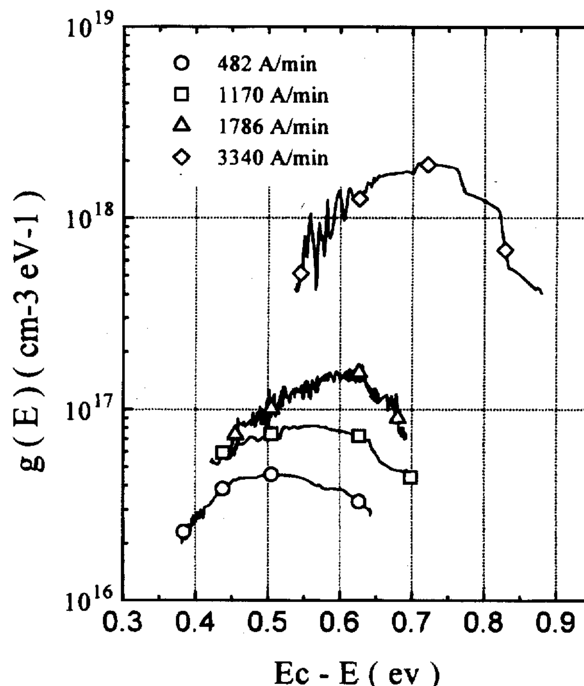

Fig. 5. The density-of-state distribution $g(E)$ for the a-Si:H films with various deposition rates.

pixel capacitance for better charge retention).[14] Therefore, not only the on-current is required to be high enough to charge the pixel capacitance, but also the linear mobility must be high enough to get the charge-on during each gate pulse time. As mentioned above, the characteristics of a-Si:H TFTs in the linear region are very important for application in high-resolution LCDs, so the characteristics of a-Si:H TFTs in the linear region are investigated further. Figure 6 is the output characteristics of the a-Si TFTs with different deposition rates for the upper layer. The high deposition rates of 1786 and 3340 Å/min result in a low I_{on} (Fig. 6c and d) and current crowding (a source-drain current which increases slowly with increasing V_g such that the output characteristics for different V_g appear to crowd together[15]). This current crowding will deteriorate the performance of amorphous silicon thin film transistors because the current crowding will cause a degradation of the electron characteristics, especially in the linear region. It is obvious that the on-current and mobility in the linear region is decreased with increasing deposition rate of upper layer as shown in Fig. 7. This on-current is a space charge limited current whose magnitude depends on the quality of the intrinsic a-Si:H layer.[12,16] The a-Si:H TFTs with a high density of bulk defects result a low linear mobility and on-current which will limit the resolution of a-Si TFT LCDs. From the Fig. 6a and b, only the deposition rate of upper layer with 1170 Å/min has little current crowding. Hence, the dual layer with the deposition rate of 1170 Å/min can be applied in the larger size and

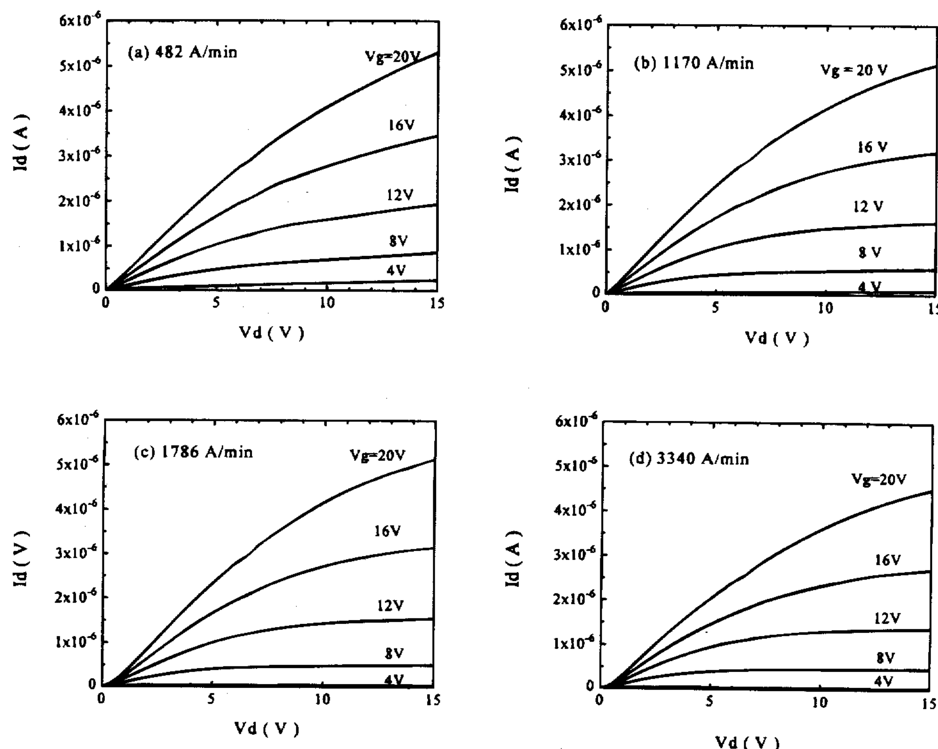

Fig. 6. The output characteristics of dual-layer a-Si:H TFTs for the upper layers with various deposition rates (a) 482 Å/min, (b) 1170 Å/min, (c) 1786 Å/min, and (d) 3340 Å/min.

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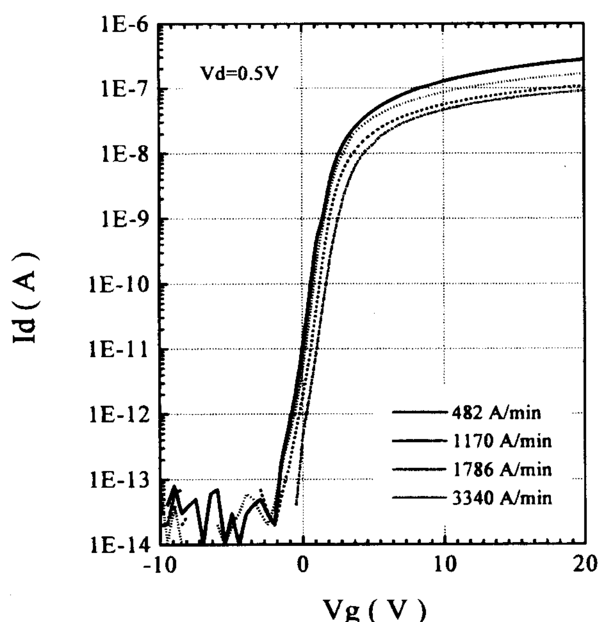

Fig. 7. The linear transfer characteristics of dual-layer a-Si:H TFTs for the upper layers with various deposition rates.

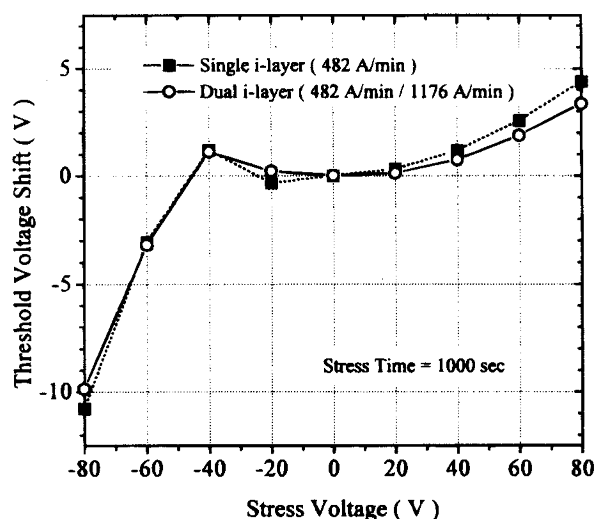

Fig. 8. The threshold voltage shift as a function of stress voltage for the dual-layer a-Si:H TFTs and single-layer a-Si:H TFTs.

higher resolution a-Si:H TFT LCDs. Furthermore, the stress stability of the dual layer with the deposition rate of 1170 Å/min was investigated. Figure 8 shows the stress stability of the dual-layer a-Si:H TFTs with the deposition rate of 1170 Å/min and conventional single a-Si:H layer. The threshold voltage shifts of dual-layer a-Si:H TFTs with the deposition rate 1170 Å/min as compared with the single layer (230 nm thick a-Si:H film with deposition rate of 482 Å/min) exhibit similar profiles at the positive gate bias stress (~20 to 80V). On the other hand, for the negative bias stress voltage from −20 to −80 V, the curves of the threshold voltage shift *vs.* the stress voltage for the single-layer and dual-layer TFTs have a similar trend. According to the report of Powell *et al.*,[13] the density of states in the bulk of the ith layer is found to be significantly less than that near the gate-insulator interface. Although the upper layer of dual-layer a-Si:H TFTs with the deposition rate of 1170 Å/min for upper layer has higher density of states than the single-layer a-Si:H TFTs, they possess the same insulator and interface of a-Si:H/gate-SiN_x since they have the same process for a bottom layer and SiN_x films. Therefore, they possess a similar interfacial structure of a-Si:H/gate-SiN_x, resulting in a similar stress stability.

Conclusions

The effect of the deposition rate on dual-layer a-Si:H TFTs was systematically investigated. It was found that the high deposition rate of upper layer resulted in high density of states. The high deposition rate of upper layer possesses an E_p position far below the conduction band E_c and toward the midgap, thus reducing the linear mobility and increasing the threshold voltage. The deposition rates of 1786 and 3340 Å/min for the upper layer led to low linear mobility and significant crowding, which degraded the contrast and the resolution of the display. On the other hand, the deposition rate of 1170 Å/min for the upper layer achieves similar characteristics as the single layer deposited with a persistent rate of 482 Å/min. In addition, the stress stability of the dual layer with the deposition rate of 1170 Å/min for the upper layer also showed similar results to the single-layer TFTs. This indicated that the dual-layer a-Si:H TFTs can improve the manufacturing throughput and return good performance only when the deposition rate for the upper layer is properly chosen.

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