


國立交通大學

電子工程學系電子研究所

博士論文

具自回授之比例記憶細胞式非線性網路  
設計與分析及其在聯想記憶之應用



THE DESIGN AND ANALYSIS OF THE  
SELF-FEEDBACK RATIO-MEMORY  
CELLULAR NONLINEAR NETWORKS AND  
THEIR APPLICATIONS IN ASSOCIATIVE  
MEMORIES

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中華民國九十三年七月

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# 具自回授之比例記憶細胞式非線性網路 設計與分析及其在聯想記憶之應用

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## 摘要

本論文的主旨在於闡述類比自回授比例記憶細胞式非線性網路架構配合修正之 Habbian 演算法在聯想記憶應用之分析與設計。本論文由三個主要部分所組成：(1)自回授比例記憶細胞式非線性網路架構應用於類比聯想記憶之分析與設計；(2)具 B 或(A 和 B)樣板之 SRMCNN 於異聯想記憶應用的設計；(3) 18x18 SRMCNN 的超大型積體電路設計及大鄰近層細胞式非線性網路泛用機器之概念設計。

首先，本論文藉由探討一個被稱為 RMCNN 之比例記憶可學習細胞式非線性網路的超大型積體電路神經網路之硬體實現設計，並正確地驗正它的功能；接著提出並分析一個自回授比例記憶細胞式非線性網路架構(SRMCNN)配合修正之 Habbian 演算法。在這比例記憶細胞式非線性網路中，自回授權重值被導入樣板 A 中。SRMCNN 如同聯想記憶般產生絕對權重值，再轉換為比例權重值於 A 樣板中，網路能夠儲存圖案樣本並辨識具有雜訊之測試圖案。從模擬的結果得知，自回授比例記憶細胞式非線性網路中之樣板權重值經學習及固定時間漏電後，對權重值做比例處理，網路具有增強樣本特徵的學習能力，SRMCNN 比 RMCNN 可儲存與辨識更多之圖案。對於 18x18 之 SRMCNN 能成功地學習、儲存及辨識 93 個具雜訊之圖案，雜訊之均勻分佈準位為 0.8 或常態分佈變動量為 0.3。SRMCNN 對較單純或雜訊較低之圖案具有較好之學習及辨識能力；反之，可允許處理之圖案數目會降低。模擬的結果成功地印證 SRMCNN 在圖案辨識上有正確地功能及良好地效能。在高整合力及圖案結合效能下，所提出的 SRMCNN 能用於聯想記憶系統執行影像處理應用。

其次，根據自回授比例記憶細胞式非線性網路架構，提出一個使用 B 或(A 和 B)樣板於自回授比例記憶之細胞式非線性網路架構；這網路能學習樣本圖案並正確輸出辨識圖案在異聯想記憶的應用上。B 樣板中之權重值可以由已知之輸出圖素和對應神經元之五個相臨輸入圖素之乘積並累積所有輸入樣本圖案得到。透過學習得到之權重值分別除以樣板中所有係數之絕對值的和，此比例記憶的效果可增強圖案的特徵，並辨識八個具黑百雜訊之圖案。將 A 和 B 樣板同時使用於 SRMCNN，在異聯想記憶應用的行為和功能其模擬結果作展示及分析，成功處理四個經旋轉之圖案；由此觀之，SRMCNN 對於變異性較大圖案之學習與辨識能力可以大大改善。

最後，針對所提出具 B 樣板於自回授比例記憶細胞式非線性網路的架構配合修正之 Habbian 演算法在異聯想記憶應用的電路設計。功能方塊由 0.25 微米互補式金氧半製程技術設計出超大型積體電路，以 HSPICE 軟體驗證電路之正確性。實現一位元具 B 樣板於 SRMCNN 之超大型積體電路晶片，觀察其比例記憶的功能動作；展示並分析 18x18 SRMCNN 行為和功能在異聯想記憶應用的模擬結果。因此，SRMCNN 具有方便超大型積體電路硬體電路實現的特點，且對圖案學習與辨識的能力有效地改善。最後提出並描述一個具有大鄰近層數不對稱模版的細胞式非線性網路泛用機器一般架構的概念性設計。

經由模擬與實驗的驗證，本論文以雙載子接面電晶體乘除法器發展出自回授比例記憶細胞式非線性網路架構，SRMCNN 在各種異聯想記憶應用中被設計於單一晶片上之神經網路系統，極具研究潛力，而大鄰近層細胞非線性網路之設計則簡化了大鄰近層連線的複雜度。在 SRMCNN 領域未來仍有繼續研究之議題；將比例記憶整合於聯想記憶功能中用於細胞式非線性網路泛用機器處理及時影像於類比平行影像處理系統是可繼續進行之研究。

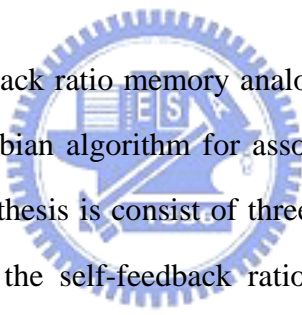
# THE DESIGN AND ANALYSIS OF THE SELF-FEEDBACK RATIO-MEMORY CELLULAR NONLINEAR NETWORKS AND THEIR APPLICATIONS IN ASSOCIATIVE MEMORIES

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## ABSTRACT



In this thesis, the self-feedback ratio memory analog cellular nonlinear network structure with the modified Hebbian algorithm for associative memory applications are designed and analyzed. The thesis is consist of three main parts: (1) the analysis and design of the structure of the self-feedback ratio memory cellular nonlinear (neural) network (SRMCNN) that applied to the implementation of the analog associative memory; (2) the design of the SRMCNN structure with **B** (**A** and **B**) template for Hetero-associative memory applications; (3) the VLSI implementation for the 18x18 SRMCNN and the conceptual design for the Cellular Nonlinear(Neural) Network Universal Machine with programmable large-neighborhood.

Firstly, a learnable cellular nonlinear network (CNN) with space-variant templates, ratio memory (RM), and modified Hebbian learning algorithm is proposed and analyzed. By integrating both the modified Hebbian learning algorithm with the self-feedback function and a ratio memory into CNN architecture, the resultant ratio-memory (RMCNN) is called the self-feedback RMCNN (SRMCNN) which can serve as the associative memory. It can generate the absolute weights and then transform them into the ratioed A-template weights as the ratio memories for

recognizing noisy input patterns. Simulation results have shown that with the stronger feature enhancement effect, the SRMCNN under constant leakage current can store and recognize more patterns than the RMCNN. For 18×18 SRMCNN, 93 noisy patterns with a uniform distribution noise level of 0.8 and a variance of normal distribution noise of 0.3 can be learned, stored, and recognized with 100% success rate. The SRMCNN has greater learning and recognition capability when the learned patterns are simpler and the noise is lower. For the learning and recognition of complicated patterns, the allowable pattern number is decreased for a 100% success rate. Simulation results have successfully verified the correct functions and better performance of SRMCNN in the pattern recognition. With high integration capability and excellent pattern association performance, the proposed SRMCNN can be applied in the associative-memory systems for image processing applications.

Secondly, the architecture with embedded ratio memory and realized the modified Hebbian learning algorithm in the SRMCNN with **B** (**A** and **B**) template is proposed. It can learn the exemplar patterns and correctly output the recognized patterns for hetero-associative memory applications. The weights of the **B** template are generated from the product of the desired output pixel value and the nearest five neighboring element as associative memory for all input exemplar patterns. The learned weights are processed in the ratio with the summation of absolute coefficients on the **B** template. The efficiency of ratio memory is enhanced the feature of pattern. The learned SRMCNN with **B** template can successful recognized the eight test patterns with white-black noise for auto-associative memory applications. The simulation results of the behavior and function of the SRMCNN with **A** and **B** templates for hetero-associative memory applications are demonstrated and analyzed. As the results shown that it was learned and recognized five exemplar patterns and output correctly pattern. The capability of SRMCNN for the more variant exemplar patterns learning and recognition is greatly improved in the hetero-associative memory applications.

Finally, the structure of the SRMCNN with **B** template and the modified Hebbian learning algorithm for auto-associative memory are proposed. The function blocks are implemented in the VLSI circuits for the 0.25  $\mu\text{m}$  1P5M n-well CMOS technology. The characteristics of the proposed circuits are correctly verified by the HSPICE software. The function of ratio memory for one bit SRMCNN with B template was realized in the VLSI chip and their behavior was observed. The simulation results of the 18x18 SRMCNN behavior and function are demonstrated and analyzed. Thus, the SRMCNN has a great feature that the network can easily implemented in VLSI hardware circuits. The capability of pattern learning and recognition is also improved. The conceptual design for the general architecture of the Large-Neighborhood Cellular Nonlinear (Neural) Network Universal Machine (LN-CNNUM) is described.

As the results, the proposed SRMCNN structure used the analog current mode four-quadrant multiplier and two quadrant divider and its applications in associative memories have a great potential for the system-on-a-chip to realize the neural network systems, and the LN-CNNUM structure can simplify the complex of the large-neighborhood interconnections. Further researches will be join in the SRMCNN research in the future, and the embedded ratio memory structure will be used into the analog parallel image processor for the real-time image processing system development.

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賴 瑞 麟  
誌於 風城交大  
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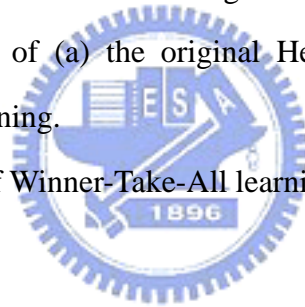
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## CHAPTER 4



Fig. 4.1 General architecture of the SRMCNN.

Fig. 4.2 Illustration for weights learning algorithm.

Fig. 4.3 Detailed architecture of (a) two neighboring cells and their ratio memories (RM) and (b) the S block in the SRMCNN during the learning period.

Fig. 4.4 Detailed architecture of (a) two neighboring cells and their ratio memories (RM) and (b) the S block in the SRMCNN during the elapsed period.

Fig. 4.5 Detailed architecture of two neighboring cells and their ratio memories (RM) in the SRMCNN during the recognition period.

Fig. 4.6 The error function during elapsed time factor.

Fig. 4.7 The test patterns of character A with white-black noise

Fig. 4.8 The test patterns of character A with normal, expanded, left-rotate, right-rotate, and reversal types

Fig. 4.9 The recognition sequence of expanded A character during recognition



period

Fig. 4.10 The recognition sequence of left-rotate A character during recognition period

## CHAPTER 5

Fig. 5.1 The detailed architecture of two neighboring cells and their ratio memory (RM) in the SRMCNN

Fig. 5.2 The S block in the SRMCNN during (a) learning period and (b) recognition period

Fig. 5.3 (a) The circuit of V-I converter of the blocks T2, and the absolute-value circuit; (b) The HSPICE simulation results

Fig. 5.4 Sign latch

Fig. 5.5 Sign detector

Fig. 5.6 The CMOS circuit of the block M/D

Fig. 5.7 HSPICE simulation results for (a) Multiplication function with  $I_2=20\mu\text{A}$  (b) Division function with  $I_1=6\mu\text{A}$

Fig. 5.8 The CMOS readout circuit for the cell output

Fig. 5.9 SRMCNN (a) learn data with the five neighboring cells for six data input; (b) the learned weights; (c) learning and ratio state; (d) the ratioed weights during each elapse time

Fig. 5.10 The layout graph of one bit SRMCNN for learning and ratio

Fig. 5.11 The HSPICE simulation (a) learn five exemplar patterns with white-black noise and the recognized output pattern; (b) zoom-out the data of exemplar patterns; (c) zoom-out the recognized pattern

Fig. 5.12 The layout graph and characteristics for 9x9 SRMCNN system

Fig. 5.13 Global architecture of LN-CNNUM.

Fig. 5.14 (a) Structure of LN-CNN kernel unit. (b) Connections between neighboring cells and

Fig. 5.15 Weights of the LN-CNNUM in (a) template **A** and (b) template **B**.

Fig. 5.16 Architecture of one cell in the LN-CNNUM



