CHAPTER 6

CONCLUSIONS AND FUTURE WORKS

6.1 MAIN RESULTS OF THIS THESIS

The ratio memory cellular nonlinear network with self-feedback (SRMCNN) is proposed and analyzed. In the SRMCNN, the modified Hebbian learning algorithm with self-feedback is applied to the generation the absolute weights from the sets of input exemplar patterns and then transform them into ratio weights through the ratio memory to form the coefficients of space-variant **A** template. With RM and the modified Hebbian learning algorithm with self-feedback, the SRMCNN can be used as the auto-associative memory for learning, recognizing, and recovering patterns. The simulation results have shown that the 18×18 SRMCNN with five weights connection can learn and recognize 93 noisy patterns with a 100% success rate at a uniform distribution level of 0.8 and a normal distribution variance of 0.3. This has successfully verified the correct function and superior performance of SRMCNN in the patterns recognition.

The proposed SRMCNN with the feature enhancement effect of the RM under constant leakage on the template coefficients can learn and recognize patterns with fewer weight connections than that of the Hopfield neural network. Moreover, the proposed SRMCNN with the self-feedback ratio weight can learn and recognize more patterns than the CNN associative memories with RM and without RM, given the same learning algorithm and the same constant leakage in the coefficients of space-variant templates. Simulation results have successfully verified the correct function of 18×18 SRMCNN. Since the proposed SRMCNN has the advantages in learning, storing, and recognizing image patterns, it is suitable for appropriate applications of the associative memory systems for real-time image processing.

The self-feedback ratio memory cellular nonlinear network with B template for associative memory applications is proposed and analyzed. In the SRMCNN, the five weights in the **B** template are generated and updated from a set of exemplar patterns, and the ratioed weights in the ratio of the absolute summation of its neighborhood was stored in the associative memory. From the simulation results, it has been verified that the 18×18 SRMCNN can learn and recognize nine patterns with white-black noise for the character A. The recognition rate was reduced for more than one-desired patterns of the English characters. The SRMCNN able to learn and recognize more patterns as compared to the CNN without RM, the capability is similar Hopfield neural network but with less network complexity.

In the SRMCNN with **A** and **B** templates, the weights are learned for the set of exemplar patterns, and the ratioed weights are generated from its neighboring weights to store in the associative memory. The SRMCNN have the capability to process the larger singularity test patterns and output correctly the recognized pattern. As the results, input test patterns as normal, expanded, left-rotate, right-rotate, and reversal of the English character A, the system is able to recognize the correct pattern during an iterations period. Therefore, the capability of the proposed SRMCNN with the modified Hebbian learning algorithm for the pattern learning and recognition has improved. Moreover, the proposed SRMCNN can easily be implemented and fabricated by the mixed signal technology in VLSI for various applications.

From the simulation results, it is found that the spatial-variant template **A** with self-feedback weight can enhance the storage capacity and recognition rate of the SRMCNN for the auto-associative memory applications. As compared to original RMCNN, the SRMCNN need an addition to one Multiplier/divider circuit, two capacitors, and V-I converters used to learn and storage for the self-feedback weight in the template **A**. Though the cell area of SRMCNN is larger than the original RMCNN, but the pattern processing capability of the SRMCNN is at least 16 times of original RMCNN. The recognition rate of SRMCNN is also great improved that better than the original RMCNN. The corresponding learning algorithm has the following beneficial: easy learning algorithm, additive learning property, and a constant learning time. In the Table 6.1 presented the comparison results that to show the SRMCNN are acceptable resolutions then other CNN-based associative memory. Except that the 18x18 SRMCNN can be used in auto or hetero associative memory for patterns processing applications.

An analog multiplier/divider based on Bipolar Junction Transistor (BJTs) has been proposed and analyzed [171]. It utilizes the exponential relationship between the emitter current and the base-emitter voltage of BJT. The cascaded base-emitter voltage of BJT can generate an emitter current, which is the product of the initial input currents. Using this relation, both multiplication and division can be realized in a simple BJT structure. The multiplier-divider can be used to calculate the learned weights, ratioed weights, and the state of neuron within the learning and recognition period for the self-feedback ratio-memory cellular nonlinear (neural) network applications. Due to its compact structure, this circuit has a great potential in neural network application. It also has been successfully applied to the implementation of the analog ratio-memory cellular nonlinear (neural) network for image processing applications. The SRMCNN has been designed and analyzed in CMOS technology and implemented into VLSI chip.

The structure of the self-feedback ratio memory cellular nonlinear network with modified Hebbian algorithm is proposed and analyzed for hetero-associative memory applications. In the SRMCNN, the weights of the **B** template are generated from a set of the exemplar patterns, the desired output pattern, and then transform the learned weights into ratio weights are stored on the ratio memory. The proposed network can be used the pattern learning, recognition, and recovery in hetero-associative memory for the various image processing applications. The function blocks has implemented by the 0.25 μm 1P5M n-well CMOS technology. The correctly characteristic of the proposed circuits are also verified by the HSPICE software. As the feature of ratio memory, the experimental chip of one bit SRMCNN with **B** template is implemented to observe the feature enhancement effect. The chip area including one neuron cell and five RMs is 350μm x 400μm. The five neighboring pixels are input in serial for six data to the SRMCNN with the period 0.5μs per each charge time. The desired output of the cell is 1. The absolute coefficients of the learned weights of the **B** template are gradually decreased with the constant leakage current for the elapsed period. The weights with leakage used in the ratio of the absolute summation for its neighboring weights of B template. The operation of ratio state in the SRMCNN is presented the zoom-out variations of the five weights versus the elapsed period from 8μs to 22μs after learning time. As the simulation results, the larger value of the weight is enhanced the ratioed weight to 1 and the smaller values of the weights are suppressed to zero during the elapsed period. The simulation results have successful verified the correct function of the 18x18 SRMCNN for patterns recognition. Thus, the SRMCNN can correctly recognize the output pattern for any one exemplar input test pattern. Due to the simulation results, the SRMCNN with **B** template and modified Hebbian algorithm can successful recognized the noisy patterns with white and black noise for hetero-associative memory applications. Finally, the conceptual design for the general architecture of the Large-Neighborhood Cellular Nonlinear (Neural) Network Universal Machine (LN-CNNUM) is introduced.

6.2 FUTURE WORKS

The proposed SRMCNN with locally connected neighboring cells have the advantage of simple and compact structure for the associative memory applications. It is very suitable in the analog VLSI implementation of the neural networks and their function has been verified by the simulation results or the measurement data from the implemented chips. The SRMCNN has ability to use in real-time image processing for the variety practically applications. Thus, the visual sensor system able to integrate the SRMCNN input the patterns for the learning and recognition operations. The CMOS smart sensor circuits are design to use the image acquisition in the future.

The SRMCNN with **B** template for auto-associative memory applications has been presented. Its processing capabilities of the patterns recognition are also improved. The SRMCNN structure with learning algorithms is successfully implemented in the analog VLSI circuits. The chip area required that the desired structure implementation is reduced with optimal design in the fabrication limit. The simplest hardware circuits or fewer components used to design the neuron and weight with same characteristics can continuously be researched.

The SRMCNN system with A and B templates realized for VLSI implementation is progress in future. This implemented circuit may be very complexity and the chip scale is largest. The improvement of the algorithm, changing the learning time of each learned pattern is another research issue. The threshold template **Z** will be developed to enhance the recognition rate of the SRMCNN, and transferring the threshold template **Z** with A or B template to the ratio form may be adopted.

The SRMCNN with visual system is used in the powerful real-time image processing systems for associative memory applications. The embedded visual image is designed to input the patterns for the learning and recognition. The CNN with fuzzy operation in the gray-level image processing can be considered and implied for the software simulation or the hardware implementation. In addition, the embedded chaos operation is used to generate the weights of the template in the SRMCNN for pattern processing. The efficiently structure is also proposed in the future.

The CNNUM with large neighborhood templates, is called LN-CNNUM, is an array analogical computer with a LN-CNN kernel. The LN-CNNUM is organized the different kinds of LN-CNN structures to perform complicated tasks that a single CNN cannot finish. The LN-CNNUM can also be used to solve some global problems that are difficult to decompose in the conventional CNN structure. Based upon the LN-CNNUM structure, the system will be designed and implemented in 0.25μm CMOS technology for image processing applications. Thus, the hardware implementation, the simpler connections of LN-CNNUM, and embedded ratio memory in CNN kernel will be also developed in the future.

Future research on efficient physical elements for the SRMCNN implementation will concern nano-scale devices and integration. Additionally, research into LN-CNNUMs will also concern the nanoelectronic regime, and lead to the development of a feasible and powerful nano-scale CNNUM (Nano-CNNUM).

Table 6.1 Recently reported of CNN-based associative memory

	RMCNN '02 [171]	SRMCNN	'93[59]	'97[109]	'01[110]	'03[173]	'04[182]
Hardware Implementation	yes	not yet	no	no	yes	N0	yes
Additional Host Computer	Not need	Not need	need	need	need	need	Cellular Array Processor
Cell Array	9x9	18x18	9x9	9x9	12x12*	64x64	2x72
Stored Patterns	3	98	25	25	8	13 (gray level)	**
r-neighborhood	*r*=1	*r*=1	*r*=3	*r*=2	*r*=1	*r*=1	*r*=1
Additive in Storage	yes	yes	no	yes	yes	yes	yes
Learning Algorithm	Modified Hebbian	Modified Hebbian	Singular de-composition	Hebbian+ gain factor	Digital learning	Ratio-rule	no
Total Learning Time	constant***	constant***	depend on no. of learned patterns	depend on no. of learned patterns	depend on no. of learned patterns	depend on no. of learned patterns	

* 12x12 cell array is simulated by computer in this paper.

** only hardware implementation

*** Total learning time can be constant by keeping the total integrating time to be constant.