國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

新穎矽奈米線元件之研製與應用

Fabrication and Analysis of Novel Silicon Nanowire Devices and Their Applications

研 究 生：蘇 俊 榮

指導教授：林 鴻 志 博士

黃 調 元 博士

中華民國九十七年十二月

新穎矽奈米線元件之研製與應用

Fabrication and Analysis of Novel Silicon Nanowire Devices and Their Applications

研 究 生：蘇俊榮　　Student：Chun-Jung Su

指導教授：林鴻志 博士　　Advisors：Dr. Horng-Chih Lin

黃調元 博士　　Dr. Tiao-Yuan Huang

國 立 交 通 大 學

電子工程學系 電子研究所

博士論文

A Dissertation

Submitted to Department of Electronics Engineering &
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering
December 2008
Hsinchu, Taiwan, Republic of China

中華民國九十七年十二月

新穎矽奈米線元件之研製與應用

研究生: 蘇俊榮　　指導教授: 林鴻志 博士

黃調元 博士

國 立 交 通 大 學

電子工程學系 電子研究所

摘要

本文提出一新穎多晶矽奈米線電晶體之結構與製作。其製備之特點為利用一般製作側壁邊襯(sidewall spacer)之概念，來形成多晶矽邊襯，此邊襯之直徑可以準確地控制至 20 nm ~ 90 nm，故可巧妙地將之作為多晶矽奈米線通道。此外，相較於一般奈米線製備方式(top-down 和 bottom-up)，本文所提出新結構的主要優越之處在於不需昂貴的設備和高門檻的技術，便可以簡易製程步驟來達到：(1) 直接控制奈米線直徑和長度，(2) 精準定義奈米線位置，(3) 定義汲極和源極之同時，可自我對準形成奈米線通道，(4) 再現性及可靠度高之多晶矽奈米線電子元件。

首先，藉由基本電性之探討結果，發現此多晶矽奈米線元件之開狀態(on-state)性能受到某種程度之限制，以及關狀態(off-state)時展現特殊的漏電流現象。這些

問題主要來自於固相結晶所形成之多晶矽具有相當多之缺陷，並且原本所設計之製程和結構有所缺失，而造成此獨特之漏電機制。此漏電流表現，可藉由本研究所提出之結構和製程修正方式明顯得到改善。此外，為了改善多晶矽之結晶品質，本研究使用電漿氫化處理來修補不完整鍵結之缺陷，以及利用金屬誘發側向結晶(MILC)或/和快速熱退火(RTA)的方式來增益奈米線本身的結晶特性。使用 MILC 製程的過程中，我們發現奈米線的長度、寬度以及結晶引洞的排列，對所形成的薄膜結晶品質有很大之影響。再者，經由結合 MILC 和 RTA 處理之多晶矽奈米線，可以得到非常優異之元件性能。由 TEM 圖分析得知，在此條件下可以獲得具有單晶品質之矽奈米線，此良好結晶性質之矽奈米線可顯著地反映至元件的性能表現上。值得注意的是，在本研究中，元件可以得到高達 550 cm^2/V-sec 之電子遷移率和 230 cm^2/V-s 之電洞遷移率，這些特性為目前奈米線相關文獻中的最佳成果。

除了改善薄膜結晶品質外，本研究更採用多重閘極結構來提升對奈米線通道之控制能力，進而增進元件性能表現。基於本研究電晶體巧妙之架構，多晶矽奈米線可精準地與側、下和上閘極排列。由於奈米線本身體積小，因此可以增強多重閘極之間的偶合作用，故在多重閘極的操控下，元件的性能可以大幅提升。傳統以雜質摻雜調整臨界電壓的方式，易導致奈米線中雜質分佈不均，而本結構的多重閘極可單獨施壓以調控通道之臨界電壓，此調控方式相當可靠且穩定，能避免雜質分佈不均之問題，因此本研究之多重閘極奈米線結構相當具有實用性。

最後，本研究探討多晶矽奈米線用於感測應用方面之可行性。當今大部份的生化感測反應皆於水溶液中進行。而本研究發現，在水溶液中，此多晶矽奈米線元件之表現可以提升至與單晶矽相當，所以其感測靈敏度也會隨之升高。其可能的原因來自於水中的氫(H^+)或/和氫氧離子(OH^-)對於奈米線內的晶體缺陷，具有明顯且完整之修補作用，並且此修補作用具有再現性。因此，我們將表面具有特定接受器(receptor)之奈米線，進行 pH 值和生化分子之感測實驗，此奈米線展現相當不錯之感測能力和選擇性。

關鍵字：金屬誘發側向結晶，多重閘極，奈米線，電漿修補處理，多晶矽，快速熱退火，感測器，側壁邊襯，固相結晶，薄膜電晶體

Fabrication and Analysis of Novel Silicon Nanowire Devices and Their Applications

Student: Chun-Jung Su Advisors: Dr. Horng-Chih Lin

Dr. Tiao-Yuan Huang

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

Abstract

A novel field-effect transistor (FET) using sidewall-spacer polycrystalline silicon nanowire (poly-Si NW) channels is disclosed and investigated. This scheme features well-controlled dimension, accurate positioning and alignment of NWs as well as reliable source/drain (S/D) contacts. In addition, the approach is reproducible and suitable for low-cost manufacturing.

From the examination of the basic electrical properties, an anomalous leakage behavior and suppressed on-state performance are found. These issues are identified to be due to a deficiency in the original device design and the inherent defective crystallinity of solid-phase crystallized (SPC) poly-Si. With the structural and process modifications proposed in this study, the unsatisfactory off-state characteristics could

be effectively eliminated. To improve the poly-Si crystal property, plasma hydrogenation, metal-induced lateral crystallization (MILC) and/or rapid thermal annealing (RTA) techniques are employed to passivate the microstructural defects and enhance the crystallinity of the NWs, respectively. In the implementation of MILC process, it is shown that the arrangement of seeding window and the dimension of the NWs play an important role in affecting the resulting film quality. Furthermore, MILC coupled with RTA results in excellent device performance. With the TEM analyses, it is found that single-crystal-like NWs are achieved, leading to significant performance improvement. It is noteworthy that superior field-effect motilities up to 550 cm^2/V-sec for electrons and 230 cm^2/V-s for holes recorded in this study are among the best reported results for NW devices in the literature.

In addition to improving the film crystal property, an alternative strategy is to uplift the gate controllability over the channel with the adoption of multiple-gated (MG) configuration. Based on the proposed device structure, poly-Si NWs can be precisely positioned with respect to the side-gate, bottom-gate and top-gate. The strong gate coupling effect of the MG operation, which is ascribed to the tiny body of NW channels, thus dramatically promotes the device performance. Moreover, another great benefit of such scheme is that the independently applied gate bias can be employed to regularly adjust the threshold voltage (V_{th}) of NW channels in a reliable

manner. The experimental results indicate that the V_{th} could be modulated by the gates with both positive and negative biases, making it suitable for practical applications.

Finally, the capability and feasibility of poly-Si NWs for sensing applications are investigated. In this work, the device performance is dramatically improved to a level comparable to the monocrystalline-Si counterparts, as poly-Si NW channels are exposed to the aqueous environment. Passivation of defects in the poly-Si NW by H^+ and/or OH^- contained in the aqueous solution is proposed to explain the phenomenon. Moreover, this passivation effect is stable and reproducible. This finding is especially important as it implies that poly-Si NWs can be cleverly operated in aqueous solutions to take advantage of the performance improvement. Consequently, by functionalizing specified receptors on their surface, poly-Si NWs exhibit good sensibility and selectivity for pH-value and biomolecules detections.

Keywords: Metal-induced Lateral Crystallization (MILC), Multiple Gate (MG), Nanowire, Plasma Passivation, Polycrystalline Silicon (Poly-Si), Rapid-thermal Annealing (RTA), Sensor, Sidewall Spacer, Solid-phase Crystallization (SPC), Thin-film Transistor (TFT)

誌　　謝

由衷地感謝指導教授林鴻志博士和黃調元博士，博學多聞且無私的指導，以及嚴謹的研究態度，著實為學習之典範，讓我受用一生。老師們對學生於獨立思考能力之要求甚鉅，並總能適時地指點和鞭策，讓我在這些年中成長許多，對於老師們的感激之情，著實難以用言語形容，僅能銘記在心。

特別感謝美國休士頓大學陳永松教授對於工程科學上之啟蒙指導，幫我開啟了浩瀚學術領域之大門。謝謝交大材料系吳耀銓教授於大學專題時之指導，當時所學之知識和實作經驗對於本論文助益匪淺。另外也感謝胡振國教授、賴朝松教授、蔡銘進博士、陳明哲教授和崔秉鉞教授對於論文給予的寶貴意見和指導。

本論文之完成另外得感謝共同參與奈米國家型計畫的楊裕雄教授和柯富祥教授，以及李政哲、蕭程允和吳佳典等同學們，藉由此堅強團隊之腦力激盪和創意開發，構築了本論文主要之架構，並開啟了許多新穎且值得深入探討之主題。

在此感謝先進元件技術實驗室所有同學們的相互鼓勵學習。感謝嘉裕學長耐心且詳盡地教導儀器之操作和經驗之分享，也謝謝宏年和明賢學長於實驗上之帶領和訓練。同時也感謝耀仁、文泰、冠麟、百宏學長和景森於研究上之討論和建議；感謝一起打拼、共同經歷爆肝生活的夥伴們：銑泓、行徽、凱翔、健銘、育峯、子銘、子儀、政雄、威臣、冠樟和漢仲等，謝謝你們於實驗上之協助和陪伴。另外，感謝國立交通大學和國家奈米元件實驗室提供良好的環境和完善的儀器設備，使研究之進行皆得以順利完成。

此外，感謝在德國期間共同於 RWTH Aachen 大學進行訪問研究的莊傑、宛邵和凌珠，在異鄉生活有你們的陪伴和互相激勵，讓我擁有許多美好回憶。

最後，特別感謝我的父母：蘇文慶先生和黃玉燕女士，由於您們無私的付出，才能讓我無後顧之憂地不斷往前邁進；感謝姐姐、姐夫和最可愛的外甥們，讓我在求學的路途上，隨時感受到最溫暖的親情慰藉。感謝岳父母：汪建民博士、陳幼雪女士和妹妹一直以來的關心、鼓勵與支持；更要感謝在求學路途和生活上長久以來互相扶持的汪砡華小姐，與我分享度過無數個人生高低潮，一起於世界上各個角落留下我們的足跡，有了妳的陪伴是我最大的福分。

謹以此論文獻給我摯愛的家人、敬重的師長和所有的朋友。

蘇　俊　榮
誌於風城交大
戊子年甲子月

Contents

Table Captions

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Appendix

Chapter 1

Introduction

One-dimensional structures, such as nanowires (NWs), could be ideal building blocks for nanoelectronics, because they can function both as devices and as the wires that access them. Owing to the inherent properties of NWs, i.e., very tiny volume and high surface-to-volume ratio, some interesting phenomena will turn up in several aspects. For development of extremely scaled-down electronic devices, NWs will show reduced phonon scattering, good gate controllability and thus suppress the undesirable short-channel effects. For memory applications, NWs can promote high programming efficiency and low voltage operations. As for sensor applications, large surface-to-volume ratio will provide high sensitivity.

1.1 An Overview of Nanowires

Minimization of silicon (Si) electronics is being actively pursued. One-dimensional structures, such as NWs, have great potential for testing and understanding fundamental concepts about the roles of dimensionality and size in electrical properties. Because Si NWs can transport electrons and holes, they could

function as building blocks for nanoscale electronics assembled without the need for complex and costly fabrication facilities [1.1]. Owing to the inherently high surface-to-volume ratio feature, NWs can suppress short-channel effects encountered in nano-scale metal-oxide-semiconductor field-effect transistors (MOSFETs) [1.2] and provide high surface sensitivity for sensing devices. Many possible applications of Si NWs have been exploited, including complementary MOS (CMOS) [1.2, 1.3], memory devices [1.4], NW thin-film transistors (TFTs) [1.5], and biosensors [1.6].

Preparations of Si NWs could be categorized into two types, namely, top-down and bottom-up, described as follows:

1.1.1 Top-down Approach

This approach employs advanced lithography techniques, such as deep UV [1.7], e-beam [1.8]. Nano-scale patterns are first defined on silicon-on-insulator (SOI) substrates, and then transferred to the underlayer to form Si NWs by dry-etching, as described in Fig. 1-1. These techniques are well developed and mature for mass production purpose. Nevertheless, very expensive equipments and cutting-edge technologies are required. The other approach to prepare nano-scale structure is by nanoimprint [1.9]. As illustrated in Fig. 1-2, a mold with nano-features is impressed into the resist, and then transferred to the substrate.

Conventional photolithography processes (e.g., G-line and I-line steppers), though relatively cheap for manufacturing, are not capable of patterning NWs directly. Some special skills such as thermal flow [1.10], chemical shrink [1.11], and spacer patterning [1.12] have been proposed to help generate the nano-scale patterns using these conventional lithography tools.

1.1.2 Bottom-up Approach

This approach typically utilizes deposition methods to prepare the NWs, and synthesize the NWs on a substrate. Afterwards, these NWs are harvested and dispersed into a solution. Depositing the harvested NWs onto another oxidized substrate and making electrical contacts to the NWs, will complete the device structure. Many deposition methods have been developed nowadays which include laser ablation catalyst growth [1.13], chemical deposition catalyst growth [1.14] and oxide-assisted catalyst-free method [1.15]. The first two methods are carried out with metal nanocluster catalyst as the energetically favored sites for absorption of gas-phase reactants, and then the cluster supersaturates and grows a wire-like structure of the materials, as shown in Fig. 1-3. The process is based on vapor-liquid-solid (VLS) mechanism. Nanometer-diameter catalyst clusters define the size of wires produced by VLS growth, in which bulk quantities of single crystalline

NWs can be obtained. The approach can also be applied to prepare NWs of other materials in addition to Si, such as III-V compounds and II-VI compounds [1.16]. However, metal contamination is a potential concern in this approach. Oxide-assisted catalyst-free method is conducted without metal nanocluster catalyst, and thus is free from metal contamination. Nevertheless, there could be plenty of defects in the wires, and hence it is not applicable to electronic devices. In addition, these aforementioned methods usually suffer from the poor control of structural parameters such as NW's diameter, length, and orientation.

Methods used to assemble and align the NWs prepared by "bottom-up" approach include electric-field-directed assembly [1.17], microfluidic channel [1.18] and Langmuir-Blodgett (LB) technique [1.19]. Electric field method is via interaction between electric field of two parallel electrodes and polarity of NWs, and therefore directs the wires. Although electric fields enable more control over assembly, this method is limited by electrostatic interference between nearby electrodes as separations are below micrometer level and the requirement of extensive lithography to fabricate the electrodes. Fluidic channel method is to align wires by flowing NWs suspension inside a polydimethylsiloxane (PDMS) mold, and could obtain layer-by-layer assembly of multiple-crossed NW arrays. However, the size of fluidic channels may limit the alignment of NWs. LB method could assemble a large-area

anisotropic NWs by compression process, but it is restricted to the preparation of one monolayer. Overall, for practical applications, more refinement is needed to improve the reproducibility and controllability of the above methods.

In brief, most of the proposed schemes for device fabrication based on "bottom-up" nanostructures are plagued by complex integration that lacks reproducible transfer and positioning of NWs and reliable ohmic contacts. Moreover, the control of doping concentrations in self-assembled semiconducting NWs remains a challenge, and it's difficult for high-density integration. On the other hand, the top-down approaches usually require expensive lithography apparatus and materials that dramatically increase the fabrication cost. To circumvent these shortcomings, we propose and develop a new method for preparation and fabrication of Si NWs devices in this thesis. The NW material in this unique method is polycrystalline in nature, and thus the general low-temperature recrystallization methods are exploited to achieve this purpose.

1.2 Low-temperature Crystallization Techniques

1.2.1 Solid-phase Crystallization

Since amorphous Si (a-Si) is a noncrystalline element solid state that is

considered to be at a metastable state. When given a sufficient energy to overcome the initial energy barrier, the phase transformation from a-Si to crystalline Si will take place by a thermodynamic driving force. The transformation is typically carried out by annealing in a furnace at a certain temperature (typically at 600 ^{o}C) to break and reorganize Si bonds. Since the structure stays in the solid state during this phase transformation, the technique is called solid-phase crystallization (SPC). The crystallization from an amorphous phase to a crystalline phase occurs through two processes, namely nucleation and grain growth [1.20], and both have characteristic activation energies. The nucleation activation energy is extracted from the time to onset of crystallization, i.e., the incubation time, while the grain growth rate is extracted from grain progression data. Normally, the nucleation activation energy is larger than the grain growth activation energy for the SPC Si [1.21]. To achieve the largest possible grains, it is desirable to suppress nucleation relative to grain growth. Therefore, SPC is typically done at a low temperature. Unfortunately, this results in a reduction in throughput through an increase in the incubation time and a decrease in the grain growth rate.

1.2.2 Metal-induced Lateral Crystallization

Metal-induced crystallization (MIC) is potentially a promising approach to grow crystalline Si at a low enough temperature because of lower energy barrier of recrystallization resulting from the reaction between metal and Si. Therefore, the annealing process could be performed at a reduced temperature (below 600 ^{o}C) and shorter time to obtain good film quality. Generally, metals employed in the MIC mechanism can be classified into two groups. One is silicide forming metals (Ni [1.22], Co [1.23] and Pd [1.24]) and the other is to form eutectics with Si instead of silicide (Al [1.25], Au [1.26] and Sb [1.27]). However, the MIC process provokes the drawback of incorporating undesirable metal impurities into crystallized Si, making it not suitable for the fabrication of TFTs. Instead, a reinforced scheme called metal-induced lateral crystallization (MILC) was proposed to achieve the purpose of reducing the possibility of metal contamination and enlarging the grain size. Fig. 1-4 displays the MIC and MILC processes employed in the fabrication of poly-Si TFTs. During the annealing, MIC will first take place, and then lateral crystallization.

In this thesis, Ni is chosen for discussion because of the lowest silicide formation temperature at about 150 ^{o}C. The final phase in the formation of Ni-silicide is $NiSi_2$, which has a cubic lattice. The lattice constant of Si and $NiSi_2$ is 5.430 Å and 5.406 Å, respectively, leading to very small lattice mismatch of 0.4 % with Si and enabling the

formation of epitaxial Si. The formation process of $NiSi_2$ precipitate is starting from Ni atoms and diffusing into a-Si matrix, leading to the formation of Ni silicide in the early stage of thermal annealing. The phase follows the sequence $Ni_2Si \rightarrow NiSi \rightarrow NiSi_2$. At temperature in the range of 450-750 ^oC, the NiSi transforms into thermodynamically favored phase, $NiSi_2$ [1.28]. Subsequently, the $NiSi_2$ crystallites serve as the nuclei for crystallization. Note that the diffusivity of Ni in a-Si is ten times higher than that in c-Si [1.29]. Hence, the $NiSi_2$ is formed due to the diffusion of Ni in the a-Si network. Fig. 1-5 shows the schematic illustration of phase transformation mediated by Ni, in which needle-like Si crystallite is formed after the migration of $NiSi_2$ in a-Si network.

The driving force for the crystallization of a-Si is the reduction of free energy [1.22]. The equilibrium free energy diagram of Si and Ni at the interface of $NiSi_2$/a-Si and $NiSi_2$/c-Si is illustrated in Fig. 1-6. Reading from the figure, the chemical potential of Ni at $NiSi_2$/c-Si interface is higher than that at the $NiSi_2$/a-Si interface, whereas the chemical potential of Si shows the reversed property. Consequently, during the migration of $NiSi_2$ crystallite, the a-Si is consumed at the $NiSi_2$/a-Si interface and needle-like Si grain is generated at the other side of the $NiSi_2$ crystallite, as shown in Fig. 1-5.

1.3 Nanowire Sensor Devices

Nanostructures such as NWs are attractive for versatile applications, particularly as biosensors, since the critical dimensions, like diameter of NWs, are comparable to the sizes of biological and chemical species [1.30]. The detection sensitivity is therefore greatly enhanced as the signal can be effectively transduced. NWs have the potential for very high sensitivity detection because the depletion or accumulation of charge carriers, which are caused by binding of charged biological molecules at the surface, can affect the entire cross-sectional conduction pathway of these nanostructures. The fundamental concept of Si NWs being used as an ultrasensitive detector is by taking advantage of the field effect. The conductance of the Si NW device is controlled by a gate electrode capacitively coupled through a dielectric layer. The dependence of the conductance on gate voltage makes FETs natural candidates for electrically based sensing since the electric field resulting from binding of a charged species to the surface is analogous to applying a voltage using a gate electrode.

The selectivity of a sensor is an important element, which can generally be configured from Si NW devices by linking recognition receptor groups to the surface of the nanowire. The unintentional native silicon oxide on Si NWs makes this receptor linkage straightforward. When the sensor device with surface receptors is exposed to

a solution containing a macromolecule which has a net positive (or negative) charge in aqueous solution, specific binding will lead to an increase (or decrease) of surface negative charges and an increase (or decrease) in conductance for a n-type NW device. The underlying concept is illustrated in Fig. 1-7.

1.4 Motivations of this Study

Si NWs have shown their potential for diverse applications as introduced in Sections 1.1 and 1.3. Development of superior performance and highly sensitive NW devices with reproducible and reliable process is essential for this purpose. However, there remain certain distressing issues for either approach of current NWs fabrication as aforementioned. These issues may hinder practical applications and manufacturing of NW devices.

Here, we propose a new technique that could potentially resolve the shortcomings mentioned above. Our approach, albeit based on “top-down” approach, involves only mature and low-cost process skills. Since it could be easily realized using state-of-the-art IC processing, this new scheme is thus very suitable and promising for future practical manufacturing. In this approach, the poly-Si NWs are formed on the sidewall of a step structure after deposition and anisotropic etching

steps. The NWs are then employed as the channel portion of the FET device. The overall process sequence is very simple. In addition to the straightforward fabrication process, this new scheme also benefits by the following advantages,

1. Controllable NW's size－feature size of NWs is related to the thickness of deposited film and could be well controlled.

2. Precise positioning and alignment of the NWs.

3. Reliable source and drain (S/D) to channel contacts.

4. Formations of S/D and NW channels in a self-aligned manner.

5. Easy to achieve CMOS integration－both p- and n-type devices are easily fabricated.

However, one of the potential issues for the proposed approach is probably the structural defects contained in the channel layer due to polycrystalline nature, which could be the noise source and contribute to the leakage current. Two strategies are thus adopted to cope with the issue. One is to passivate the defects by employing the well-known hydrogenation post-treatment [1.31]. The other is to promote the crystallinity of the NWs by implementing MILC technique. Many studies have shown that MILC [1.32] can dramatically improve crystallinity of the Si layer and enlarge grain size to about one micrometer. If the MILC grain is large enough and comparable

to the size of NW channel, monocrystalline-like Si NW could be obtained and thus boost the device performance.

In addition to improving the film crystal property, an alternative strategy is to uplift the gate controllability over the channel with the adoption of multiple-gated (MG) configuration. This is because potential barriers provoked by the grain boundary defects can be modulated by the gate control. Based on the developed poly-Si NW structure, MG architecture could be easily achieved by a slight modification in device manufacture and mask design. Besides, the multiple gates are capable of independently operating for adjusting the threshold voltage of NW channels. Accordingly, the doping process could be skipped and the concern of dopant distribution in the NWs is thus lessened.

1.5 Organizations of the Thesis

This dissertation comprises of six chapters. Chapter 1 describes the background and purpose of this study. Chapter 2 introduces the main architecture of the devices proposed in this work. Chapter 3 and Chapter 4 investigate and analyze some constructive methods to improve the device performance. In Chapter 5, we will discuss the feasibility of poly-Si NWs for practical sensing applications. And all the efforts and results are concluded in Chapter 6. The detailed content of each chapter is

described as follows.

In Chapter 1, an overview of NWs is described, together with a brief introduction of low-temperature crystallization techniques and NW-based sensor devices. To overcome the issues encountered in the present NWs' preparation methods, a novel Si NW fabrication scheme is thus proposed as the main motivation of this study. Then, the organization of the thesis is presented in the last section.

In Chapter 2, the structure and fabrication process of the poly-Si NW devices are specified. The basic electrical behaviors are then examined. To address the off-state issues found in the original design of the devices, several improvement methods are exploited, including structural and process modification. Afterwards, plasma post-treatment and MILC technique are employed to passivate the microstructural defects and to enhance the crystallinity of the NWs, respectively. Furthermore, MILC coupled with post high-temperature annealing will lead to excellent device performance.

In Chapter 3, the influence of structure and process parameters on MILC mechanism is investigated for better understanding of MILC-enhanced Si NWs. In the implementation of MILC process, it is shown that the arrangement of seeding window plays an important role in affecting the resulting film quality and the device

performance. In addition, the dimension of NWs also affects the effectiveness of MILC improvement. TEM analyses are extensively used in this chapter to inspect the microscopic properties.

In Chapter 4, a novel MG TFT with poly-Si NW channels is fabricated using a straightforward manner. The combination of an ultra-thin channel layer with MG structure is expected to further improve the device performance. In the proposed transistors, poly-Si NWs are formed in a self-aligned manner and precisely positioned with respect to the side-gate, top-gate and bottom-gate, resulting in much stronger gate controllability over the NW channels, thus dramatically boosting the device performance over conventional single-gated TFTs. Another great benefit of such scheme is that the independently applied gate bias could be utilized to adjust the threshold voltage of NW channels in a reliable manner, making it very favorable for practical applications.

In Chapter 5, poly-Si NWs are employed to study their feasibility and capability for chemical and biological sensing applications. Due to easy preparation and fabrication on a number types of substrates, poly-Si NW devices could reduce production cost and be favorable for constructing on versatile platforms. However, poly-Si suffers from inherent defects in inter/intra grains which would impede carrier transport. This might make poly-Si seemingly improper for sensor applications

because of the issue of sensitivity degradation. In this work, we show that such concern could be alleviated as long as the measurement is carried out in an aqueous solution, and possible mechanism for this phenomenon is also addressed. Under all sensing measurements, the NW devices are encapsulated in a microfluidic system, which will provide safe and reliable environment for chemical and biological reactions on the NWs. As a result, the sensing capability of poly-Si NW device for detection of pH-value and biomolecules could be performed and investigated.

Finally, contributions and conclusions of this dissertation as well as recommendations for future research are given in Chapter 6.

References

[1.1] J. Hu, T. W. Odom and C. M. Lieber, "Chemistry and physics in one dimension: synthesis and properties of nanowires and nanotubes," *Acc. Chem. Res.*, **32**, 435 (1999).

[1.2] H. C. Lin and S. M. Sze, "Nanoelectronic technology: in search of the ultimate device structure," *Future Trends in Microelectronics: the Nano Millennium*, S. Luryi, J. M. Xu, and A. Zaslavsky, eds., pp.4-14 (New York: Wiley 2004).

[1.3] B. Doyle, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios and R. Chau, "Tri-Gate fully-depleted CMOS transistors: fabrication, design and layout," *Symp. VLSI Tech. Dig.*, 133, June 10-12 (2003).

[1.4] X. Duan, Y. Huang and C. M. Lieber, "Nonvolatile memory and programmable logic from molecule-gated nanowires," *Nano Lett.*, **2**, 487 (2002).

[1.5] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles and J. L. Goldma, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature*, **425**, 274 (2003).

[1.6] Y. Cui, Q. Wei, H. Park and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*,

293, 1289 (2001).

[1.7] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu, and C. C. Huang *et al*, "5 nm-gate nanowire FinFET," *Symp. VLSI Tech. Dig.*, 196, June 15-17 (2004).

[1.8] H. C. Lin, M. F. Wang, F. J. Hou, H. N. Lin, C. Y. Lu, J. T. Liu and T. Y. Huang, "High-performance p-channel schottky-barrier SOI FinFET featuring self-aligned PtSi source/drain and electrical junctions," *IEEE Electron Device Lett.*, **24**, 102 (2003).

[1.9] J. Gu, C. P. Jen, Q. Wei, C. Chou and F. Zenhausern, "Mask fabrication towards sub-10 nm imprint lithography," *Proc. SPIE*, **5751**, 382 (2005).

[1.10] H. L. Chen, C. H. Chen and F. H. Ko, "Thermal-flow techniques for sub-35 nm contact-hole fabrication in electron-beam lithography," *J. Vac. Sci. Technol. B*, **20**, 2973 (2002).

[1.11] F. H. Ko, H. C. You, T. C. Chu, T. F. Lei, C. C. Hsu and H. L. Chen, "Fabrication of sub-60-nm contact holes in silicon dioxide layers," *Microelectronic Engineering*, **73-74**, 323 (2004).

[1.12] Y. K. Choi, Ji. Zhu, J. Grunes, J. Bokor and G. A. Somorjai, "Fabrication of sub-10-nm silicon nanowire arrays by size reduction lithography," *J. Phys.*

Chem. B, **107**, 3340 (2003).

[1.13] A. M. Morales and C. M. Lieber, "A laser ablation method for the synthesis of crystalline semiconductor nanowires," *Science*, **279**, 208 (1998).

[1.14] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan and K. C. Saraswat, "Germanium nanowire field-effect transistors with SiO_2 and high-κ HfO_2 gate dielectrics," *Appl. Phys. Lett.*, **83**, 2432 (2003).

[1.15] N. Wang, Y. F. Zhang, Y. H. Tang, C. S. Lee and S. T. Lee, "SiO_2-enhanced synthesis of Si nanowires by laser ablation," *Appl. Phys. Lett.*, **73**, 3902 (1998).

[1.16] X. Duan and C. M. Lieber, "General synthesis of compound semiconductor nanowires," *Adv. Mat.*, **12**, 298 (2000).

[1.17] X. Duan, Y. Huang, Y. Cui, J. Wang and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, **409**, 66 (2001).

[1.18] Y. Huang, X. Duan, Q. Wei and C. M. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," *Science*, **291**, 630 (2001).

[1.19] A. Tao, F. Kim, C. Hess, J. Goldberger, R. He, Y. Sun, Y. Xia and P. Yang, "Langmuir-blodgett silver nanowire monolayers for molecular sensing using surface-enhanced raman spectroscopy," *Nano Lett.*, **3**, 1229 (2003).

[1.20] N. Yamauchi and R. Reif, "Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization: theory, experiments, and thin-film transistor applications," *J. Appl. Phys.*, **75**, 3235 (1994).

[1.21] K. Zellama, P. Germain, S. Squelard, J. C. Bourgoin and P. A. Thomas, "Crystallization in amorphous silicon," *J. Appl. Phys.*, **50**, 6995 (1979).

[1.22] C. Hayzelden and J. L. Batstone, "Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films," *J. Appl. Phys.*, **73**, 8279 (1993)

[1.23] J. L. Batstone and C. Hayzelden, "Microscopic processes in crystallisation," *Solid State Phenom.*, **37-38**, 257 (1994)

[1.24] S. W. Lee, Y. C. Jeon and S. K Joo, "Pd induced lateral crystallization of amorphous Si thin films," *Appl. Phys. Lett.*, **66**, 1671 (1995)

[1.25] J. H. Kim and J. Y. Lee, "Al-induced crystallization of an amorphous Si thin film in a polycrystalline Al/native SiO_2/amorphous Si structure," *Jpn. J. Appl.*

Phys., **35**, 2052 (1996)

[1.26] T. J. Konno and R. Sinclair, "Metal-contact-induced crystallization of semiconductors," *Mater. Sci. Eng. A*, **179**, 426 (1994)

[1.27] S. F. Gong, H. T. G. Hentzell and A. E. Robertsson, "Initial solid-state reactions between crystalline Sb and amorphous Si thin films," *J. Appl. Phys.*, **64**, 1457 (1988)

[1.28] R. T. Tung, J. M. Gibson, D. C. Jacobson and J. M. Poate, "Liquid phase growth of epitaxial Ni and Co silicides," *Appl. Phys. Lett.*, **43**, 476 (1983).

[1.29] A. Yu. Kuznetsov and B. G. Svensson "Nickel atomic diffusion in amorphous silicon," *Appl. Phys. Lett.*, **66**, 2229 (1995)

[1.30] G. J. Chin, "Structural biology: proton/protein transport," *Science*, **293**, 17 (2001)

[1.31] H. C. Cheng, F. S. Wang, and C. Y. Huang "Effects of NH_3 plasma passivation on N-channel polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, **44**, 64 (1997).

[1.32] M. Wang, Z. Meng and Man Wong, "Anisotropic conduction behavior in metal-induced laterally crystallized polycrystalline silicon thin films," *Appl. Phys. Lett.*, **76**, 448 (2000).

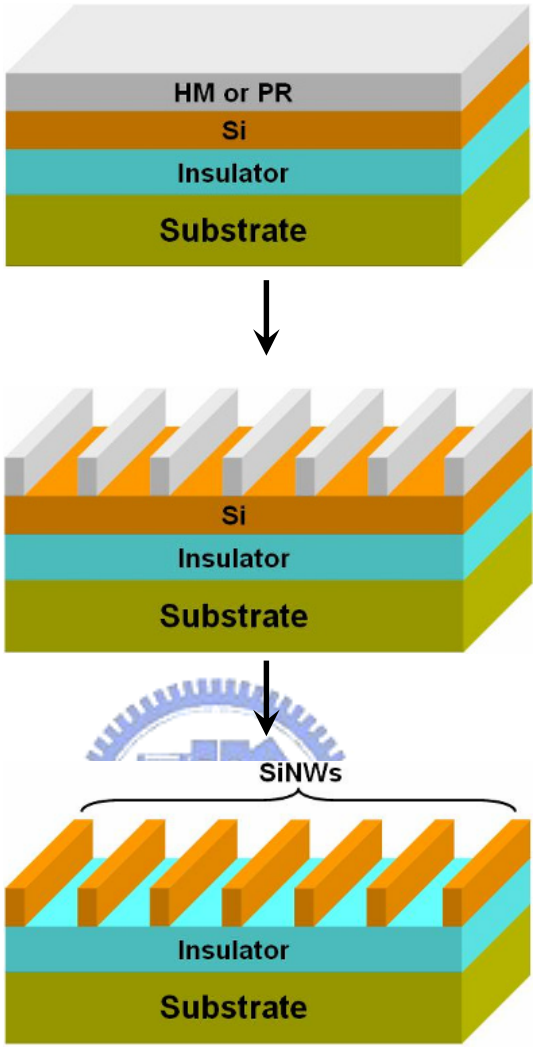


Fig. 1-1 Schematic illustration of Si NWs fabrication on SOI substrate by advanced lithography technique.

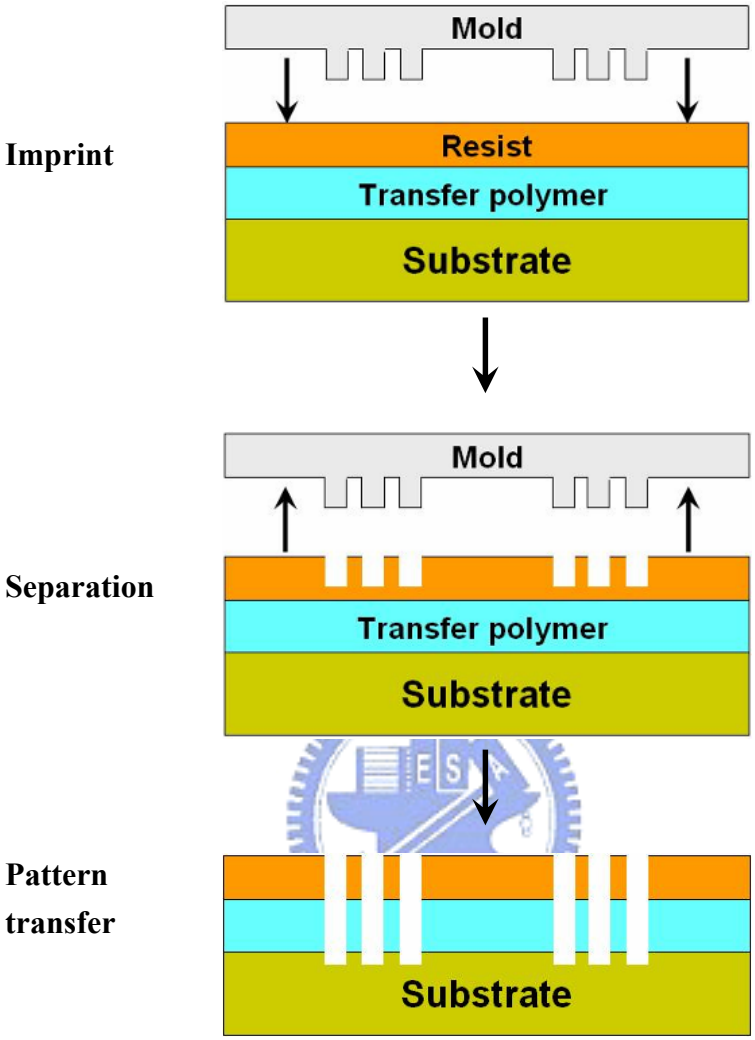


Fig. 1-2 Principle of imprint lithography: 1) mold with nano features is used to physically deform thin layer of resist; 2) mold is separated from the resist after curing; 3) nano patterns in resist are transferred into substrate.

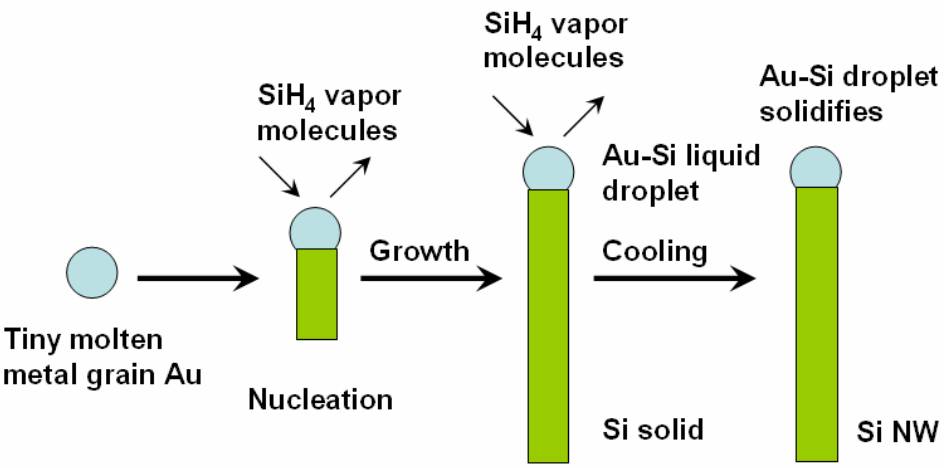


Fig. 1-3 Growth mechanism of nanowire by VLS method.

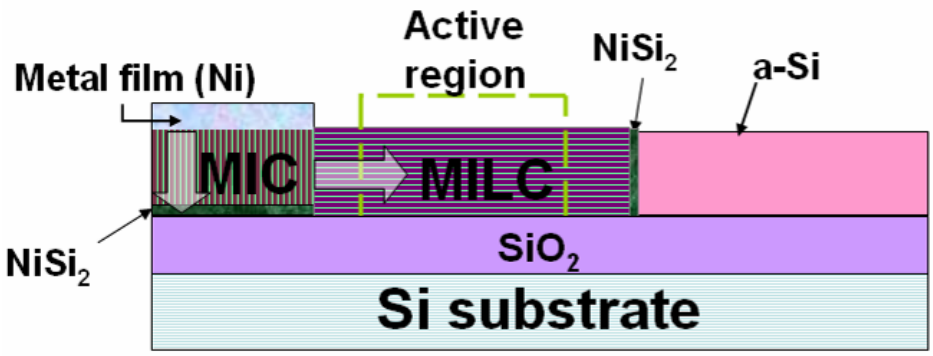


Fig. 1-4 Schematic illustration of the metal-induced crystallization (MIC) and metal-induced lateral crystallization (MILC). The arrows indicate the crystallization direction for each mechanism.

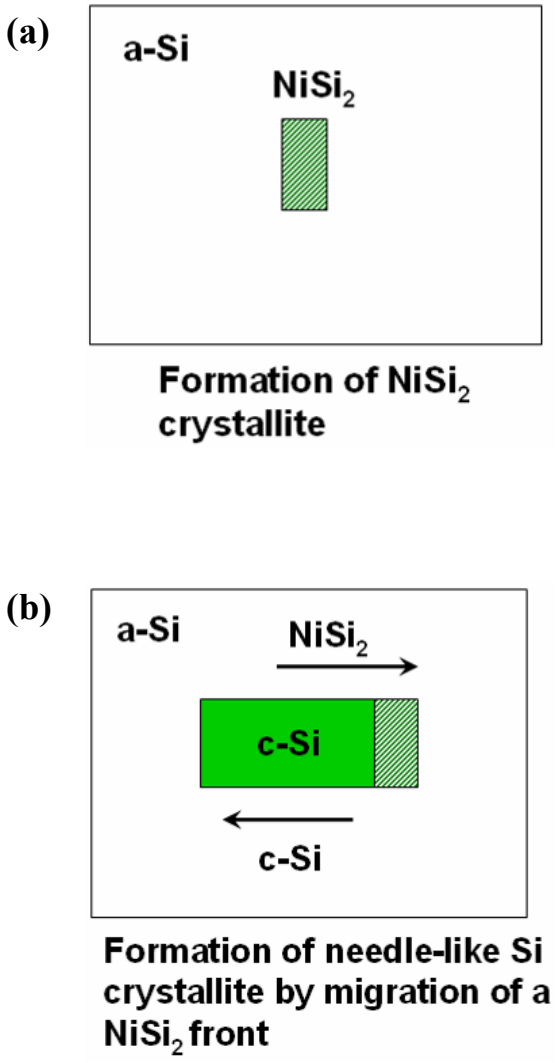


Fig. 1-5 Schematic representation of the formation of (a) $NiSi_2$ precipitate in a-Si network, and (b) c-Si crystallite after the migration of $NiSi_2$.

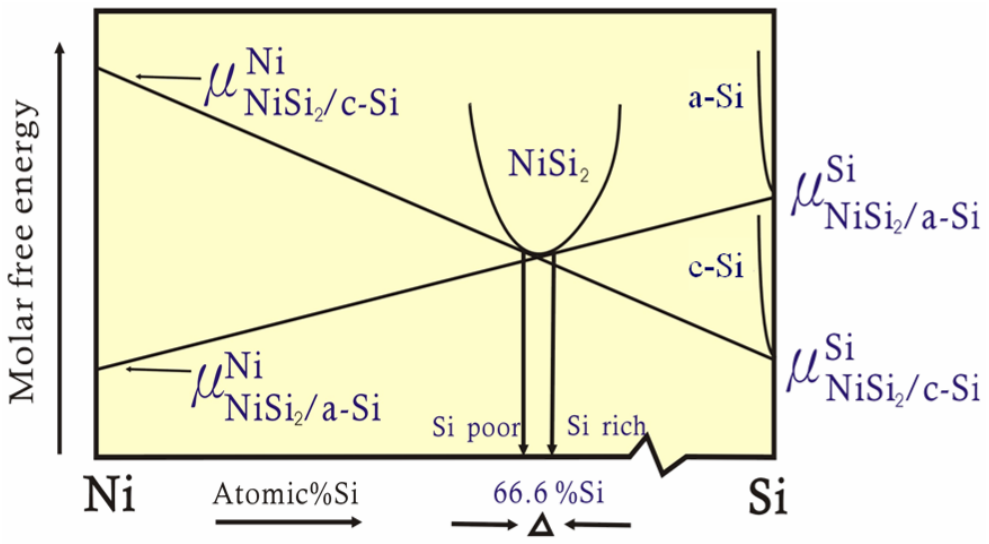


Fig. 1-6 Schematic equilibrium free energy diagram for $NiSi_2$ in contact with a-Si and c-Si.

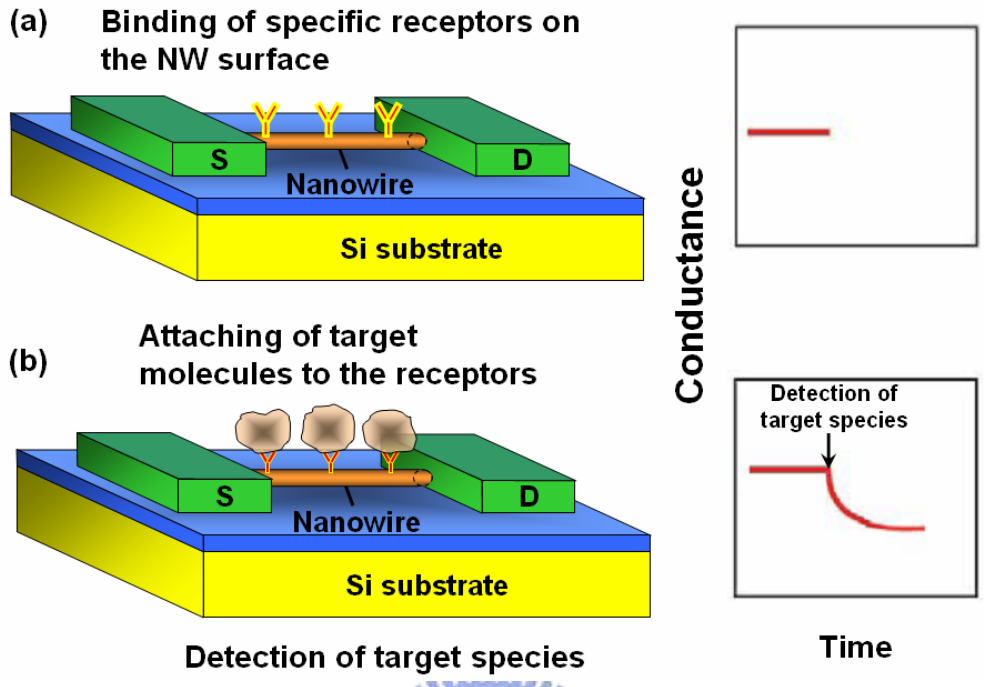


Fig. 1-7 Illustrations of sensing process for a Si NW device. (a) NW's surface is modified with specific receptors and the conductance is recorded. (b) Target species are introduced and attached to the receptors. If the NW device is n-type and the target molecules are negatively charged, then the corresponding conductance is reduced.

Chapter 2

Novel Thin-Film Transistors Featuring Sidewall-Spacer Poly-Si Nanowire Channels

2.1 Introduction

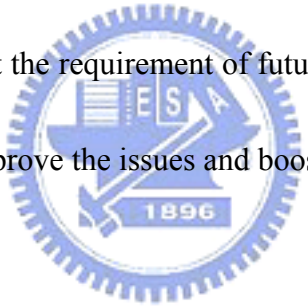
Nanowire (NW) has attracted great interest as essential building blocks for functional devices because of its potential applications in nanoelectronics [2.1, 2.2]. Since the surface-to-volume ratio of a semiconductor wire is inversely proportional to its diameter or feature size, the characteristics of a NW device would be significantly affected by the surface condition during operation. Furthermore, thanks to its tiny body, the gate can exert better control over NW channels and thus effectively suppresses short-channel effects (SCEs) in extremely scaled-down field-effect transistors (FETs) [2.3]. These properties therefore lend NW itself nicely to a number of applications, including NW thin-film transistors (TFTs) [2.1], nano-scale complementary metal-oxide-semiconductor (CMOS) [2.3], memory devices [2.4], large-area electronics [2.1, 2.5], and sensors for sensing chemical or biological species [2.6, 2.7]. Among these applications, the NWs are traditionally prepared by either top-down [2.3, 2.7] or bottom-up approaches [2.1, 2.2, 2.4, 2.5]. The top-down approaches typically utilize advanced optical or e-beam lithography tools to generate

the NW patterns. Although compatible with mass-production, the use of advanced lithography tools with nanometer size resolution is costly. On the other hand, the bottom-up approaches usually employ metal-catalytic growth for preparation of NWs. The later approaches, however, suffer seriously from the difficulty in precisely positioning the device location. Metal contamination and control of structural parameters are additional issues that need to be addressed for practical manufacturing.

Previously, the sidewall spacer formation technique has been proposed to define the nano-scale hardmask (HM) itself, with subsequent etching step to pattern the target materials underneath the HM [2.8]. In contrast, we propose instead to define directly the nano-scale Si lines that serve as the device channel in this work. The top-view layout of the proposed NW device is shown in Fig. 2-1(a), while the cross-sectional view is depicted in Fig. 2-1(b). It features a side-gate configuration with NW channels abutting against the gate. Note that the side-gate could be used to adjust the channel potential, thus controlling the device's switching behavior. In addition, for the sidewall Si layer only the regions between the source and drain are shown and defined as the channel length. Also worth noting that, with large portion of the NW surface exposing to the environment, the surface serves as the sensing site when the device is used as a sensor. After specific immobilization treatment, the receptor agents formed on the surface could selectively detect the target species

contained in the test solutions [2.6, 2.7]. As comparing with other proposed NW approaches (either bottom-up or top-down), our approach presents several advantages comprising very simple fabrication flow [2.9], reliable source/drain (S/D) contacts, and accurate control of NWs' dimensions as well as precise positioning and alignment. In addition, it is also reproducible and suitable for low-cost manufacturing.

In this chapter, a novel TFT structure with sidewall-spacer NW channels is introduced and demonstrated. Though this distinctive scheme profits easy and reliable fabrication process, some distressing parts are revealed and should be addressed. Consequently, in order to meet the requirement of future applications, several feasible approaches are explored to improve the issues and boost device performance.



2.2 Experimental

Since poly-Si film obtained by direct deposition method suffers from smaller grains and defective structure, the poly-Si NW TFTs in this study are fulfilled by crystallizing amorphous Si film into polycrystalline state to achieve better crystal property. Here, the recrystallization methods utilized are solid-phase crystallization (SPC) and metal-induced lateral crystallization (MILC), respectively.

2.2.1 Solid-phase Crystallized Poly-Si NW TFTs

Fig. 2-2(d) shows schematic structure of the proposed NW device. It adopts a side-gate scheme where two NW channels are formed on the sidewall of the gate. S/D regions lying across the gate are defined simultaneously with the formation of NW channels in a self-aligned manner. The key device fabrication steps are illustrated in Fig. 2-2 and 2-3. Briefly, an n^+-poly-Si gate was first formed on a thermally oxidized Si substrate (Fig. 2-2(a)). For better step coverage, tetraethyl orthosilicate oxide (TEOS-SiO_2) was selected to serve as the gate dielectric by low-pressure chemical vapor deposition (LPCVD) system. A 100 nm amorphous Si (a-Si) layer was then deposited on the 40 nm-thick TEOS gate oxide by LPCVD. Next, a SPC treatment was carried out at 600 ^oC in N_2 ambient for 24 hours to transform the a-Si into poly-Si into polycrystalline (Fig. 2-2(b)). Subsequently, S/D dopants were implanted by P_{31}^+ ion beam with a dose of 1 x 10^{15} cm^{-2} at 15 keV and BF_2^+ with 1 x 10^{15} cm^{-2} at 20 keV for n- and p-type transistors, respectively (Fig. 2-2(c)). Note that the implant energy was kept low so that most implanted dopants were located near the top portion of the Si layer. S/D photoresist patterns were then generated by a G-line stepper. Anisotropic plasma dry-etching with Cl_2/HBr etchant was subsequently employed to shape the poly-Si layer. During the etching process, the NW channels were simultaneously formed abutting against the gate (Fig. 2-2(d)), similar to the formation

of sidewall spacers in standard CMOS manufacturing. Note that the NW channels were accomplished in a self-aligned manner with respect to the S/D and remained undoped because the aforementioned implant was done at a low energy so that the implanted dopants do not reach the channel. Afterwards, wafers were capped with a 200 nm-thick TEOS oxide as the passivation layer at 700 ^{o}C, and the S/D dopants were activated in this thermal process. The fabrication was completed after the formation of contact pads using standard metallization steps. It is noteworthy that only four-mask process is required to accomplish the NW TFT.

2.2.2 Metal-induced Lateral Crystallized Poly-Si NW TFTs

In the previous subsection, the NW TFT illustrated was prepared by crystallizing an amorphous Si layer with SPC scheme and the NWs are polycrystalline in nature. The device performance is thus limited by the existence of inter/intra-grain boundary defects. For the purpose of further improving NW crystalline property, a common low-temperature poly-Si (LTPS) process is exploited. Namely, MILC technique is investigated to enhance the device performance in this work.

Basically the fabrication flow follows that described in Section 2.2.1, with the addition of the implementation of MILC process. After formation of the active regions,

the Si layer, unlike SPC-processed split, was still in amorphous state as shown in Fig. 2-4(a). A 100 nm-thick low-temperature oxide (LTO) was then deposited onto the device by plasma-enhanced CVD (PECVD). For MILC purpose, the seeding window was opened in the LTO layer on the source side (Fig. 2-4(b)). Here the source region was defined as the terminal that serves as the grounded source during normal device electrical characterization. Before the MILC treatment, a 5 nm-thick Ni layer was deposited in the window area as the seeding layer. The Ni induced crystallization was carried out at 550 ^{o}C for 16 hours in an N_2 ambient, which also served the dual purpose of dopant activation. The un-reacted Ni was then removed by a mixture of H_2SO_4/H_2O_2 solution. The arrows in Fig. 2-4(c) indicate the induced crystallization directions. After the deposition of a 200 nm-thick passivation oxide layer and opening of contact holes, a standard metallization step was performed to complete the device fabrication. It is evident that the overall process flow is also quite simple and straightforward.

Figs. 2-5(a) and 2-5(b) are optical micrograph (OM) pictures of n- and p-type MILC NW devices, respectively. The portion surrounding the window with different colors indicates the region that has been laterally crystallized. Inside the window, however, the crystallization mechanism is called metal-induced crystallization (MIC), and normally with a lot amount of metal species and smaller grains compared with

that in the MILC region. From Fig. 2-5, MILC rate in p-type film is apparently higher than that in n-type film. This is because Ni acts as a cation (Ni^+) when diffusing in Si. The addition of electron acceptors, such as boron, into the Si layer will generate positive holes, and accordingly Ni atoms can easily give up their outermost electrons leading to lower ionization energy. This also explains why the formation temperature of $NiSi_2$ is lowered down to 250-280 ^oC [2.10], though it is normally above 400 ^oC in the case of intrinsic film. Therefore, the hole-rich environment is conducive to the formation of Ni^+ and enhances the Ni diffusion. On the contrary, higher ionization energy is required to create Ni^+ in the electron-rich environment of an n-type film. Besides, phosphorous and arsenic dopants are known for gettering transition metal elements, and thus tend to trap Ni atoms [2.11]. As a result, the Ni diffusion is retarded. The correlation of MILC rate and dopant type is revealed in Fig. 2-6, where the MILC rate is about 3.41 μm/hr for p-type and 1.72 μm/hr for n-type films.

Fig. 2-7 shows a SEM image taken near the seeding window. It can be seen that the needle-like Si grains protrude from the MILC seeding window, and the width of them could achieve 90 nm. Generally, the size of NW fabricated in our study is smaller than 50 nm in width. As a result, with the combination of our NW device architecture and MILC technique, monocrystalline Si NWs are expected. Moreover, it should also be noted that much smaller grains and more defects are observed in the

MIC region. Hence, device active region is usually constructed in the MILC region rather than MIC area.

2.2.3 Electrical Characterization Methods

First, the extraction method and definition of several important electrical parameters in this dissertation are briefly described. All the measurements are performed by HP 4156A semiconductor parameter analyzer together with Interactive Characterization Software (ICS).

1. Threshold voltage (V_{th})

The threshold voltage (V_{th}) is obtained by the constant current method and defined as the gate voltage (V_G) needed to achieve a specific drain current (I_D). The expression is as follows,

$$V_{th} = V_G \; at \; I_D = \frac{W}{L} \times 100 \, nA \tag{2-1}$$

where W and L are the channel width and length, respectively.

2. Subthreshold slope (S.S.)

This parameter is calculated from the subthreshold current in the weak inversion region, given by

$$S.S. = \frac{\partial V_G}{\partial(\log I_D)} \tag{2-2}$$

3. Field-effect mobility (μ_{FE})

The mobility is derived from the formula of I_D as function of V_G and described as follows,

$$I_D = \frac{W}{L} \cdot C_{ox} \cdot \mu_{FE} \cdot (V_G - V_{th} - \frac{1}{2} V_D) \cdot V_D$$

$$\Rightarrow \mu_{FE} = \frac{L \cdot G_m}{W \cdot C_{ox} \cdot V_D} \tag{2-3}$$

where C_{ox} is the gate oxide capacitance per unit area, and G_m stands for the transconductance given by,

$$G_m = \frac{\partial I_D}{\partial V_G}\bigg|_{V_D = const.} \tag{2-4}$$

Note that the drain current used for the extraction is divided by two because of the two effective conduction channels contributed to the current.

4. ON/OFF current ratio (I_{ON}/I_{OFF})

I_{ON} and I_{OFF} are determined from the I_D-V_G curves, where I_{ON} is chosen as the maximal I_D and I_{OFF} is the minimal one.

Note that all the parameters are extracted from the I_D versus V_G characteristics operated in the linear regime, except for the I_{ON}/I_{OFF} which is in the saturation regime.

2.3 Results and Discussions

2.3.1 Fabricated Device Structure

Major benefits of the proposed scheme are accurate positioning of NWs and reliable contacts between NW and S/D regions. Fig. 2-8 is the SEM image of a fabricated NW device showing such features. In addition, the dimension of NW could be effectively controlled by utilizing such sidewall-spacer scheme [2.12]. Fig. 2-9(a) shows cross-sectional TEM of the device in the aligned section of Fig. 2-1(a). The channel conduction width and thickness are 56 nm and 54 nm, respectively. By tuning the etching conditions properly, the size of NW can be further scaled down to smaller than 20 nm in both width and thickness as depicted in Fig. 2-9(b). As a result, this unique NW structure appears to be very promising and reliable for NW device fabrication.

2.3.2 Basic Electrical Characteristics of SPC Poly-Si NW TFTs

Fig. 2-10 shows the basic transfer and output characteristics of the SPC poly-Si NW TFT with NW dimension of 38 nm in width and 1μm in length. The ON/OFF current ratio of 10^5 is attained and reasonable for practical application. The undesirable part, however, is the anomalous leakage behavior. This is somewhat

unexpected, as the small volume of NW channels should yield limited leakage paths. The anomalous leakage behavior has been ascribed to process and structural factors causing gate-induced drain leakage (GIDL) current, as described in our previous study [2.13] and will be addressed in Section 2.3.4. For the output characteristics, it is found that I_D increases monotonically with V_D bias. The fine grain structure with grain boundaries presents the potential barrier for carrier transport. The grain boundary potential barrier deceases as the gate voltage is increased, leading to increase of the current and transconductance. Such barrier is also lowered with increasing drain voltage. This effect is called drain induced grain barrier lowering (DIGBL) (Fig. 2-11) [2.14]. As a consequence, I_D in the saturation regime exhibits strong dependence on V_D. This effect could be lessened by passivating defects in poly-Si or improving film crystallinity.

2.3.3 Impacts of Recrystallization and NW Formation Sequence

In the very beginning, the formation of the spacer NWs was designed to be etched before the SPC annealing step to keep dopants off the NWs. However, such process degraded device performance. Fig. 2-12 compares poly-Si NW devices fabricated with SPC performed either before or after NW formation. In the subthreshold and ON regimes, the device with SPC before NWs etching exhibits

better electrical characteristics. This could be ascribed to worse crystalline properties for SPC executing in NW dimension. It is well-known that SPC grains generally depict random orientations and sizes. If crystallization takes place in a confined space, smaller grains should be expected. Moreover, it is demonstrated that surface nucleation rate is much slower than that at the interface [2.15]. Also, the interface between Si NW and oxide is a preferred nucleation site for heterogeneous crystallization, and normally there exists an inevitable native oxide on the Si surface. In this regard, grain growth from the side of NW and gate oxide would compete with that from the bevel edge of NW as sketched in Fig. 2-13. Hence, smaller grains and larger amount of defects are expected in this process. By extracting the defect density (N_t) from $\ln(I_D/V_G)$ vs. $(1/V_G)$ characteristics by Levison methodology [2.16], fewer defects are revealed in the sample with SPC before NW formation, i.e., $N_t = 2.75 \times 10^{12}/cm^2$ compared with $3.18 \times 10^{12}/cm^2$ for SPC after NW formation (Fig. 2-14). This confirms our speculation that processing space for SPC would influence the crystallinity. Furthermore, in the OFF regime, the I_D-V_G curves roughly coincide with each other, implying similar leakage mechanism. This is mainly due to GIDL effect because of the unique layout design of the NW TFT structure and process causing the anomalous high leakage behavior since the thin body of NW should alleviate leakage paths. This mechanism has been demonstrated in the previous work and the

improvement will be addressed in detail in the next subsection.

However, the case of the MILC NW devices shows a reversed phenomenon (Fig. 2-15). For MILC process executed after NW formation, the needle-like grain growth is deliberately confined in a designated space and direction. As revealed in the literature [2.17], wire widths narrower than 30 nm resulted in little lateral crystallization, while for wire widths above 250 nm, multiple grains started to form. This implies only few $NiSi_2$ front could proceed in the NWs and accordingly leaving few Ni trace in the channel. For MILC before NW channels etching, shown in Fig. 2-16, lateral growth radially spreads from the seeding window. There is no NW serving as filter to suppress the amount of $NiSi_2$ front from proceeding, and more dendritic grains exist in the channel region as depicted in Fig. 2-7, rather than aligning parallel to the channel. Also, it is reported that higher Ni concentration stays in the MIC region and the $NiSi_2$ front [2.18]. Therefore, the more dendrite structures in the NW channel, the more Ni residues in it. These factors cause severe leakage behavior and worse subthreshold characteristics for devices with MILC before NW formation, as obviously depicted in Fig. 2-15.

2.3.4 Leakage Reduction in Poly-Si NW TFTs

In the former subsection, anomalous leakage behavior of the SPC poly-Si NW TFTs is found. It has been demonstrated that the major leakage mechanism in this NW TFT is due to severe GIDL mechanism [2.13]. This GIDL effect could be identified with dependence on the extent of gate-to-drain (GD) overlap region under high electric field between the gate and the drain ($|V_{GD}|$) when operating in the OFF regime, as illustrated in Figs. 2-17 and 2-18. The origin of GIDL effect is ascribed to the distinctive doping profile in the drain region. The S/D implantation was purposefully executed at a quite low energy to keep excess dopants off the NW channels. This results in the dopant concentration diminishing toward the interface between poly-Si drain and gate-oxide. When operating in the OFF regime, an increase of $|V_{GD}|$ would cause a depletion region in the n-type drain overlapping the gate. Accordingly, under high electric field condition, the quasi-Fermi level at the channel/oxide interface shifts nearer to the valance band edge. This eventually results in the generation of electron-hole pairs via the electron tunneling from the valance band into the conduction band, i.e., band-to-band (BTB) tunneling or trap-assisted BTB tunneling (Fig. 2-19). It should be emphasized that this mechanism entirely takes place in the Si drain region instead of tunneling through the gate oxide.

The electric field distribution inside the drain terminal that directly accounts for

the GIDL mechanism can be modulated from structural and process aspects, respectively. Thus, two major processing parameters were exploited as follows.

(A) Increasing Dielectric Thickness between Gate and Drain Regions

Since the dielectric has the ability to sustain voltage drop, lower electric field strength could be achieved by increasing its thickness. An effective method for reducing the electrical field strength near the gate and drain overlap region is simply by inserting a thicker dielectric layer between them (denoted as hard mask approach, or HM approach for short), and thus without any change in the original gate-oxide thickness. In this approach, the fabrication process is almost identical to that of the original scheme. The additional step is to deposit a Si_3N_4 layer of 100 nm after deposition of n^+-poly-Si film as the gate material. After that, the process follows that described in Section 2.2.1. The final architecture is shown in Fig. 2-20.

(B) Increasing Drain Dopant Concentration toward Gate

As mentioned above, the doping level determines the position of the Fermi level and influences the depletion width. In this approach, a supplementary ion implantation (denoted as deep I/I approach) was employed to increase the dopant

concentration in the drain region near the gate oxide, which was conducted by the implantation of P_{31}^{+} with a dose of 3 x 13 cm^{-2} at 40 keV, and followed by the S/D I/I. Note that the dopant activation process was performed after the formation of NW channels to prevent deeper diffusion of dopants into the channels. Likewise, the subsequent process follows that described in Section 2.2.1.

Figs. 2-21(a) and 2-21(b) display the off-state I_D-V_G characteristics with various GD overlap area for NW devices with HM and deep I/I, respectively. It is clear to see that the off-currents are comparable and independent of the GD overlap area. Although NWs' dimensions are not identical in these three splits, all off-currents of each device at specific V_{GD} (V_G = V_D = -5 V) were normalized to the minimal overlap ones, and then volume effect should be neglected. Fig. 2-22 shows the normalized current versus GD area for these three splits. The results evidently reveal that such structural and process modifications could effectively alleviate the GIDL effect.

2.3.5 Performance Enhancement of Poly-Si NW TFTs

The NWs were prepared by crystallizing an amorphous Si layer in a furnace (i.e., the so called SPC scheme) and they are polycrystalline in nature. The device performance is thus limited by the existence of inter/intra-grain boundary defects. To

address this issue, we investigate and implement several process techniques to enhance the device performance.

(A) Plasma Hydrogenation

Plasma hydrogenation is the most commonly used method to passivate trap states contained in the poly-Si channel film [2.19, 2.20]. This is because hydrogen atoms can passivate Si dangling bonds and inter/intra grain defects as well as the interface states between poly-Si channel and gate dielectric, and thus improve device performance. In this work, the hydrogenation post-treatment was performed in NH_3 plasma at 300 ^oC after the fabrication of poly-Si NW TFTs. Detailed parameters are illustrated in Table 2-I. The results are shown in Fig. 2-23. Clearly the device performance is greatly improved by the plasma treatment. Note the required treatment time to effectively passivate the defects (~2 hour in Fig. 2-23) is short as compared with that for conventional planar structure (~16 hour) [2.21]. This is attributed to the small volume of the NWs as well as the unique device structure. The device structure in this study leads to shorter H diffusion paths compared with that for conventional planar TFT structure. Fig. 2-24 illustrates possible pathways for hydrogen migration from the gas source to the poly-Si NW TFT and planar TFT, respectively. Also,

hydrogen exhibits faster diffusion in oxide film than poly-Si film [2.22]. Together with these factors, hydrogenation could passivate the defects more efficiently in a much shorter time. However, the electron mobility (50 cm^2/V-sec) after the treatment is still limited by the fine-grain structure of the SPC poly-Si layer. In this regard, improving the crystalline property of NWs is necessary.

(B) Metal-induced Lateral Crystallization (MILC)

In Section 2.3.2, we have preliminarily observed that MILC NW TFT depicts better electrical characteristics than SPC device. Transfer characteristics of SPC and MILC poly-Si TFTs with NW channels are compared in Fig. 2-25. The devices have nominal channel length L = 1 μm and channel width W = 45 nm. The field-effect mobility extracted from maximum transconductance is 252 cm^2/V-sec for the MILC device, which is much higher than 31 cm^2/V-sec of the SPC counterpart. In addition, the MILC TFT has better S.S. (about 0.29 V/dec) and higher ON/OFF current ratio (about 10^7). These results clearly indicate that NW channels formed by MILC are suitable for high performance device applications. We believe this is because the grain is large, needle-like, and parallel to the channel for the MILC device. Fig. 2-26(a) shows the cross-sectional transmission electron microscopy (TEM) image of a

fabricated device with MILC channels. As compared with the SPC sample (Fig. 2-9(a)), in which microtwins and stacking faults exist, the film crystallinity is significantly improved, demonstrating the effectiveness of the MILC process in the NW structures. When the size of the NW channel is shrunk to a dimension comparable to the grain size, a quasi-single-crystalline Si NW could be further obtained [2.17]. For better understanding of detailed crystalline property in the NW channels, Fig. 2-26(b) displays plane-view TEM image of the MILC sample near the seeding window on the test structure. The NW shows long and large grains in it. It is apparent that the grain structure of the MILC NW reflects upon its electrical characteristics.

Fig. 2-27 shows the trap densities (N_t) extracted from the slope of $\ln(I_D/V_G)$ vs. $(1/V_G)$ according to the grain-boundary trap model [2.16]. It can be found that N_t of MILC TFT is about four times smaller than that of SPC TFT. This result further confirms that MILC technique results in much fewer grain boundaries and microstructural defects in the NW channel. It should also be noted that the MILC NW devices with high mobility and ON/OFF ratio could provide favorable conductivity and switching characteristics suitable for high-sensitivity chemical and biological sensor applications.

Though the aforementioned enhancement in device performance is magnificent,

the off-state leakage of the devices remains high despite the MILC treatment. This is likely to be due to potential Ni contamination. The formation of silicide at the grain boundaries during the MILC process has been reported previously [2.23], which would aggravate the leakage. This drawback could be alleviated by adopting the long Ni-offset structure [2.24] or by proper annealing condition [2.23], which will be discussed later. Through further post-treatment (e.g., hydrogenation or high-temperature annealing), further improvement in electrical performance is expected.

(C) Rapid Thermal Annealing (RTA)

To further promote the film quality, a high-temperature post-treatment was performed by RTA at 900 ^{o}C for 30 sec. The results for SPC NW device are shown in Fig. 2-28, in which SPC device without RTA is also plotted for comparison. In the SPC sample, although the characteristics improve after the RTA treatment, the mobility value (80 cm^2/V-sec) is still far behind that of MILC samples either with or without RTA treatment. This indicates that the fine-grain structure of the channels imposes a limit on the performance improvement eventually. On the other hand, RTA leads to a dramatic performance improvement in the MILC samples (Fig. 2-29). It is

reported that the second grain growth for MILC poly-Si takes place at around 800 ^{o}C [2.25]. Other research has shown that crystalline quality is boosted after post-annealing at 900 ^{o}C, and the annealed sample is with a monocrystalline-like structure [2.26]. It is suggested that the RTA treatment helps remove the weak or strained bonds contained in the grains and leads to a better film crystallinity, and is evidenced by the enhanced contrast of the diffraction patterns mentioned above.

The TEM pictures of MILC and SPC poly-Si NWs with RTA treatment are exhibited in Figs. 2-30 and 2-31, respectively. The image reveals that the SPC poly-Si contains a number of microstructural defects, while the crystalline orientation of the grains is random. However, it can be seen that the crystallinity of the MILC sample with RTA is significantly improved and a monocrystalline structure is obtained. The length of the single-crystal Si grain in this picture is about 1 μm, which is comparable to the channel length of the measured device in Fig. 2-29. The selective electron diffraction pattern at the circled region in Fig. 2-30(b) indicates this visible Si NW exhibits monocrystalline structure with <110> orientation. As compared with Figs. 2-26 and 2-31, the grain is much enlarged and some defects are further eliminated. It is noteworthy that electron mobility of the MILC with RTA is up to 550 cm^2/V-s. This value is among the best results reported in the literature [2.18, 2.26]. The important device parameters obtained in this work for n-TFTs are summarized in Table 2-II. The

best performance could be achieved with the combination of MILC and RTA treatments.

In addition, the effect of MILC and RTA technique on the NW devices is also demonstrated for p-TFTs. Fig. 2-32 depicts the comparison of MILC NW p-TFTs with and without RTA post-treatment. For the device without RTA treatment, good electrical characteristics with field-effect mobility of 145 cm^2/V-s and ON/OFF current ratio larger than 10^6 are recorded. However, the leakage currents are not satisfactory. This phenomenon could mainly be ascribed to the trace amount of Ni residues in the devices. Another set of I_D-V_G curves in Fig. 2-32 was measured from a NW device with RTA treatment. As compared with the results just mentioned, superior characteristics are obtained in terms of steeper S.S., higher hole mobility, and larger ON/OFF current ratio. It is believed that the significantly improved electrical properties are mainly due to the formation of single-crystal NW structure indicated in Fig. 2-30. Furthermore, residual Ni in the NW channel could also be expelled during the high temperature treatment, thus further lowering the leakage current [2.23].

The important device parameters acquired in this work are summarized in Table 2-III, along with the reported data for p-channel devices from previous works with MILC [2.27], MILC with high temperature annealing [2.28], excimer laser annealing (ELA) [2.29], NW channels prepared by vapor-liquid-solid (VLS) [2.1], and SOI

substrates [2.29]. As revealed in this table, in the two categories of “high-T” and “low-T” fabrication, the results obtained in this work are among the best values reported in the literature. This demonstrates that the combination of MILC process and the unique NW structure we have developed provides an excellent approach for the fabrication of high-performance Si NW devices.

2.4 Summary

In conclusion, a unique TFT structure with sidewall-spacer NW channels is introduced and investigated. This scheme benefits well-controlled dimension, accurate positioning and alignment of NWs as well as reliable S/D contacts. In addition, the approach is reproducible and suitable for low-cost manufacturing.

To meet the performance demand required for future practical applications, the basic electrical characteristics of the proposed poly-Si NW TFT were first studied. Reasonable on-state property but with inefficient off-state behavior was found for general SPC recrystallization process. These results are attributed to fine grains and microstructural defects in the SPC Si NW channels. In addition, non-optimum doping profile and device structure could aggravate GIDL currents. For the purpose of mending such issues, several feasible techniques and modification methods were

implemented.

To address the anomalous off-state leakage current, alterations from structural and process aspects were exploited. One approach is to decrease the effective vertical electric field strength in the drain region by inserting a thick HM between the gate and the drain. The other is by adding a deep I/I to increase the drain dopant concentration toward the gate, thus reducing the depletion width. With these modifications, severe GIDL effect was greatly alleviated.

In order to improve the inherent poor crystalline properties of poly-Si, plasma hydrogenation treatment and MILC technique were employed to passivate the defects and promote NWs' crystallinity, respectively. Significant boost of the device performance was obtained especially for MILC Si NW devices. Due to the nature of the large MILC grain combined with appropriate NW channel dimension, defective crystallinity was thus greatly suppressed. The fabricated devices exhibit large on-current, high I_{ON}/I_{OFF} ratio, low S.S., and favorable output characteristics. The extracted effective trap density and mobility as well as TEM analyses further confirm that fewer defects and good crystallinity in the NW channels are indeed achieved by MILC. In addition, we also found the sequence of recrystallization and NW channel formation affects the device performance. Reversed effect for SPC and MILC processing was revealed due to the different crystallization mechanism in these two

techniques.

To eliminate the microstructural defects and drive residual Ni out off the channel region, the MILC NW devices with subsequent RTA treatment exhibit dramatic performance improvement. The TEM images reveal single-crystal Si NW channel is acquired. The highest electron mobility (550 cm^2/V-s) and hole mobility (230 cm^2/V-s) achieved in this work are among the best for NW and poly-Si devices ever reported in the literature.

In short, with the proposed improvement techniques and process modification investigated in this chapter, the proposed Si NW device with high performance and simple manufacturing procedure appears to be highly promising for future practical manufacturing and applications.

References

[2.1] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles and J. L. Goldma, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature,* **425**, 274 (2003).

[2.2] Y. Cui and C. M. Lieber, "Functional nanoscale electronic devices assembled using silicon nanowire building blocks," *Science*, **291**, 851 (2001).

[2.3] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu and C. C. Huang *et al*, "5 nm-gate nanowire FinFET," *Symp. VLSI Tech. Dig.*, 196, June 15-17 (2004).

[2.4] X. Duan, Y. Huang and C. M. Lieber, "Nonvolatile memory and programmable logic from molecule-gated nanowires," *Nano Lett.*, 2, **487** (2002).

[2.5] M. C. McAlpine, R. S. Friedman, S. Jin, K. H. Lin, W. U. Wang and C. M. Lieber, "High-performance nanowire electronics and photonics on glass and plastic substrates," *Nano Lett.*, **3**, 1531 (2003).

[2.6] Y. Cui, Q. Wei, H. Park and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, **293**, 1289 (2001).

[2.7] Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka and R. S. Williams, "Sequence-specific label-free DNA sensors based on silicon nanowires," *Nano Lett.*, **4**, 245 (2004).

[2.8] Y. K. Choi, Ji. Zhu, J. Grunes, J. Bokor and G. A. Somorjai, "Fabrication of sub-10-nm silicon nanowire arrays by size reduction lithography," *J. Phys. Chem. B*, **107**, 3340 (2003).

[2.9] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee and Y. S. Yang, "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel," *IEEE Electron Device Lett.*, **26**, 643 (2005).

[2.10] S. W. Lu, C. W. Nieh and L. J. Chen, "Epitaxial growth of $NiSi_2$ on ion-implanted silicon at 250–280 °C," *Appl. Phys. Lett.*, **49**, 1770 (1986).

[2.11] T. Ma and M. Wong, "Dopant and thickness dependence of metal-induced lateral crystallization of amorphous silicon films.pdf," *J. Appl. Phys.*, **91**, 1236 (2002).

[2.12] C. J. Su, H. C. Lin, H. H. Tsai1, T. Y. Huang and W. N. Ni, "Fabrication and characterization of poly-Si nanowire devices with performance enhancement techniques," *IEEE Int'l Symp. VLSI-TSA,* 120, April 23-25 (2007).

[2.13] H. C. Lin, M. H. Lee, C. J. Su and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels," *IEEE Trans. Electron Devices*, **53**, 2471 (2006).

[2.14] H. L. Chen and C. Y. Wu, "A new model considering the impact-ionization effect initiated by the DIGBL current for the intrinsic n-Channel poly-Si TFT's," *IEEE Trans. Electron Devices*, **46**, 722 (1999).

[2.15] M. K. Ryu, S. M. Hwang, T. H. Kim, K. B. Kim and S. H. Min, "The effect of surface nucleation on the evolution of crystalline microstructure during solid

phase crystallization of amorphous Si films on SiO_2," *App. Phys. Lett.*, **71**, 3063 (1997).

[2.16] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.* **53**, 1193 (1982).

[2.17] J. Gu, S. Y. Chou, N. Yao, H. Zandbergen and J. K. Farrer, "Single-crystal Si formed on amorphous substrate at low temperature by nanopatterning and nickel-induced lateral crystallization," *Appl. Phys. Lett.,* **81**, 1104 (2002).

[2.18] M. Wong, Z. Jin, G. A. Bhat, P. C. Wong and H. S. Kwok, "Characterization of the MIC/MILC interface and its effects on the performance of MILC thin-film transistors," *IEEE Trans. Electron Devices*, **47**, 1061 (2000).

[2.19] H. C. Cheng, F. S. Wang and C. Y. Huang "Effects of NH_3 plasma passivation on N-channel polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, **44**, 64 (1997).

[2.20] F. S. Wang, M. J. Tsai and H. C. Cheng, "The effects of NH_3 plasma passivation on polysilicon thin-film transistors," *IEEE Electron Device Lett.*, **16**, 503 (1995).

[2.21] I. W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis and A. Chiang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Lett.*, **12**, 181 (1991).

[2.22] W. B. Jackson, N. M. Johnson, C. C. Tsai, L. W. Wu, A. Chiang and D. Smith, "Hydrogen diffusion in polycrystalline silicon thin films," *Appl. Phys. Lett.*, **61**, 1670 (1992).

[2.23] C. K. Chan, C. F. Cheng and M. Chan,"Effects of dopants on the electrical behavior of grain boundary in metal-induced crystallized polysilicon film," *IEEE Trans. Electron Devices*, **52**, 1917 (2005).

[2.24] G. B. Kim, Y. G. Yoon, M. S. Kim, H. Jung, S. W. Lee and S. K. Joo, "Electrical characteristics of MILC poly-Si TFTs with long Ni-offset structure," *IEEE Trans. Electron Devices*, **50**, 2344 (2003).

[2.25] G. Liu and S. J. Fonash, "Polycrystalline silicon thin film transistors on Corning 7059 glass substrates using short time, low-temperature processing," *Appl. Phys. Lett.*, **62**, 2554 (1993).

[2.26] H. Wang, M. Chan, S. Jagar, Poon, Vincent M. C., M. Qin, Y. Wang and P. K. Ko, "Super thin-film transistor with SOI CMOS performance formed by a novel grain enhancement method," *IEEE Trans. Electron Devices*, **47**, 1580 (2000).

[2.27] Z. Meng, M. Wang and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, **47**, 404 (2000).

[2.28] Y. Lee, S. Bae and S. J. Fonash, "High-performance nonhydrogenated nickel-induced laterally crystallized p-channel poly-Si TFTs," *IEEE Electron Device Lett.*, **26**, 900 (2005).

[2.29] Y. Nakazaki, G. Kawachi, M. Jyumonjiy, H. Ogawaz, M. Hiramatux, K. Azuma, T. Warabisako and M. Matsumura, *Jpn. J. Appl. Phys.*, **45**, 1489 (2001).

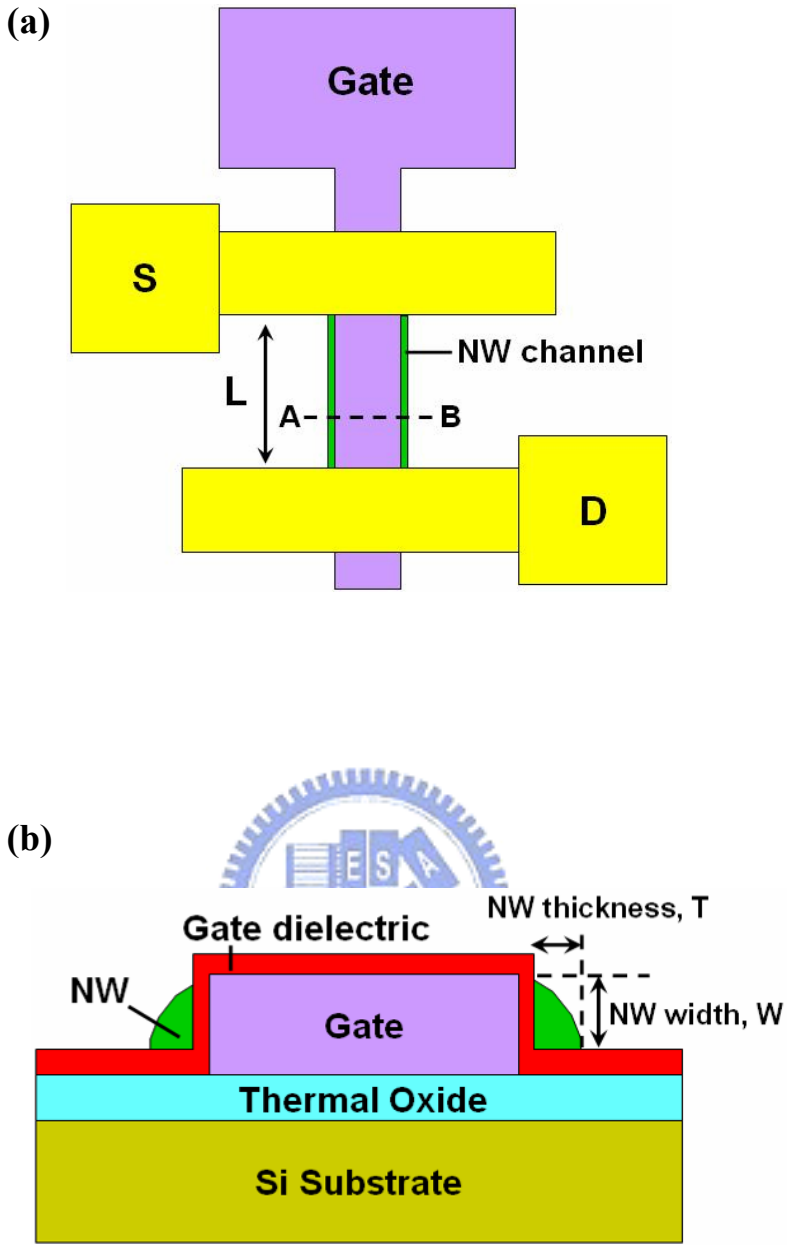


Fig. 2-1 (a) Top view of the proposed NW device, where channel length is defined as the spacing between source and drain, (b) cross-sectional view of the device along A-B direction in (a), featuring the NWs with sidewall spacer structure. Definitions of NW width and thickness are also illustrated.

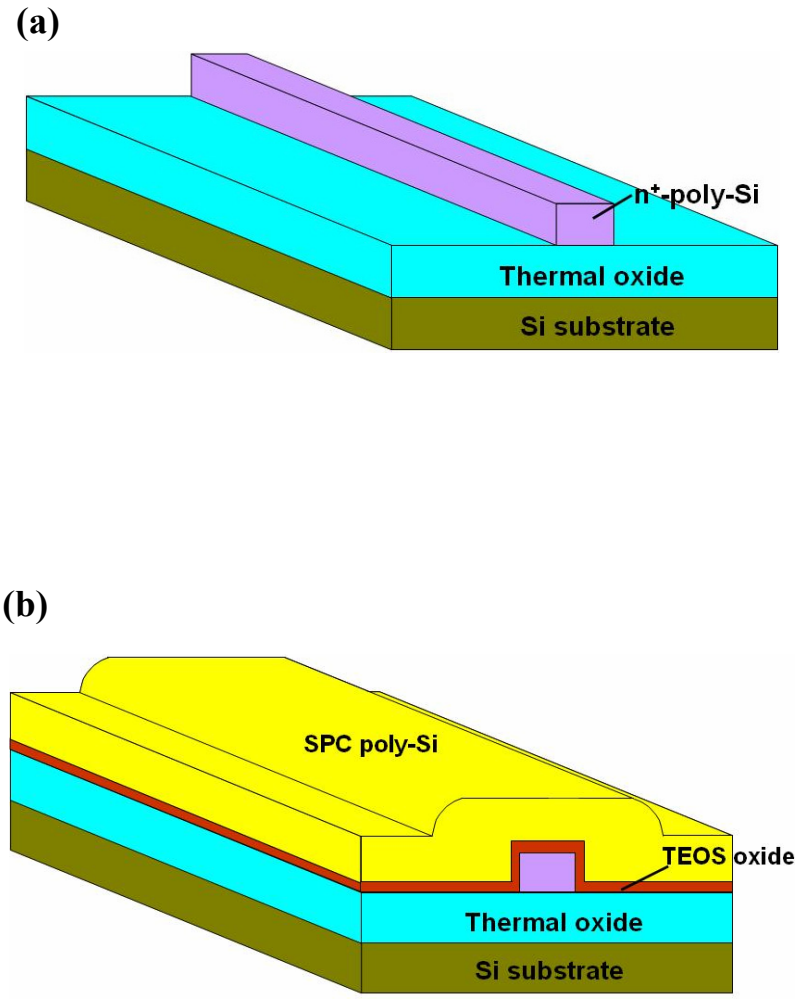


Fig. 2-2 Diagrams of major fabrication steps of the SPC poly-Si NW TFT. (a) Formation of n^+-poly-Si gate on an oxidized Si substrate. (b) Deposition of the gate oxide, followed by solid-phase crystallized (SPC) poly-Si layer. (Continued)

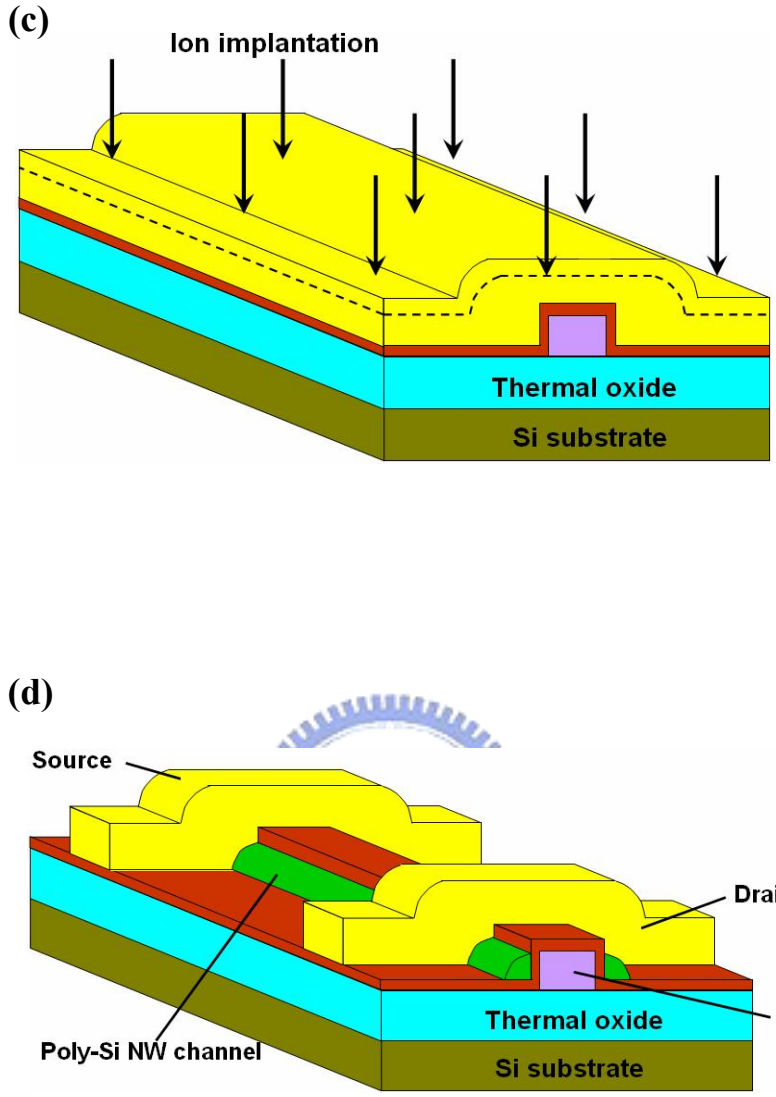


Fig. 2-2 (c) Low-energy S/D ion implantation into the poly-Si layer. The dashed contour indicates the projected range of ion implantation, which is located in the top portion of Si layer. (d) Schematic structure of the fabricated poly-Si NW TFT.

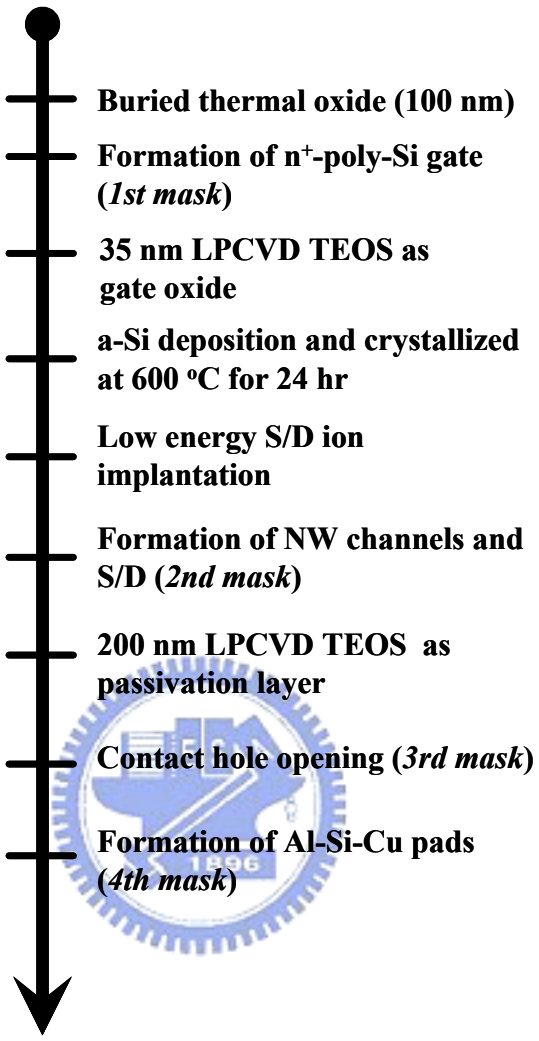


Fig. 2-3 Key fabrication flow of the poly-Si NW TFT. Only four masks are required in the whole process.

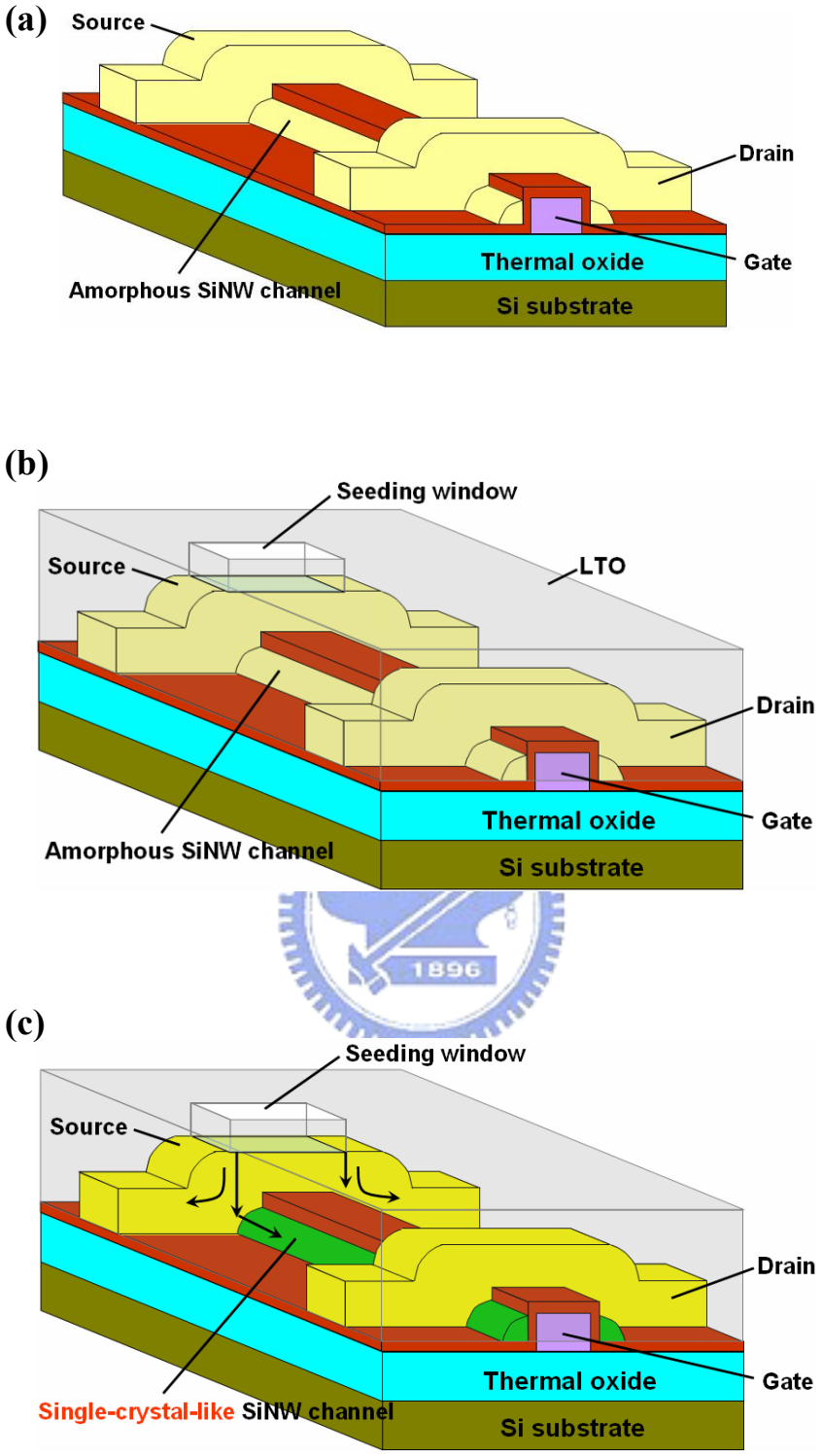


Fig. 2-4 Diagrams of major fabrication steps of the MILC poly-Si NW TFT. (a) Formation of a basic amorphous Si NW TFT. (b) Deposition of LTO and patterning the seeding window. (c) Schematic device structure after MILC annealing. The arrows indicate crystallization directions.

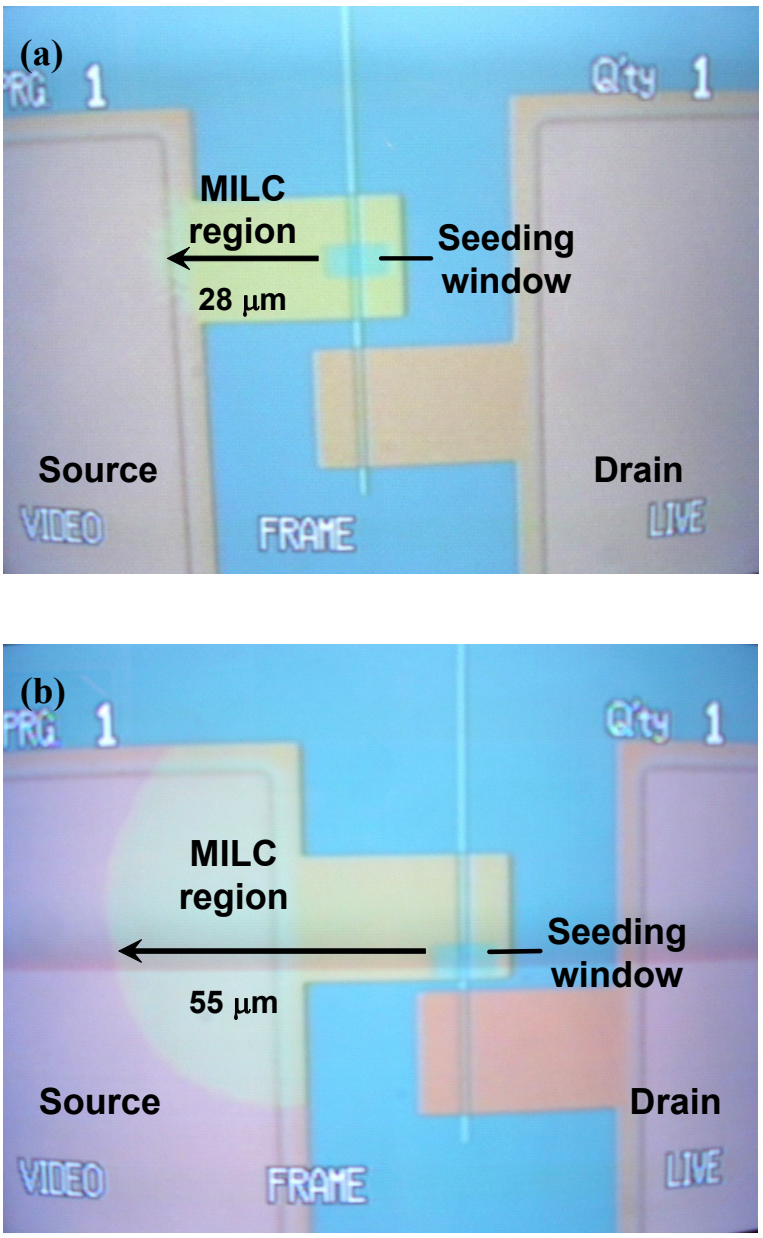


Fig. 2-5 Optical micrograph (OM) photos of (a) n-type and (b) p-type MILC samples annealing at 550 ^{o}C for 16 hours.

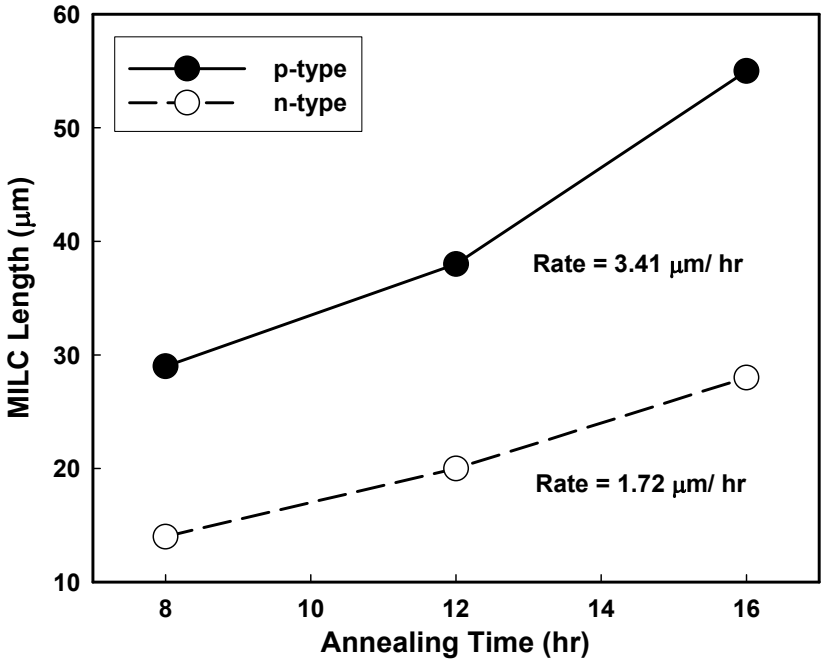


Fig. 2-6 MILC rate for n- and p-type doped poly-Si films.

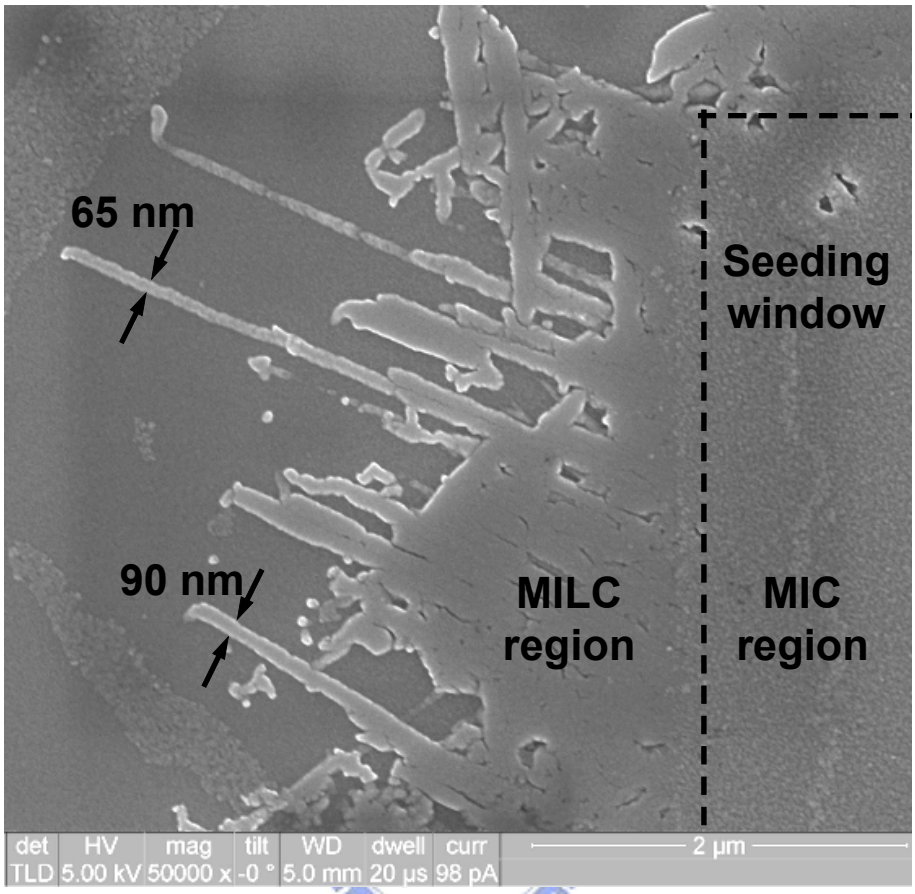


Fig. 2-7 SEM image of MILC sample near the seeding window. Secco etching was used to remove most of amorphous Si.

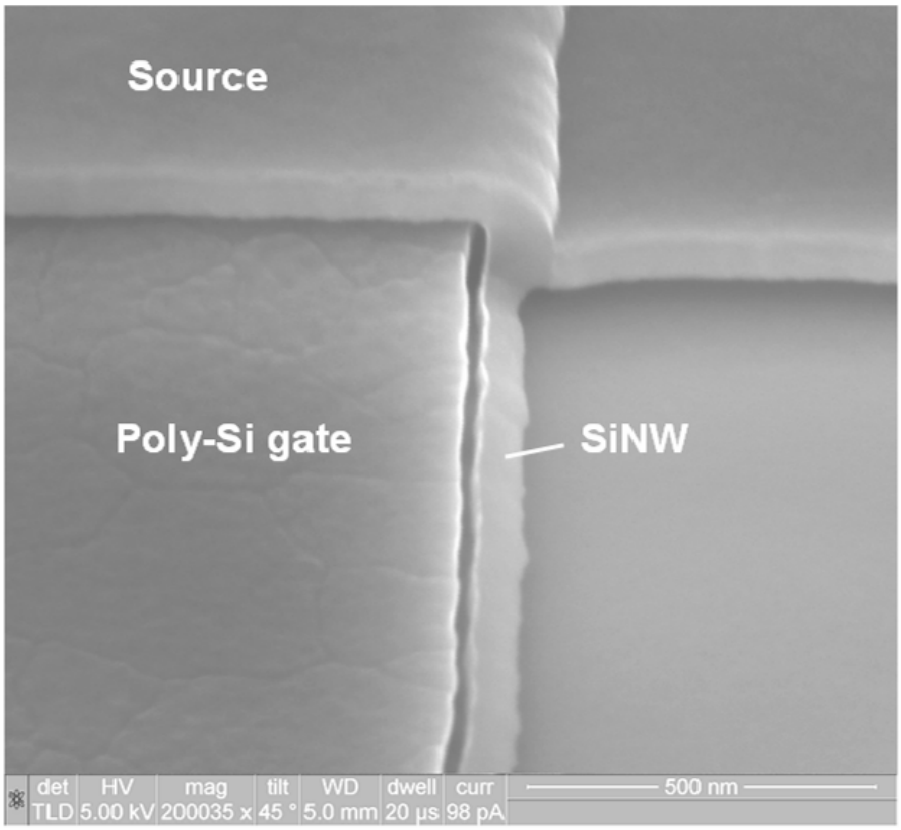


Fig. 2-8 SEM image shows the accurate alignment of NW channel with gate and reliable contact with source region.

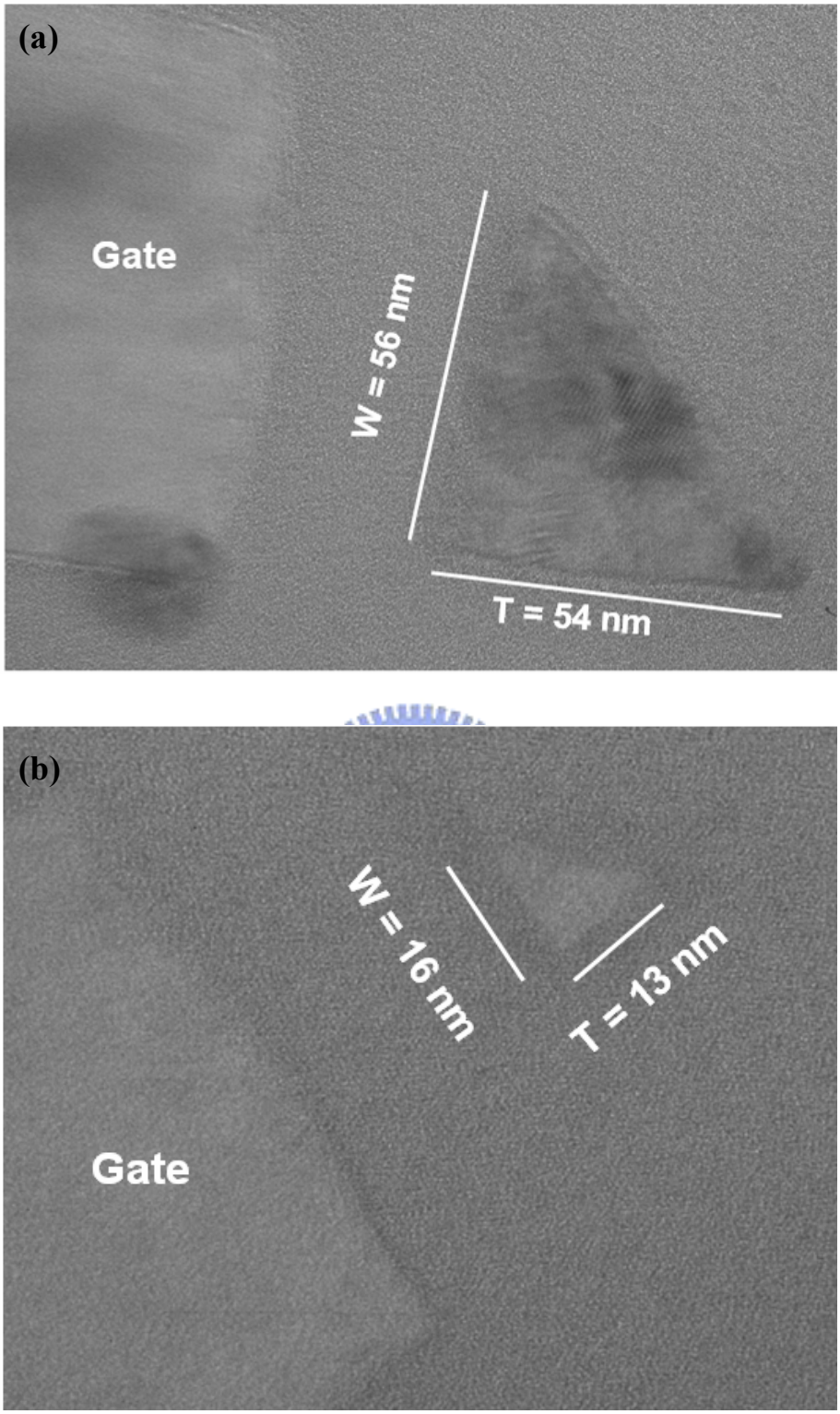


Fig. 2-9 TEM images of fabricated poly-Si NW TFTs. (a) NW size is 56 nm by 54 nm.

(b) NW dimension is 16 nm by 13 nm.

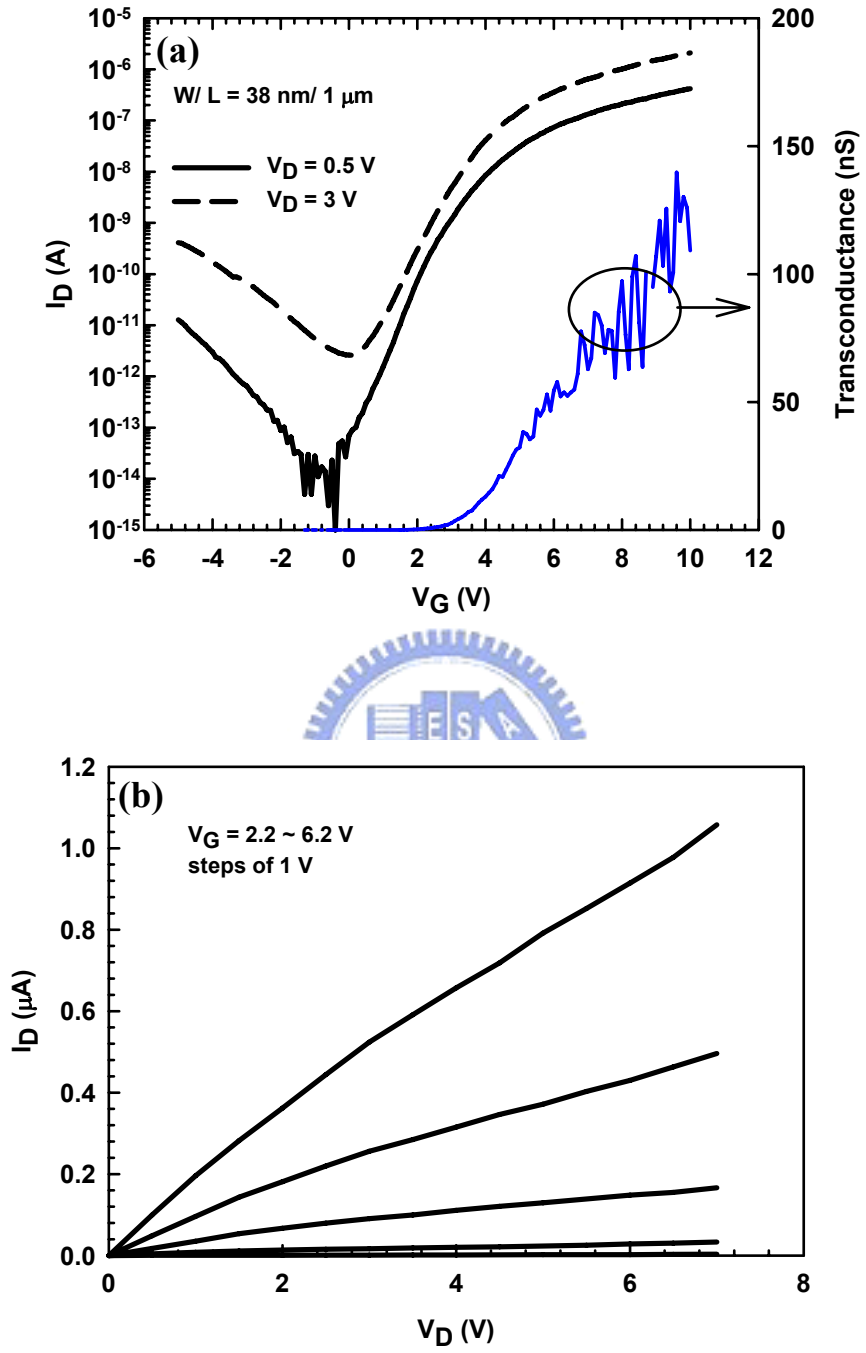


Fig. 2-10 (a) Typical transfer and (b) output characteristics of the SPC poly-Si NW TFT.

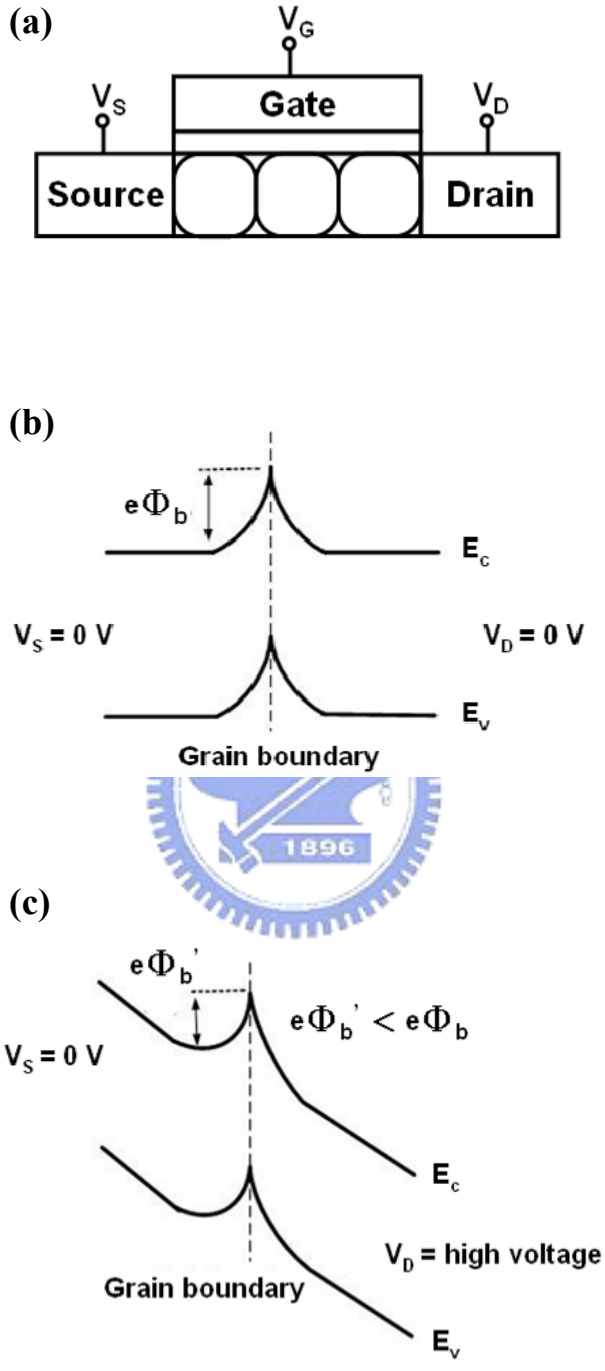


Fig. 2-11 (a) Cross-sectional view of a poly-Si TFT, and potential distribution around the grain boundary (b) without and (c) with lateral electric field.

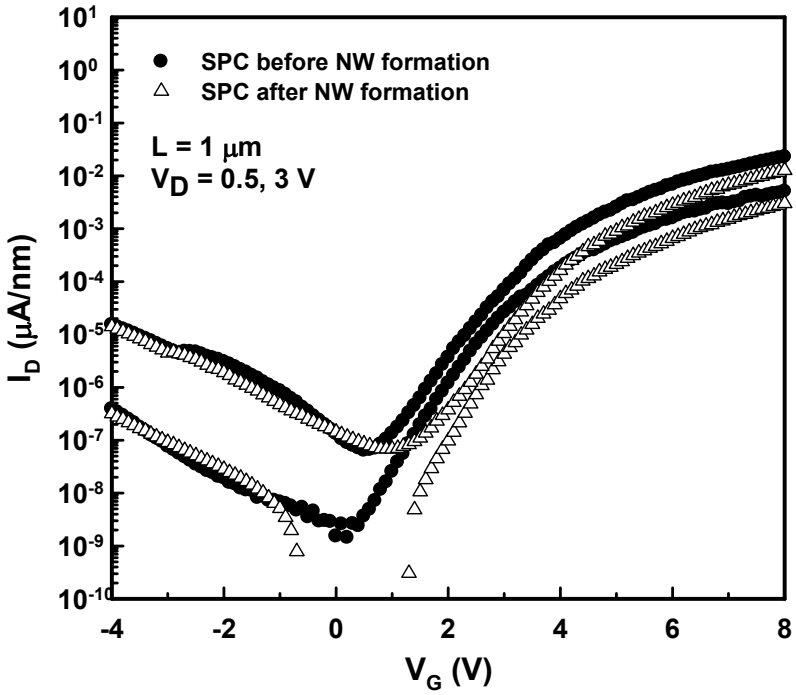


Fig. 2-12 Transfer characteristics of poly-Si NW devices for SPC before/after NW formation.

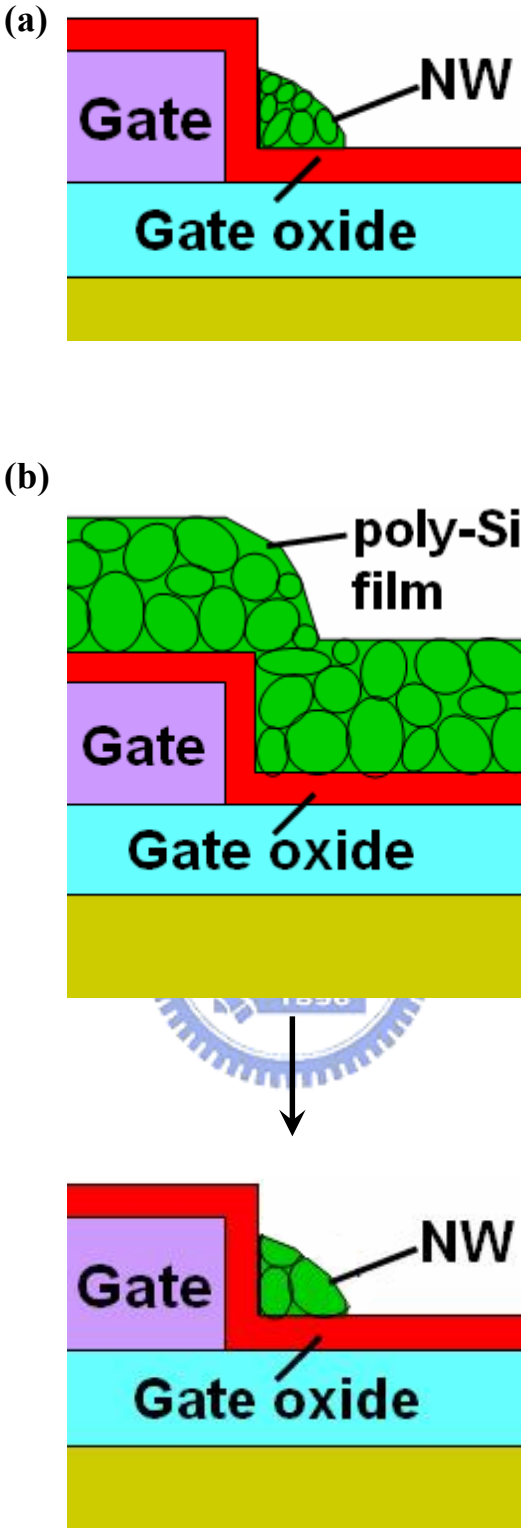


Fig. 2-13 Schematic correlation between poly-Si NW crystal property and SPC process for SPC performed (a) after NW formation, and (b) before NW formation.

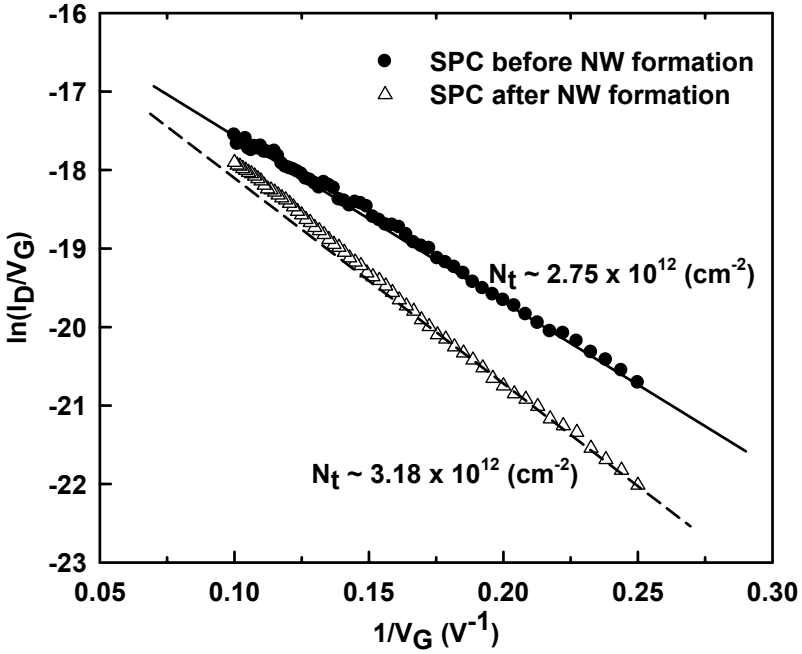


Fig. 2-14 Plot of $\ln(I_D/V_G)$ vs. $(1/V_G)$ and the extracted effective trap density of SPC poly-Si NW TFT. I_D was measured at V_D = 0.5V.

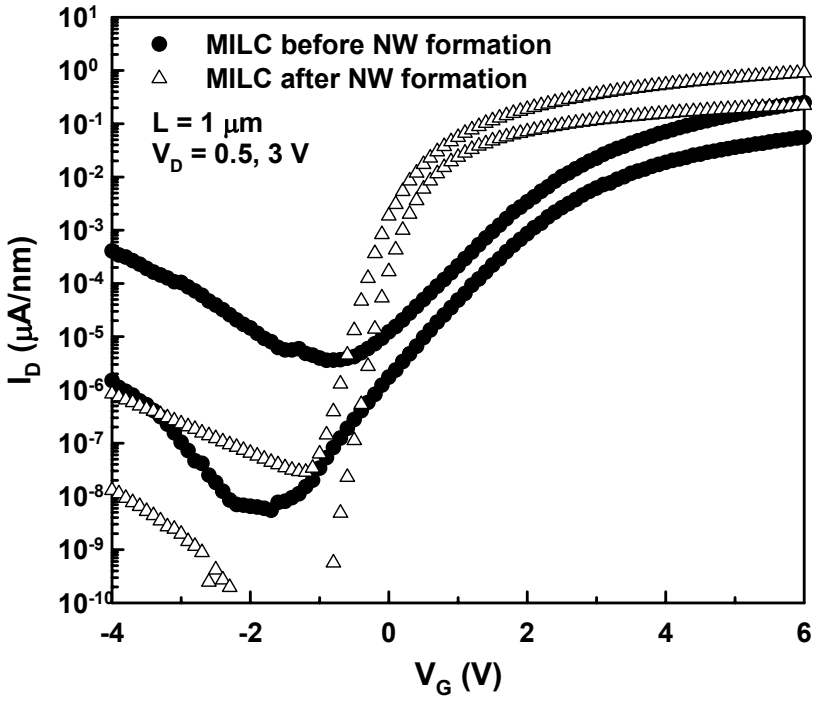


Fig. 2-15 Transfer characteristics of poly-Si NW devices for MILC before and after NW formation.

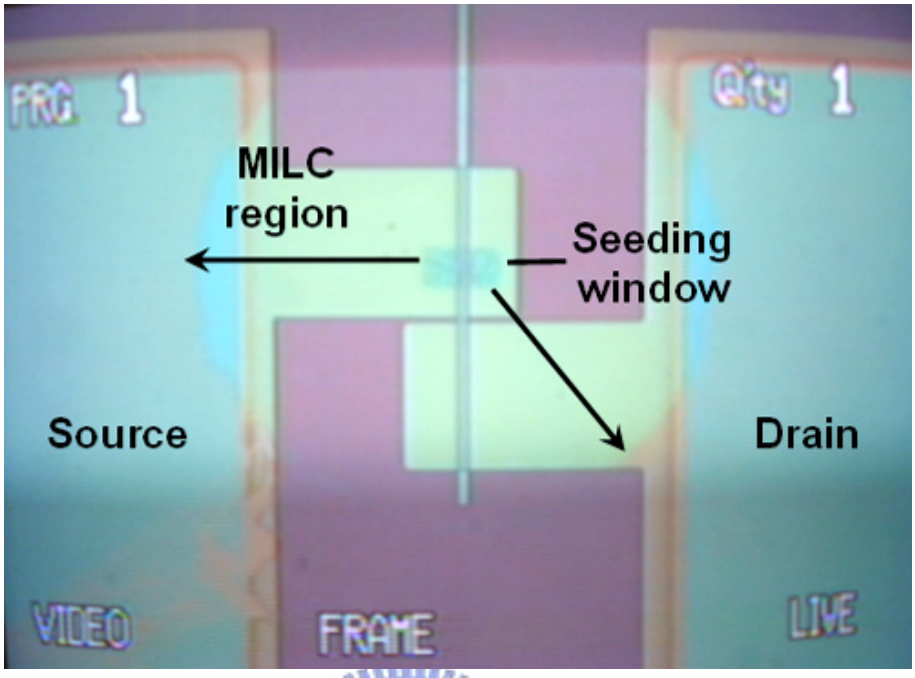


Fig. 2-16 OM photo of the MILC sample for MILC before NW formation.

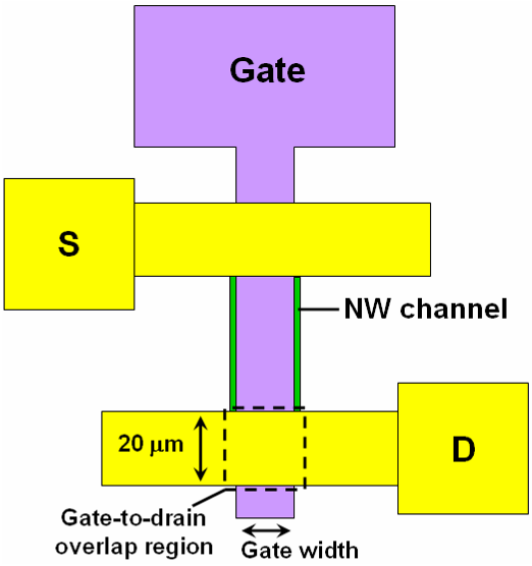


Fig. 2-17 Top-view layout of the NW device showing gate-to-drain (GD) overlap region.

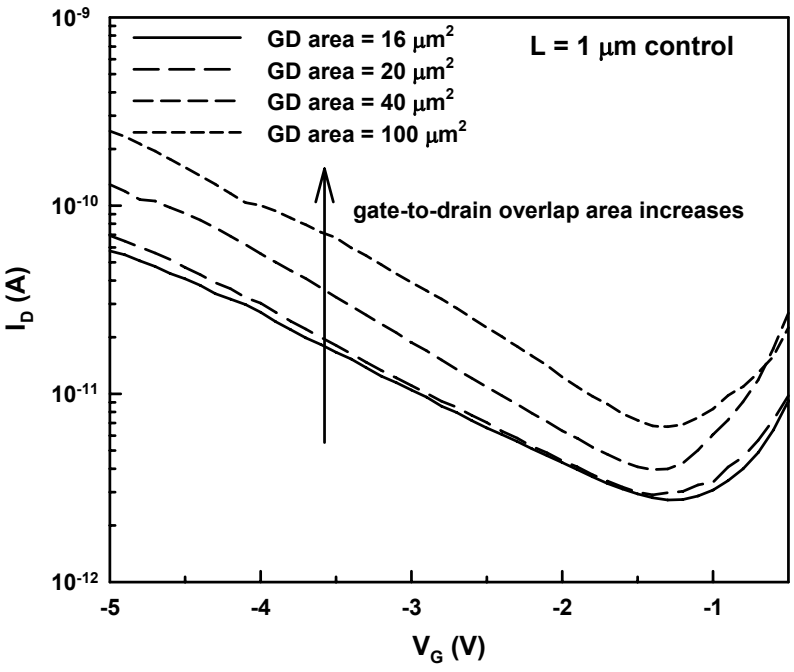


Fig. 2-18 Dependence of off-state current for poly-Si NW TFTs with various gate-to-drain overlap area.

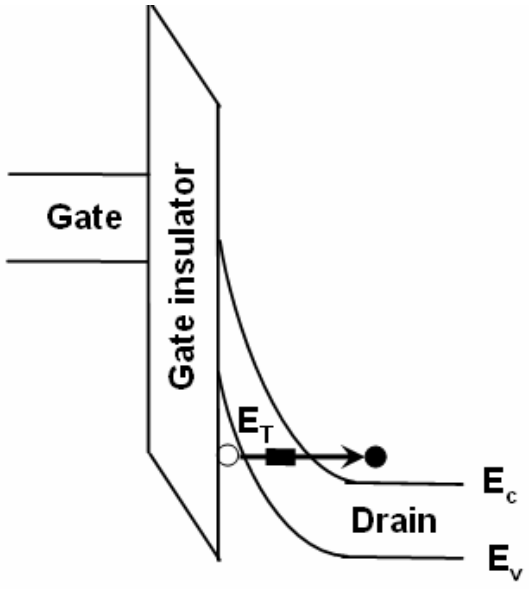


Fig. 2-19 Band diagram of gate-to-drain overlap region under high electric field showing (trap assisted) band-to-band tunneling.

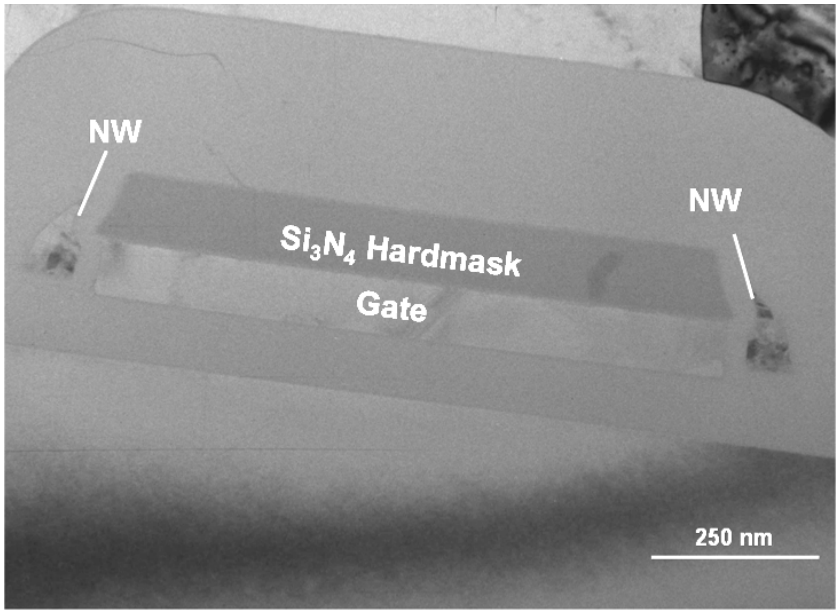


Fig. 2-20 Cross-sectional-view TEM of the poly-Si NW TFT with hardmask structure.

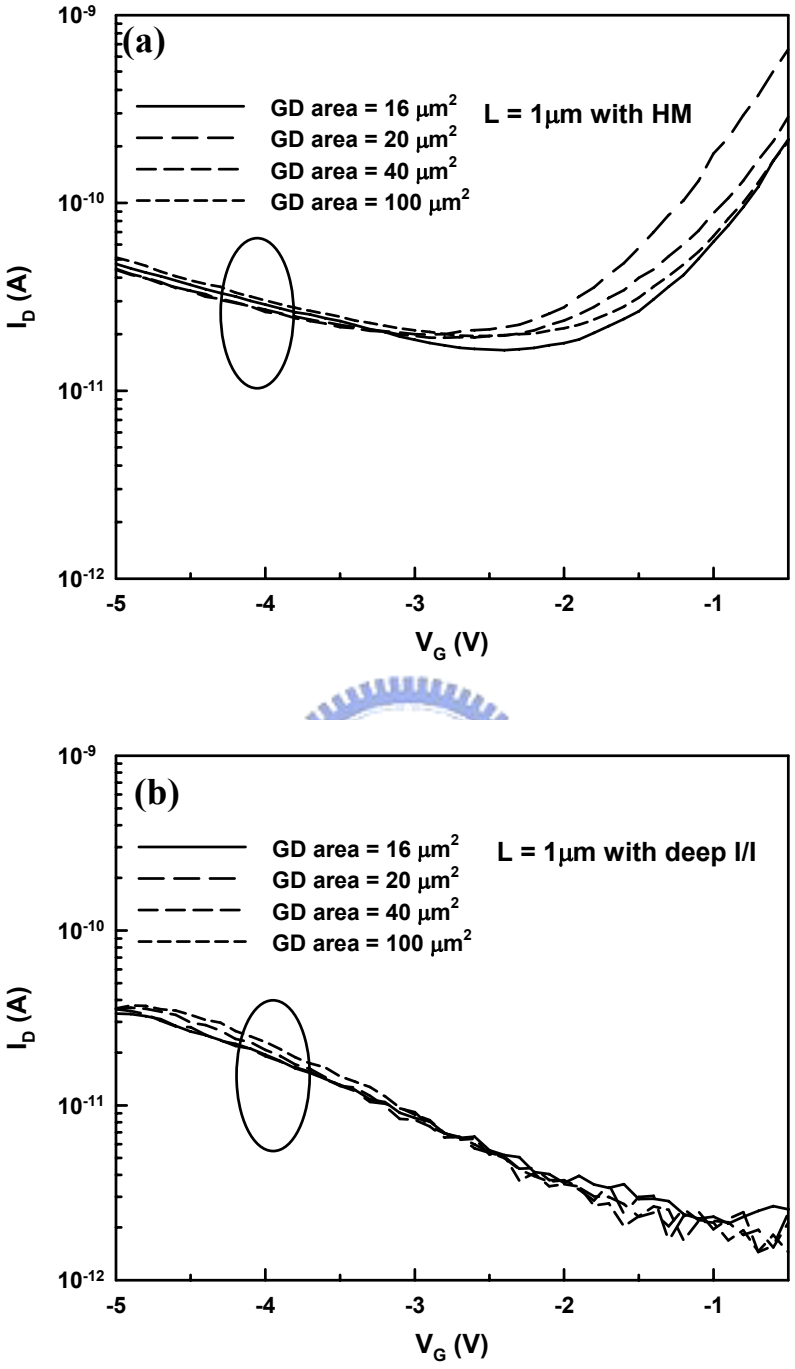


Fig. 2-21 Off-state behaviors of the poly-Si NW TFTs with (a) hardmask and (b) deep ion implantation.

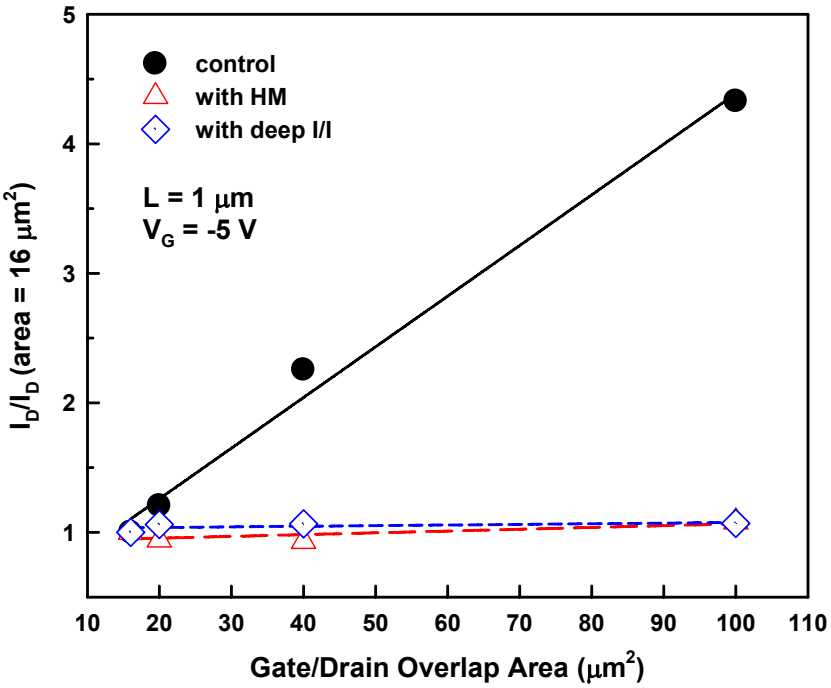


Fig. 2-22 Normalized off-currents of the devices with different modification approaches.

Table 2-I Parameters of plasma hydrogenation treatment.

Plasma source	RF power (watt)	Pressure (mtorr)	Flow rate (sccm)	Temperature (^{o}C)
NH_3	200	300	700	300

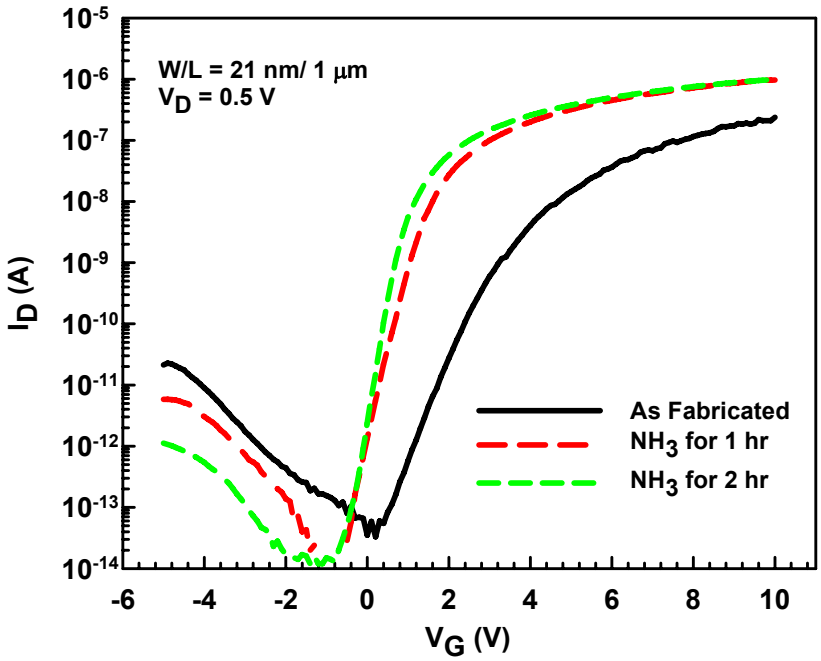


Fig. 2-23 Comparisons of transfer properties for the devices without and with plasma treatment.

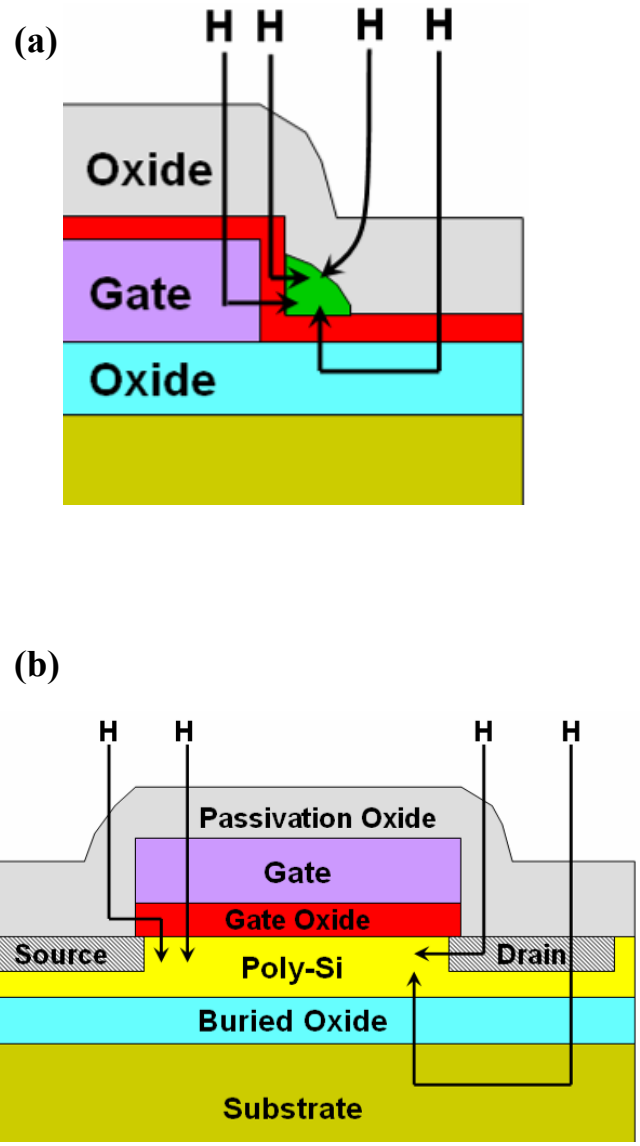


Fig. 2-24 Diagrams illustrating possible pathways for hydrogen migration from the gas source to (a) poly-Si NW TFT and (b) planar TFT.

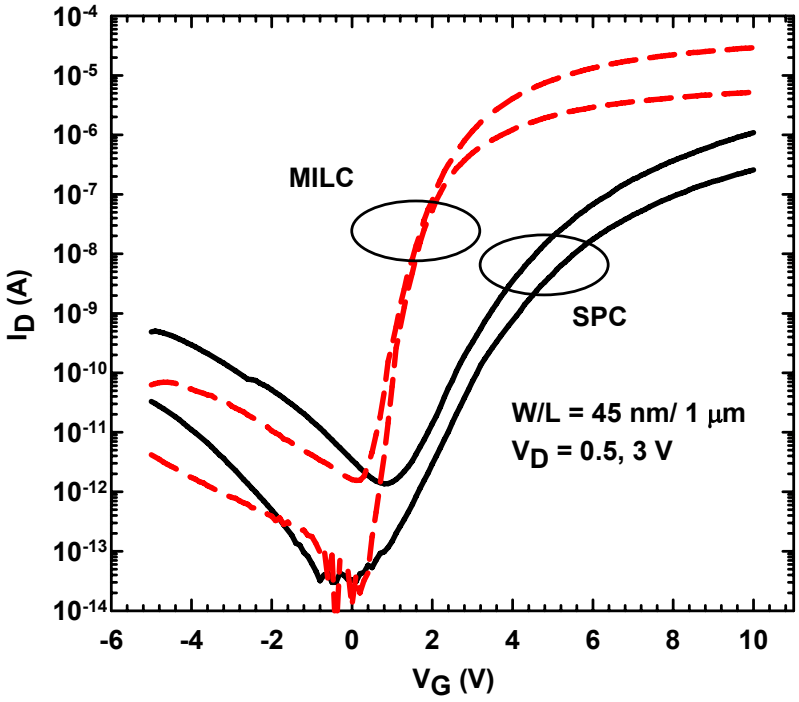


Fig. 2-25 Comparisons of transfer characteristics for SPC and MILC poly-Si NW TFTs with NW channels.

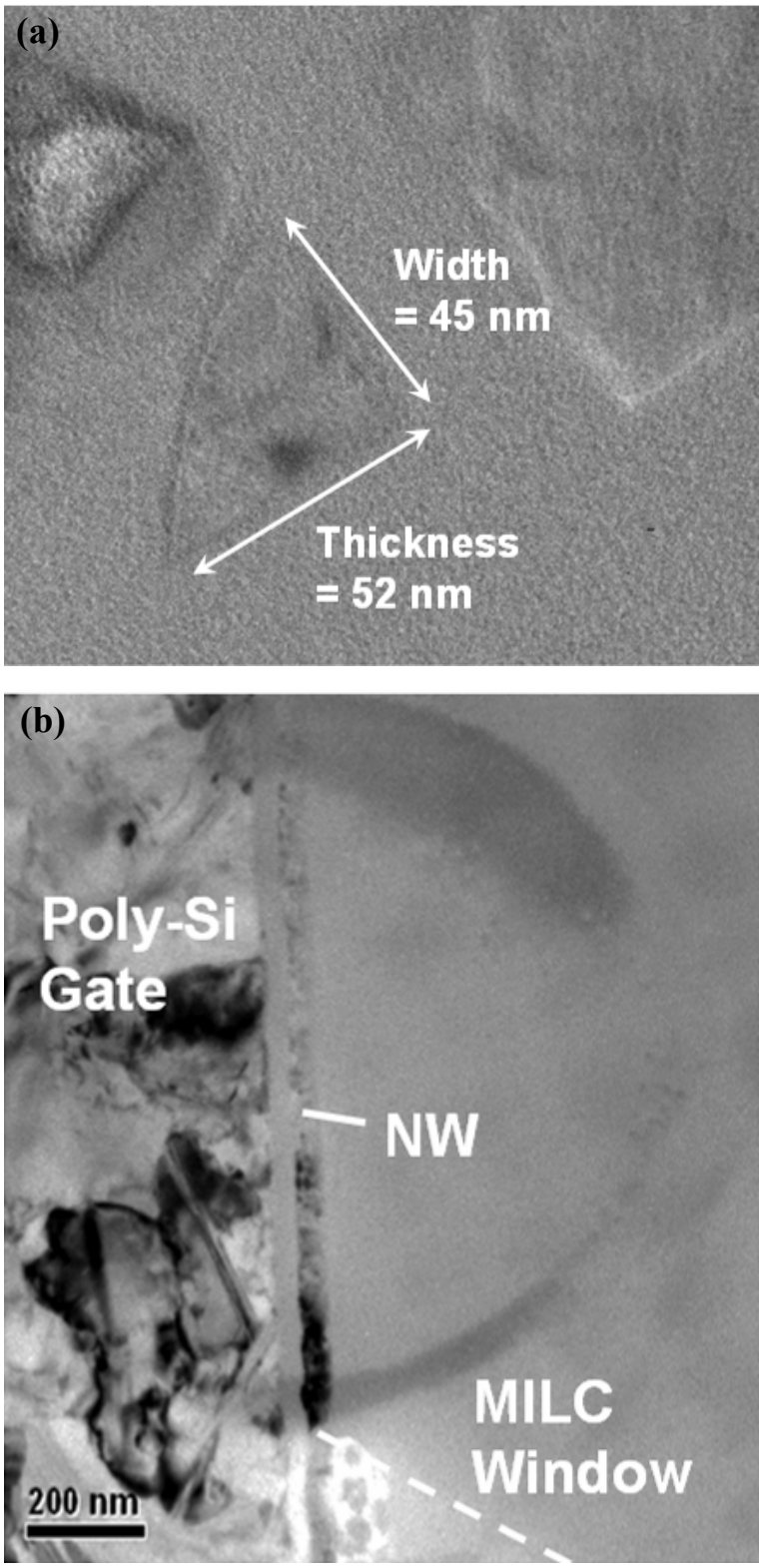


Fig. 2-26 TEM images of MILC poly-Si NW device (a) cross-sectional view and (b) plane-view near the MILC seeding window.

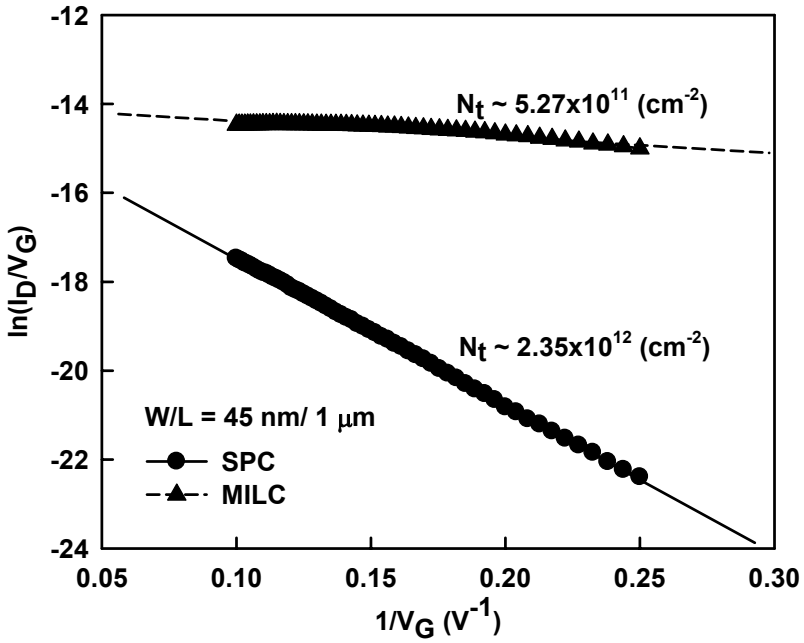


Fig. 2-27 Plot of $\ln(I_D/V_G)$ vs. $(1/V_G)$ and the extracted effective trap density of SPC and MILC poly-Si NW TFTs. I_D were measured at V_D = 0.5V.

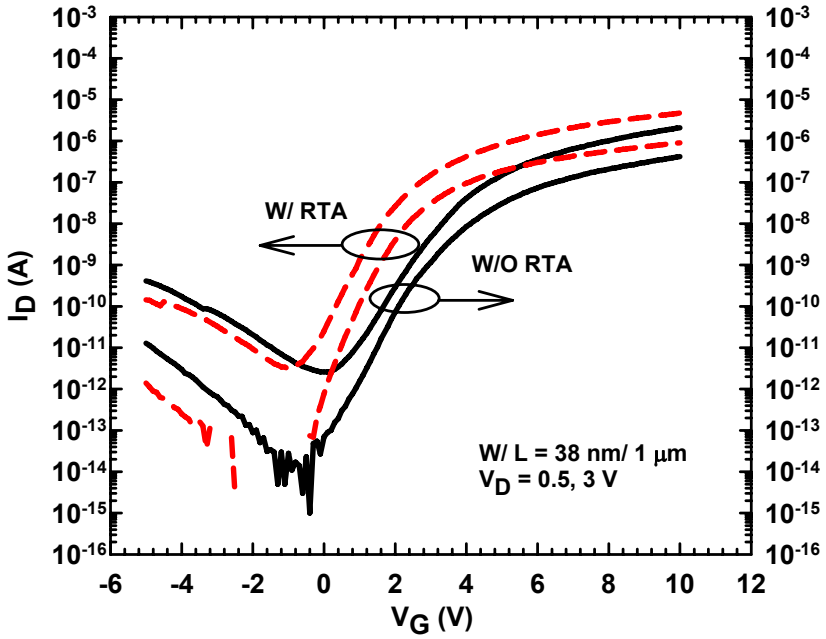


Fig. 2-28 Transfer characteristics of SPC NW devices before and after RTA treatment.

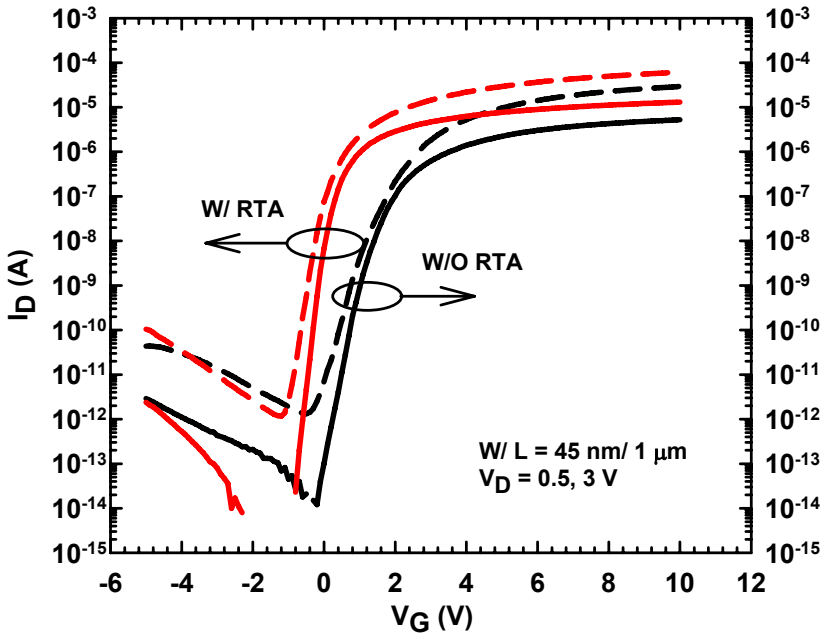


Fig. 2-29 Transfer characteristics of MILC NW devices before and after RTA treatment

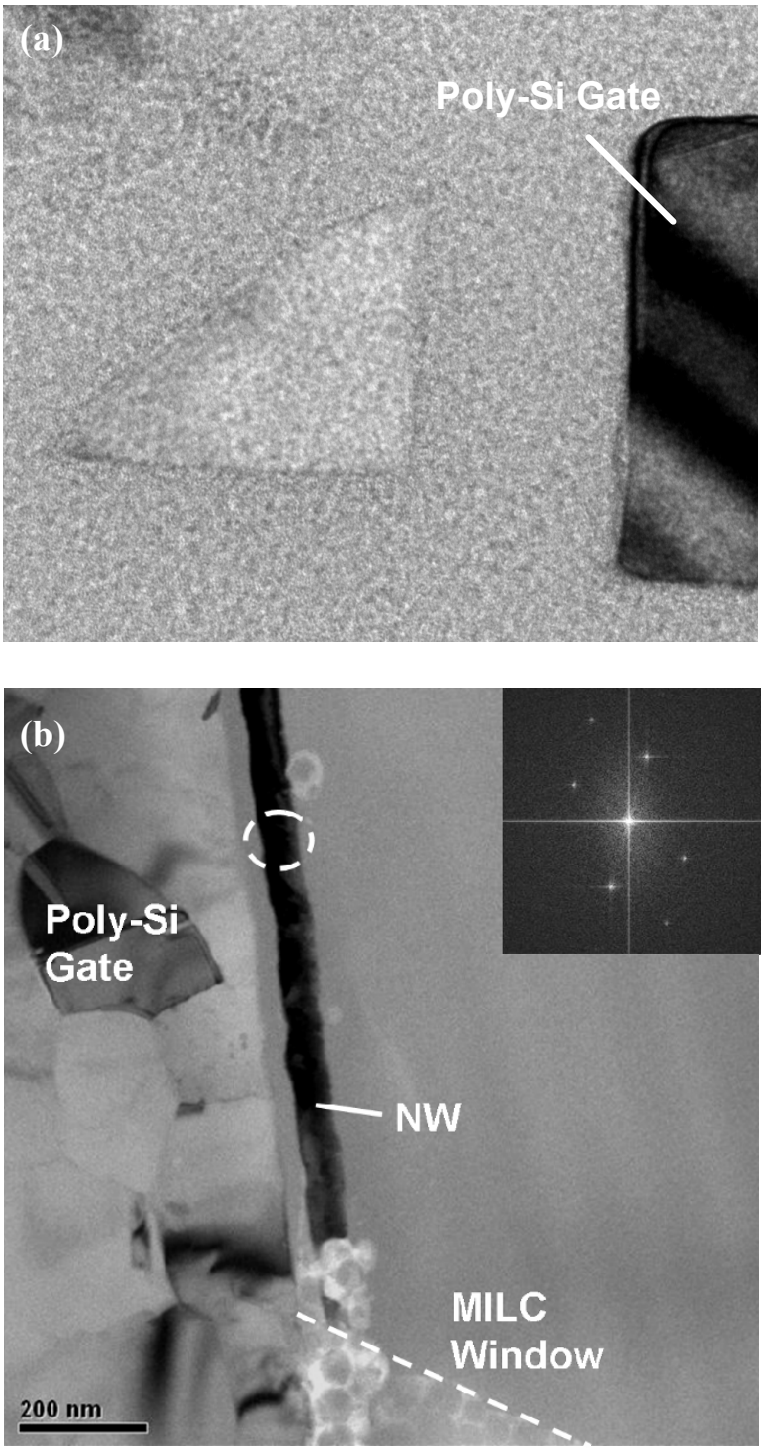


Fig. 2-30 (a) Cross-sectional TEM and (b) plane-view TEM images of MILC device with RTA treatment. The selective diffraction pattern was taken from the circled region in (b), implying single-crystalline property.

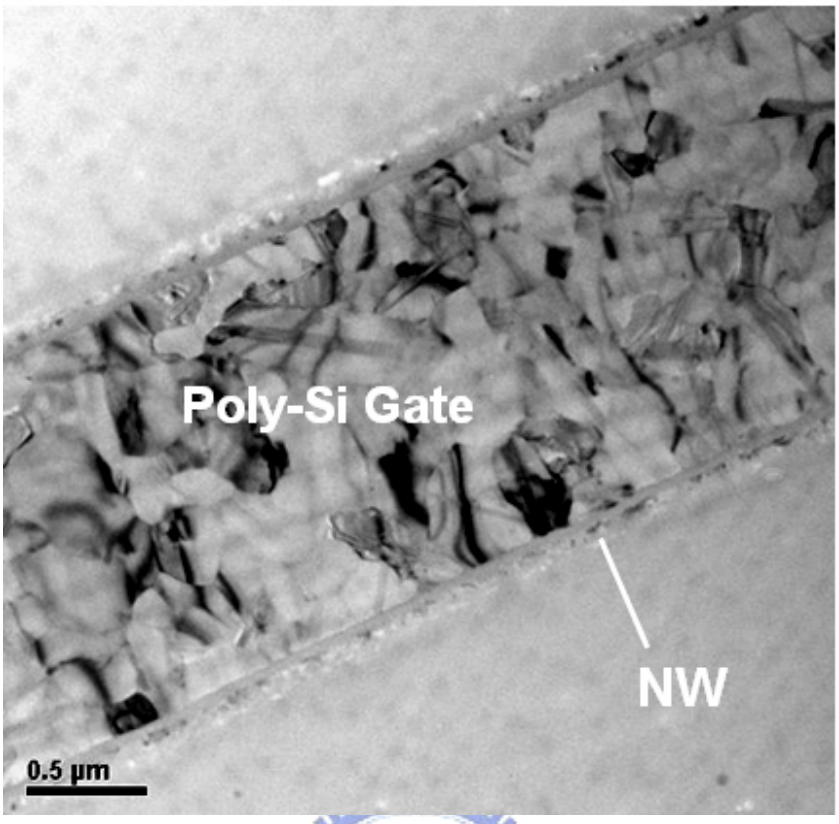


Fig. 2-31 Top-view TEM picture of SPC device with RTA treatment.

Table 2-II Summary of electrical parameters for poly-Si NW devices with various treatments.

	SPC				MILC	
	N	N, RTA	N, 1 hr NH_3	N, 2 hr NH_3	N	N, RTA
V_{th} (V)	5.97	2.35	2.67	1.87	1.62	0.03
S.S. (V/dec)	0.88	0.60	0.35	0.29	0.29	0.16
μ_{FE} (cm^2/V-s)	24	82	48	50	252	550
I_{ON}/I_{OFF} ($x10^6$)	0.14	1.52	2.33	8.9	18.9	52.9

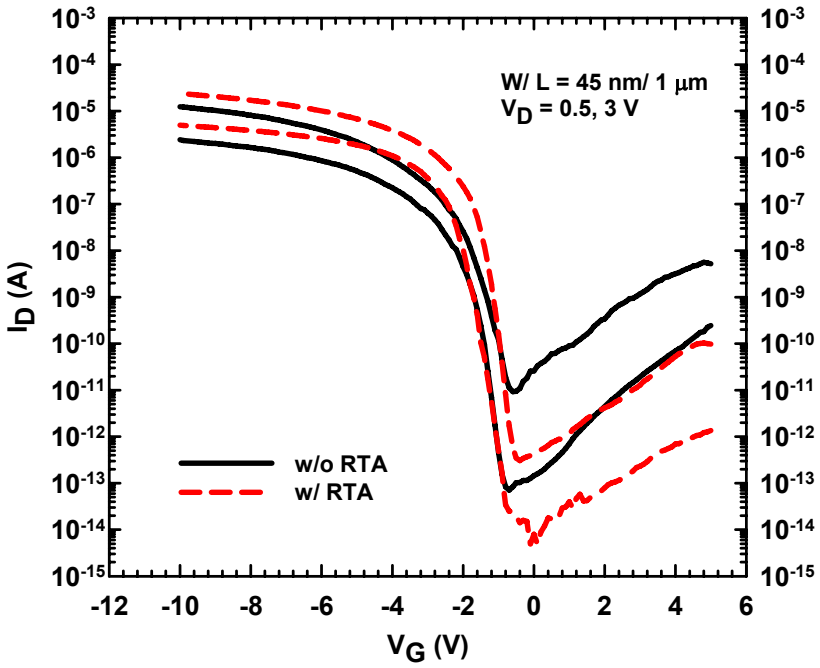


Fig. 2-32 Transfer characteristics of MILC NW p-TFTs devices without and with RTA treatment

Table 2-III Summary of the device characteristics obtained in this work. Data reported in several previous publications in the literature are also included for comparisons.

Process Scheme	Low-T process[1]				High-T process[2]		
	MILC NW	MILC	ELA	VLS[3] NW	MILC NW	MILC	SOI
V_{th} (V)	-2.0	-4.2	-1.57	0.45	-1.9	-2.2	-0.86
μ_h (cm^2/V-s)	145	98	145	119	230	156	242
S.S. (V/dec)	0.230	1	0.104	0.6	0.174	0.16	0.110
I_{off} (pA)	9.4	8	< 10	< 10	0.22	0.4	N/A
I_{on}/I_{off} ($\times 10^6$)	1.3	34	N/A	~ 100	92	~ 100	N/A
Source	This study	Ref. 2.27	Ref. 2.29	Ref. 2.1	This study	Ref. 2.28	Ref. 2.29

[1] Low-T process indicates the whole process temperature is under 700℃.

[2] High-T process indicates some process temperatures are above 900℃.

[3] VLS = vapor-liquid-solid

Chapter 3
Analyses of Silicon Nanowire Thin-Film Transistors Enhanced by Metal-Induced Lateral Crystallization

In Chapter 2, it is demonstrated that the crystallinity of the poly-Si nanowires (poly-Si NWs) can be significantly enhanced by adopting metal-induced lateral crystallization (MILC) and/or rapid thermal annealing (RTA) techniques in the fabrication. Accordingly, the device performance is dramatically improved. In this chapter, the influence of structure and process parameters on MILC mechanism will be investigated for better understanding of MILC enhanced Si NWs.

3.1 Introduction

Si nanowires (NWs) have recently drawn a lot of attentions and have been proposed for a number of potential applications. Here, the NW is referred to the stripe structure with its cross-sectional dimensions smaller than 100 nm. For nanoscale CMOS manufacturing, the NW could be employed as the channel and enable the fabrication of nearly or all-around gate configuration to improve the control over the

short-channel effects [3.1]. Besides, the NW could also be applied to the building of high-performance thin-film transistors (TFTs) on glass or plastic substrates [3.2], light-emitting devices [3.3], and memory devices [3.4].

For practical manufacturing and application, the precise positioning and alignment of NW structures on a chip are essential. This could of course be easily achieved by using advanced lithography techniques. However, the manufacturing cost is high since expensive tools are involved in the fabrication. To address this issue, we have proposed a novel Si NW device [3.5, 3.6] with structure similar to that shown in Fig. 3-1. The device fabrication is simple and does not require costly lithography tools. It thus represents a promising approach for fabricating NW devices on a working chip.

In our previous work, the Si NW was originally annealed at a low temperature to convert the as-deposited amorphous silicon layer into polycrystalline silicon. The so-called solid-phase crystallization (SPC) technique has been widely used in the fabrication of poly-Si TFTs. The device performance, however, is compromised by the large amount of defects contained in the materials, owing to the rather small grain size (i.e., typically less than 50 nm). To improve the film crystallinity, we have successfully developed an improved process implemented with the MILC technique, and the preliminary results are reported in Chapter 2 and recent publications [3.7, 3.8].

In this work, we present the material characterization results to examine the effect of the MILC treatment on the film crystallinity and to understand its impacts on the device performance in detail. Special attention is also paid to the effect of seeding window arrangement and the influence of NW dimension on MILC. In addition, RTA is performed on the NWs to further improve the device characteristics. It is found that more than an order of magnitude of improvement on the filed-effect mobility of electrons relative to the SPC counterpart is achievable when both treatments are combined.

3.2 Device Structure and Fabrication

The devices featuring Si NW channels, as shown in Fig. 3-1, were fabricated with similar process sequence as described in Section 2.2.1, except for the different treatments used for enhancing the film crystallization. Briefly, the fabrication of n-channel devices started with an n^+-poly-Si gate deposition and patterning on an oxidized Si substrate. Then, a 40 nm-thick TEOS serving as the gate oxide was deposited by a low-pressure chemical vapor deposition (LPCVD) system, followed by the deposition of a 100 nm-thick amorphous Si (a-Si) layer. Afterwards, source/drain (S/D) dopants were implanted with P_{31}^+ ion beam with a dose of 1×10^{15} cm^{-2} at 15 keV for n-TFTs and BF_2^+ with 1×10^{15} cm^{-2} at 20 keV for p-TFTs. Subsequently, S/D

photoresist patterns were generated using a g-line stepper and the regions were subsequently patterned by an anisotropic dry etching step. During the etching process, the NW channels were simultaneously formed on the sidewalls of the gate structure, similar to the formation of sidewall spacers used in standard CMOS manufacturing. Note that the NW channels were accomplished in a self-aligned manner with respect to the S/D and remained undoped because the aforementioned implant was done at a low energy so that the implanted dopants do not reach the channel. A 100 nm-thick low-temperature oxide (LTO) was then deposited by a plasma-enhanced (PE) CVD. For MILC purpose, the seeding windows were opened in the LTO layer. In this work, two splits of samples were exploited, as illustrated in Fig. 3-1. In one split, denoted as the Asymmetric Seeding Window (ASW) split, as shown in Fig. 3-1(a), only a single window was opened on the source region. (Here the source region is defined as the terminal that serves as the grounded source during normal device characterization). In the other split, two windows symmetrical to the channel center were opened on both the source and drain regions, and denoted as the Symmetric Seeding Window (SSW) split (Fig. 3-1(b)). After opening the seeding windows, a 5 nm-thick Ni layer was deposited to serve as the seeding layer. The lateral crystallization was carried out at 550 ^{o}C for 16 hours in N_2 ambient. The arrows illustrated in Fig. 3-1 depict the crystallization paths. The MILC step also serves the dual purpose of dopant activation.

Next, the unreacted Ni was disposed off in an H_2SO_4/H_2O_2 solution at 120 ^oC for 10 min. Afterwards, some samples were treated with an additional RTA step at 900 ^oC for 30 sec to further enhance the crystallinity of poly-Si NWs. This condition was chosen since it was reported that the second grain growth of recrystallization took place at around 800 ^oC for MILC poly-Si [3.9]. After depositing a 200 nm passivation oxide layer and opening contact holes, a standard metallization step was performed to complete the device fabrication. It is worth noting that the overall process flow is quite simple and straightforward.

In this study, several parameters, including different MILC seeding window offset (spacing between the window and the channel region, as shown in Fig. 3-1), NW channel length and width, were designed for better comprehension of MILC mechanism in the NW regime.

3.3 Material Characterization

It is well known that needle-like grains formed by MILC are large in length and the “needle” direction could be deliberately arranged to be parallel to the channel direction [3.10]. Once the NW feature size is shrunk to less than the lateral size of the needle grain, it becomes feasible to achieve single-crystal NW structure. Fig. 3-2

shows the migration of a $NiSi_2$ precipitate with size of 50 nm by 10 nm in the NW, leaving behind the needle-like Si crystallite. In this case, single-crystalline Si property is thus obtained. In this section, we characterized the crystallinity of the NWs with transmission electron microscopy (TEM) technique performed on test bar structures. Fig. 3-3 shows the plane-view TEM image of an NW channel abutting the poly-Si gate and the seeding window after the MILC process. As can be seen in the picture, the MILC NW shows "bamboo" structure. In contrast to the fine-grain structure of the SPC NW, the film crystallinity of the MILC sample is dramatically improved and the length of the grains could reach several tens of nanometers.

To further enlarge the grain size and eliminate defects like stacking faults and microtwins in the MILC films, it is necessary to perform post-annealing treatment. Previously excimer laser annealing (ELA) [3.11, 3.12], and high temperature annealing [3.13] have been proposed for this purpose. In this study, some samples received an additional RTA step at 900 ^{o}C for 30 sec. The TEM picture of a RTA-treated sample is shown in Fig. 3-4. Apparently, the crystallinity of the annealed NW is significantly improved and a monocrystalline structure is achieved. The length of a single grain is about 2 μm in this region. Diffraction pattern obtained by performing the Fast Fourier Transform (FFT) technique on the high resolution TEM (HRTEM) image (Fig. 3-4(b)) indicates the formation of single-crystal Si with <110>

orientation. For comparisons, the TEM image of a SPC poly-Si NW that also received the RTA treatment is shown in Fig. 2-31. The image reveals that the SPC poly-Si contains a number of micro-structural defects while the crystalline orientation of the grains is random.

Film crystallinity of the NW is also expected to show dependence on the distance from the MILC seeding window. To confirm this point, the TEM images taken at different locations in the NWs are presented in Figs. 3-5 and 3-6 for the MILC samples without and with RTA, respectively. Fig. 3-5 shows the overview of the characterization region. The results show that the crystalline quality is poorer in the area located about 5 μm away from the seeding window (region 2) than in the area near the window (region 1). The trend that the grain size becomes smaller as the region is farther away from the window is reasonable, since the grain growth due to heterogeneous nucleation of SPC process is apt to compete with MILC grain growth. Such mechanism needs a period to trigger and thus is not important as the crystallization region is near the seeding window.

The MILC NW with RTA also possesses this feature, as shown in Fig. 3-6. However, it should be noted the crystallinity is greatly improved after receiving the RTA, especially for the region closer to the seeding window. From the TEM results we conclude that, the combination of MILC and RTA treatments together with

suitable control over the NW length from the seeding window (say, smaller than 5 μm in the present process conditions), single-crystal NW structure could be obtained and excellent device performance is achievable.

3.4 Electrical Characteristics of the Fabricated Devices

3.4.1 Effects of Seeding Window Arrangement

Figs. 3-7 and 3-8 compare the transfer and output characteristics between MILC ASW and SSW splits. As can be seen in the figures, it is worthy to note that the two MILC splits show greatly improved characteristics in terms of higher drive current and carrier mobility as well as reduced threshold voltage and subthreshold slopes as compared with the SPC device (Fig. 2-10). This confirms the effectiveness of this technique in improving the film crystallinity. The extracted performance parameters are preliminarily summarized in Table 3-I. The mobility values are 252 and 169 cm^2/V-sec for ASW and SSW samples, respectively. The improvement is more significant for the ASW configuration. This trend is consistent with that reported in the previous work [3.14] and the TEM results presented in previous section. Note that in the MILC process, the crystallization proceeds radially from the seeding window as described in Fig. 2-7. In the symmetric case, the fronts of crystallization from the

opposite sides confront each other at the central region of the channel. Trace amount of metallic species may be left inside the channel and lead to poorer on-state performance as compared with the asymmetric case.

In the aspect of off-state leakage, however, the results indicate that it is not effectively suppressed when MILC is implemented. The situation becomes even worse when SSW is implemented. In one of our previous studies, we have identified that the magnitude of leakage current is closely related to the dimension of the top gate-to-drain overlap region [3.6]. When drain voltage is high, the strong electric field together with the defects at grain boundaries triggers the anomalously high leakage current. In the MILC sample with SSW configuration, one of the seeding windows is located in the drain region, and it is expected that a considerable amount of metallic species remain within the window. In line with the analysis in the previous report [3.6], it is believed that those defect sites are responsible for the excess leakage current. In the ASW case, the window is opened only on the source side in which the electric field strength is low during operation. Also, the NW could serve as a filter for $NiSi_2$ crystallites since the dimension of the NW is comparable to the general $NiSi_2$ precipitate. The ASW sample thus depicts much lower off-sate leakage than the SSW one. This also implies that the characteristics of the devices with ASW configuration depend on the electrodes where source and drain biases are assigned. This issue will

be addressed later.

3.4.2 Impacts of RTA on Device Performance

In this subsection, we examine the effect of RTA on ASW and SSW devices. Results for the splits of samples are shown in Fig. 3-9 and Table 3-I. The RTA treatment could further promote the device characteristics of the MILC devices. For the ASW sample, the electron mobility is boosted from 252 cm^2/V-sec to 550 cm^2/V-sec. This value is among the best results reported in the literature [3.13, 3.15]. It is suspected that the RTA treatment helps remove the weak or strained bonds contained in the grains and leads to a better film crystallinity, and is evidenced by the enhanced contrast of the diffraction patterns mentioned above. For SSW case, the mobility is also promoted about twice from MILC device without RTA. Also should be noted is the reduction of parasitic source/drain resistance due to the activation of dopants by RTA which is also beneficial for device characteristics. For the MILC samples, the sheet resistance of the S/D doping regions is found to reduce from 360 ohm/sq. to 250 ohm/sq. after RTA. Series resistance of the fabricated devices is extracted based on a method reported previously [3.16]. Typical values for MILC devices are around 7×10^4 ohm, and reduce to around 2×10^4 ohm after RTA. Note the

mobility data shown in Table 3-I are extracted from the maximum transconductance at V_D = 0.5 V without considering the effect of series resistance. When the series resistance is taken into account, the intrinsic mobility can be obtained, and the values are 324 and 591 cm^2/V-s for MILC devices without and with RTA, respectively. The impact of RTA on the mobility enhancement is still significant.

The off-state leakage is also suppressed for the SSW split, as shown in Fig. 3-9(b). These findings are consistent with the TEM characterization results presented in previous section. In Fig. 3-9(a), it is seen that the off-state leakage does not seem to be dramatically affected by the RTA treatment. We have checked the fabricated devices about this phenomenon and found that the impact of RTA on the OFF leakage current of the ASW devices is actually similar to that of SPC sample shown in Fig. 2-28. Based on this finding we suggest that the drain region of the ASW samples is crystallized mainly via the SPC process. This is reasonable since the drain region is away from and separated by the NW channel. The SPC regions are with fine grains while the grain size is not dramatically affected by the RTA treatment. Detailed mechanism about the leakage mechanism is addressed in another publication [3.6].

3.4.3 Forward and Reverse Modes of Operation in ASW Devices

For the ASW devices, it is interesting to investigate the impact of reversing the S/D assignment during operation on the device characteristics. The results are illustrated in Fig. 3-10 for devices without and with RTA treatment, respectively. Here the "forward mode" denotes the case when the drain bias is applied to the electrode having no seeding window (i.e., the same situation as in Figs. 3-7 and 3-9(a)) while the other electrode with seeding window is grounded and serves as the source electrode. For "reverse mode" of operation, the source and drain electrodes are simply exchanged. Obviously the change of operation modes may result in different outcome. As can be seen in Fig. 3-10(a), the reverse mode of operation depicts a high off-state and subthreshold leakage. The excessive defects originating from the seeding window located at the gate-to-drain overlap region are responsible for the leakage. Residual Ni contamination is mainly responsible for this phenomenon [3.14, 3.17]. Also should be noted is the large fluctuation of such leakage [3.17], explaining why the leakage shown in Fig. 3-10(a) under reverse-mode operation is even higher than that shown in Fig. 3-8 for the SSW device. Such asymmetry in device characteristics is largely alleviated as the RTA is applied, as shown in Fig. 3-10(b). After the RTA the grains are enlarged and most of the defects are eliminated or driven away from the region where the leakage takes place.

To study the effect of trace amount of Ni in the channel and keep the defective MIC/MILC intersection region away from the channel, various offset lengths were designed. The split parameters are 0.5, 1.5, 2.5, 4 and 5.5 μm. All electrical characterizations were performed under both forward and reverse modes of operations. The off-state current as a function of offset length for ASW and SSW devices under both forward and reverse modes of operations are shown in Fig. 3-11. It is apparent that for the ASW device, the leakage current under reverse mode of operation is at least two orders of magnitude larger and with much larger variation, compared with the forward mode of operation. This is mainly attributed to the defective MIC/MILC interface (as shown in Fig. 2-7) and residual Ni species causing additional trap-assisted leakage paths if the seeding window resides on the drain side [3.14]. Particularly, this phenomenon becomes more serious as the offset is smaller than 1 μm. However, the leakage current is almost independent of the offset length under forward mode of operation for the ASW device, which can be explained by the fact that the drain terminal is possibly free from the highly defective trap states. It also reveals that the leakage current of the ASW device under forward mode could be decreased by about three orders of magnitude over that under reverse mode as offset is 0.5 μm. Moreover, it is noted that comparable trend and variation as well as magnitude of the leakage current are revealed in the three splits of reverse-mode ASW,

forward-mode SSW and reverse-mode SSW. It implies that the severe leakage current is largely dependent on the amount of trap densities existing at the drain terminal, but not at the source side. These results are conducive to obtaining optimal MILC NW device structure.

3.4.4 Length Effects on MILC Si NWs

In Figs. 3-5 and 3-6, the region near the seeding window shows good crystallinity, while the crystalline quality is worsened in the area located 5 μm away from the seeding window. The location dependence in material quality reflects on the device characteristics. Fig. 3-12 compares the transfer characteristics between the ASW and SSW devices with L = 1 μm. It is seen that the performance is better for the ASW device. In the symmetric case, the fronts of crystallization from opposite sides confront with each other at the central region of the channel. Trace amount of metallic species may be left inside the channel and leads to the degraded on-state performance as compared with the asymmetric case. Nevertheless, the trend is reversed in the case of devices with L = 5 μm, as shown in Fig. 3-13. This could be understood with schematic drawing of the grain structure in NW for the ASW devices shown in Fig. 3-13(c). When the channel is long, SPC NW will most probably take place in the

region near the drain. As a result, the mobility and on-state current would be worse than those with the SSW device, as shown in Fig. 3-13. This is because the SSW configuration has better crystalline property in the channel due to the needle-like grains growth from both sides. Fig. 3-14 is the series TEM pictures taken in the test structure near the two adjacent seeding windows. Note that the sample received RTA post-treatment. In this picture, two large grains protruding from the corresponding MILC windows show comparatively restrained SPC growth.

In addition, p-TFTs also suffer from small grain structures due to SPC growth competing with MILC process especially in the channel length, and show similar trends for ASW and SSW configurations. As mentioned in Section 2.2.2, boron could enhance MILC rate; however, the NW channels in this study is nominally undoped. As a result, $NiSi_2$ front still proceeds in a slow rate.

In addition to less dependence on the length for the SSW configuration, two main strategies could be adopted to address the length issue. One is to increase MILC rate; the other is to suppress SPC growth. As described in Fig. 2-5, MILC rate is found to be faster in p-type poly-Si films. In this regard, if NW channels are doped with p-type dopants, MILC rate will increase. However, dopant distribution in NWs will remain an issue. Furthermore, V_{th} adjustment for both n- and p-type devices will be inflexible. The other approach is by lowering annealing temperature, thus

suppressing the SPC process. It is known that the activation energy is about 3.2 eV for SPC, while 1.85 eV for MILC [3.18]. Hence, Fig. 3-15 displays the on-current behaviors as a function of the channel length for devices annealed at 525 ^{o}C and 550 ^{o}C. It can be seen that the on-current for the 525 ^{o}C-annealed device is indeed larger than that for the 550 ^{o}C-annealed counterpart. Fig. 3-16 shows the schematic illustrations for the crystalline properties of MILC NW channels at higher and lower annealing temperatures. It is inferred that fewer small-size SPC grains could retard MILC grain growth at lower annealing temperature, and thus enhancing the crystallinity of NW channels and increasing the on-current.

3.4.5 Width Effects on MILC Si NWs

Fig. 3-17 shows the transfer characteristics of 22 nm-wide MILC NW as compared with 22 nm-wide SPC and 50 nm-wide MILC NW devices. For fair comparisons, all currents are expressed as current density by dividing the current by the cross-sectional conduction width of NW. The SPC sample here is the device fabricated on the same wafer but without MILC seeding window, thus only received the thermal annealing. Apparently, the 50 nm-wide NW device depicts pronounced MILC effect and superior performance in the subthreshold and ON regions. However,

MILC and SPC effects are nearly comparable for the narrow-channel (i.e., 22 nm) devices, revealing similar crystallinity and the NW is mostly comprising of SPC grains. This phenomenon is also observed in the previous research [3.19]. Width of NWs smaller than 30 nm would result in little lateral crystallization. Moreover, larger leakage current is found for narrower MILC NWs, which could be ascribed to the slower MILC rate and defective structures induced by possible metal residues in the channel. If considering the aforementioned GIDL effect, the leakage is thus aggravated.

In addition to spatial confinement for $NiSi_2$ crystallite to proceed in the NW channel, the competing heterogeneous SPC growth is believed to be more pronounced in a smaller space. The proposed scheme could be interpreted as shown in Fig. 2-13. Therefore, MILC NW process in an aggressively scaled volume becomes much more complicated to analyze. Such effect certainly needs plenty of samples and careful TEM analysis, and is still currently under investigation.

3.5 Summary

In this work, we have successfully implemented the MILC process to enhance the film crystallinity of Si NW channels in a novel NW FET device. With such

scheme, significant improvement in device performance is achieved. The TEM analysis indicates that “bamboo” structure is formed in the NW near the seeding window. Combined with an additional RTA treatment, single-crystal NW structure becomes feasible. In the region of NW farther away from the seeding window, the SPC mechanism may compete with the MILC during crystallization process, and leads to poor film crystallinity.

In the implementation of MILC process, it is shown that the arrangement of seeding window plays an important role in affecting the resulting film quality and the device performance. In this regard, ASW arrangement is preferred. When MILC and RTA techniques are combined, it is found that single-crystal-like NWs are achieved. Moreover, the offset length of the seeding window is found to be an important factor to influence the leakage behavior of MILC NW devices.

In order to suppress SPC grains in MILC channels especially in long NWs, SSW configuration turns out to be a better choice of device structure, since needle-like grains growing from opposite sides of the channel could comparatively retrain SPC process. In addition, by reducing recrystallization temperature, SPC rate could be retarded and thus promote on-state behaviors.

References

[3.1] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu and C. C. Huang *et al*, "5 nm-gate nanowire FinFET," *Symp. VLSI Tech. Dig.*, 196, June 15-17 (2004).

[3.2] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles and J. L. Goldma, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature*, **425**, 274 (2003).

[3.3] X. Duan, Y. Huang, Y. Cui, J. Wang and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, **409**, 66 (2001).

[3.4] X. Duan, Y. Huang and C. M. Lieber, "Nonvolatile memory and programmable logic from molecule-gated nanowires," *Nano Lett.*, **2**, 487 (2002).

[3.5] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee and Y. S. Yang, "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel," *IEEE Electron Device Lett.*, **26**, 643 (2005).

[3.6] H. C. Lin, M. H. Lee, C. J. Su and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si

channels," *IEEE Trans. Electron Devices*, **53**, 2471 (2006).

[3.7] C. J. Su, H. C. Lin and T. Y. Huang, "High performance TFTs with Si nanowire channels enhanced by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, **27**, 582 (2006).

[3.8] C. J. Su, H. C. Lin, M. H. Lee, H. H. Tsai, Raymond C. T. Lin, S. W. Shen, C. C. Lee, T. Y. Huang and Y. S. Yang, "Effects of seeding window arrangement on the performance of Si nanowire transistors with MILC channels", *IEEE Silicon Nanoelectronics Workshop*, 167, June 11-12 (2006).

[3.9] G. Liu and S. J. Fonash, "Polycrystalline silicon thin film transistors on Corning 7059 glass substrates using short time, low-temperature processing," *Appl. Phys. Lett.,* **62**, 2554 (1993).

[3.10] S. Jagar, H. Wang and M. Chan," Effects of longitudinal and latitudinal grain boundaries on the performance of large-grain polysilicon MOSFET," *IEEE Electron Device Lett.*, **22**, 218 (2001).

[3.11] D. Murley, N. Young, M. Trainor and D. McCulloch, "An investigation of laser annealed and metal-induced crystallized polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices,* **48**, 1145 (2001).

[3.12] G. Hu, Y. S. Wu, C. Chao and H. Shih, "Growth mechanism of laser annealing

of nickel-induced lateral crystallized silicon films," *Jpn. J. Appl. Phys.,* **45**, 21 (2006).

[3.13] H. Wang, M. Chan, S. Jagar, V. M. C. Poon, M. Qin, Y. Wang and P. K. Ko, "Super thin-film transistor with SOI CMOS performance formed by a novel grain enhancement method," *IEEE Trans. Electron Devices*, **47**, 1580 (2000).

[3.14] M. Wong, Z. Jin, G. A. Bhat, P. C. Wong and H. S. Kwok, "Characterization of the MIC/MILC interface and its effects on the performance of MILC thin-film transistors," *IEEE Trans. Electron Devices*, **47**, 1061 (2000).

[3.15] C. Hou and Y. S. Wu, "Comparison of TFTs made by IMPRINT and IMPRINT-ELA methods," *Electrochem. Solid-State Lett.*, **9**, H71 (2006).

[3.16] K. Terada and H. Muta, "A new method to determine effective MOSFET channel length," *Jpn. J. Appl. Phys.*, **18**, 953 (1979).

[3.17] Z. Meng, M. Wang and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, **47**, 404 (2000).

[3.18] L. K. Lam, S. K. Chen and D. G. Ast, "Kinetics of nickel-induced lateral crystallization of amorphous silicon thin-film transistors by rapid thermal and

furnace anneals," *Appl. Phys. Lett.,* **74**, 1866 (1999).

[3.19] J. Gu, S. Y. Chou, N. Yao, H. Zandbergen and J. K. Farrer, "Single-crystal Si formed on amorphous substrate at low temperature by nanopatterning and nickel-induced lateral crystallization," *Appl. Phys. Lett.,* **81**, 1104 (2002).

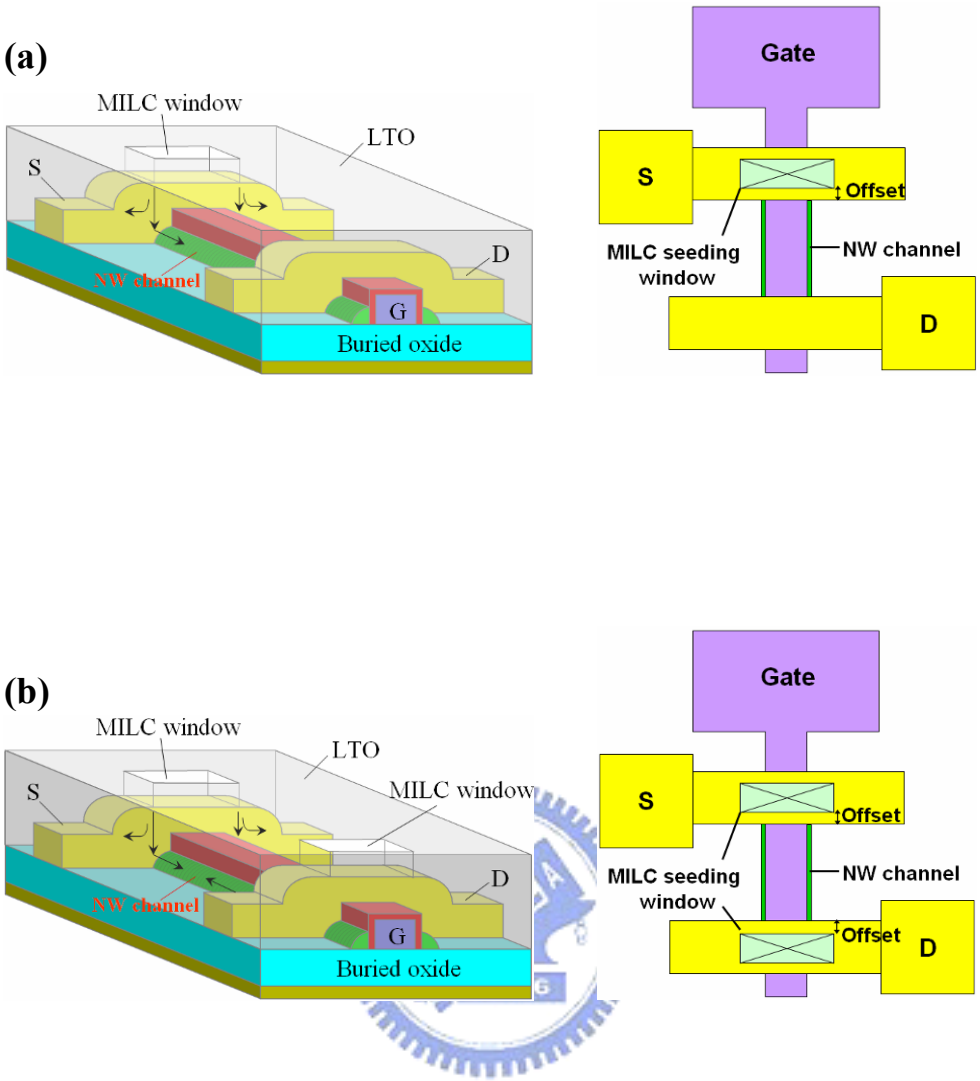


Fig. 3-1 Top and side views of the MILC devices with (a) ASW and (b) SSW configurations. Note that NW spacers actually remain on the sidewall of the gate pad and gate-end regions, but are not shown in the top views of the devices for simplicity.

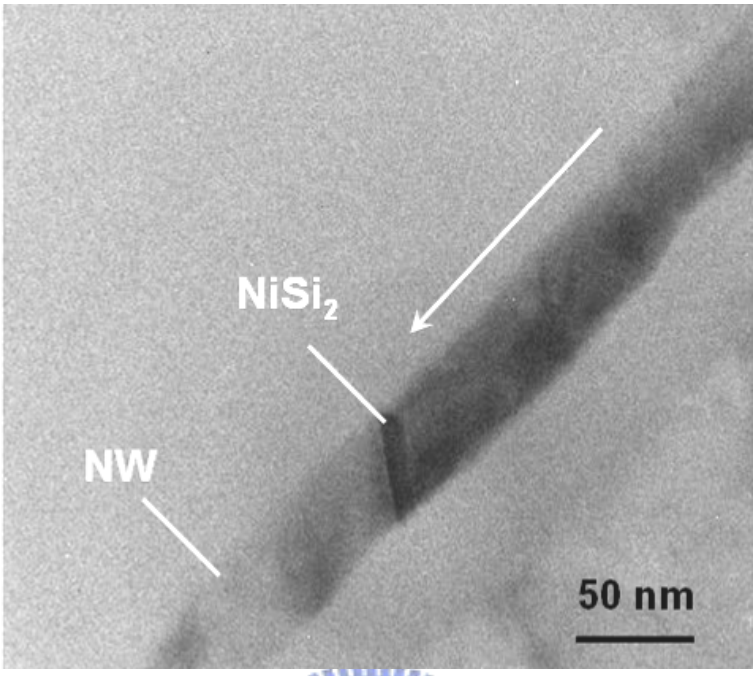


Fig. 3-2 The migration of a $NiSi_2$ crystallite leaving behind the needle-like Si grain. The arrow indicates the crystallite proceeding direction.

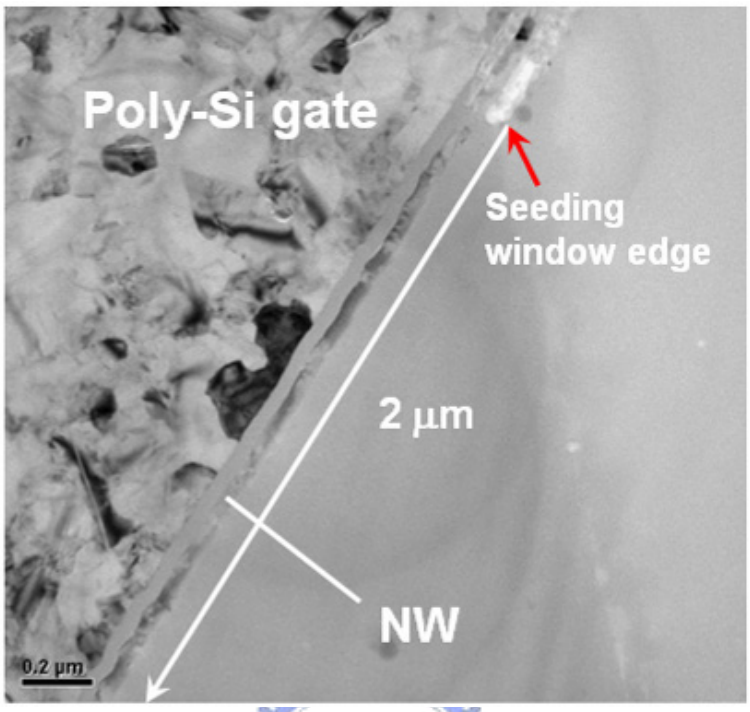
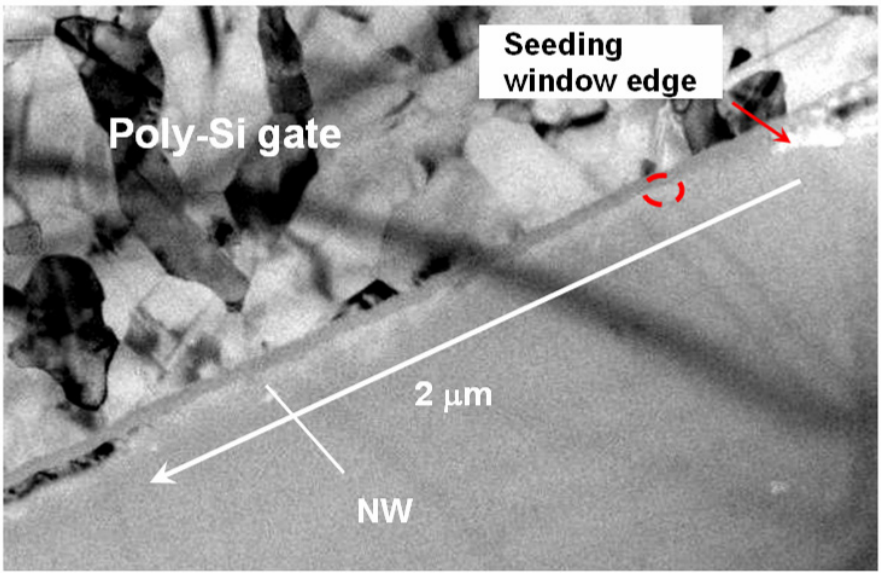


Fig. 3-3 Top-view TEM image of an MILC Si NW.

(a)



(b)

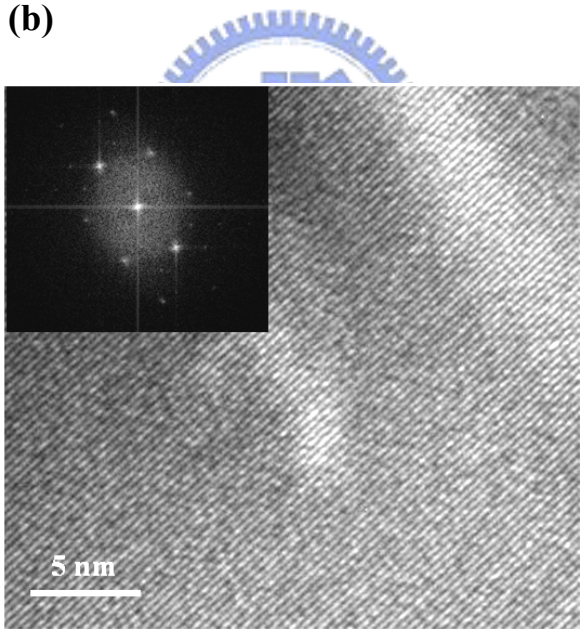


Fig. 3-4 (a) TEM image of an MILC Si NW with RTA treatment. (b) A high-resolution view of the NW channel (the circled region in (a)) and the associated diffraction patterns.

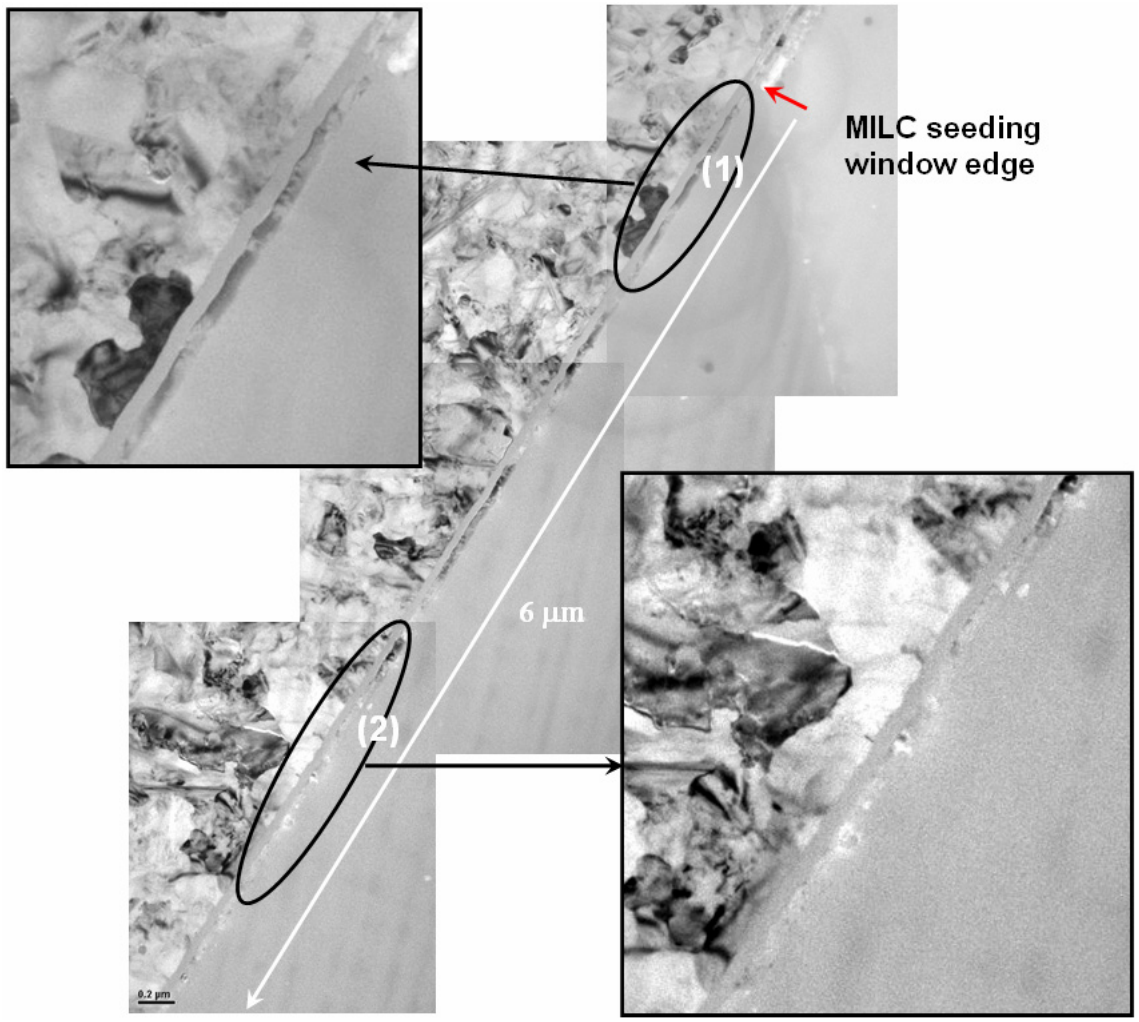


Fig. 3-5 An overview on the crystallization region of an MILC Si NW. The inset pictures are enlarged view of region 1 (close to the seeding window) and region 2 (about 5 μm away from the seeding window) in the characterization region. Due to the distance effect, SPC mechanism also proceeds in region 2 and leads to a smaller grain structure as compared with region 1.

Fig. 3-6 An overview on the crystallization region of an MILC Si NW with RTA treatment. The inset pictures are enlarged view of regions 1 and 2 in the characterization region. Note that the grain structure in region 2 is not significantly affected by the RTA treatment.

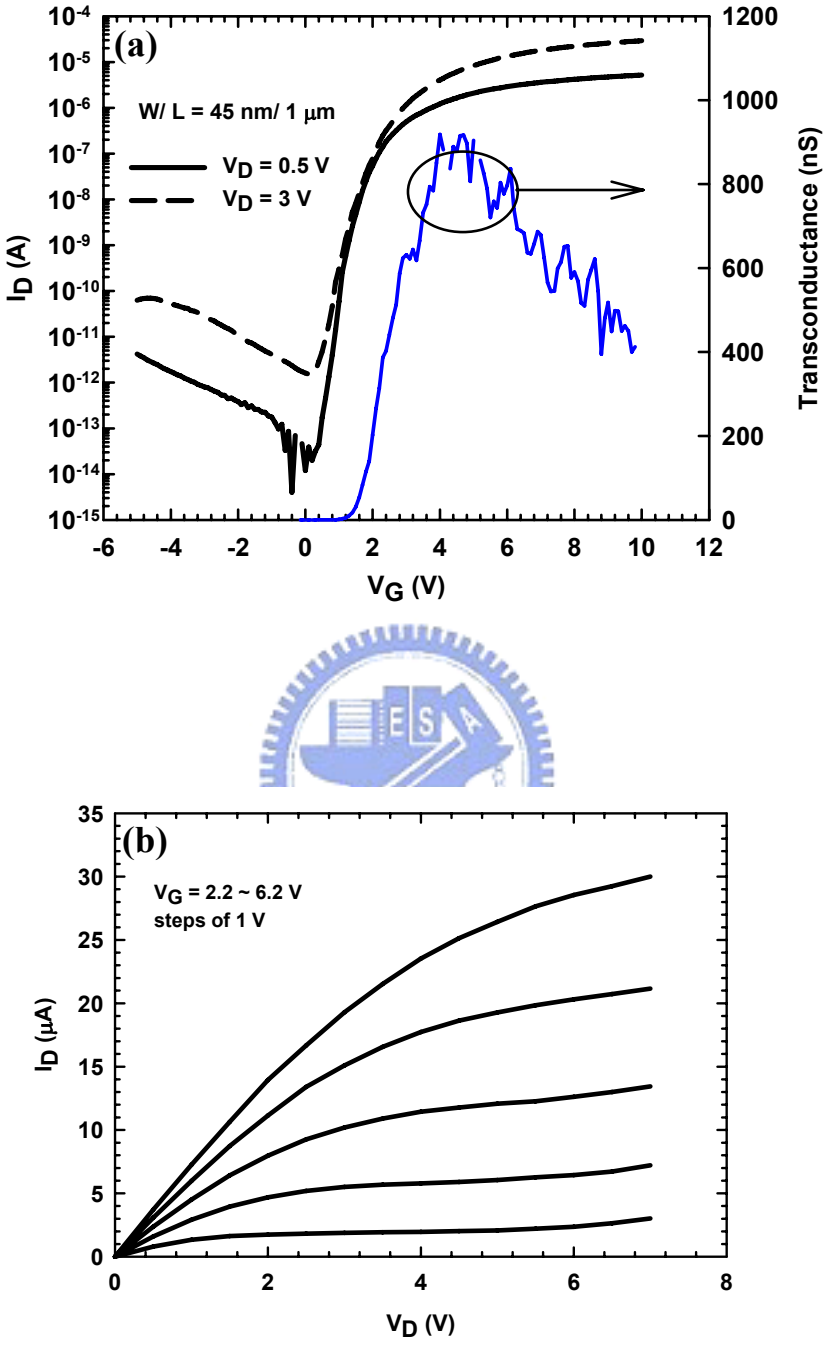


Fig. 3-7 (a) Transfer and (b) output characteristics of an MILC device with ASW configuration.

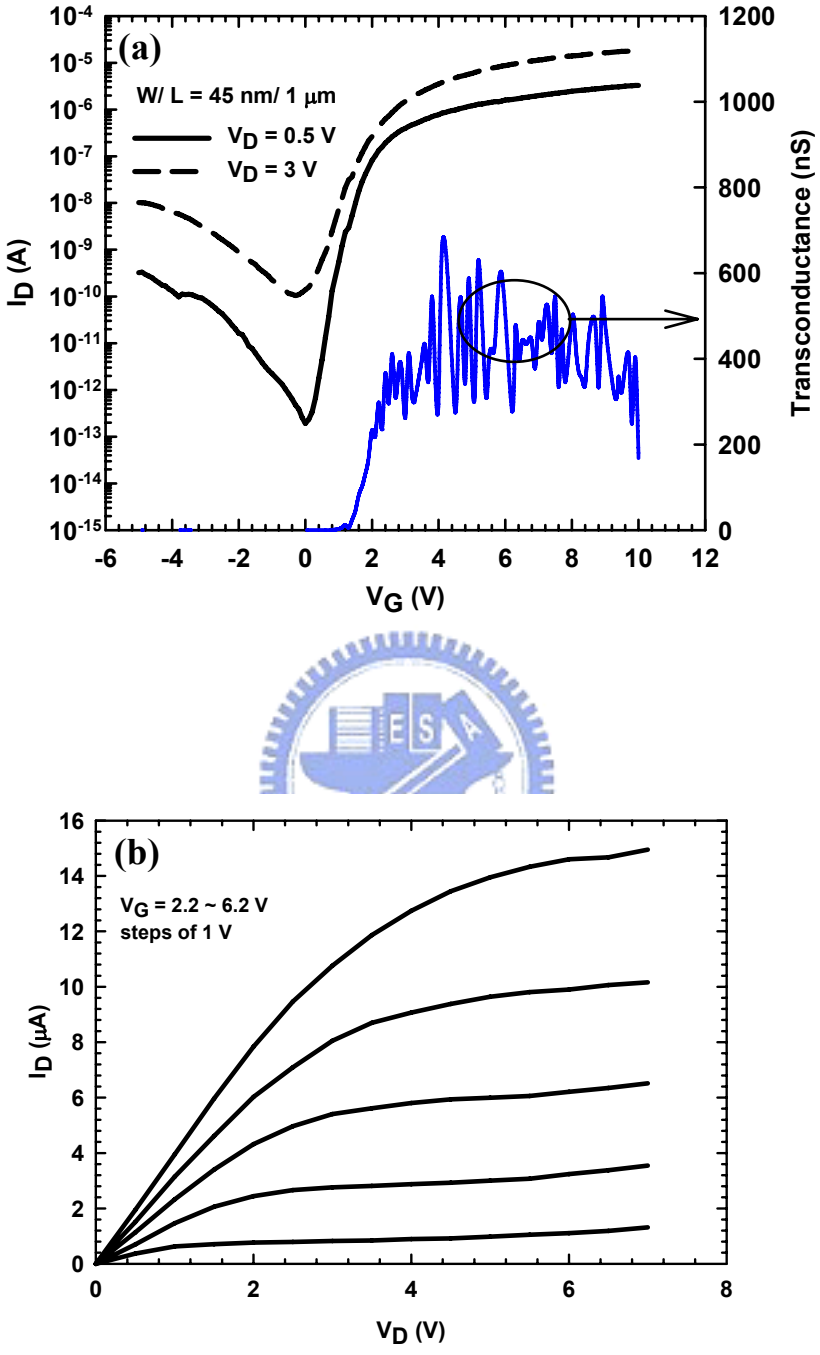
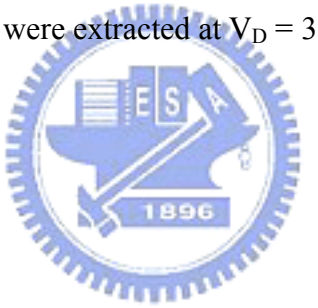


Fig. 3-8 (a) Transfer and (b) output characteristics of an MILC device with SSW configuration.

Table 3-I Comparisons of device parameters for ASW MILC and SSW MILC TFTs.

	ASW	ASW (RTA)	SSW	SSW (RTA)
V_{th} (V)	1.62	0.03	1.50	0.44
S.S. (V/dec)	0.29	0.16	0.40	0.19
μ_{FE} (cm^2/V-s)	252	550	201	313
I_{ON}/I_{OFF} ($x10^6$)	18.9	52.9	0.181	18.7

All parameters were extracted at V_D = 0.5 V except for the off-state current, I_{OFF}, and ON/OFF ratio, I_{ON}/I_{OFF}, which were extracted at V_D = 3 V.



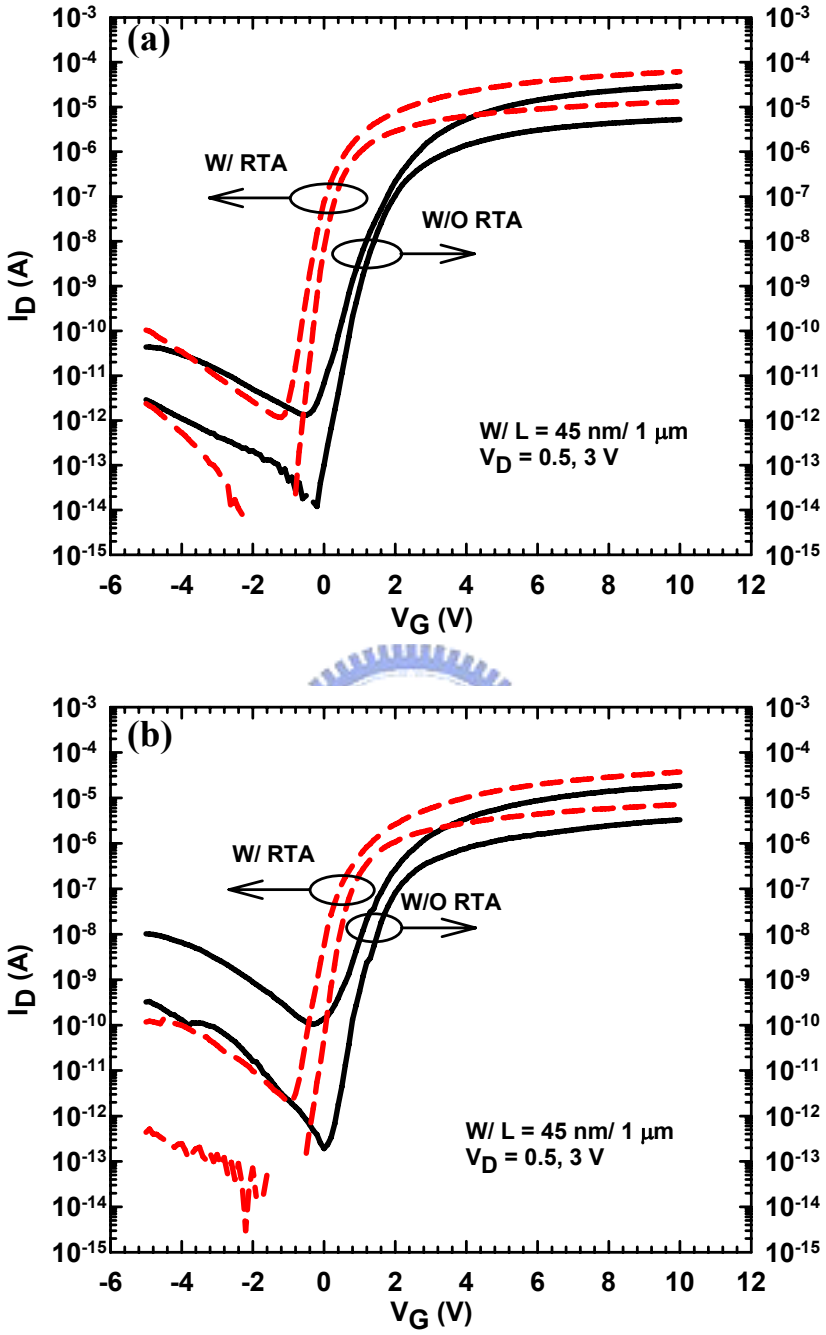


Fig. 3-9 Transfer characteristics of MILC devices with (a) ASW and (b) SSW configuration with and without RTA treatment.

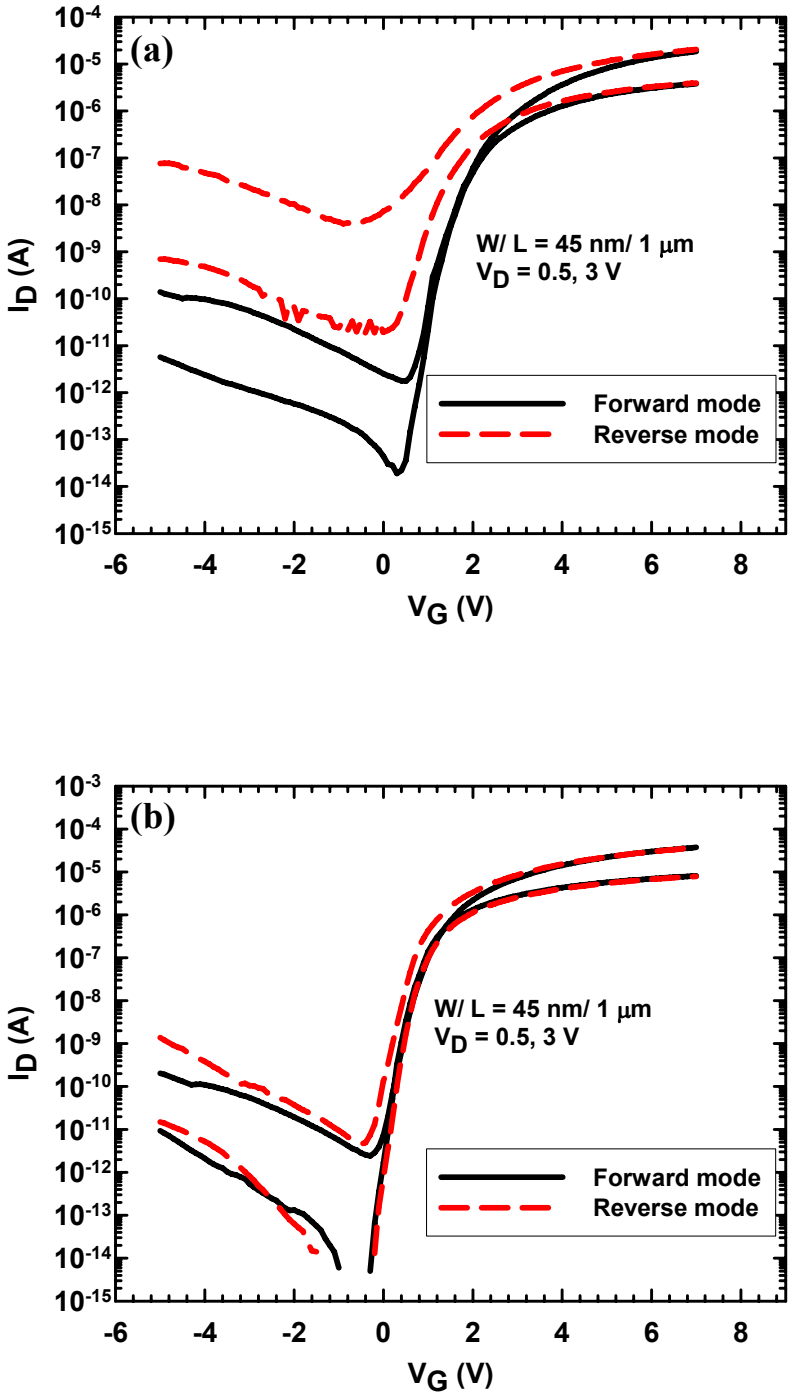


Fig. 3-10 Transfer characteristics of ASW MILC devices (a) without and (b) with RTA treatment under forward and reverse modes of operation.

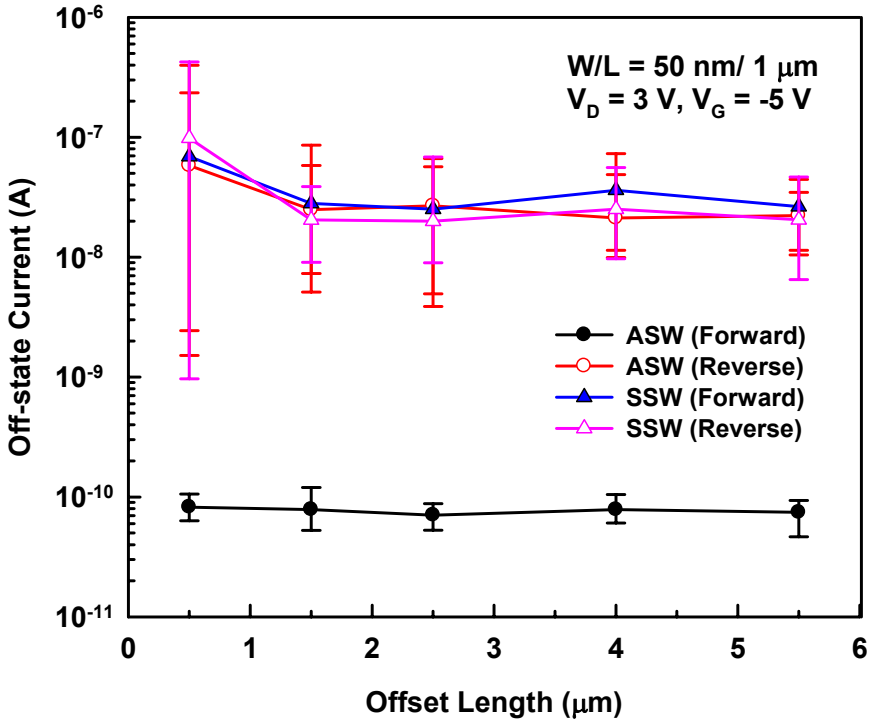


Fig. 3-11 Off-state leakage current as a function of the offset length for ASW and SSW devices operated in forward and reverse modes, respectively. The number of devices characterized for each condition is 20.

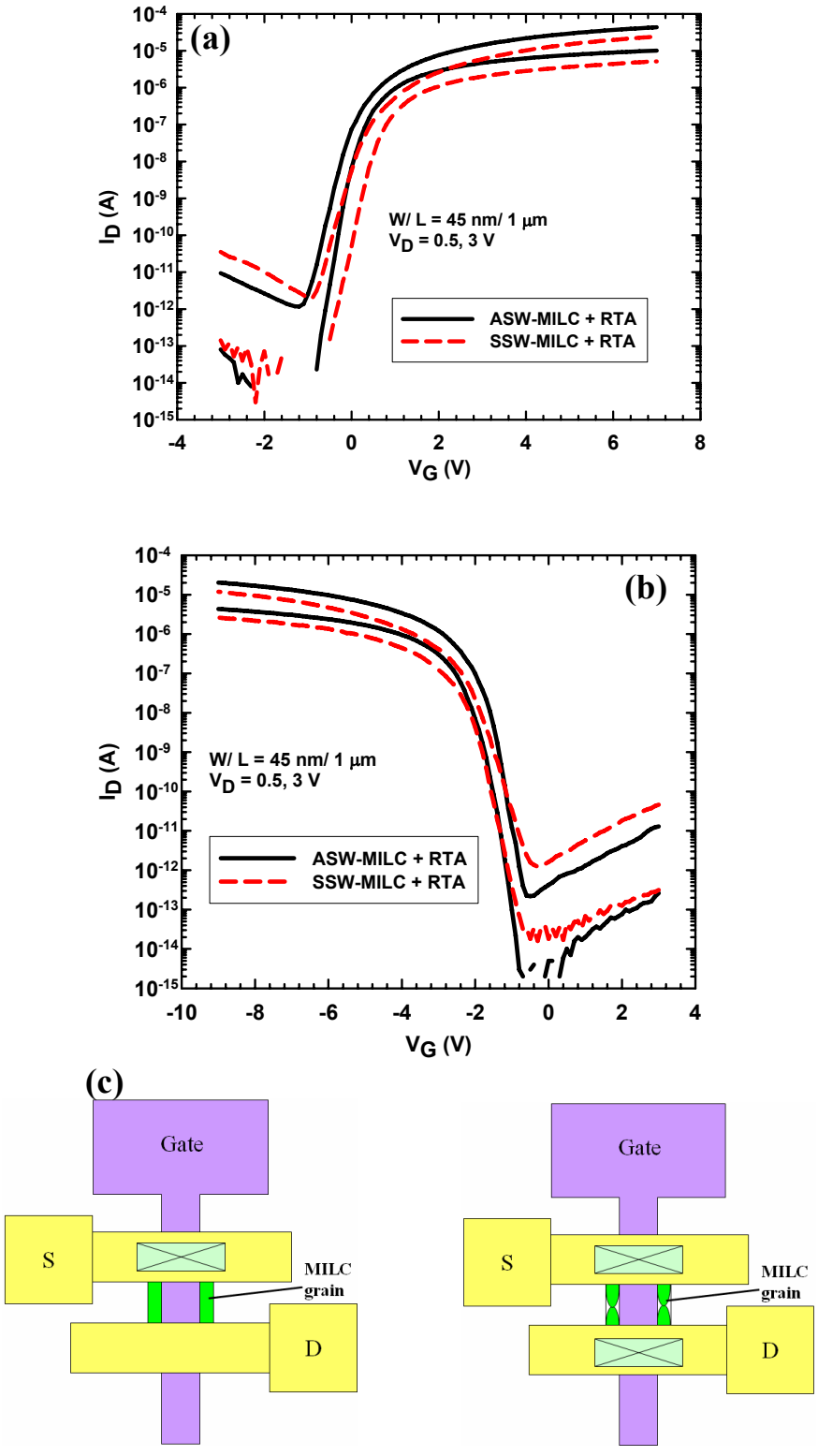


Fig. 3-12 Comparisons of transfer characteristics for ASW and SSW structures with L = 1µm in (a) n-TFTs and (b) p-TFTs. (c) Schematic grain distribution in NW channels for ASW and SSW configurations.

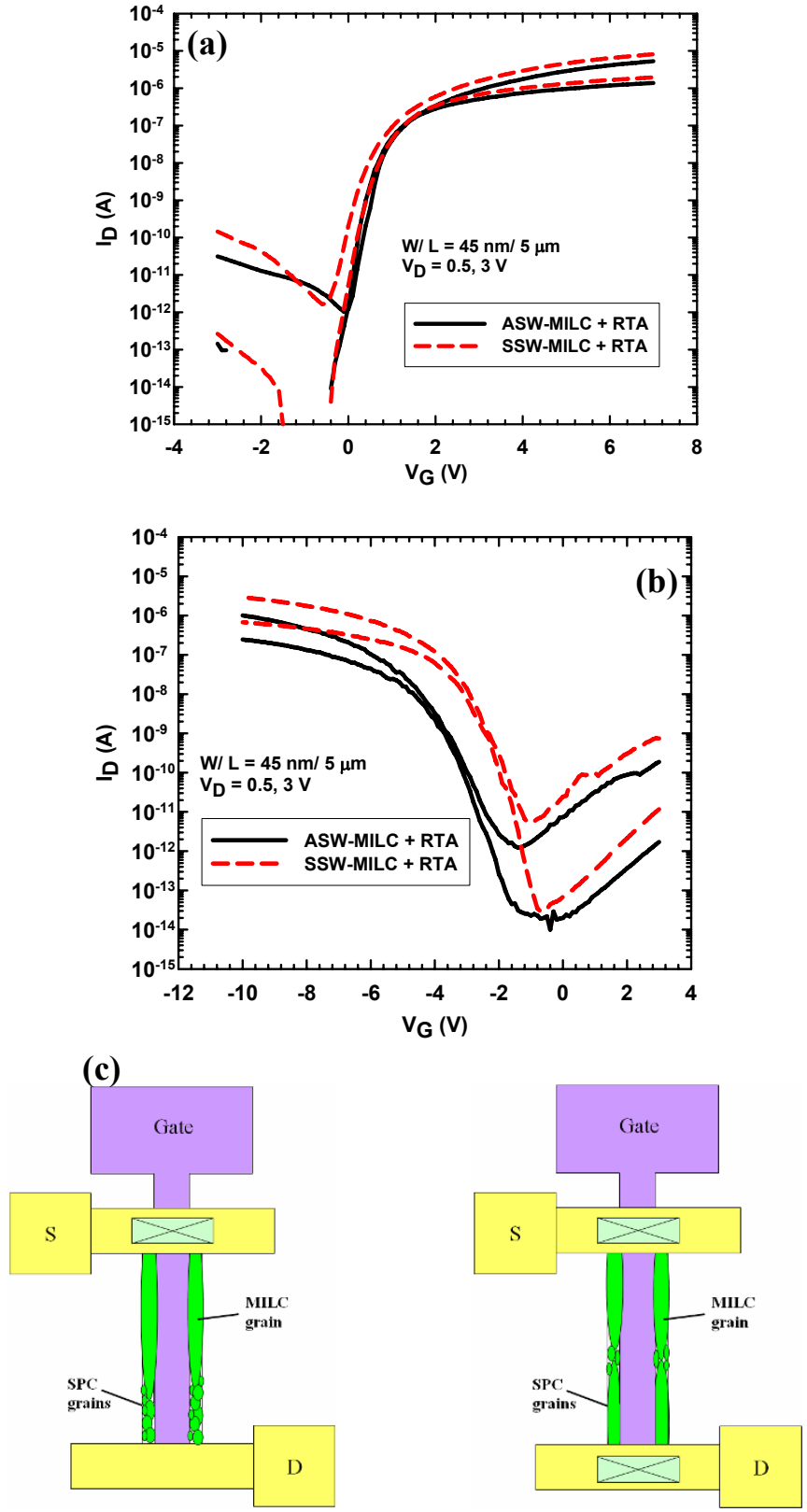


Fig. 3-13 Comparisons of transfer characteristics for ASW and SSW structures with L = 5 µm in (a) n-TFTs and (b) p-TFTs. (c) Schematic grain distribution in NW channels for ASW and SSW configurations.

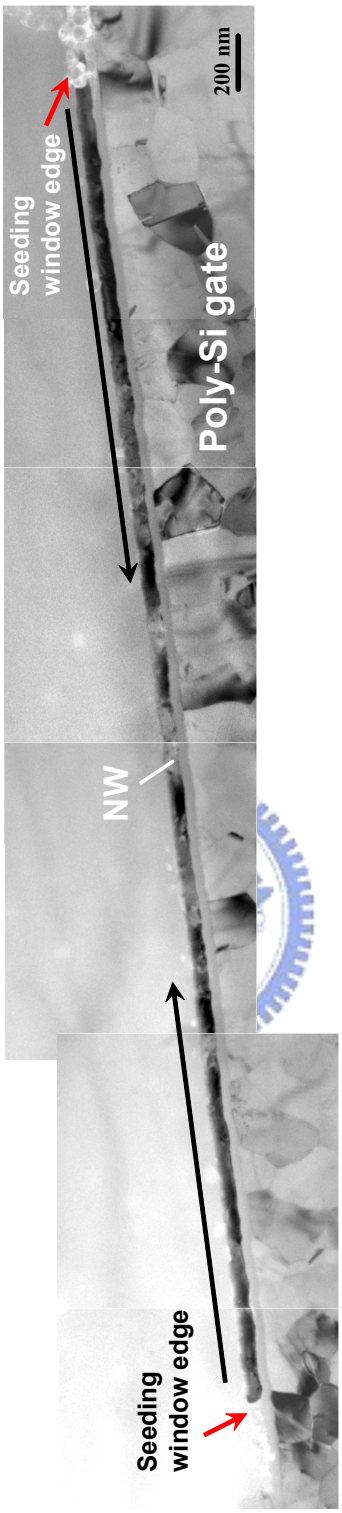


Fig. 3-14 Successive TEM pictures taken in the two adjacent seeding windows.

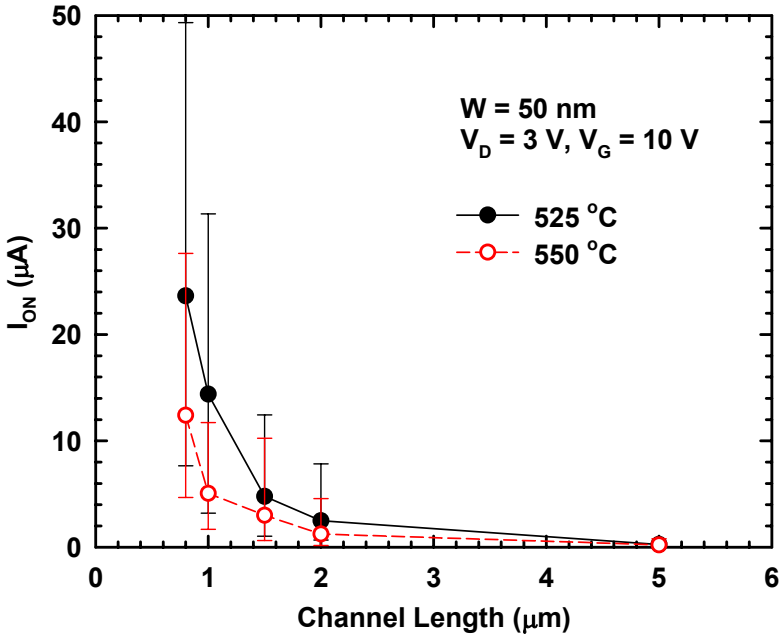


Fig. 3-15 On-current as a function of the channel length for devices re-crystallized at 525 °C and 550 °C, respectively. The number of devices characterized for each condition is 20.

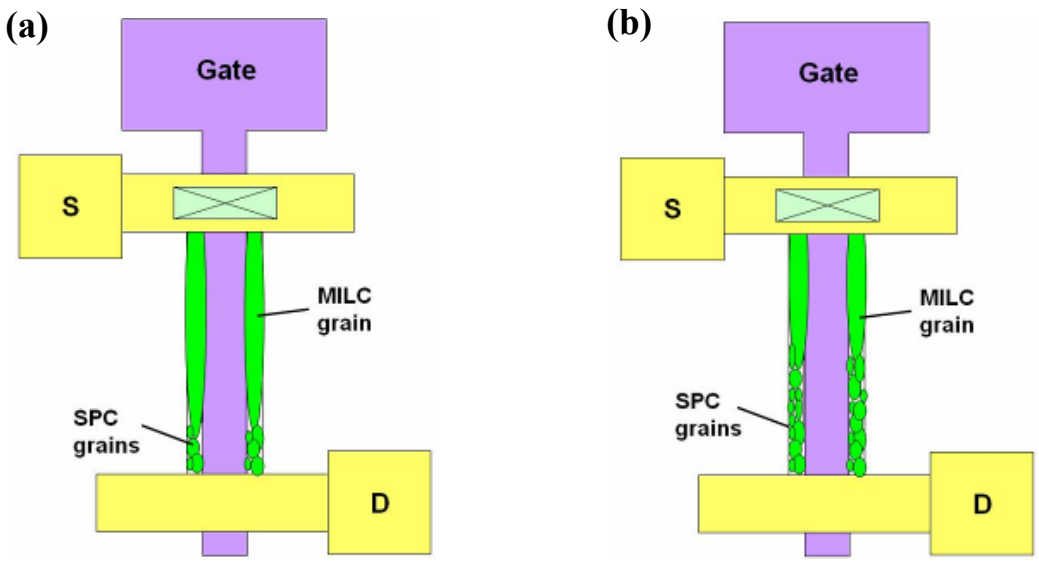


Fig. 3-16 Schematic illustration for the crystallinity of NW channels performed at (a) lower and (b) higher annealing temperatures during MILC process.

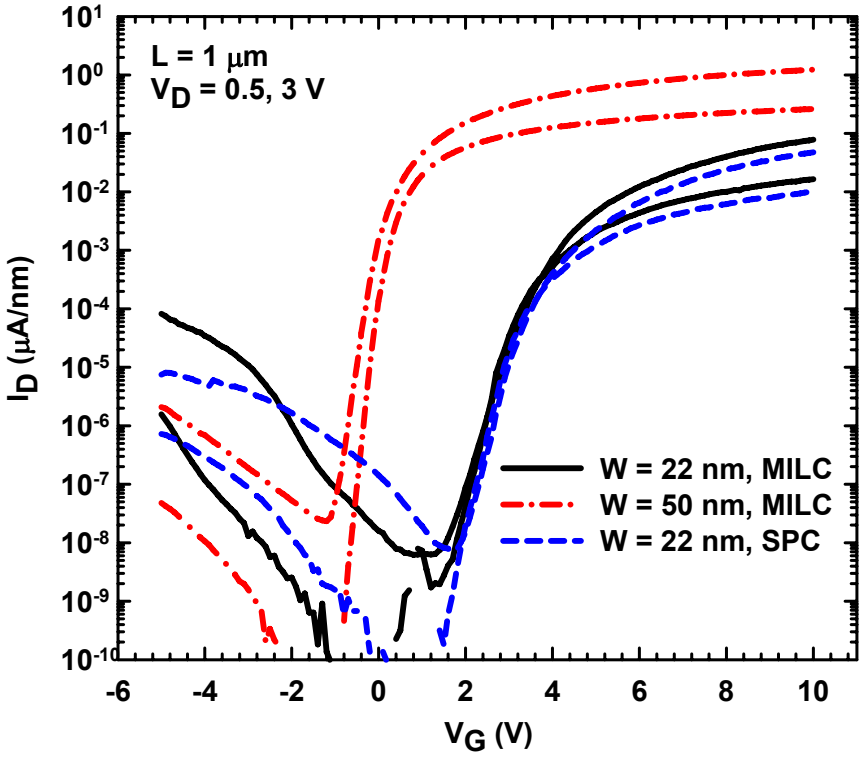


Fig. 3-17 Transfer characteristics of NW devices with various NW widths and crystallization approaches. All samples received RTA post-treatment. Note that the SPC sample was performed at 550 °C for 16 hours.

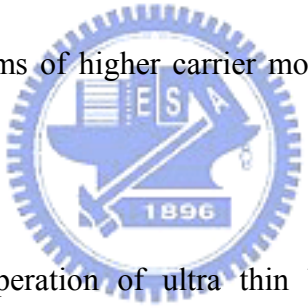
Chapter 4

Poly-Si Nanowire Thin-Film Transistors with Multiple-Gated Configuration

In this chapter, a novel multiple-gated (MG) thin-film transistor (TFT) with poly-Si nanowire (NW) channels is fabricated using a simple and straightforward manner. Since poly-Si NW is with a tiny volume, MG configuration is expected to significantly improve the performance of poly-Si NW devices. In the proposed transistors, poly-Si NWs were formed in a self-aligned manner and were precisely positioned with respect to the source/drain, and the side-gate. In addition, the NW channels are surrounded by three gates, i.e., top-, side- and bottom-gates, resulting in much stronger gate controllability over the NW channels, thus dramatically boosting the device performance over conventional single-gated TFTs. Another great benefit of such scheme is that the independently applied top-gate and/or bottom-gate biases could be utilized to adjust the threshold voltage of NW channels in a reliable manner, making it very favorable for practical applications. Furthermore, for better comprehension of geometric structure influencing MG operation, diverse dimensions of NWs were designed for investigation.

4.1 Introduction

Field-effect transistors (FETs) constructed of Si NWs are promising candidates for extremely downscaled MOSFETs as substitutes for traditional bulk devices [4.1-4.3]. With their inherently high surface-to-volume ratio, Si NWs lend themselves nicely to superior gate controllability over the NW channels, and thus suppressing the undesirable short-channel effects (SCEs) encountered in conventional nanoscale FETs [4.4, 4.5]. Moreover, owing to their small body and the accompanying reduction in defects, NWs serving as the channel in TFTs has been demonstrated with excellent performance [4.3, 4.6], in terms of higher carrier mobility and steeper subthreshold slope (S.S.).



Concurrently, for the operation of ultra thin body MOSFETs, it has been experimentally and theoretically shown that double- and triple-gated configurations can substantially improve the device performance in terms of higher on-current (I_{ON}), steeper S.S., as well as suppressed SCEs, owing to the stronger gate controllability over the channel [4.5, 4.7]. The combination of an ultra-thin channel layer with MG structure can further improve the device performance [4.8, 4.9]. MG NW devices therefore represent a potential and interesting device architecture for practical applications, although several issues relating to device preparation need to be resolved first. For example, the reported bottom-up approaches are usually plagued by

concerns such as positioning, alignment, and precise structural parameter control of NWs [4.1-4.3]. On the other hand, advanced lithography tools and expensive materials are required for top-down approaches to generate the nanoscale patterns [4.4, 4.5, 4.10]. To address these issues, we have recently proposed a novel NW TFT fabrication method which features the precise-positioning of NWs and good controllability over NW dimensions, while requiring only very simple processing without involving costly production tools or materials as described in Chapter 2 [4.6, 4.11]. Nevertheless, the fine-grain structure of poly-Si NW is considered to hinder carrier transport and constrain device performance. Several ways are possible to alleviate such concern. One is to enhance the film crystallinity by implementing available schemes such as metal-induced lateral crystallization (MILC) in the fabrication as described in Chapter 3. An alternative strategy is to boost the gate controllability over the channel with the adoption of MG configuration. Since poly-Si NW is with a small body and high surface-to-volume ratio, MG architecture is expected to improve the performance of poly-Si NW devices. Moreover, the MG configuration may consist of several separate gates and each gate can be biased independently. Such design allows more freedom for device operation [4.12]. In our previous works, single-gated operation was demonstrated. In this study, only with a

slight modification in device manufacture and mask design, a unique MG NW TFT is fabricated and characterized.

4.2 Device Structure and Fabrication

4.2.1 Fabrication Process

Basically, the new MG NW device is constructed from the sidewall-spacer NW device scheme. Principal fabrication steps and process flow are schematically illustrated in Figs. 4-1 and 4-2, respectively. First, an n^+-poly-Si layer was deposited and patterned as the side-gate (SG) on a Si substrate covered with a 100 nm-thick thermally-grown SiO_2 layer. A 40 nm tetraethyl orthosilicate oxide (TEOS-SiO_2) layer was then deposited by low-pressure chemical vapor deposition (LPCVD) to serve as the SG dielectric, followed by the deposition of 100 nm amorphous Si (a-Si) channel layer. Next, to transform the a-Si layer into polycrystalline state, a solid-phase crystallization (SPC) treatment was executed at 600 ^oC for 24 hours in a furnace. Subsequently, source and drain (S/D) doping was performed by phosphorus ion implantation with a dose of 1 x 10^{15} cm^{-2} at 15 keV (Fig. 4-1(a)). Afterwards, NW channels and S/D regions were formed simultaneously by an anisotropic plasma (Cl_2/ HBr) dry-etching step, and the resultant structure is shown in Fig. 4-1(b). Note that

the low implant energy was chosen to ensure that the dopants were located near the top portion of the poly-Si layer, so the poly-Si NWs remained undoped. The dopant activation was performed at 900 ^{o}C for 30 sec. A 200 nm-thick TEOS was then deposited to serve both as the top-gate (TG) oxide and passivation layer. Afterwards, an Al-Si-Cu metal layer was deposited and patterned to form the TG electrodes as well as S/D and SG contact pads. It is worth noting that the NW channels formed by the unique sidewall spacer etching technique are literally surrounded by the three gates, as schematically shown in Fig. 4-1(c). The top view of the fabricated device is shown in Fig. 4-1(d). In addition to the SG and TG formed in the fabrication sequence mentioned above, the Si substrate itself serves as the bottom-gate (BG). The process flow and fabricated structure are similar to that described in our previous work [4.6, 4.11], except that a TG is added lying over the passivation oxide. It should be noted that for the devices characterized in this work, the oxide thickness between the gate and the NW is 140 nm for the BG, 40 nm for the SG, and 200 nm for the TG, respectively. In this configuration, the three gates could be biased either independently or jointly. To reduce trap density and improve interface quality, the devices also received a NH_3 plasma treatment at 300 ^{o}C for 2 hours. It is particularly noteworthy that the overall fabrication process flow is very simple, and involves no costly lithography tools to form the NW structure.

4.2.2 Device Structure and Operation Modes of NW TFTs

Fig.4-3(a) is a scanning electron microscopy (SEM) photograph showing the top view of a device right after the step of NW and S/D definition (Fig. 4-1(b)). To clearly illustrate the structure, the oxide layer between the NWs and the side-gate is deliberately removed. The picture reveals the high fidelity of NW channels' alignment with respect to the SG as well as the S/D regions. The cross-sectional SEM image of a fabricated NW TFT with MG structure is shown in Fig. 4-3(b). This picture clearly shows that the NW channels are surrounded by the three gates (TG, BG and SG). Also shown in the figure is a close-up transmission electron microscopy (TEM) photograph exhibiting the triangular shape of the NW. The width (W) and thickness (t) of the NW structure defined in the picture are 30 nm and 40 nm, respectively. From these micrographic analyses, it can be clearly seen that the proposed approach provides a very simple method to form NW-channel devices with multiple gates.

In our previous studies [4.6, 4.11], the bias was applied only to the SG for controlling the device switching. Here we examine the drain current-versus-gate voltage (I_D-V_G) characteristics of MG configurations in reference to that of the SG operation. Three MG operation modes specified in Table 4-I were investigated, including two double-gated (DG-1 and DG-2) and one triple-gated (TriG) modes. For double-gated modes, the remaining gate was grounded throughout the measurements.

4.3 Results and Discussion

4.3.1 Multiple-gated Operation of NW TFTs

Fig. 4-4 sketches a NW surrounded by three gates and how electric filed of these gates exerting on the channel. SG is expected to exhibit better controllability thanks to the thinner SG oxide. Figs. 4-5(a)-(c) present and compare the transfer characteristics of a NW device under the three modes of operations with that of SG operation. The significant merits of MG operations include lower threshold voltage (V_{th}), steeper S.S. and higher I_{ON}, owing to the stronger gate controllability over the NW channels. With these merits, ON/OFF current ratio higher than 10^7 is achieved. Output characteristics for all modes of operations are shown in Fig. 4-5(d), in which the I_{ON} at $V_G = V_D = 3$ V is 1.3, 1.5 and 1.8 times that of SG operation under DG-1, DG-2 and TriG modes, respectively. For the two double-gated modes, the performance is better under DG-2 mode. This is mainly attributed to the thinner gate dielectric used for the BG. Fig. 4-6 shows the transconductance ($G_m = dI_D/dV_G$ at $V_D = 0.5$ V) characteristics under various modes. Due to the more effective conduction width evoked under the active gates, the MG operations indeed yield higher G_m as compared with the SG mode. To visualize this phenomenon, simulated electron densities in the two-dimensional cross-sectional area of the NW channel for on-state operation of DG-1, DG-2 and TriG modes are illustrated in Fig. 4-7. The simulation was carried using an ISE

TCAD (Integrated Systems Engineering Technology-Computer-Aided Design) tool and the applied voltages to the active gates were all +5V [4.13]. It is evident that more carrier density is induced with the MG modes. The enhancement in gate controllability also effectively reduces the subthreshold leakage current path inside the NW. This consistently explains the steeper subthreshold slope of MG modes than that of SG mode. Moreover, the increase in the effective conduction channel width leads to higher I_{ON} and G_m, especially under TriG mode of operation. The electron density is higher around the corners owing to the high electric-field strength. To quantitatively compare device performance among different modes, several important electrical parameters are summarized in Table 4-II.

To further highlight the enhancement in gate controllability under MG configuration, I-V characteristics of a device operated under individual gate control are measured first, and then the sum is compared with that of MG operations. In Fig. 4-8, the characteristics of the three individual gate control modes are shown. In the measurements the two remaining gates were grounded, therefore these curves have a common intersection point at zero gate voltage. As can be seen in the figure, TG and BG operations exhibit larger S.S. and lower on-state current than those under SG operation, which is reasonable because of their thicker gate dielectrics.

The effectiveness of the MG configuration in improving the device performance can be understood from the results shown in Figs. 4-9~4-11. In Fig. 4-9, the curves denoted as “SG + TG” indicate the sum of currents under individually side-gated and individually top-gated operations, as shown in Fig. 4-8. From the inset in the figure, it can be seen that the on-state current of the DG-1 mode is larger than the sum of the two single-gated modes. On the other hand, the subthreshold current is much smaller than the sum of the two single-gated modes. Similar findings are also observed for DG-2 and TriG modes of operations, as depicted in Figs. 4-10 and 4-11, respectively. The above phenomena are attributed to the strong coupling of the two adjacent gates during the MG operation, which tends to increase the effective conduction width in the on-state, leading to a higher conduction current. While it tends to reduce the area of leakage path, thus a reduced subthreshold leakage is obtained. These effects are magnified as the “body” of NW is tiny. Fig. 4-12 displays the percentage increase in I_{ON} for the MG modes over the sum of individual operations. It can be seen that TriG mode indeed shows the most significant improvement.

4.3.2 Effects of NW Channel Dimension

In the previous section, electrical characteristics of the NW TFT have been investigated and it is found that the improvement is mainly due to the combination of

tiny NW structure and gate coupling effect. To obtain better understanding of such phenomenon, influence of geometric structure variation of NW channels is discussed in this subsection, and for simplicity, the discussion will focus on the DG-1 mode.

(A) Impacts of NW Length

Fig. 4-13 illustrates the enhancement of S.S. and I_{ON} under DG-1 operation compared with SG mode. At first glance, the improvement is more pronounced for the device with channel length of 5 μm. The comparatively less I_{ON} enhancement for short channel devices is attributed to SCEs. In addition, as mentioned earlier, if more grain boundaries and defects exist in the fine grain texture of poly-Si NWs, carrier transport in the channel would be seriously impeded. Therefore, this effect should be more noticeable in long channels with correspondingly lower carrier mobility. The concept of DG operation to lessen such influence is by exploiting vertical electric field to lower the barrier height generated by defects, and hence carriers could transport more freely in the channel as schematically illustrated in Fig. 4-14. Consequently, SG operation when coupled with the additional control of TG is conducive to eliminate more obstacles existing in the long channel devices, so more apparent I_{ON} enhancement is obtained. This is also evidenced by the S.S. reduction as shown in Fig. 4-13.

(B) Impacts of NW Thickness

To investigate the effect of NW thickness on gate coupling, devices with L = 1 μm and various cross-sectional channel area were designed. S.S. and G_m values acquired from SG and DG-1 modes of operation were studied since these parameters could reflect gate controllability straightforwardly. Fig. 4-15 shows the dependence of S.S. and G_m enhancement on NW cross-sectional area. For channel thickness and width smaller than 35 nm, G_m improvement almost saturates. However, about 10 % decrease in the enhancement is found for device with W = 54 nm and t = 54 nm. This reduction indicates less gate-coupling effect of DG operation, which could be ascribed to the thicker channel body [4.14]. S.S. behaviors reveal similar trend as well. These results indicate that the benefit of DG operation diminishes when the dimension of NW is larger than 35 nm.

4.3.3 Tunable Threshold Voltage of MG NW TFTs

In addition to the MG operations demonstrated above, V_{th} adjustment by applying a fixed TG and/or BG bias is also feasible in the proposed device structure. Figs. 4-16(a)-(c) show typical results in this aspect. In the figures, the SG acts as the active gate for controlling the device switching behavior. For each curve, a specific

voltage (V_{set}) ranging from -4 V to +4 V is applied to TG (V_{TG}, Fig. 4-16(a)) or BG (V_{BG}, Fig. 4-16(b)) alone, or jointly (V_{TG-BG}, Fig. 4-16(c)). It can be found that the curves are shifted in parallel by varying the biases. This is because the potential of NW channel is modulated by V_{set}. Similar threshold voltage modulation has been studied on double-gated SOI devices previously, and was ascribed to the potential profile adjustment in the channel by the V_{set} [4.7, 4.15]. To qualitatively understand the situation, band diagrams of the NW under the influence of the gate bias conditions are shown in Fig. 4-17. When negative V_{set} is applied, it is conducive to suppress the generation of inversion charges in the channel, hence resulting in higher V_{th}. On the other hand, lower V_{th} is obtained when V_{set} is positive.

Fig. 4-18 shows V_{th} as a function of the applied V_{set} extracted from the data shown in Figs. 4-16(a)~(c). The results reveal that V_{th} could be linearly tuned to a suitable range. Magnitude of the slope can be regarded as an indicator that reflects the tuning capability of V_{set}. Among the three cases, the slope is the smallest when V_{set} is applied to TG only, due to the thick oxide used. The field strength is reduced with a thicker oxide, so the potential adjustment capability is degraded accordingly. While the largest slope is obtained when V_{set} is applied to both TG and BG, thanks to the strong gate coupling effect mentioned above. Similarly, for DG modes of operations, V_{th} could also be modulated by applying V_{set} to the remaining gate, as depicted in

Figs. 4-19 and 4-20. However, the tuning ability of V_{set} declines under DG modes as compared with that under SG mode. For instance, ΔV_{th} set by BG for SG and DG-1 mode are 0.40 and 0.36, respectively. This is because SG coupling with TG could induce stronger control over the channel, and BG comparatively exhibits less effect on the V_{th} adjustment. Nevertheless, these results suggest that the threshold voltage of the new MG NW TFT could be easily adjusted to suit various applications.

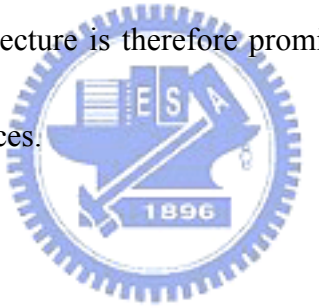
For NW devices, the variation of structural parameters such as the feature size of the NW and the gate dielectric thickness, as well as dopant concentrations in the channel, could result in large fluctuation in V_{th}. Yet, in the proposed method, V_{th} could be modulated by an electrical manner, and therefore the issue could be effectively resolved. Note that, the unique capability of electrically tuning the threshold voltage in the new NW structure is beneficial not only for circuit applications in electronics, but also for gas and biologic sensing applications. As described in a previous paper [4.6], the new NW architecture could be applied to chemical and biological sensing purposes, as some portion of the channel is exposed to the environment, as schematically shown in Fig. 4-21. After immobilization treatment, receptors are formed on the surface of the exposed channel. During the sensing stage, the receptors can capture the target species contained in the test environment with good selectivity, and the charges brought with the captured target

species will modulate the channel conductance. Overall the detection process functions as a virtual gate in the FET operation, and thus in reality the device is doubled-gated when the side-gate is also considered. To make the detection highly sensitive, it would be better if the device is operated in a bias condition in which the channel conductance is most sensitive to the surface charges. This could be achieved by applying a proper voltage (V_{set}) to the side-gate according to the above analyses, as shown in the figure. The applied side-gate voltage could be generated from a control circuit designed and fabricated by using modern complementary metal-oxide-semiconductor (CMOS) technology. This certainly increases the feasibility of the new NW device in practical applications.

4.4 Summary

In conclusion, a new poly-Si NW device with MG configuration was proposed and studied in this chapter. The NW channels are surrounded by three gates, i.e., top-, side- and bottom-gates, fabricated with a very simple and controllable process flow. With MG operations, excellent electrical characteristics such as high ON/OFF current ratio of 10^7 and subthreshold slope of 250 mV/dec are obtained, which are significantly better than those reported in the previous work using only the side-gate

to control the device switching. The strong gate coupling effect of the MG operation, which is ascribed to the tiny body of NW channels, accounts for the observed improvement. The effect of NW volume on DG operation and gate coupling effect was investigated likewise. It is found that the benefit of DG control diminishes as the diameter of NW is larger than 35 nm. Moreover, the independently applied TG or/and BG biases can be employed to regularly adjust the V_{th} of NW channels in a reliable manner. The experimental results indicate that the V_{th} could be modulated by the gates with both positive and negative biases, making it suitable for practical applications. The proposed NW TFT architecture is therefore promising for future manufacturing of high-performance NW devices.



References

[4.1] Y. Cui and C. M. Lieber, “Functional nanoscale electronic devices assembled using silicon nanowire building blocks,” *Science*, **291**, 851 (2001).

[4.2] Y. Cui, Z. Zhong, D.Wang, J.Wang and C. M. Lieber, “High performance silicon nanowire field effect transistors,” *Nano Lett*., **3**, 149 (2003).

[4.3] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles and J. L. Goldman, “High-performance thin-film transistors using semiconductor nanowires and nanoribbons,” *Nature*, **425**, 274 (2003).

[4.4] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu and C. C. Huang *et al*, “5 nm-gate nanowire FinFET,” *Symp. VLSI Tech. Dig.*, 196, June 15-17 (2004).

[4.5] B. Yu , L. Chang, S. Ahmed, H. Wang, S. Bell, C. Y. Yang, C. Tabery, C. Ho, Q. Xiang, T. J. King, J. Bokor, C. Hu, M. R. Lin, D. Kyser,” FinFET scaling to 10nm gate length,” *IEDM Tech. Dig.*, 251 (2002).

[4.6] H. C. Lin, M. H. Lee, C. J. Su and S. W. Shen, “Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels,” *IEEE Trans. Electron Devices*, **53**, 2471 (2006).

[4.7] H. S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wang and J. J. Welser, "Nanoscale CMOS," *Proc. of the IEEE*, **87**, 537 (1999).

[4.8] S. D. Zhang, C. Zhu, J. K. O. Sin and P. K. T. Mok, "Ultra-thin elevated channel poly-Si TFT technology for fully-integrated AMLCD system on glass," *IEEE Trans. Electron Devices*, **47**, 569 (2000).

[4.9] H. Kuriyama, Y. Ishigaki, Y. Fujii, S. Maegawa, S. Maeda, S. Miyamoto, K. Tsutsumi, H. Miyoshi and A. Yasuoka, "A C-switch cell for low-voltage and high-density SRAM's," *IEEE Trans. Electron Devices*, **45**, 2483 (1998).

[4.10] Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka and R. S. Williams, "Sequence-specific label-free DNA sensors based on silicon nanowires," *Nano Lett.*, **4**, 245 (2004).

[4.11] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee and Y. S. Yang, "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel," *IEEE Electron Device Lett.*, **26**, 643 (2005).

[4.12] M. Masahara, Y. Liu, K. Sakamoto, K. Endo, T. Matsukawa, K. Ishii, T. Sekigawa, H. Yamauchi, H. Tanoue, S. Kanemaru, H. Koike and E. Suzuki, "Demonstration, analysis and device design considerations for independent double-gate MOSFETs," *IEEE Trans. Electron Devices*, **52**, 2046 (2005).

[4.13] *ISE-TCAD DESSIS User's Guide Version 10.0* 2004 (Zürich, Switzerland: Integrated Systems Engineering).

[4.14] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor and C. Hu, "A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, **47**, 2320 (2000).

[4.15] S. M. Koo, Q. Li, M. D. Edelstein, C. A. Richter and E. M. Vogel, "Enhanced channel modulation in dual-gated silicon nanowire transistors," *Nano Lett.*, **5**, 2519 (2005).

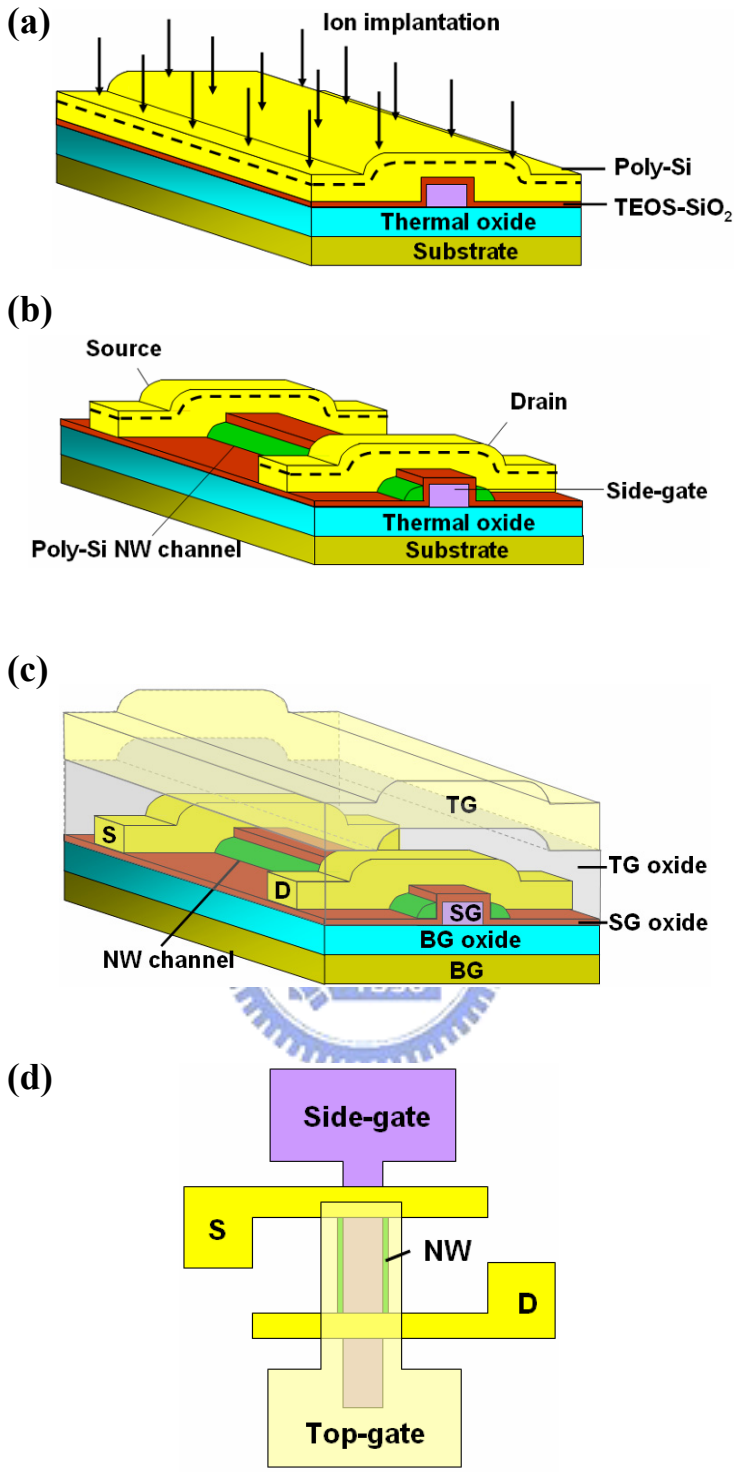


Fig. 4-1 Key fabrication steps of the MG NW TFT. (a) Source/drain ion implantation. The dashed line represents the projected range which is near the top surface due to the low implant energy used. (b) Formation of source, drain and NW channels. The NW channels remain undoped due to the low implant energy used. (c) Stereo-view of the fabricated NW TFT. Top-, side-, and bottom-gates are formed in the structure. (d) Top-view of the fabricated device.

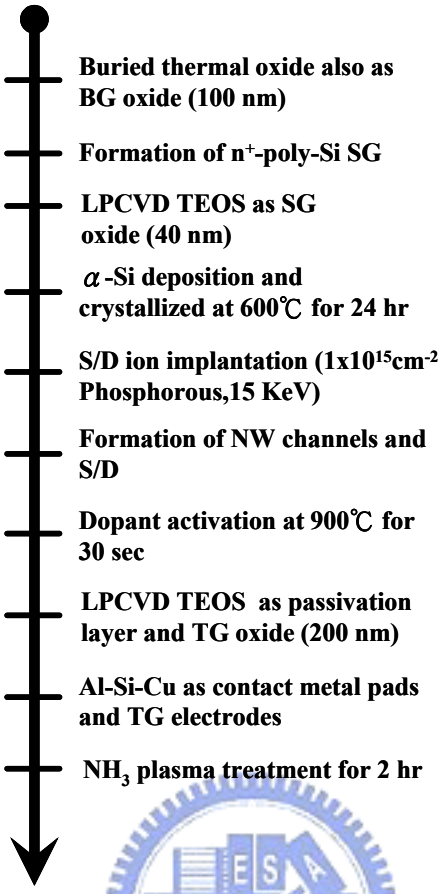


Fig. 4-2 Process flow for the fabrication of MG NW TFTs.

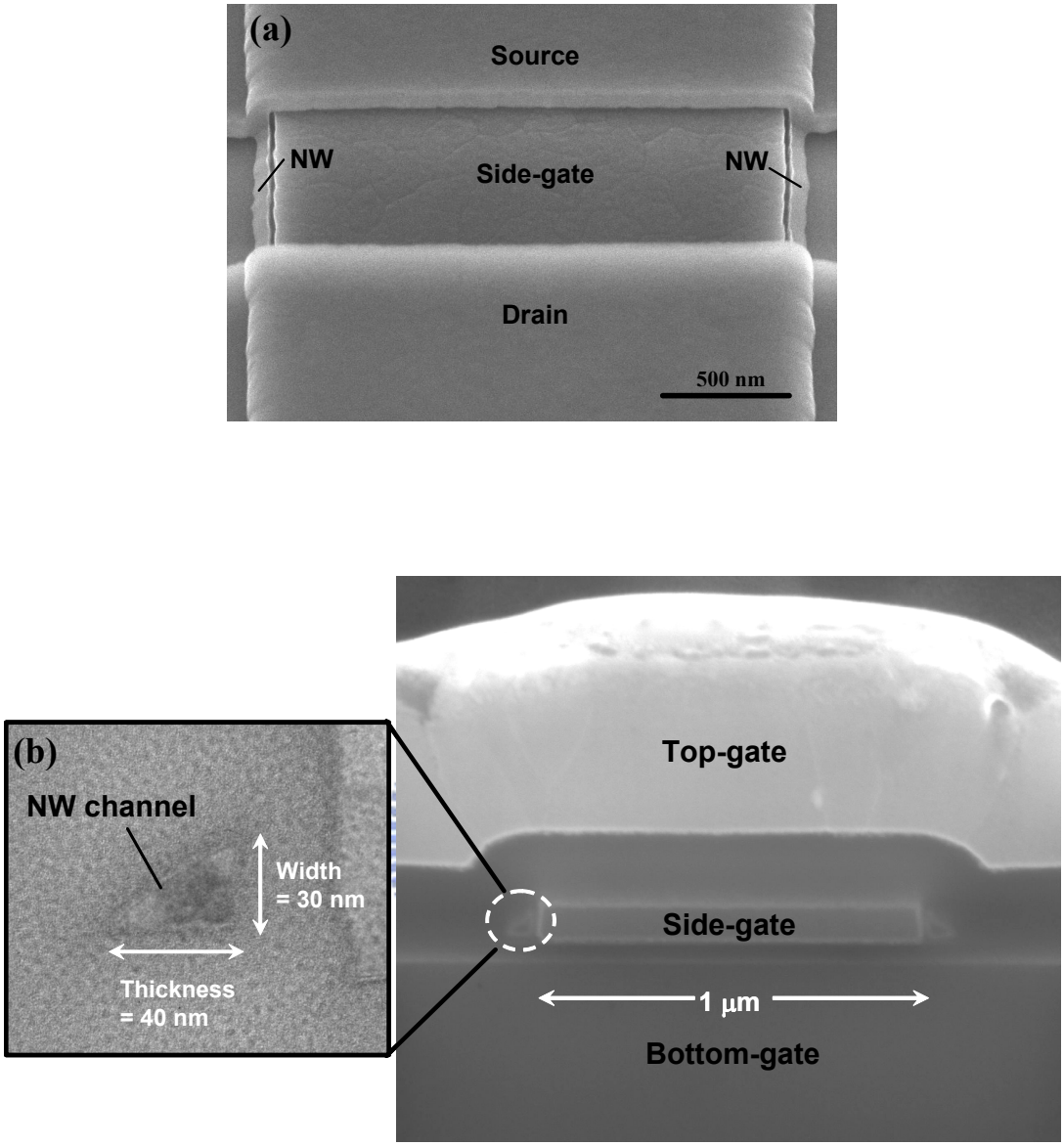


Fig. 4-3 (a) SEM image of a NW TFT before the deposition of passivation oxide and top-gate electrode, showing the self-aligned NW channels. (b) (Right) Cross-sectional view SEM photograph of a fabricated MG TFT showing NW channels surrounded by top-, side- and bottom-gates. (Left) Close-up TEM image of a NW channel specifying the width and thickness.

Table 4-I Active operating gates used in multiple-gated modes

gate \ mode	DG-1	DG-2	TriG
SG	active	active	active
TG	active	grounded	active
BG	grounded	active	active

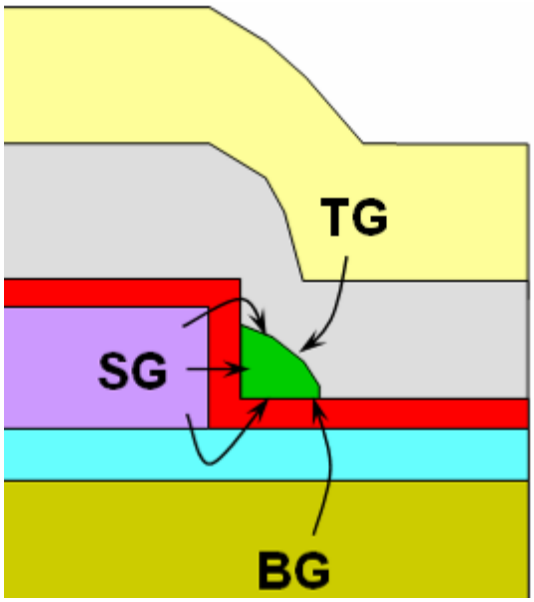


Fig. 4-4 Diagram of a NW channel under the control of the three gates.

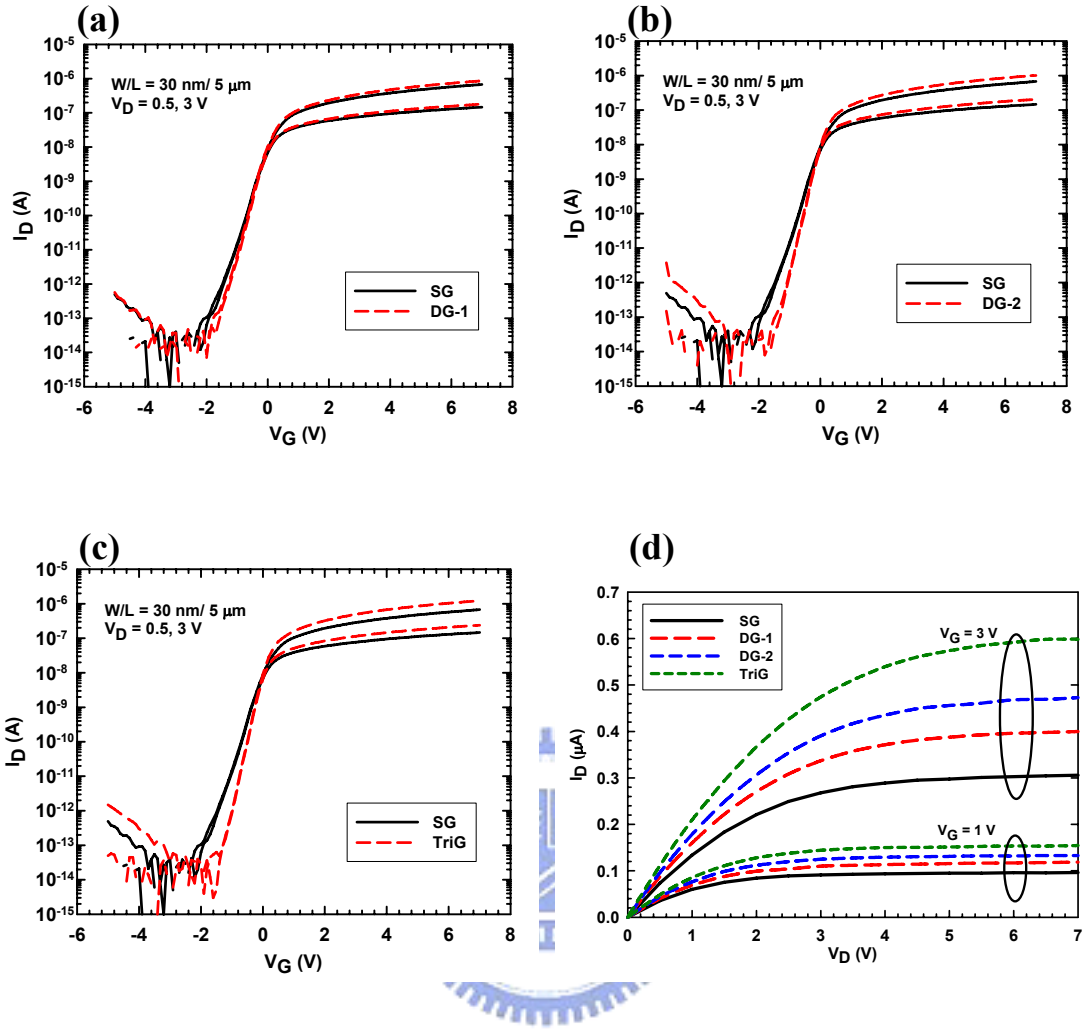


Fig. 4-5 Typical transfer characteristics of a NW TFT under (a) DG-1, (b) DG-2 and (c) TriG modes of operations compared with SG mode, respectively. (d) Comparisons of output characteristics between MG and SG modes of operations.

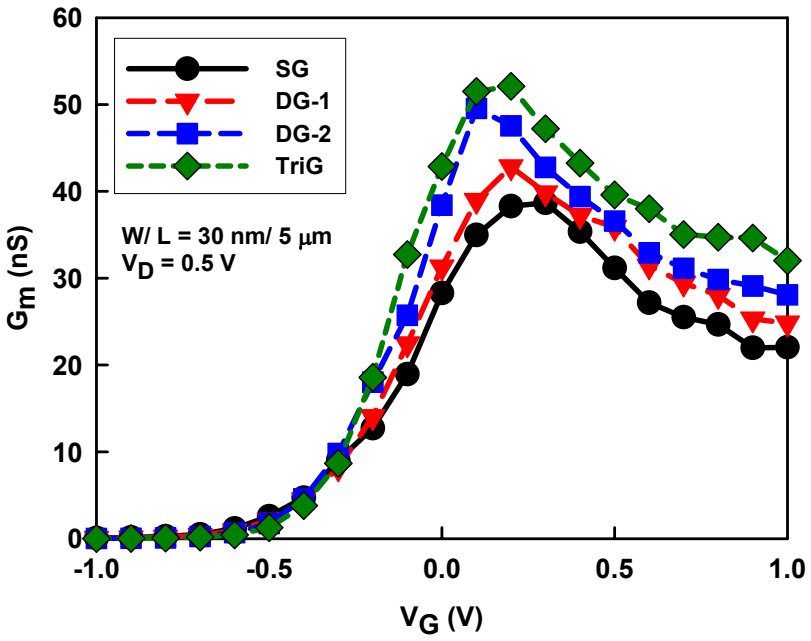


Fig. 4-6 Transconductance characteristics of a NW device under various modes of operation.

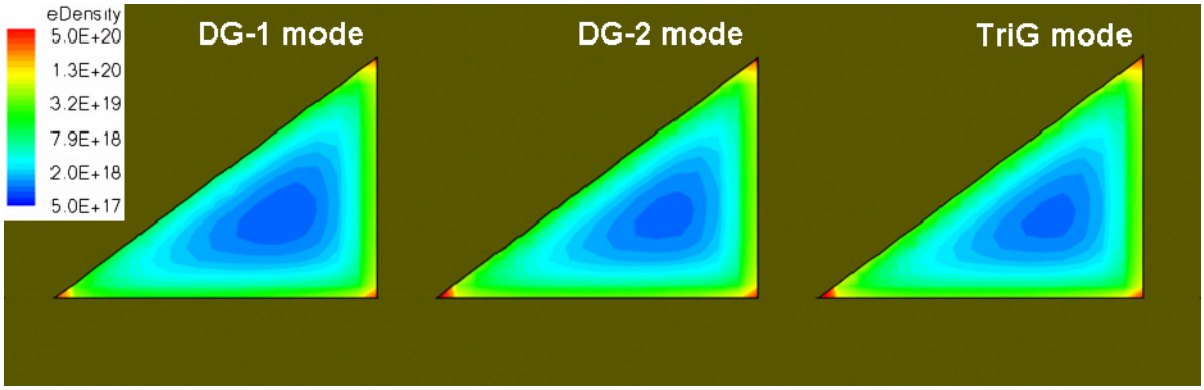


Fig. 4-7 2-dimensional simulation of electron density (eDensity) in NWs under DG-1, DG-2 and TriG modes of operation. The applied gate voltage is 5 V.

Table 4-II Comparisons of the electrical parameters among various modes of multiple-gated operations

	SG	DG-1	DG-2	TriG
V_{th} (V)	-0.45	-0.39	-0.34	-0.30
S.S. (V/dec.)	0.342	0.290	0.265	0.251
I_{ON} (A)	2.7×10^{-7}	3.4×10^{-7}	3.9×10^{-7}	4.8×10^{-7}
$G_{m,max}$ (nS)	42	45	55	60

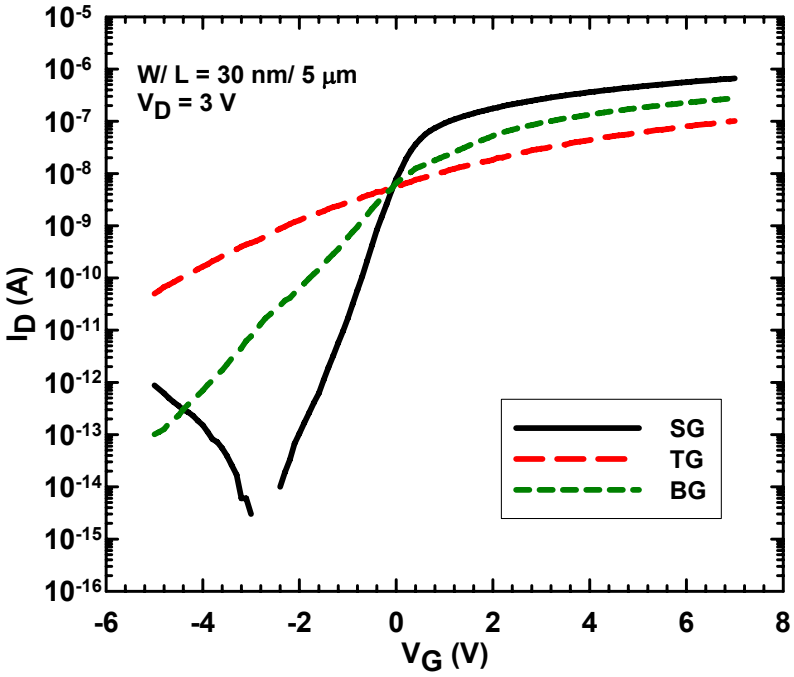


Fig. 4-8 I-V curves of single-gated mode of operation.

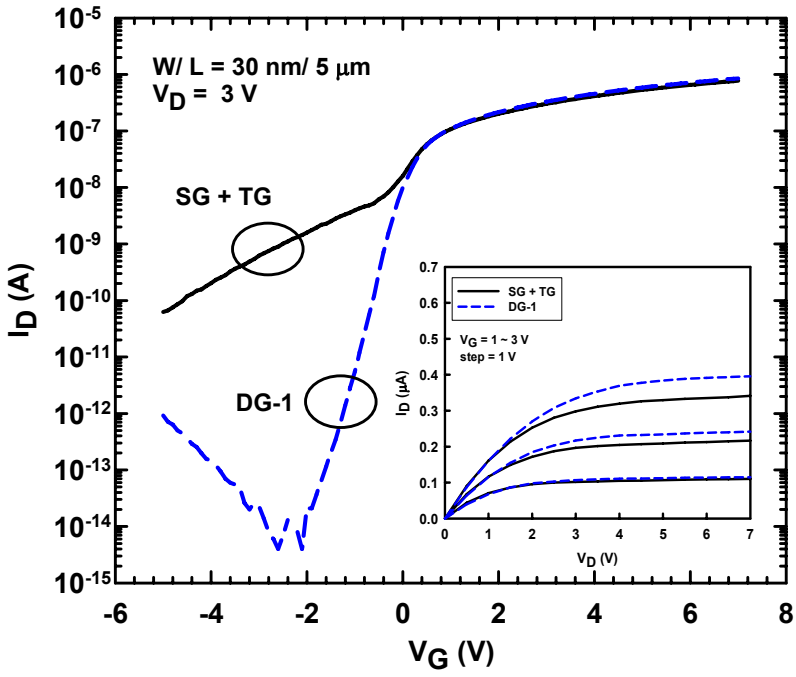


Fig. 4-9 Transfer and output (inset) characteristics for DG-1 operation as compared with the sum of the current of two individual single-gated operations.

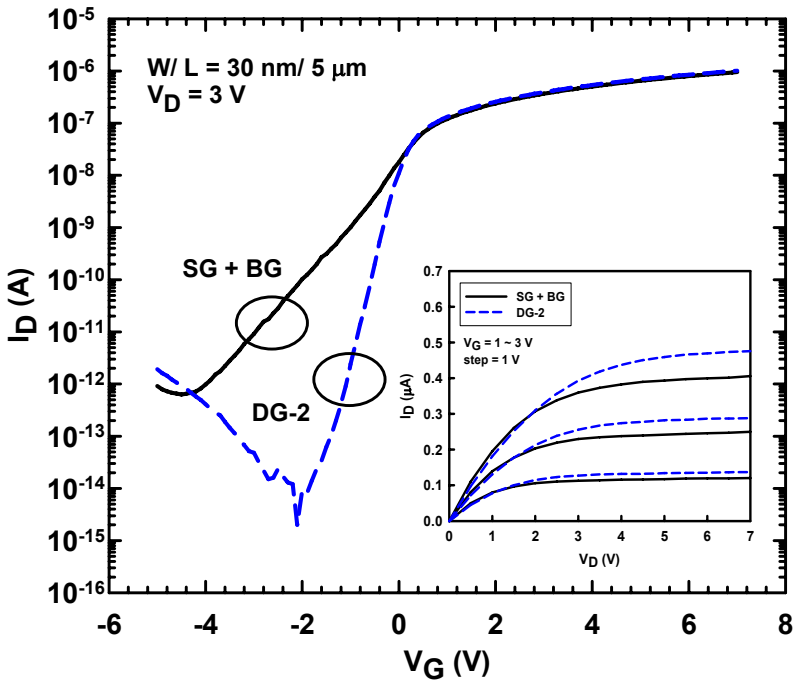


Fig. 4-10 Transfer and output (inset) characteristics for DG-2 operation as compared with the sum of the current of two individual single-gated operations.

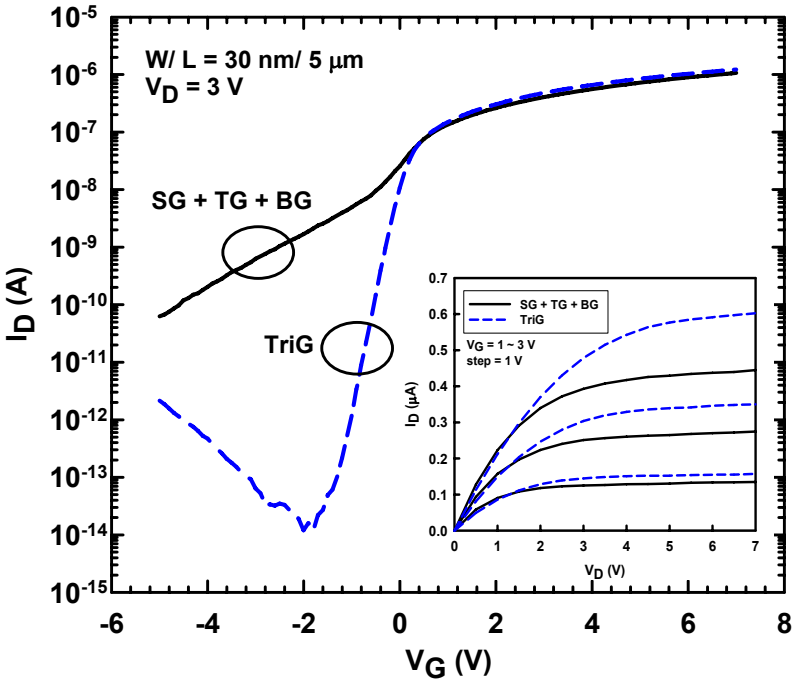


Fig. 4-11 Transfer and output (inset) characteristics for TriG operation as compared with the sum of the current of three individual single-gated operations.

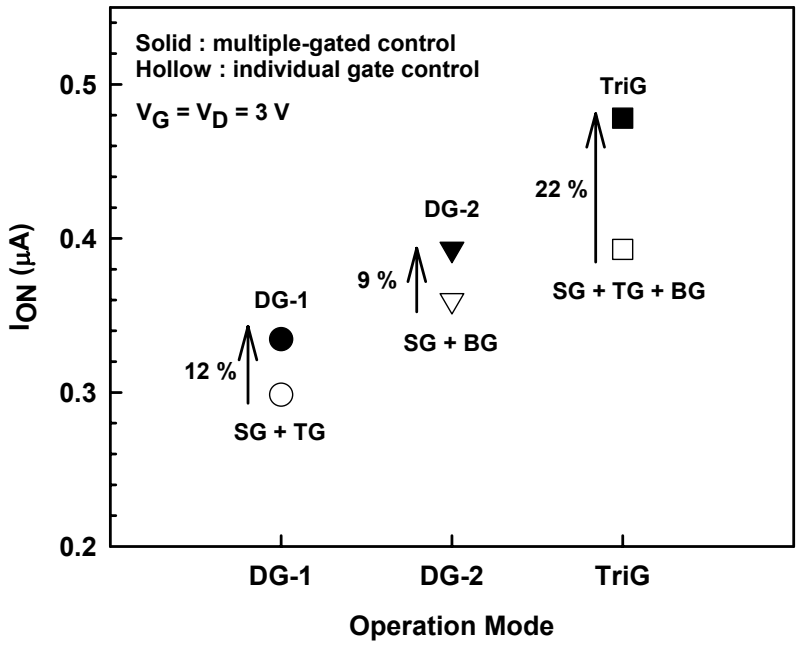


Fig. 4-12 I_{ON} enhancement under MG control for the data shown in Figs. 4-9~4-11. Solid symbols indicate I_{ON} of MG control, whereas hollow ones represent the sum of I_{ON} of individual gate control.

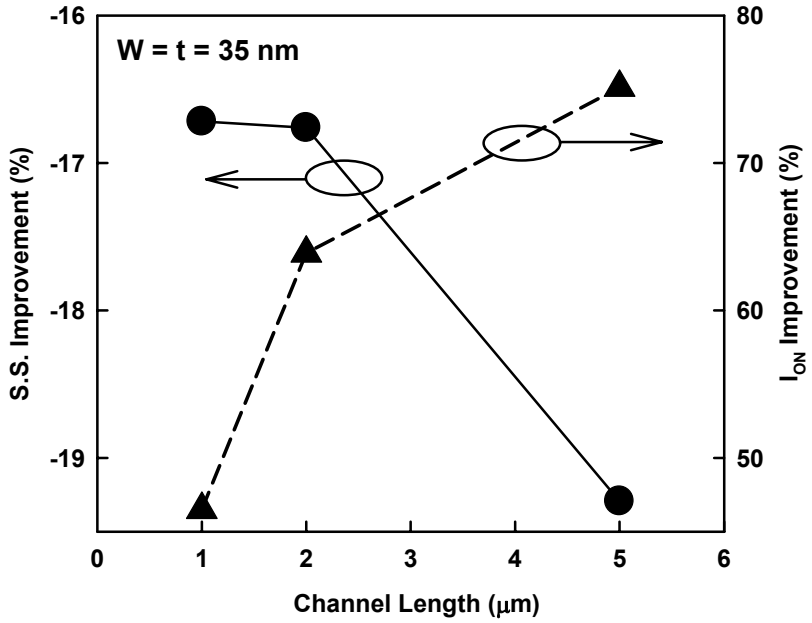


Fig. 4-13 S.S. and I_{ON} improvement versus poly-Si NW channel length under DG-1 control compared with SG mode.

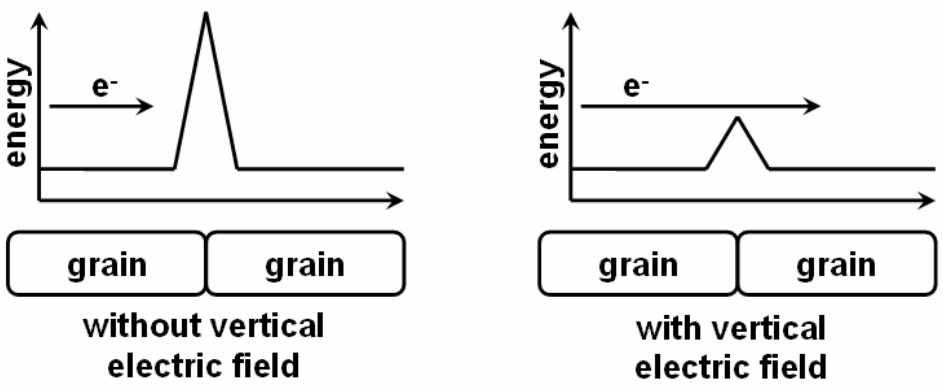


Fig. 4-14 Schematic carrier transport in polycrystalline structure without and with electric field.

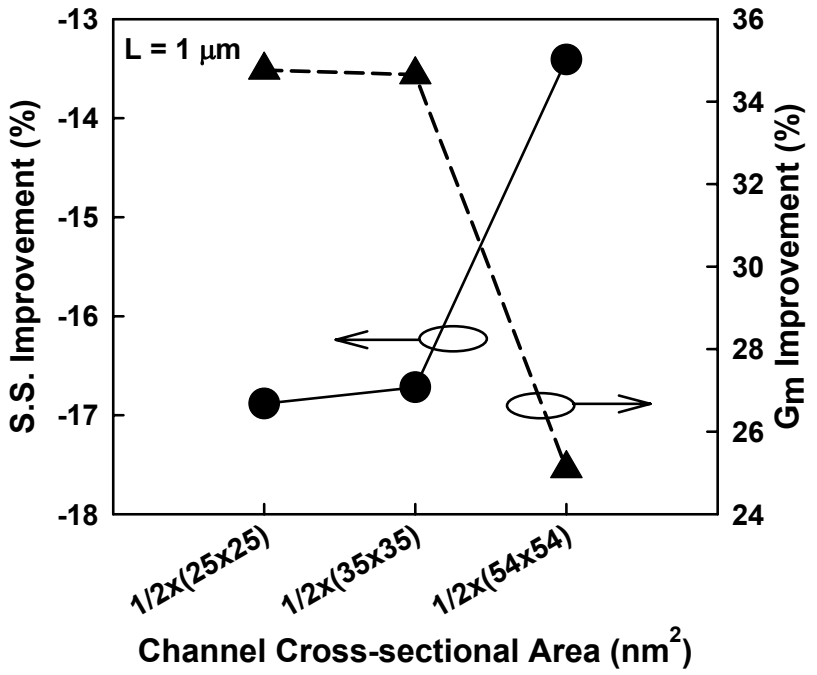


Fig. 4-15 S.S. and G_m improvement of poly-Si NW TFT with various channel volume under DG-1 operation with respect to SG mode.

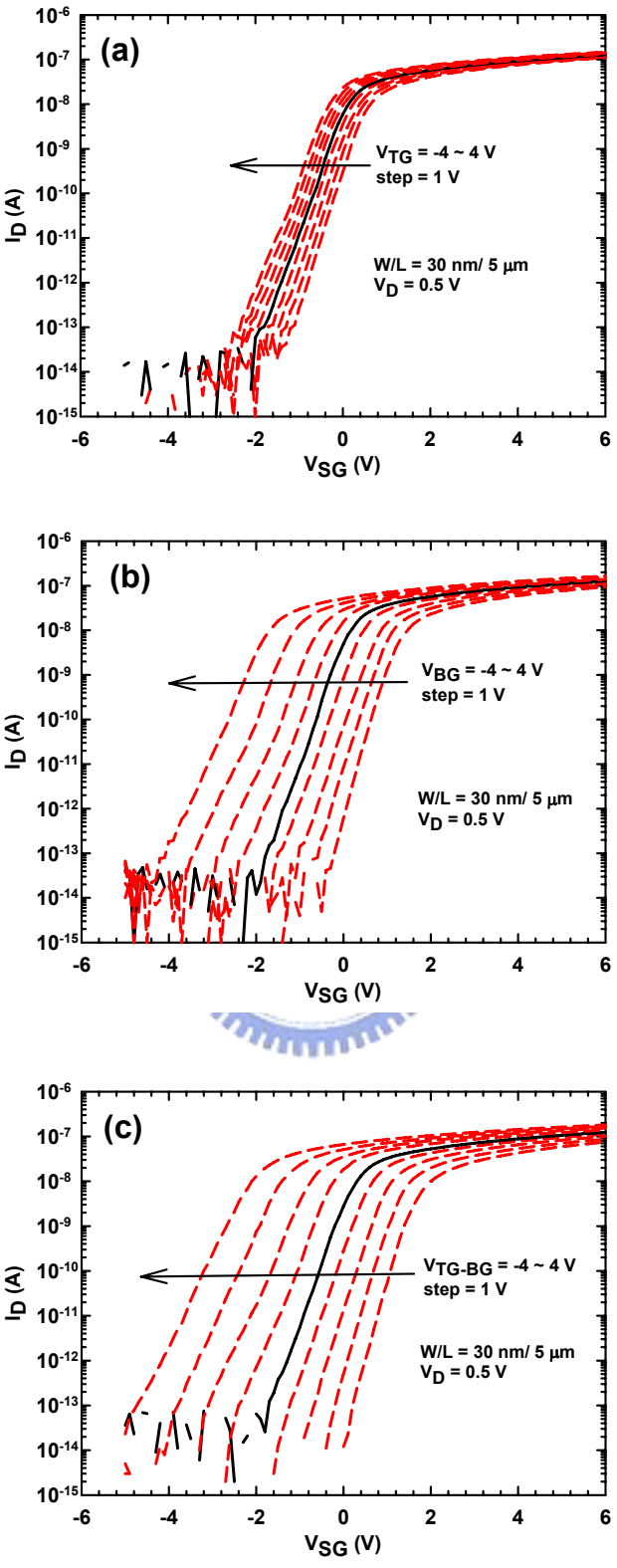


Fig. 4-16 I_D-V_{SG} characteristics of a side-gated transistor with V_{set} applied to (a) TG, (b) BG and (c) both TG and BG.

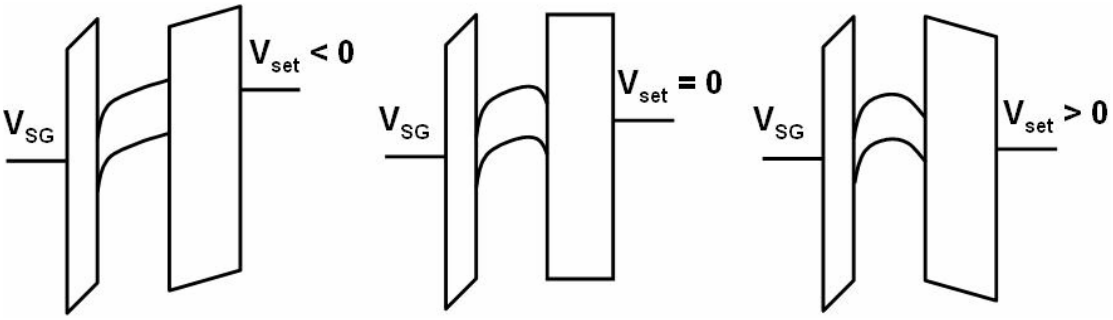


Fig. 4-17 Band diagrams of the NW channel with varying V_{TG} or V_{BG}.

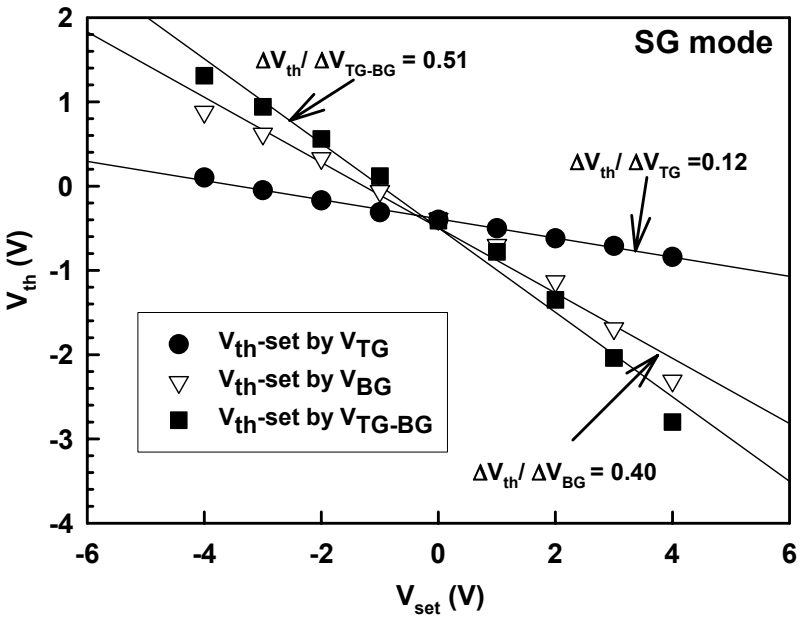


Fig. 4-18 Dependence of V_{th} as a function of V_{set} in SG operation mode.

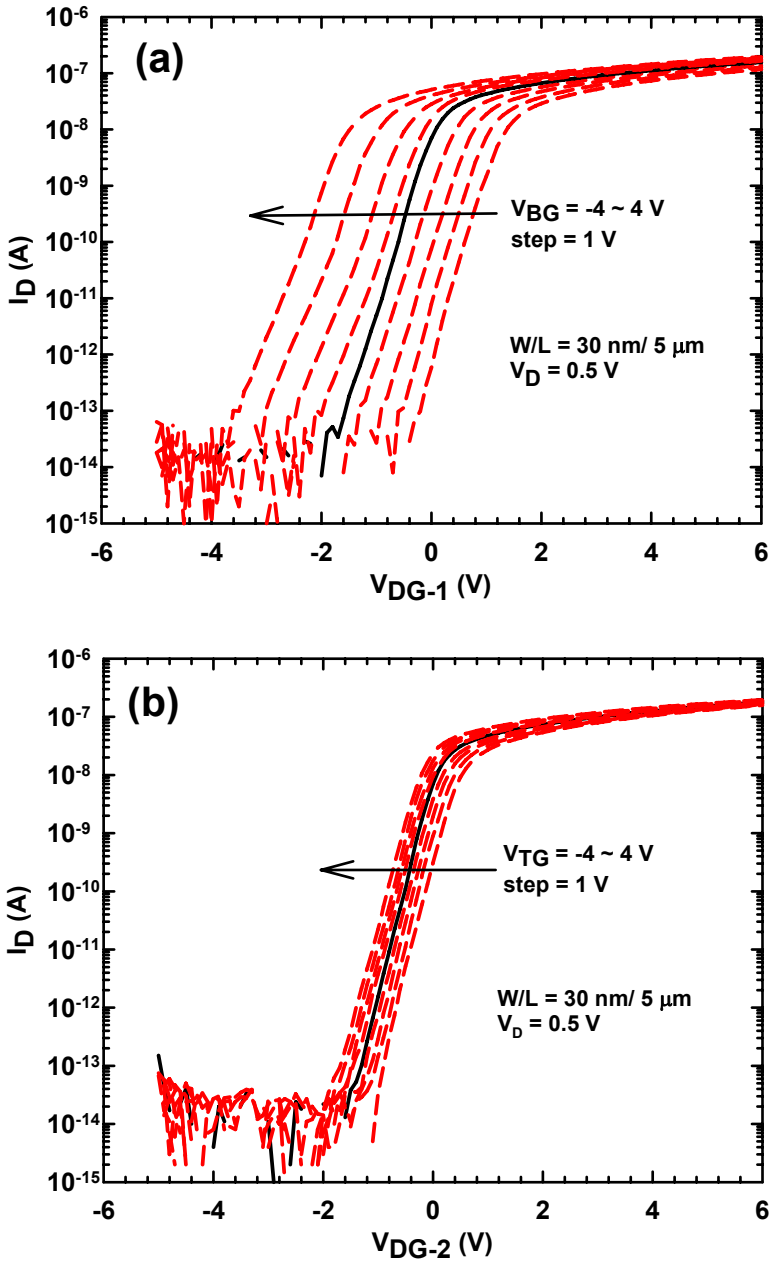


Fig. 4-19 Transfer behaviors of the double-gated transistor with various TG or BG biases: (a) DG-1 mode and (b) DG-2 mode.

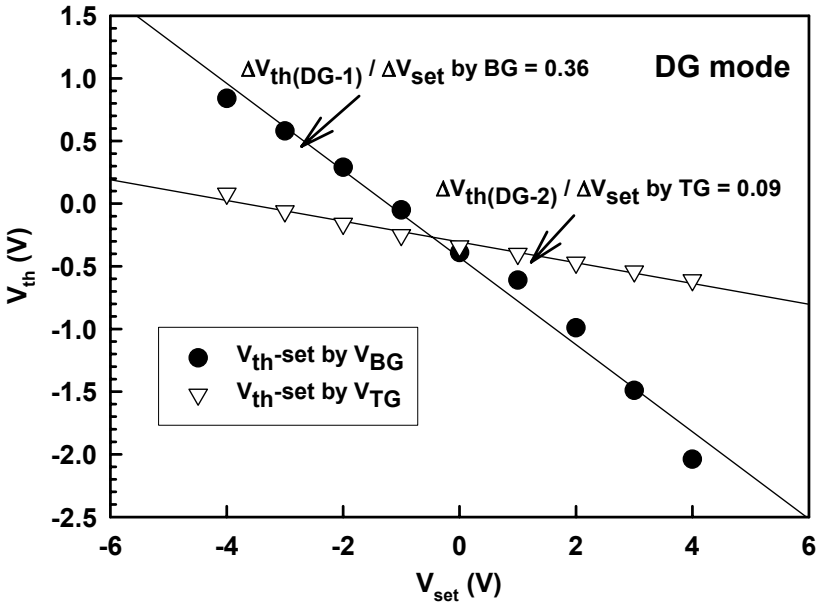


Fig. 4-20 Dependence of V_{th} as a function of V_{set} in DG operation modes.

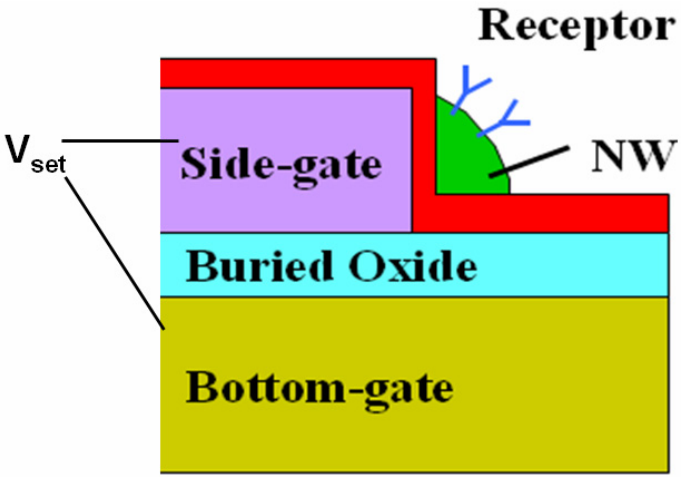


Fig. 4-21 For sensing applications, V_{set} generated from a control circuit (not shown) could be used to set the NW channel potential to a condition most sensitive to the surface charges of the exposing site.

Chapter 5
Sensing Devices Based on Poly-Si Nanowire Field-Effect Transistors

Nano-devices based on silicon nanowire (Si NW) structures have drawn much attention in the recent decade. Si NWs are particularly attractive as sensors because their critical dimension is comparable to the size of chemical and biological species. Due to its high surface-to-volume ratio, the NW's sensitivity is greatly enhanced when the signal is effectively transduced. In the preceding chapters, we have investigated and demonstrated the use of poly-Si NW field-effect-transistors (FETs). With its easy preparation, low-cost, and compatibility with various substrates, poly-Si NW devices are favorable for many applications. However, poly-Si suffers from inherent defects in inter/intra grains that impede carrier transport. This could potentially hinder poly-Si from sensor applications because of sensitivity degradation issue. In this work, we show that such concern is alleviated as long as the operation is carried out in an aqueous solution. Finally, the sensing capability of poly-Si NW devices for detection of pH-value and biomolecules is also presented.

5.1 Introduction

Field-effect transistors (FETs) have been proposed for chemical sensor applications since 1975 by Lundstrom *et al.,* who reported a hydrogen-sensitive FET with palladium as gate metal [5.1]. The fundamental concept is that FETs exhibit a conductivity change in response to variations in the electric field or potential at the surface since the electric field resulting from binding of charged species to the surface is analogous to applying a voltage using gate electrode. In addition to gas detection, FET can also be used to measure pH or ions in aqueous solutions [5.2]. In those early works, the test devices adopted a planar structure having a channel exposed to the environment. During the sensing operation, the channel conductance is modulated by the amount of charges bound to the channel surface. Such scheme is easy to fabricate. However, the sensitivity is seriously affected by the leakage current from source to drain through the bulk of the substrate. To address this issue, recently a new sensing structure utilizing Si NW as the channel was proposed [5.3]. Si NWs can overcome the limitations of planar FETs because the one-dimensional morphology and nano-scale cross-section of the NW lead to nearly depletion or accumulation of carriers in the channel of the device when a species is bound to the surface [5.3, 5.4]. Also owing to the high surface-to-volume ratio and tiny body, the bulk leakage could be effectively suppressed and thus the sensitivity is greatly improved. Such Si NW

sensors have demonstrated their function and sufficient sensitivity to detect protein [5.3], DNA [5.5], glucose [5.6] and virus [5.7].

The aforementioned works on biosensing applications employed monocrystalline Si NWs as the channel layer. Few defects are contained in such materials, enabling a high carrier mobility which is essential for good device performance. Recently we investigated the use of poly-Si NW channels for building novel electronic devices [5.8, 5.9]. The scheme we proposed could greatly simplify the fabrication process. However, defects contained in the grain boundaries of the poly-Si NW would impede carrier transport and thus degrade the mobility [5.10]. For biological sensors, the polycrystalline nature of NWs raises the concern of sensitivity degradation. In this work, we show that such concern could be lifted as long as the measurement is carried out in an aqueous solution. Possible mechanism for this phenomenon is also proposed.

5.2 Fabrications of Poly-Si NW Sensors

5.2.1 Fabrications of Poly-Si NW Sensing FETs

The fabrication of the poly-Si NW devices is briefly described as follows: a 90 nm-thick amorphous Si was first deposited on a Si substrate with 100 nm-thick SiO_2 by a low-pressure chemical vapor deposition (LPCVD) system. After doping of

source/drain (S/D) regions with phosphorus species, the film was annealed at 600 ^{o}C for 24 hours to fulfil dual purpose of Si re-crystallization and dopant activation. Formations of poly-Si NW channels and S/D regions were simultaneously accomplished by e-beam lithography and the following dry-etching step. Fig. 5-1(a) shows the scanning electron microscopic (SEM) picture of a device which contains six NW channels. Planar width of each NW is 70 nm. Afterwards, a passivation oxide deposited by LPCVD was capped on the wafer surface. The Si NW channels were then exposed by removing the covering oxide, and the entire device was then enclosed in a polydimethylsiloxane (PDMS) microfluidic structure with an aim of performing electrical measurements in an aqueous environment (Fig. 5-1(b)). During the measurements the Si substrate itself serves as the gate electrode upon which a bias is applied to modulate the drain current.

5.2.2 Preparations of Microfluidic Systems

To perform biosensing process, a robust microfluidic channel is required to flow the sample solutions in and out of the sensing site. The microchannels used in this study were fabricated with replica molding technique by employing PDMS as the material. PDMS possesses several advantages, such as good thermal stability,

biochemical compatibility and easy molding. The transparent nature of this material allows the sensing process to be monitored directly by human eyes. Fabrication process of the poly-Si NW sensing device with microfluidic structure is schematically shown in Fig. 5-2 and briefly described as follows:

(1) Using a glass substrate as the master mold and fashioning reverse microfluidic patterns on it.

(2) Mixing PDMS and curing agent with a ratio of 10 to 1, followed by using vacuum pump to degas air in PDMS.

(3) Pouring PDMS onto the master mold and curing it at 80 ^{o}C for 20 min.

(4) Carefully peeling off PDMS from the mold, and cleaning PDMS and the NW device with acetone.

(5) Performing O_2 plasma treatment on both PDMS and NW devices for 1 min.

(6) Bonding PDMS microfluidic structure to the NW device.

(7) Baking them at 90 ^{o}C for 30 min to remove surplus moisture.

Note that the purpose of O_2 plasma treatment in step (5) is to create –OH bonds on both PDMS and the NW device surfaces so that PDMS can covalently bond to the NW device. Next, baking the system to expel residual H_2O molecules and achieve

better bonding effects. This procedure is illustrated in Fig. 5-3.

5.2.3 Immobilization of Biomolecules on Poly-Si NWs

For the purpose of selectivity and specificity, the poly-Si NW's surface must be functionalized with a specific molecule to attach the target active compound. 3-aminopropyltriethoxysilane (APTES) has been widely used in affinity-based biosensors because the silane group can tightly bind to Si or glass substrates, while its amine group can form covalent bonds with carboxyl groups (functional groups that are commonly found in biomolecules) [5.11]. The structural formula is show in Fig. 5-4. In this study, the natively oxidized poly-Si NW's surface provides natural sites for the immobilization of APTES on it. The procedure is briefly described as follows:

(1) Using ethanol to wash the poly-Si NW device.

(2) Immersing the device in 2 % APTES ethanol solution for 30 min.

(3) Washing the device with pure ethanol.

(4) Heating the device at 120 °C for 10 min to remove excess ethanol.

To explore biomolecular sensors, the detection of the reaction between mouse-IgG and anti-mouse-IgG is inspected in this work. The immobilization of

mouse-IgG on the poly-Si NW FET is performed by the following steps:

(1) Immobilizing APTES on the poly-Si NW device as described above.

(2) Mixing the device with 2.5 % glutaraldehyde in phosphate buffered saline (PBS) buffer that contains 4 mM sodium cyanoborohydride for 1.5 hours.

(3) Washing the device with PBS buffer.

(4) Coupling mouse-IgG (50 μg/ml) in PBS buffer that contains 4 mM sodium cyanoborohydride to the surface of NW for 9 hours.

(5) Washing the device with PBS buffer.

(6) Blocking the un-reacted aldehyde groups with ethanolamine.

(7) Washing the device with PBS buffer.

To carry out the biosensing process, anti-mouse-IgG (6.9 μg/ml) and α-rabbit-IgG (9.3 μg/ml) were used for experimental and control groups, respectively. Also note that all the immobilization processes were done in the microfluidic system.

5.3 Experimental Setup

Basically, the sensing experiment is done with the general electrical

characterization setup as introduced in Chapter 2. First, the fabricated poly-Si NW device with PDMS microfluidic channel is connected with inlet and outlet pipes, as shown in Fig. 5-5(a). To continuously transport the test solutions in and out of the sensing device in a steady-state, a pneumatic micro-pump with an injector is used, as displayed in Fig. 5-5(b). Therefore, real-time measurement of the sensing process can be achieved. Note that the device substrate itself simply acts as the bottom gate during the measurement. In addition to sweeping the gate bias, the bottom gate could tune the V_{th} of the NW channel to a desired level to attain better sensitivity.

5.4 Analyses of Poly-Si NW Behaviors in De-ionized Water

5.4.1 Electrical Characteristics

Most chemical and biological sensing environments are in aqueous conditions. In this regard, the poly-Si NWs device is first tested in the deionized water (DIW) to examine the corresponding electrical behaviors.

Fig. 5-6 shows the typical subthreshold characteristics of the NW transistor operated in atmospheric (dry) and aqueous (wet) states at room temperature. First, the measurement was carried out in a dry ambient. Afterwards, DIW was infused continually and stably to flow through the micro-fluid cavity and immerse the NW

channels. Then, the same measurement procedures were repeated. Detailed performance parameters are summarized in Table 5-I. Specifically, the performance in terms of subthreshold swing (S.S.), carrier mobility and threshold voltage (V_{th}), is significantly enhanced when the device is operating in wet ambient. The S.S. dramatically reduces as the measurement environment becomes wet. Note that the very large S.S. value recorded in the dry ambient is consistent with the fact that the polycrystalline material used in this study contains a large amount of defects. These defects act as trapping centers for carriers [5.10] and tend to slow down the modulation of channel surface potential with increasing gate voltage. Dramatic reduction in S.S. of the device when operating in a wet environment implies that these trapping sites become ineffective. It is also worth noting that the S.S. is reduced to 0.2 V/dec in wet ambient (c.f., 0.9 V/dec in dry ambient), which is very comparable to that of monocrystalline Si NW (e.g., 0.174-0.649 V/dec) [5.12]. The other important finding is that the significant increase in mobility and the saturation drain current, when measured in a wet environment, indicates that the resistance of Si NW under on-state operation is dramatically reduced. This again evidences the decrease in the amount of active defects in the channels, which is further confirmed by extracting the trap density adopting the Levinson method [5.13]. The results are also depicted in Table 5-I. These differences originating from the different measurement environments

reveal that the ingredients contained in the water play an essential role in modifying the conduction behavior of carriers inside the NW. It is worth noting that when measured in a wet environment, the performance of poly-Si NW devices is almost on a par with that of monocrystalline Si NW devices [5.12]. This finding is very important because biologic and chemical sensing is usually performed in aqueous solutions. In this regard, the unique enhanced behaviors of poly-Si NW in aqueous ambient thus lend itself nicely to sensing applications.

5.4.2 Mechanisms of Water Passivation Effects

Passivations of defects in poly-Si by hydrogen-related species are well-known and have been utilized extensively for improving the device performance of poly-Si thin-film transistors (TFTs). Such treatment is typically done by exposing the devices to an H-containing plasma [5.14], or via a high-pressure water vapor annealing step [5.15, 5.16]. Since TFTs are normally capped with a dielectric (typically a silicon oxide layer), these process treatments are usually performed at an elevated temperature so that the hydrogen species can effectively diffuse through the dielectric and into the poly-Si channel to passivate the defects. Among the previously developed techniques, the process ambient of high-pressure vapor anneal contains same

ingredients as the wet environment investigated in this work. So we postulate that similar mechanisms may occur in our devices. The DIW is neutral with pH value of 7. This means that the concentration of H^+ (and OH^-) is 10^{-7} mole/L, or $6.02x10^{13}$ cm^{-3}. This value is actually much higher than the ion density in typical H-containing plasmas (~ 10^{10} cm^{-3}) [5.14]. The abundant H^+ and/or OH^- may diffuse into the grain boundaries and terminate on the dangling bonds there. As a consequence, the amount of electrically active defects is substantially reduced, resulting in a dramatic improvement of device performance.

In addition, another possible factor causing this improvement is the high relative dielectric permittivity of water, $\kappa \sim 80$, leading to a situation which is similar to that of gate-all-around operation. Therefore, the bottom-gate could exert stronger control over the channel, inducing more conduction pathways in the NWs.

5.4.3 Reproducibility of Water Passivation Effects

To test the reproducibility of the water passivation effect, measurements were repeatedly performed on a device which went through seven stages of exposure to alternate dry and wet environments. Within each stage the device was characterized several times to confirm the stability of device performance. The representative I-V

curves for all stages are shown in Fig. 5-7. Clearly, the device characteristics recover when the device was switched from wet to dry environment and vice versa. Fig. 5-8 shows the plot of S.S. and V_{th} extracted from the seven stages in Fig. 5-7. Much smaller variation and better stability of electrical characteristics in wet ambient can be observed in addition to the lower S.S. and V_{th}. These electrical parameters are closely related to the reproducibility, conductivity and sensitivity of a device required for sensing applications. Also worth noting in this figure is that the passivation effect occurs only in water, indicating that the passivation bonds are metastable and could easily be desorbed from the poly-Si NWs when the water is pumped away from the microfluid cavity.

5.5 Poly-Si NW Sensing Devices

5.5.1 pH Sensing

In this work, the phosphate buffered saline (abbreviated PBS), comprising of 10 mM sodium phosphate and 100 mM sodium chloride, was used for the pH value measurement and maintaining a constant pH. In order to achieve different pH values, the buffer solutions were mixed with a solution of NaOH and HCl. A commercial pH meter was used to determine the pH level of the PBS, and pH indicators were

prepared from pH 4 to pH 10.

To study electrical response to pH, surfaces of poly-Si NWs were functionalized with APTES to produce amino groups ($–NH_2$) as well as silanol (–SiOH) on the NW surface which act as receptors of hydrogen ions (H^+). The underlying concept is that the covalent links of APTES to poly-Si NW oxide surface results in a surface terminating in both $–NH_2$ and –SiOH groups, which have various dissociation constants, pKa [5.17]. At high pH range, –SiOH is deprotonated to $–SiO^–$, serving as a negatively charged gate. While at low pH, $–NH_2$ is protonated to $–NH_3^+$, correspondingly acting as a positive gate. This mechanism is schematically depicted in Fig. 5-9(a). Therefore, the change of surface charge state on the Si NWs will in turn modulate the NW conductance. Since our NW device is operating as n-type FET, more positive charges on NW surface will induce more carriers for transport, and therefore higher conductance with lower pH value. As shown in Fig. 5-9(b), the poly-Si NW device indeed shows strong dependence of conductance on pH value.

5.5.2 Biomolecule Detection

For the purpose of biological detection, the poly-Si NW's surface is modified in sequence with APTES and goat mouse-IgG biomolecules, as illustrated in Fig. 5-10(a).

The detailed procedure is described in Section 5.2.3. When the NWs are immersed in goat α-rabbit-IgG solution (9.3 μg/ml), the conductance is slightly higher than that in the buffer, as shown in Fig. 5-10(b). This is ascribed to some ionic effect as α-rabbit-IgG is not supposed to react with mouse-IgG. However, huge drop in conductance is observed when anti-mouse-IgG (6.9 μg/ml) is injected into the microfluidic chamber. This indicates that the charge state over the NW surface has changed, as a result of the bonding of anti-mouse-IgG to the modified NW surface (Fig. 5-10(a)). Such result also implies the resultant bonding induces negatively charged macromolecules.

5.6 Summary

In this chapter, the feasibility of poly-Si NWs for sensing applications is demonstrated. We found that the performance of poly-Si NWs is significantly boosted by water passivation effect. Furthermore, such effect is testified with high reproducibility and stability. This finding is important as it suggests that poly-Si NWs can be cleverly operated in aqueous solutions to take advantage of the performance improvement. By functionalizing specified receptor on its surface, poly-Si NW exhibits good sensibility and selectivity for ionic and biologic detection. Our finding,

coupled with simple preparation method, makes poly-Si NWs very promising for future sensor device fabrication in terms of good integrity and reduced cost.

References

[5.1] I. Lundstrom, M. S. Shivaraman and C. M. Svensson, "A hydrogen-sensitive Pd-gate MOS transistor," *J. Appl. Phys*., **46**, 3876 (1975).

[5.2] P. Bergveld, "Development of an ion-sensitive solid-state device for neurophysiological measurements," *IEEE Trans. Biomed. Eng*., **BME-17**, 70 (1970).

[5.3] Y. Cui, Q. Wei, H. Park and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, **293**, 1289 (2001).

[5.4] J. I. Hanm and C. M. Lieber, "Direct ultrasensitive electrical detection of DNA and DNA sequence variations using nanowire sensors," *Nano Lett*., **4**, 51 (2004).

[5.5] Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka and R.S. Williams, "Sequence-specific label-free DNA sensors based on silicon nanowires," *Nano Lett.*, **4**, 245 (2004).

[5.6] W. Chen, H. Yao, C. H. Tzang, J. Zhu, M. Yang and S.T. Lee, "Silicon nanowires for high-sensitivity glucose detection," *Appl. Phys. Lett.*, **88**, 213104 (2006).

[5.7] F. Patolsky and C. M. Lieber, “Nanowire nanosensors,” *Material Today*, **8**, 20 (2005).

[5.8] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee and Y. S. Yang, “A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel,” *IEEE Electron Device Lett.*, **26**, 643 (2005).

[5.9] H. C. Lin, M. H. Lee, C. J. Su and S. W. Shen, “Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels,” *IEEE Trans. Electron Devices*, **53**, 2471 (2006).

[5.10] J. Y. W. Seto, “The electrical properties of polycrystalline silicon films,” *J. Appl. Phys*., **46**, 5247 (1975).

[5.11] T. Cass and F. S. Ligler, “Immobilized biomolecules in analysis: A practical approach,” Oxford University Press, New York (1998).

[5.12] Y. Cui, Z. Zhong, D. Wang, W. U. Wang and C. M. Lieber “High performance silicon nanowire field effect transistors,” *Nano Lett.*, **3**, 149 (2003)

[5.13] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westood, G. Este and M. Rider, “Conductivity behavior in polycrystalline semiconductor thin film transistors,” *J. Appl. Phys*., **53**, 1193 (1982).

[5.14] M. Yu, H. C. Lin, K. L. Yeh, T. Y. Huang and T. F. Lei, "H_2 and NH_3 plasma Passivation on poly-Si TFTs with bottom-sub-gate induced electrical junctions," *J. Electrochemical Soc*., **150**, G843 (2003).

[5.15] U. Mira, J. Chen, B. Khan and E. Stupp, "Low-temperature polysilicon TFT with gate oxide grown by high-pressure oxidation," *IEEE Electron Device Lett.*, **12**, 390 (1991).

[5.16] M. Kunii, "Evaluation of electrical characteristics and trap-state density in bottom-gate polycrystalline thin film transistors processed with high-pressure water vapor annealing," *Jpn. J. Appl. Phys*., **45**, 660 (2006).

[5.17] A. Noy, D. V. Vezenov, L. F. Rozsnyai and C. M. Lieber, "Force titrations and ionization state sensitive imaging of functional groups in aqueous solutions by chemical force microscopy," *J. Am. Chem. Soc.*, **119**, 2006 (1997).

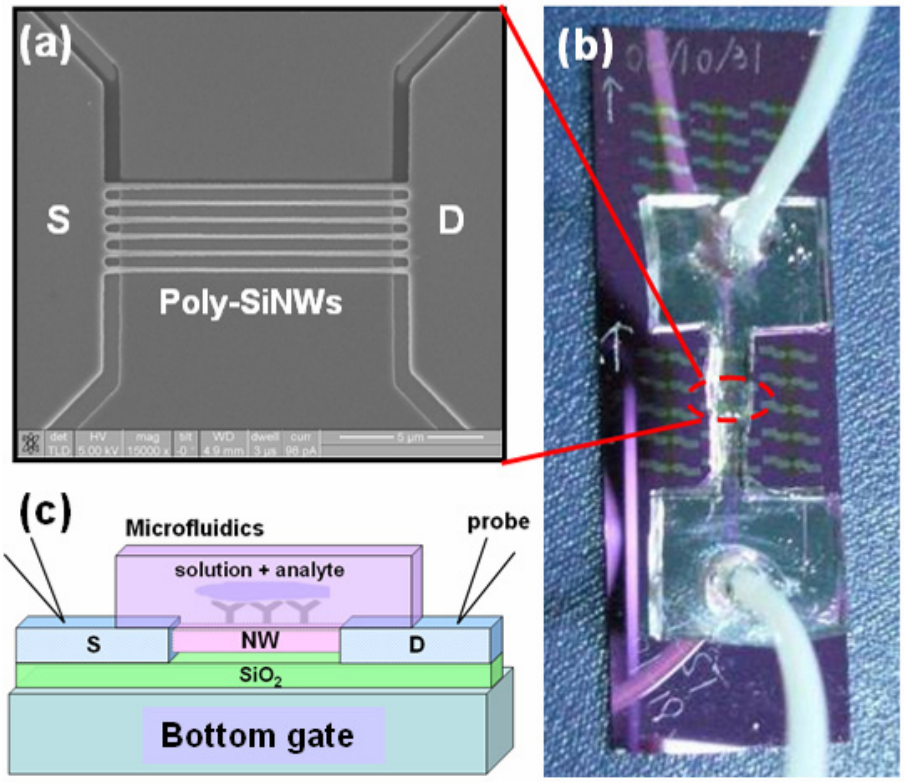


Fig. 5-1 (a) Top-view scanning electron micrograph (SEM) of the poly-Si NW device. The NW channels discussed here are with 10 μm in length, 70 nm in width and 90 nm in thickness. (b) Photo of the device enclosed with PDMS flow chamber. (c) Schematic diagram of poly-Si NW sensing device with bottom-gate and microfluidic system.

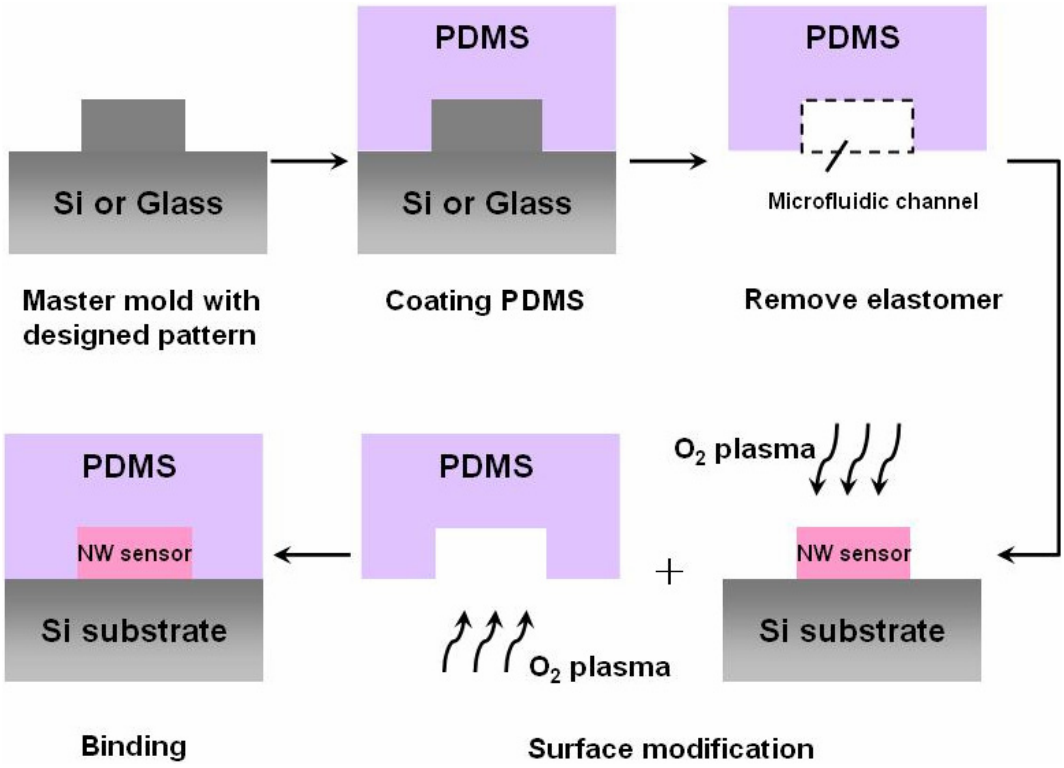


Fig. 5-2 Fabrication process of a NW sensing device with PDMS microfluidic channel.

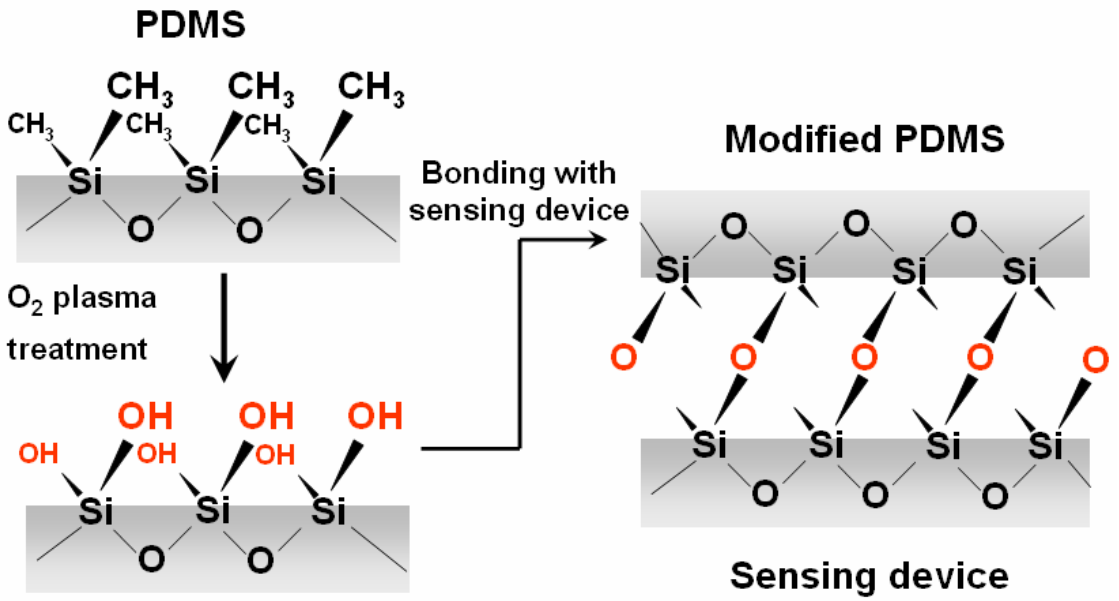


Fig. 5-3 Detailed bonding process of PDMS to the sensing device.

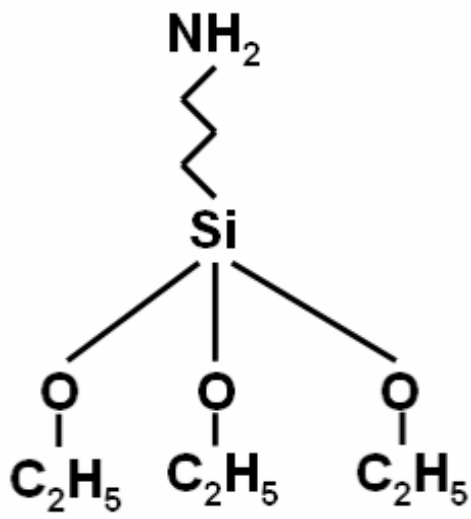


Fig. 5-4 Structural formula of APTES.

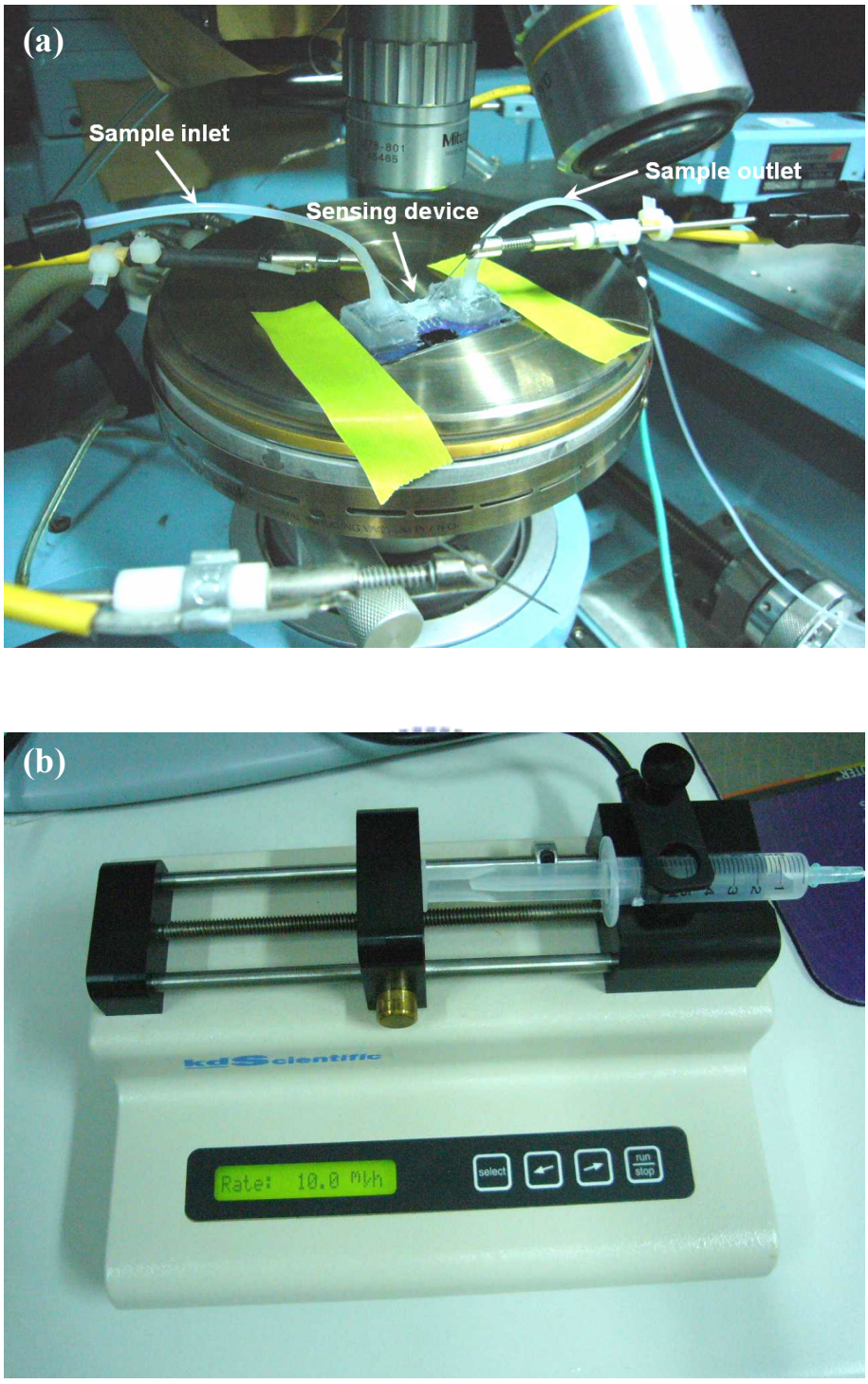


Fig. 5-5 (a) Experimental setup of the sensing measurement. (b) The micro-pump is used to inject the sample into the sensing site.

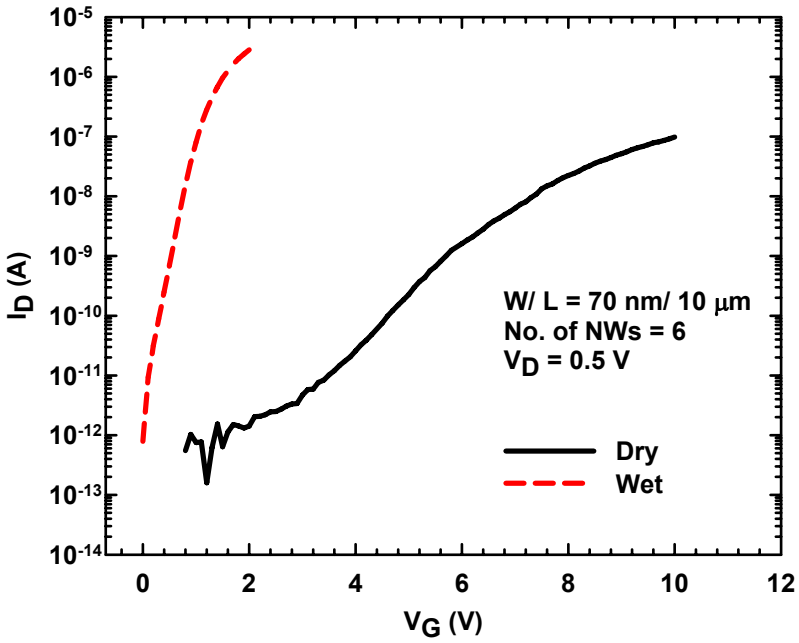


Fig. 5-6 Transfer characteristics of a poly-Si NW device operating in atmospheric (dry) and de-ionized water (wet) environments.

Table 5-I Comparisons of device performance parameters measured in dry and wet (DI water) ambients.

Ambient	Dry	Wet
Threshold Voltage, V_{th} (V)	6.8	0.7
Mobility, μ (cm^2/V-sec)*	75	126
Subthreshold Swing, S.S. (V/dec.)	1.1	0.2
Trap Density, N_t (10^{12} cm^{-2})#	1.2	0.41

* The channel width used in mobility extraction procedure is 70 nm (the planar width of the Si NW) for the case of dry ambient. However, owing to the high dielectric constant of water (~80), a gate-all-around operation scheme is assumed for the case of wet ambient. In other words, the effective width is assumed to be 320 nm (the total edge length of the NW's cross-section) for the case of wet ambient.

\# Trap density was extracted using Levinson's method [5.13].

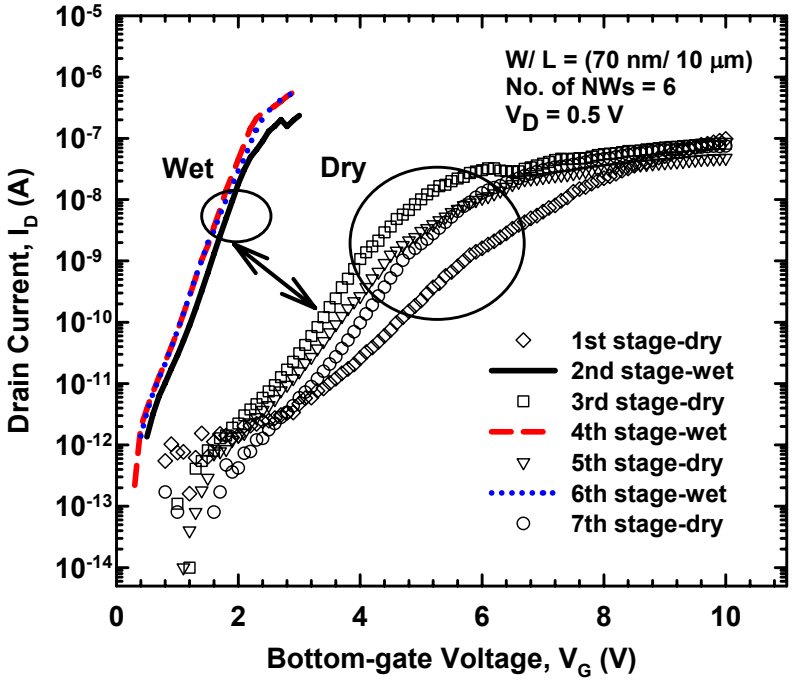


Fig. 5-7 Current-voltage characteristics of poly-Si NW device in several stages of exposure to alternate dry and wet ambients, also showing the reproducibility of water passivation effects.

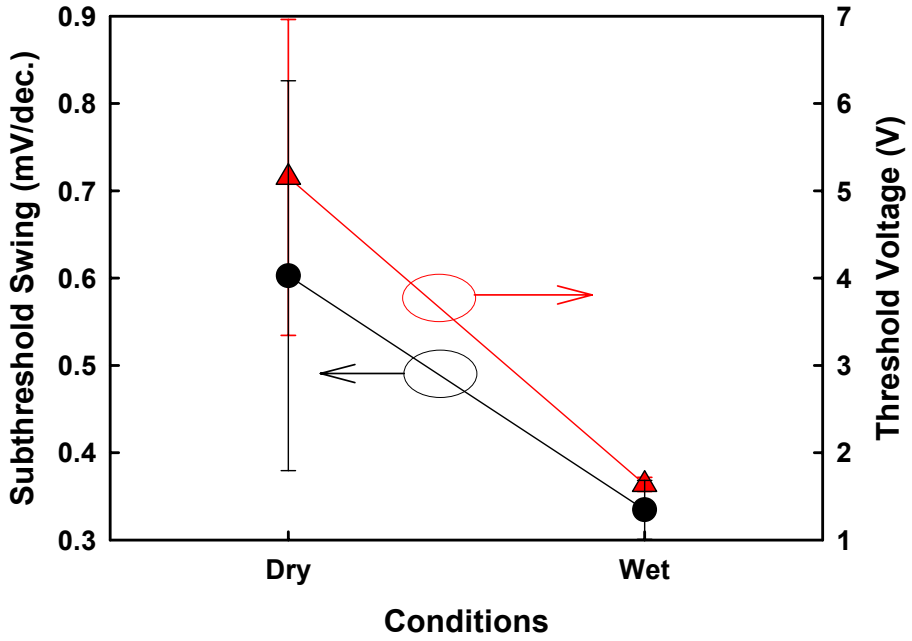
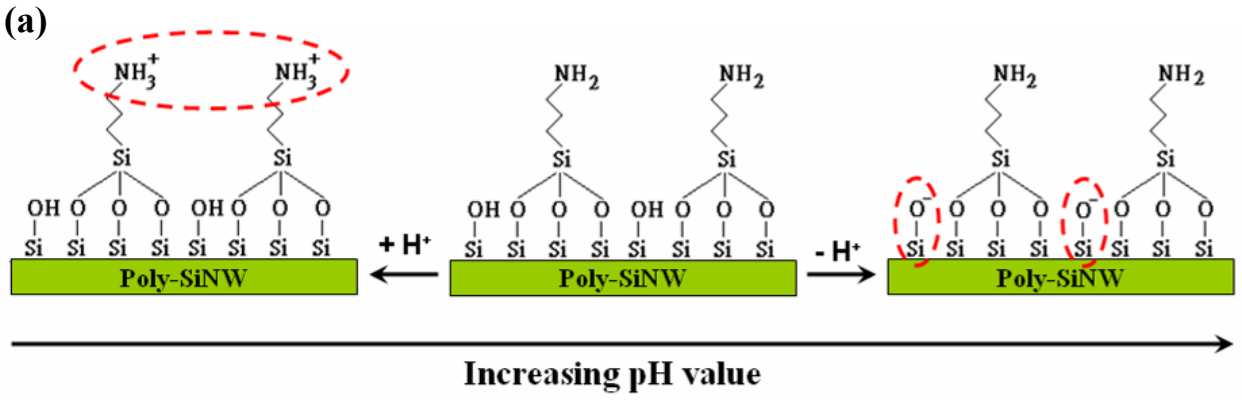


Fig. 5-8 Plot of subthreshold swing (S.S.) and threshold voltage (V_{th}) extracted from the seven stages in Fig. 5-7. Much smaller variation and better stability of electrical characteristics in wet ambient can be observed besides lower S.S. and V_{th}.



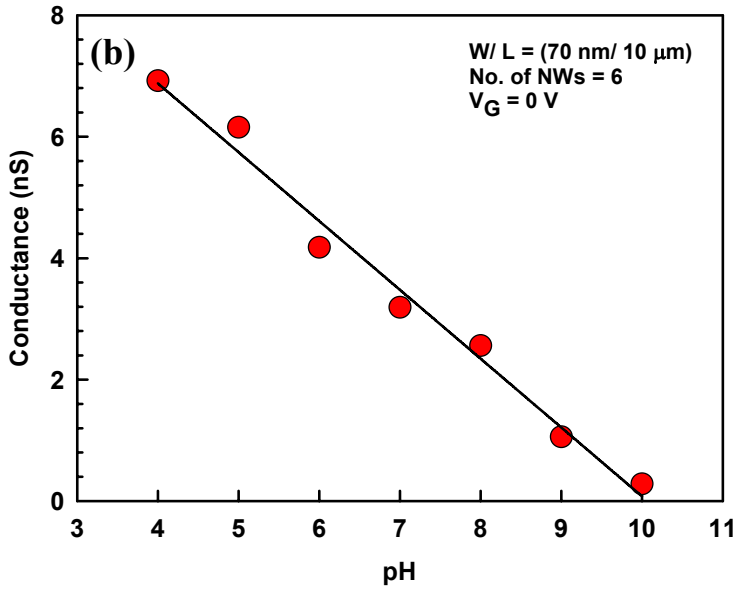


Fig. 5-9 (a) APTES-modified Si NW surface illustrating changes in the surface charge state with pH values, (b) conductance response as a function of pH value.

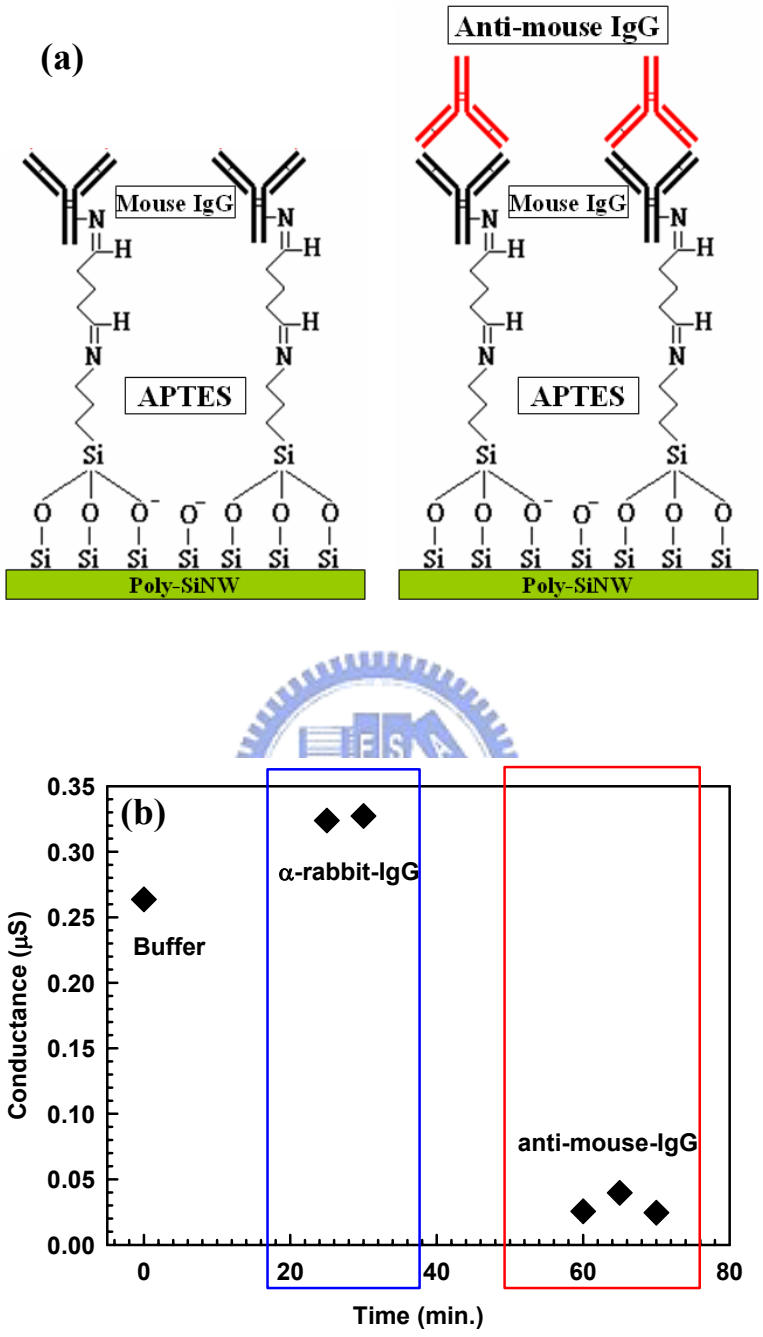


Fig. 5-10 (a) Schematic diagram illustrating a mouse-IgG modified Si NW (left) and subsequent binding of anti-mouse-IgG to the Si NW surface (right), (b) electrical responses of the modified poly-Si NWs to buffer, α-rabbit-IgG, and anti-mouse-IgG, respectively.

Chapter 6
Conclusions and Future Works

6.1 Conclusions

Overall, a unique technique for the fabrication of Si NWs and FETs superior to conventional "top-down" and "bottom-up" methods is proposed and demonstrated. Table 6-I highlights major advantages of the proposed scheme. This technique is manufacturable and economic, and is capable of providing a reliable high-performance poly-Si NW FET not only for investigating nano-scale semiconductor behaviors and physics but also for biosensors. It is also compatible with the low-temperature poly-Si (LTPS) technologies, and could be integrated on low-cost and flexible substrates (such as glass or plastic), making the fabrication of system-on-panel (SOP) for biologic sensing purpose possible.

To meet the requirement of high device performance for future applications, several feasible techniques and modification methods were implemented and studied on the proposed poly-Si NW FET. To address the anomalous off-state leakage current, alterations from structural and process aspects were exploited. By inserting a thicker hardmask between the gate and the drain and/or by increasing the drain dopant concentration toward the gate, severe leakage behavior was greatly alleviated.

In order to improve the poor crystalline properties of poly-Si films, plasma hydrogenation treatment and metal-induced lateral crystallization (MILC) technique were employed to passivate the defects and promote NWs' crystallinity, respectively. Significant boost in the device performance was obtained especially for MILC Si NW devices. By taking advantage of large MILC grain combined with appropriate NW channel dimension, Si NW crystallinity was thus greatly enhanced. In addition, the MILC NW devices with subsequent RTA treatment further exhibit dramatically high performance. TEM analyses reveal that single-crystal Si NW channel was acquired. The high electron mobility (550 cm^2/V-s) and hole mobility (230 cm^2/V-s) achieved in this work are actually among the best reported results for NW and poly-Si devices in the literature. Moreover, by reducing recrystallization temperature to suppress SPC mechanism, MILC grain length can be extended, thus promoting the on-current.

Based on the developed poly-Si NW structure, multiple-gated (MG) architecture could be easily achieved by a slight modification in device manufacture. The NW channels are precisely surrounded by three gates, i.e., top-, side- and bottom-gates. With MG operations, excellent electrical characteristics, such as high on/off current ratio of 10^7, were obtained. The strong gate coupling effect of the MG operation, which is ascribed to the tiny body of NW channels, accounts for the observed improvement. It is also found that the benefit of MG control diminishes as the

diameter of NW is larger than 35 nm. Moreover, the independently applied MG biases can be employed to regularly adjust the V_{th} of NW channels in a reliable manner, making it suitable for practical applications.

Finally, the feasibility of poly-Si NWs for sensing applications is demonstrated. The performance of poly-Si NWs can be significantly enhanced to a level comparable to the monocrystalline counterparts by water passivation effect. This finding is important as it suggests that poly-Si NWs can be cleverly operated in aqueous solutions to take advantage of the performance improvement. By functionalizing specified receptor on its surface, poly-Si NW exhibits good sensibility and selectivity for ionic and biologic detection. Our finding, coupled with simple preparation method, makes poly-Si NWs very promising for future sensor device fabrication in terms of good integrity and reduced cost.

6.2 Future Works

Although many topics and aspects of the proposed NW scheme have been discussed in this study, there are still interesting prospects worthy of further investigation, including improvement in device performance and promising applications.

6.2.1 Morphology of the Poly-Si NWs

Fig. 6-1 is a TEM image showing the microscopic morphology of the NW, where variation in NW dimensions is found. Such fact is mainly owing to the rough surface morphology of poly-Si side-gate as observed in the picture. This effect should be addressed since in the nano-scale regime, electrical behaviors, such as S.S. and V_{th}, are very sensitive to channel film thickness and width [6.8]. To this point, with the modification of etching process parameter, this issue is supposed to be alleviated.

6.2.2 Smart Microfluidic System

Recently, a new microfluidic system has been developed by our collaborative group (Laboratory of Enzyme & Protein Engineering, NCTU). Fig. 6-2 shows this system, which employs removable metal holders to fasten the PDMS and the NW device together seamlessly. In this regard, the O_2 plasma treatment as described in Section 5.2.2 is thus skipped. Note that this system also features easy alignment, easy observation and reusability. Furthermore, the gate voltage can be directly applied to the NW device through the metal holder, which facilitates the measurement process. Therefore, this system is particularly favorable for research purpose.

6.2.3 Nano-electro-mechanical System

Mechanical devices constructed on NWs with nano-scale thickness and width could reduce mass and lower force constants, and thus increase resonant frequency. Nano-electro-mechanical systems have hence become attractive alternatives for a number of applications such as switches [6.9] and memory devices [6.10]. The NWs in our scheme can be deliberately made freestanding with respect to the gate, while connecting directly to S/D regions (Fig. 6-3). During operation, the suspending NW channels may touch (i.e., pull-in) or keep a distance away from the side-gate (i.e., pull-out) due to the attractive electrostatic force exerted by the gate. Thus, a non-volatile memory device could be envisaged based on this scheme due to their electronic bistability, i.e., states of "0" and "1" (Fig. 6-4). Therefore, the investigation of nano-switch devices is one of the subjects worthy of undertaking in the future.

References

[6.1] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu and C. C. Huang *et al*, "5 nm-gate nanowire FinFET," *Symp. VLSI Tech. Dig.*, 196, June 15-17 (2004).

[6.2] H. C. Lin, M. F. Wang, F. J. Hou, H. N. Lin, C. Y. Lu, J. T. Liu and T. Y. Huang, "High-performance p-channel schottky-barrier SOI FinFET featuring self-aligned PtSi source/drain and electrical junctions," *IEEE Electron Device Lett.*, **24**, 102 (2003).

[6.3] Y. K. Choi, Ji. Zhu, J. Grunes, J. Bokor and G. A. Somorjai, "Fabrication of sub-10-nm silicon nanowire arrays by size reduction lithography," *J. Phys. Chem. B*, **107**, 3340 (2003).

[6.4] A. M. Morales and C. M. Lieber, "A laser ablation method for the synthesis of crystalline semiconductor nanowires," *Science*, **279**, 208 (1998).

[6.5] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan and K. C. Saraswat, "Germanium nanowire field-effect transistors with SiO_2 and high-κ HfO_2 gate dielectrics," *Appl. Phys. Lett.*, **83**, 2432 (2003).

[6.6] X. Duan, Y. Huang, Y. Cui, J. Wang and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, **409**, 66 (2001).

[6.7] Y. Huang, X. Duan, Q. Wei and C. M. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," *Science*, **291**, 630 (2001).

[6.8] A. Vandooren, D. Jovanovic, S. Egley, M. Sadd, B. Y. Nguyen, B. White, M. Orlowski and J. Mogab, "Scaling assessment of fully-depleted SOI technology at the 30 nm gate length generation," *IEEE Int'l SOI Conf.*, 25, October 7-10 (2002)

[6.9] B. A. Cruden and A. M. Cassell, "Vertically oriented carbon nanofiber based nanoelectromechanical switch," *IEEE Trans. Nanotechnology*, **5**, 350 (2006).

[6.10] A. Varfolomeev, V. Pokalyakin, S. Tereshin, D. Zaretsky and S. Bandyopadhyay, "Switching time of nanowire memory," *J. Nanosci. Nanotechnol.*, **5**, 753 (2005).

Table 6-I Comparisons of Si NW formation between top-down, bottom-up and our approach.

Characteristics / Process & Scheme	Size of NWs	Alignment of NWs	Performance	Cost & Process
Top-down [6.1-6.3]	Good control	Good control	Can be high	Expensive, high techniques and complicated
Bottom-up [6.4-6.7]	Relying on nanocluster and growth time	Not easy to control	Can be high	Medium, but complex integration
Our Approach	*Good control*	*Good control*	*Can be greatly improved by recrystallization*	*Cheap and simple, reliable and reproducible*

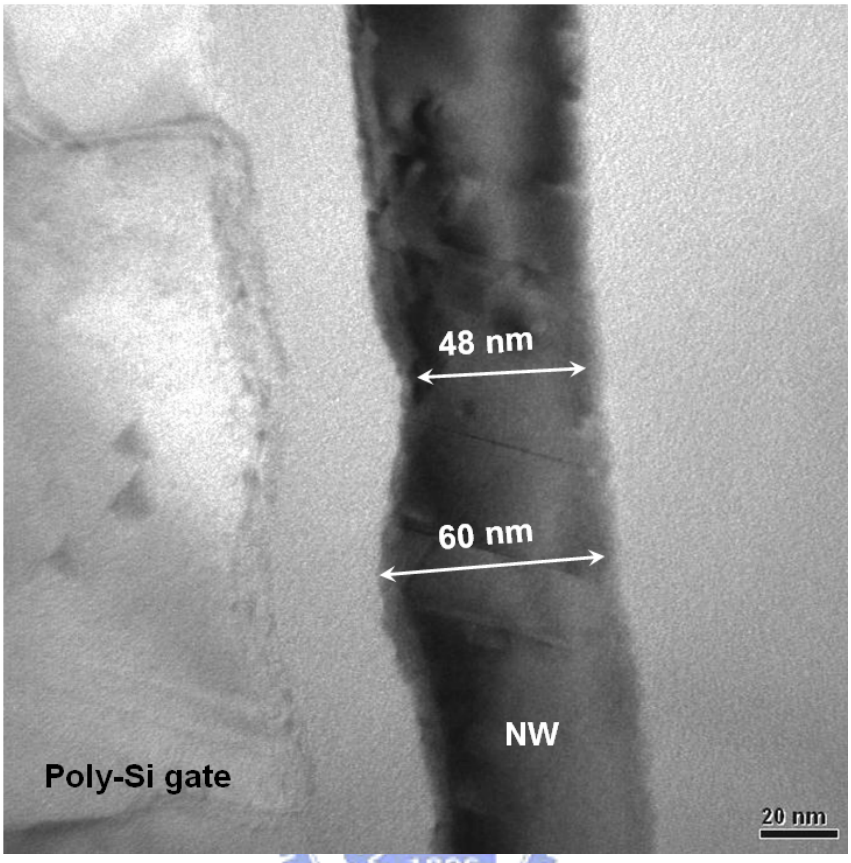


Fig. 6- 1 TEM image showing variation in NW dimension due to the morphology of the poly-Si gate.

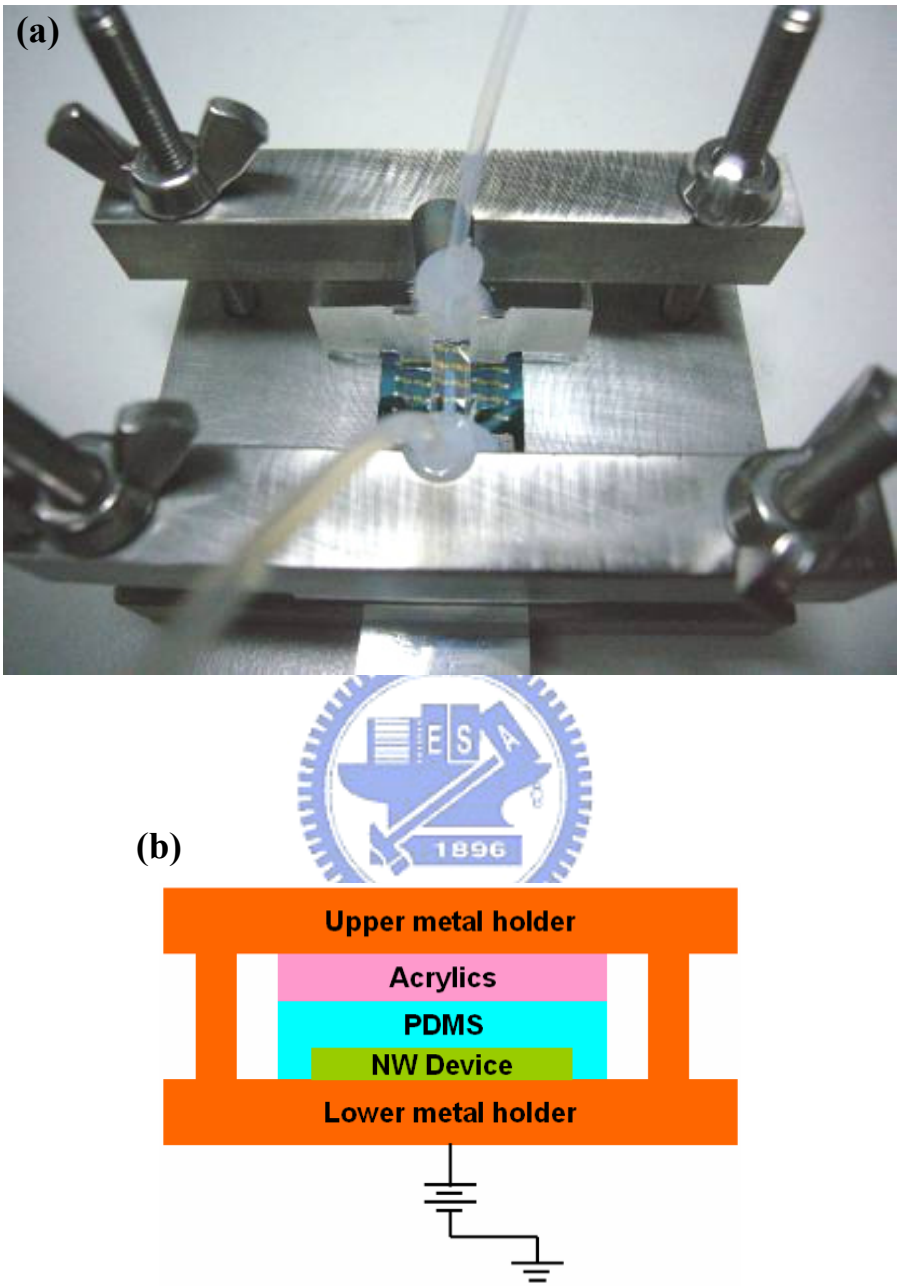


Fig. 6-2 (a) Photo of the NW sensing device equipped with the new microfluidic system.

(b) Schematic cross-sectional view of the system.

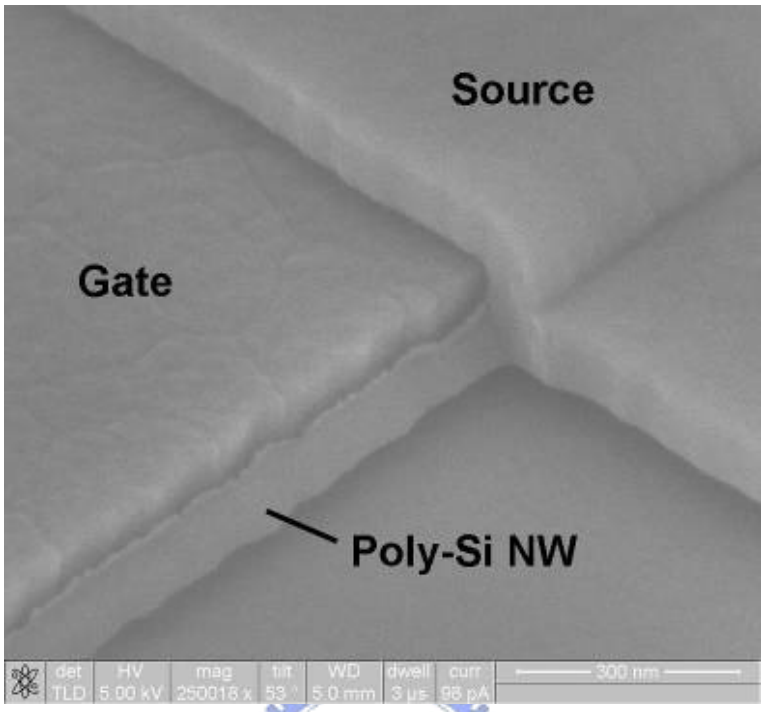


Fig. 6-3 SEM image of our poly-Si NW device showing NW connecting directly to source while freestanding with respect to the gate.

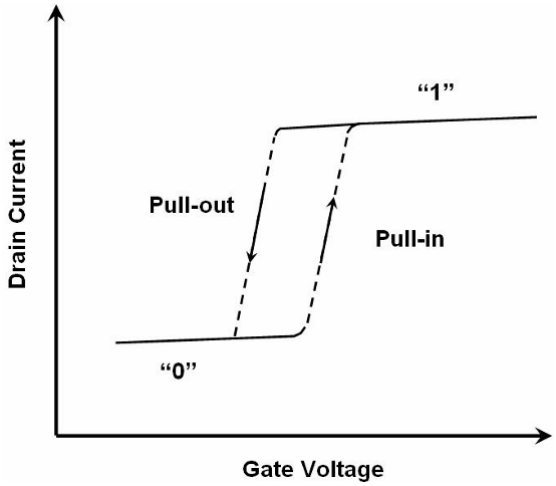


Fig. 6-4 Schematic plot of current behavior for the NW switching device.

Appendix
Capacitance-Voltage Characterizations of Silicon Nanodots Embedded in SiO_2 Double-Barrier Structure

A.1 Introduction

In recent years, three-dimensionally confined silicon nanodot (Si ND) embedded in dielectric metrics [A.1, A.2] is one of the attractive research fields in nanoelectronics area. This is because of their promising applications in logic nanodevices [A.3], memory devices [A.4], Si photonics [A.5] and third generation photovoltaics [A.6]. The high compatibility of Si ND based devices with integrated circuits further makes them a favorable candidate for mass production on an industrial scale. Among these applications, the mechanism of charge storage in Si NDs and carrier tunneling transport through them plays an important role. In particular, resonant tunneling via discrete energy levels of the NDs is a unique property to achieve high speed logic devices or selective energy contacts (SECs) required in hot carrier solar cells (HCSCs) as one implementation of the third generation photovoltaic strategies. HCSCs could address the power loss mechanism in today's solar cell and allow reaching theoretical energy conversion efficiencies of up to 85 % [A.7]. HCSC

scheme requires two important elements: an absorber with slow carrier cooling properties and SECs as shown in Fig. A-1. SECs serve the role to collect hot carriers from the absorber and prevent them from cooling down by external cold carriers. In this regard, the selective contacts need to provide a certain energy level to allow carriers only with specific energy to tunnel to the electron and hole contacts, respectively. Resonant tunneling structures based on Si NDs embedded in the center of two SiO_2 tunneling barriers meet the requirements for SECs since they have wide bandgap energy and allow high transmission only through their discrete energy levels [A.6]. Schematic description of this mechanism is depicted in Fig. A-2, in which the schematic illustrations of the corresponding current-voltage (IV) characteristics under various bias conditions and resonant tunneling induced negative differential resistance (NDR) effect are revealed.

In our previous outcome, IV properties with the NDR effect have been investigated on a double-barrier structure (SiO_2/Si NDs/SiO_2) at low temperatures as shown in Fig. A-3, in the range of V_G = 0.25 V and 0.5 V. In this study, capacitance-voltage (CV) method was further employed to study resonant tunneling behavior at room temperature because for developing practical devices into commercial products, room temperature operation capability is necessary.

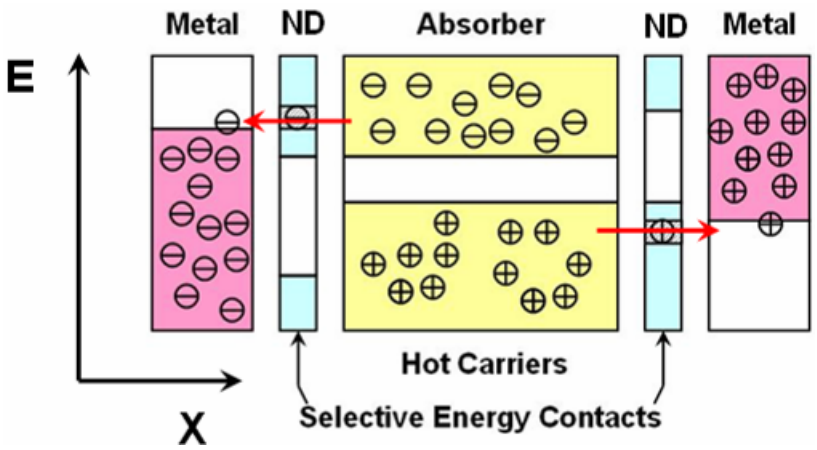


Fig. A-1 Hot carrier solar cell (HCSC) structure. Carriers only with specific energy corresponding to the discrete energy levels of Si NDs can tunnel through the selective energy contacts and thus alleviating power loss.

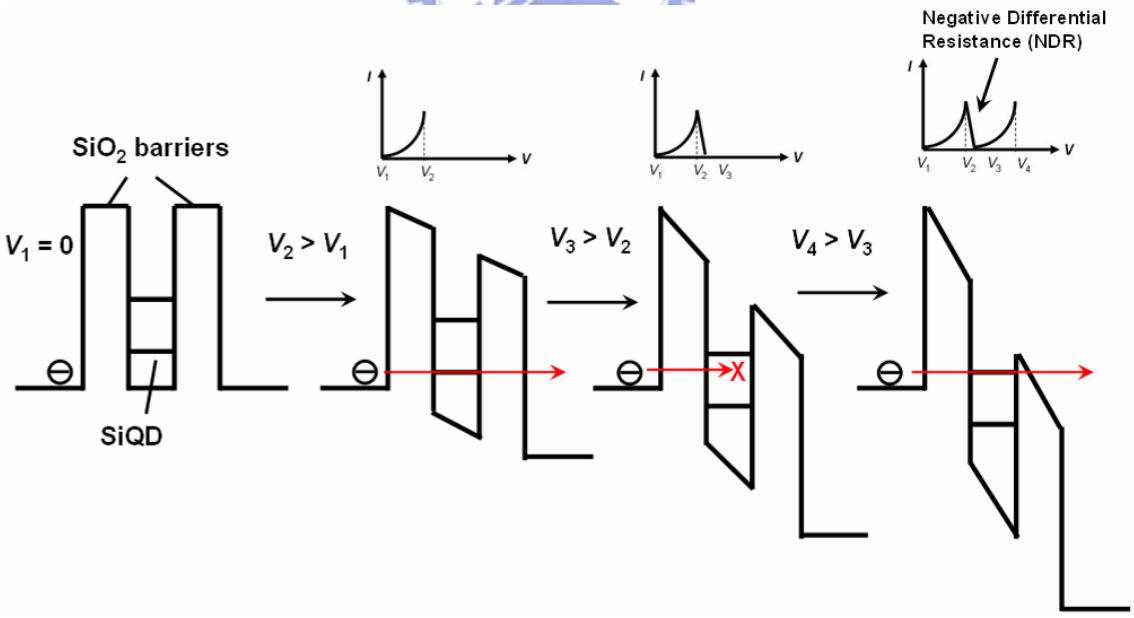


Fig. A-2 Simplified band diagrams illustrating resonant tunneling behavior under various biases and corresponding current-voltage characteristics.

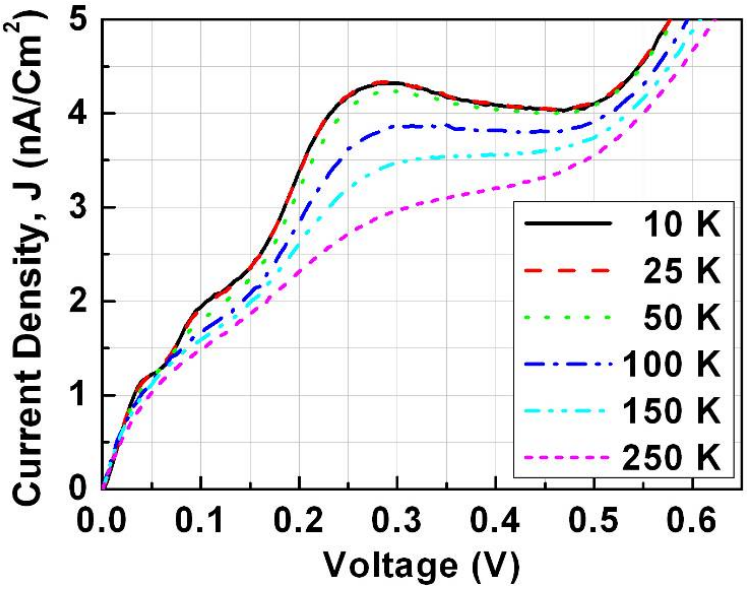


Fig. A-3 Temperature-dependent current-voltage characteristics of resonant tunneling structure with 3 nm SiO_2/2 nm Si NDs/3 nm SiO_2 stack [A.8].

A.2 Device Structure and Fabrication

Samples with Si NDs embedded in double-barrier structure were fabricated as follows. First, a stack of 3 nm-thick tunneling SiO_2, 2 nm-thick SiO_x (x = 1) and 3 nm-thick SiO_2 were in situ deposited layer-by-layer on a p-type Si substrate (ρ = 5~10 Ω-cm) in a remote plasma-enhanced chemical vapor deposition (RPECVD) system. The RPECVD technique offers the advantage of low radiation damage and lower defect density in the deposited layers compared to conventional PECVD deposition or sputtering techniques [A.9]. Subsequently, a 25 nm amorphous Si (a-Si) was deposited on the stack also in the same chamber. The samples were annealed at 1100

^{o}C for 1 hour in N_2 ambient, resulting in a distinct phase separation of the SiO_x layer into nanocrystalline Si NDs and amorphous SiO_2. Aluminum (Al) films were then deposited as the contacts on both front and back sides of the samples. The top gate is circular with diameter of 400 μm. The structure of a fabricated device is schematically shown in Fig. A-4. To reduce defect states in the oxide and at the Si/SiO_2 interface, the samples received forming gas (90 % N_2, 10 % H_2) annealing at 400 ^{o}C for 30 min. For comparison, the control samples with equivalent physical thickness of 8 nm SiO_2 (without Si NDs) by a similar processing were also prepared. In this study, CV measurements were performed on the samples using HP4284A Precision LCR meter at room temperature.

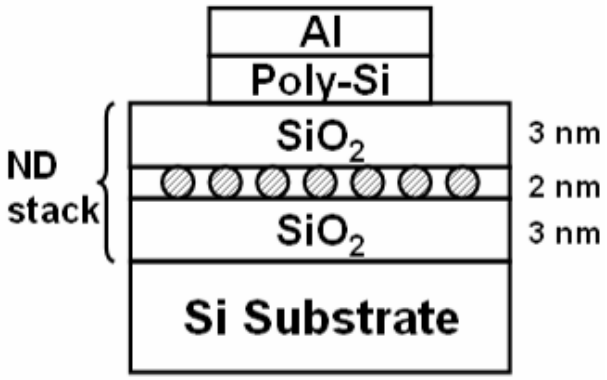


Fig. A-4 Schematic diagram of MOS diode with Si NDs embedded in SiO_2.

A.3 Results and Discussions

A.3.1 Capacitance-voltage Characteristics of the Si ND Diodes

Typical CV characteristics of the investigated Si NDs device are plotted in Fig. A-5. At first glance, a capacitance hump is clearly seen at around V_G = 0.3 V. In contrast, such hump is not observed in the control sample that contains no Si NDs in the embedded layer, as shown in the inset. It is noteworthy that the position of the capacitance peak is corresponding to the NDR region in IV plot (cf. Fig. A-3). Note that the NDR effect corresponds to the process of resonant tunneling through the energy states associated with the Si NDs. Therefore, this anomalous capacitance peak should be attributed to resonant tunneling transport via the Si NDs with composition of a sequential tunneling mechanism [A.10], i.e., the carriers tunnel into the Si NDs (charging) and then tunnel out of the NDs (discharging) sequentially, and thus contributing to the capacitance hump. Furthermore, through the measurement of forward (from -1.5 V to 1 V) and backward gate voltage sweeping (from 1 V to -1.5 V), no hysteresis or distortion is observed in the CV curves for samples with and without Si NDs embedded in SiO_2 inferring good property of the deposited films. This indication also indicates that the dominant charges contributing to the capacitance hump are trapped in the Si NDs or at the interface of Si NDs, rather than by trap states in the oxide layer or at interface between the tunneling oxide and the Si substrate.

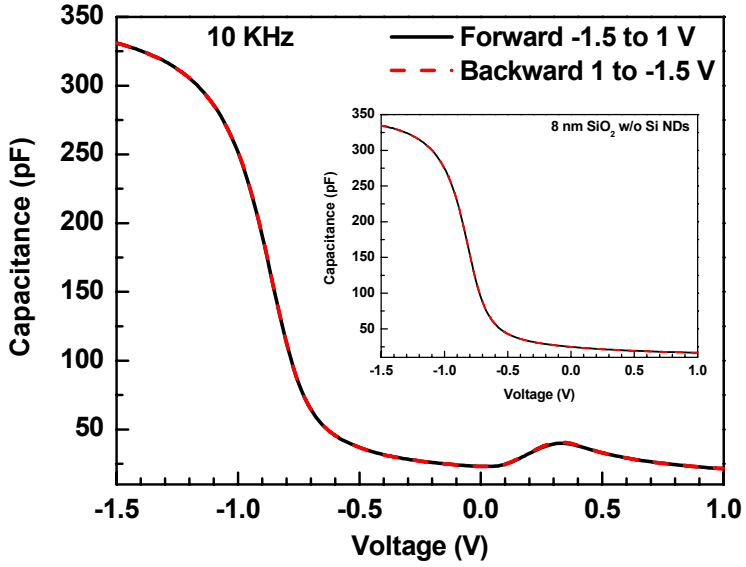


Fig. A-5 Typical capacitance-voltage characteristics of the Si ND device with double-barrier structure. Inset is the control sample without Si NDs in the embedded layer.

In addition, the constitution of the hump could be interpreted as gradual charging of the dots. When the applied gate voltage induces band bending to a level aligning with the discrete energy state in the Si NDs, carriers have the chance to be trapped (charging) into the dots via the sequential resonant tunneling through the double-barrier structure. This process will lead to gradual charge buildup in the Si NDs, causing parallel shift of the CV curves and accordingly constructing the hump as shown in Fig. A-6. Consequently, the amount of shifted CV curve and the peak height reflect the quantity of Si NDs participating in charging/discharging process.

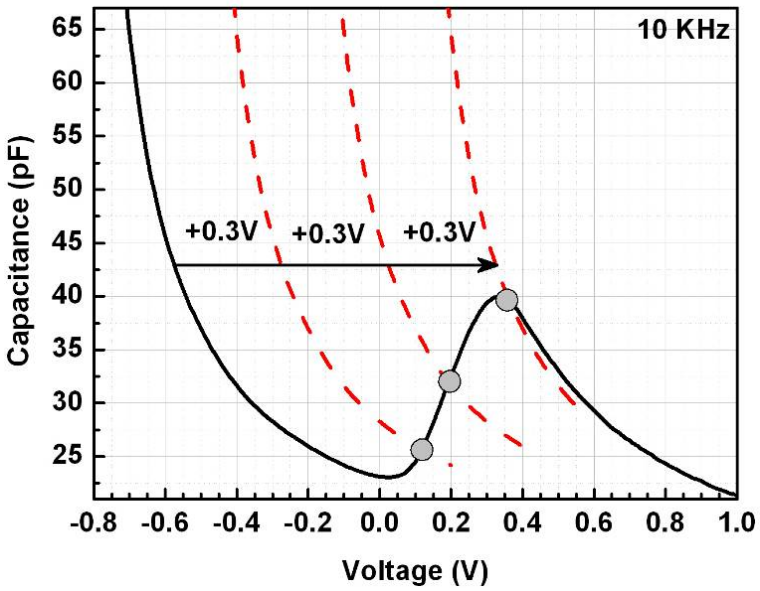


Fig. A-6 Schematic illustration for construction of the hump. The dashed curves in the plot represent the shift of the original one (solid).

In order to further support the feature of CV hump resulting from the charging/discharging process via the Si NDs, we here discuss whether the charge density (ρ) contributing to the peak corresponds to the ND density (ρ_{ND}). The charge density can be simply evaluated by integrating the area of the CV hump as shown in Fig. A-7 and Eq. (1). On the other hand, the capacitance density of NDs (C_{ND}) is extracted from Fig. A-7 by subtracting the peak capacitance density (C_{peak}) from the background one (C_B) as described in Eq. (2). Then the dot density (ρ_{ND}) could be estimated by using $\rho_{ND} = C_{ND}/C_{self}$, where C_{self} is the self-capacitance of a Si ND embedded in SiO_2 [A.11]. Comparing the results of Eq.(1) with Eq.(2), the fact that ρ

nearly equals ρ_{ND} suggests that roughly each ND provides one electron, and implies that the composition of the unique CV peak feature is owing to the charges existing in the Si NDs.

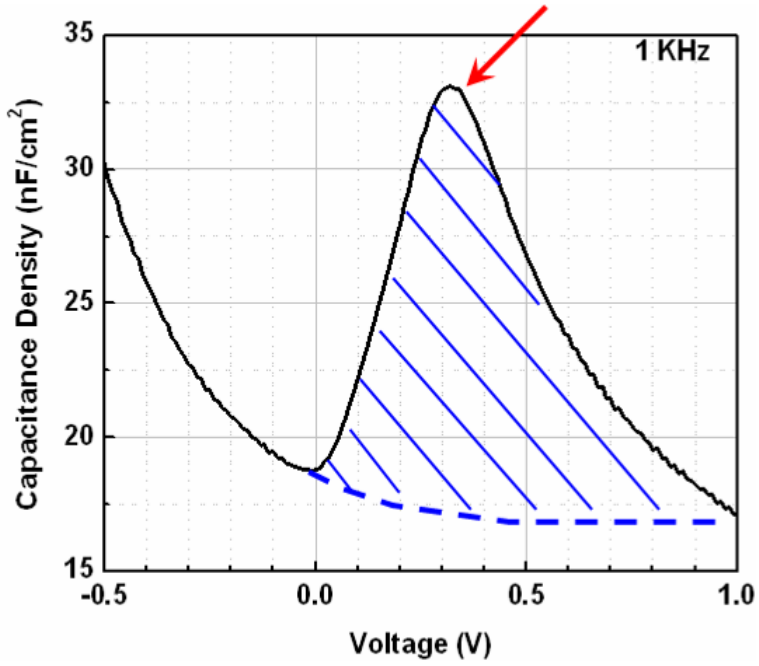


Fig. A-7 Capacitance density vs. voltage of the SiO_2/Si NDs/SiO_2 double-barrier structure near the peak position.

Charge density from the integral of the CV peak

$$\rho \cong \int \frac{(C \cdot V)_{peak}}{q} \cong 4.2 \times 10^{10} (cm^{-2}) \text{ ----------(1)}$$

$$\text{Peak capacitance density, } C_{peak} \cong 3.35\times10^{-8}(F/cm^2)$$

$$\text{Background capacitance density, } C_B \cong 1.75\times10^{-8}(F/cm^2)$$

$$\Rightarrow C_{ND} = C_{peak} - C_B \cong 1.6\times10^{-8}(F/cm^2)$$

$$\cong C_{self}\times\rho_{ND}$$

$$\Rightarrow \rho_{ND} \cong \frac{C_{ND}}{C_{self}} \cong 3.69\times10^{10}(cm^{-2}) \text{----------(2)}$$

$$(C_{self} = 4\pi\varepsilon_i\varepsilon_0 r \cong 4.34\times10^{-19}(F);\ \text{dot radius, } r \cong 1\,nm, \text{ in this work})$$

A.3.2 Frequency-dependent Properties of the Capacitance Peaks

Fig. A-8 shows frequency-dependent CV properties from 200 Hz to 1 MHz. It can be seen that there exists a dispersion of the capacitance with frequency in the hump region and the height of the peak increases as the ac frequency decreases. These properties could be explained by the schematic band diagram in Fig. A-9. For lower frequencies, most of the electrons in the inversion layer can follow the applied ac signal and tunnel through the tunnel oxide. When the Fermi level of the substrate is aligned with the discrete level of Si NDs, electrons can resonantly tunnel into the dots and result in the capacitance peak. While for higher frequencies, electrons can follow the ac modulation only near the interface. In addition, carriers are found to have different tunneling ability at various frequencies [A.12] and Si NDs with different orientation, size and shape lead to various tunneling time [A.13]. Also it is noted that the distribution of the Si NDs is not completely confined in the original SiO_x layer as

shown in Fig. A-10. Consequently, at higher frequencies, carriers can only charge the dots locating near the lower SiO_x/SiO_2 interface while for lower frequency, carriers have more possibility to tunnel into the dots near the upper SiO_2/SiO_x interface as illustrated in Fig. A-11. Overall, the dispersion of the capacitance hump found in Fig. A-8 involving frequency-dependent peak positions, peak heights and widths of the hump is associated with crystalline properties and tunneling capability of NDs and their distribution in the embedded layer.

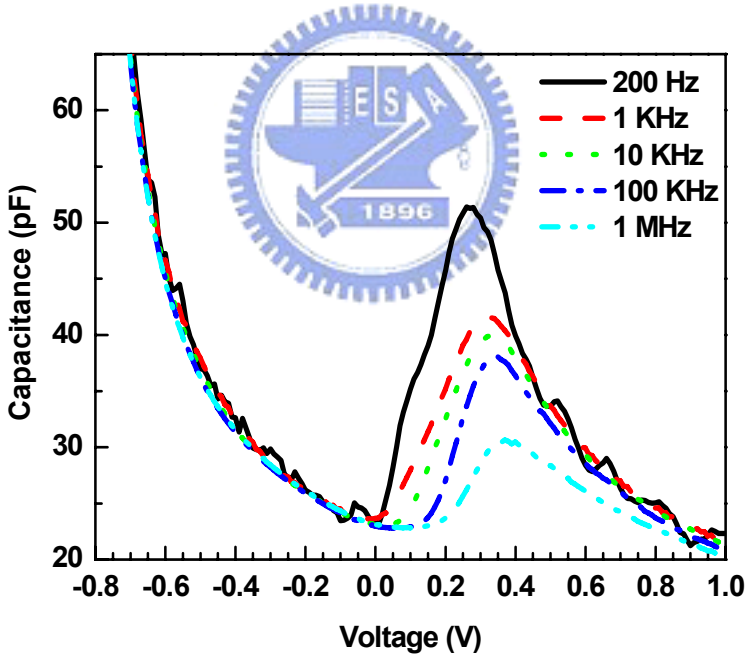


Fig. A-8 Plot of frequency-dependent CV characteristics.

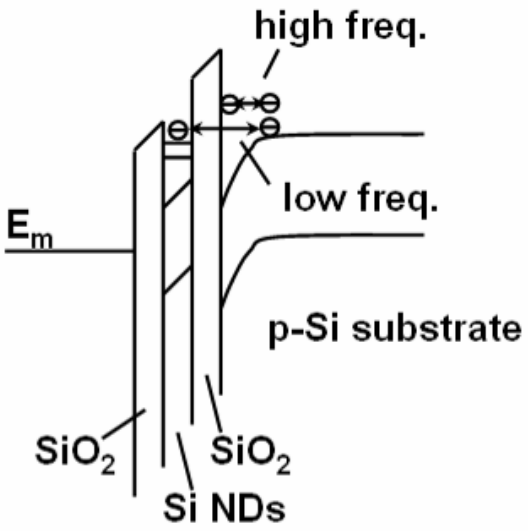


Fig. A-9 Schematic band diagram schematically illustrating the loading process of electrons into the discrete energy levels of Si NDs.

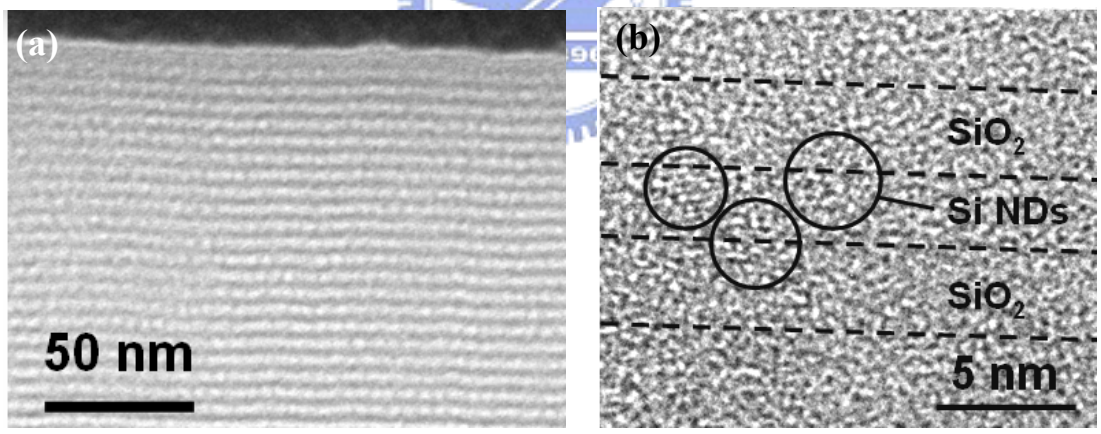


Fig. A-10 (a) Cross-sectional TEM image of a Si NDs/SiO_2 stack. The original SiO_2 layer was 3 nm and the SiO_x layer where the Si NDs precipitated from was 2 nm. The bright (dark) layers represent SiO_2 without (with) Si NDs. (b) HRTEM picture from (a) shows distribution of NDs [A.14].

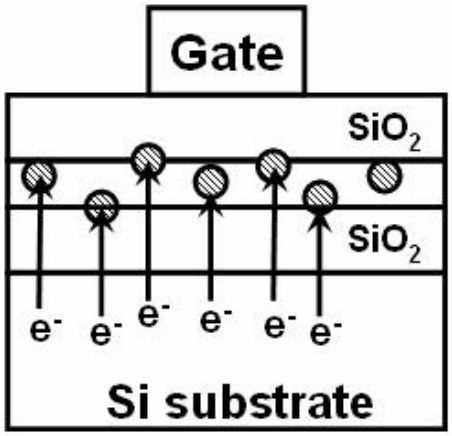


Fig. A-11 Schematic device diagram with nonuniform distribution of NDs embedded in the double-barrier oxide layers.

Fig. A-12 plots the peak capacitance at various frequencies extracted from the frequency-dependent CV curves. Note that three regimes can be observed in the plot. The first slope in the high-frequency regime (peak capacitance increases with decreasing frequency) could be ascribed to the response time. The response time (t) was simply estimated from the product of the measured capacitance (C) and the reciprocal of the measured conductance (R), which is approximately 5 μs. The corresponding frequency is thus 200 kHz, nearly responding to the turning point of the peak capacitance versus frequency plot. Beyond this frequency, most carriers could follow the ac modulation and tunnel into the Si NDs, resulting in the slight change in the capacitance peak behavior in the range of 1 kHz to 200 KHz. The time

constant evaluated in our study is in good agreement with the theoretically calculated results of Sousa *et al.* [A.13, A.15], in which the transfer time is found to be associated with the size, shape and orientation of Si NDs as well as the thickness of tunnel oxide. However, the peak capacitance increases with decreasing frequency when the frequency is below 1 kHz. This phenomenon could be understood by reviewing the CV curve at 200 Hz in Fig. A-8, which is composed of two peaks at around V_G = 0.12 V and 0.26 V, respectively. The superposition of these two peaks accordingly results in a more pronounced capacitance hump. This effect may be ascribed to the influence of slow trap states at the interface of Si NDs [A.16] or another energy states in NDs.

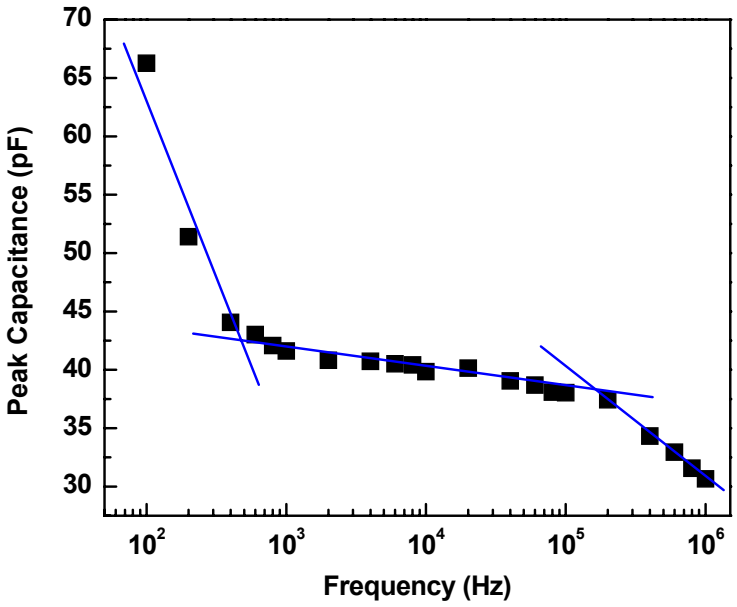


Fig. A-12 Plot of peak capacitance vs. frequency.

A.3.3 Stability of Resonant Tunneling Behaviors

To examine the stability and repeatability of charging/discharging and tunneling behaviors of the Si ND device with double-barrier structure, capacitance response at two alternant gate bias conditions for several cycles was monitored as shown in Fig. A-13. The two applied gate biases are chosen as V_1 (at capacitance peak position) and V_2 (the bias at the foot of the peak), as depicted in Fig. A-14. In Fig. A-13(a), the two corresponding capacitance values are steady with time when biased at V_1 and V_2, respectively. The constant peak capacitance over time infers that the carriers are stably tunneling into, storing and tunneling out of the dots during the operation. Moreover, when the gate voltages changes from V_1 (V_2) to V_2 (V_1), the capacitance decreases (increases) immediately since the Fermi level of the Si substrate is not (is) aligned with the energy level of the dots. This fact signifies that the resonant tunneling process could respond immediately to the change of band structure at low frequency. However, the capacitance increases with time during the operation at 1 MHz as shown in Fig. A-13(b). This effect is ascribed to the fact that the charging/discharging of carriers in the Si NDs cannot follow the ac modulation at high frequency. After the device is biased at V_1 for a period of time, most of carriers cannot detrap instantaneously from the dots when the bias is changed back to V_2, causing a higher capacitance over the preceding cycle. These results imply that the stability and

reliability of the resonant tunneling behavior of the Si ND devices is related to the applied ac frequencies.

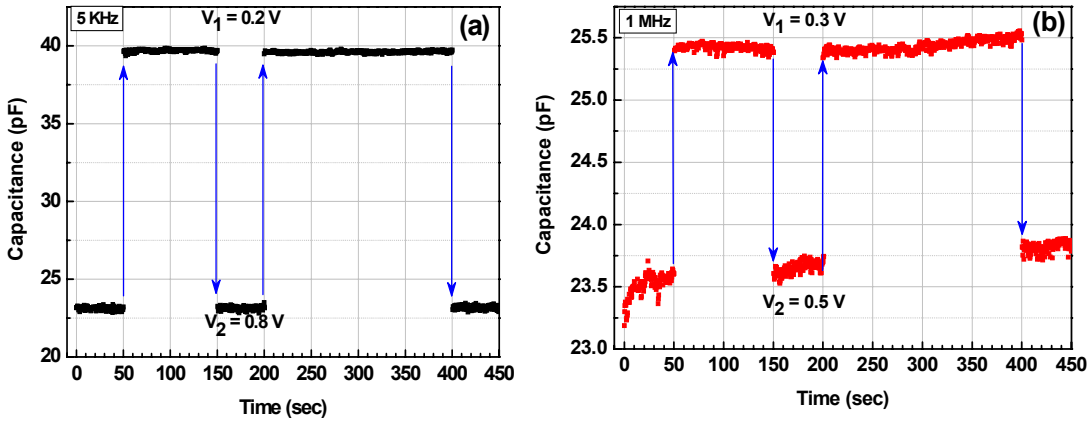


Fig. A-13 Capacitance vs. time at two alternant gate voltages at (a) 5 kHz and (b) 1 MHz.

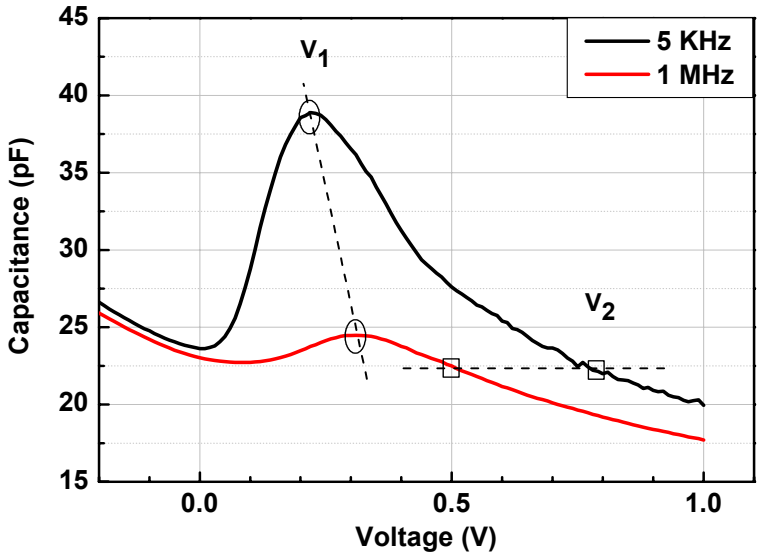


Fig. A-14 C-V characteristics near the peak positions showing the selection method of V_1 and V_2.

A.4 Summary

In conclusion, experimental evidence for electron tunneling and storage in SiO_2/Si NDs/SiO_2 double-barrier structure has been studied by CV characterization at room temperature. The anomalous peaks in CV curves are found to be associated with the sequential resonant tunneling transport and gradual charging effect in Si NDs. Moreover, apparent frequency-dependent properties of the capacitance peaks were also observed and were attributed to the response time, distribution and size fluctuation of the Si NDs as well as the potential contribution of slow trap states. The time-dependent CV measurement at low frequency further reveals high stability and repeatability of charging/discharging effects of the Si ND devices. As a consequence, a better understanding of carrier transport behaviors via Si NDs embedded in SiO_2 structures at room temperature is achieved by CV characterizations. This information therefore could form the basis for practical applications such as nanomemory and high speed logic nanodevices as well as hot carrier solar cells.

A.5 Acknowledgment

This work was mainly done in the Institute of Semiconductor Electronics (IHT) at RWTH Aachen University during the execution of the Sandwich program (No.

96-2911-I-009-024-2) in Germany (September 2007- August 2008). The author would like to express the deepest gratitude to NSC (Taiwan) and DAAD (Germany) for the grant. He also shows his appreciation to Prof. H. Kurz, Mr. B. Berghoff and all IHT colleagues for invaluable instruction and discussions as well as helpful experiment support.

References

[A.1] T. Baron, P. Gentile, N. Magnea and P. Mur, "Single-electron charging effect in individual Si nanocrystals," *Appl. Phys. Lett.*, **79**, 1175 (2001).

[A.2] T. Müller, K. H. Heinig and W. Möller, "Size and location control of Si nanocrystals at ion beam synthesis in thin SiO_2 films," *Appl. Phys. Lett.*, **81**, 3049 (2002).

[A.3] N. M. Park, S. H. Kim, S. Maeng and S. J. Park, "High negative differential resistance in silicon quantum dot metal-insulator-semiconductor structure," *Appl. Phys. Lett.*, **89**, 153117 (2006).

[A.4] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe´ and K. Chan, "A silicon nanocrystals based memory," *Appl. Phys. Lett.*, **68**, 1377 (1996).

[A.5] A. Irrera, F. Iacona, I. Crupi, C. D. Presti, G. Franzo, C. Bongiorno, D. Sanfilippo, G. D. Stefano, A. Piana, P. G. Fallica, A. Canino and F. Priolo, "Electroluminescence and transport properties in amorphous silicon nanostructures," *Nanotechnology*, **17**, 1428 (2006).

[A.6] G. Conibeer, M. Green, R. Corkish, Y. Cho, E. C. Cho, C. W. Jiang, T. Fangsuwannarak, E. Pink, Y. Huang, T. Puzzer, T. Trupke, B. Richards, A. Shalav and K. L. Lin, "Silicon nanostructures for third generation

photovoltaic solar cells," *Thin Solid Films*, **511-512**, 654 (2006)

[A.7] P. Würfel, "Solar energy conversion with hot electrons from impact ionisation," *Sol. Energ. Mat. Sol. C.*, **46**, 43 (1997).

[A.8] B. Berghoff, R. Rölver, D. L. Bätzner, B. Spangenberg and H. Kurz, "Temperature dependent i-v measurements on resonant tunneling structures based on silicon quantum dots for energy selective contacts," *Proceedings of the 22nd European Photovoltaic Solar Energy Conference*, 571, 3-7 September (2007).

[A.9] P. D. Richard, R. J. Markunas, G. Lucovsky, G. G. Fountain, A. N. Mansour and D. V. Tsu, "Remote plasma enhanced CVD deposition of silicon nitride and oxide for gate insulators in (In, Ga)As FET devices," *J. Vac. Sci. Technol. A*, **3**, 867 (1985).

[A.10] M. Büttiker, "Coherent and sequential tunneling in series barriers," *IBM J. Res. Dev.*, **32**, 63 (1998).

[A.11] S. Tiwari, J. A. Wahl, H. Silva, F. Rana and J. J. Welser, "Small silicon memories: confinement, single-electron, and interface state considerations," *Appl. Phys. A*, **71**, 403 (2000).

[A.12] R. J. Luyken, A. Lorke, A. O. Govorov,J. P. Kotthaus, G. Medeiros-Ribeiro and P. M. Petroff, "The dynamics of tunneling into self-assembled InAs dots," *Appl. Phys. Lett.*, **74**, 2486 (1999).

[A.13] J. S. de Sousa, J. P. Leburton, A. V. Thean, V. N. Freire and E. F. da Silva, Jr., "Effects of crystallographic orientations on the charging time in silicon nanocrystal flash memories," *Appl. Phys. Lett.*, **82**, 2685 (2003).

[A.14] B. Berghoff, S. Suckow, R. Rölver, B. Spangenberg, H. Kurz, A. Dimyati and J. Mayer, "Resonant and phonon-assisted tunneling transport through silicon quantum dots embedded in SiO_2," *Appl. Phys. Lett.*, **93**, 132111 (2008).

[A.15] J. S. de Sousa, A. V. Thean, J. P. Leburton and V. N. Freire, "Three-dimensional self-consistent simulation of the charging time response in silicon nanocrystal flash memories," *J. Appl. Phys.*, **92**, 6182 (2002).

[A.16] E. H. Nicollian and A. Goetzberger, "The Si-SiO_2 interface-electrical properties as determined by the MIS conductance technique," *Bell Syst. Tech. J.*, **46**, 1055 (1967).

Vita

姓　　名：蘇俊榮　Chun-Jung Su

性　　別：男

出生日期：1979 年 9 月 7 日

地　　址：台南縣歸仁鄉文化村文化北二街 66 號

學 經 歷：

國立交通大學材料科學與工程學系　1998. 9 - 2002. 6

美國休士頓大學德州超導體中心 實習　2000. 7 - 2000. 8

Texas Center for Superconductivity, University of Houston, U.S.A.

國立交通大學電子研究所碩士班　2002. 9 - 2003. 6

國立交通大學電子研究所博士班　2003. 9 - 2008. 11

德國阿亨工業大學半導體電子研究所 訪問研究　2007. 9 - 2008. 8

Institute of Semiconductor Electronics, RWTH Aachen University, Germany

榮　　譽：2005 年第三屆國家新創獎學生獎第二名

2007 年行政院國科會與德國學術交流總署三明治計畫獎學金

博士論文：新穎矽奈米線元件之研製與應用

Fabrication and Analysis of Novel Silicon Nanowire Devices and Their Applications

Publication List

A. Journal Papers

1. H. C. Lin, M. H. Lee and **C. J. Su**, "Fabrication and characterization of nanowire transistors with solid-phased crystallized poly-Si channels," *IEEE Trans. Electron Devices*, **53**, 2471 (2006).

2. H. C. Lin and **C. J. Su**, "High-performance poly-si nanowire NMOS transistors," *IEEE Trans. Nanotechnology*, **6**, 206 (2007).

3. **C. J. Su**, H. C. Lin, H. H. Tsai, H. H. Hsu, T. M. Wang, T. Y. Huang and W. X. Ni, "Operations of poly-Si nanowire thin-Film transistors with multiple-gated configuration," *Nanotechnology*, **18**, 215205 (2007).

4. M. W. Ma, C. Y. Chen, W. C. Wu, **C. J. Su**, K. H. Kao and T. F. Lei, "Reliability mechanisms of LTPS-TFT with HfO_2 gate dielectric: PBTI, NBTI, and hot-carrier stress," *IEEE Trans. Electron Devices*, **55**, 1153 (2008).

5. M. W. Ma, C. Y. Chen, **C. J. Su**, W. C. Wu, T. Y. Yang, K. H. Kao, T. S. Chao and T. F. Lei, "Improvement on performance and reliability of TaN/HfO_2 LTPS-TFTs with fluorine implantation," *Solid-State Electronics*, **52**, 342 (2008).

6. C. Y. Hsiao, C. H. Lin, C. H. Hung, **C. J. Su**, Y. R. Lo, C. C. Lee, H. C. Lin, F. H. Ko, T. Y. Huang and Y. S. Yang, "Novel poly-silicon nanowire field effect transistor for biosensing application," *Biosensors and Bioelectronics*, in press (2008).

B. Letter Papers

1. H. C. Lin, M. H. Lee, **C. J. Su**, T. Y. Huang, C. C. Lee and Y. S. Yang, " A simple and low-cost method to fabricate thin-film transistors with poly-si nanowire channel," *IEEE Electron Device Lett.*, **26**, 643 (2005).

2. **C. J. Su**, H. C. Lin and T. Y. Huang, "High-performance TFTs with Si nanowire channels enhanced by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, **27**, 582 (2006).

3. H. C. Lin, **C. J. Su**, C. Y. Hsiao, Y. S. Yang and T. Y. Huang, "Water passivation

effect on polycrystalline silicon nanowires," *Appl. Phys. Lett.*, **91**, 202113 (2007).

4. M. W. Ma, T. S. Chao, **C. J. Su**, W. C. Wu, Y. H. Wu, T. Y. Yang, K. H. Kao and T. F. Lei, "Impacts of fluorine ion implantation with low-temperature solid-phase crystallized activation on high-κ LTPS-TFT," *IEEE Electron Device Lett.*, **29**, 168 (2008).

5. M. W. Ma, T. S. Chao, **C. J. Su**, W. C. Wu, Y. H. Wu, K. H. Kao and T. F. Lei, "Characteristics of PBTI and hot carrier stress for LTPS-TFT with high-κ gate dielectric," *IEEE Electron Device Lett.*, **29**, 171 (2008).

6. M. W. Ma, T. S. Chao, **C. J. Su**, W. C. Wu, K. H. Kao and T. F. Lei, "High-performance metal-induced laterally crystallized polycrystalline silicon p-channel thin-film transistor with TaN/HfO_2 gate stack structure," *IEEE Electron Device Lett.*, **29**, 592 (2008).

7. H. C. Lin, H. H. Hsu, **C. J. Su** and T. Y. Huang, "A novel multiple-gate polycrystalline silicon nanowire transistor featuring an inverse-T gate," *IEEE Electron Device Lett.*, **29**, 718 (2008).

8. C. H. Lin, C. Y. Hsiao, C. H. Hung, Y. R. Lo, C. C. Lee, **C. J. Su**, H. C. Lin, F. H. Ko, T. Y. Huang and Y. S. Yang, "Ultrasensitive detection of dopamine using a polysilicon nanowire field-effect transistor," *Chem. Commun*, 5749 (2008).

C. Conference Papers

1. **C. J. Su**, H. C. Lin, M. H. Lee, H. H. Tsai, Raymond C. T. Lin, S. W. Shen, C. C. Lee, T. Y. Huang and Y. S. Yang, "Effects of seeding window arrangement on the performance of Si nanowire transistors with MILC channels," *IEEE Silicon Nanoelectronics Workshop*, 167, June 11-12 (2006).

2. H. C. Lin, M. H. Lee, **C. J. Su**, H. H. Tsai, J. J. Hung and Raymond C. T. Lin, "Off-state leakage mechanism in novel Si nanowire transistors with solid-phase crystallized channels," *IEEE Silicon Nanoelectronics Workshop*, 65, June 11-12 (2006).

3. Raymond Lin, H. C. Lin, J. Y. Yang, S.-W. Shen and **C. J. Su**, "A novel method for the preparation of Si nanowires," *Int'l Conf. Solid State Devices and Materials*, 692, September 12-15 (2006).

4. **C. J. Su**, H. C. Lin, C. C. Hung, H. H. Tsai, Y. J. Lee, T. Y. Huang,

"Characteristics of poly-Si nanowire thin film transistors with double-gate structures," *Int'l Conf. Solid State Devices and Materials*, 510, September 12-15 (2006).

5. M. H. Lee, H.-H. Tsai, **C. J. Su**, C. C. Hung, H. C. Lin and T. Y. Huang, "Process and material modifications for leakage reduction in poly-Si thin-film transistors with nanowire channels," *Int'l Electron Devices and Materials Symp.*, OB006, December 7-8 (2006).

6. **C. J. Su**, H. C. Lin, H. H. Tsai, T. Y Huang, W. X. Ni, "Fabrication and Characterization of poly-Si nanowire devices with performance enhancement techniques," *IEEE Int'l Symp. VLSI-TSA*, 120, April 23-25 (2007).

7. Y. F. Huang, **C. J. Su**, M. H. Lee, H. H. Tsai, H. C. Lin, T. Y. Huang, "Suppression of off-state leakage in a novel poly-Si nanowire thin-film transistor," *IEEE Silicon Nanoelectronics Workshop*, 49, June 10-11 (2007).

8. H. H. Hsu, H. C. Lin, J. F. Huang and **C. J. Su**, "Poly-Si nanowire thin-film transistors with inverse-T gate," *Int'l Conf. Solid State Devices and Materials*, 818, September 18-21 (2007).

9. **C. J. Su**, C. Y. Hsiao, H. C. Lin, C. C. Lee, T. Y Huang and Y. S. Yang, "Polycrystalline silicon nanowire sensing devices," *Nanobioeurope Conf.*, June 9-13 (2008).

D. Local Journals

1. **蘇俊榮**、王子銘和林鴻志, "奈米線感測電晶體元件," *電子月刊*, 1 月號第 138 期, pp.199-207 (2007).

2. **蘇俊榮**、林鴻志、李明賢和黃調元, "多晶矽奈米線場效電晶體之製作與分析," *奈米通訊*, 第 14 卷第 1 期, pp.19-24 (2007).

3. **蘇俊榮**、林鴻志和黃調元, "高性能多晶矽奈米線場效電晶體," *電子月刊*, 10 月號第 147 期, pp.182-192 (2007).

E. Patents

1. C. C. Lee, H. C. Lin, **C. J. Su**, Y. S. Yang, T. Y. Huang, "矽奈米線場效電晶體裝置及作為奈米線生物感測與調控元件，及其製造 (Fabrication of nanowire transistors and nanowire bio-sensing and bio-regulating devices)," Patent No.

I294183, Taiwan.

2. H. C. Lin, **C. J. Su**, H. H. Hsu, "新穎奈米線通道非揮發性記憶體元件結構與製程 (Novel structures and processes of non-volatile memory devices with nanowire channels)," Taiwan and USA patents, pending.

3. H. C. Lin, **C. J. Su**, H. H. Hsu, G. J. Lee "新穎懸浮式奈米線通道之元件結構與製程 (Novel structures and processes of suspended nanowire channels)," Taiwan, USA, and Japan patents, pending.