國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

先進互補式金氧半元件的閘極層厚度 1nm 範圍下之

低漏電電荷幫浦量測技術

Low Leakage Charge Pumping Measurement Techniques for Advanced CMOS with Gate Oxide in the 1nm Range

研 究 生 ：馮信榮

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中華民國 九十三 年 七 月

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碩士論文

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摘要

美國半導體產業協會 (SIA) ITRS Roadmap 指出，到了西元 2005 年元件通道長度將進展到 75nm，而閘氧化層厚度將縮為 10~15Å。因此，如何觀察高穿隧漏電的 10~15Å 氧化層對下一代的 CMOS 技術是一大關鍵，尤其是觀察氧化層中界面缺陷和氧化層缺陷電荷的可靠性量測技術，相當欠缺。截至目前，有幾種量測氧化層可靠性的方法，如 DCIV, Gated-Diode (GD)、charge pumping(CP)等。然而，當超薄氧化層厚度低到 20 Å 以下，它們受限於量測時導致大量的閘極穿隧漏電流(gate leakage tunneling current)而產生嚴重量測誤差。

本論文主要的重點在於發展一套對於超薄氧化層 90nm CMOS 元件新的量測技術。我們已經成功的發展出這套結合 IFCP 方法和分離界面缺陷以及氧化層缺陷電荷的三步驟電荷中和的嶄新量測技術。

在這裡所使用的量測樣本的氧化層是經由DPN處理的製程。氧化層厚度有 14 Å 和 16Å，而且每種厚度分別都包含三種不同的氮含量。我們以介面缺陷和氧化層缺陷電荷的通道方向分佈情形來觀察不同厚度以及不同氮含

量的CMOS元件，在熱載子和NBTI影響下的可靠性比較。在短通道的情形下，元件衰退的主要偏壓條件從$I_{B,max}$轉換到$V_G = V_D$。在$V_G = V_D$的偏壓情形下，有高含量的氮以及較薄的nMOSFET元件有較好的可靠性，而有低含量的氮和較厚的pMOSFET元件有較好的可靠性。此外，在NBTI的影響下，我們發現氮含量對於元件的可靠度扮演一個重要的角色。從界面缺陷的分步情形，pMOSFET在NBTI影響下，擁有較高的氮含量會導致最差的元件衰退狀況。此外，我們也發現，pMOSFET在NBTI-like影響下會在高溫下增加熱載子對元件的影響，而且低含量的氮會有最佳的可靠性。

Low Leakage Charge Pumping Measurement Techniques for Advanced CMOS with Gate Oxide in the 1nm Range

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Abstract

As device scaling continues, the sub-100nm CMOS device needs a gate oxide thickness in the range of 10-15Å and with 75nm gate length in 2005, as predicted from the SIA roadmap. How to monitor oxide quality for ultra-thin gate oxide with tunneling leakage current is crucial for the next generation CMOS technology, in particular the monitoring of interface traps (N_{it}) and oxide trapped charges (Q_{ot}) in the gate oxide. So far, various gate oxide reliability diagnostic tools, such as DCIV, GD(Gated-Diode), CP(Charge-Pumping) etc. have been employed for such a purpose. For ultra-thin gate oxide down to below 20 Å, the above methods are limited by the tunneling leakage through the gate oxide during the measurement since direct tunneling exists.

This thesis has been focused on developing new techniques for the measurement of ultra-thin gate oxide 90nm CMOS devices. We have successfully developed new method,

combing IFCP method to remove direct tunneling current and an improved three-steps neutralization to separate N_{it} and Q_{ot} measurement technique.

The test sample in this work is prepared based on the DPN gate oxide process. The EOT of gate oxide thickness are 14Å and 16 Å, which have three different nitrogen concentrations, respectively. We compare the oxide thickness dependence and concentration of plasma nitridation of CMOS device under HC stress and NBTI stress from the lateral profiling of interface traps and oxide traps. In short channel length, the dominate stress condition of device degradation switched from $I_{B,max}$ to $V_G = V_D$. Under $V_G = V_D$ stress condition, the gate oxide with higher plasma nitrogen density and thinner thickness has better reliability for nMOSFET and the gate oxide with lower plasma nitrogen density and thicker thickness has better reliability for pMOSFET. Moreover, we found that nitrogen played an important role in device reliability under NBTI stress. From the result of the distribution for interface traps, we know that the highest plasma nitrogen density in oxide has the worst case of device degradation under NBTI stress for pMOSFET. In addition, we have seen that NBTI-like stress enhances HC effect at high temperature and the lowest nitrogen content has the best reliability in pMOSFET.

誌 謝

在兩年碩士研究生涯中，首先要向我的指導教授莊紹勳老師表達深摯的謝意。尤其是老師對於事物的嚴謹態度，使我在處理事情的態度上有所成長。除此之外，他對於學生的默默關懷，我必須在此表達感謝之意。

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最後要感謝是我的家人和女友，你們是我精神上最大的支柱，所有的壓力在回家和你們閒聊中得以解脫。沒有你們默默的支持和關愛，我無法堅持到最後。

謹將這份榮耀獻給培養我多年的父母親。

Contents

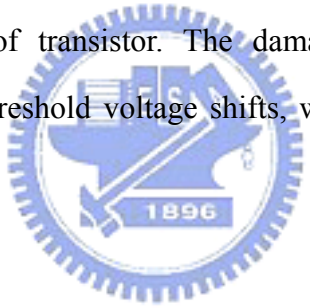
Figure Captions

Table Captions

Chapter 1
Introduction

1.1 The Motivation of This Work

As gate oxide thickness in MOS device is reduced below 1.6nm, the increasing gate leakage current is crucial for a continuous transistor scaling. Reliability of the ultra-thin SiO_2 presents another major concern. With the shrink of the channel length, electrons or holes in the channel or in the saturated region of MOSFET's can gain sufficient energy from the high lateral field to trigger the impact ionization phenomenon. Part of these heated carriers can surmount the energy barrier or tunnel into the gate oxide leading to the generation of traps at the interface or into the oxide. This consequently induces the trapping of electrons or holes in the stress region at the drain of transistor. The damage effect results in current and transconductance degradations, threshold voltage shifts, which thereby significantly reduces the device speed performance.

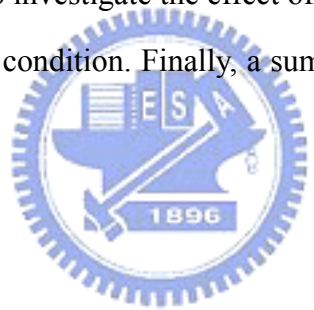


There are three major techniques, i.e., charge pumping [1-2], gated diode [3], and DCIV [4], for the characterization of interface/oxide traps (N_{it}/Q_{ot}) in CMOS devices. However, for sub-100nm device with t_{ox} in the range 10-20Å, none of the above has been provided for quantitative calculation of N_{it}/Q_{ot}. A recent one reported by our group using gated-diode for a thicker oxide is given in [5] where N_{it} and Q_{ot} can be separated. The gated-diode [3] and DCIV can measure the generation-recombination current due to N_{it} and/or Q_{ot} in the form of drain or substrate current, however, for very thin gate oxide, a quantitative analysis is difficult and not available so far. Also, during measurement, we need to overcome the induced leakage current using any of the above methods. In [6], it has demonstrated successfully an IFCP (Incremental Frequency Charge Pumping) method for the interface characterization. However, further effort is needed for a full characterization of device reliability, including hot carrier and NBTI for devices with tox$\leqq$20Å.

In this thesis, a complete solution has been provided for the characterization of HC (hot carrier) and NBTI effects. Results have been demonstrated for nMOSFET and pMOSFET with short channel length and ultra-thin gate oxide.

1.2 **Organization of This Thesis**

This thesis has been divided into five chapters. Chapter 2 describes the devices used in this work and experimental setup. The low leakage IFCP method and a simple neutralization method will be used to determine the lateral profiling of both interface traps and oxide traps. At the same time, the improvement of GIDL measurement will be described. In Chapter 3, we will use the method of Chapter 2 to discuss hot carrier reliability of CMOS device. In Chapter 4., we also use the same method to investigate the effect of concentration of plasma nitridation under NBTI and NBTI-like stress condition. Finally, a summary and conclusion will be given in Chapter 5.



Chapter 2

Device Fabrication and Experimental Measurements

After long-term operation or hot carrier stress, MOSFET device interface will induce damage, especially locating at the overlap region of gate to drain. This damage will cause MOSFET device degradation, including drain current degradation, transconductance degradation, and threshold voltage shift etc. In addition, as mentioned in the previous chapter, the increasing gate leakage current due to decreasing oxide thickness must be overcome for accurately evaluating the distribution of interface traps and oxide traps.

To investigate the hot carrier and NBTI induced MOSFET device degradation, the technique which has been able to determine the interface traps and oxide traps distribution becomes important. This chapter is divided into four sections. In the first section, the devices used in this study are examined. Then, the experimental analysis methods used in thesis will be introduced, including the low leakage IFCP method, three steps neutralization method for separate interface traps and oxide traps, and the improvement of GIDL method.

2.1 Device Fabrication

Fabrication process for gate oxide thickness technology used in this work is shown in Fig. 2.1. Gate dielectrics were grown with a decoupled plasma nitridation (DPN) process, consisting of three steps. First, a ultra-thin SiO_2 film with optical thickness of 12 Å and 14 Å is grown using *in-situ* steam generation oxidation or rapid thermal oxidation. The next step consists of exposing the oxide to a high density, pulsed-RF N_2-plasma, during which nitrogen is incorporated in the dielectric film. The idea behind using a pulsed plasma, where the source power is turned on and off at kHz frequencies, as compared to continuous (non-pulsed) wave plasma, is to have ions striking the wafer surface with lower kinetic energy. This less aggressive nitridation is then used in an attempt to, upon incorporation of higher amounts of

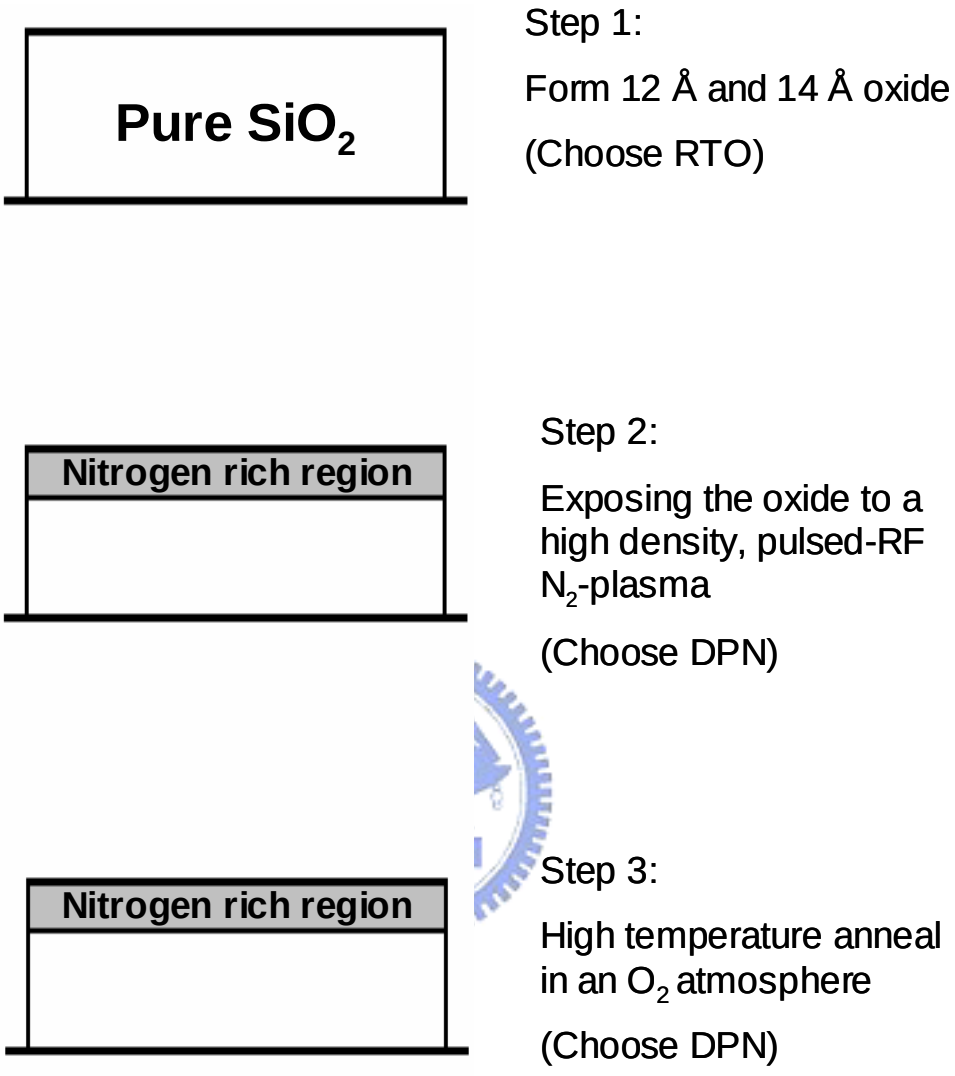


Fig. 2.1 Fabrication process for DPN gate oxide CMOS technology.

nitrogen into the films, minimize degradation in reliability and effective mobility of the carriers. Various nitridation time, pulsed RF frequencies, and plasma effective powers were thus studied. A final stabilization step consists of a high temperature anneal, the so-called post-nitridation anneal (PNA), in an O_2 atmosphere. The effect of using different PNA temperatures and pressures was investigated. For electrical evaluation, these oxynitrides were capped with 100 nm-thick polysilicon and incorporated into NMOS and PMOS transistors (90 nm technology) and capacitors. The EOT (equivalent of thickness) of gate oxide in these test samples were 14 Å and 16 Å and the concentrations of plasma nitridation have three different contents (low, medium, and high).

2.2 The Low Leakage IFCP Technique

2.2.1 Basic Experimental Setup

The experimental setup for the I-V measurement of MOS device is illustrated in Fig. 2.2. Based on the PC controlled instrument environment, the complicated and long-term characterization procedures for analyzing the intrinsic and degradation behavior in MOSFET's can be easily achieved. As shown in Fig. 2.2, the characterization equipment, including the semiconductor parameter analyzer (HP4156c), the dual channel pulse generator (HP8110A), low leakage switch mainframe (HP E5250A), the cascade guarded thermal probe station and thermal controller, provides an adequate capability for measuring the device I-V characteristics.

2.2.2 Experimental Setup of Charge Pumping Measurement

The basic setup of charge pumping measurement is shown in Fig. 2.3. The source, drain and bulk electrodes of tested devices are grounded. A 1MHz square pulse waveform provided by HP8110A with fixed base level (V_{gl}) is applied to NMOS gate, or with fixed top level (V_{gh}) is applied to PMOS gate. We keep V_{gl} at –1.0V while increase V_{gh} from –1.0V to 1.0V by step 0.1V, or keep V_{gh} at 1.0V while decrease V_{gl} from 1.0V to –1.0V by step –0.1V.

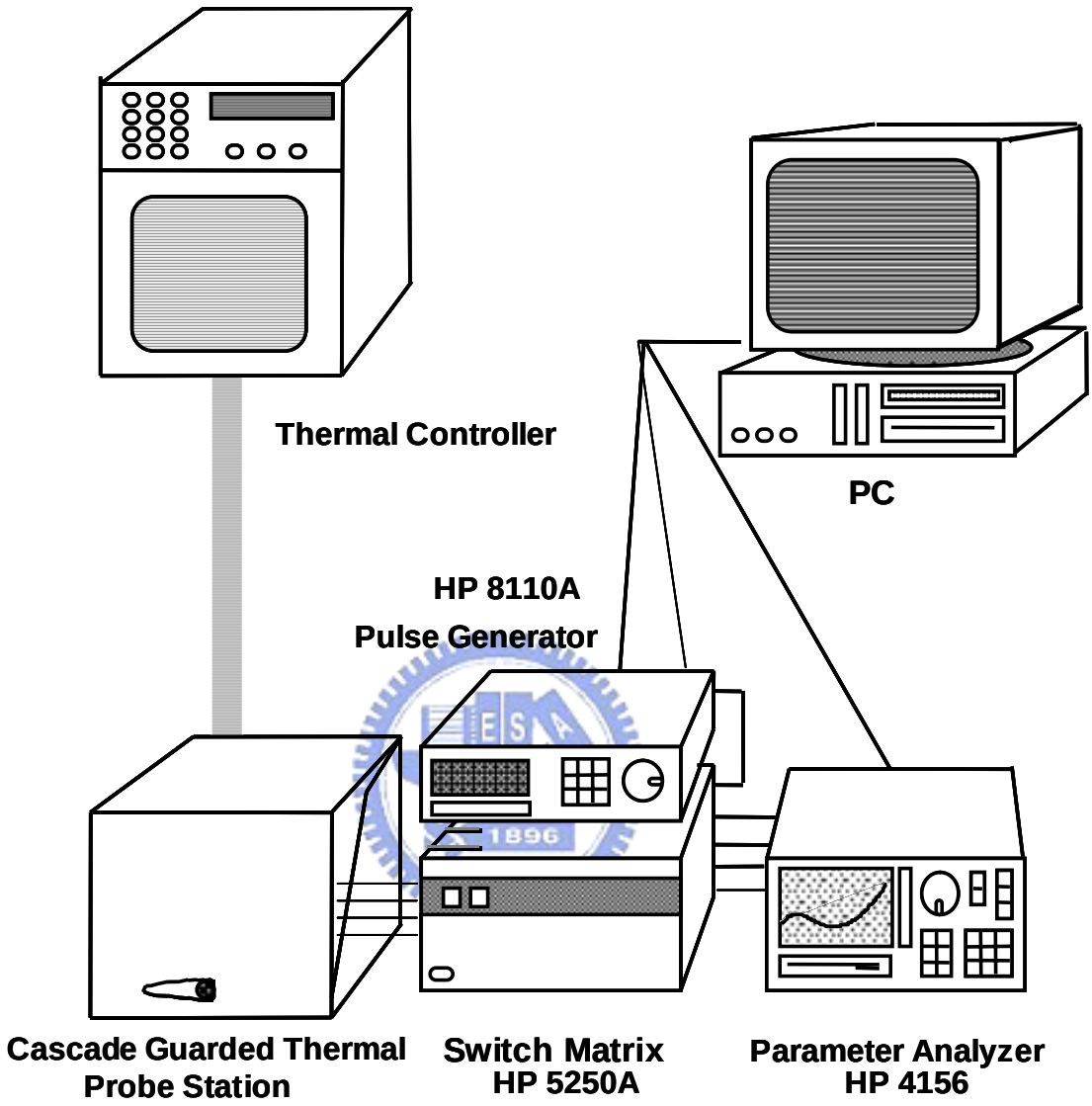


Fig. 2.2 The experiment setup for the current-voltage measurement. An automatic controlled characterization system is set up based on the PC controlled instrument environment.

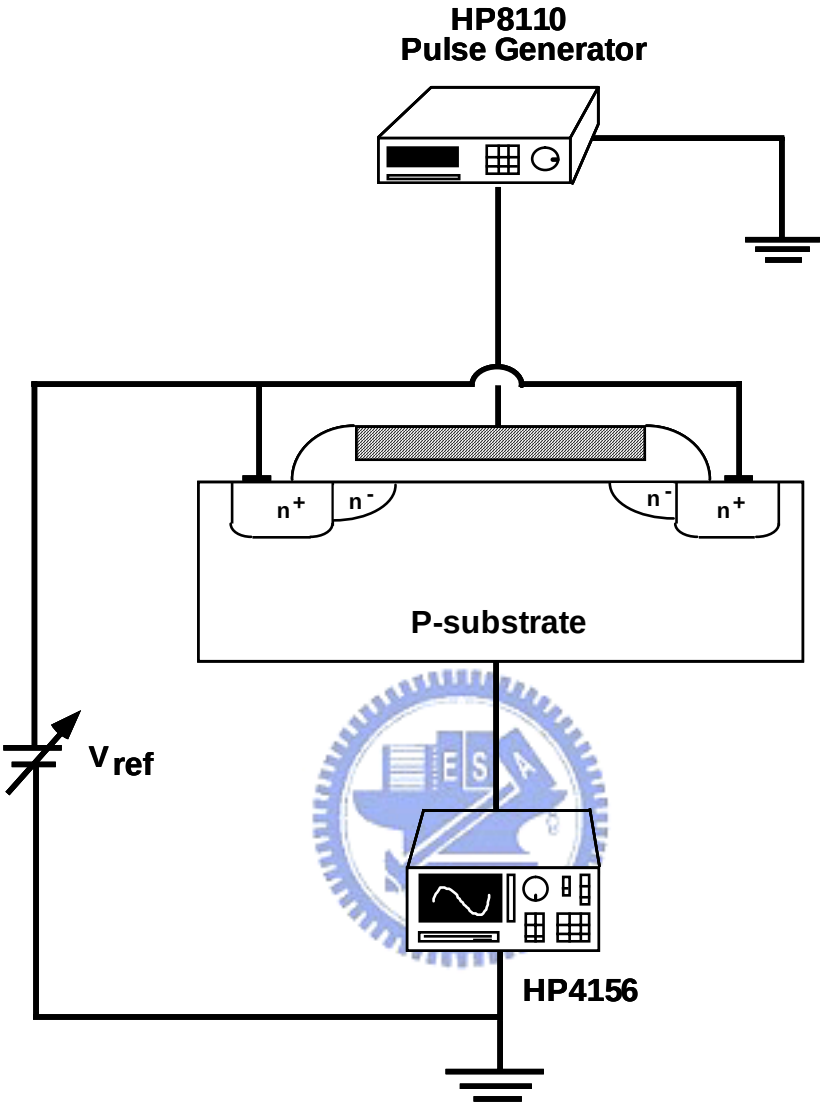


Fig. 2.3 Basic experimental setup for the charge pumping measurement.

With a smaller voltage step, we get a higher profiling resolution. The parameter analyzer HP4156C is used to measure the charge pumping current (I_{CP}).

2.2.3 Principle of the Low Leakage IFCP Method

Figures 2.4 (a) and (b) show the schematic of a low leakage IFCP measurement for CMOS developed by [6]. With both S/D grounded and by applying a gate pulse with a fixed base level (V_{gl}) and a varying high level voltage (V_{gh}) for NMOS, the channel will operate between accumulation and inversion. This gives rise to the charge pumping current I_{CP} (=I_B) measured from the bulk. However, leakage current I_G is unavoidable, as we see from Fig. 2.4 (a), the leakage of I_{CP} is very small when t_{ox} >30Å. However, as reveals in Fig. 2.5 that the leakage current increases, curves (1) and curves (2), for tested sample (EOT= 14Å). From the measured I_{CP} for two frequencies, f_1 and f_2, can be expressed as

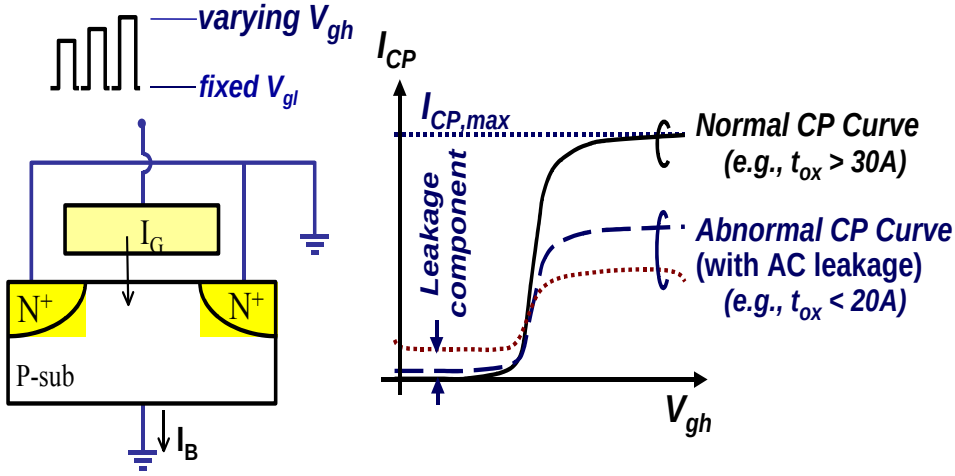
$$I_{CP,\, f1 \text{ with-leakage}} = I_{CP,\, f1 \text{ correct}} + I_{CP,\, \underline{\text{leakage@}f1}} \quad (2.1)$$

and

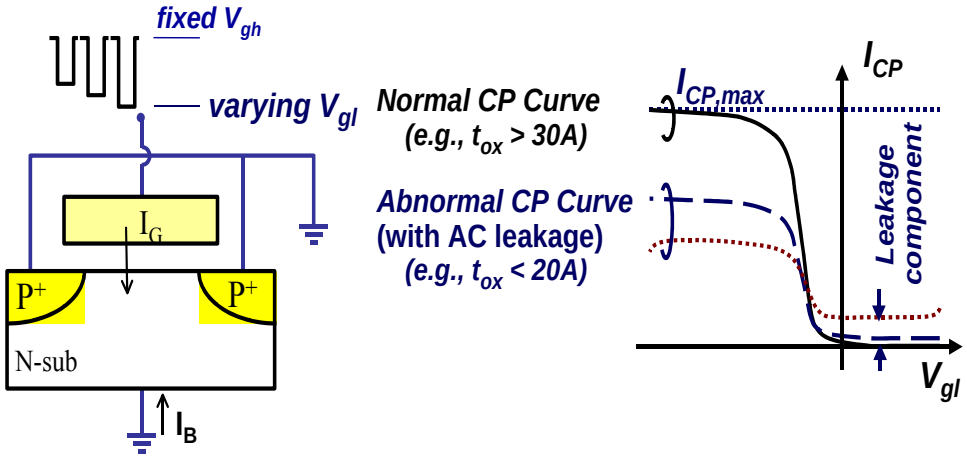
$$I_{CP,\, f2 \text{ with-leakage}} = I_{CP,\, f2 \text{ correct}} + I_{CP,\, \underline{\text{leakage@}f2}}. \quad (2.2)$$

When the frequency is sufficient high, the leakage components in these two frequencies are almost the same ($I_{CP,\, \text{leakage@}f1} \approx I_{CP,\, \underline{\text{leakage@}f2}}$). We take the difference of I_{CP} ($\Delta I_{CP,\, f1-f2}$) between two frequencies. From equations (2.1) and (2.2), the difference of these two CP curves gives

$$\Delta I_{CP,\, f1-f2} = I_{CP,\, f1 \text{ with-leakage}} - I_{CP,\, f2 \text{ with-leakage}}. \quad (2.3)$$



(a)



(b)

Fig. 2.4 The schematic of charge pumping (CP) for
(a) nMOSFET measurement. (b) pMOSFET measurement.
Induced leakage current(I_G) occurs when t_{ox}< 20A.

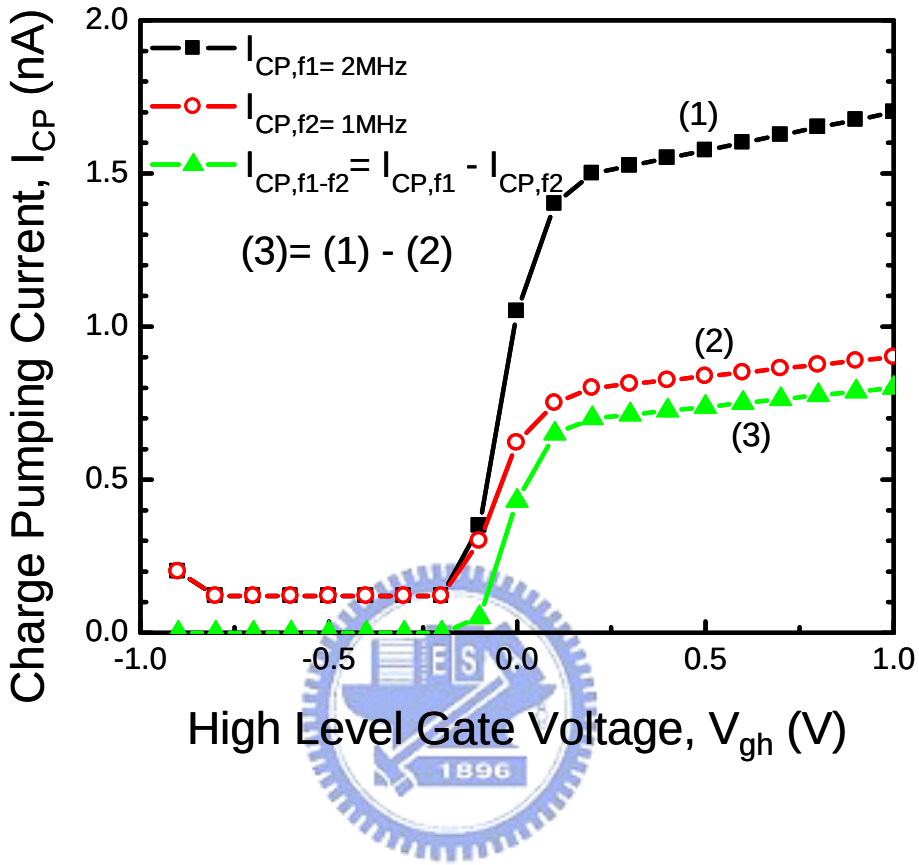


Fig. 2.5 Measurement I_{CP} at two different frequencies. The low leakage IFCP method is achieved by substracting I_{CP} at two successive frequencies

Since the correct CP curve is directly proportional to the frequency, it will be equal to the difference of two CP curves. Therefore, in the IFCP method, the correct CP curve at frequency ($f1$- $f2$) can be given by

$$I_{CP,\ f1-f2} = \Delta I_{CP,\ f1-f2}. \tag{2.4}$$

For example, $I_{CP(2MHz)} - I_{CP(1MHz)}$ is regarded as the I_{CP} at their difference frequency, 1MHz. The correct result is shown in curve (3).

2.2.4 Extraction of the Effective Channel Length

Figure 2.6 shows the non-uniform interface trap distribution for extraction of effective channel length. Using two different channel lengths, the interface traps can be represented by

$$N_{it,\ 1,\ total} = N_{it,\ 11}(\text{edge}) + N_{it,\ 12}(\text{center}), \tag{2.5}$$

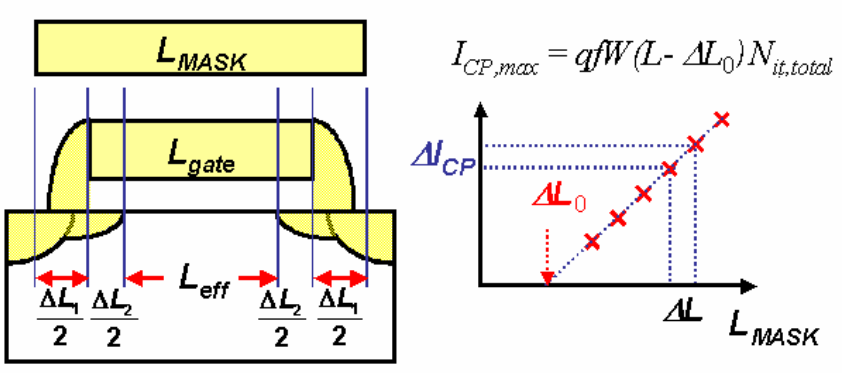
and

$$N_{it,\ 2,\ total} = N_{it,\ 21}(\text{edge}) + N_{it,\ 22}(\text{center}). \tag{2.6}$$

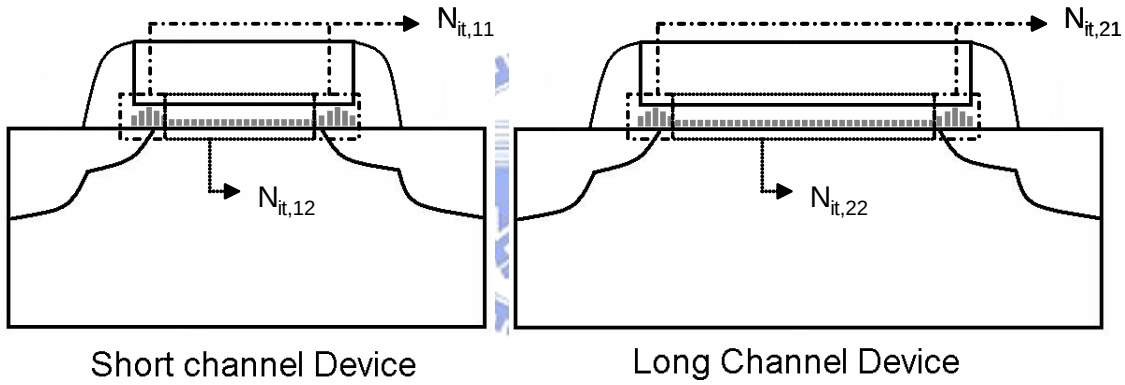
Since the mechanical stress in two different channel devices are almost the same, $N_{it,\ 11}$ is approximately equal to $N_{it,\ 21}$. To eliminate the traps generated at the edge region, the difference of these two interface traps can be used, which is directly proportion to the ΔL. Hence, we have

$$\Delta I_{CP,\ max} \propto \Delta N_{it,\ total} = N_{it,\ 1,\ total} - N_{it,\ 2,\ total} = N_{it,\ 12} - N_{it,\ 22} \propto \Delta L. \tag{2.7}$$

Figure 2.6 (a) shows the definitions of ΔL_1, ΔL_2, and ΔL_0, which can be expressed by



(a)



(b)

Fig. 2.6 Illustration of ΔL_0 extraction from CP data. (a) Parameter definition and extraction method. (b) Interface traps distribution is short and long channel length device.

$$\Delta L_1 = L_{MASK} - L_{gate}, \quad (2.8)$$

$$\Delta L_2 = L_{gate} - L_{eff}, \quad (2.9)$$

and

$$\Delta L_0 = L_{MASK} - L_{eff} = \Delta L_1 + \Delta L_2. \quad (2.10)$$

Figures 2.7 (a) and (b) show the calculated interface traps, N_{it}, per unit width and offset length, $\Delta L_0 = L_{MASK} - L_{eff}$, for measured 24 devices with nMOSFET and pMOSFET in this work.

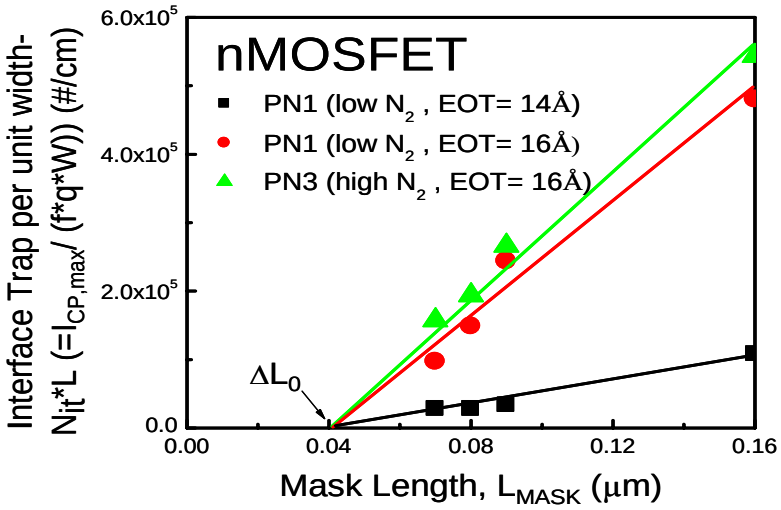
2.3 Principle of the Interface/Oxide Traps Profiling Technique

Based on [7-8] and Table 2.1, we can separate the Q_{ot} from N_{it} and then we get the lateral profiling of interface and oxide traps. The steps are as follows.

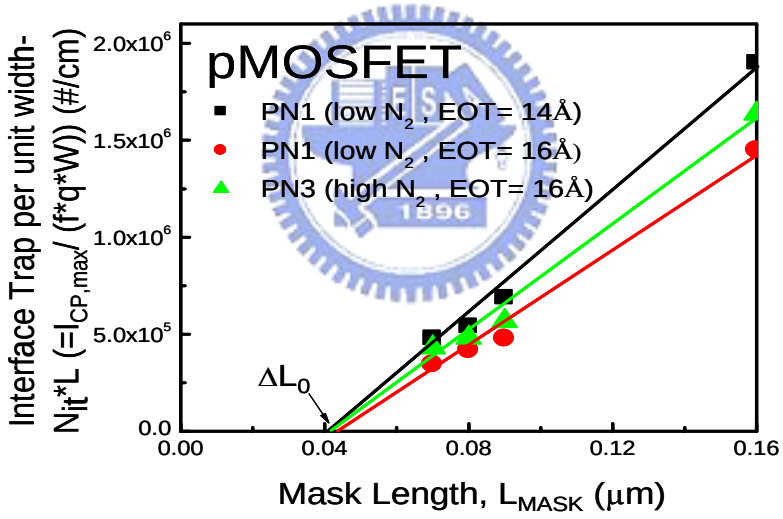
1. For a fresh device, the drain current (at V_G= -2V) is measured, curve (1). Again, the device is stressed and its current, curve (2), is measured, Fig. 2.8.
2. To identify whether Q_{ot} is generated, we monitor the GIDL current as given in Fig. 2.9, from which we see a threshold voltage shift, V_T, caused by the Q_{ot}. The process of neutralization is performed in three-step [5], in which curve is moved to curve (3) and then be aligned with the fresh one, curve (1).
3. Simultaneously, I_{CP}'s are measured as in Fig. 2.10, the difference between curve (1) and (3) gives the value of N_{it}, while the difference between (2) and (3) gives the value of Q_{ot}.
4. A local $V_T(x)$ is calculated, following [1] and [2], and from Eq.(2.13) in Table 2.1, calculation of $N_{it}(x)$ and $Q_{ot}(x)$ is completed.

2.4 The Improvement of GIDL Current Measurement

2.4.1 Experiment Setup of GIDL Current Measurement



(a)



(b)

Fig. 2.7 Calculated $\Delta L_0 \approx 0.04\mu m$ (a) nMOSFET, (b) pMOSFET in this work.

$$\Delta I_{CP} = qfW \int_0^x N_{it}(x)dx \qquad (2.11)$$

$$N_{it} = \frac{1}{qfW} \frac{d\Delta I_{CP}}{dV_{gl}} \frac{dV_{gl}}{dx} \qquad (2.12)$$

$$\frac{dV_{gl}}{dx} = \frac{dV_T(x)}{dx} \qquad (2.13)$$

$$N_{ot}(x) = Q_{ot}(x)/q = \frac{C_{ox}\Delta V_G}{q} \qquad (2.14)$$

Table 2.1 Equations used to calculate the distributions of N_{it} and N_{ot}.

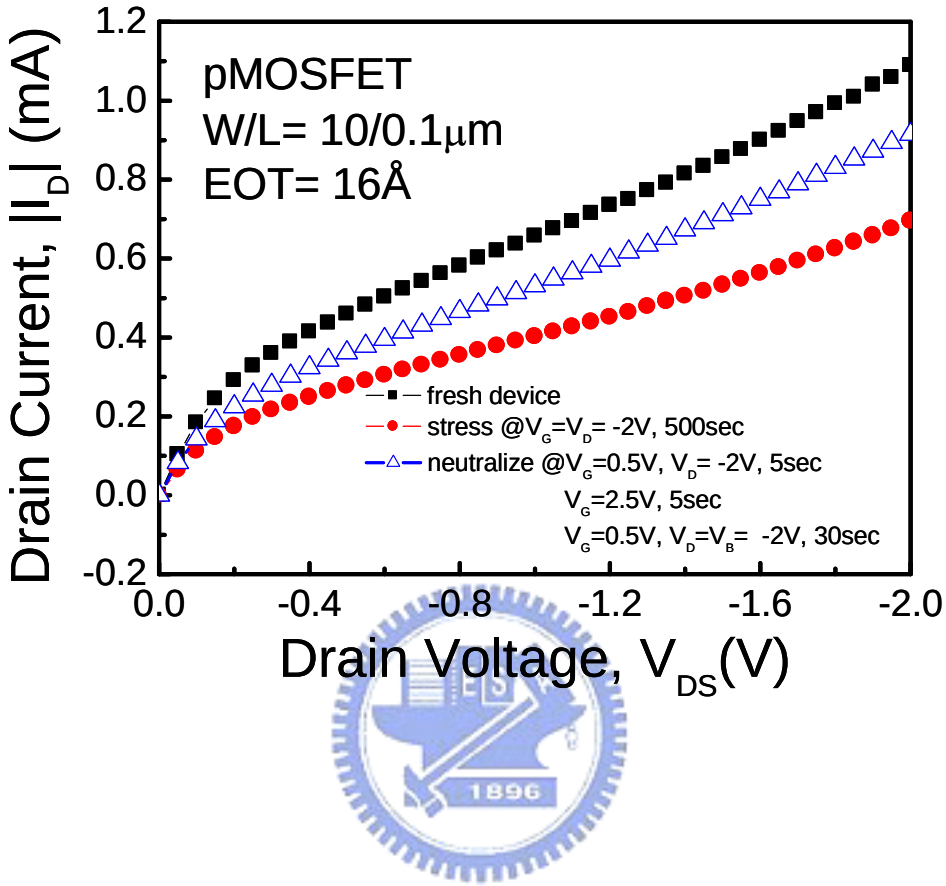


Fig. 2.8 Measured I_D currents for a fresh(1), stressed(2), and after neutralization(3) under V_G=V_D stress

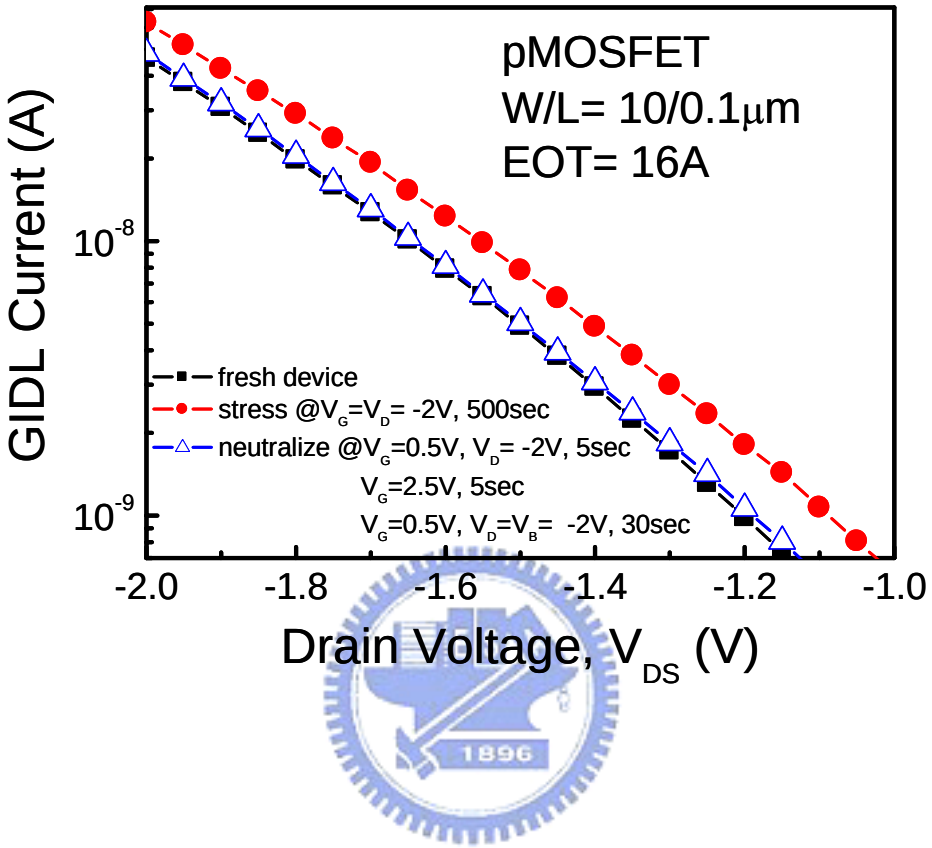


Fig. 2.9 Measured GIDL currents for fresh, stressed(2), and after neutralization(3). Note that hole trap is eliminated in the neutralized step.

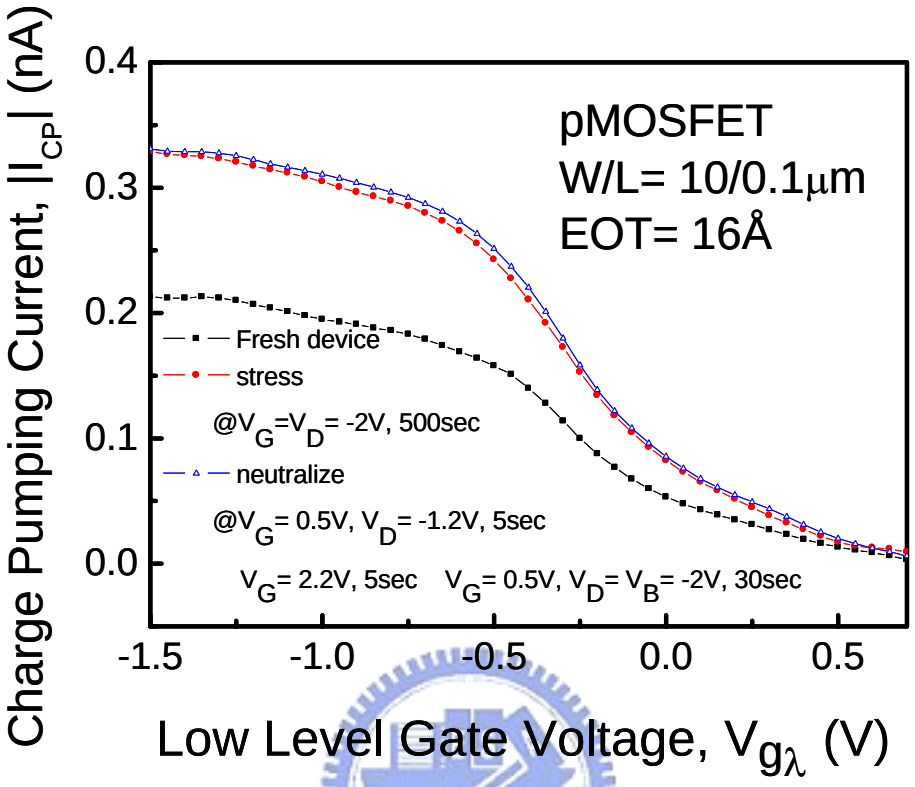


Fig 2.10 Measured I_{CP}-curve(1) fresh, curve(2) stressed. Curve(3) after neutralization.

As shown in Figs. 2.11 (a) and (b), we give the measurement range of V_G in the accumulation region, V_S floating, V_D= 1.5V (-1.5V) and V_B ground for NMOSFET (pMOSFET). We extract the drain current I_D for GIDL current.

2.4.2 Removing Tunneling Current from GIDL Current

As aforementioned, we monitor the GIDL current to observe the generated Q_{ot} and its annihilation by a three-step neutralization. However, the amount of gate to drain FN tunneling current can not be ignored during the bias condition of GIDL measurement. Therefore, the drain current I_D is not applied for monitoring GIDL current. Instead, we use the base current $I_{B,GIDL}$ for monitoring. As shown in Figs. 2.11 (a) and (b), the reason we choose $I_{B,GIDL}$ is that $|I_{B,leakage}| < |I_{FN}|$.

$$\text{GIDL current } (I_{D,GIDL}) = I_{B,total} - I_{FN}, \tag{2.14}$$

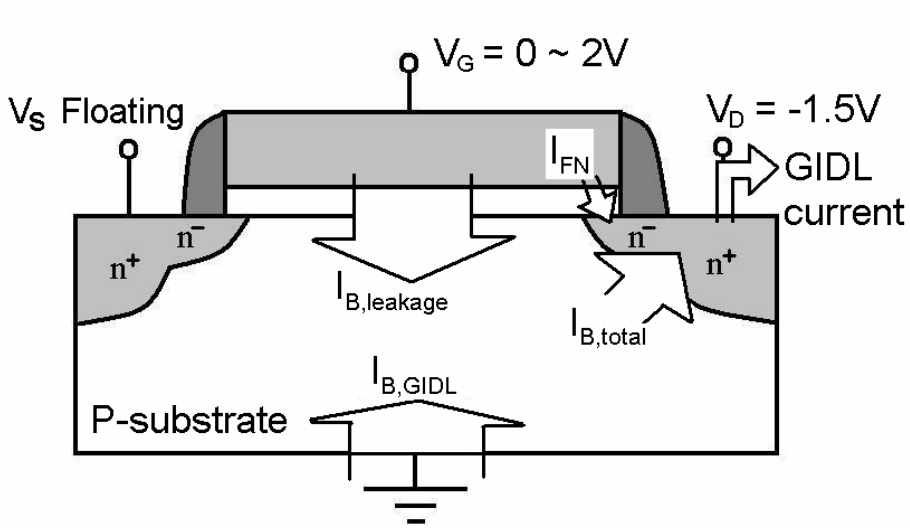
and

$$I_{B,GIDL} = I_{B,total} - I_{B,leakage}. \tag{2.15}$$

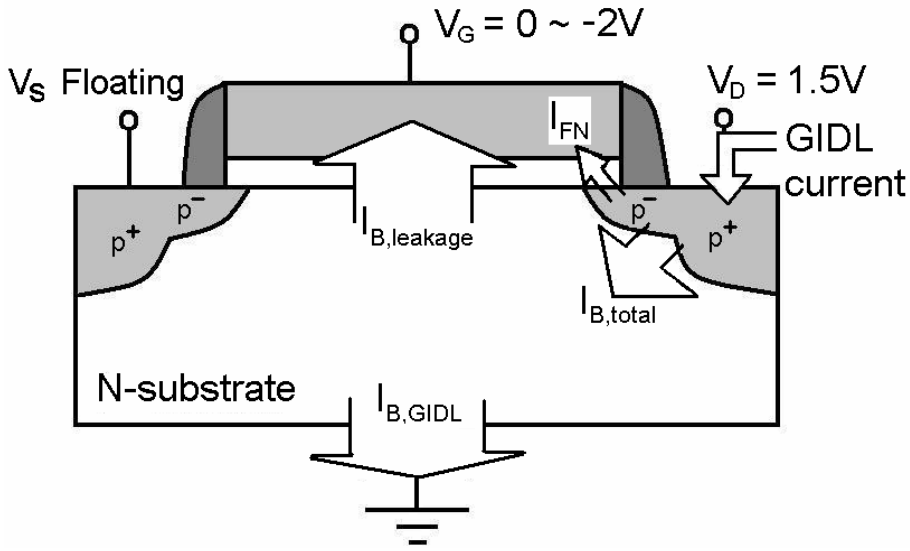
From Eqs. (2.14) and (2.15), we ensure that using $I_{B,GIDL}$ as a monitor is more suitable than $I_{D,GIDL}$ during the GIDL measurement of ultra-thin gate oxide.

2.5 Summary

In this chapter, experiment analysis methods have been described. In the later discussions, we will use these experimental techniques to discuss the lateral profiling of interface traps and oxide traps for CMOS device under HC stress and NBTI stress By using the IFCP method and the method of separating N_{it} and Q_{ot}, the degradation of CMOS device will also be studied.



(a)



(b)

Fig. 2.11 Experiment setup of GIDL current measurement.

(a) for nMOSFET, (b) for pMOSFET

Chapter 3
The Analysis of HC Reliability in Ultra Thin Gate Oxide CMOS Devices

3.1 Introduction

Reducing the size of MOSFET transistors enables high speed, lower power, denser and cheaper circuit, but introduces many challenges in process technology. As the gate oxide thickness is reduced, and as electric field in the MOSFET increase, there are increased concerns about hot carrier damage and dielectric breakdown. The hot carrier induced localized negative oxide charge in nMOSFET device, positive oxide charge in pMOSFET device and interface traps in CMOS device. This HC effect induced damage will be one of reliability problem of scaled ultra-thin gate MOSFET devices [9-10]. As the gate oxide reduce to the ultra-thin region, the direct tunneling current of gate oxide increase. Therefore, the leakage current will induce measurement error for ultra-thin gate oxide CMOS devices. For investigating HC induced damage correctly, we will eliminate the leakage current from the measurement by IFCP method. In addition, we use the three-step neutralization to separate interface traps and oxide traps which are induced by HC stress. Recombination of this two methods, we will get accuracy lateral profiling of interface traps and oxide traps under HC stress.

In this chapter, we first introduce device fabrication with different plasma nitrogen concentration and gate oxide thickness. Second, we will show the IFCP method and neutralization step to separate N_{it} and Q_{ot} for nMOSFET device. Subsequently, the stress bias dependence hot carrier induced degradation for nMOSFET including $I_{G,max}$ stress, $I_{B,max}$ stress, and $V_G = V_D$ stress will be investigated. We also discuss the plasma nitrogen concentration dependence and gate oxide thickness dependence of HC stress. Third, we discuss the HC stress result of pMOSFET like nMOSFET. Finally, we compare the result of hot carrier stress

in nMOSFET and pMOSFET device.

3.2 Device Fabrication

The devices which are used in this work were fabricated using 0.09μm CMOS technology. Test samples are nMOSFET and pMOSFET which have shallow S/D extension structure with gate oxide thickness of 14Å and 16Å, respectively. Furthermore, both of the gate oxide thickness have three different plasma nitrogen concentrations (see Table 3.1).

3.3 The Analysis of HC reliability in nMOSFET Devices

3.3.1 Lateral Profiling Steps of Interface/Oxide Traps

1. Figure 2. is the experiment setup for CP method. Here, we can find CP current with leakage current without correction. The IFCP method can eliminate the error of leakage current by using two different frequencies. From now on, the CP current measurement use IFCP method to get accuracy CP current without leakage current.
2. According to the CP current (Fig. 3.1(a)), we can get local threshold voltage distribution. We select the $I_{cp,max}$ at V_{gh}= 0.25V and then use the Eq. 3.1 to calculate the relation figure of x(the position of channel length) - V_t (local threshold voltage), as Fig. 3.1(b) .

$$x = \frac{L * I_{CP}(V_{gh})}{I_{CP,\max}} \tag{3.1}$$

3. To measure I_D-V_{DS}, GIDL, and I_{CP} for fresh, stress, and after neutralization, as Figs. 3.2, 3.3,and 3.4. To observe the GIDL, we can find the GIDL of stressed device shift to right due to negative charge inject to gate oxide. We have to use three

Tox		14Å	16Å
The concentration of plasma nitrogen	Low	PN1	PN1
	Medium	PN2	PN2
	High	PN3	PN3
W/L		10 μ m/0.09 μ m	

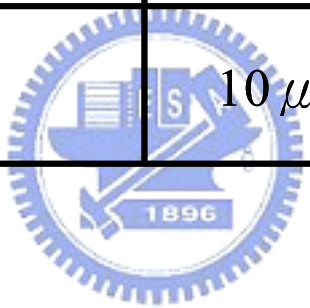
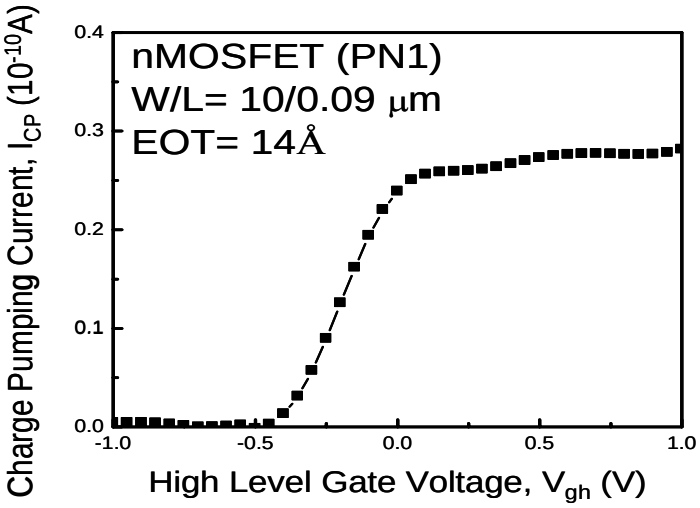
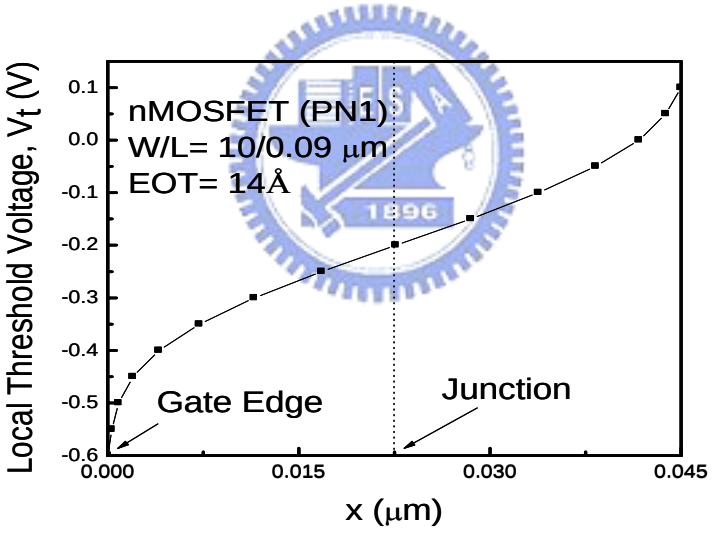


Table 3.1 The split condition of samples used in this work, in which device have three different concentration of plasma nitridation and two different gate oxide thickness.



(a)



(b)

Fig. 3.1 (a) Charge pumping current with correction for a fresh device .
(b) Local threshold voltage distribution for a fresh device.

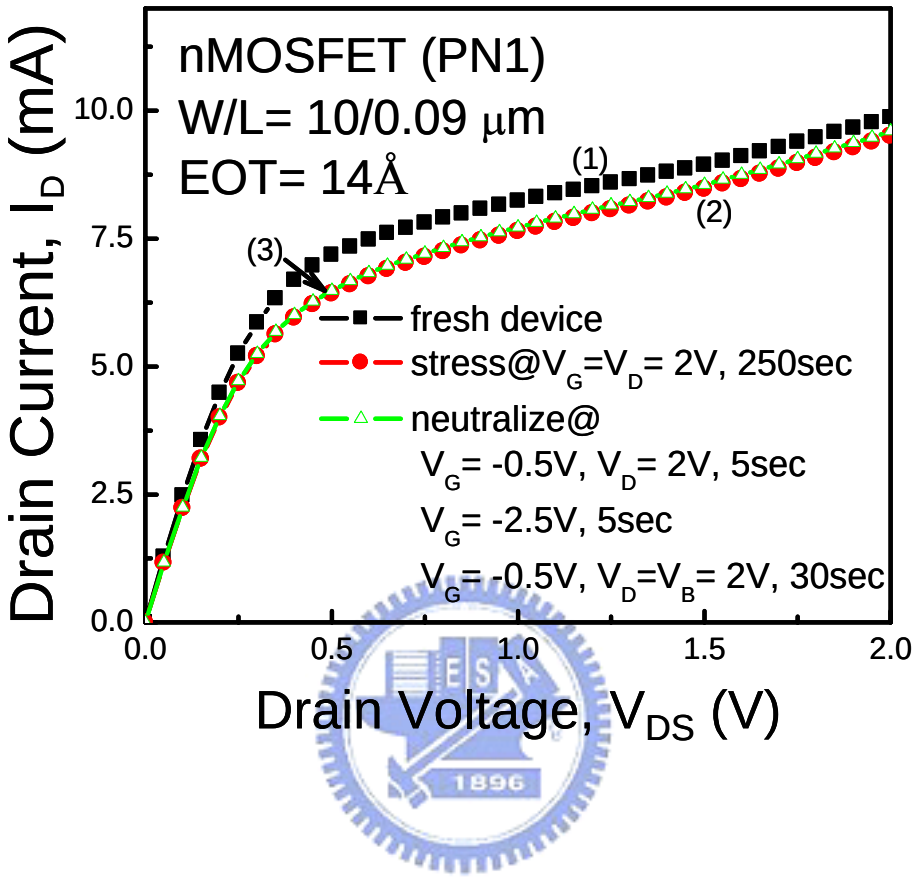


Fig. 3.2 Measured I_D current for fresh (1), stress (2),and after neutralization (3) under $V_D = V_G$ stress.

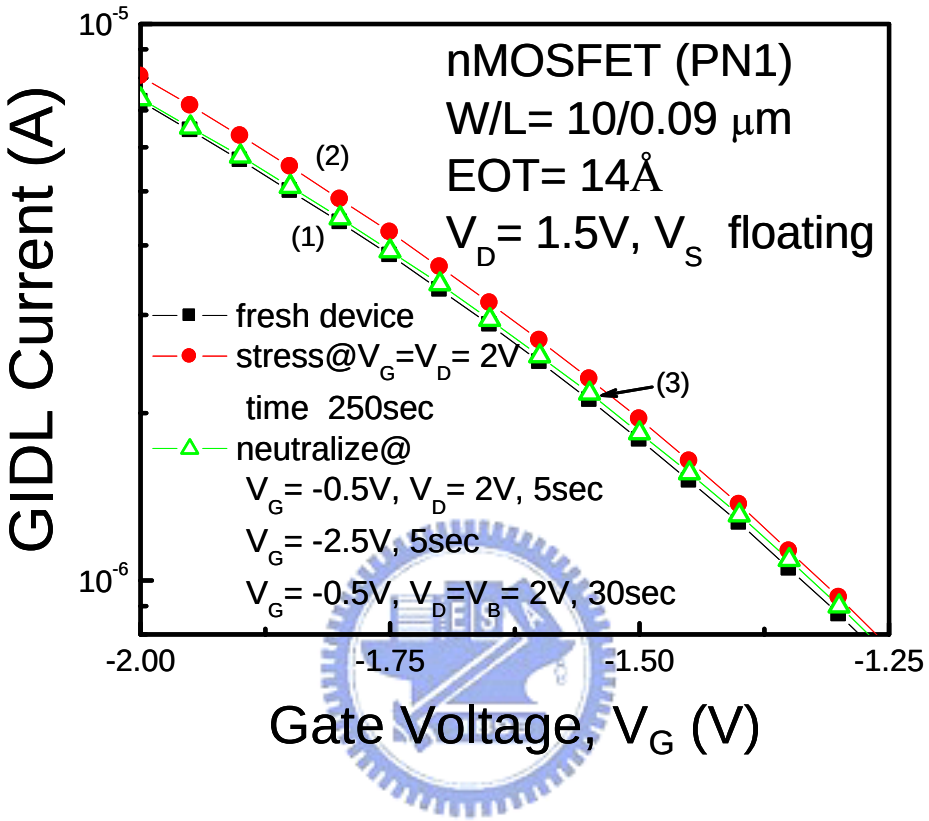


Fig. 3.3 Measured GIDL current for fresh (1), stress(2), and after neutralization (3). Note electron trap is eliminated in the neutralization step.

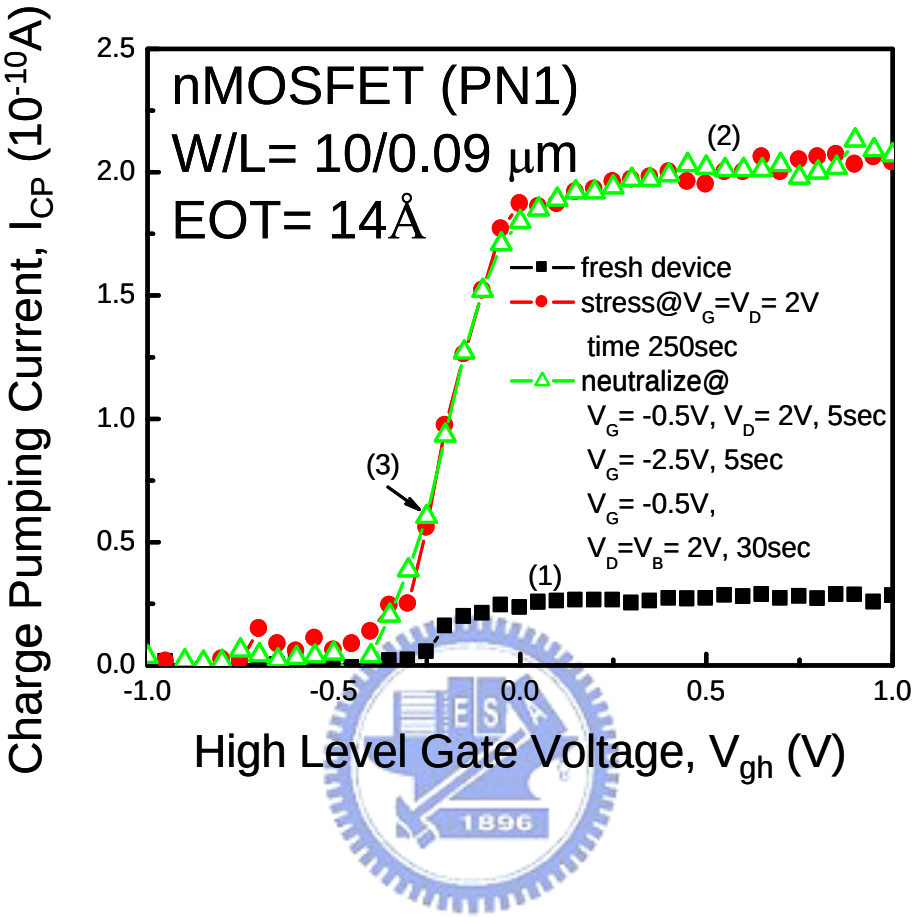


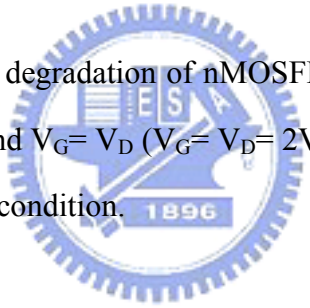
Fig. 3.4 Measured I_{CP} for fresh (1), stress (2), and after neutralization (3).

neutralization steps to separate interface/oxide traps. First, we inject positive charge from gate edge (V_G= -0.5V, V_D= 2V, time= 5sec). Second, we inject positive charge by FN tunneling under gate channel (V_G= -2.5V, time=5sec). Finally, we use the bias condition (V_G= -0.5, V_D=V_B= 2V, time= 30sec) for eliminating the electron trap completely. In Fig. 3.3, we see the GIDL shift back to fresh state.

4. At the same time, I_{CP} are measurement in Fig. 3.4 , the difference between curves (1) and (3) gives the ΔI_{CP}. In accordance with Eq. 2.12, we calculate the value of $d\Delta I_{CP}/dV_{gh}$ and dV_{gh}/dx to get the $N_{it}(x)$. On the side, the difference between curves (2) and (3) give the $Q_{ot}(x)$ by using Eq. 2.14 in Table 2.1.

3.3.2 I_D Degradation at Different Stress Bias

In Fig. 3.5, we measure I_D degradation of nMOSFET device at $I_{G,max}$ (V_G= 0.5V, V_D= 2V), $I_{B,max}$ (V_G= 1.4V, V_D= 2V), and V_G= V_D (V_G= V_D= 2V) stress condition. The maximum I_D degradation is at V_G= V_D stress condition.



The reason why V_G = V_D stress is the worst-case stress condition may be understood by considering the shape of the I_{SUB} versus V_G characteristic [11]. With a given technology, the I_{SUB} versus V_G curve becomes flatter, as the channel length is reduced. When the ratio of $I_{SUB|\ Ib,\ peak}$ to $I_{SUB|\ vg=vd}$ is smaller, the worst-case stress condition may switch from $I_{B,\ MAX}$ to V_G = V_D. This explanation of the cross over effect has been proposed by E. Rosenbaum et al. [11].

3.3.3 Experimental Results

We adopt the above method to separate N_{it} and Q_{ot} and then we get the lateral profiling

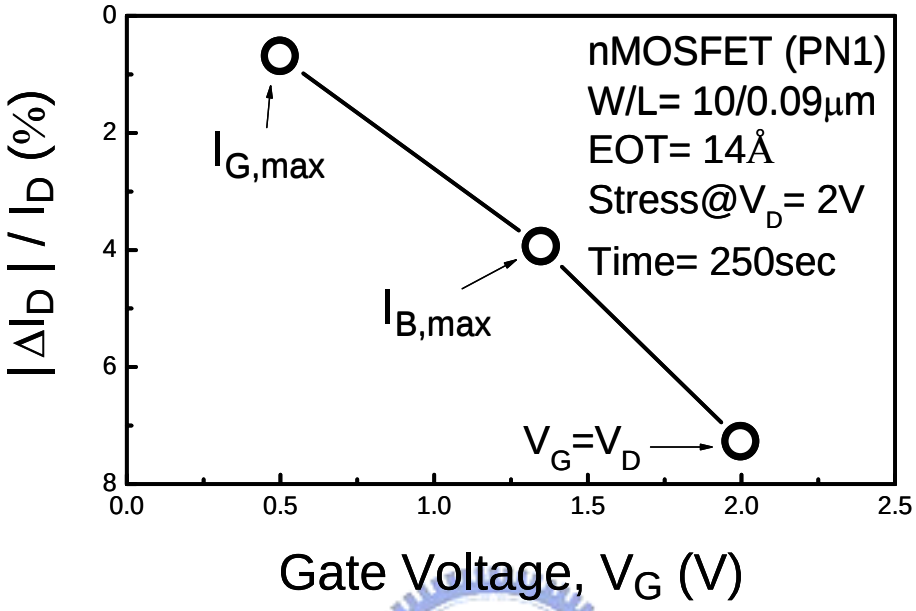


Fig. 3.5 (nMOSFET) Measured device I_D degradation at $I_{G,max}$, $I_{B,max}$, and $V_G=V_D$ stress condition.

of interface traps $N_{it}(x)$ and oxide traps $Q_{ot}(x)$, as Fig. 3.6. As Fig. 3.6 shown, we observe the greater part distribution of oxide traps at the region of gate-drain overlap and the distribution of interface traps under gate channel. To follow the precedent of Fig. 3.2, we discover that the I_D increase a little after neutralization step. This result indicates the effect of oxide traps to I_D degradation not dominant. In Fig. 3.2, the different between curves (1) and (3) is the effect of interface traps. Interface trap is the dominant effect to I_D degradation. Due to interface traps occupy the larger area under gate channel for dominate to I_D degradation, the I_D-V_{DS} result is consistent with lateral profiling of $N_{it}(x)$ and $Q_{ot}(x)$. Moreover, we compare of N_{it} distribution between $I_{B,max}$ and $V_G = V_D$ stress condition, as Fig. 3.7. We find the larger amount of interface traps under gate channel at $V_G = V_D$ stress condition. From the previous section, we know the $V_G = V_D$ stress condition have larger I_D degradation than $I_{B,max}$ stress condition. Hence, we can find the reason of larger I_D degradation at $V_G = V_D$ stress condition from $N_{it}(x)$.

3.3.4 The Dependency of Hot Electron Reliability on Plasma Nitridation

Table 3.2(a) show the comparison of $I_{D,sat}$ degradation and G_m degradation between the PN1 and the PN3 at the same gate oxide thickness (Tox= 16Å). We observe the PN1 sample is worse than PN3 sample after $V_G = V_D = 2V$ stress. As the Fig. 3.8 shown, the $N_{it}(x)$ of PN1 sample is larger than PN3 sample whether in gate channel or in overlap region. For the reason, we get a conclusion that the higher concentration of plasma nitridation is better to resist channel hot electron injection. In other words, higher concentration of plasma nitridation has better HC stress reliability for nMOSFET. This result is consistence with [12].

3.3.5 The Dependency of the Hot Electron Reliability on the Gate Oxide Thickness

At this experiment, we choose different gate oxide thickness (14Å and 16Å) device at the same concentration of plasma nitridation (PN1). We also compare the change of $I_{D,sat}$ and

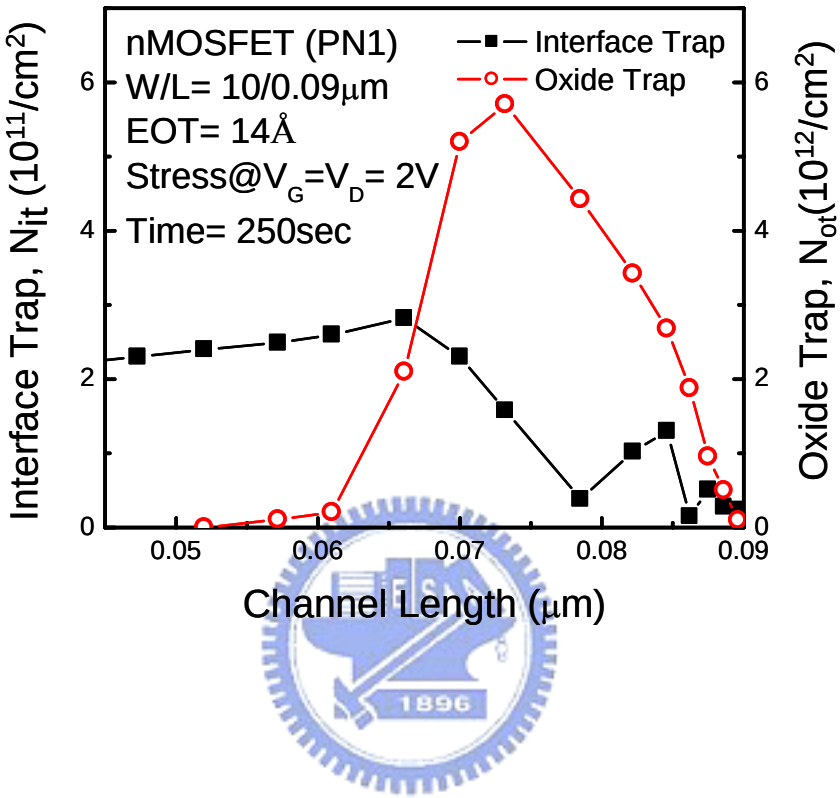


Fig. 3.6 Calculated lateral distribution of N_{it} and N_{ot} (= Q_{ot}/q) along the channel length under $V_G = V_D$ stress.

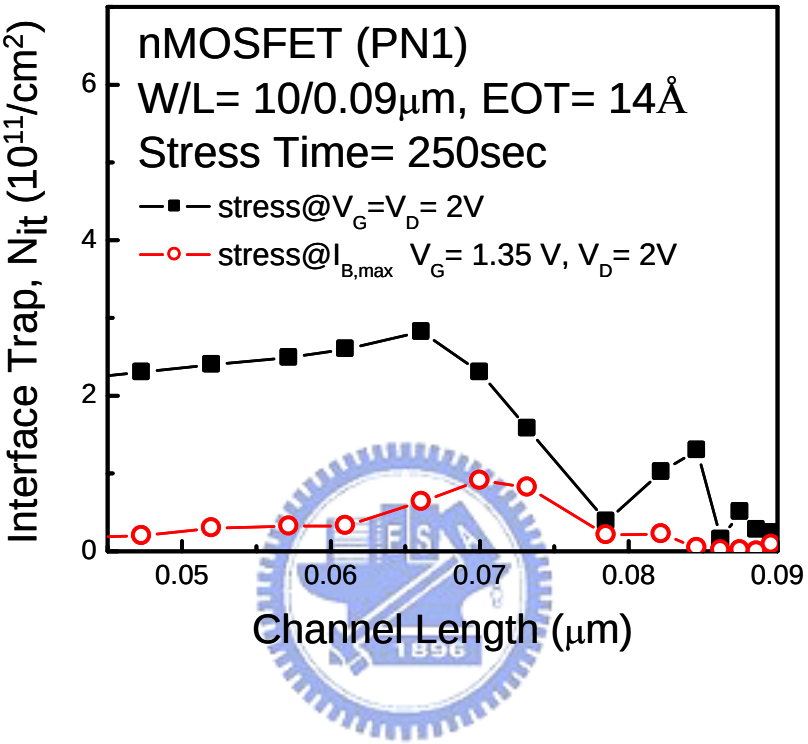


Fig. 3.7 Comparison of N_{it} distribution between $I_{B,max}$ and $V_G = V_D$ stress conditions. Note that $V_G = V_D$ has larger values of N_{it}.

Gate Oxide Thickness	16Å	
The Concentration of Plasma nitridation	PN1	PN3
$\lvert \Delta G_m \rvert / G_m$ (%)	17.9	15.2
$\lvert \Delta I_{D,sat} \rvert / I_{D,sat}$ (%)	10	9.5

(a)

The Concentration of Plasma nitridation	PN1	
Gate Oxide Thickness	14Å	16Å
$\lvert \Delta G_m \rvert / G_m$ (%)	14.5	17.9
$\lvert \Delta I_{D,sat} \rvert / I_{D,sat}$ (%)	7.3	10

(b)

Table 3.2 The $\Delta G_m/G_m$ and $\Delta I_{D,sat}/ I_{D,sat}$ of nMOSFET under $V_G=V_D=$ 2V stress.
(a)The comparison with different concentrations of plasma nitridation.
(b)The comparison with different gate oxide thicknesses.

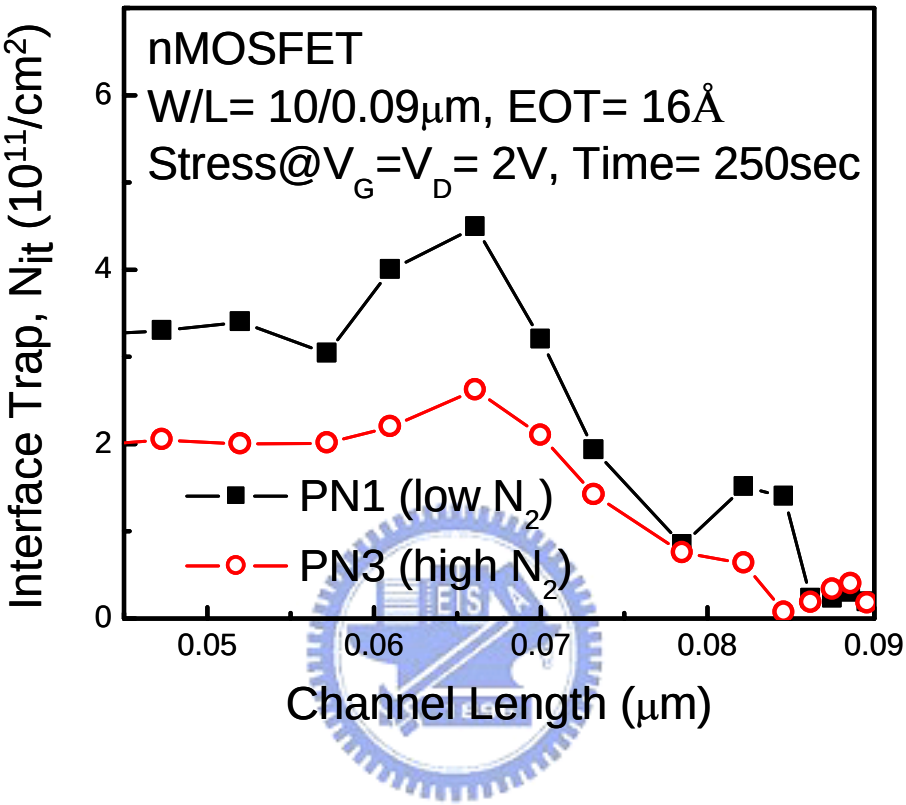


Fig. 3.8 Comparison of the generate N_{it} for two different plasma nitrided samples, where PN3 reliability has been improved with a high plasma density and N_2 content close to poly-Si.

G_m between the two sample after hot electron stress. (Table 3.2(b)) We find the thicker sample has worse case after stress. This result is consistence with lateral profiling of two different gate oxide thickness. The thicker sample (16Å) has larger area of N_{it} than thinner sample (14Å) so that it has worse hot electron reliability. We think the N_{it} at p-sub at fresh device is donor type interface trap, so above the quasi fermi level E_{fp}, the polarity of N_{it} is positive. In Fig. 3.9, we find thinner sample (14Å) has less N_{it} than thicker sample (16Å) at fresh device condition. So, we think the N_{it} of thinner sample (14Å) provide less attractive force to channel hot electron injection cause less ΔN_{it} after stress. According to the reason, we think the N_{it} of fresh device will affect the amount of hot electron injection for nMOSFET device.

3.4 The analysis of HC Reliability in pMOSFET device

3.4.1 Lateral Profiling Steps of Interface/Oxide Traps

1. Figure 2. is the experiment setup for CP method. Here, we use the similar step in 3.3.1 for nMOSFET. The IFCP method can eliminate the error of leakage current by using two different frequencies. From now on, the CP current measurement use IFCP method to get accuracy CP current without leakage current.
2. According to the CP current (Fig. 3.10(a)), we can get local threshold voltage distribution. We select the $I_{cp,max}$ at V_{gl}= -0.3V and then use the Eq. 3.2 to calculate the relation figure of x(the position of channel length) - V_t (threshold voltage), as Fig. 3.10(b).

$$x = \frac{L * I_{CP}(V_{gl})}{I_{CP,\max}} \tag{3.2}$$

3. To measure I_D-V_{DS}, GIDL, and I_{CP} for fresh, stress, and after neutralization, as Figs. 3.11 and 3.12. To observe the GIDL, we can find the GIDL of stressed device shift to

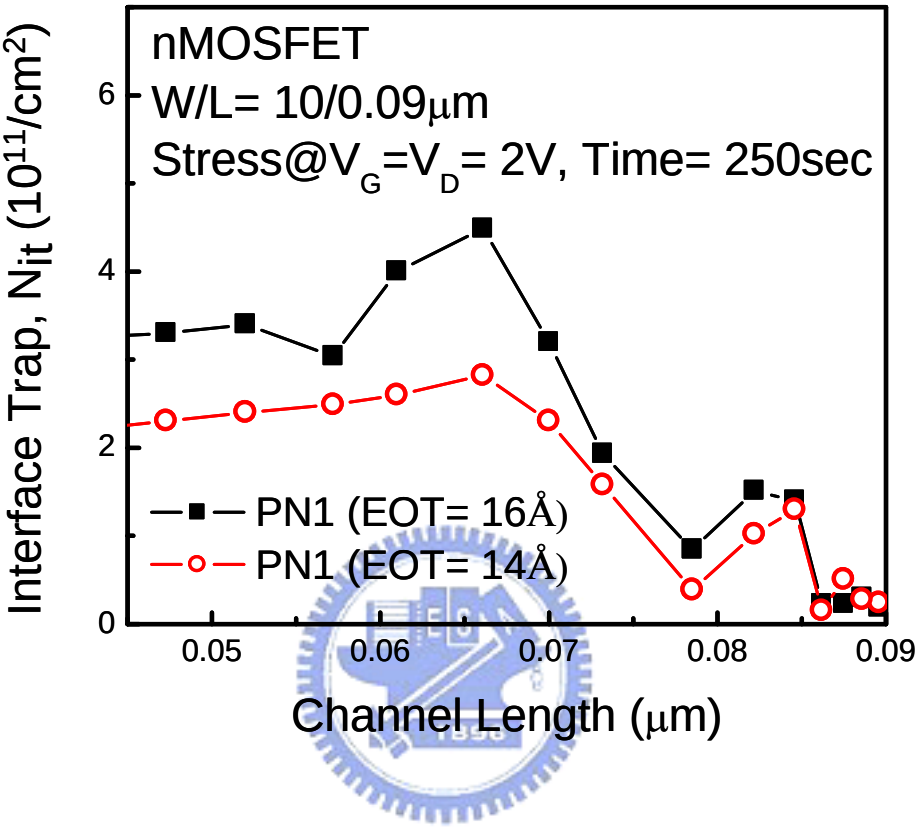
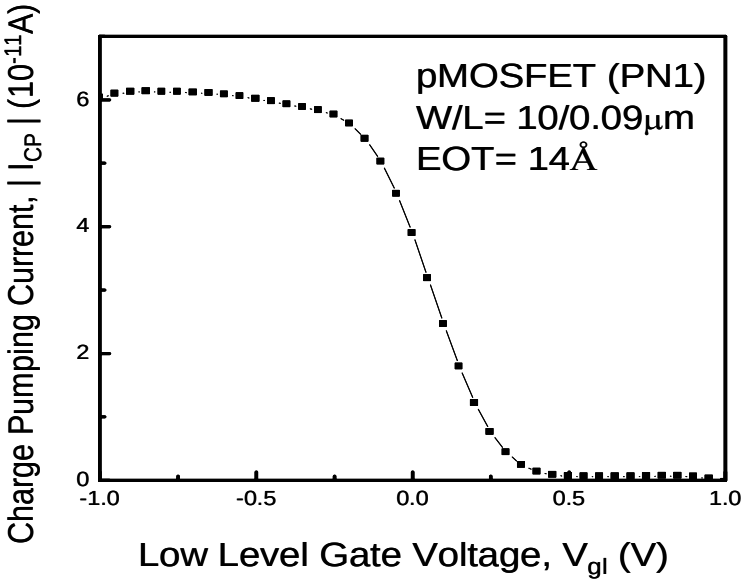
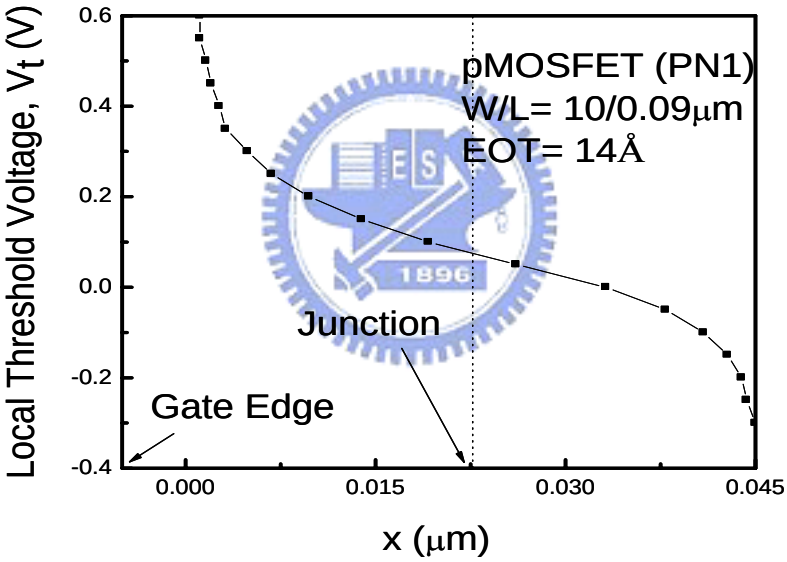


Fig. 3.9 Comparison of the generated N_{it} for two different gate oxide thickness, where thinner oxide shows better reliability.



(a)



(b)

Fig. 3.10 (a) Charge pumping current with correction at fresh device .

(b) Local threshold voltage distribution at fresh device

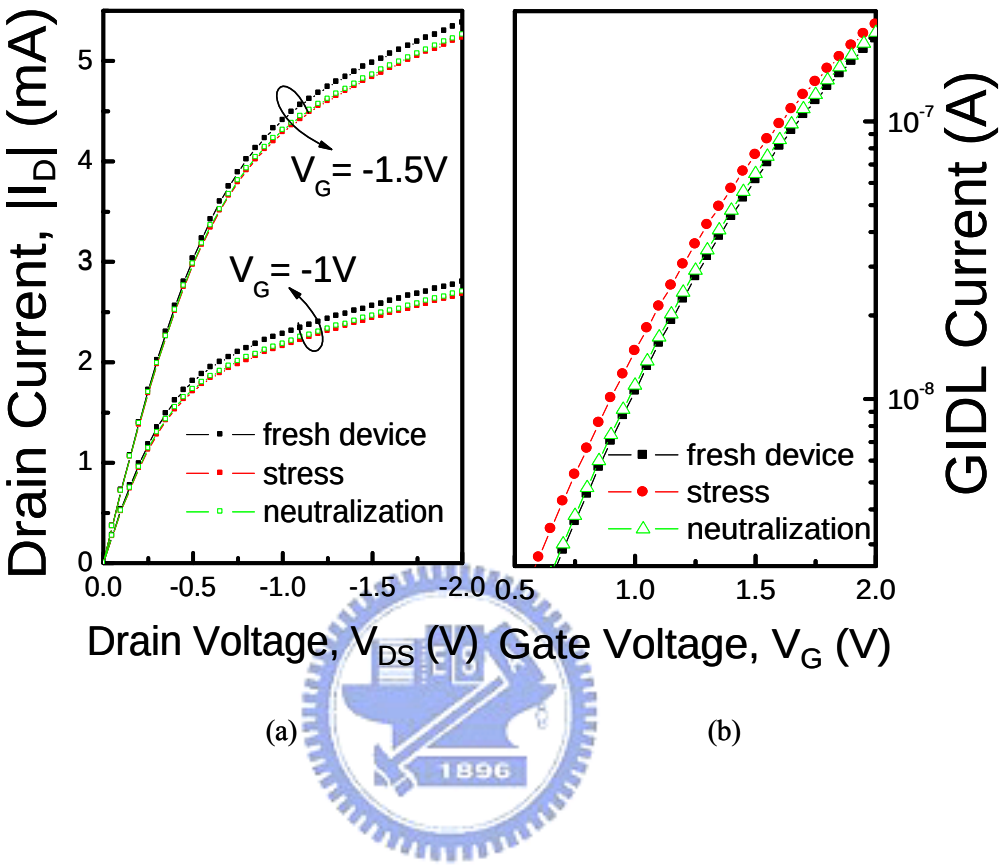


Fig. 3.11 (a) Drain Currents for fresh, stressed, and after neutralization. N_{it} is dominant from these curves.

(b) The neutralization procedure is similar to Fig. 3.3.

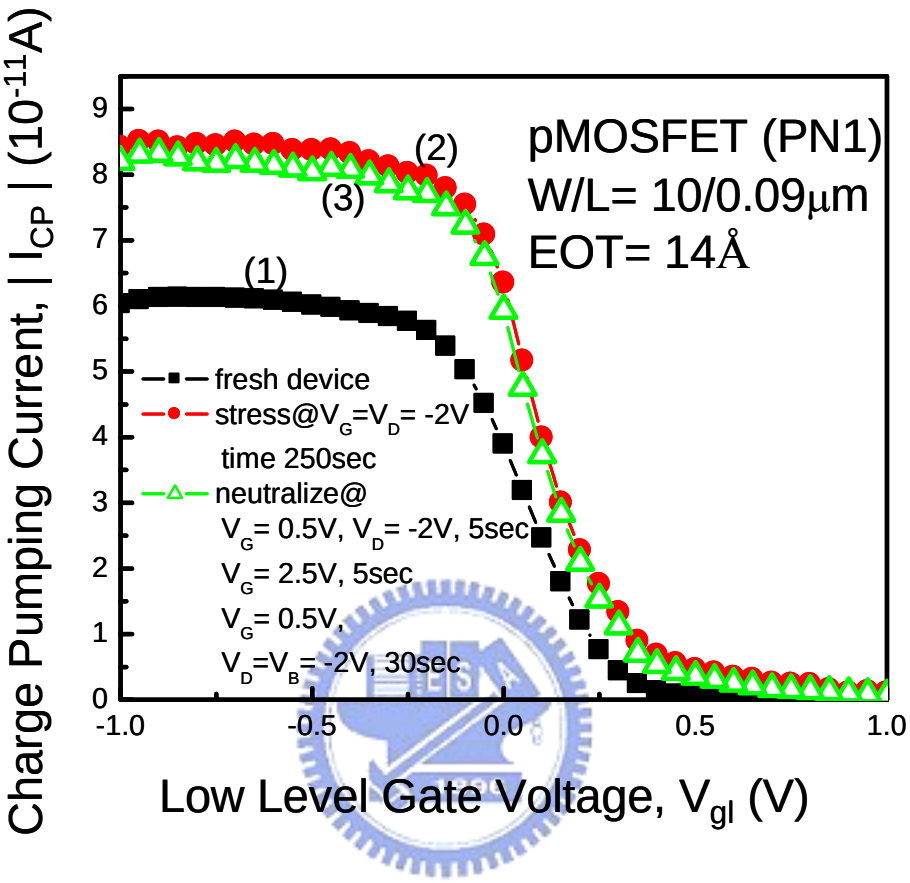


Fig. 3.12 Measured I_{CP} for fresh (1), stress (2), and after neutralization(3).

left due to positive charge inject to gate oxide. We have to use three neutralization steps to separate interface/oxide traps. First, we inject negative charge from gate edge (V_G= 0.5V, V_D= -2V, time= 5sec). Second, we inject negative charge by FN tunneling under gate channel (V_G= 2.5V, time=5sec). Finally, we use the bias condition (V_G= 0.5, V_D=V_B= -2V, time= 30sec) for eliminating the hole trap completely. In Fig. 3.11(b), we see the GIDL shift back to fresh state.

4. At the same time, I_{CP} are measurement in Fig. 3.12, the difference between curves (1) and (3) gives the ΔI_{CP}. In accordance with Eq. 2.12, we calculate the value of $d\Delta I_{CP}/dV_{gl}$ and dV_{gl}/dx to get the $N_{it}(x)$. On the side, the difference between curves (2) and (3) give the $Q_{ot}(x)$ by using Eq. 2.14 in Table 2.1.

3.4.2 I_D Degradation at Different Stress Bias

In Fig. 3.13, we measure I_D degradation of pMOSFET device at $I_{G,max}$ (V_G= -0.5V, V_D= -2V), $I_{B,max}$ (V_G= -0.8V, V_D= -2V), and V_G= V_D (V_G= V_D= -2V) stress condition. The maximum I_D degradation is at V_G= V_D stress condition. Except for V_G= V_D stress condition, we can find I_D hardly unchanged at the others stress condition.

From the comparison of $I_{B,max}$ and V_G= V_D stress, we can see that the most degradation occurs at V_G= V_D. This is consistent with nMOSFET as above.

3.4.3 Experiment Result

Using the above method to separate N_{it} and Q_{ot} , we can obtain the lateral profiling of interface traps $N_{it}(x)$ and oxide traps $Q_{ot}(x)$, as in Fig. 3.14. Here, we observe that a larger portion of the distribution of oxide traps in the region of gate-drain overlap and the

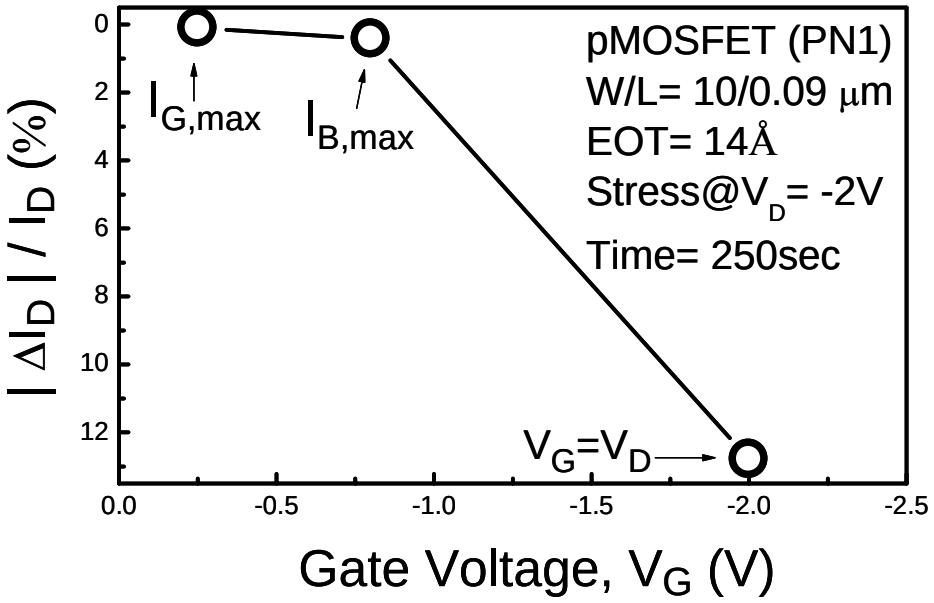


Fig. 3.13 (pMOSFET) Measured device I_D degradation at $I_{G,max}$, $I_{B,max}$, and $V_G=V_D$ stress condition.

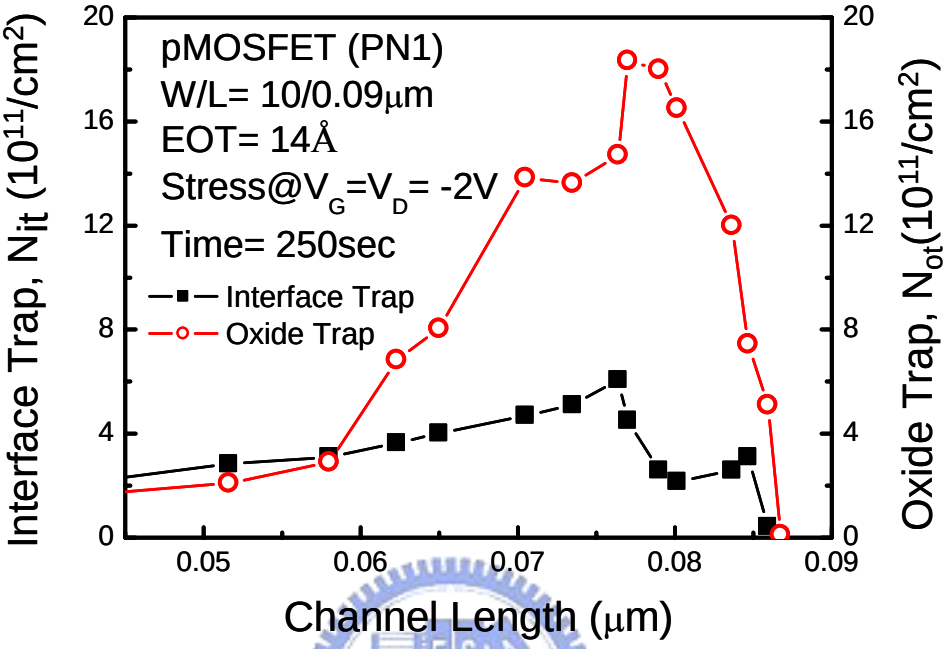


Fig. 3.14 Calculated lateral distribution of N_{it} and N_{ot} (= Q_{ot}/q) along the channel length under $V_G = V_D$ stress.

distribution of interface traps under gate channel. To follow the precedent of Fig. 3.11(a), we discover that the I_D increases a little after the neutralization step. This result indicates the effect of oxide traps to I_D degradation is not dominant. In Fig. 3.11(a), the different between curves (1) and (3) is the effect of interface traps. Interface trap is the dominant factor of I_D degradation. Since interface traps occupy a larger area in the gate channel which dominates the I_D degradation, the I_D-V_{DS} result is consistent with lateral profiling of $N_{it}(x)$ and $Q_{ot}(x)$. Moreover, we compare of N_{it} distribution between $I_{B,max}$ and $V_G = V_D$ stress condition, as Fig. 3.15. We found that a larger amount of interface traps under gate channel at $V_G = V_D$ stress condition. From the previous section, we know the $V_G = V_D$ stress condition have larger I_D degradation than $I_{B,max}$ stress condition. Hence, we can find the reason why larger I_D degradation occurs at $V_G = V_D$ stress condition from $N_{it}(x)$.

3.4.4 The Dependency of Hot Hole Reliability on Plasma Nitridation

Table 3.3(a) shows the comparison of $I_{D,sat}$ degradation and G_m degradation between the PN1 and the PN3 at the same gate oxide thickness (Tox= 16Å). We observe the PN3 sample is worse than PN1 sample after $V_G = V_D = -2V$ stress. As Fig. 3.16 shows, the $N_{it}(x)$ of PN3 sample is larger than that of PN1 sample either in gate channel or in overlap region. For the reason, we have a conclusion that the higher concentration of plasma nitridation is worse to resist the channel hot hole injection. In other words, higher concentration of plasma nitridation has worse HC stress reliability for pMOSFET. This result is consistence with [12]. We think it might be acceptor type interface trap at n-sub and if the interface traps are under the quasi fermi level E_{fn}, the polarity of N_{it} are negative can attract hot hole injection. Since PN3 has higher amount of N_{it}, PN3 has higher attractive force for hot hole injection during the stress and leads to more damage, as shown in the experimental result in Fig. 3.16.

3.4.5 The Dependency of Hot Hole Reliability on the Gate Oxide Thickness

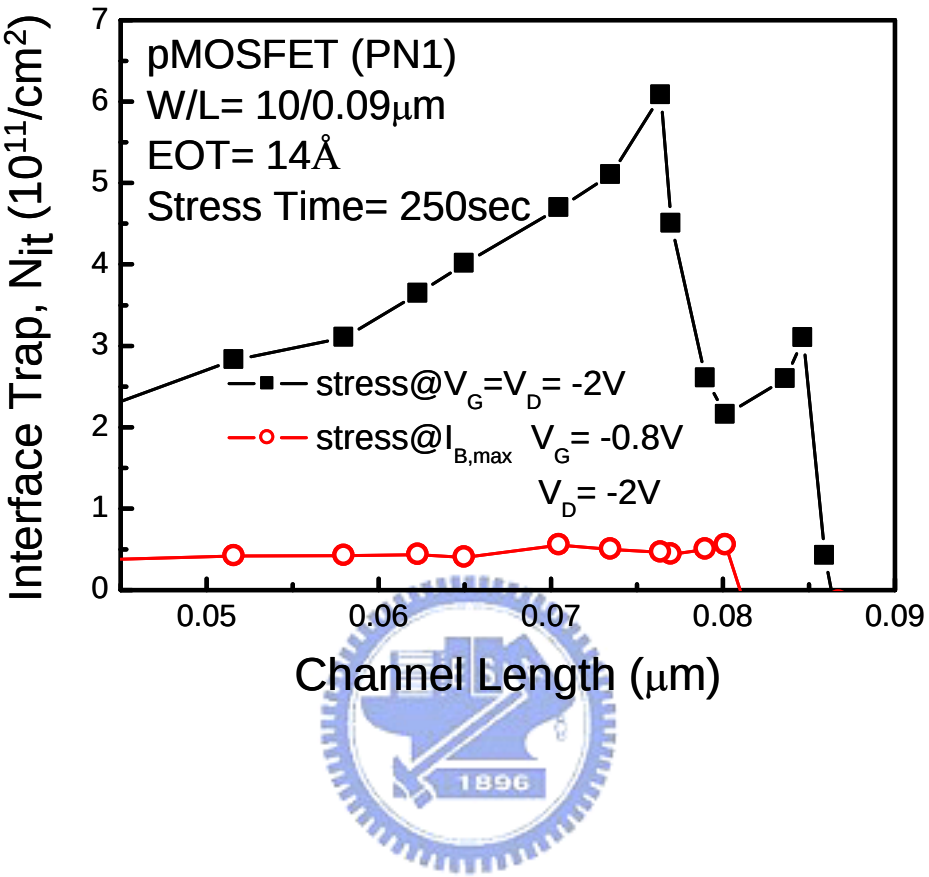


Fig. 3.15 Comparison of N_{it} distribution between $I_{B,max}$ and $V_G = V_D$ stress conditions. Note that $V_G = V_D$ has larger values of N_{it} .

Gate Oxide Thickness	16Å	
The Concentration of Plasma nitridation	PN1	PN3
$\lvert \Delta G_m \rvert / G_m$ (%)	1.8	2.5
$\lvert \Delta I_{D,sat} \rvert / I_{D,sat}$ (%)	10.7	12.3

(a)

The Concentration of Plasma nitridation	PN1	
Gate Oxide Thickness	14Å	16Å
$\lvert \Delta G_m \rvert / G_m$ (%)	2.6	1.8
$\lvert \Delta I_{D,sat} \rvert / I_{D,sat}$ (%)	13.1	10.7

(b)

Table 3.3 The $\Delta G_m/G_m$ and $\Delta I_{D,sat}/ I_{D,sat}$ of pMOSFET under $V_G=V_D= -2V$ stress.
(a)The comparison with different concentrations of plasma nitridation.
(b)The comparison with different gate oxide thicknesses.

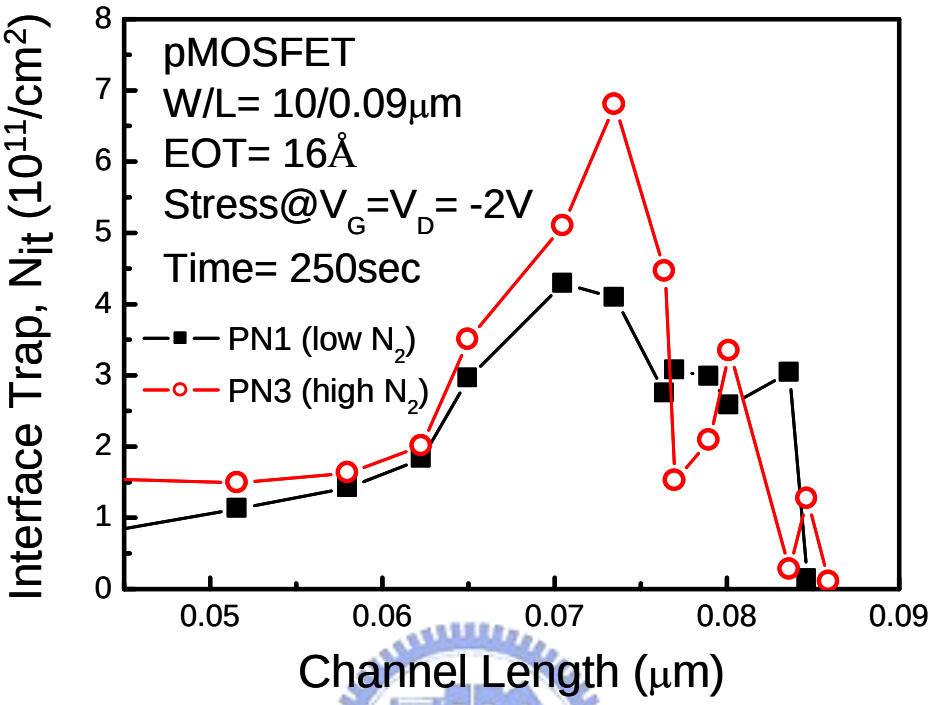


Fig. 3.16 Comparison of the generate N_{it} for two different plasma nitrided samples, where PN1 reliability has been improved with a lower plasma density and lower N_2 content.

In this experiment, we choose different gate oxide thickness (14Å and 16Å) device at the same concentration of plasma nitridation (PN1). We also compare the change of $I_{D,sat}$ and G_m between the two sample after hot electron stress (Table 3.3(b)). We find the thicker sample has worse case after stress. This result is consistent with lateral profiling of two different gate oxide thickness. The thinner sample (14Å) has larger area of N_{it} than thicker sample (16Å) so that it has worse hot hole reliability. We think the N_{it} at p-sub at fresh device is acceptor type interface trap, so above the quasi fermi level E_{fp}, the polarity of N_{it} is negative. In Fig. 3.17, we find thinner sample (14Å) has more N_{it} than thicker sample (16Å) at fresh device condition. So, we think the N_{it} of thinner sample (14Å) provide more attractive force to channel hot electron injection cause more ΔN_{it} after stress. According to the reason, we think the N_{it} of fresh device will affect the amount of hot hole injection for pMOSFET device.

3.5 Summary

In this chapter, we combine IFCP method and neutralization steps to obtain lateral profiling of interface/oxide traps. The IFCP method improves traditional charge pumping measurement by eliminating direct tunneling leakage current. On the side, three steps of neutralization successfully separate N_{it} and Q_{ot} in accordance with GIDL current measurement.

In both of nMOSFET and pMOSFET, we find the interface traps cause the dominant I_D degradation at $V_G = V_D$ stress condition and the worst I_D degradation is at $V_G = V_D$ stress condition.

For the comparison of plasma nitridation with different concentrations, we find PN3 sample has better hot electron reliability for nMOSFET device and PN1 sample has better hot hole reliability for pMOSFET device. For the comparison of different gate oxide thickness, we find thinner sample (14Å) has better hot electron reliability for nMOSFET and thicker sample

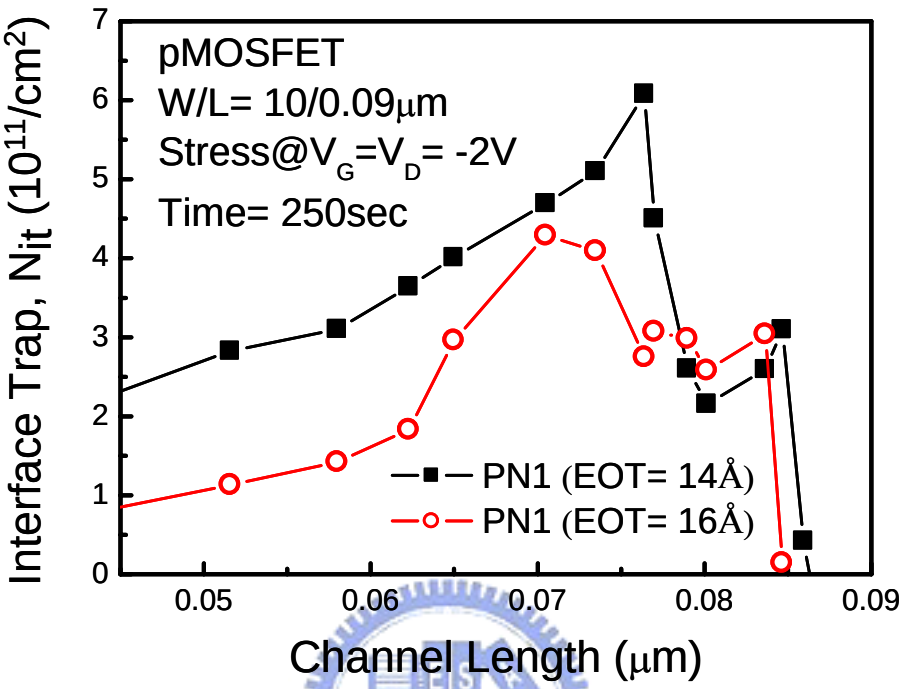


Fig. 3.17 Comparison of the generated N_{it} for two different gate oxide thickness, where thicker oxide shows better reliability.

(16Å) has better hot hole reliability.

According to the result of experiment, we think the polarity of interface trap will affect the amount of hot carrier damage the device. In nMOSFET, we think higher N_{it} at fresh device is donor type can attract hot electron injection to induce more ΔN_{it} . In contrast to pMOSFET, we think N_{it} at fresh device is acceptor type which can attract hot hole similar to nMOSFET.

Chapter 4

The Analysis of NBTI Degradation in pMOSFET

4.1 Introduction

In order to improve the electrical properties and reliability of ultra-thin gate dielectric films for MOS devices, intensive studies have been made. Nitrogen incorporation is one of the promising way to modify a silicon dioxide film. However, it has been found to significantly increase the device degradation such as negative-bias temperature instability (NBTI) of a pMOSFET device [13]. In NBTI, a threshold voltage shift and a transconductance degradation are caused by negative bias of the gate at high temperature. These stresses generate interface trap and positive fixed oxide charges in the Si/dielectric interface. NBTI is expected to be enhanced by the incorporation of nitrogen into gate oxide [13] and N_{it} will increase with increase in nitrogen concentration in the gate oxide [13].

In chapter 3, we have already used the new method to investigate the hot carrier degradation. In this chapter, we will also use the method to investigate the NBTI degradation and the NBTI enhanced HC effect. The NBTI effect arises at high temperatures under the influence of small negative voltages on the gate of p-channel transistors. The effect seen is a shift in the threshold of the transistor to more negative gate voltages, and a decrease in the $I_{D,sat}$ curve due to an increase in the amount of positive oxide charge, as well as an increase in interface state densities [14-15].

It was found that the hot carrier stress damage at $V_G = V_D$ stress increases as temperature increases, contrary to conventional hot carrier induced degradation. Finally, we further investigate the correlation of the CHC and NBTI contributions to the device damage.

4.2 NBTI Degradation in PMOSFET

4.2.1 The Devices Under Test

In this section, we use the devices with gate oxide thickness (EOT= 14Å) to investigate the NBTI and NBTI-like characteristics under different concentrations of plasma nitridation (PN1, PN2, and PN3), as in Table 3.1.

4.2.2 NBTI Degradation

First, we stress on pMOSFET with V_G= -2V at 100^{o}C for 250 seconds. After finishing the stress process for different three samples, we use the method of lateral profiling of interface trap, as described in chapter 2. We can draw the distribution of interface trap along the direction of gate channel. As reveals in Fig. 4.1, we observe the concentration dependence of NBTI effect. The amount of N_{it} increases along with increasing the concentration of plasma nitridation. The PN3 sample, i.e., the largest plasma density has the largest value of interface trap. We can find the worst-case degradation occurs near the drain junction region.

The degradation near the gate edge is caused by the locally enhanced degradation reactions between the holes and oxide defects, since the region of gate edge and gate-S/D overlap have a higher concentration of holes. In addition, during device processing, there are many initial oxide defects as induced by gate etching and S/D ion implantation. Because the number of holes and initial oxide defects are higher near gate edge, the N_{it} has a higher value for three samples locally in these regions.

For longer-channel pMOSFET, local degradation does not greatly affect device characteristics. In contrast, for shorter-channel devices, this local degradation affects the device characteristics significantly, and results in a larger NBTI degradation.

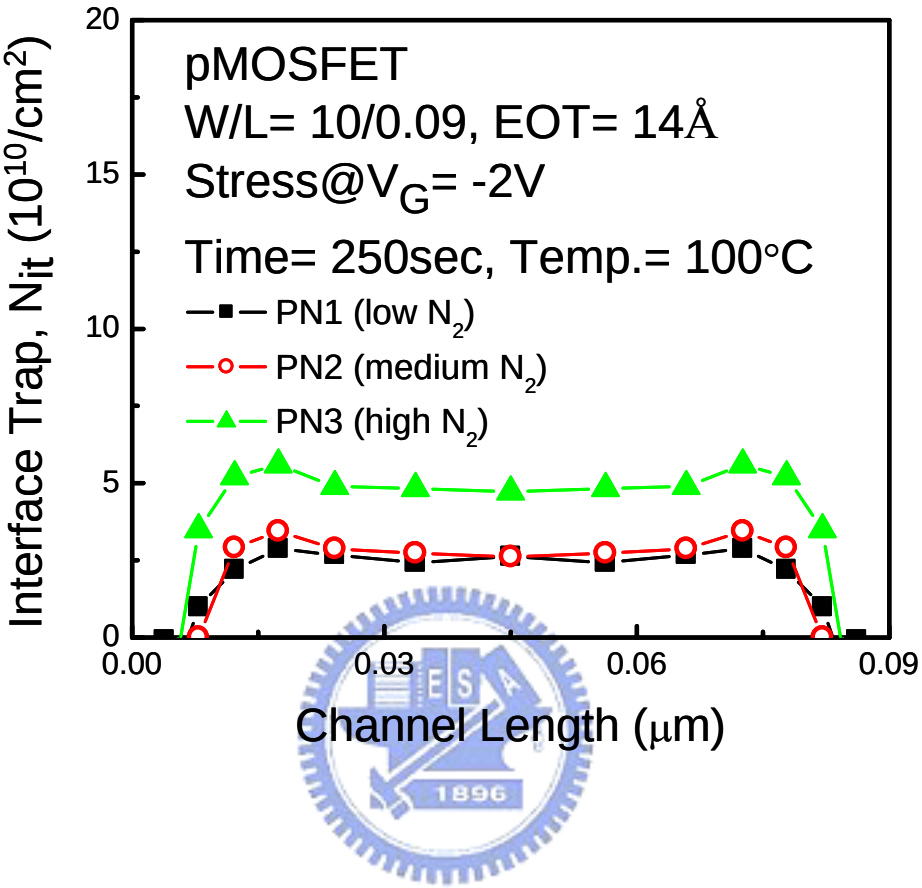


Fig. 4.1 Symmetrical NBTI stress where D and S are grounded and V_G= - 2V, stressed at T= 100°C. The N_{it} distribution with a double-hump can be seen at both the S/D side.

4.2.3 NBTI-like Degradation

In this section, we stress the pMOSFET under NBTI-like condition (V_G= V_D= -2V, Temp.= 100^{o}C) for 250 seconds. We may expect the damage of NBTI-like include with NBTI effect and HC effect. From the lateral profiling of interface trap of three different samples, as shown in Fig. 4.2, we can observe the amount of N_{it} under NBTI-like stress condition is far larger than NBTI stress condition. Furthermore, the peak value of N_{it} go toward gate-S/D overlap region from junction. From Fig. 4.2, we make comparisons for devices with different concentrations of plasma nitridation. We can find the PN3 sample has a worst case degradation after NBTI-like stress which is similar to the result of previous section. Plasma nitrogen density affects pMOSFET reliability indeed.

As shown in Figs. 4.3, 4.4, and 4.5, it shows the comparison of interface trap and oxide trap respectively. We can find the peak of oxide trap is close to the gate edge and the amount of oxide trap is almost located at gate-S/D overlap region. Moreover, we may find the plasma density independence of value of oxide trap and the interface trap is dominant of the degradation in pMOSFET owing to N_{it} is larger than Q_{ot} at the position of gate channel. Also a summarized device degradation region under the NBTI and NBTI-like stresses, is given in Fig. 4.6.

4.3 Summary

In this chapter, we use the IFCP method and the neutralization method to obtain the lateral profiling of N_{it} and Q_{ot} after various stress conditions. We have investigated the degradation of NBTI and NBTI-like degradation from the distribution of N_{it} and Q_{ot}. We can find that the PN3 is the worst case either under NBTI or NBTI-like stress condition. Therefore, we conclude that the amount of N_{it} increase with the plasma nitrogen density after NBTI and NBTI-like stress. In addition, the results of NBTI degradation show that most of the oxide

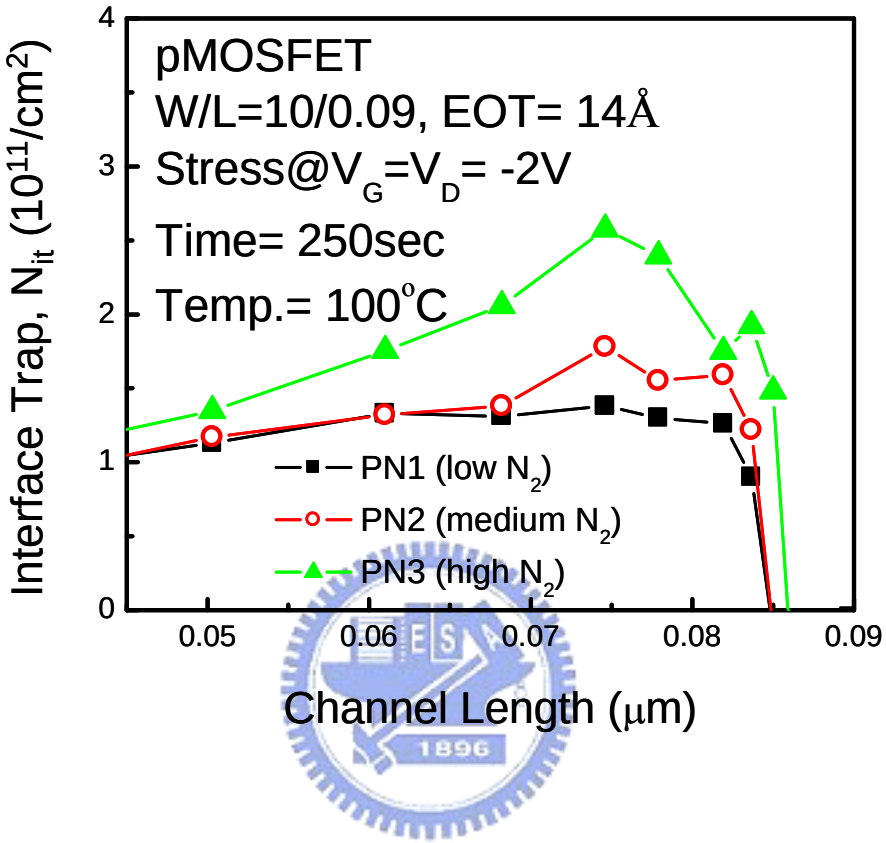


Fig. 4.2 Asymmetrical NBTI stress where source is grounded while $V_G = V_D = -2V$ is applied at the drain side. Note that PN1 has a lower plasma nitridation density and a better reliability.

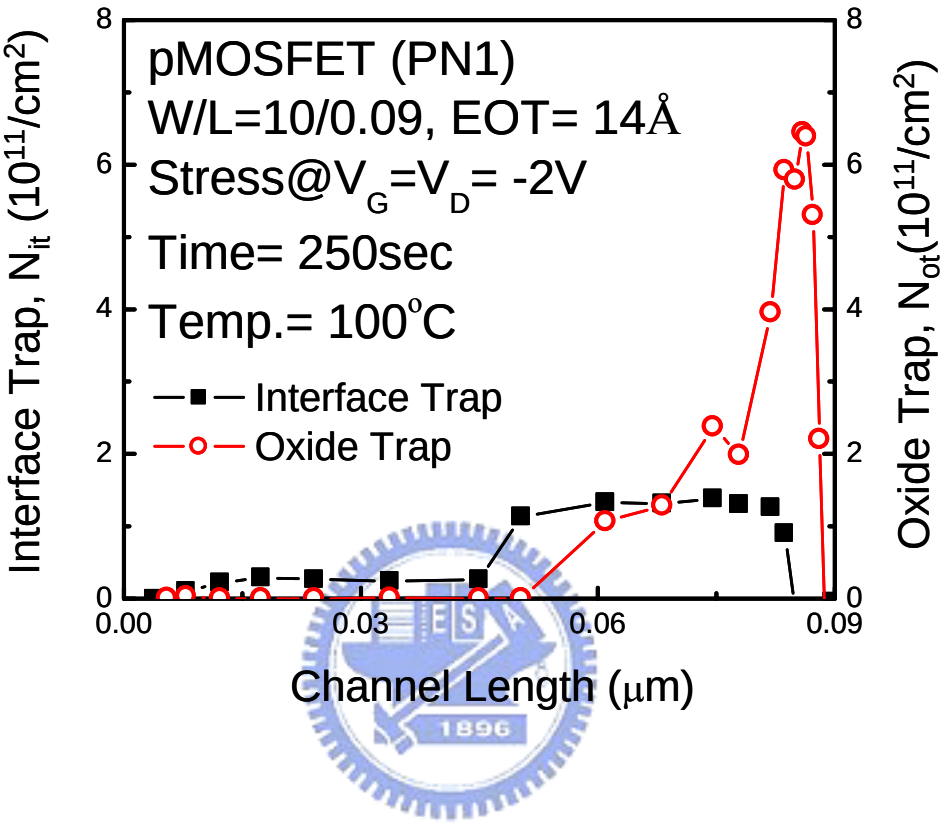


Fig. 4.3 Asymmetrical NBTI stress where source is grounded while $V_G = V_D = -2V$ is applied at the drain side (PN1). Note that N_{it} is dominant of the device degradation since N_{it} has larger values inside the channel region.

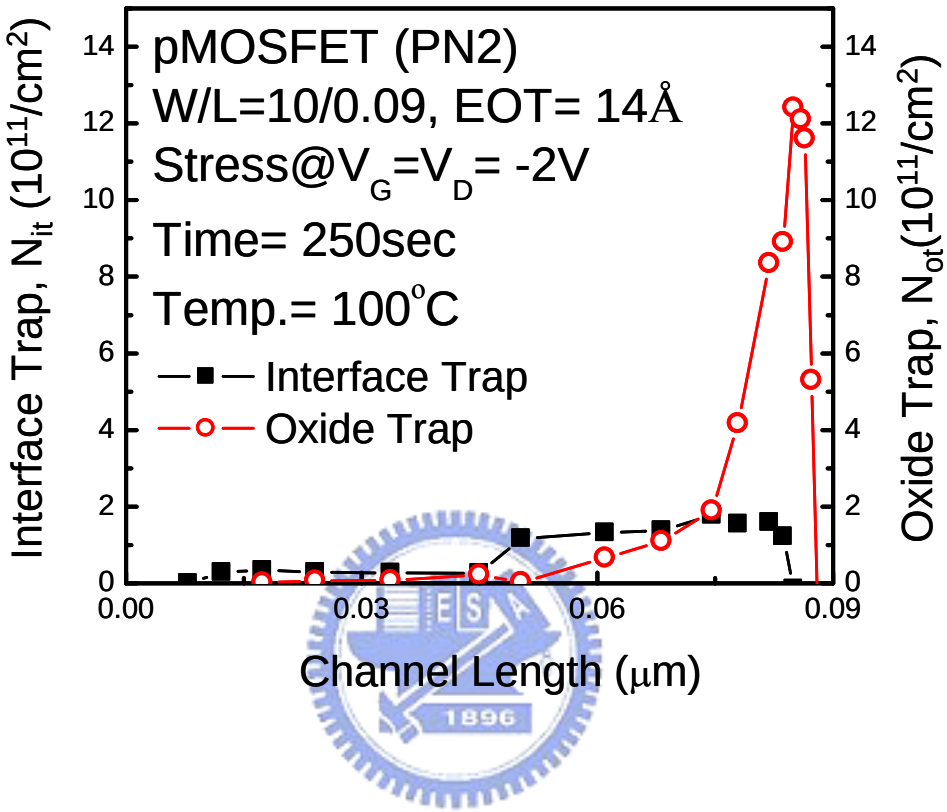


Fig. 4.4 Asymmetrical NBTI stress where source is grounded while $V_G = V_D = -2V$ is applied at the drain side (PN2). Note that N_{it} is dominant of the device degradation since N_{it} has larger values inside the channel region.

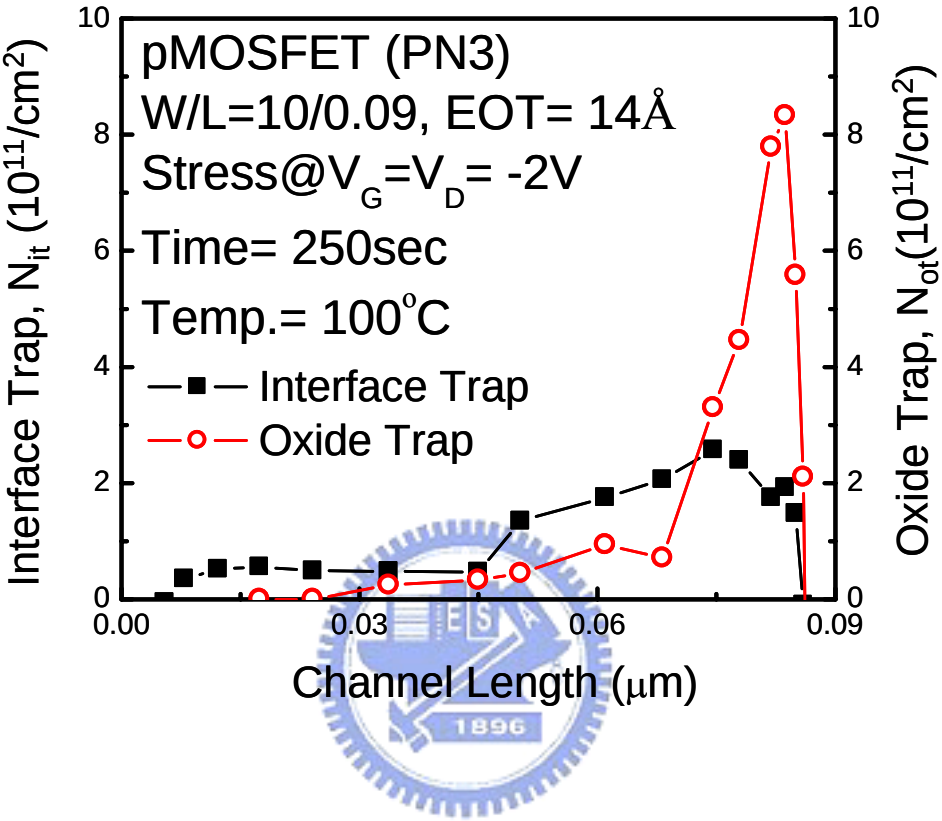
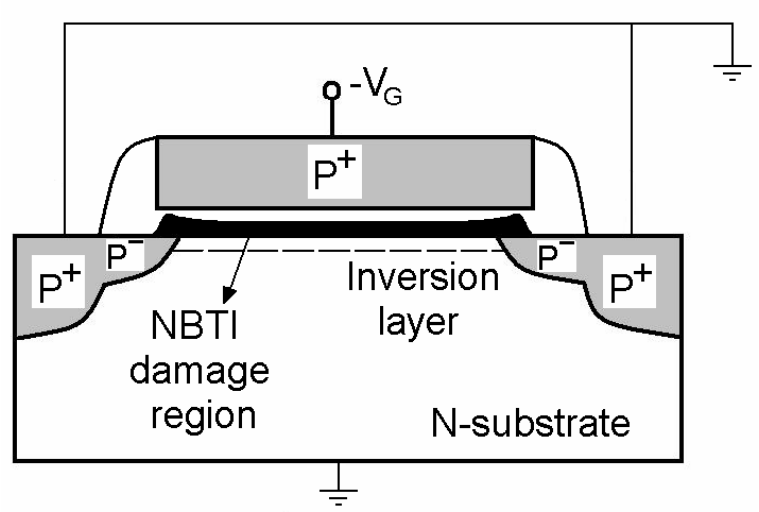
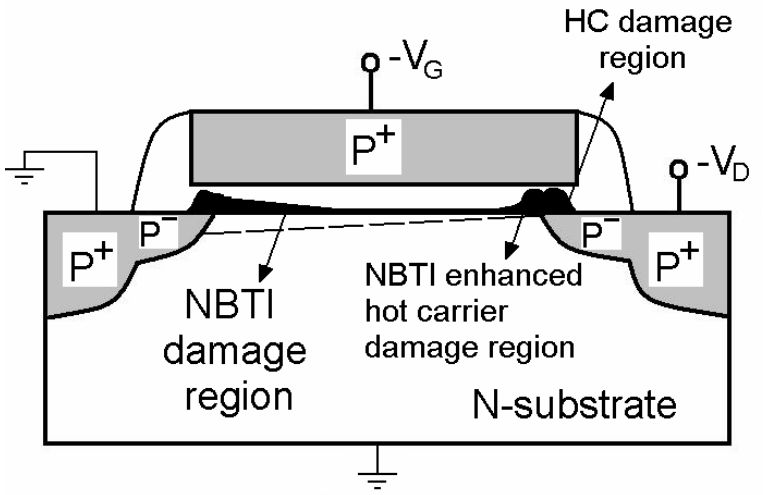


Fig. 4.5 Asymmetrical NBTI stress where source is grounded while V_G= V_D= -2V is applied at the drain side (PN3). Note that N_{it} is dominant of the device degradation since N_{it} has larger values inside the channel region.



(a)



(b)

Fig. 4.6 The degradation region under

(a) NBTI stress.

(b) NBTI-like HC stress (V_G= V_D stress at high-T).

damage occurred near the channel edge region (gate-S/D overlap), which is caused by the locally enhanced degradation reactions between the holes and oxide defects. Finally, we know that the NBTI will enhance the hot carrier degradation from the experiment of NBTI-like stress.

Chapter 5

Summary and Conclusion

As gate oxide thickness continues to scale, it will cause experiment measurement error as a result of direct tunneling current. Under such circumstances, the accuracy is poor for the determination of interface traps and oxide traps of device after HC and NBTI stress. On the basis of this reason, we develop a new method that combines IFCP method and three-steps neutralization to obtain the distribution of N_{it} and Q_{ot} after the hot carrier stress. The IFCP method has been validated to remove the tunneling leakage current during measurement and neutralization step was used to separate the N_{it} and Q_{ot}.

In this thesis, the test samples were fabricated using DPN treatment to have nitrogen rich on the top of silicon dioxide, including three different concentrations of nitrogen with 14Å and 16 Å, respectively. The concentration dependence and oxide thickness of HC effect were performed. Subsequently, the concentration dependence of NBTI and NBTI-like effect were evaluated.

Based on the experimental results, we found that the interface trap is the dominant I_D degradation at $V_G = V_D$ stress condition and the worst I_D degradation is under $V_G = V_D$ stress condition in both of nMOSFET and pMOSFET. From the distribution of interface traps, we found the oxide degradation under HC stress has better reliability in nMOSFET with thinner gate oxide thickness and higher nitrogen content and has better reliability in pMOSFET with thicker gate oxide thickness and lower nitrogen content. Furthermore, NBTI and NBTI-like effect enhance the device degradation with higher nitrogen content. Therefore, for reliability test, the content of nitrogen in gate oxide will become increasingly important in future nanoscale CMOS devices before using high-k dielectric.

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