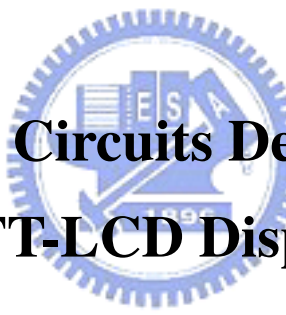


國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用於薄膜電晶體液晶顯示器
驅動電路之設計



**Driver Circuits Design for
TFT-LCD Display**

研 究 生：林棋樺

指 導 教 授：吳錦川 教授

中華民國九十三年六月

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摘要

本篇論文的目標是設計應用在液晶顯示器的驅動電路，並且探討能夠達到快速充放電、高解析度、低飄移電壓以及低功率的可能性。液晶顯示器的驅動電路可分為閘級驅動電路和源級驅動電路；閘級驅動電路是由移位暫存器、電位轉換器和輸出緩衝器組成，而源級驅動電路則是由移位暫存器、閃鎖器、電位轉換器、數位對類比轉換器和輸出緩衝器所組成。

要達到快速充放電的目標，我們採用了有快速充放電、超低靜態電流特色的B類緩衝器架構。由於隨著解析度的提升，相對的源級驅動器的輸出緩衝器準確度更顯的重要，因此本論文主要的重點在於設計出一個低飄移電壓的源級驅動器，而為了達到此目標我們運用了chopper offset cancellation技巧，把飄移電壓壓到最小。在高解析度方面，我們實作了一個10位元解析度數位對類比轉換器，架構則是採用Voltage scaling架構，有面積小的優點。

另外在低功率消耗方面，我們設計了電荷共享的電路，half recycling可節省二分之一動態功率，而triple charge recycling可節省三分之二的動態功率。以上電路皆在 $0.35\mu\text{m}$ CMOS製程中試製晶片。

Driver Circuits Design for TFT-LCD Display

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ABSTRACT

In this thesis, we focus on the driver circuits design for TFT-LCD display, and the possibility of high slew-rate, high-resolution, low-offset-voltage, and low power consumption is discussed. The driver circuits of LCD are composed of two parts, the gate driver and the data driver. Gate driver consists of shift registers, level shifters, and output buffers. Data driver is composed of shift register, level shifter, latch, digital to analog converter, and output buffers.

In order to achieve high slew-rate performance, a class-B buffer which is capable of high slew-rate and extremely low static current has been proposed. As the resolution bits become higher, the accuracy of the output buffer becomes more and more important. In this thesis, chopper offset cancellation techniques to reduce input offset voltage has been achieved. For high resolution, a 10-bit digital to analog converter with voltage scaling architecture and small layout area has been implemented.

In addition, charge recycling circuits has been introduced to reduce more power consumption. Half recycling can reduce about 1/2 dynamic power, where Triple charge recycling can reduce about 2/3 dynamic power. All of the above circuits has been designed and fabricated in a 0.35 μm CMOS process.

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國立交通大學

2004/5/31

CONTENTS

CHINESE ABSTRACT

ENGLISH ABSTRACT

ACKNOWLEDGEMENTS

CONTENTS.....	i
TABLE CAPTION.....	v
FIGURE CAPTIONS.....	vi

CHAPTER 1 INTRODUCTION.....	1
1.1 Motivation.....	1
1.2 Thesis Organization.....	2

CHAPTER 2 LIQUID CRYSTAL DISPLAY.....	3
2.1 Liquid Crystal Display Structure.....	3
2.1.1 Introduction to Liquid Crystal.....	3
2.1.2 Passive/Active Matrix LCD.....	5
2.1.3 Pixel Structure of TFT-LCD.....	6
2.1.4 Structure of LCD Panel.....	8
2.2 TFT-LCD Driving Method.....	9

2.2.1	Inversion Driving Method.....	9
2.2.2	Direct Driving and AC Modulation Driving.....	10
2.3	Periphery Driver Circuits.....	11
2.3.1	Scan Driver.....	12
2.3.2	Data Driver.....	13

CHAPTER 3 OUTPUT BUFFERS FOR DATA

	DRIVER.....	15
3.1	Design Consideration of OP-AMP for AMLCD....	15
3.2	Unity-Gain Voltage Buffers.....	18
3.2.1	Unity-Gain Voltage Buffers.....	18
3.2.2	Input/Output Rail-to-Rail Operational Amplifier.....	19
3.2.3	High-Speed Operational Amplifier.....	19
3.2.4	Class-B Buffer.....	21
3.3	High-Speed Class-B Buffer.....	21
3.4	Amplifier with Chopper Techniques.....	26
3.5	High-Speed Low-Offset-Voltage Class-B Buffer with Chopper Techniques.....	27
3.6	Simulation Results.....	29

3.6.1	Simulation Results of High-Speed Class-B Buffer.....	29
3.6.2	Simulation Results of Low-Offset-Voltage Class-B Buffer with Chopper Techniques.....	35

CHAPTER 4 DIGITAL TO ANALOG CONVERTER AND CHARGE RECYCLING FOR DATA DRIVER.....37

4.1	Gamma Correction.....	37
4.2	Digital to Analog Converter.....	37
4.2.1	Voltage Scaling DAC.....	38
4.2.2	Charge Scaling DAC.....	40
4.2.3	Time Scaling DAC.....	42
4.3	Low Power Design Consideration.....	44
4.3.1	Half Charge Recycling.....	45
4.3.2	Triple Charge Recycling.....	46

CHAPTER 5 CIRCUIT LAYOUT AND MEASUREMENT

	RESULTS.....	49
5.1	Layout Considerations.....	49
5.2	Measurement Results.....	53

5.2.1	Class-B Buffer.....	55
5.2.2	Class-B Buffer with Chopper Techniques.....	58
5.2.3	Two buffers without charge recycling.....	60
5.2.4	Half charge recycling.....	65
5.2.5	Triple charge recycling.....	66
5.2.6	10-bit Digital to Analog Converter.....	68

CHAPTER 6 CONCLUSIONS AND FUTURE

	WORKS.....	71
6.1	Conclusions.....	71
6.2	Future Works.....	72
	REFERENCES.....	73
	VITA.....	75

TABLE CAPTIONS

Table. I	Timing specification of standard video signal.
Table. II	Timing specification of NEC- $\mu PD16721$.
Table. III	DC voltage values of measured class-B buffer.
Table. IV	Current consumption of measured class-B buffer.
Table. V	Current consumption of two buffers while $V_{in} =4V$.
Table. VI	Current consumption of two buffers as input swing varies at different supply voltages.
Table VII	Current consumption of two buffers as input frequency equals zero.
Table. VIII	Current consumption of half charge recycling at $F_{vin}=33kHz$.
Table. IX	Current consumption of triple charge recycling at $F_{vin}=33kHz$.
Table. X	Calculation of dynamic current consumption.
Table. XI	Measured DAC output values.

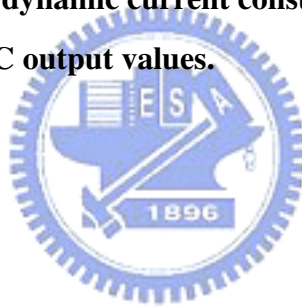


FIGURE CAPTIONS

- Fig.2.1** Liquid crystal materials phases versus temperature.
- Fig.2.2** Basic theory of liquid crystal display. (a) twisted liquid crystal (b) non-twisted liquid crystal.
- Fig.2.3** Passive matrix LCD.
- Fig.2.4** Active matrix LCD.
- Fig.2.5** Effective circuit of pixel.
- Fig.2.6** Pixel layout of TFT-LCD.
- Fig.2.7** Structure of AMLCD system.
- Fig.2.8.** Inversion driving methods of TFT-LCD.
- Fig.2.9** Direct Driving.
- Fig.2.10** AC Modulation Driving.
- Fig.2.11** Periphery driver circuits of TFT-LCD Panel.
- Fig.2.12** Block diagram of scan driver.
- Fig.2.13** Block diagram of data driver.
- Fig.3.1** The block diagram of NEC- $\mu PD16721$.
- Fig.3.2** Relationship between output circuit and D/A converter.
- Fig.3.3** Test model for TFT-LCD source driver.
- Fig.3.4** Traditional input/output rail-to-rail constant- g_m class-AB operational amplifier.
- Fig.3.5** Block diagram of the class-B amplifier.
- Fig.3.6** Circuit schematic of the p-input class-B output buffer.
- Fig.3.7** Complete circuit schematic of the rail-to-rail class-B output buffer.
- Fig.3.8** Proposed driving scheme.
- Fig.3.9** Chopping principle including signals in frequency and time domain.
- Fig.3.10** Architecture of class-B buffer with chopper techniques. (a) Chopper block circuit. (b) Complete circuit schematic of class-B buffer with chopper techniques.
- Fig.3.11** DC values of class-B buffer with V_{in} equals 0.2V.
- Fig.3.12** DC values of class-B buffer with V_{in} equals 4.2V.
- Fig.3.13** Dead zone simulation method.
- Fig.3.14** Dead zone with input voltage = 0.2V.
- Fig.3.15** Dead zone with input voltage = 4.2V.
- Fig.3.16** Alternative method to measure dead zone.
- Fig.3.17** Dead zone of class-B buffer with $1\ \mu\text{A}$ drawn at the output.
- Fig.3.18** Frequency response with $V_{in}=3.196\text{V}$, $V_{in}=3.2\text{V}$, bandwidth=1.62MHz, PM=63° , DC gain=51.2dB.

- Fig.3.19** Frequency response with $V_{in}=3.2V$, $V_{in}=-3.207V$, bandwidth=1.87MHz, PM=67° , DC gain=54.9dB.
- Fig.3.20** Transient response simulation results.
- Fig.3.21** Transient response with input=0.2V, settling time = 4 μ s.
- Fig.3.22** Transient response with input=4.2V, settling time = 4 μ s.
- Fig.3.23** Transient response of first 4.2V, $V_{out} = 4.1957V$.
- Fig.3.24** Transient response of second 4.2V, $V_{out} = 4.2011V$.
- Fig.3.25** Transient response of first 0.2V, $V_{out} = 197.9$ mV.
- Fig.3.26** Transient response of second 0.2V, $V_{out} = 204.05$ mV.
- Fig.4.1** Transparency-to-voltage curve with γ -correction.
- Fig.4.2** Voltage scaling DAC (1).
- Fig.4.3** Voltage scaling DAC (2).
- Fig.4.4** Charge-Redistribution DAC.
- Fig.4.5** Two-step charge scaling DAC.
- Fig.4.6** C-2C charge scaling DAC.
- Fig.4.7** The concept of time scaling DAC.
- Fig.4.8** The circuit diagram of the half charge recycling.
- Fig.4.9** Waveform of the half charge recycling and its current consumption.
- Fig.4.10** The circuit diagram of the triple charge recycling.
- Fig.4.11** Waveform of the triple charge recycling and its current consumption.
- Fig.4.12** Input waveform of the triple charge recycling.
- Fig.5.1** Layout of input differential amplifier.
- Fig.5.2** Layout of feedback capacitor.
- Fig.5.3** Layout of whole voltage buffer.
- Fig.5.4** Layout of 10-bit voltage scaling DAC.
- Fig.5.5** Layout of whole chip and pad names.
- Fig.5.6** Layout floorplain.
- Fig.5.7** Chip die photo.
- Fig.5.8** Several measurement PCB boards.
- Fig.5.9** Simulation results of current consumptions of SS, TT, FF corners and measured current.
- Fig.5.10** Measurement condition of measuring transient response.
- Fig.5.11** Measurement results of transient response.
- Fig.5.12** Transient response: chopping clock and V_{out} of class-B buffer with chopper.
- Fig.5.13** Three adjacent V_{out} waveforms.
- Fig.5.14** Another three adjacent V_{out} waveforms.
- Fig.5.15** Two buffers without charge recycling.

- Fig.5.16** Current consumptions of different input swings at $V_{dd}=5.0V$.
- Fig.5.17** Current consumptions of different input swings at $V_{dd}=6.0V$.
- Fig.5.18** Current of input stage mirrored current source at $V_{dd}=5.0V$ and $V_{dd}=6.0V$.
- Fig.5.19** Current of different stage transistors at $V_{dd}=5.0V$.
- Fig.5.20** Gate voltages of two output stage MOS transistors.
- Fig.5.21** Waveform of half charge recycling.
- Fig.5.22** Waveform of triple charge recycling.
- Fig.5.23** DAC resistor string.
- Fig.5.24** Resistance of N-well grows larger as the voltage drop across itself becomes larger.
- Fig.5.25** Output waveform of DAC when input code changes from 0000000000 to 1111111111.




CHAPTER 1

INTRODUCTION

1.1 Motivation

In recent years, flat panel display has been widely used and become the main stream of future display devices. The most popular display material is liquid crystal. For LCD (liquid crystal display), its advantages compared with traditional CRT (cathode ray tube) display devices are lower power consumption, lighter weight, smaller volume, and less radiation.

As the display technology advances, the future system requirements for LCD devices are listed below:

- 
- Higher color depth. (10 bits/color).
 - High resolution. (more than 45 dots per inch)
 - Larger panel size. (LCD-TV applications)
 - Wide view-angle. ($> \pm 60^\circ$ in both horizontal and vertical directions)
 - Ultra high contrast ratio. ($> 600:1$)
 - Low power consumption.

The market of LCD devices is growing larger and larger because of the electronic products of next generation are all using flat panel displays, such as cell phone, notebook, digital camera, portable digital assistant, LCD-TV, etc. Actually, LCD has already replaced the traditional CRT.

The key considerations of future specification of LCD are higher color depth and less response time. At present days, the response time of the LCD-TV is not good

enough for catching objects with high velocity in display. Also, as the panel size of LCD-TV become larger and larger, driving large panel is another challenge. But since LCD-TVs are superior in many ways compared with traditional display methods, they have already become the main stream of future display devices. As a result, design of driver circuits on LCD display is certainly worth of future research.

1.2 Organization

In this thesis, we focus on the design of high resolution, high accuracy, low response time, and low power consumption data drivers for TFT-LCD (thin film transistor-liquid crystal display).

In Chapter 2, some background knowledge of LCD, such as passive/active matrix LCD, pixel structure, panel structure, frame driving method and periphery circuits, is described.

In Chapter 3, we discuss the output buffers for data driver. The characteristic of low offset voltage is especially emphasized. Also, low power dissipation and high slew rate are certainly important considerations.

In Chapter 4, digital to analog converter for data driver is discussed. The main considerations for the design of DAC are small area and high resolution. Charge recycling circuits are also introduced.

In Chapter 5, the circuit layouts, measurement results are discussed.

In Chapter 6, conclusions and future works have been made.

CHAPTER 2

LIQUID CRYSTAL DISPLAY

2.1 Liquid Crystal Display Structure

2.1.1 Introduction to Liquid Crystal

Liquid crystal was first found by F. Reinizer in Australia in 1888, but it was not applied for modern display until 1960's [1]. There are many kinds of liquid crystal materials. Distinguished by the arrangement of liquid crystal molecules, they can be divided into three groups, Smectic liquid crystal, Nematic liquid crystal, and Cholesteric liquid crystal. Different kinds of materials are usually blend for different applications.

Differing by the temperature, one important characteristic of liquid crystal materials is called “twice melting”. Below the melting point T_m they are solid crystalline, where above the clearing point T_c they are clear liquid. Between T_m and T_c , the materials look milky liquid but still exhibit the order phases, called mesophase. Fig.2.1 illustrates the temperature versus phases. For TFT-LCD applications, it is always used in mesophase.

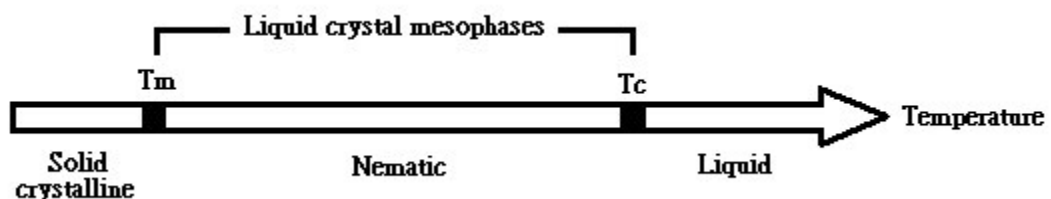


Fig.2.1 Liquid crystal materials phases versus temperature [1].

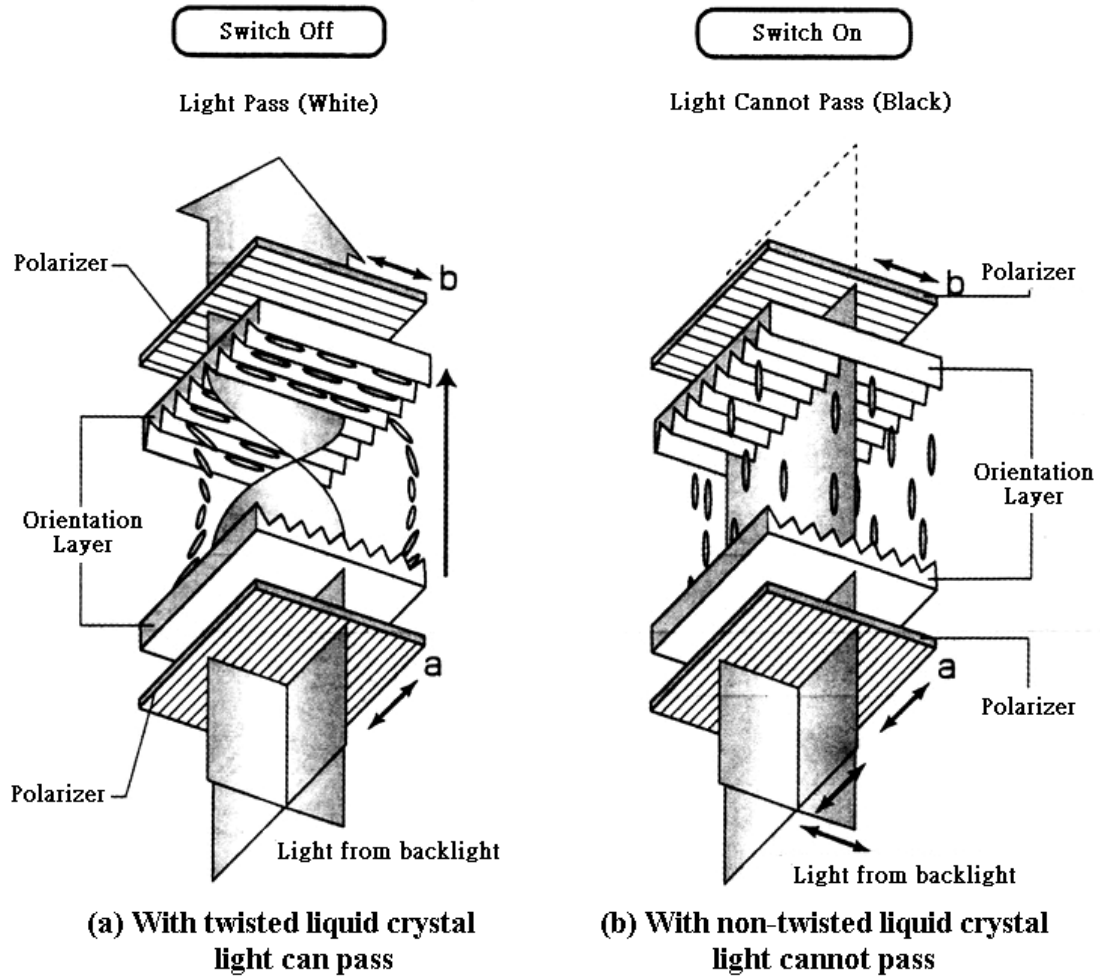


Fig.2.2 Basic theory of liquid crystal display. (a) twisted liquid crystal (b) non-twisted liquid crystal [2].

Fig.2.2 shows the basic theory of LCD. The basic structure of liquid crystal display is upper and lower polarizers with orientation layers. For upper and lower polarizers with 90° phase difference, we call it “Normally White” where both polarizers with the same phase are called “Normally Black”. In Fig.2.2 (a), without applying any external voltage, the liquid crystal twists 90° phase and guide the light to pass both the polarizers in “Normally White” case. But in Fig.2.2 (b), applying a large voltage supplied by transparent electrodes outside the orientation layers causes all liquid crystal molecules turn into one direction and the light cannot pass. If we apply a smaller voltage in between, the panel would look between black and white. By controlling the applied voltage, LCD can display different gray levels.

2.1.2 Passive/Active Matrix LCD

For dynamic drive, it can be divided into two different methods, passive matrix LCD (PMLCD) and active matrix LCD (AMLCD). Fig.2.3 and Fig.2.4 illustrate the two methods. The PMLCD uses row electrode (X) and column electrode (Y) to determine the gray scales of each pixel. The drawback of PMLCD is that pixels on the same row or column would influence one another. To solve this problem, in AMLCD we use a TFT (thin film transistor) or a diode as a switch for each pixel. Another advantage of AMLCD is its higher operating frequency compared to PMLCD. Since that AMLCD has been commonly used in large and high-resolution panel products.

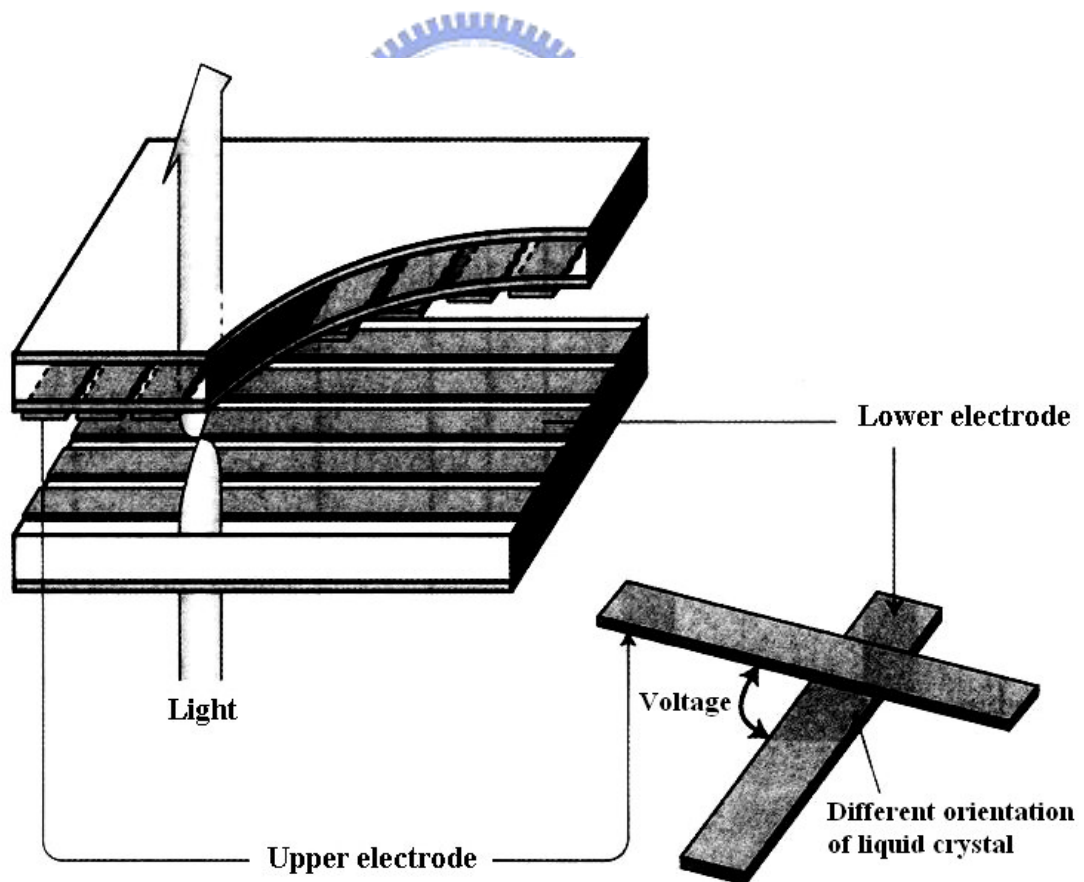


Fig.2.3 Passive matrix LCD [2].

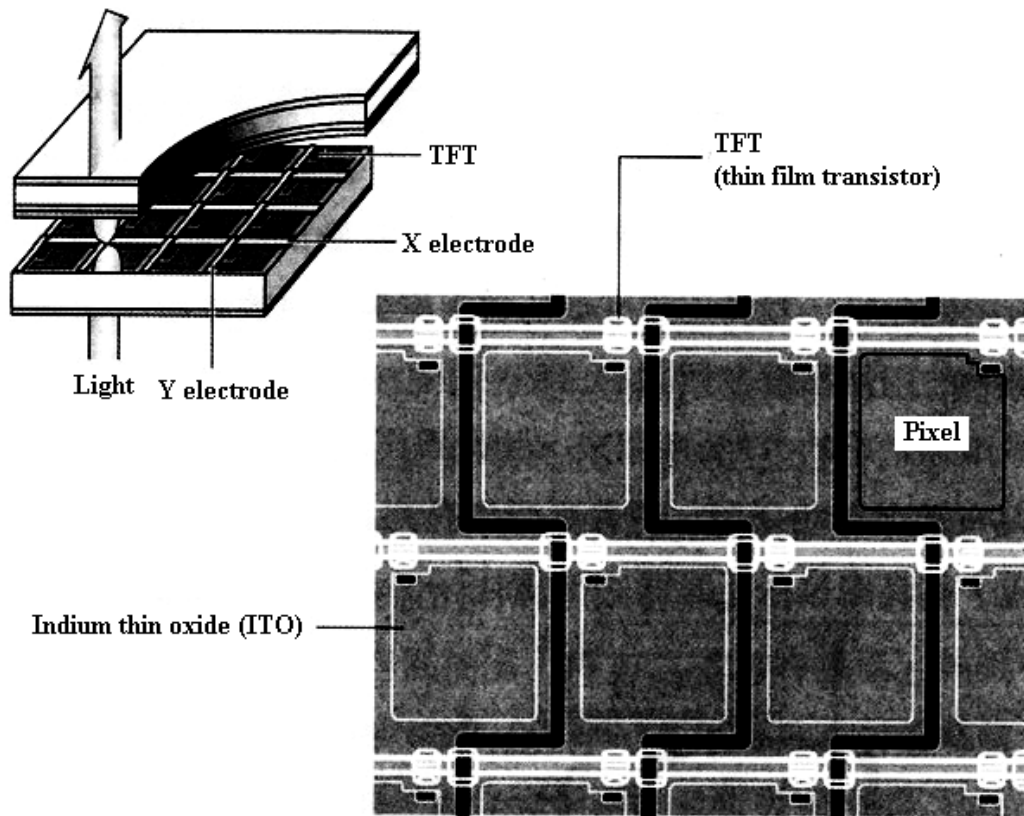


Fig.2.4 Active matrix LCD [2].

2.1.3 Pixel Structure of TFT-LCD

One pixel is the basic unit of LCD panel. Pixel structures and its layouts are shown in Fig.2.5 and Fig.2.6. There are two kinds of pixel structure, Cs on common and Cs on gate. Comparing Cs on common and Cs on gate, Cs on gate has the advantage of compensating the unstableness of voltage level caused by feed-through effect from C_{gd} , but Cs on gate need more complicated scan-line signals than Cs on common. Fig.2.5 shows the effective circuit of each pixel. C_{ls} stands for the effective capacitor of liquid crystals, C_{gd} is the parasitic capacitor between scan-lines and effective liquid crystal capacitor, and C_s is the storage capacitor that stores the voltage between frame transitions. The transistor in each pixel is a TFT (thin film transistor)

used as a switch. Fig.2.6 illustrates the layout of each pixel. The layout area exclusive of the dash-line squared region is called aperture region, where the light can pass from the backlight source. Of course, the larger aperture region, the higher panel brightness it is.

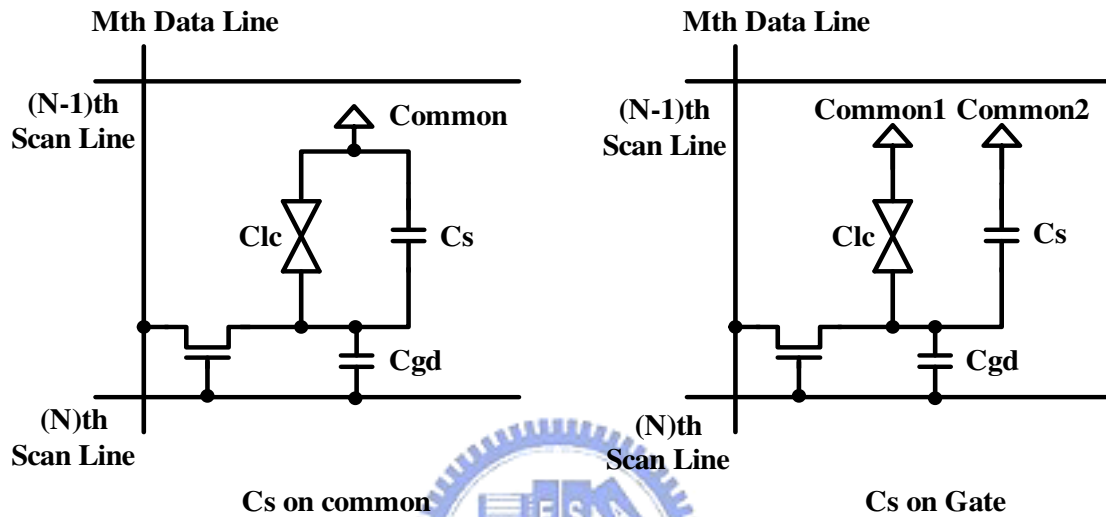


Fig.2.5 Effective circuit of pixel [3].

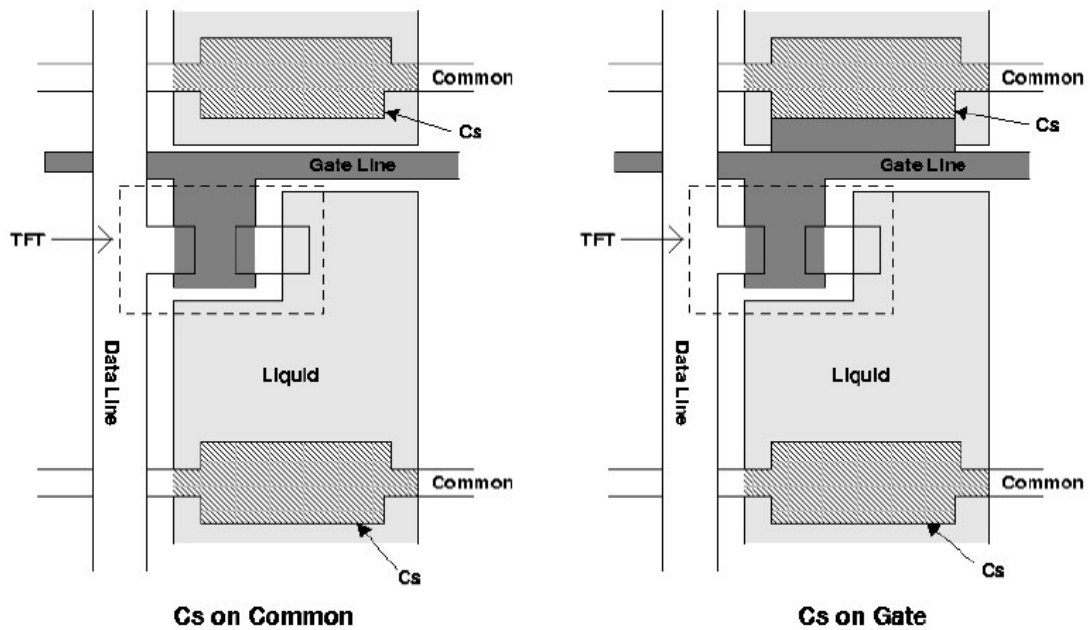


Fig.2.6 Pixel layout of TFT-LCD [3].

2.1.4 Structure of LCD Panel

The structure of LCD panel is shown in Fig.2.7. As described in 2.1.1, there are two polarizers, backlight, and liquid crystal layer. Between the lower polarizer and liquid crystal is the TFT substrate, which is used to control the applied voltage of each pixel. TFT substrate contains a glass substrate, TFT switches, transparent electrodes, and alignment layers. Transparent electrodes are made by ITO (Indium Thin Oxide), and by voltage supplied from TFT on the glass substrate they can be used to control the directions of liquid crystal molecules in each pixel. There are also color filters, which contain three original colors, red, green, and blue (RGB). For color filter substrate, we also need an alignment layer, a transparent electrode, color filters, a glass substrate and a polarizer. By controlling the amount of light passing through color filter, i.e., different kinds of color intensities, million kinds of colors can be realized.

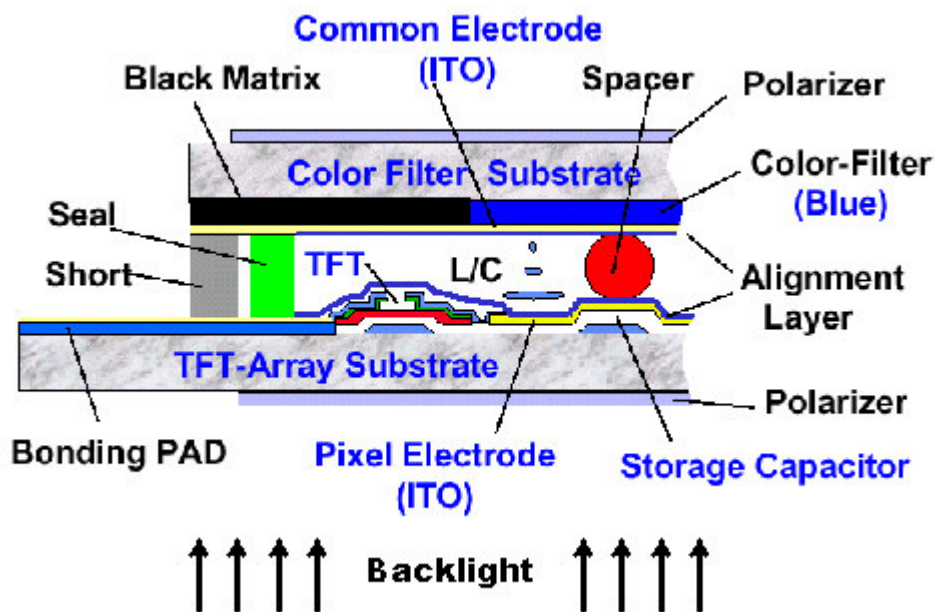


Fig.2.7 Structure of AMLCD system [4].

2.2 TFT-LCD Driving Method

2.2.1 Inversion Driving Method

Liquid crystal materials contain ionic impurities that drift to electrode under a DC field. If sufficient impurities collect to an electrode, they nullify the charge on the electrode. This would cause a permanent damage of LCD and thus abnormal operations. Since keeping a net zero DC field across the LC materials is the basic driving method of LCD panels. Each pixel should be driven with alternating polarity signal to keep a net zero DC field. This is called “Inversion Driving”.

There are four types of inversion driving: frame inversion, row inversion, column inversion, and dot inversion. These are illustrated in Fig.2.8. The best display quality is the dot inversion, but this method needs more complicated driving signal.

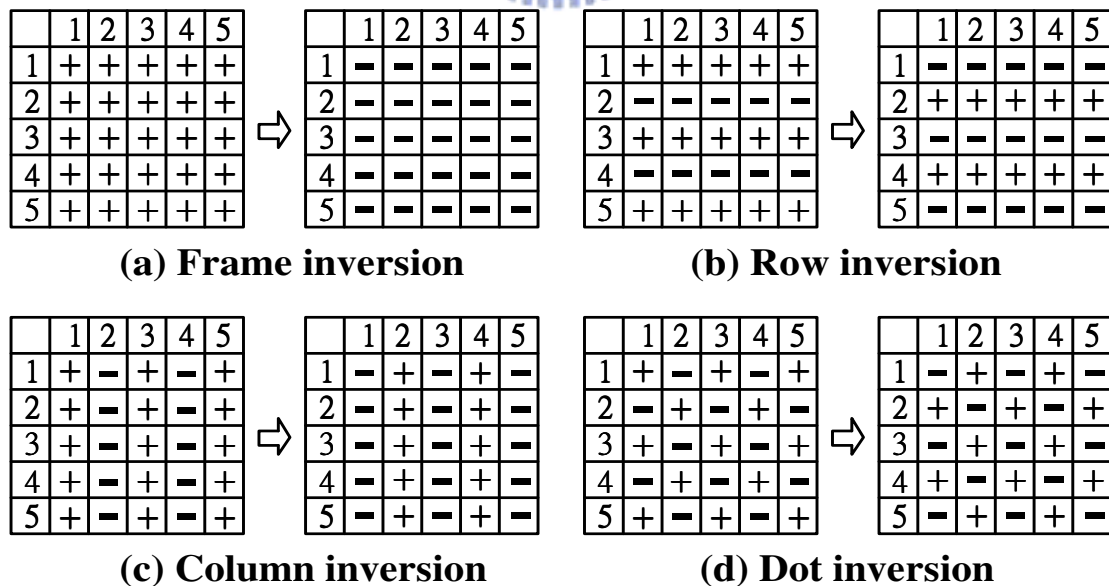


Fig.2.8. Inversion driving methods of TFT-LCD.

2.2.2 Direct Driving and AC Modulation Driving

As described in 2.2.1, an effective zero DC field across the liquid materials should always be kept. There are two kinds of data driving method, “Direct Driving” and “AC Modulation Driving” as shown in Fig.2.9 and Fig.2.10. In Direct Driving the common voltage of each pixel is fixed where in AC Modulation Driving is not. For better display quality and simpler design, Direct Driving is better. But the voltage swing of AC Modulation Driving is smaller and it is more suitable for low power consumption cases.

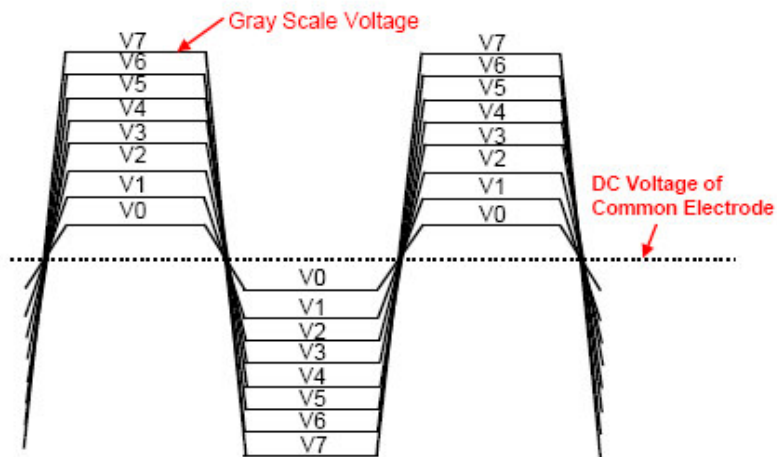


Fig.2.9 Direct Driving [5].

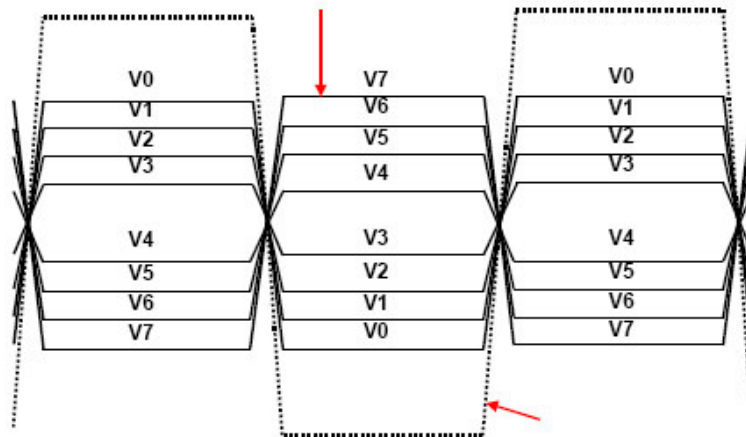


Fig.2.10 AC Modulation Driving [5].

2.3 Periphery Driver Circuits

The periphery driver circuits of TFT-LCD panel are shown in Fig.2.11. There are three major parts of the driver circuits, Timing Controller, Data Driver (also called Source Driver), and Scan Driver (also called Gate Driver). Timing Controller receives the input RGB signals and clock from the previous digital circuits and translates these signals to proper signals for Data Driver and Scan Driver.

The Scan Driver would rise gate voltage of each scan line and turn on the transistors sequentially. Meanwhile, the Data Driver sends the display data to each pixel. Same process will repeat again and again during refresh cycles. Detail descriptions of Scan Driver and Data Driver will be discussed below.

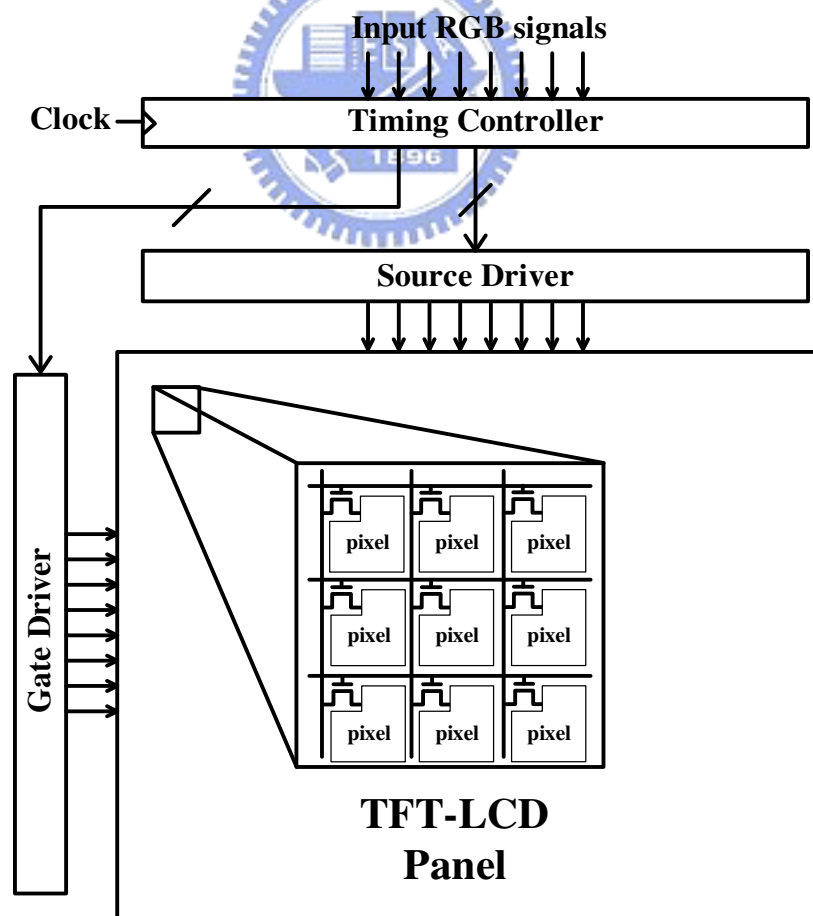


Fig.2.11 Periphery driver circuits of TFT-LCD Panel.

2.3.1 Scan Driver

The block diagram of scan driver is illustrated in Fig.2.12. Scan driver contains shift register, level shifter, and output buffer. The scan driver is just to turn on the TFT switches of a single row in order. Shifter registers can storage input digital signals and pass these to level shifters according to clock timing. Since the voltage to rotate liquid crystal molecules is usually higher than 10V, we need level shifters to get higher voltage. Finally, because each row line can be modeled as a RC-ladder, it is necessary to use some digital buffers that lower the delay time of gate pulse to drive the panel. The numbers of channels of scan driver depend on the TFT-LCD panel size. Table.I also shows the timing specification of standard video signal.

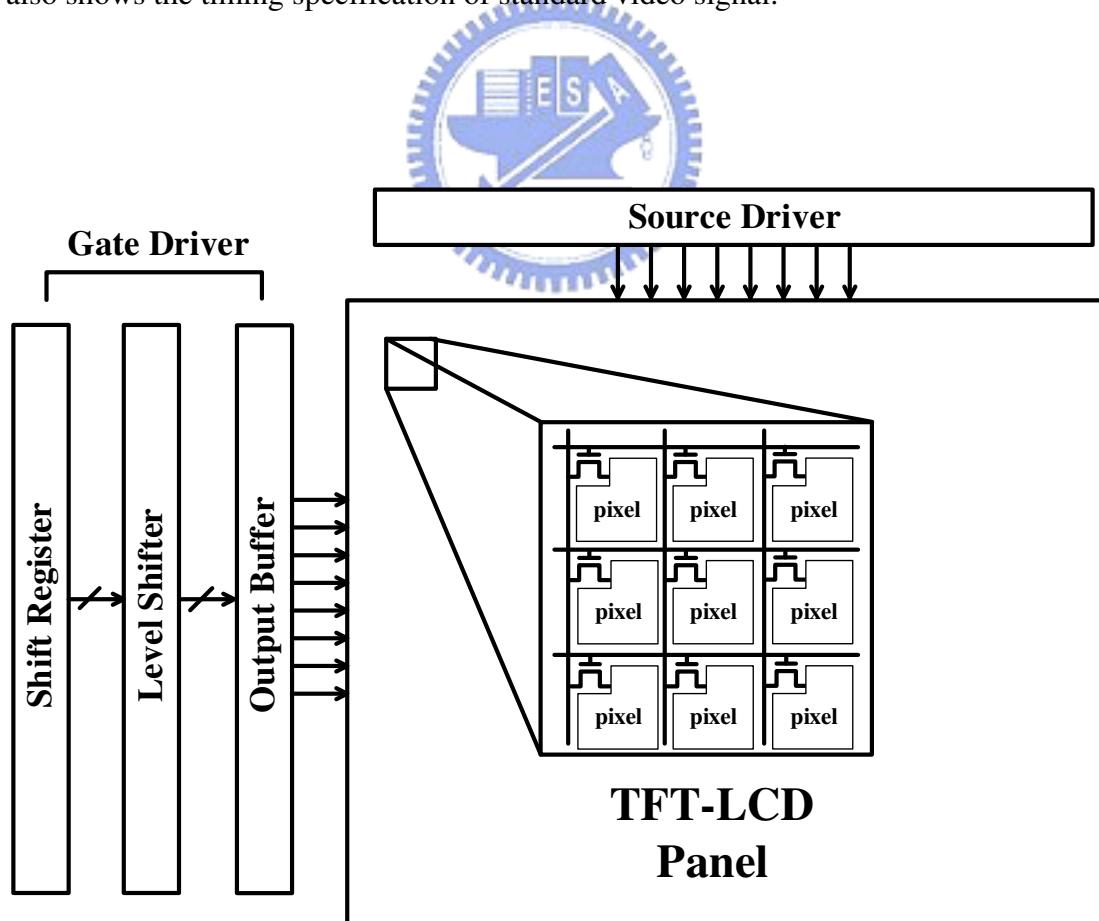


Fig.2.12 Block diagram of scan driver.

Mode	VGA	SVGA	XGA	SXGA	UXGA
Total	800x525	1056x628	1344x806	1688x1066	2160x1250
Active	640x480	800x600	1024x768	1280x1024	1600x1200
Pixel Clock	25.18MHz	40.11MHz	65.00MHz	108.0MHz	162.0MHz
Fh	31.469kHz	37.879kHz	48.363kHz	63.981kHz	75.000kHz
Fv	59.941Hz	60.317Hz	60.004Hz	60.020Hz	60.000Hz
H Total (A)	31.78 us	26.40 us	20.68 us	15.63 us	13.33 us
H Display (D)	25.42 us	20.00 us	15.75 us	11.852 us	9.877 us
V Total (O)	16.68 ms	16.58 ms	16.67 ms	16.66 ms	16.67 ms
V Display (R)	15.52 ms	15.84 ms	15.88 ms	16.01 ms	16.00 ms

Table.I Timing specification of standard video signal.

2.3.2 Data Driver

There are two kinds of TFT-LCD data driver, analog and digital type. Since analog data driver is only suitable for small panels due to its sample and hold architecture, in this thesis we only discuss digital data driver which is used to drive large panels. Digital data driver contains five parts: shift registers, data latches, level shifter, DAC with gamma correction and analog output buffer. Fig.2.13 illustrates the block diagram of data driver. Input data signals are serially read and stored by shift registers and data latches. Digital to analog converter converts digital display data into analog voltage signals, and gamma correction is used to compensate the sense of sight for human eyes. Finally, to drive the effective RC-ladder liquid crystal, it is necessary to design output analog buffer with high slew-rate.

As the accuracy bits of digital display data become higher, the design of low offset voltage output analog buffer become a challenge. Since in this thesis, low offset voltage buffer will be mainly discussed.

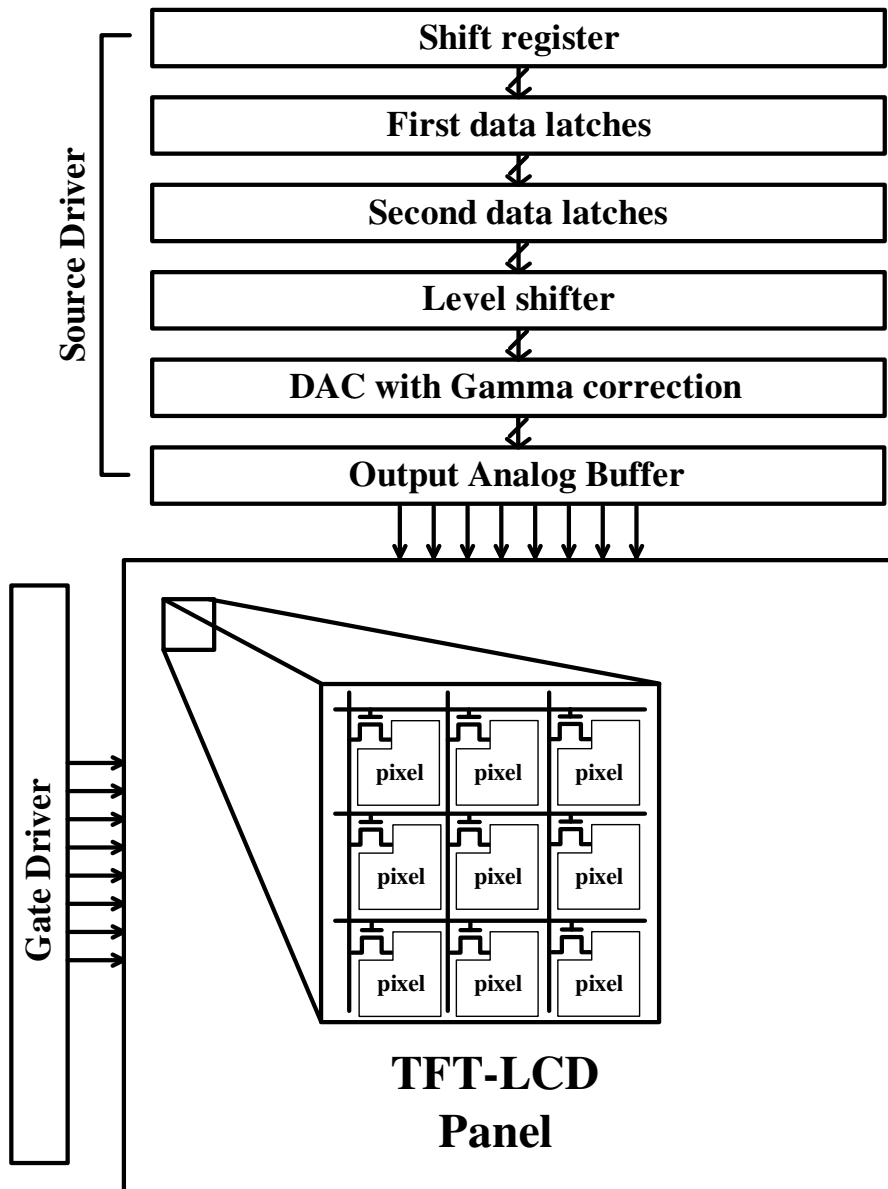


Fig.2.13 Block diagram of data driver.

CHAPTER 3

OUTPUT BUFFERS FOR DATA DRIVER

3.1 Design Consideration of OP-AMP for AMLCD

For TFT-LCD data driver, it contains shift registers, data latches, level shifter, DAC, and output buffer as described in chapter 2. To discuss the design consideration of OP-AMP for AMLCD, let us take NEC- $\mu PD16721$ as an example [6]. The NEC- $\mu PD16721$ is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ -corrected by an internal D/A converter. The block diagram of NEC- $\mu PD16721$ is as shown in Fig.3.1. Shift register and data register are used to store the input digital data in order, and due to inversion driving method we need a latch to control the signal polarities. In order to drive liquid crystal, it is necessary to use high voltage around 12V, and the level shifter is used to shift low voltage digital signals to high voltage ones. Also, since the NEC- $\mu PD16721$ is designed to display 256-gray scales, its D/A converter consists of a string of resistance which is divided into 256 segments, and 8-to-256 multiplexer and some voltage buffers. The relationship between output circuit and D/A converter is illustrated in Fig.3.2. When the voltage supplied to resistor string is between 9.8V to 5.5V or between 4.5V and 0.2V, according to the data sheet the standard output deviation of output buffer is ± 10 mV and the allowed maximum value is ± 20 mV.

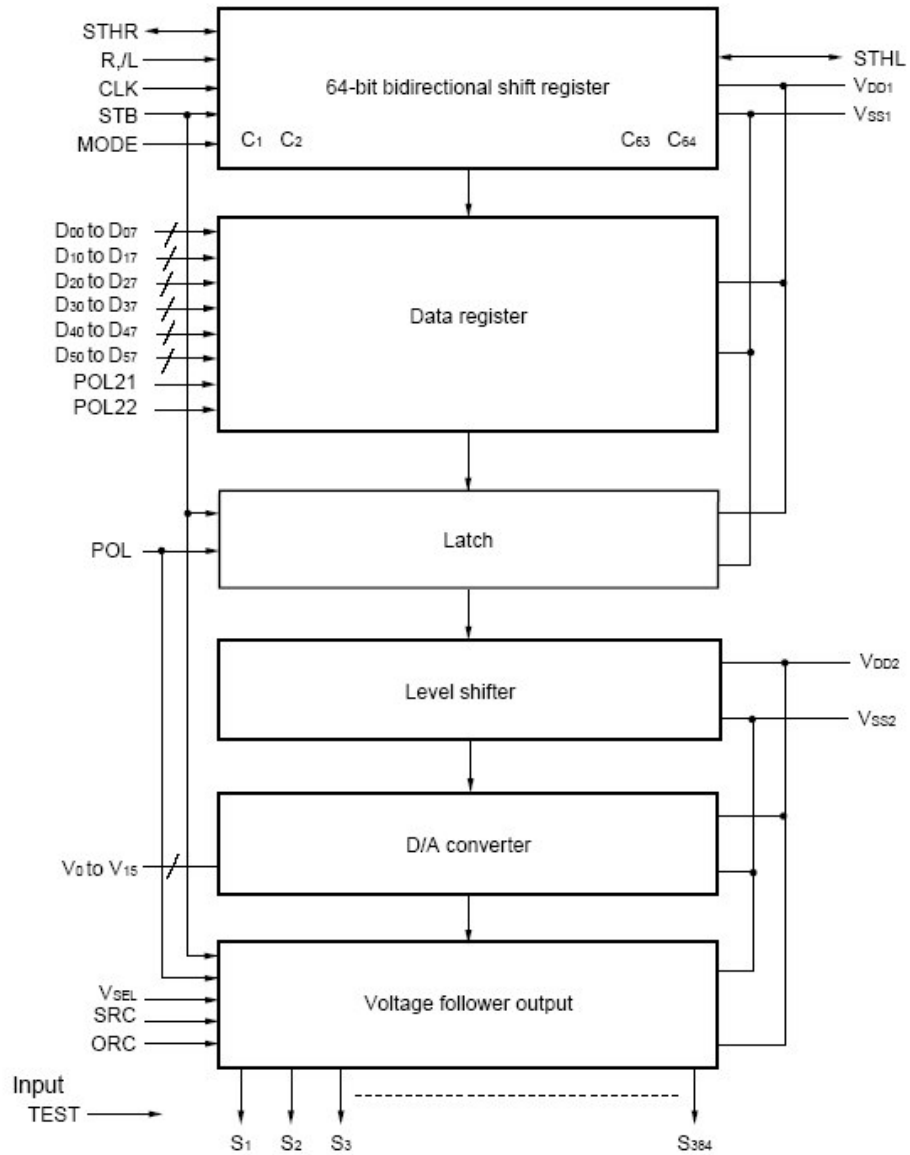


Fig.3.1 The block diagram of NEC-μPD16721 [6].

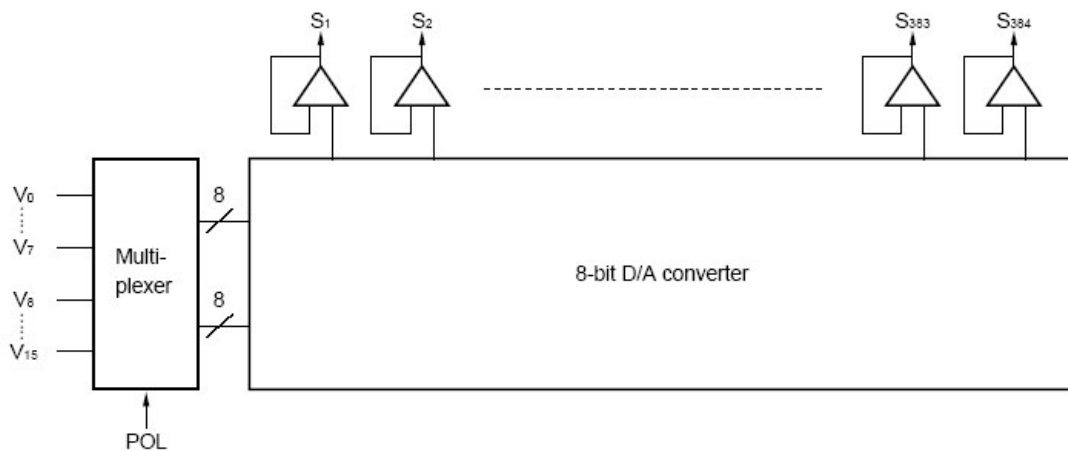


Fig.3.2 Relationship between output circuit and D/A converter [6].

For output voltage between 9.8V to 5.5V or between 4.5V and 0.2V with 8-bit resolution, i.e., 256 gray levels, the maximum allowed deviation of output buffers are calculated as followed:

$$\text{Voltage Range } V_R = 9.8V - 5.5V = 4.3V \quad (3-1)$$

$$\text{LSB} = \frac{4.3V}{256} = 16.8mV \quad (3-2)$$

$$\frac{1}{2} \text{LSB} = \frac{16.8mV}{2} = 8.4mV \quad (3-3)$$

Since the calculated result is 8.4mV, the ± 10 mV on data sheet is a reasonable range.

The POL signal is used to control the polarity of output voltage due to the inversion driving method. When POL is high, the voltage across the resistor string is between 9.8V and 5.5V. And if POL is low, the voltage across the resistor string is between 0.2V and 4.5V. In Fig.3.3, the testing model of column driver is illustrated. In actual practice, the resistance and capacitance values depend on the panel size. There is only about 10 microseconds to settle the display analog voltage, or the TFT switch will turn off and the pixel will get incorrect display value. The timing specification of NEC- μ PD16721 is listed in Table.II. Since the output buffer should be designed as input/output rail-to-rail, high slew-rate, and low output voltage deviation for different voltage applications.

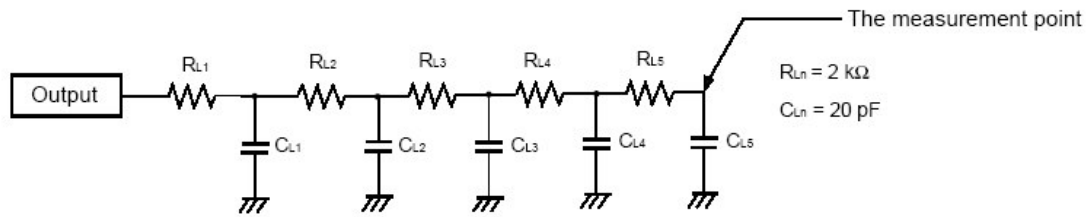


Fig.3.3 Test model for TFT-LCD source driver [6].

Time	Specification
Arrival time through digital block to analog output	Output-target voltage within 10% in 5us
Settling time from output voltage to target voltage	Settled voltage within 10mV in another 5us

Table. II Timing specification of NEC- $\mu PD16721$ [6].

3.2 Unity-Gain Voltage Buffers

3.2.1 Unity-Gain Voltage Buffers

From the above discussions, the design considerations of voltage buffer for LCD data driver could be concluded. First, we need input/output rail-to-rail operational amplifier due to inversion driving method. Second, we need high slew-rate unity-gain voltage buffer due to timing constrains. Also, layout area and power consumption are important issues. For example, to drive a LCD panel such as XGA standard, it is necessary to use eight 384-pin data driver ICs to drive 3072 columns. Since there are 384 output buffers in a single IC, any wasted area or unnecessary power consumption

in a single buffer would result in a huge penalty. We can conclude that input/output rail-to-rail, speed, layout area, and power consumption are main design considerations. In this thesis, all will be considered.

3.2.2 Input/Output Rail-to-Rail Operational Amplifier

One traditional input/output rail-to-rail constant- g_m class-AB operational amplifier is illustrated in Fig.3.4 [7]. In order to achieve input rail-to-rail, two differential amplifiers including PMOS and NMOS type are used. Class-AB output stage is used because of output rail-to-rail. Left part of this circuit is constant- g_m design, since we wish the current conductance g_m be the same between different operational regions. There are several drawbacks in this traditional input/output rail-to-rail operational amplifier. First, it is necessary to use many transistors in the circuit, and this would cause unnecessary layout area. Second, the current consumption of this circuit is huge since there are many stages, and class-AB output stage consumes power. Finally, slew-rate and current consumption are trade-off in this design.

3.2.3 High-Speed Operational Amplifier

From the above discussions, this unity-gain voltage buffer is basically a slew-rate limited buffer. There are several reasons for this. First, the input display signals are always unit step functions due to different digital display data. Second, since it is necessary to use inversion driving method, i.e., even with the same gray level during two scan period, the input voltage for this buffer would swing between two different

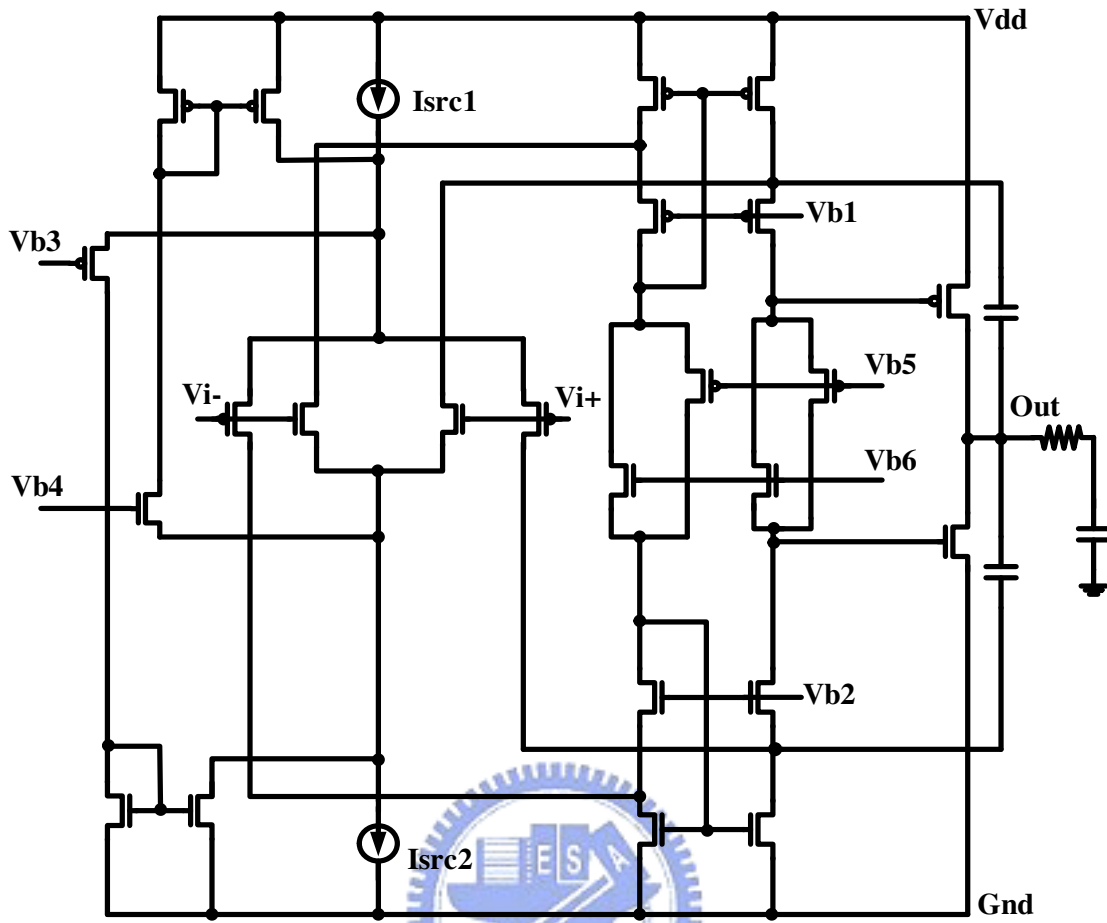


Fig.3.4 Traditional input/output rail-to-rail constant- g_m class-AB operational amplifier [7].

polarities. The worst operation condition of this buffer occurs when the LCD panel displays normally white/black, where the output voltage buffer will be sent during 9.8V and 0.2V between frames to maintain inversion driving. Obviously, the slew rate of this voltage buffer must be enhanced. Several methods to achieve high slew-rate have been proposed [8]-[9].

3.2.4 Class-B Buffer

For traditional operational amplifier with class-AB output stage, the sizes of the output stage MOSs are usually made large for driving large capacitance and resistance loading. But the drawback of this kind of design is that the output stage would consume large current. When designing TFT-LCD driver circuit, there are 384 output voltage buffers and each voltage buffer must consume only a little current, or the total current consumption would be way too huge. Also, class-AB buffer consumes large power even when input signal is static, which means that even when there is no transition, it still wastes power.

Class-B buffer design is a good solution for solving above problems. The main characteristics of class-B are large driving capability, which means high-slew rate, extremely low static current consumption, and low output voltage deviation. Several class-B buffer designs for driving TFT-LCD panel had been proposed [10]-[11].

3.3 High-Speed Class-B Buffer

The class-B amplifier had been presented as a LCD column driver [12]. Although class-B amplifier is limited to some specific applications due to its inherent crossover distortion, it can be used as an output buffer for a stepwise signal as long as the crossover distortion is smaller than the smallest required resolution. Thus, it is suitable for a flat-panel-display column driver because the input to the driver is always a step function. Fig.3.5 shows the block diagram of the class-B amplifier [12]. It contains one pre-amplifier (AMP), two inverter-type comparators (INV_N, INV_P), and two output transistors (Mn, Mp).

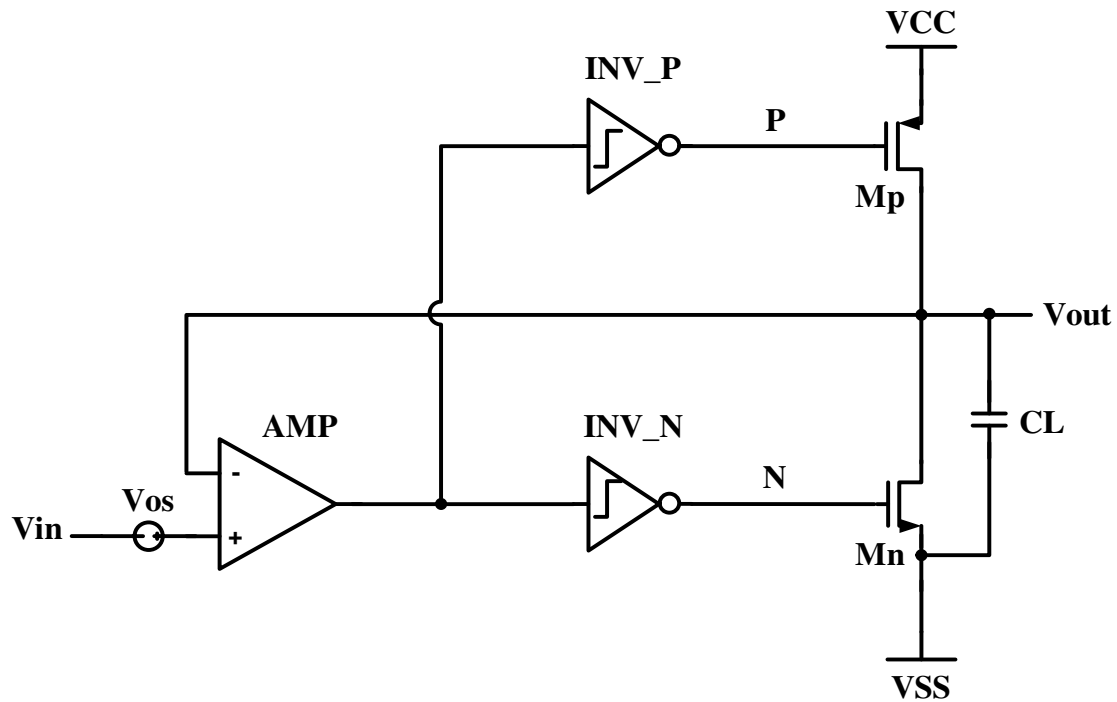


Fig.3.5 Block diagram of the class-B amplifier [12].

This circuit is connected as a negative feedback type. Basic operation principle of the class-B amplifier is described as followed. At the pre-amplifier, AMP amplifies the difference between V_{out} and V_{in} , and the output of this pre-amplifier is connected to two inverters with designed decision level of the comparator. If the voltage of V_{in} is higher than that of V_{out} , it would cause node P logically low and turn on M_p to charge V_{out} . On the other hand, if V_{in} is lower than V_{out} , node N is logically high and turn on M_n to discharge V_{out} . When V_{in} is close enough to V_{out} , i.e., in the dead-zone of this class-B amplifier, it would cause node P logically high and node N logically low, thus both of the output transistors are cutoff. This is the reason why class-B has very low static current, but is capable of charging/discharging loading capacitance quickly enough. The complete circuit schematic of p-input class-B buffer is shown in Fig.3.6. The circuits of pre-amplifier and comparator are modified from the current mirror amplifier. C_1 and C_2 are compensation capacitors.

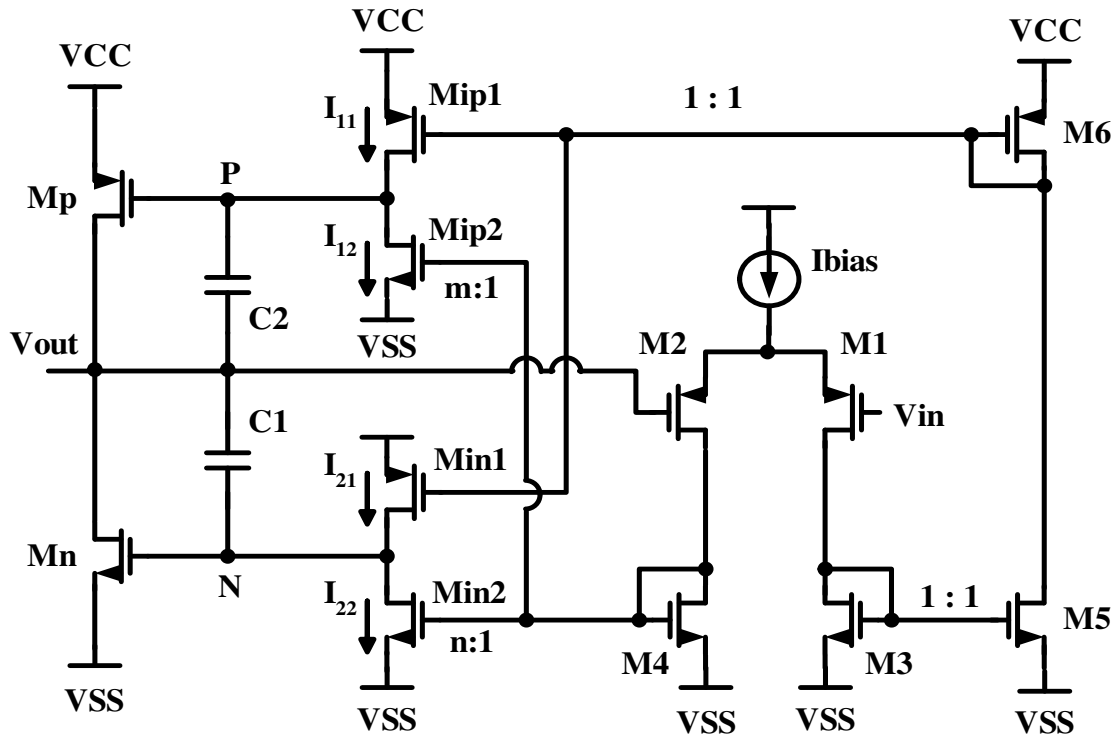


Fig.3.6 Circuit schematic of the p-input class-B output buffer [12].

In order to eliminate quiescent current under class-B operation when V_{out} is equal to V_{in} , both output transistors M_n and M_p must be completely turned off. Thus, the outputs of the comparator INV_N (node N) and INV_P (node P) have to be V_{SS} and V_{CC} , respectively. The following description of circuit operation explains the above requirement. When the V_{out} is equal to V_{in} , the diode-connected loads (M_3 and M_4) of the differential amplifier draw the same current ($I_{M_3} = I_{M_4} = I_{BIAS} / 2$). The current of M_3 is copied to M_{ip1} and M_{in1} via an NMOS (M_5) and a PMOS (M_6) mirror. The ratios of all these mirrors are assumed to be 1 for the ease of discussion, so that the currents of M_{ip1} (I_{11}) and M_{in1} (I_{21}) are the same as I_{M_3} . The current of M_4 is directly mirrored to M_{ip2} and M_{in2} with different ratio of m and n respectively, where m is always smaller than 1 and n is larger than 1, i.e. the current of M_{ip2} (I_{12}) is lower than I_{M_4} and the current of M_{in2} (I_{22}) is higher than I_{M_4} . In consequence, $I_{11} > I_{12}$ and $I_{21} < I_{22}$, which makes the voltage of node P and node N approach V_{CC} and

VSS, respectively. This condition ensures that both output transistors are off when $V_{out} = V_{in}$. When V_{in} is smaller than V_{out} to let $I_{21} > I_{22}$, the voltage of node N will increase to turn on M_n for discharging. On the other hand, when V_{in} is larger than V_{out} to let $I_{11} < I_{12}$, the voltage of node P will decrease to turn on M_p for charging.

The use of current mirror as comparators has two advantages. First, the currents of INV_N and INV_P are limited, so that the device sizes need only to satisfy the required current matching. Second, the tracking of comparators decision level with respect to process and temperature variations is better than the inverters. Fig.3.7 shows the circuit schematic of the rail-to-rail output buffer. The circuit consists of one n-input buffer amplifier and one p-input amplifier, with the common output transistors. The operation principle is the same as n-input buffer mentioned above. But in actual practice, since LCD panel is inherently inversion driving, we can group each two adjacent channels and switch positive polarity and negative polarity during two scan periods as shown in Fig.3.8.

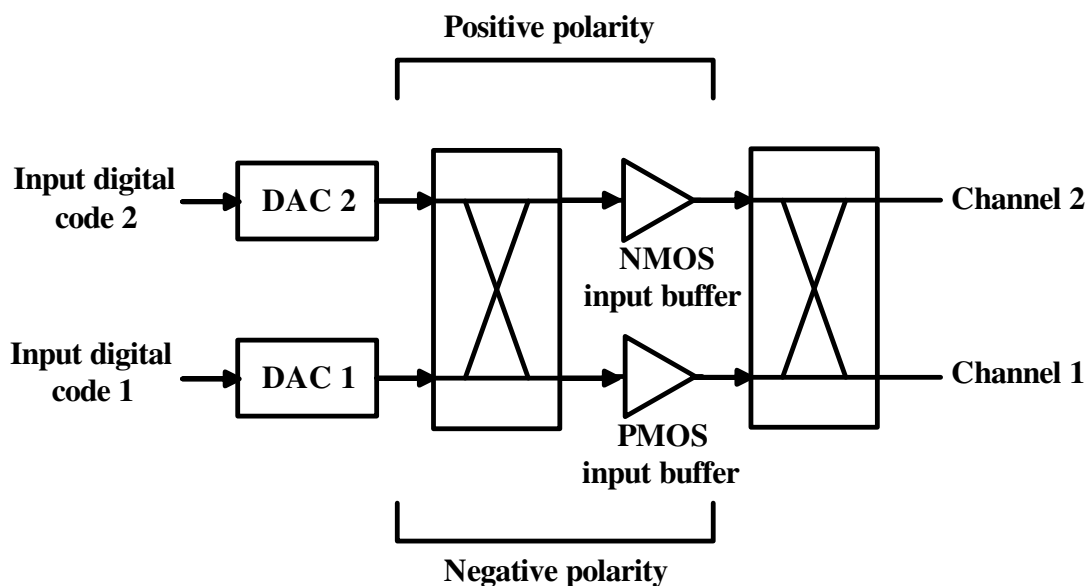


Fig.3.8 Proposed driving scheme [13].

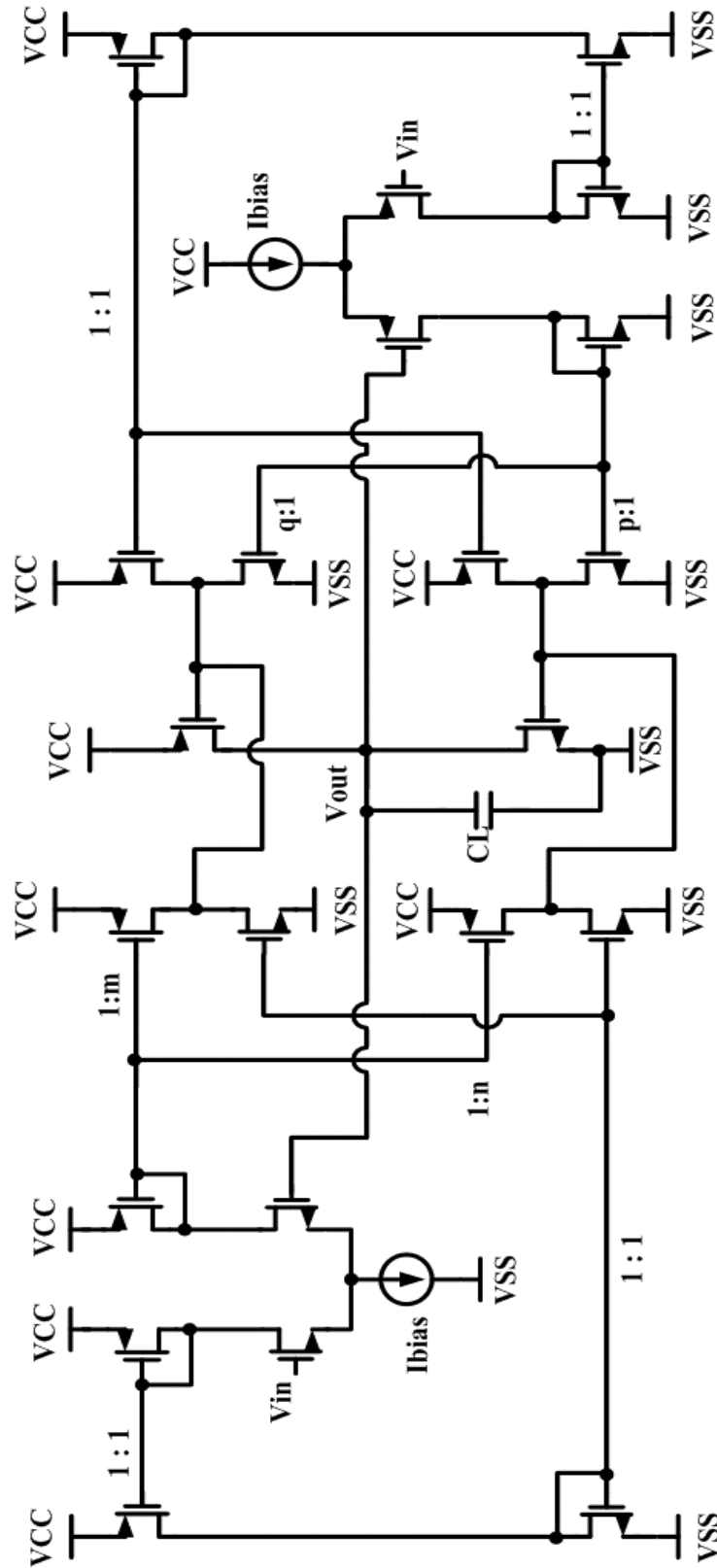


Fig.3.7 Complete circuit schematic of the rail-to-rail class-B output buffer [12].

3.4 Amplifier with Chopper Techniques

The example IC NEC- $\mu PD16721$ discussed in section 3.1 is an 8-bit resolution TFT-LCD data driver. In this thesis, the goal is to achieve a 10-bit high-resolution data driver. Since applying offset cancellation technology is necessary. There are several methods such as calibration, autozeroing, correlated double sampling, and chopper stabilization to reducing the offset voltage of opamp [14]. The most efficient, easily implement way is chopper techniques [15].

Fig.3.9 shows the chopping principle including signals in frequency and time domain. The input signal V_{in} is modulated to the chopping frequency, amplified and modulated back to the baseband. The offset is modulated only once and appears at the chopping frequency and its odd harmonics. These frequency components need to be removed by a low-pass filter. Next to the frequency domain, the chopping principle can also be explained in the time-domain. In that case, the input signal V_{in} is periodically inverted by the first multiplier or chopper. After amplification, the inverted and amplified signal is inverted for the second time, resulting again in a dc signal. The offset is periodically inverted only once and therefore appears as a square wave at the output. Finally, the low-pass filter can filter out the square wave.

In TFT-LCD data driver case, the output buffer is used to drive liquid crystal, which is effectively resistor and capacitor ladder strings as previously shown in Fig.3.3. Since it appears like a low-pass filter, it does not need an extra low-pass filter circuit at the output of the voltage buffer.

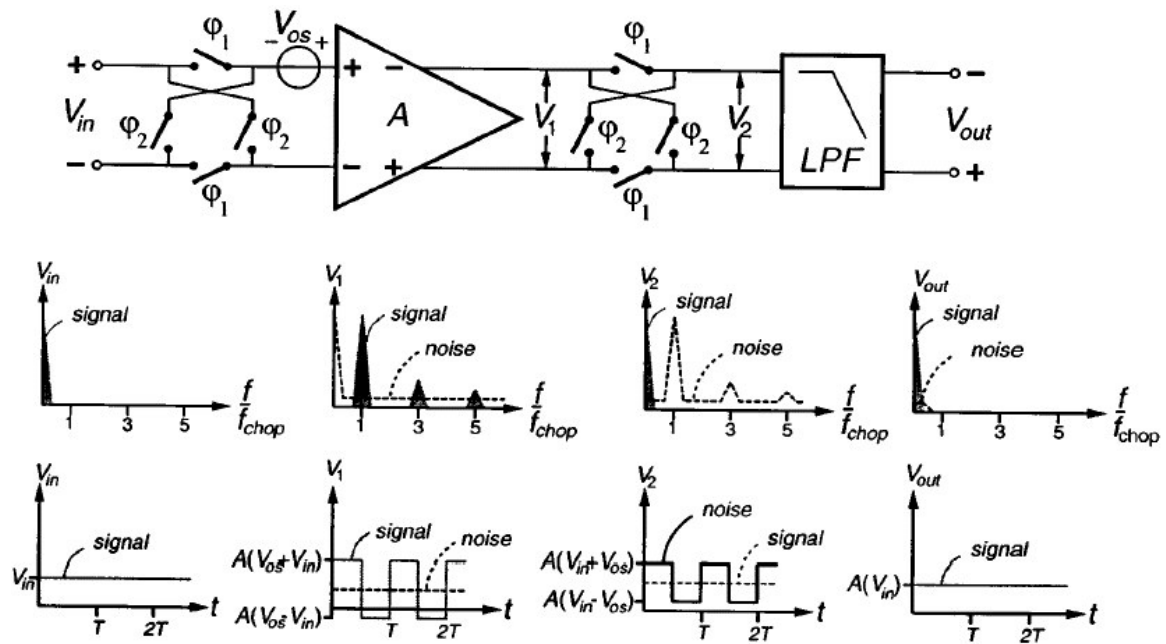
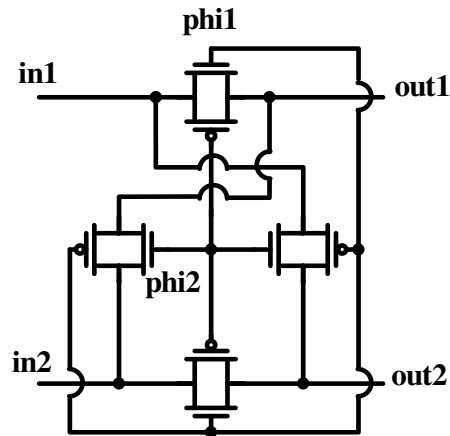


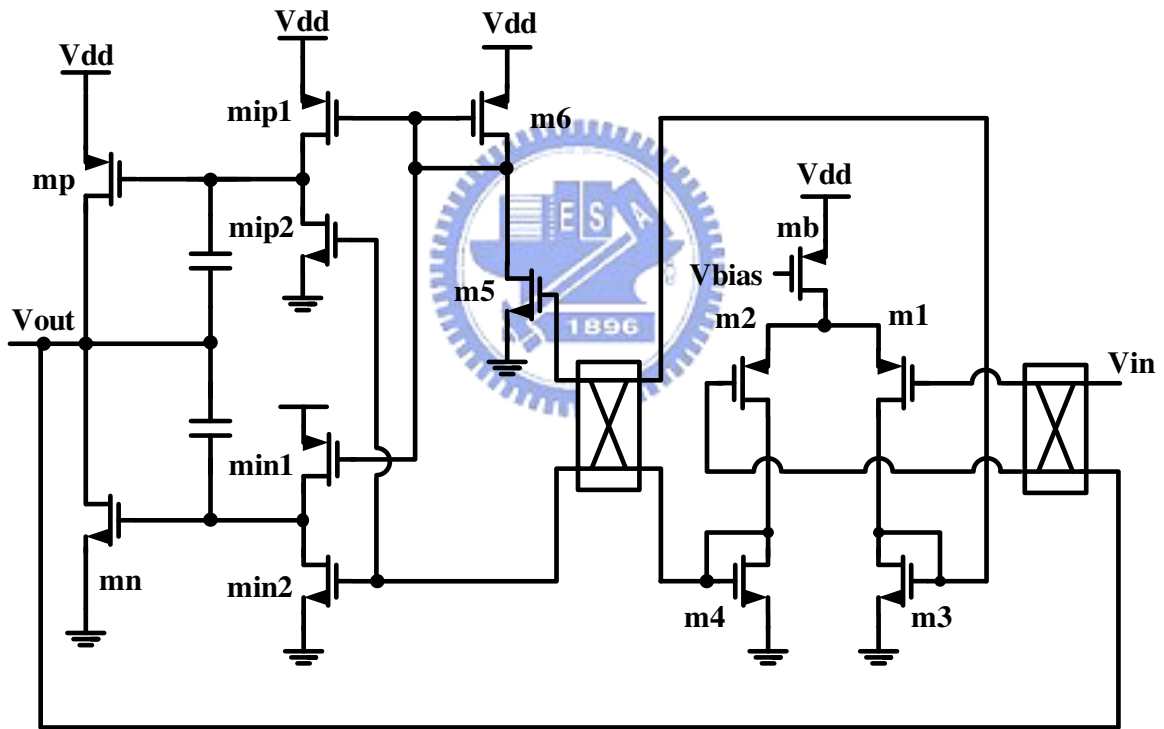
Fig.3.9 Chopping principle including signals in frequency and time domain [15].

3.5 High-Speed Low-Offset-Voltage Class-B Buffer with Chopper Techniques

Fig.3.10 illustrates the high-speed low-offset-voltage class-B buffer with chopper techniques. The basic class-B architecture is the same as discussed in section 3.3, and two choppers are added. At V_{in} , the input differential signal is chopped. The offset voltage is added at the differential pair, M1 and M2. When the differential signal is transformed into single end, the voltage signal is chopped again. Since the input voltage analog data is modulated back into baseband, and the offset voltage stays at high frequency, which would be filtered out due to the inherent low-pass filter characteristic of liquid crystal. This phenomenon can also be explained in time domain.



(a)



(b)

Fig.3.10 Architecture of class-B buffer with chopper techniques. (a) Chopper block circuit. (b) Complete circuit schematic of class-B buffer with chopper techniques.

3.6 Simulation Results

3.6.1 Simulation Results of High-Speed Class-B Buffer

In actual case, it is necessary to implement data driver IC in a 12-V HV-CMOS process in order to drive liquid crystal. But in this thesis, we only simulate and implement the PMOS input buffer in a TSMC 0.35 μm 6-V CMOS process because of lacking the resource of HV-CMOS process. For output voltage between 4.2V to 0.2V with 10-bit resolution, i.e., 1024 gray levels, the maximum allowed deviation of output buffers are calculated as followed:

$$\text{Voltage Range } V_R = 4.2V - 0.2V = 4.0V \quad (3-4)$$

$$\text{LSB} = \frac{4.0V}{1024} = 3.91mV \quad (3-5)$$

$$\frac{1}{2} \text{LSB} = \frac{3.91mV}{2} = 1.95mV \cong 2mV \quad (3-6)$$

Hence the goal is to design a class-B buffer with output deviation within 2mV.

The following figures show the simulation results. Fig.3.11 and Fig.3.12 show the dc values with V_{in} equals 0.2V and 4.2V (node i2 is connected to a current source which is not shown here). The maximum static current consumption is about $9.5 \mu\text{A}$ and the maximum output deviation is about 1.5mV, which both match our design goals. Fig.3.13 illustrates the dead zone simulation method, and Fig.3.14 and Fig.3.15 show the dead zone with input voltage equals 0.2V and 4.2V, respectively. Both dead zones are less than $\pm 2\text{mV}$.

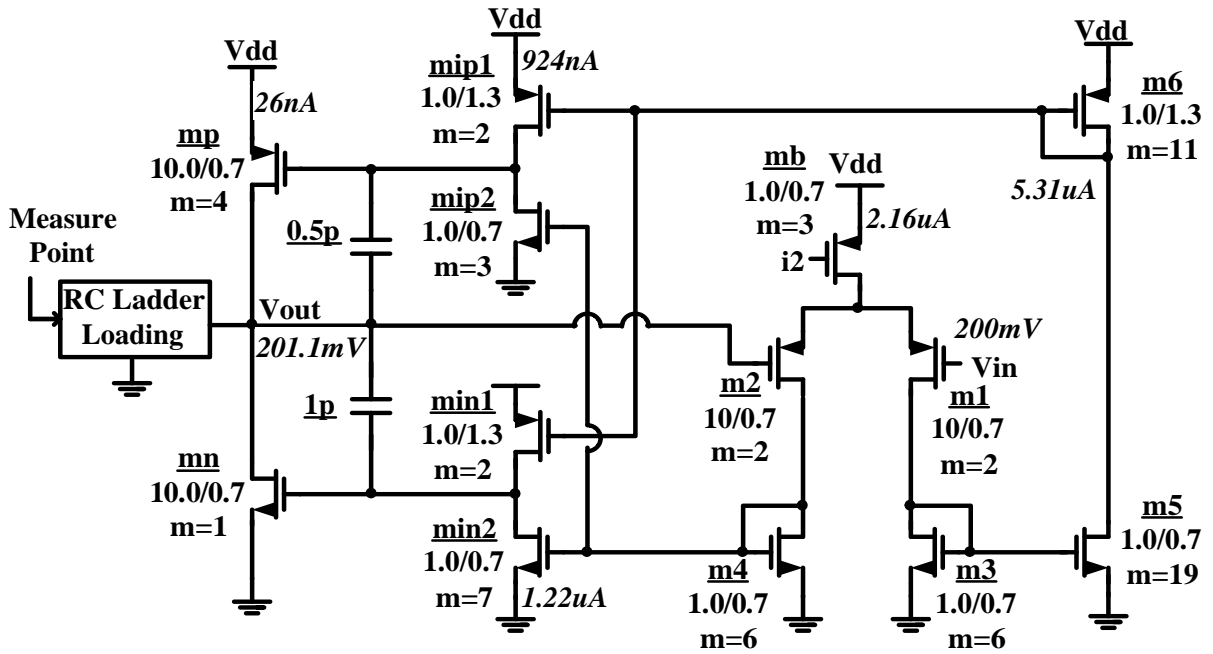


Fig.3.11 DC values of class-B buffer with V_{in} equals 0.2V.

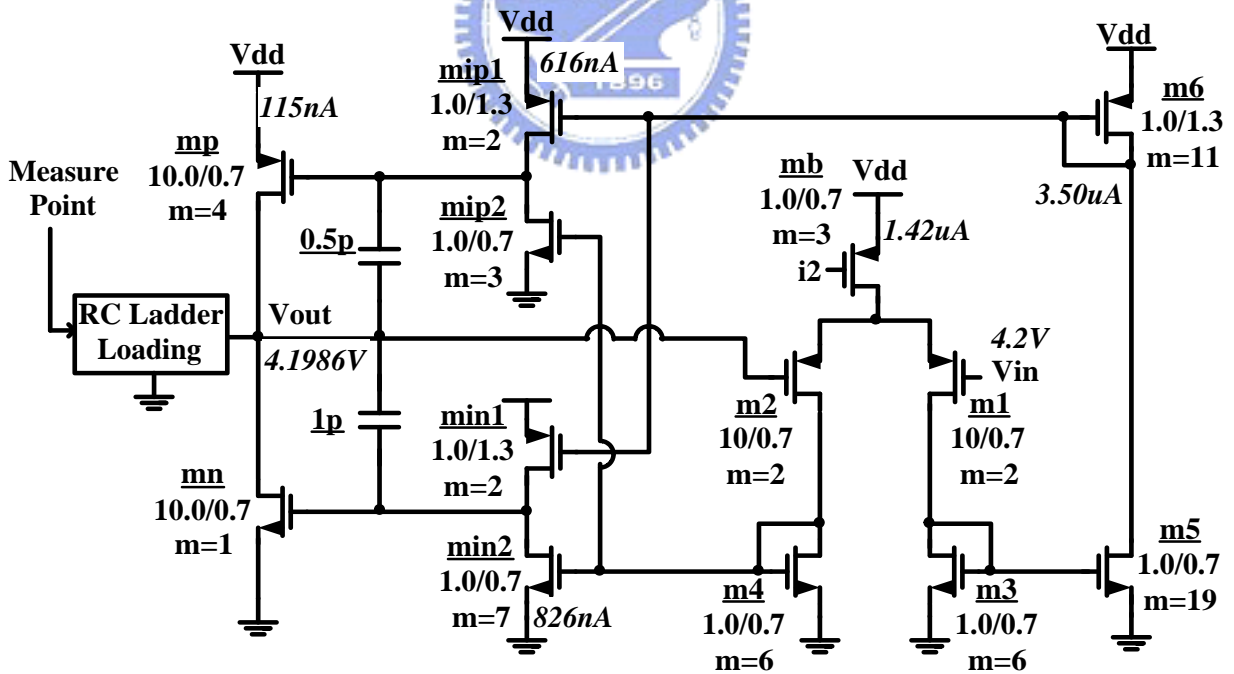


Fig.3.12 DC values of class-B buffer with V_{in} equals 4.2V.

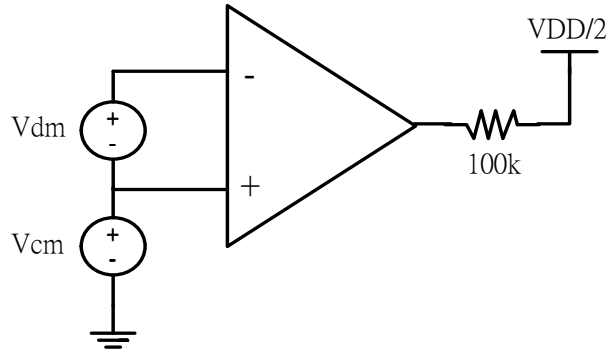


Fig.3.13 Dead zone simulation method.

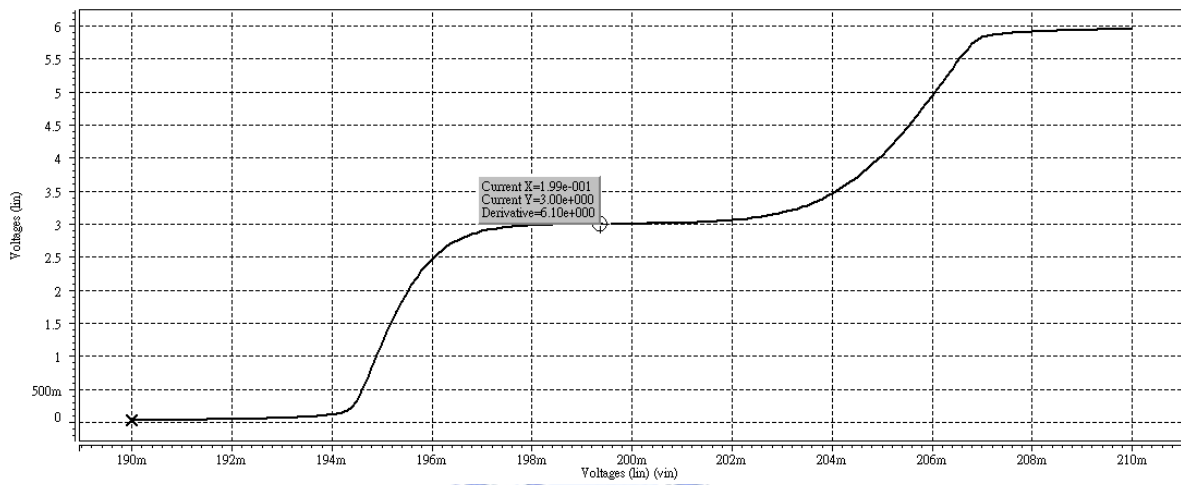


Fig.3.14 Dead zone with input voltage = 0.2V.

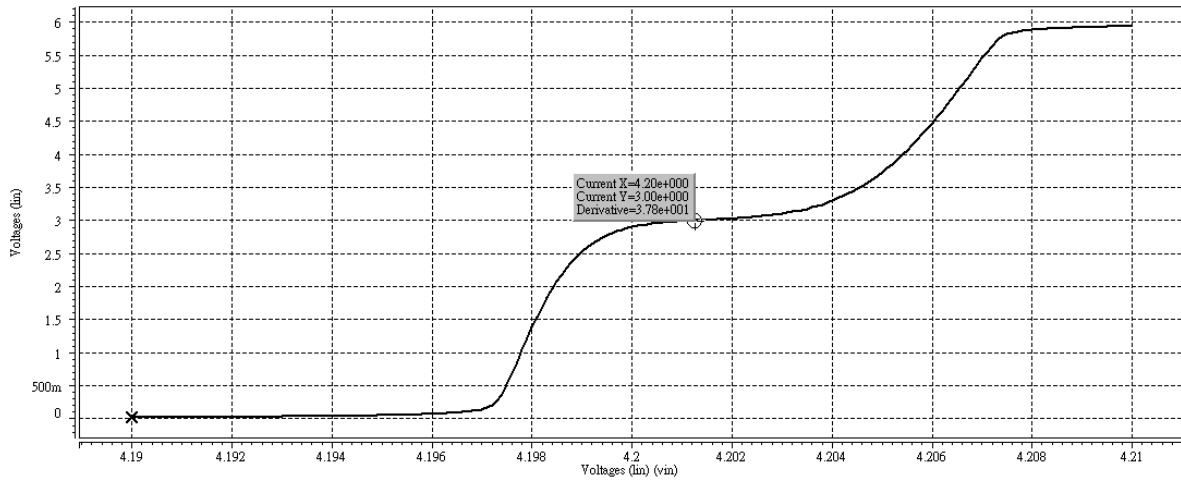


Fig.3.15 Dead zone with input voltage = 4.2V.

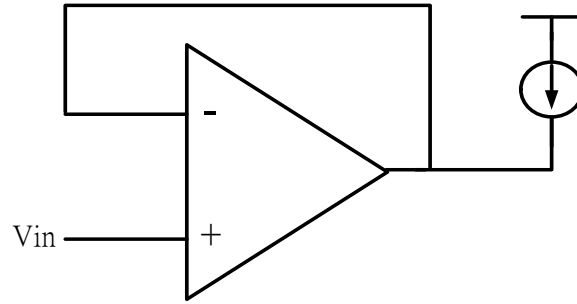


Fig.3.16 Alternative method to measure dead zone.

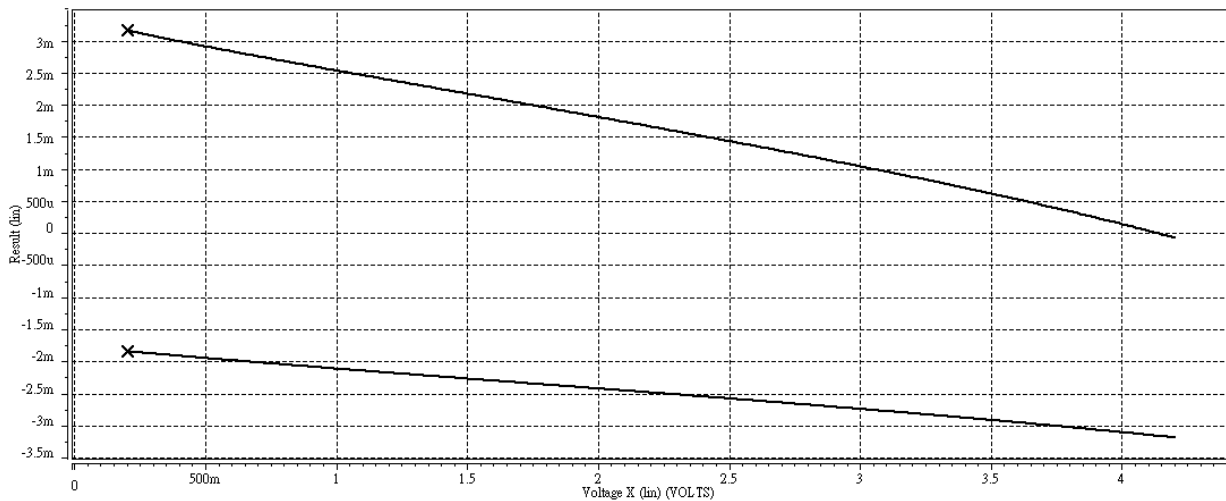


Fig.3.17 Dead zone of class-B buffer with $1 \mu A$ drawn at the output.

Fig.3.16 shows an alternative way to measure the dead zone of class-B amplifier, and the simulation results are illustrated in Fig.3.17. When the forced current at output is about $1 \mu A$, the offset voltage is within acceptable range.

To ensure the stability of this operational amplifier, the ac condition must be considered. Since the frequency response of charge and discharge are different, they need to be simulated and compensated separately. Fig.3.18 and Fig.3.19 show both the frequency response with different input condition. After compensation, the phase margin is quite enough to avoid oscillation.

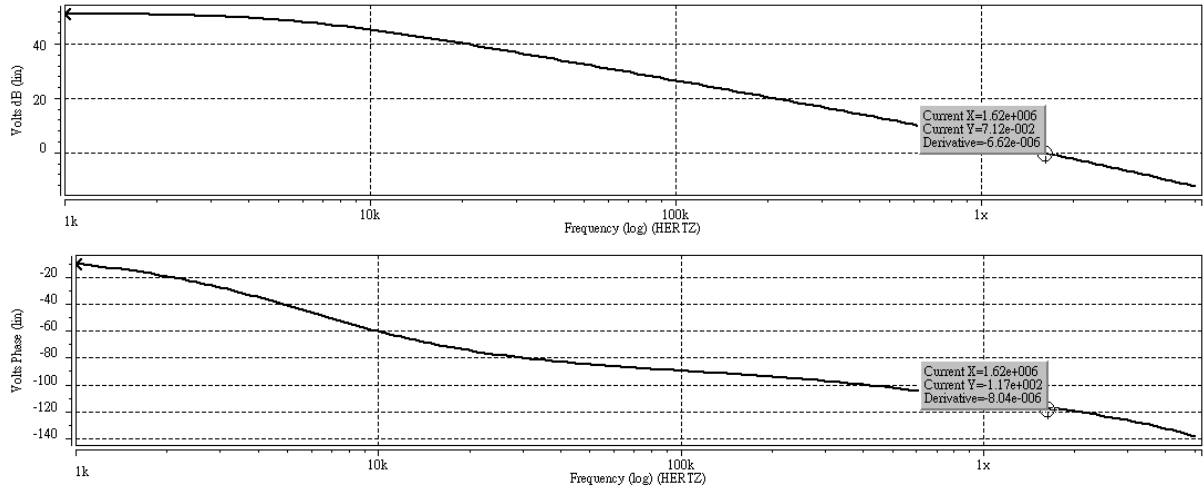


Fig.3.18 Frequency response with $V_{in}=3.196V$, $V_{in}=-3.2V$
 Bandwidth=1.62MHz, $PM=63^\circ$, DC gain=51.2dB.

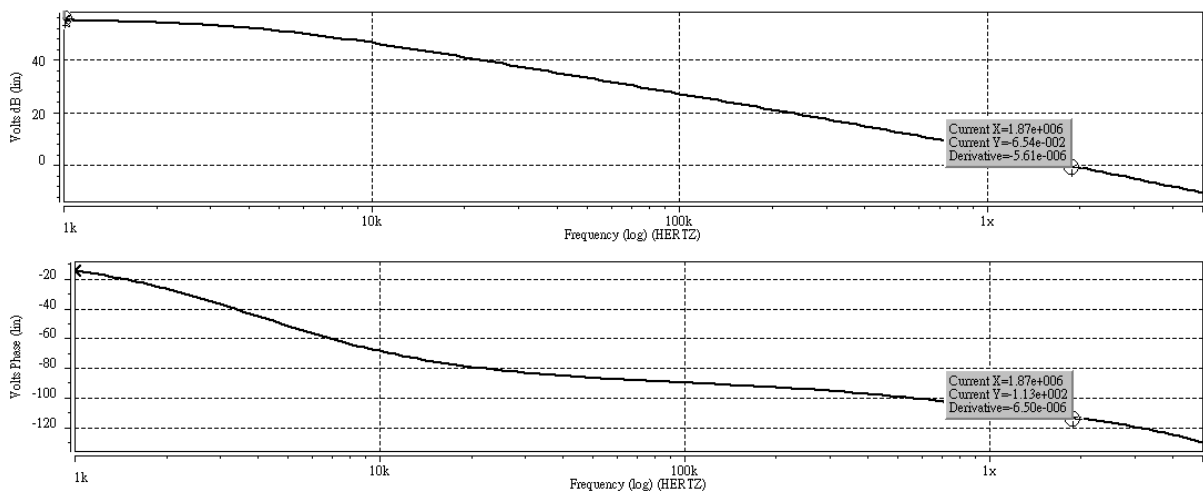


Fig.3.19 Frequency response with $V_{in}=3.2V$, $V_{in}=-3.207V$
 Bandwidth=1.87MHz, $PM=67^\circ$, DC gain=54.9dB.

Finally, the transient response is simulated with output loading discussed in Fig.3.3. The definition of settling time is that when the output and input voltage is within ± 2 mV deviation. Fig.3.20, Fig.3.21, and Fig.3.22 show the transient response simulation results. As a result, both rise settling time and fall settling time are in acceptable range.

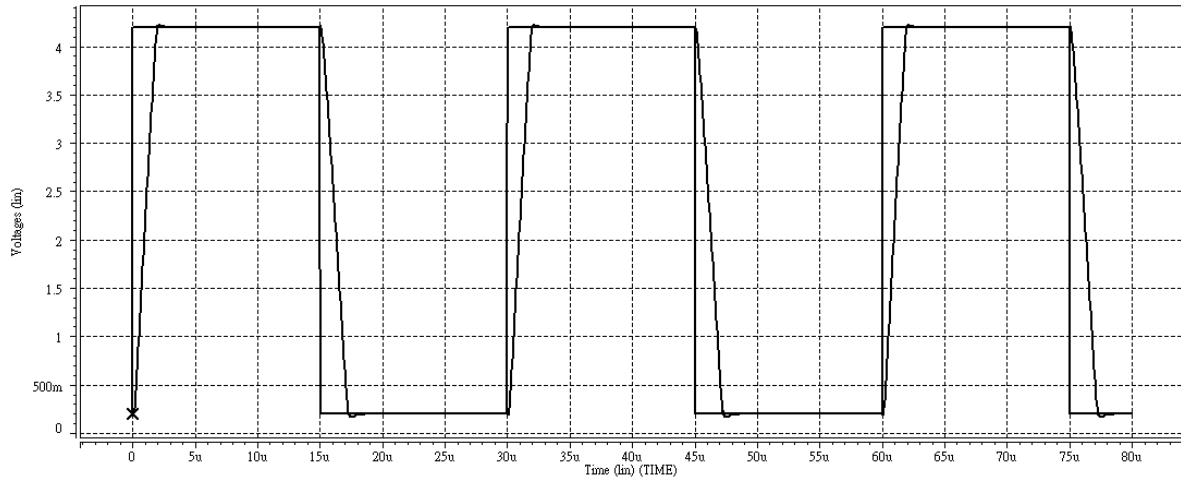
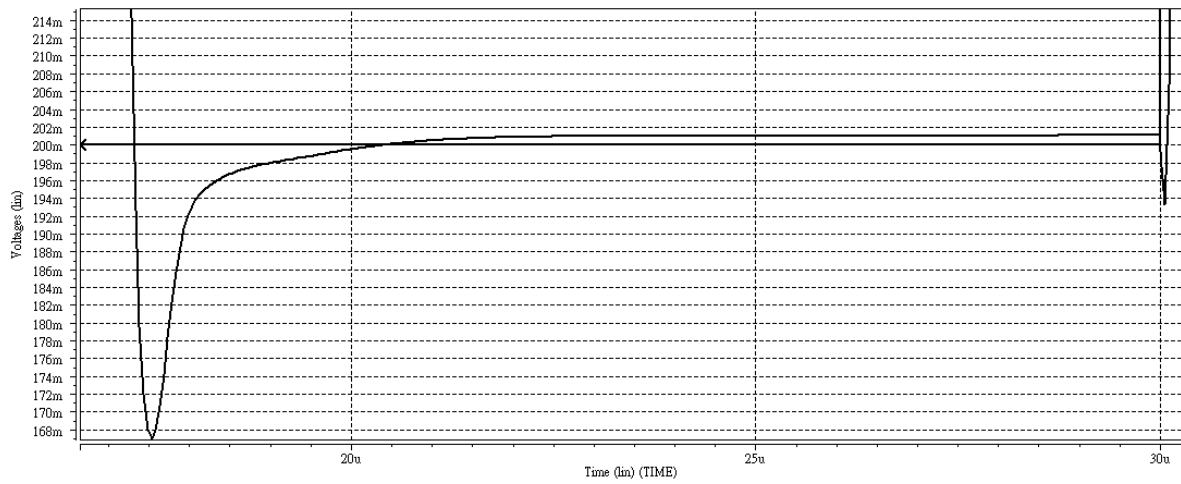
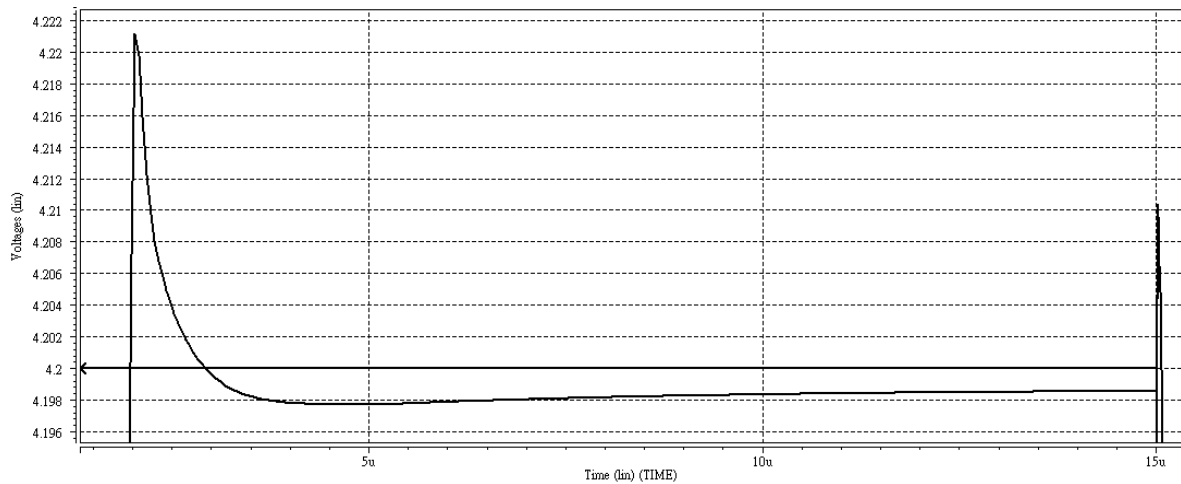


Fig.3.20 Transient response simulation results.



**Fig.3.21 Transient response with input=0.2V,
settling time = 4 μ s.**



**Fig.3.22 Transient response with input=4.2V,
settling time = 4 μ s.**

3.6.2 Simulation Results of Low-Offset-Voltage Class-B Buffer with Chopper Techniques

The circuit schematic of low-offset-voltage class-B buffer with chopper techniques is as shown in Fig.3.10. The input offset voltage 2.7mV is externally added, and the period of the two clocks, ph1 and ph2, are set equally twice the input signal. Since in time domain, the output voltage is input voltage plus offset voltage in first period, and input voltage minus offset voltage in second period, and so on as shown in Fig.3.23 and Fig.3.24, Fig.3.25 and Fig.3.26. This is an ac signal in frequency domain, which can be filtered out by the inherent low-pass filter characteristic of liquid crystals. When input signal equals 4.2V, the first output voltage is equal to 4.1957V and the second output voltage is equal to 4.2011V; the average voltage is equal to 4.1984V which is within ± 2 mV output voltage deviation. When input signal equals 0.2V, the result is similar, and the average voltage is equal to 200.975mV.

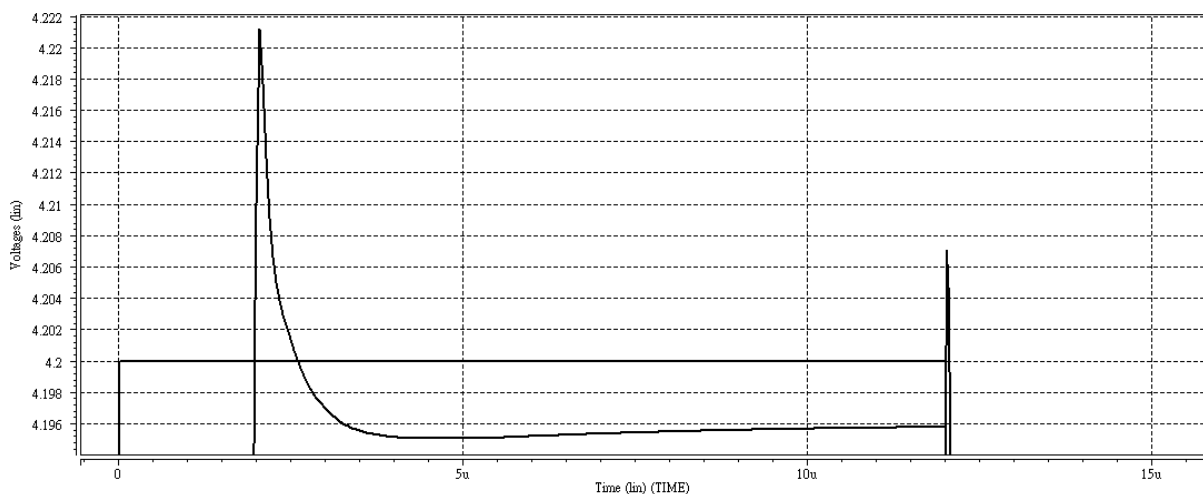


Fig.3.23 Transient response of first 4.2V, Vout = 4.1957V.

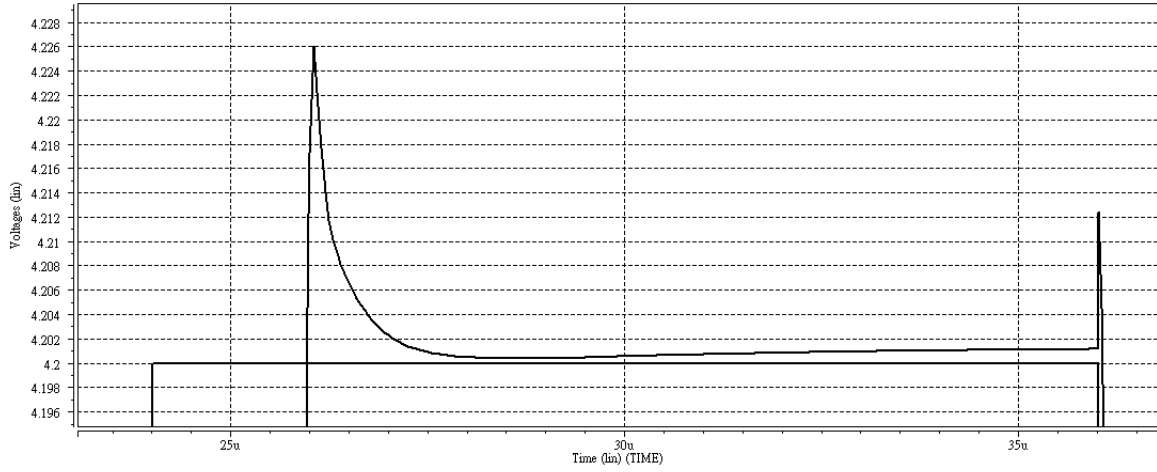


Fig.3.24 Transient response of second 4.2V, $V_{out} = 4.2011V$.

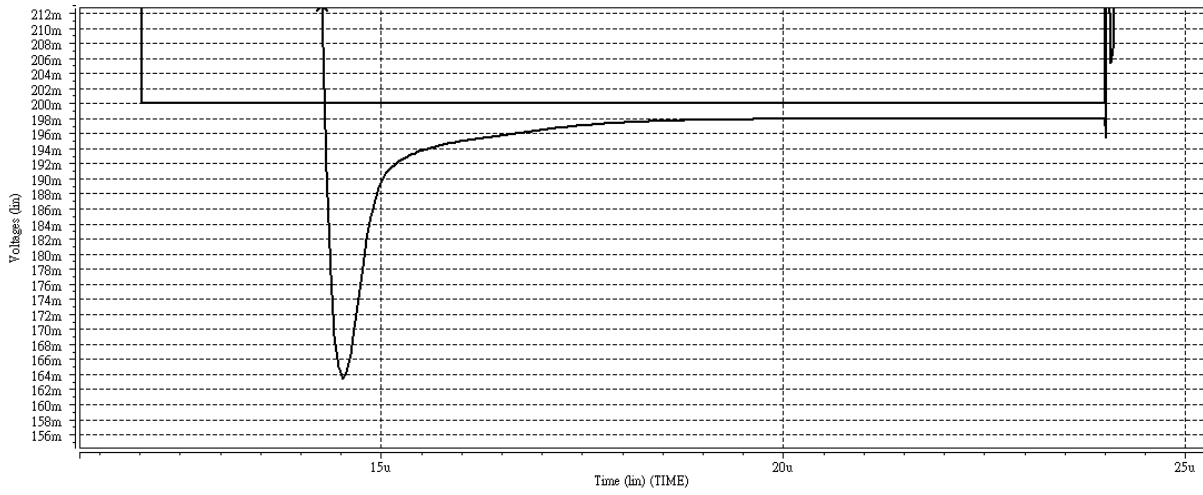


Fig.3.25 Transient response of first 0.2V, $V_{out} = 197.9\text{ mV}$.

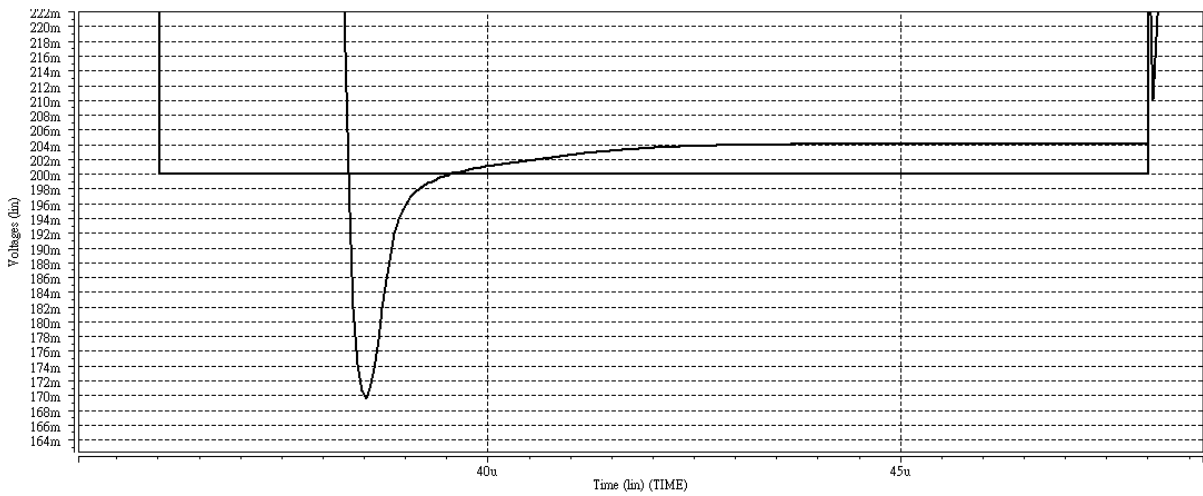


Fig.3.26 Transient response of second 0.2V, $V_{out} = 204.05\text{ mV}$.

CHAPTER 4

DIGITAL TO ANALOG CONVERTER AND CHARGE RECYCLING FOR DATA DRIVER

4.1 Gamma Correction

The Gamma Correction is needed because of the color sensitivity of human eye is not linear. If we apply a linear voltage to control the gray levels of a LCD panel, the human eye would consider it non-linear. Thus, the digital to analog converter (DAC) used in TFT-LCD data driver is necessary to be implemented with a modified T-V curve (Transparency-to-Voltage curve), which is so called “Gamma Correction”. Fig.4.1 shows an example of T-V curve and we can find the T-V curve is symmetrical to transparency axis [6]. The reason is the same as inversion driving method that is discussed in section 2.2.1, where a LCD panel should be driven by AC signals.

4.2 Digital to Analog Converter

There are several general types of digital to analog converter (DAC), which are voltage scaling DAC, charge scaling DAC, timing scaling DAC, and current scaling DAC. For TFT-LCD data driver, current scaling architecture wastes too much power and will not be discussed here. In this chapter, the three other types of DAC architecture will be discussed.

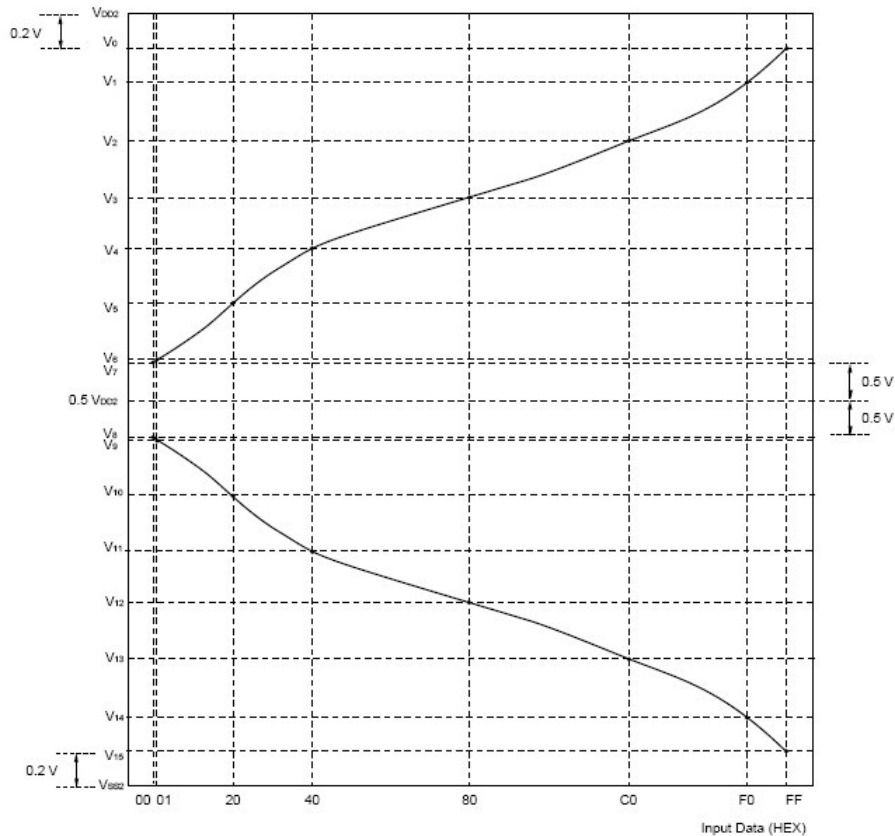


Fig.4.1 Transparency-to-voltage curve with γ -correction [6].

4.2.1 Voltage Scaling DAC

The theory of voltage scaling DAC is by using a resistor ladder, a given reference voltage (V_{ref}) can be divided into N segments. Fig.4.2 and Fig.4.3 illustrate two fundamental voltage scaling DAC architectures. The properties of the two architectures are compared below.

Common properties:

- Simple and monotonic
- Large chip size at higher bits.
- Good DNL and poor INL.
- Lower noise.
- Optimized Gamma Correction.

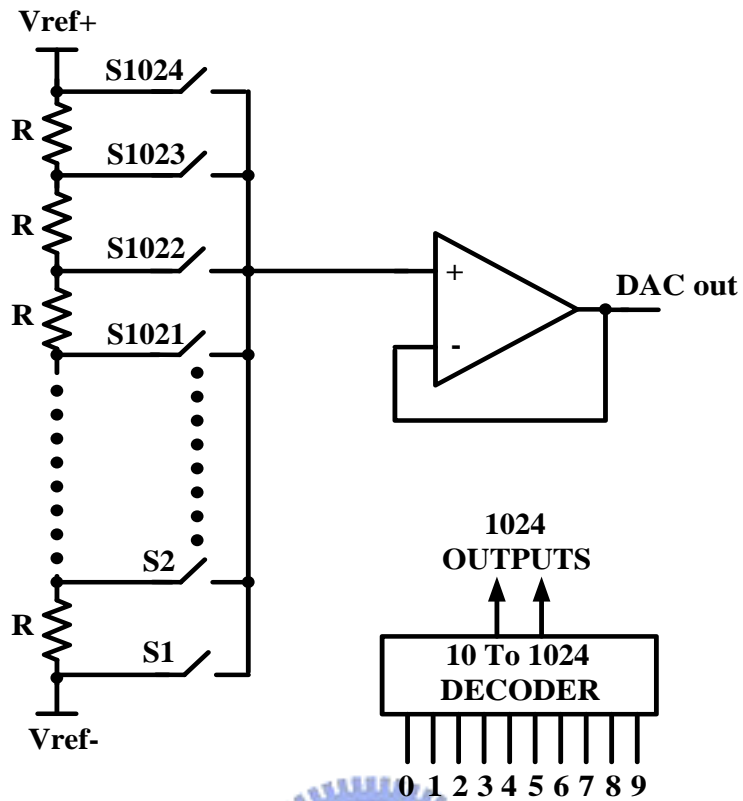


Fig.4.2 Voltage scaling DAC (1).

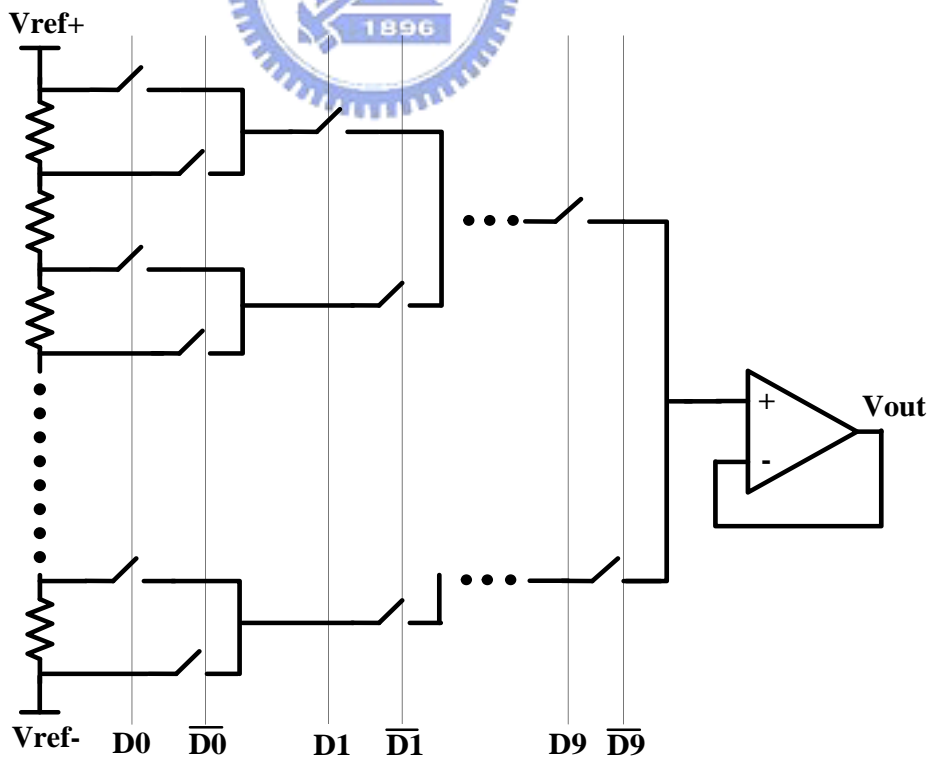


Fig.4.3 Voltage scaling DAC (2).

Different properties:

- Architecture in Fig.4.2 uses an n -to- 2^n decoder, where architecture in Fig.4.3 uses binary code.
- Delay time of architecture in Fig.4.2 is $2^n \times C \times R_{on}$, where in Fig.4.3 is $N \times R_{on} \times C \times 2$.

In TFT-LCD driver circuit design, there are hundreds of output voltage buffers in a single chip. If we want to display the same display data in all outputs, their voltage reference must be the same or there will be gray level differences. Also, for gamma correction, voltage scaling DAC is the easiest way to implement different segments. For higher bits applications, decoders in Fig.4.2 would be too huge to implement for TFT-LCD layout. For TFT-LCD applications, its layout width must be within $60 \mu\text{m}$. Chip area and operational speed of architecture in Fig.4.3 is similar to Fig.4.2, but its width can be implemented in $60 \mu\text{m}$. Thus, in this thesis, voltage scaling DAC in Fig.4.3 is decided.



4.2.2 Charge Scaling DAC

As voltage scaling DAC, a reference charge can be divided into N equal packets by using N identical capacitors. A conventional charge scaling DAC is illustrated in Fig.4.4. In this circuit, it has two steps. The capacitors storage the reference voltage first, and then transfer the charge to output capacitor. By this operation, the output voltage can be determined by the following equation:

$$V_0 = V_{ref} \times \frac{C}{2^N C} \times \sum_{i=0}^{N-1} b_i 2^i \quad (4-1)$$

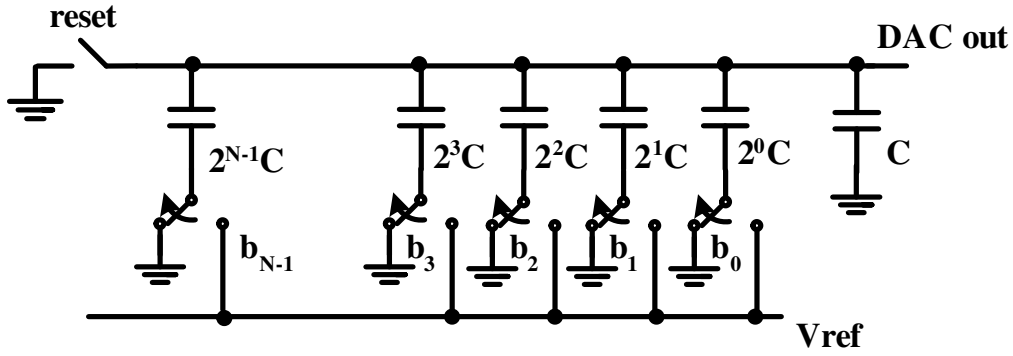


Fig.4.4 Charge-Redistribution DAC.

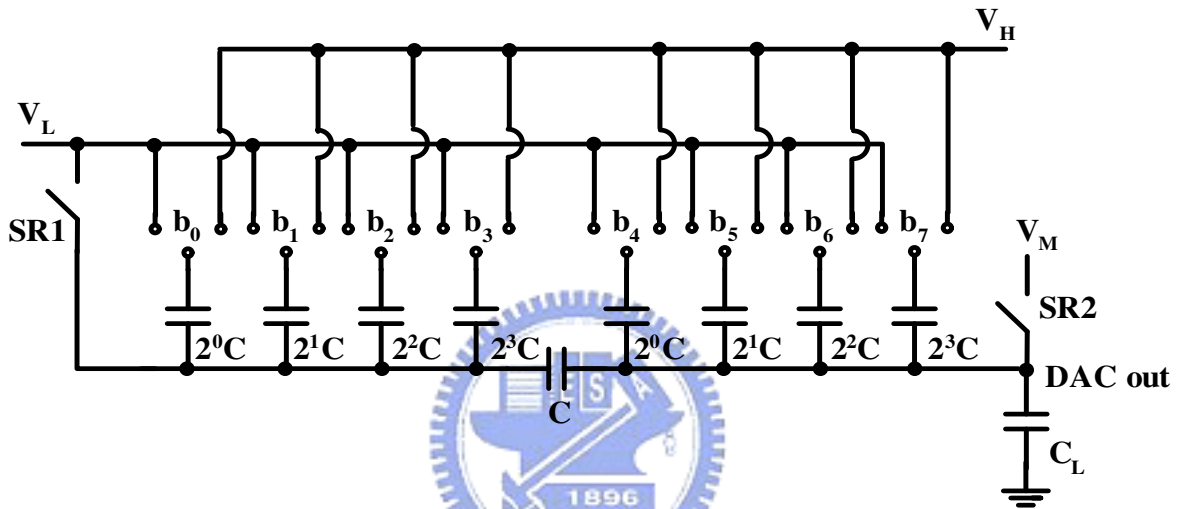


Fig.4.5 Two-step charge scaling DAC.

As we can see from Fig.4.4, this circuit has a big disadvantage, large size at higher bits. Therefore, an alternative architecture called two-step charge scaling DAC which can solve this problem is illustrated in Fig.4.5. The operation method of this circuit is similar as conventional DAC. Take 8-bit DAC as an example, the output voltage of this circuit can be also determined by (4-2):

$$V_{OUT} = V_M + \alpha \times \frac{\sum_{i=0}^7 b_i \times 2^i}{255} (V_H - V_L)$$

where $\alpha^{-1} = 1 + \left(\frac{16}{255}\right) \times \left(\frac{C_L}{C}\right)$ (4-2)

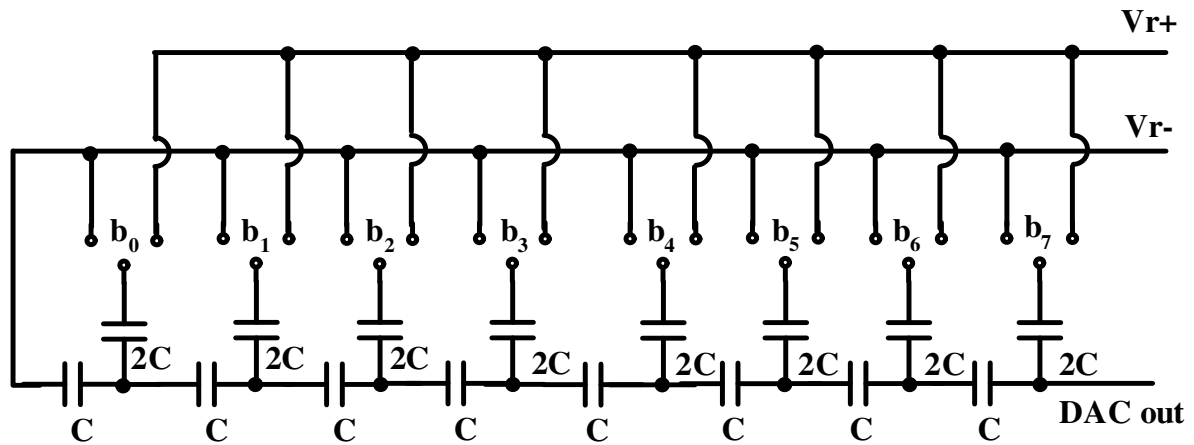


Fig.4.6 C-2C charge scaling DAC.

Besides these two circuits, there is another type of architecture that can reduce more chip size, called C-2C DAC which is shown in Fig.4.6. In summary, all of them have some advantages better than voltage scaling DAC. First, the matching for capacitor is better than resistor ladder. Second, the charge scaling can save more power. But they have several problems in TFT-LCD applications. First, the reference voltage of all output voltage buffers cannot be implemented identically by using charge scaling DACs. Second, all of them are very difficult to achieve gamma correction. From the above discussions, charge scaling DACs are not applied in this thesis.

4.2.3 Time Scaling DAC

In Fig.4.7, a diagram about the concept of time scaling DAC is illustrated. In this architecture, a ramp source that can be distributed to many parallel DAC, and this ramp source drives several DAC simultaneously. As the ramp increases, the data line is slowly charged by the ramp. When the voltage of the data line reach the desired voltage, the data line is disconnected from the ramp source by the DAC, and the data

line holds the proper voltage. At the beginning of the next conversion, the ramp source is reset and repeats the same process. The DAC is just like a switch that controls the time of connection between ramp source and data line. Therefore, the different voltage can be controlled by the different connection time.

As discussed above, the major advantage of this architecture is consistency across all parallel data line, but it also has a major disadvantage, speed. First, the loading of ramp source is very large. Second, if the pixel resolution is too high, the slope of the ramp would be much sharper. Therefore, this architecture isn't suitable for high resolution and large size TFT-LCD applications.

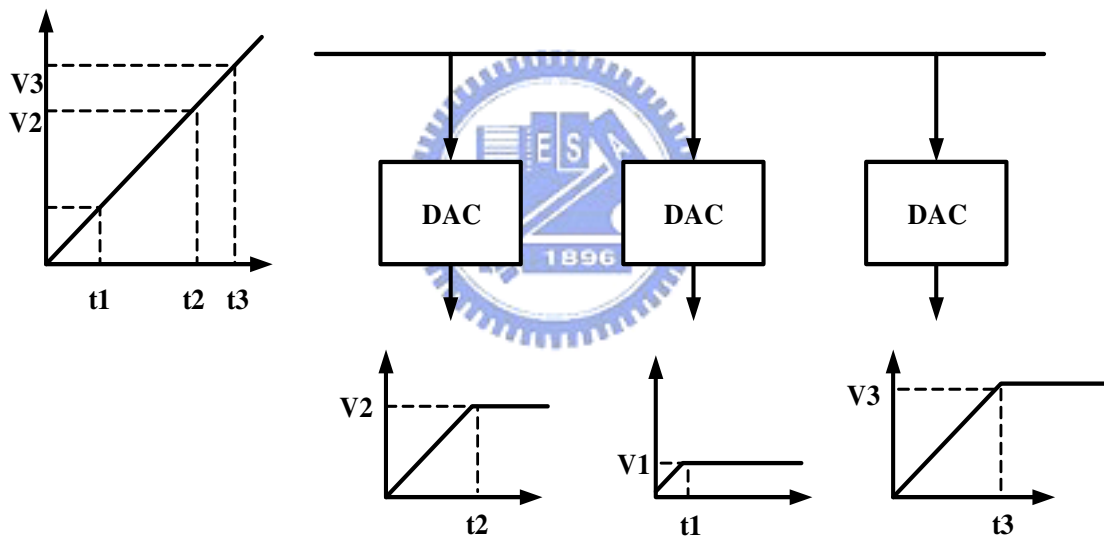


Fig.4.7 The concept of time scaling DAC.

4.3 Low Power Design Consideration

The power dissipation for an electronic system has four sources:

- **Dynamic power** is the result of charging capacitances in the circuit such as wires and transistor gates. It is governed by the following equation[16]:

$$P_{dyn} = \alpha_{0 \rightarrow 1} f C V^2 \quad (4-3)$$

where $\alpha_{0 \rightarrow 1}$ is the fraction of clock periods in which component switches from a logical zero to one.

- **Short circuit power** is the result of resistive paths from power to ground while circuits are transitioning.
- **Static power** is the result of resistive paths from power to ground when circuits are not transitioning.
- **Leakage power** is the result of reverse bias between diffusion regions and substrate.

In this thesis, dynamic power is focused. To reduce dynamic power, charge recycling method is applied.

4.3.1 Half Charge Recycling

Fig.5.1 and Fig.5.2 illustrate a circuit and simulation waveform of the half charge recycling. In dot or column inversion, the voltages of the neighboring data lines are alternated every row line time to inverse polarity. Therefore, the adjacent data lines are shorted together before the gray scales decision. Adjacent data lines share their charges and their voltage would become the average voltage of all data lines. Thus, the voltage swing is reduced to the half of that of the conventional data driver, and driver circuits could save about 1/2 power consumption.

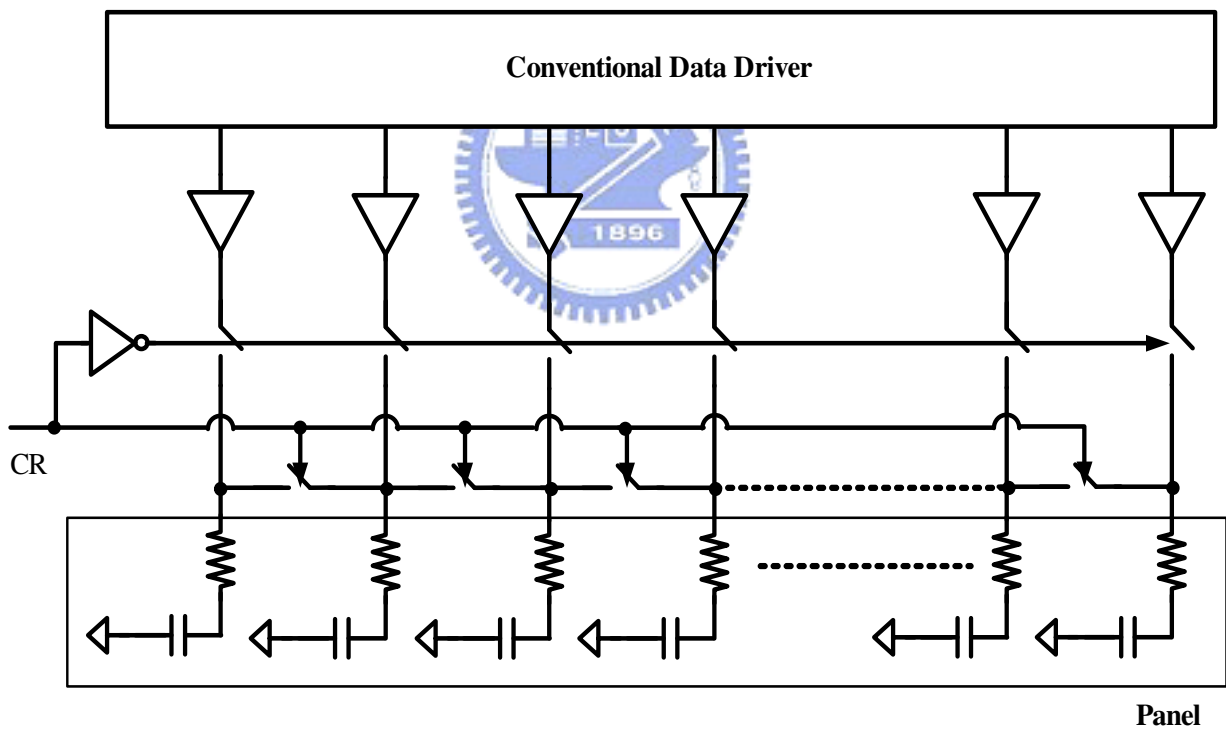


Fig.4.8 The circuit diagram of the half charge recycling.

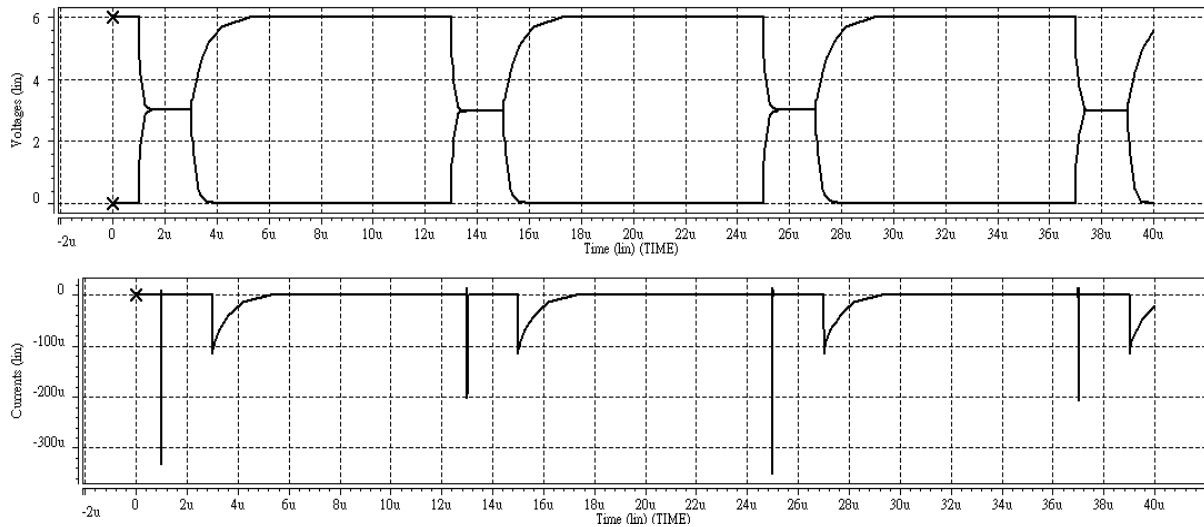


Fig.4.9 Waveform of the half charge recycling and its current consumption.

4.3.2 Triple Charge Recycling

Fig.5.3 shows a circuit of the triple charge sharing. In this circuit, an external large capacitor is needed, $C_{EXT} \gg N \times C_L$, where N is the number of the data lines. The input signal is shown in Fig.5.4, and its operation of the triple charge sharing is shown in Fig.5.5. First, the external capacitor is supposed to have been charged to $V_L + (1/3)V_{SWING}$. During the first charge sharing, SEL1 is high, the even-numbered data lines are shorted to C_{EXT} and charged to $V_L + (1/3)V_{SWING}$. And then all the output data lines would share the charge and change the voltage to $V_L + (2/3)V_{SWING}$. Finally, the odd-number data lines are shorted to external capacitor and the voltage of data line would discharge to $V_L + (1/3)V_{SWING}$. Meanwhile, the odd-numbered data lines would recover the charge of external capacitor. After charge sharing, the data driver drives the data line. Then the voltage swing is reduced to the third of that of the conventional data driver, thus driver circuits can save 2/3 power consumption.

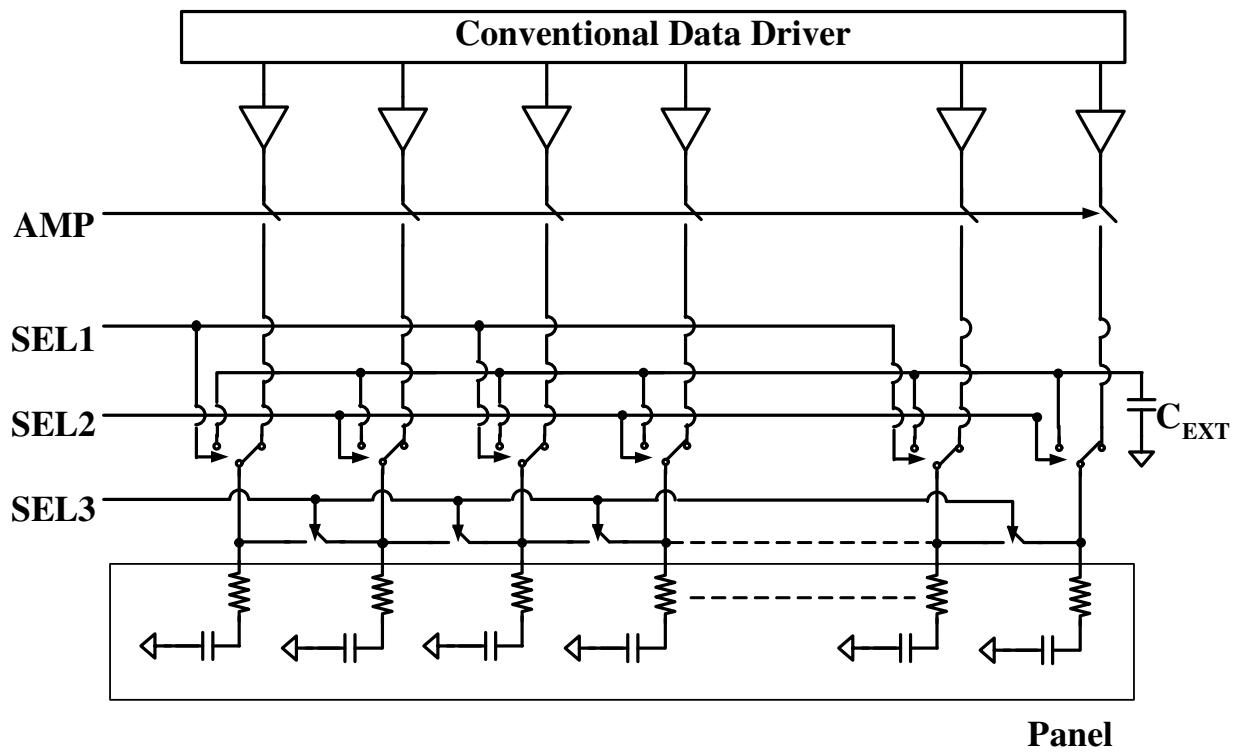


Fig.4.10 The circuit diagram of the triple charge recycling.

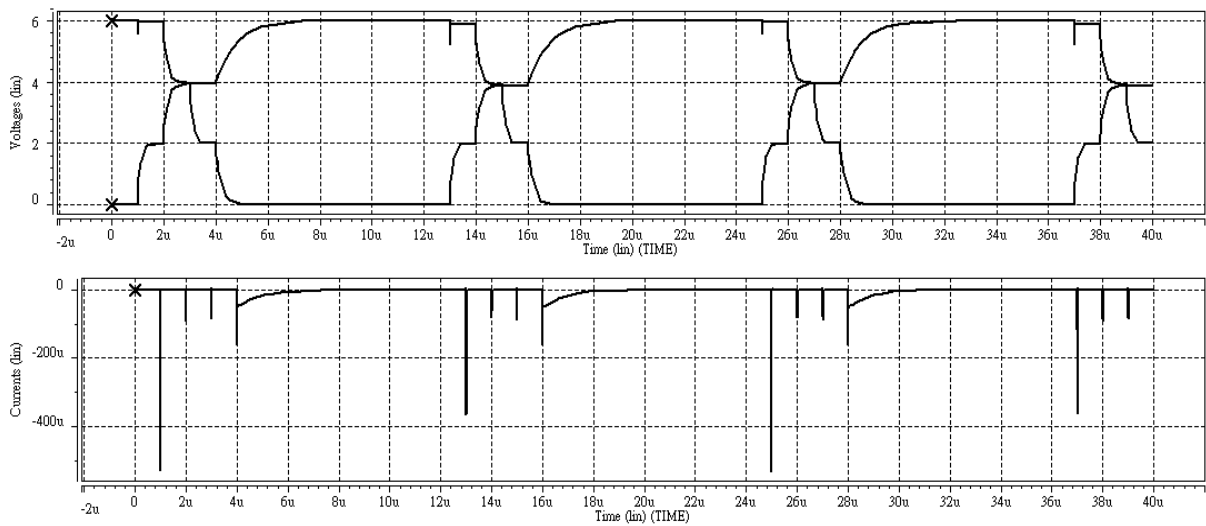


Fig.4.11 Waveform of the triple charge recycling and its current consumption.

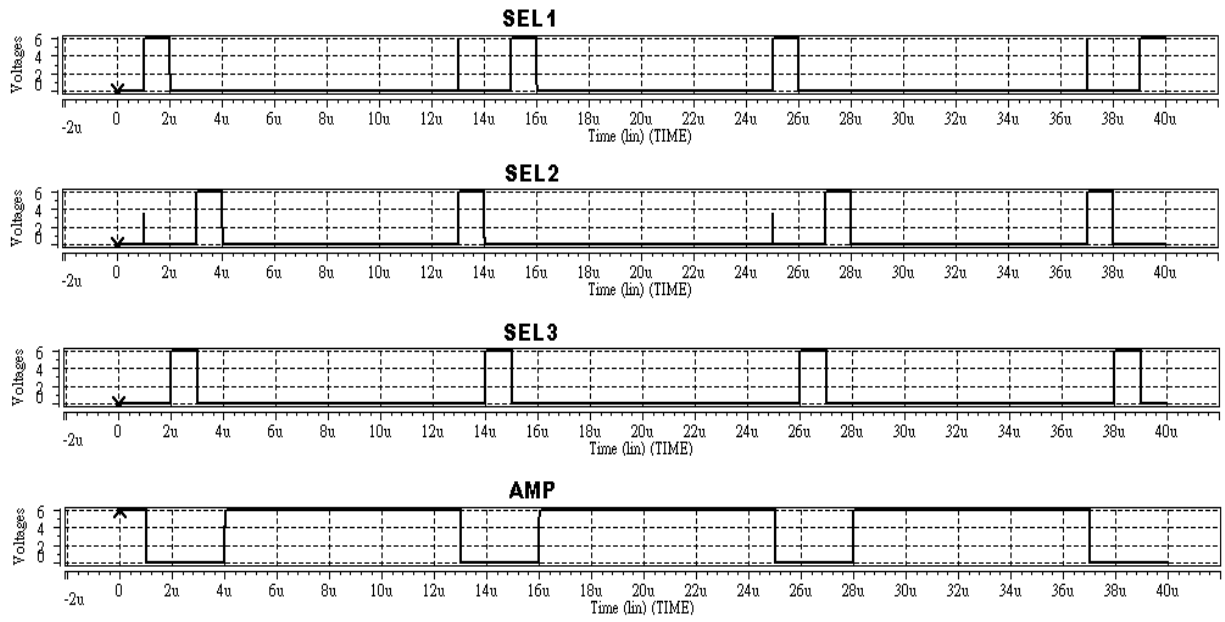


Fig.4.12 Input waveform of the triple charge recycling.



CHAPTER 5

CIRCUIT LAYOUT AND MEASUREMENT RESULTS

5.1 Layout Considerations

The circuits for data driver that was discussed in previous sections, the output buffer, the output buffer with chopper cancellation, voltage scaling DAC, charge recycling are designed and layout. All of these circuits have been designed as testkey. The purpose of designing testkey is to measure the separate performance and see whether it works. By modifying and refine these circuits, whole data driver can be composed. All circuits are fabricated in a TSMC $0.35\ \mu\text{m}$ CMOS technology.

Fig.6.1 shows the layout of input differential amplifier. Here we use dummy, guard ring, and layout symmetrically to reduce input offset voltage. Fig.6.2 shows the layout of feedback capacitor, which is symmetric with dummy. Fig.6.3 shows the whole voltage buffer, where its width must be within $60\ \mu\text{m}$ since we have 384 output pins on a single driver IC. Fig.6.4 shows the layout of 10-bit DAC, where its width is also less than $60\ \mu\text{m}$ although its height is quite long. The layout of whole chip is shown in Fig.6.5. Since all the circuits are implemented on a single chip, power supply pads and ground pads of all circuits are separated to avoid crosstalk. Fig.6.6 illustrates the layout floorplain.

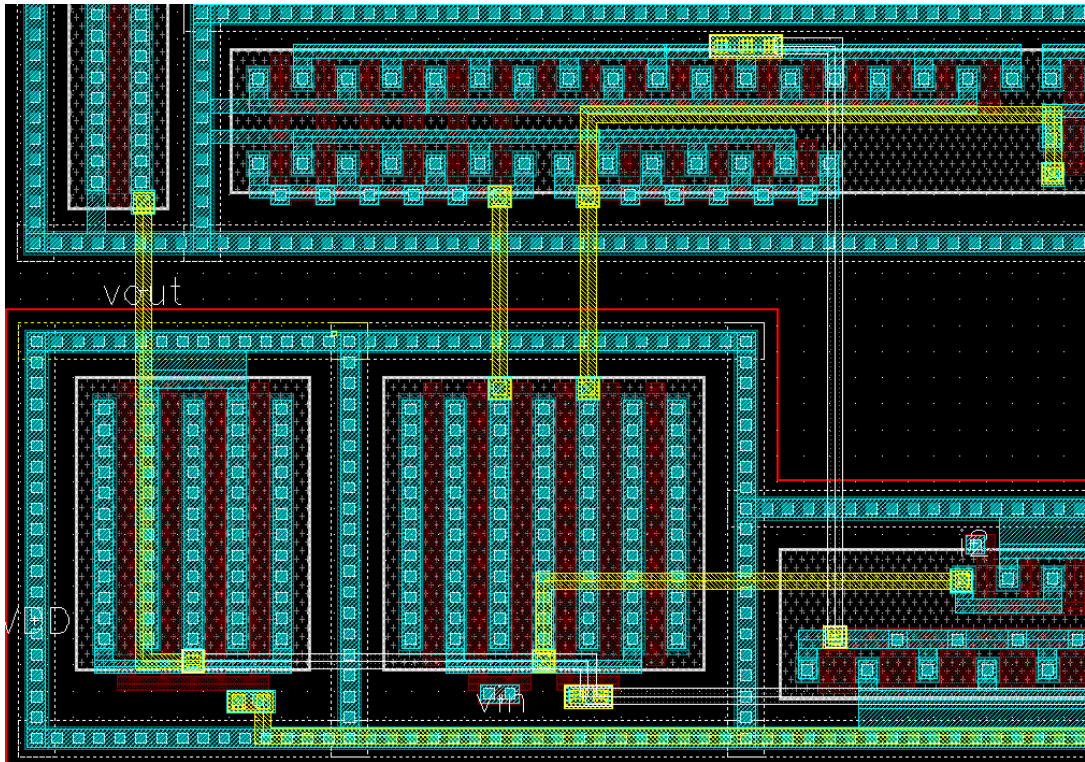


Fig.5.1 Layout of input differential amplifier.

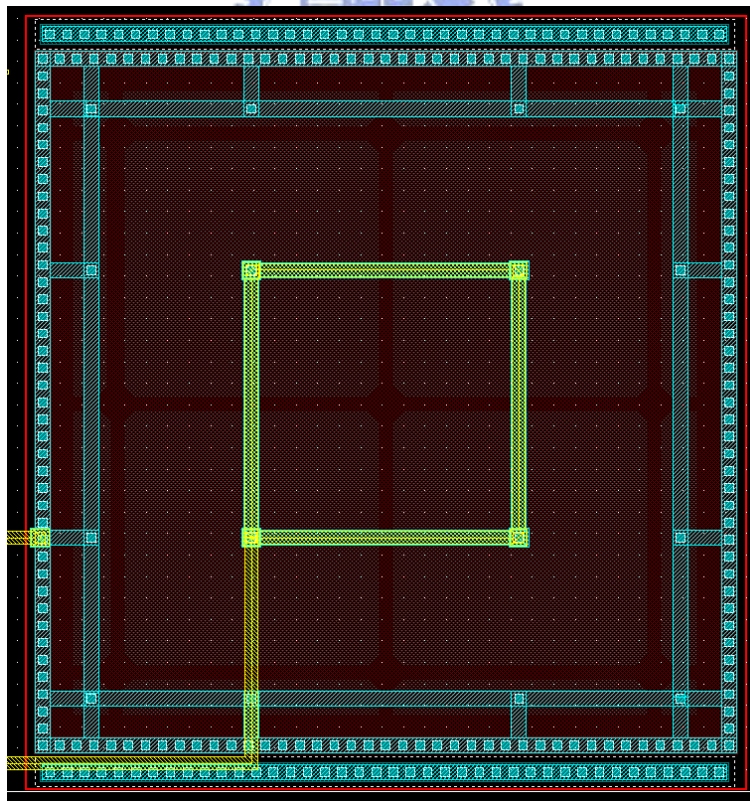


Fig.5.2 Layout of feedback capacitor.

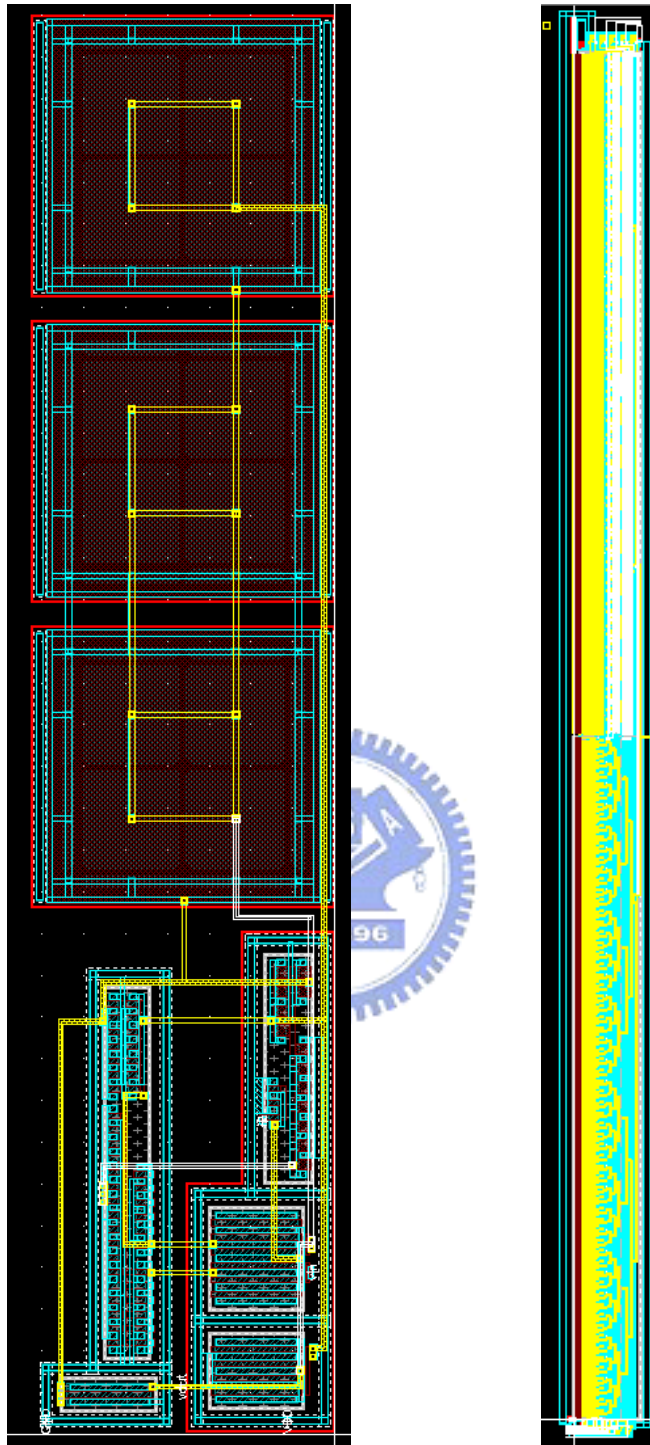


Fig.5.3 (Left figure) Layout of whole voltage buffer.

Fig.5.4 (Right figure) Layout of 10-bit voltage scaling DAC.

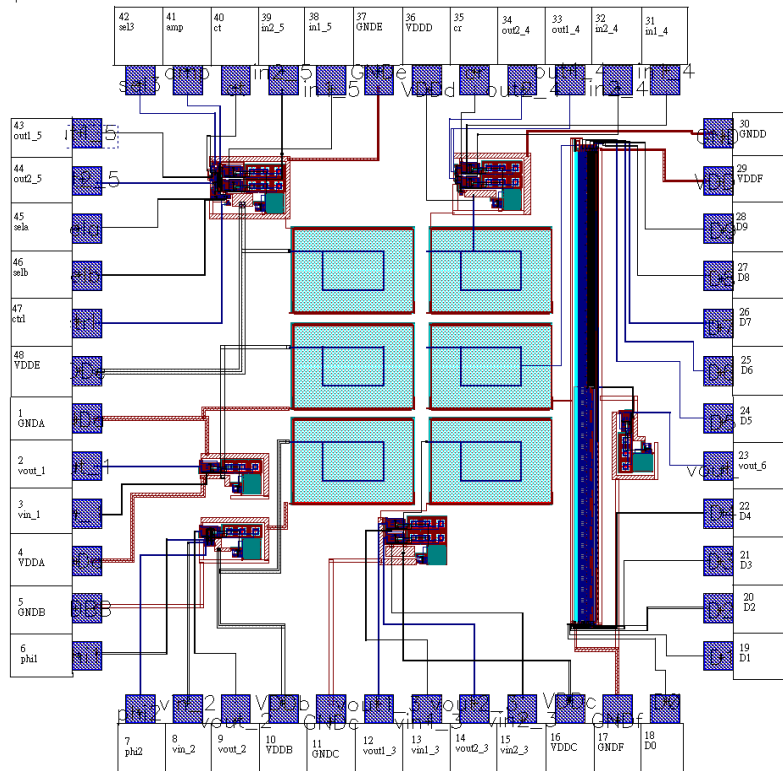


Fig.5.5 Layout of whole chip and pad names.

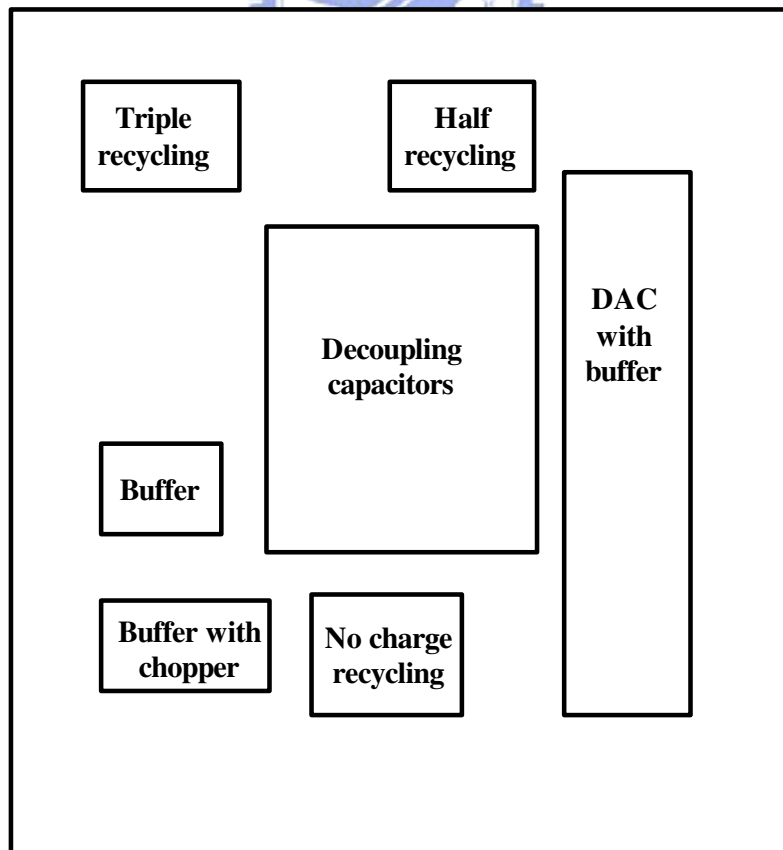


Fig.5.6 Layout floorplan.

5.2 Measurement Results

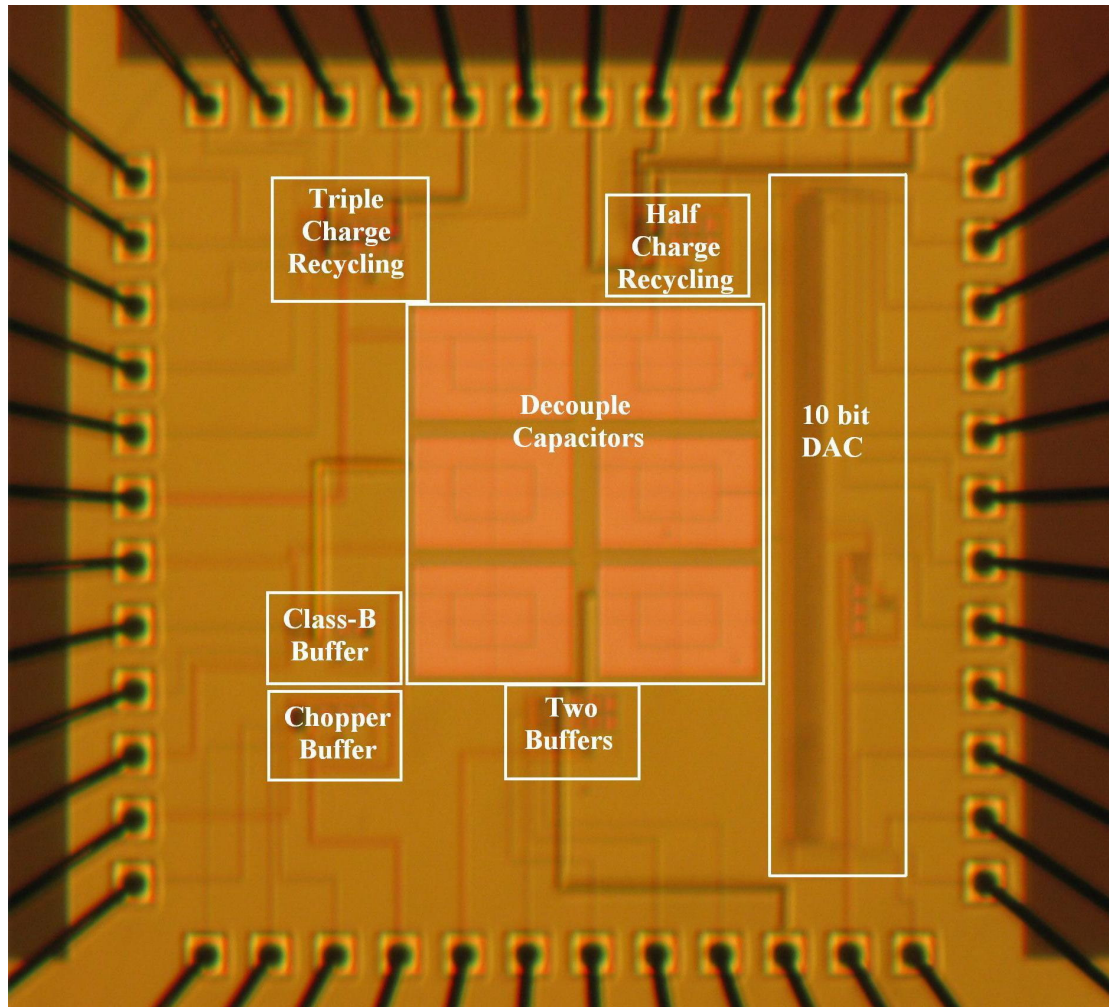
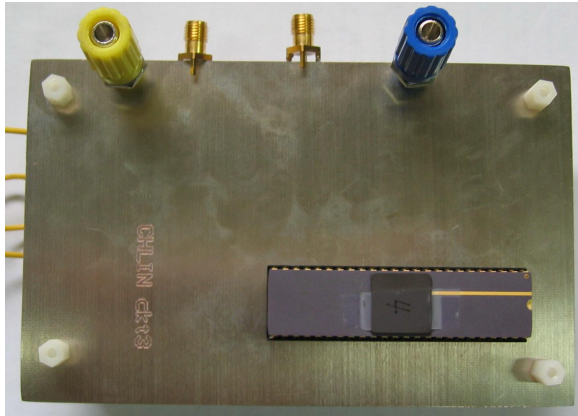
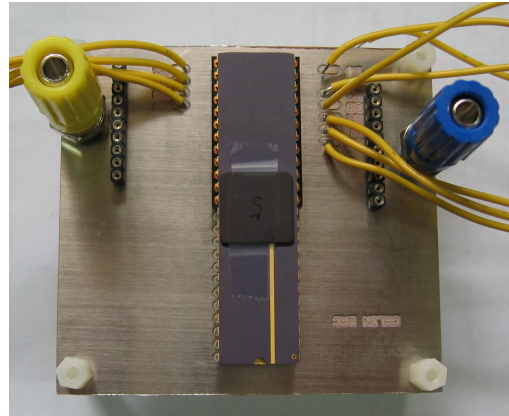


Fig.5.7 Chip die photo.

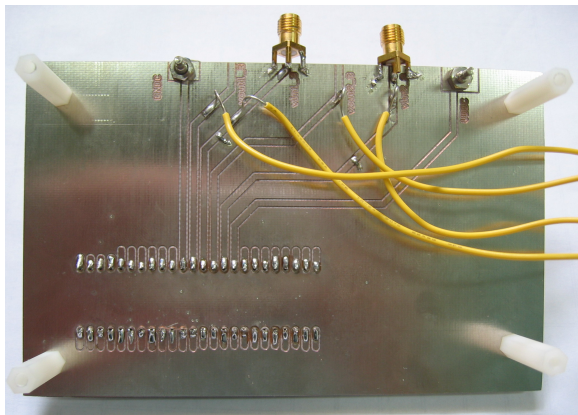
Fig.5.7 shows the die photo of this implemented IC. There are six major parts of this chip, which are Class-B buffer, Class-B buffer with chopper techniques, Two buffers without charge recycling, 10-bit digital to analog converter, Half charge recycling and Triple charge recycling. All above circuits are measured on different PCBs, and measurement environments are carefully set up. Fig.5.8 shows several measurement PCB boards.



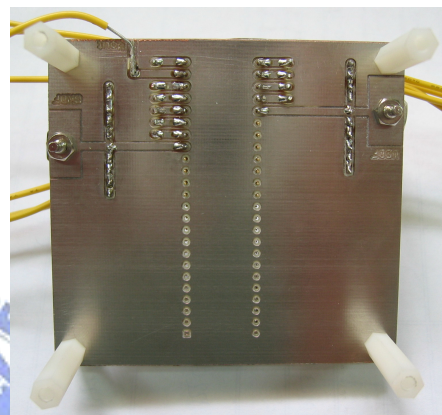
Two Buffers without Recycling (Front)



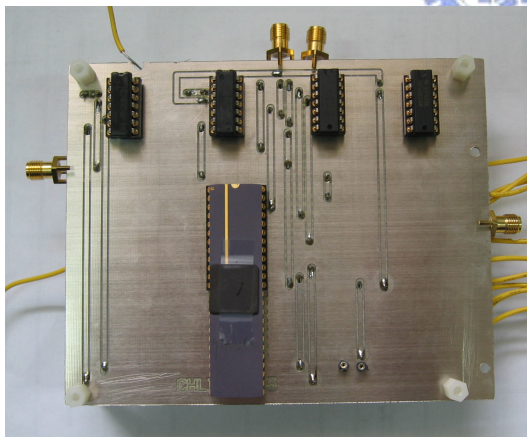
10-bit DAC (Front)



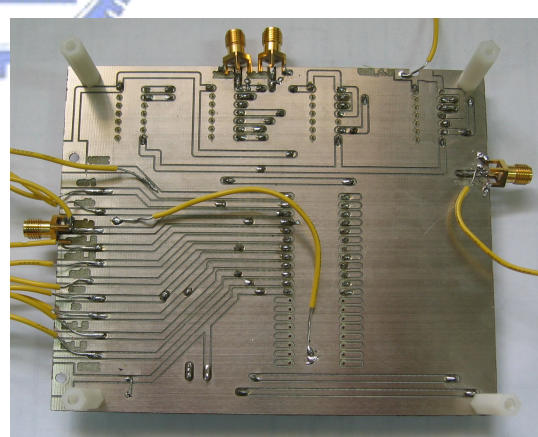
Two Buffers without Recycling (Back)



10-bit DAC (Back)



Triple Charge Recycling (Front)



Triple Charge Recycling (Back)

Fig.5.8 Several measurement PCB boards.

5.2.1 Class-B Buffer

Some DC values of measured class-B buffer are listed in Table. III. Since the input range of the class-B buffer is from 0.2V to 4.2V, some values of the unity-gain buffer is measured. As we can see, the voltage differences between input and output are about 3mV to 5mV.

Vin (V)	Vout (V)	Vin-Vout	Vin (V)	Vout (V)	Vin-Vout
4.2006	4.1952	5.4mV	2.0873	2.0774	3.9mV
4.0227	4.0177	5.0mV	1.8854	1.8820	3.4mV
3.8567	3.8516	5.1mV	1.7121	1.7086	3.5mV
3.5448	3.5398	5.0mV	1.5383	1.5353	3.0mV
3.1227	3.1180	4.7mV	1.3693	1.3660	3.3mV
3.0605	3.0560	4.5mV	0.9950	0.9910	4.0mV
2.5791	2.5749	4.2mV	0.4684	0.4646	3.8mV
2.2760	2.2712	4.8mV	0.2001	0.1959	4.2mV

Table. III. DC voltage values of measured class-B buffer.

Vcc	Current	Vcc	Current
6.0V	35.5 μ A	4.6V	9.3 μ A
5.6V	23.3 μ A	4.35V	7.0 μ A
5.3V	17.5 μ A	4.0V	3.4 μ A
5.0V	13.4 μ A	3.5V	2.0 μ A

Table. IV. Current consumption of measured class-B buffer.

The static current consumption of this buffer is about $35 \mu A$, which is way too high comparing to simulation results. Also, the current consumption drops too quickly as the V_{cc} drops. To explain this, let us see the corner simulation results of this proposed buffer plus the measurement result graph, as shown in Fig.5.9.

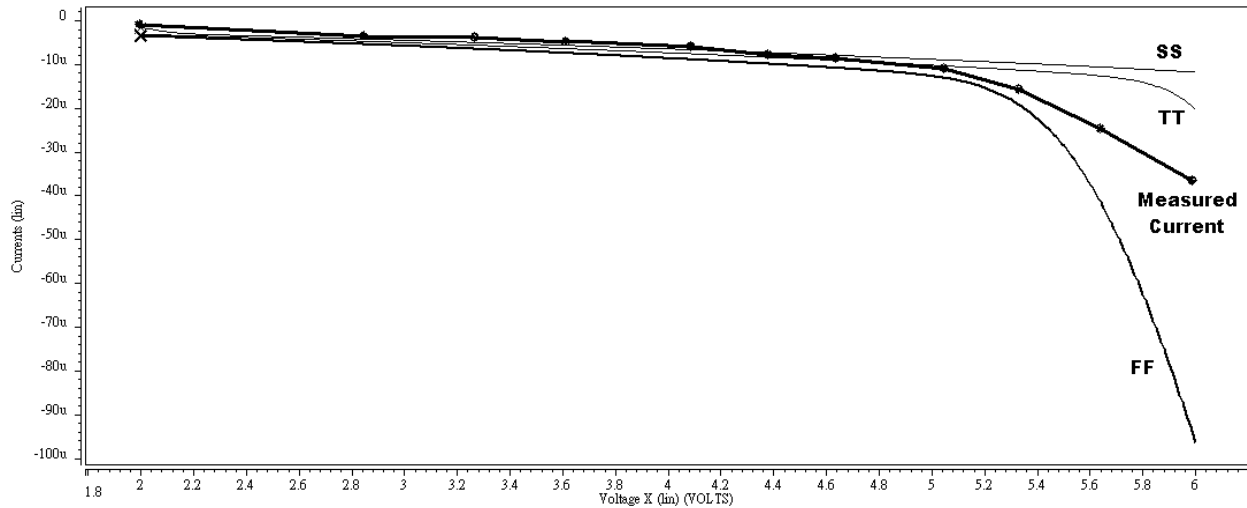


Fig.5.9 Simulation results of current consumptions of SS, TT, FF corners and measured current.

By checking the simulation DC data, when the process corner goes to fast-fast, the class-B buffer becomes class-A buffer, which means the output stage MOS transistors do not turn off and consume huge current about $74 \mu A$. The plotted measured current shows that this chip process drops between typical-typical and fast-fast.

The condition of testing transient response of this buffer is shown in Fig.5.10, and the measurement results are shown in Fig.5.11. As we can see, the transient response of this buffer is quick enough to charge the loading.

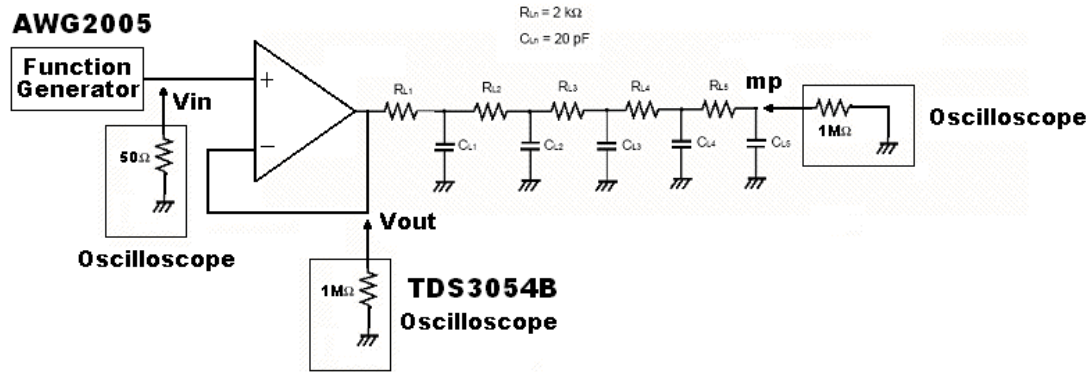


Fig.5.10 Measurement condition of measuring transient response.

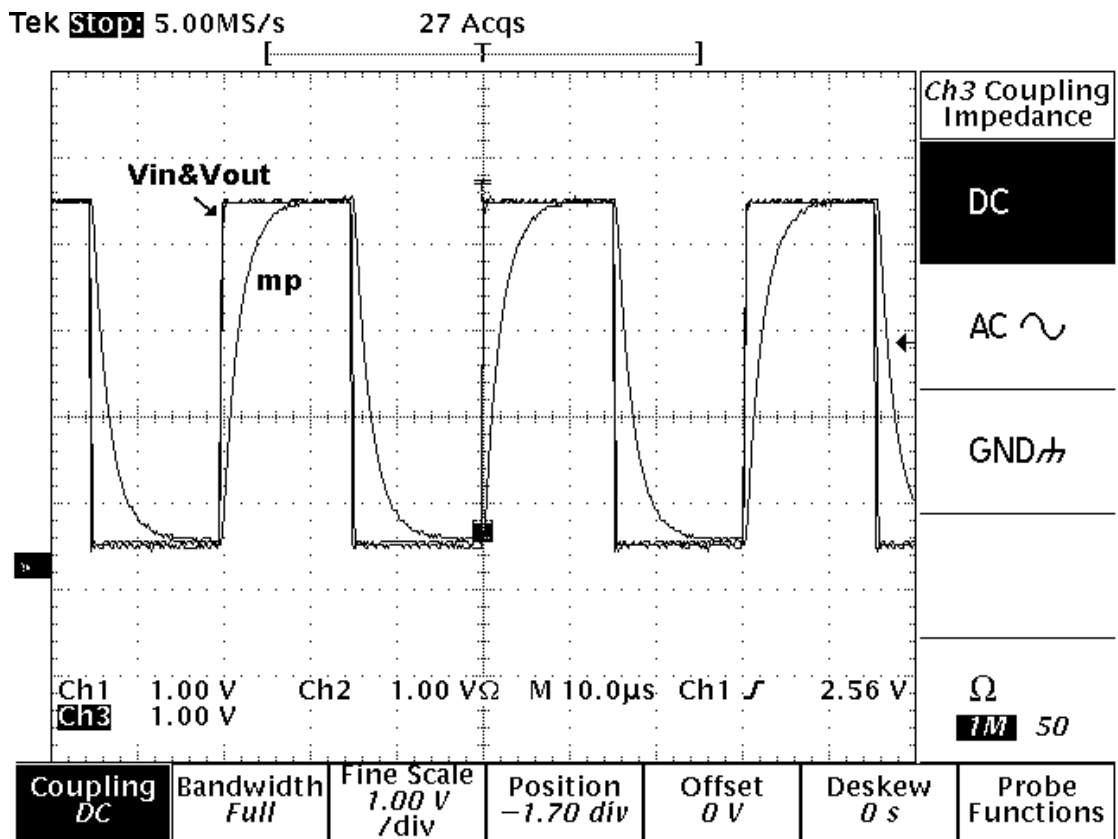


Fig.5.11 Measurement results of transient response.

5.2.2 Class-B Buffer with Chopper Techniques

The test condition of measuring class-B with chopper is similar as class-B buffer, but adding chopping signals. The measurement results are shown in Fig.5.12, Fig.5.13 and Fig.5.14. By adjusting the oscilloscope scale to very small, we can see that the V_{os} is added one time and subtracted next time. By this chopping operation, the liquid crystal sees the average voltage of two input voltage values and the V_{os} could be cancelled. Notice that the chopping clock is disturbed as the V_{out} changes since it is created from V_{out} by D-type flip flops.

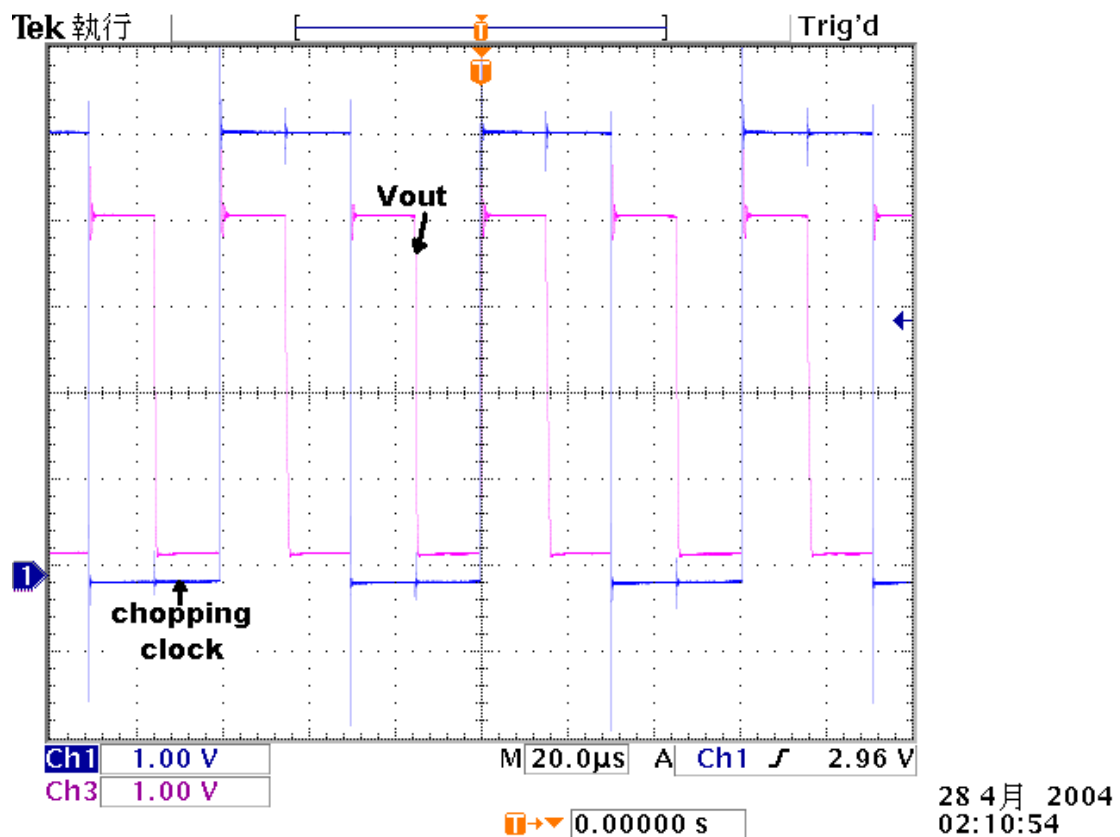
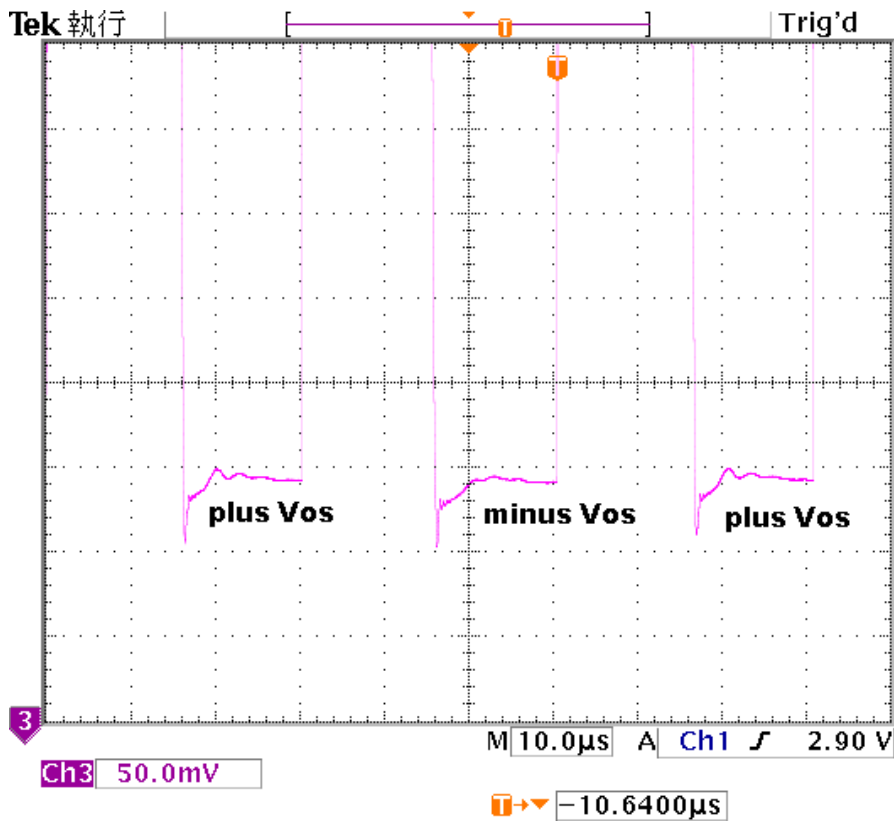
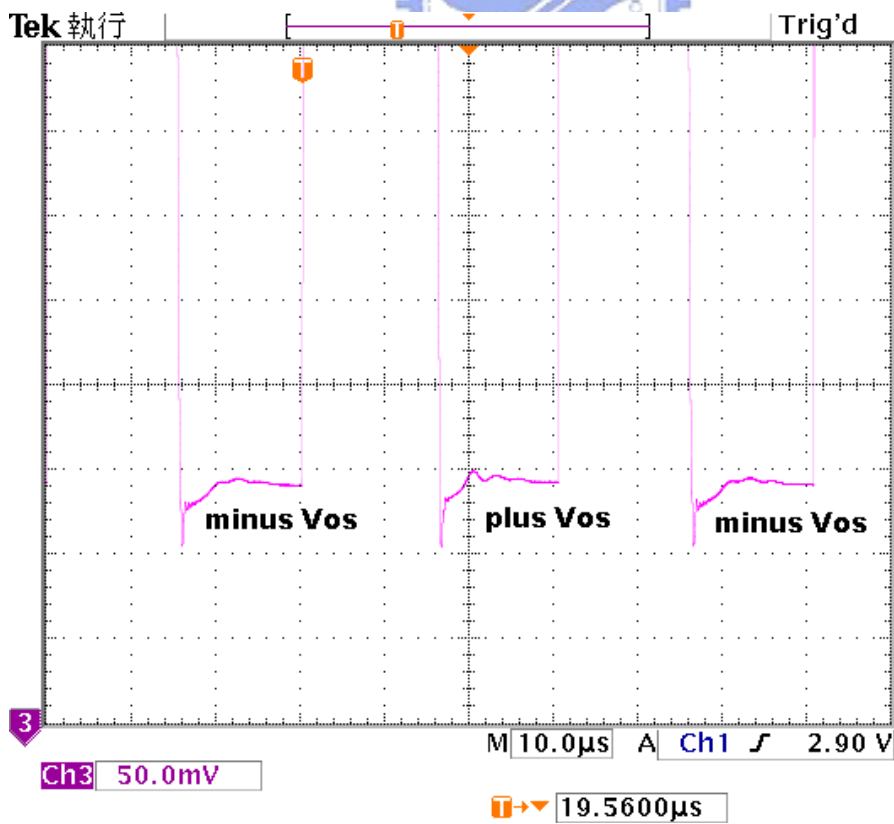


Fig.5.12 Transient response: chopping clock and V_{out} of class-B buffer with chopper.



28 4月 2004
02:09:23

Fig.5.13 Three adjacent Vout waveforms.



28 4月 2004
02:10:00

Fig.5.14 Another three adjacent Vout waveforms.

5.2.3 Two buffers without charge recycling

This circuit is only measured in order to compare with the other charge recycling circuits. The output waveform of this circuit is shown in Fig.5.15.

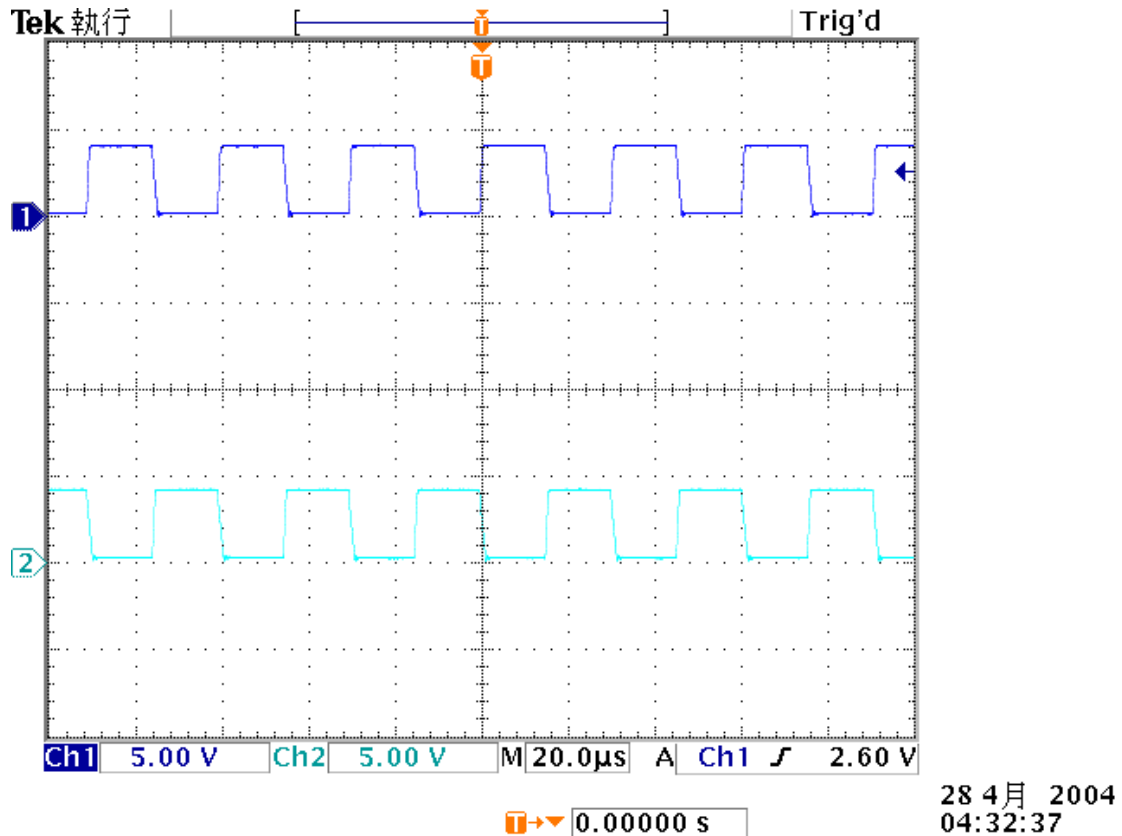


Fig.5.15 Two buffers without charge recycling.

While trying to measure its current consumption, an interesting data that listed in Table. V is observed. As we can see, if input frequency equals 33kHz and input swing equals 4V, the current consumption is strangely **inverse proportional** to V_{dd}:

V _{dd} =4.7V	I=472 µA	V _{dd} =5.3V	I=117 µA
V _{dd} =4.9V	I=509 µA	V _{dd} =5.6V	I=113 µA
V _{dd} =5.0V	I=237 µA	V _{dd} =6.0V	I=130 µA

Table. V. Current consumption of two buffers while |V_{in}|=4V.

In order to find out why this happens, several measurements are made and results are shown in Table. VI and Table. VII:

Vdd=5.0V	 Vin =0.05V	I=23.0 μ A	Vdd=5.8V	 Vin =0.05V	I=47.9 μ A
	 Vin =1.0V	I=31.3 μ A		 Vin =1.0V	I=58.6 μ A
	 Vin =2.0V	I=40.1 μ A		 Vin =2.0V	I=66.3 μ A
	 Vin =3.0V	I=64.0 μ A		 Vin =3.0V	I=78.1 μ A
	 Vin =4.0V	I=492.3 μ A		 Vin =4.0V	I=100.0 μ A
Vdd=5.2V	 Vin =0.05V	I=27.5 μ A	Vdd=6.0V	 Vin =0.05V	I=59.5 μ A
	 Vin =1.0V	I=36.3 μ A		 Vin =1.0V	I=70.6 μ A
	 Vin =2.0V	I=44.5 μ A		 Vin =2.0V	I=78.8 μ A
	 Vin =3.0V	I=64.5 μ A		 Vin =3.0V	I=89.5 μ A
	 Vin =4.0V	I=134.8 μ A		 Vin =4.0V	I=105.8 μ A
Vdd=5.5V	 Vin =0.05V	I=36.1 μ A	(Vin swings between 0.2V and 4.2V)		
	 Vin =1.0V	I=45.6 μ A			
	 Vin =2.0V	I=53.7 μ A			
	 Vin =3.0V	I=68.5 μ A			
	 Vin =4.0V	I=98.5 μ A			

Table VI. Current consumption of two buffers as input swing varies at different supply voltages.

Vdd=5.0V	Vin1=0.2V, Vin2=4.2V	I=14.3 μ A
Vdd=6.0V	Vin1=0.2V, Vin2=4.2V	I=60.1 μ A

Table VII. Current consumption of two buffers as input frequency equals zero.

From the above data, we can tell that the current consumption bursts out when supply voltage goes low (less than 5.5V) and input swing goes high (4V), which means the measured current does not follow the current consumption equation,

$I_{total} = I_{static} + I_{dynamic} = I_{static} + sCV$ (this will be further calculated in 5.2.5). Also,

if input frequency equals zero, this phenomenon would not occur.

In order to find out the explanation, going back to check HSPICE simulation is necessary. As illustrated in Fig.5.16 and Fig.5.17, if Vdd equals 5.0V, the current consumption goes terribly large when input swing goes to 4.0V, while the current consumptions are all normal if Vdd equals 6.0V.

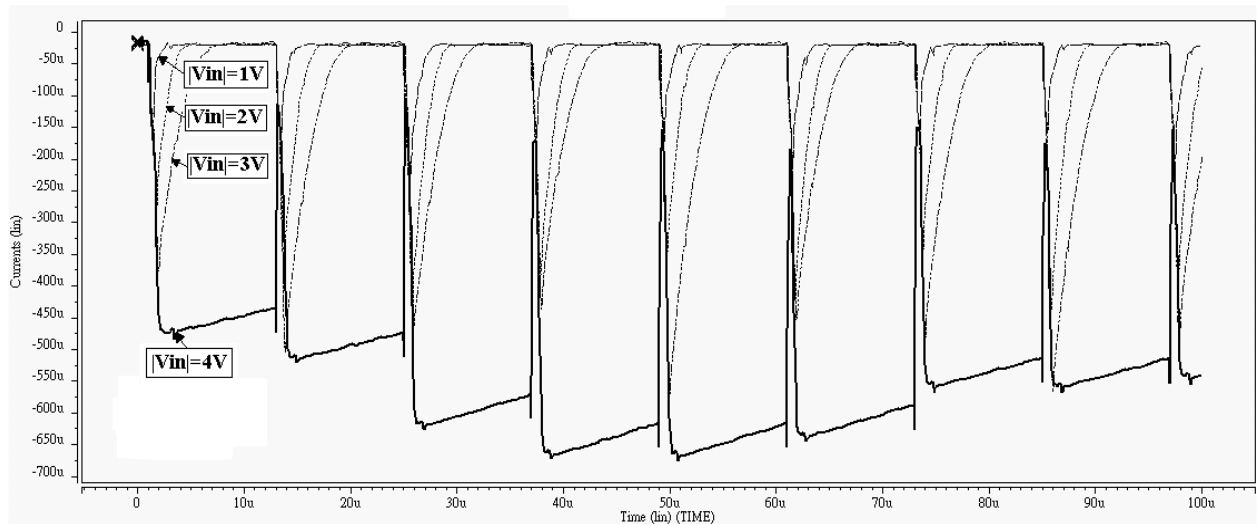


Fig.5.16 Current consumptions of different input swings at Vdd=5.0V.

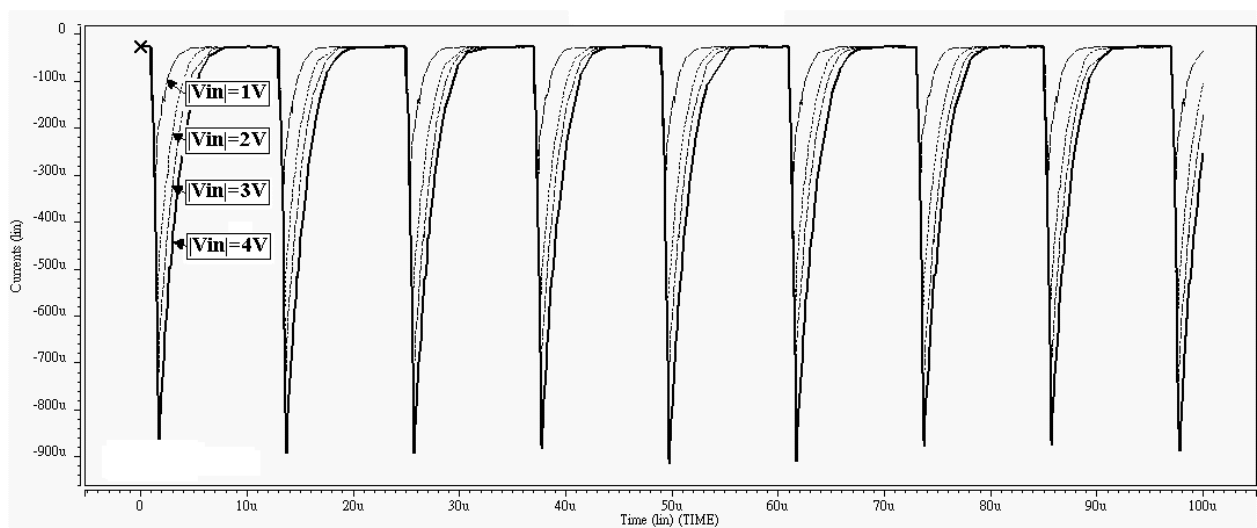


Fig.5.17 Current consumptions of different input swings at Vdd=6.0V.

Analyzing the input common mode voltage would tell the answer to current consumption, as shown in Fig.5.18. As we can see, the input common mode voltage is limited at $V_{dd}=5.0$, i.e., when the input voltage is greater than 3.75V, the I_{bias} of input stage (Fig.3.6) would decline, eventually cutoff. During transient response, the high input voltage would cause I_{bias} of input stage to be cutoff. Once it is cutoff, all the rest MOS transistors will be cutoff except output stage MOS transistors. Under this condition, the results are illustrated in Fig.5.19 and Fig.5.20.

At first, the V_{out} are 0.2V and V_{in} are 4.2V. The common mode voltage is 2.2V and the circuit is still under normal operation, thus the inverter stage would make output stage MOS transistors on and chase the input voltage level. After a while, as V_{out} approaches V_{in} and the input common mode voltage goes greater than 3.75V, all transistors turn off suddenly as the I_{bias} turns off. Thus, the gate voltages of output stage transistors remain the same, resulting great current consumption during transient response. If V_{dd} equals 6.0V, input voltage of 4.2V is still in input common mode range, all transistors are under normal operation.

Notice that there is still a small current while V_{in} equals 4.2V at $V_{dd}=5.0V$. This explains why DC values are correct.

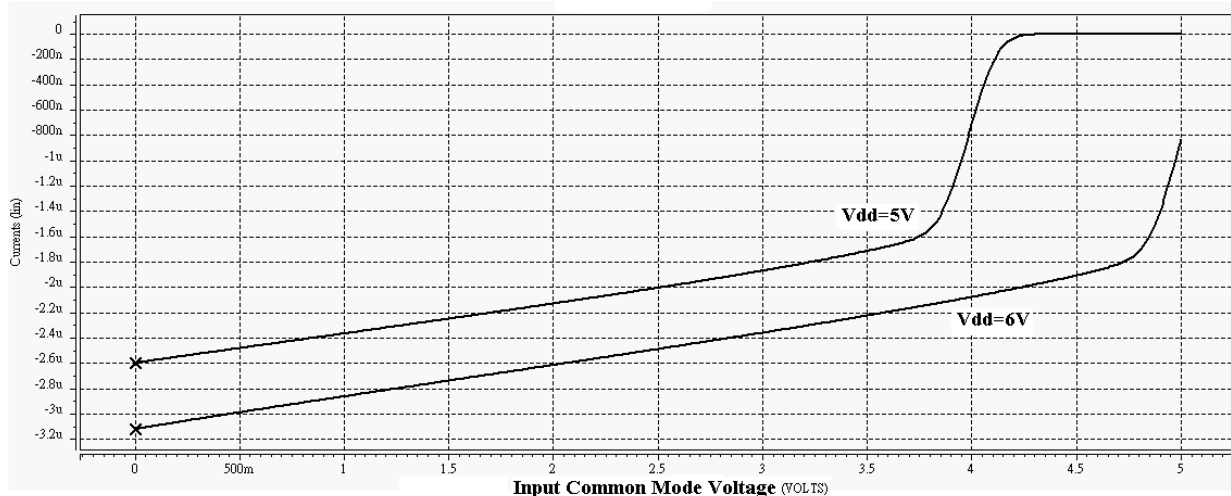


Fig.5.18 Current of input stage mirrored current source at $V_{dd}=5.0V$ and $V_{dd}=6.0V$.

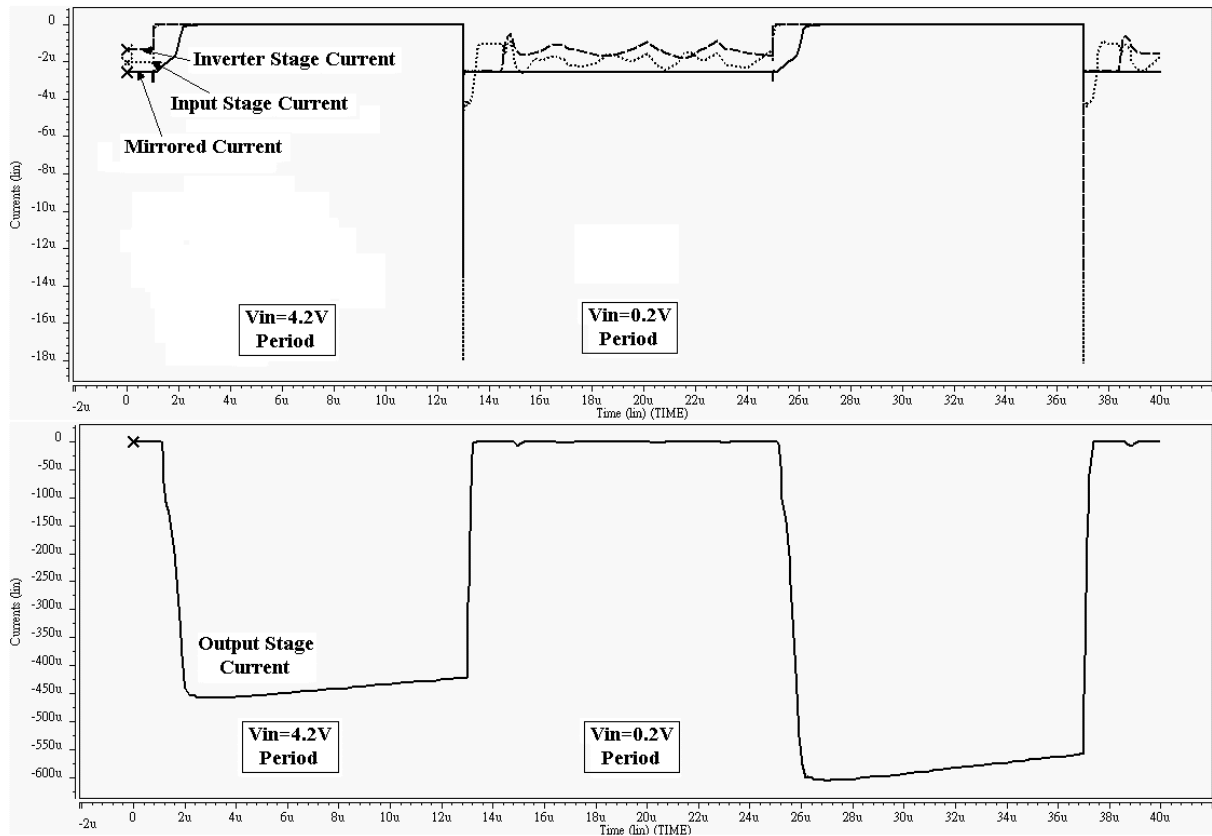


Fig.5.19 Current of different stage transistors at $V_{dd}=5.0V$.

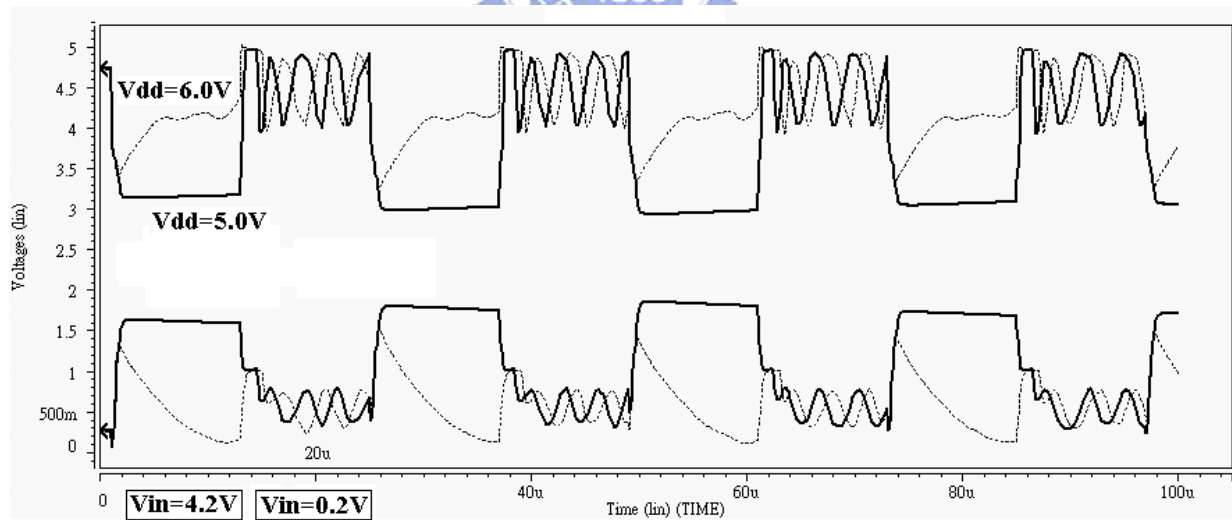


Fig.5.20 Gate voltages of two output stage MOS transistors.

5.2.4 Half charge recycling

The input signals of half charge recycling are already described earlier in 4.3.1. The measurement results of half charge recycling are shown in Fig.5.21, and its current consumption is listed in Table. VIII.

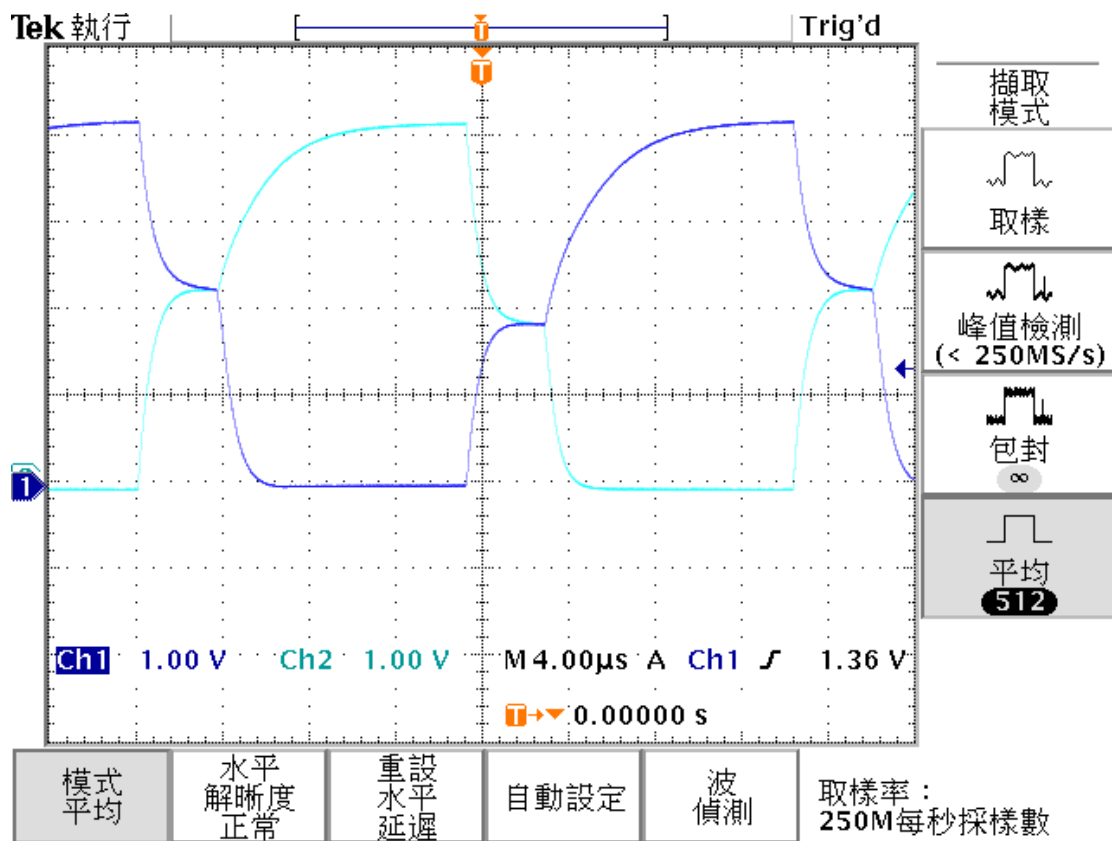


Fig.5.21 Waveform of half charge recycling.

Vdd=6.0V	I=80µA
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Table. VIII Current consumption of half charge recycling at Fvin=33kHz.

5.2.5 Triple charge recycling

Similarly, the input signals of triple charge recycling are discussed in 4.3.2. The output waveform of triple charge recycling is shown in Fig.5.22, and its current consumption is listed in Table. IX.

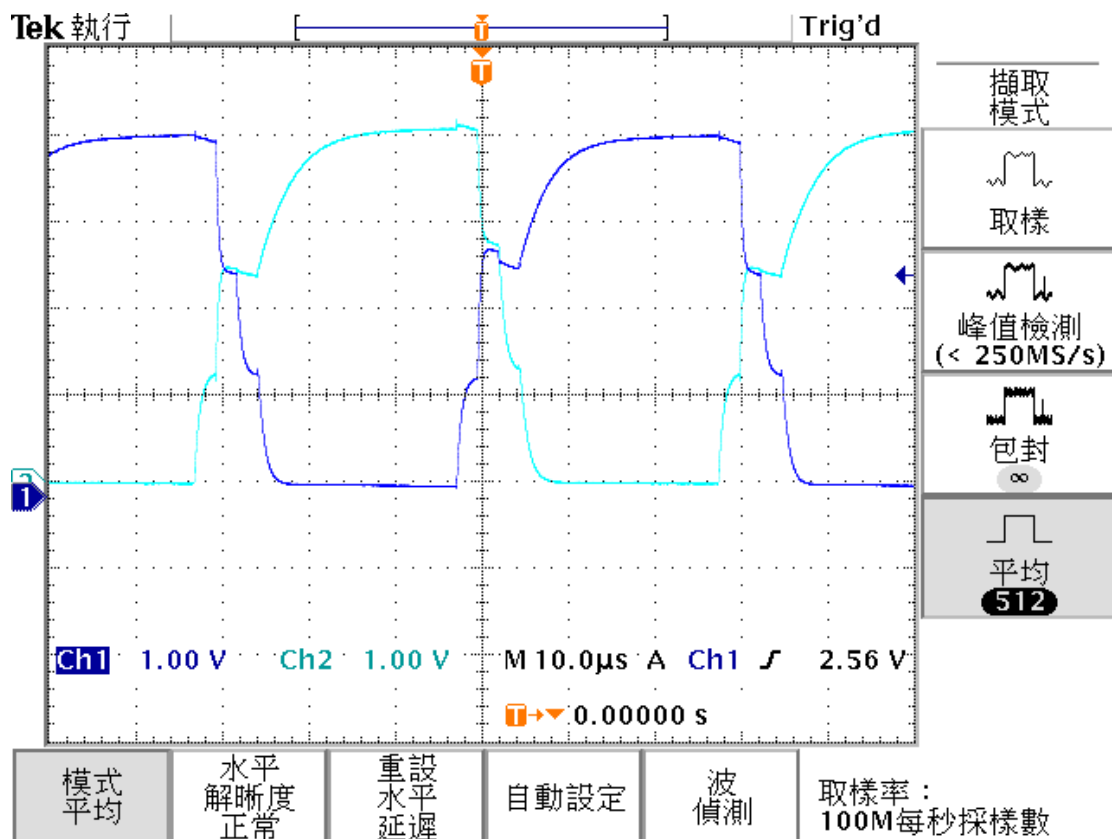


Fig.5.22 Waveform of triple charge recycling.

Vdd=6.0V	I=75.6 µA
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Table. IX Current consumption of triple charge recycling at Fvin=33kHz.

In order to calculate how much dynamic power that charge recycling saves, we must go back to the data of 5.2.3 and calculate the static power and dynamic power. It follows the equation, $I_{total} = I_{static} + I_{dynamic} = I_{static} + sCV$:

Two Buffers Without Charge Recycling		
Vdd=6.0V		$I_{static} + sC \times 0.05 = 59.5 \mu A \Rightarrow I_{static} \cong 59.5 \mu A$
 Vin =0.05V	I=59.5 μ A	
 Vin =1.0V	I=70.6 μ A	$I_{static} + sC \times 1 = 70.6 \mu A \Rightarrow sC \cong 11.1 \mu A$
 Vin =2.0V	I=78.8 μ A	$59.5 + sC \times 2 = 81.9 \mu A \cong 78.8 \mu A$
 Vin =3.0V	I=89.5 μ A	$59.5 + sC \times 3 = 93.1 \mu A \cong 89.5 \mu A$
 Vin =4.0V	I=105.8 μ A	$59.5 + sC \times 4 = 104.7 \mu A \cong 105.8 \mu A$
Under Vdd=6.0V and Vin =4.0V, $I_{dynamic} = 46.3 \mu A$		
Half Charge Recycling		
Vdd=6.0V	I=80.0 μ A	$I_{dynamic} = 80 \mu A - 59.5 \mu A = 20.5 \mu A$
Triple Charge Recycling		
Vdd=6.0V	I=75.6 μ A	$I_{dynamic} = 75.6 \mu A - 59.5 \mu A = 16.1 \mu A$

Table. X Calculation of dynamic current consumption.

From the above calculation, the dynamic power that half charge recycling saves is about $\frac{(46.3 - 20.5)}{46.3} = 55.7\% \cong \frac{1}{2}$, where the triple charge recycling saves $\frac{(46.3 - 16.1)}{46.3} = 65.2\% \cong \frac{2}{3}$ dynamic power.

5.2.6 10-bit Digital to Analog Converter

The measurement results of this digital to analog converter are quite bad. The desired output voltage range is from 0.2V (input code 0000000000) to 4.2V (input code 1111111111), but the measured voltages are from about 0.12605V (input code 0000000000) to about 2.7723V (input code 1111111111). This is caused by improper layout method. As illustrated in Fig.5.23, since the supply voltage is 6V and 0.2V to 4.2V is required, two kinds of resistance materials, N-well and Poly have been used as resistor string. This is because the square resistance value of N-well is much larger than that of Poly. But as shown in Fig.5.24, N-well resistance grows larger as the voltage drop across itself becomes larger due to the growth of depletion region. Thus the voltage division is a disaster.

The measurement results of different input code are listed in Table. XI. Although the result is still linearity, due to its wrong output voltage range, calculating DNL, INL is meaningless. Fig.5.25 shows its operating frequency when the input code changes from 0000000000 to 1111111111.

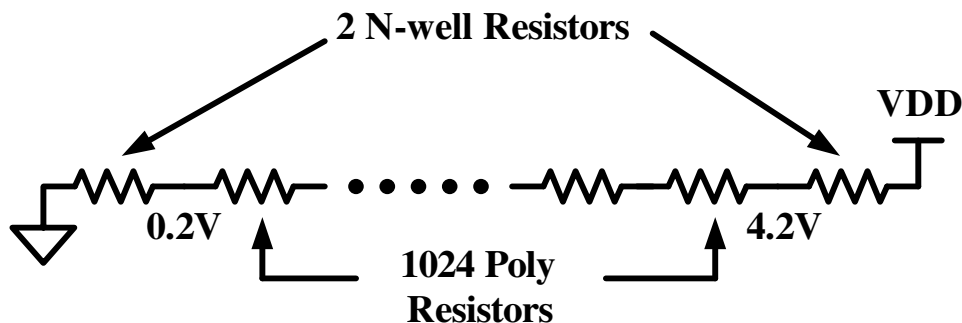


Fig.5.23 DAC resistor string.

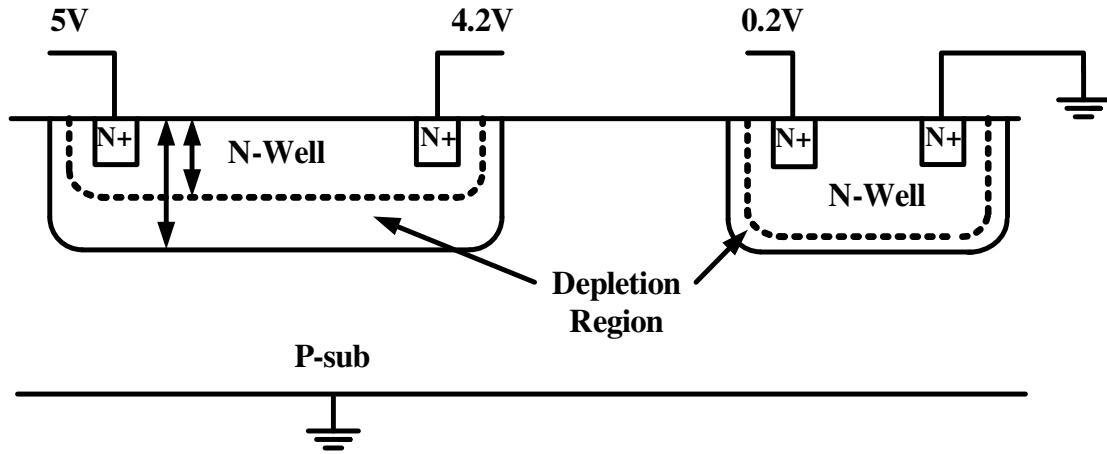


Fig.5.24 Resistance of N-well grows larger as the voltage drop across itself becomes larger.

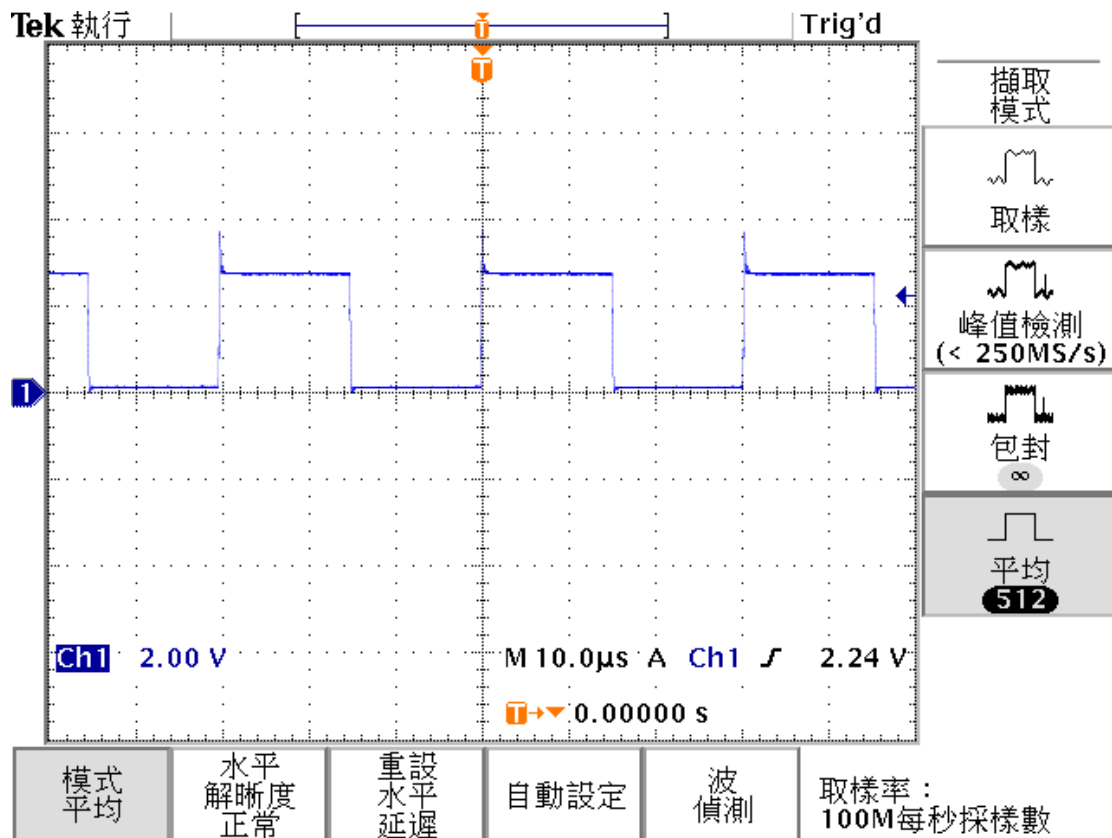


Fig.5.25 Output waveform of DAC when input code changes from 000000000 to 111111111.

Input code	Vout	ΔV	Input	Vout	ΔV
000000000	0.1260V	--	0000010010	0.1719V	2.4mV
000000001	0.1283V	2.3mV	0000010011	0.1745V	2.6mV
000000010	0.1310V	2.7mV	0000010100	0.1773V	2.8mV
000000011	0.1333V	2.3mV	0000010101	0.1798V	2.5mV
000000100	0.1362V	2.9mV	0000010110	0.1825V	2.7mV
000000101	0.1388V	2.6mV	0000010111	0.1846V	2.1mV
000000110	0.1412V	2.4mV	0000011000	0.1874V	2.8mV
000000111	0.1439V	2.7mV	0000011001	0.1899V	2.5mV
000001000	0.1466V	2.7mV	0000011010	0.1926V	2.7mV
000001001	0.1489V	2.3mV	0000011011	0.1953V	2.7mV
000001010	0.1516V	2.7mV	0000011100	0.1979V	2.6mV
000001011	0.1540V	2.4mV	0000011101	0.2003V	2.4mV
000001100	0.1567V	2.7mV	0000011110	0.2030V	2.7mV
000001101	0.1591V	2.4mV	:	:	
000001110	0.1617V	2.6mV	0111111111	1.4437V	--
000001111	0.1642V	2.5mV	:	:	
000010000	0.1668V	2.6mV	1111111110	2.7703V	--
000010001	0.1695V	2.7mV	1111111111	2.7723V	2.0mV

Table. XI Measured DAC output values at Vdd=6V.

$$\Delta V = V_{present} - V_{previous} \cdot$$

CHAPTER 6

CONCLUSIONS AND FUTURE WORKS

6.1 Conclusions

Scan driver and data driver is necessary in TFT-LCD panel. They are used to process the signals from graphic cards and transfer the signals properly to LCD panel. The display quality of TFT-LCD is highly depending on the design of data driver. Also, as the market of LCD-TV grows, the loading for driver circuits become larger because of larger panel size. Hence the design of driver circuits is more and more challenging and the specification of circuit speed is higher. For this reason, a high performance driver is needed. Also, the power consumption is a key issue that should be considered in this technology.

A high-speed low-offset-voltage output buffer has been proposed. It is highly accuracy, low power consuming and small area. The rising and falling time of the buffer can be smaller than 4μ sec, which can drive the display resolution of 1280x1024. The offset voltage of the buffer is less than 2mV, which means it is capable of displaying 10-bit resolution images. Also, a 10-bits DAC is implemented. The operation range is 0.2V to 4.2V and its LSB equals to 4mV.

Finally, two circuits, half and triple charge recycling, have been verified by Hspice and fabricated in a 0.35μ m CMOS process. The dynamic power can be reduced to 1/2 by half charge recycling, and 1/3 by triple charge recycling.

6.2 Future works

The main design goals of TFT-LCD driver is high speed, high accuracy, and low power consumption. In this thesis, the data driver that meets the present specification has been proposed. But as the applications of LCD panel grow, new challenges will come out and needed to be solved. For example, the larger size the panel is, the loading becomes larger and the operation speed is the key issue. Another major issue is the power consumption. More and more mobile devices such as cell phones and PDAs use small LCD panel. The smaller the power consumption is, the longer the battery life it is.

Finally, for LCD-TV applications, the major drawback is its response time, and the problem need to be solved in the years to come. There are still many efforts needed in this field.



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