Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this thesis, we propose a high performance outer receiver for WLAN IEEE 802.11a/g. For soft decision resolution issue, we apply 4-bit soft decision for demapping design. For traceback-length issue, we employ traceback-length 63 in Viterbi decoder. For the demand of real-time decoding mechanism, we do not use SRAM module in Viterbi decoder. We use 20MHz clock rate generated from RF to be baseband receiver clock rate. The outer receiver and inner receiver can be integrated directly without concerning about the interface problem. We also prevent the outer receiver from decoding wrong outputs while the header goes wrong. The test chip is fabricated in 0.18 CMOS process, and can operate at a maximum frequency 25MHz under 1.8V. It can achieve the maximum throughput rate of 67Mbps under 1.8v.

6.2 Future Work

In the proposed outer receiver architecture, we adopt 20MHz to be the system clock rate. If we employ the double or triple of the proposed clock rate, we can use lower complexity Viterbi decoder architecture to meet the data flow request. Therefore, the gate count will decrease, and the maximum operation speed will improve. And we will integrate with IEEE 802.11a transmitter, inner receiver, and the proposed outer receiver into a transceiver and try to contain MAC in the future.

UWB (Ultra Wide Band) application will be used popularly for WPANs (Wireless Personal Area Networks) in recently years. The bottleneck of UWB baseband circuit is to implement a high speed channel decoder. For example, IEEE 802.15.3a standard requests a high speed Viterbi decoder which the throughput rate is 480Mbps. The mandatory issue focuses on the critical path elimination of ACS module. Thus, we can employ bit-pipeline method to solve the problem in the future.