

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

二氧化鈣基底電阻式記憶體
之動態轉換物理模型

The Physical Model of the Switching Dynamics in
HfO₂-based Resistive Random Access Memory

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中華民國 九十九 年 七 月

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摘要

傳統非揮發性記憶體如 FLASH 和 SONOS 等快閃記憶體有著許多先天上的微縮限制，如隨機摻雜擾動 (Random Dopant Fluctuation)、隨機電報雜訊 (Random Telegraph Noise) 和最小穿隧氧化層厚度。為了解決上述的問題，一種藉由電阻轉換的全新記憶體在近年來被廣泛地討論及研究。在所有電阻轉換記憶體當中，以過渡金屬氧化物作為介電基層的電阻式隨機存取記憶體 (Resistive Random Access Memory) 被最為看好，因為它製程與結構簡單，還有極佳的微縮性質，低電壓操作和多位元儲存的可能性。

已經有相當多的文獻討論不同電阻式記憶體介電層和電極材料的影響與特性，但是對於其電阻轉換機制卻缺乏完整的了解。截至目前雖有不少文獻針對電阻式記憶體電流電壓特性提出的模型，例如空間電荷限制電流 (Space Charge Limited Current)、法蘭克—普爾傳輸 (Frenkel-Poole Transport)、蕭基能障熱發

射 (Shottcky Barrier Thermal Emission) 和離子的飄移擴散模型。這些模型往往只能解釋部份的電阻轉換現象，但在別的現象是失效的。本篇論文的研究目的在於建立一個既簡單明瞭又能完整解釋電阻式記憶體各種電阻轉換現象的模型，並且深入地了解電阻式記憶體特殊的遲滯電流電壓特性曲線。

由於電阻式記憶體的讀取電壓很小 (約 0.1V)，介電層的厚度可以只有幾個奈米，而且其金屬—絕緣體—金屬的結構肯定會產生一個電流傳輸能障，這些因素皆滿足直接穿遂理論的條件。根據溫度變化實驗，我們發現穿遂能障高度並不會跟著不同電阻值狀態而改變，因此關鍵必定在於穿遂能障的寬度。基於 WKB 近似法所作的模擬結果與實際量測數據相當吻合。模擬的結果顯示穿遂能障寬度與施加的重設電壓成正比關係，也就是說在電極與氧空缺 (Oxygen Vacancy) 構成的導電細絲尖端之間形成了一層不含電荷的介電層。阻態的開/關比例則受控於穿遂能障高度、電子等效質量和陷阱最大距離。我們也同時研究穿遂能障寬度的時變性質，我們發現在阻值轉換期間，穿遂能障寬度變化量與對數時間成線性關係，而轉換時間乃受控於電流大小、導電細絲的電荷密度和截面積的大小。

近年來的研究指出電阻式記憶體可能成為第四種被動元件：憶阻器，由於憶阻器的電壓電流特性與電阻式記憶體相當類似。在本篇論文中我們提出一套系統化的數學方法並根據真實實驗數據來模擬電阻式記憶體的憶阻特性，以便將來可以應用在 SPICE 電路模擬程式之中。

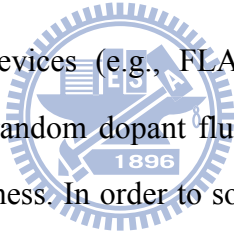
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ABSTRACT



Carrier-trapping memory devices (e.g., FLASH, SONOS etc.) have several inherent scaling limits, such as random dopant fluctuation, random telegraph noise, and minimum tunnel oxide thickness. In order to solve the problems as above, a new type of resistive-changing memory has been widely studied in recent years. Among all of the resistive-changing memories, the transition metal oxide based resistive random access memory (RRAM) is most promising owing to its simple structure (Metal-Insulator-Metal, MIM) and fabrication, excellent potential of scaling, small voltage operation, and possibility for multi-level storage.

Many papers with focus on RRAM dielectric and electrode materials have been published, but the switching mechanism of RRAM has not been well understood. So far, several models based on RRAM current-voltage characteristic have been published, for example, space-charge-limited current (SCLC), Frenkle-Poole transport, Schottky barrier thermionic emission, and Ionic drift-diffusion, etc. Each of them explains on some perspectives, but with loss of generality. The main purpose of my

research is to construct a simple and well-explained model for RRAM switching mechanism and investigate the secret of RRAM specific hysteresis current-voltage characteristic.

Since RRAM reading voltage is small (about 0.1V), the dielectric layer could be ultrathin (about few nanometers), and its MIM structure surely exhibits a barrier for transport electrons, which satisfies the constraints for direct tunneling. Based on temperature experiments, I found the tunnel barrier height is not changing for different resistance states, so the key must lie on the tunnel barrier width. The simulation based on WKB approximation successfully fits the real measurement data. The simulation shows that the tunnel barrier width is proportional to the reset voltage, which means there is a charge free dielectric layer formed between metal electrode and the tip of the conduction filament composed of oxygen vacancies. The resistance on/off ratio is controlled by the barrier height, electron effective mass, and the maximum defect distance. The tunnel barrier width time varying property is also studied. During the transition, tunnel barrier width changes with logarithmic time. The switching time is controlled mainly by the current amplitude, conduction filament charge density, and the cross section.

The possibility of RRAM as a long-missing forth passive element, memristor, has been widely discussed in more recent years. The memristor theoretical hysteresis current-voltage characteristic happens to be similar to the behavior of RRAM. We proposed a mathematical method to simulate RRAM memristive behavior in SPICE based on real transient measurement data.

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兩年的實驗室生活是精采豐富的，但同時也充滿艱辛與汗水。首先要感謝的是我的指導教授：莊紹勳教授，老師給予的生活上與專業上的指導與建議，讓我在學業上與研究上獲益良多並學習到對事物應有的嚴謹態度以及處理方法。除此之外，對於課業外的生活技能、觀念的督促，讓我必須在此表達感謝之意。

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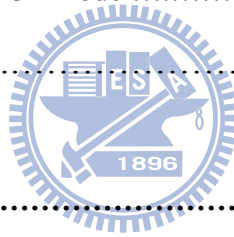


Table caption

Table 3.1 Device parameters used in simulation.

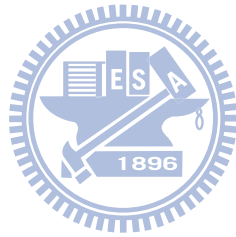


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Chapter 1

Introduction

1.1 Background

Today, Silicon-based Flash represents the most promising nonvolatile memory because their high density and low fabrication loss. However, Flash now faces an inevitable scaling problem limited by the tunnel oxide thickness [1.1]. To solve this issue, nitride storage Flash, usually called SONOS, has been developed [1.2]. Although SONOS can continue the scaling of tunnel oxide thickness, several inherent problems of these charge-trapping type nonvolatile memories emerges, such as random dopant fluctuation [1.3], random telegraph noise [1.4], stress induced leakage current [1.5], and trap-assist tunneling [1.6], etc. The next generation nonvolatile memories are focused on resistance type structures. There are four main streams: Ferroelectric RAM (FeRAM), Magnetoresistive RAM (MRAM), Phase Change Memory (PCM), and Resistive RAM (RRAM). FeRAM exhibits lowest power, while MRAM shows fastest switching. PCM and RRAM have moderate power consumption and switching rate but promising scaling potential, which makes them more attractive [1.7, 1.8]. Nevertheless, the self heating of PCM exhibits great challenges due to frequent high temperature re-crystallization. RRAM becomes the most popular new nonvolatile memory owing to its simple structure (MIM), easy fabrication, and good compatibility with conventional CMOS technology.

1.2 The Motivation of This Work

About forty years ago, scattered reports discover chalcogenide material sandwiched by two metal electrodes may change its conductivity under applied electric field [1.9-1.10]. This property did not attract much attention at that time because nonvolatile memory was not popular at that time and the device scaling was not a critical issue. Not until the publication of electric-pulse-induced reversible resistance change made by S. Q. Liu in 2000 [1.11], this kind of resistive random access memory draws many interests as a potential candidate which will dominate the next generation nonvolatile memory.

Many materials have been investigated as RRAM dielectric. In general, we may classify these materials into three categories: (1) Perovskite, (2) Transition Metal Oxide, and (3) Organic and Macromolecule materials. The perovskite material, such as PCMO and LCMO, was first developed due to its close connection with FeRAM [1.12-1.14]. The organic materials attract lots of interests in recent years because of their various application possibilities [1.15]. However, the transition metal oxide based RRAM shows best performance, reliability, and conventional fabrication compatibility. There have been numerous reports on transition metal oxide materials, such as SrTiO₃, TiO₂, ZrO₂, NiO, TaO₂, HfO₂, WO₂, etc. [1.16-1.22]. Some reports also mentioned the importance of electrode material, which may decide whether RRAM behavior exists using the same insulator [1.23].

Besides the variety of dielectric materials, the switching mechanism of RRAM also aroused controversies, such as Mott transition, Jahn-Teller Effect, and ionic dopant drift,

etc [1.12, 1.13, 1.24]. A more widely accepted model for transition metal oxide based RRAM manifested that there is one or several conduction filaments connecting between two electrodes, and the formation and rupture of the filaments control the measured resistance [1.25].

The current-voltage characteristic of RRAM is the simplest way to verify switching mechanism. Different switching mechanisms are usually accompanied by different current models, for example, Space-Charge-Limited Current with Mott transition, Shottcky barrier thermionic emission, and Coupled ionic and electronic transport with ionic dopant drift, Frenkle-Poole transport and tunneling with conduction filament theory [1.18, 1.20, 1.26,1.27].



Besides nonvolatile memory application, RRAM is also a possible candidate to realize the long-missing two-terminal circuit element: memristor. The theory of memristor was proposed in 1971 by Leon Chua [1.28], which states that there should be a fourth passive element to complete the relation between voltage, current, charge, and magnetic flux, except the existing resistor, capacitor, and inductor. If we apply a sinusoidal voltage input to a memristor, we can expect a hysteresis loop in current-voltage plot, which is very similar to RRAM behavior [1.29]. Benefitting from its nonlinear characteristic, memristor has broad applications from analog/digital circuits to neuromorphic computing [1.30-1.32].

In this thesis, we use hafnium oxide as RRAM dielectric to investigate transition metal oxide based RRAM switching mechanism. We perform temperature experiments,

constant voltage stress experiments, transient analysis, and pulse experiments to verify each of known current models and find out that direct tunneling model is the only solution to connect every phenomenon in real measurement data. We established the direct tunneling model to explain other RRAM behaviors like multi-level storage, exponential dependent switching time, and asymmetric SET/RESET behavior. Finally, based on the proposed switching mechanism model, we link the relation between RRAM and memristor using a mathematical method. This method provides a systematic way to characterize any type of RRAM memristor based on real measurement data.

1.3 Organization of the Thesis

There are six parts in this thesis. Chapter 1 is the introduction. We describe the motivation and organization of this thesis. In Chapter 2, we show the fabrication and equipment setup used in experiments. In Chapter 3, we will discuss the current models and switching mechanism on the basis of experimental data. In Chapter 4, the transient behavior of RRAM is discussed and for the first time, we propose two models to quantitatively describe RRAM switching time. In Chapter 5, RRAM memristive characteristic is fully examined. Compared with original theory, we will discuss the limitations and possibilities of RRAM as a memristor. Finally, the summary and conclusions are given in Chapter 6.

Chapter 2

Device Fabrication, Equipment Setup and Measurement Methods

2.1 Device Fabrication

The structure of RRAM was the TiN / TiO_x / HfO_x / TiN stack, which was deposited on the Ti / SiO₂ / Si substrate. The HfO₂ thin film was deposited by atomic layer deposition (ALD), while all the other thin films were deposited by sputtering methods. Owing to the well known ability of Ti to absorb oxygen atom [2.1], oxygen atoms diffuse from the HfO₂ layer to the Ti, which resulting in the formation of HfO_x (x~1.4) with a large amount of oxygen deficiency and the oxidation of Ti. The corresponding XTEM image made by the XPS examination is presented in Fig. 2.1 [2.2].

2.2 Equipment Setup

The whole experimental setup for the I-V and pulse characteristics measurement of RRAM is illustrated in Fig. 2.2. Based on the PC controlled instrument environment by HP-IB (GP-IB, IEEE-488 Standard) interface, the complicated and long-term characterization procedures to analyze the behaviors in RRAM cells can be easily achieved. As shown in Fig. 2.2, the equipments, including the semiconductor parameter analyzer (Agilent 4156C), low leakage switch mainframe (HP 5250A Switching Matrix), pulse generator (Agilent 81110A), and probe station, were used for our measurements on

RRAM. Programs written by HT-Basic were used to execute the measurement via HP-IB interface.

The Agilent 4156C provides a high current resolution up to pico-ampere range, and is equipped with four programmable source/monitor units. Two source units, and two monitor units for supplying or monitoring the voltage and the current. The pulse generator Agilent 81110A with high timing resolution provides for P/E cycling endurance and transient characterization. The HP 5250A switching matrix equipped with an 8-input x 12-output switching matrix switches the signals from the Agilent 4156C and Agilent 81110A to device under test in probe station automatically.


In order to control the pulse timing of Agilent 81110A during transient and P/E cycling endurance characteristics precisely, we select the triggered pattern mode to achieve this goal. Fig. 2.3 (a) and Fig. 2.3 (b) show the program and erase schemes on the RRAM respectively. For example, by taking the programming timing pattern as shown in Fig. 2.3, the triggered pattern mode can be explained as follows. In Fig. 2.3 (a), the VSU1 of Agilent 4156C generated a voltage signal which is equal to the low voltage level of Agilent 81110A. This triggered pattern mode method can provide a substrate bias during programming, and prevent additional stress to device during P/E cycling endurance operation. The pattern mode defined as 01000 in Fig. 2.3 (a) from Agilent 81110A is then sent and the program or erase operation is performed.

2.3 Measurement Methods

2.3.1 Introduction

There are four measurement techniques used in this thesis. First, a forming process is required for every fresh device before normal operation. Second, normal operation using bipolar voltage/current sweep is necessary for basic device characterization. The last two methods are designed to examine RRAM transient behavior: series resistor sensing and continuous pulse measurement for different applications.

2.3.2 Forming



Before we start to operate the resistive switching random access memory correctly, we need to perform the so-called “forming” procedure first, as shown in Fig. 2.4. We add a ramped voltage on the top TiN electrode which is near the Ti buffer layer, and measure the corresponding current by Agilent 4156C semiconductor parameter analyzer. When the accumulated energy exceeds a certain limit determined by device material and thickness [2.3], the current rushes to the value of compliance current, and the forming step is accomplished, as shown in Fig. 2.5. The compliance current is usually set to be a little less than the compliance used in normal SET process.

2.3.3 Sweep

After the “forming” process, this device switches to LRS (Low Resistance State).

The following step is to turn it off, i.e., to switch the RRAM from LRS to HRS (High Resistance State). There are two operation mode to identify the switching type of RRAM [2.4]. As shown in Fig. 2.6, one is uni-polar, and the other one is bi-polar. Uni-polar means that the turn on voltage and turn off voltage are at the same polarity, where the turn on voltage is usually larger than turn off voltage. On the other hand, the bi-polar means that the turn on voltage and turn off voltage are in opposite polarities. Usually the bi-polar switching device is more suitable for future CMOS technology due to less operation voltage and power consumption. Our device basic characteristic is shown in Fig. 2.7, which is obviously a bi-polar device. The illustrations of voltage sweep operations in this thesis are shown in Fig. 2.8 and Fig. 2.9.

For SET process, besides voltage sweep method, we can also use current sweep to eliminate current compliance, which is illustrated in Fig. 2.10. In this method, we simply exchange the current compliance to the target current amplitude. This method avoids large current flow through RRAM during SET process and thus improves device consistency and reliability. There are also some reports indicating the benefit of current sweep method [2.5, 2.6].

2.3.4 Series Resistor Sensing

To measure RRAM transient behavior, we use an oscilloscope to directly monitor RRAM real-time current. The equipment setup is illustrated in Fig. 2.11. The sensing resistor is chosen to be $100\ \Omega$ to avoid significant voltage dividing while giving enough signal amplification, because normally lowest resistance state is about $1\text{k}\ \Omega$. This

technique allows us to investigate RRAM transient behavior in linear time scale, which is very useful in analyzing RRAM memristive characteristics.

2.3.5 Continuous Pulse Measurement

The linear time scale measurement can not see the whole story about RRAM switching behavior, as we will discuss later in Chapter 4, so we need another technique to measure logarithmic time scale behavior. Fig. 2.12 illustrates the concept of this measurement technique. We use Agilent 81110A to generate a series of pulses with the same top and bottom levels. After ten same pulses, the eleventh pulse width increase one order so that the overall stress time continues in logarithmic time scale. After each pulse, HP 5250A switches the input to Agilent 4156C to start small voltage sampling. This sampling procedure “reads” RRAM temporary state by applying 0.1V to evaluate current and resistance. The 0.1V is chosen to be less than RRAM switching threshold to avoid disturbance. This method is helpful in giving an overview on RRAM transient switching behavior.

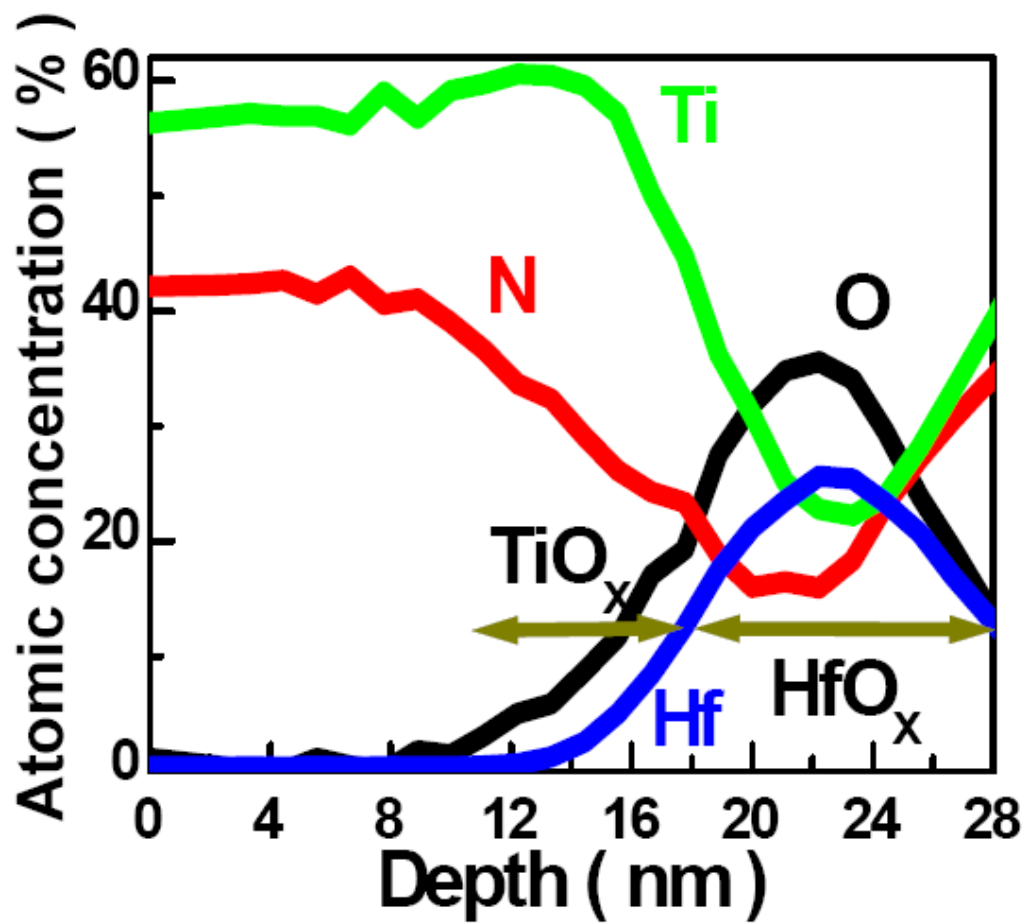


Fig. 2.1 XPS depth profile of TiN/Ti/HfO₂/TiN stack layers after alloying

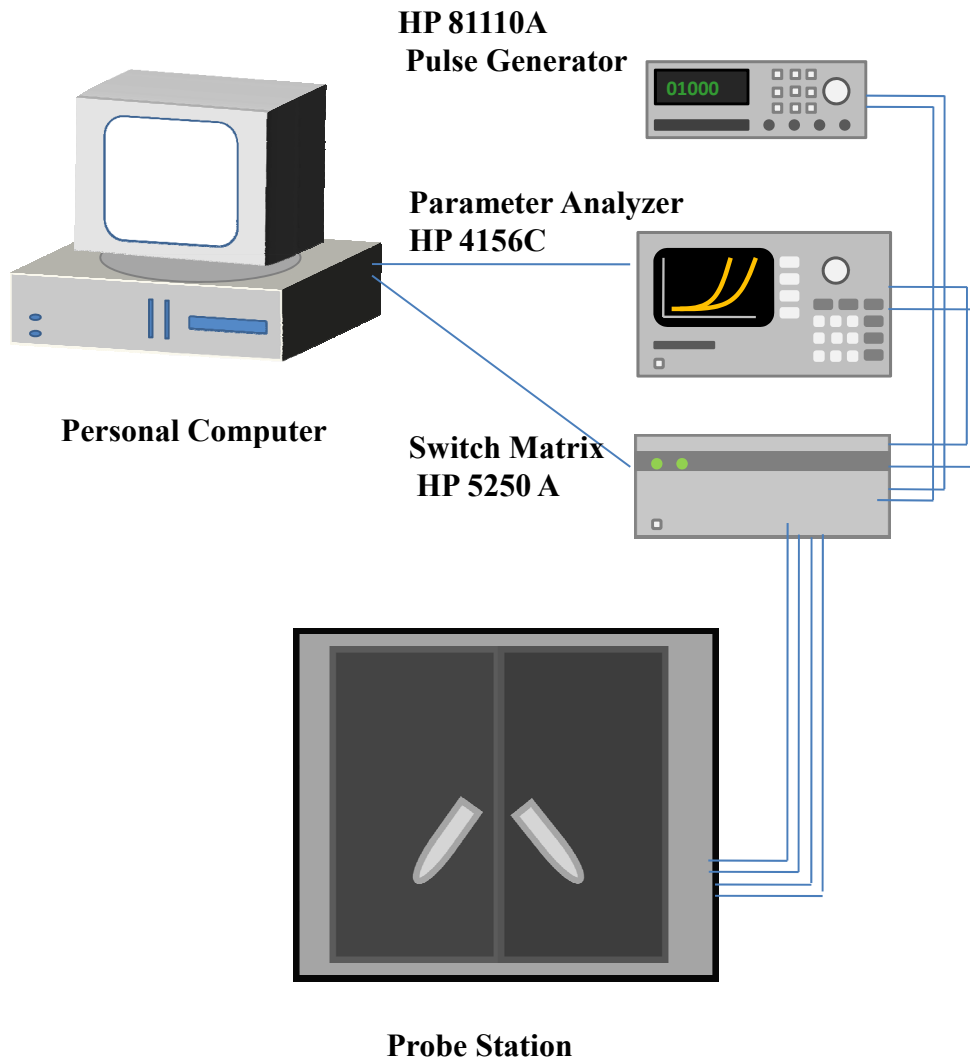
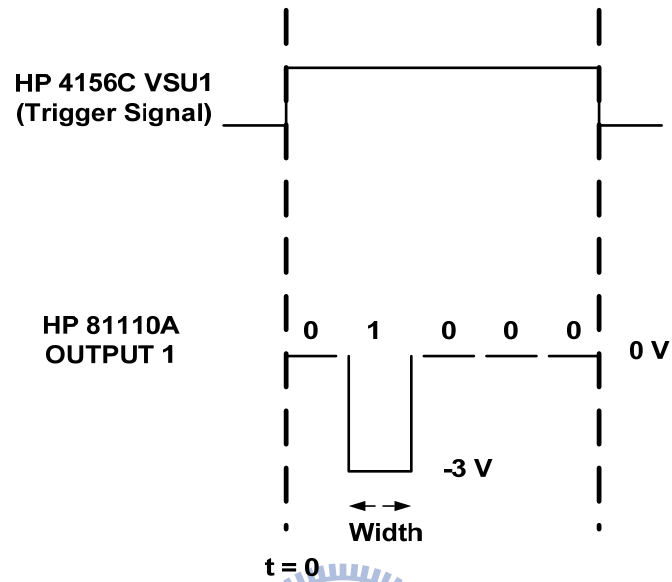


Fig. 2.2 The experimental setup of the current-voltage and the P/E cycling endurance characteristics measurement in RRAM. Automatic controlled characterizations system is setup based on the PC controlled instrument environment.

(a) PROGRAM



(b) ERASE

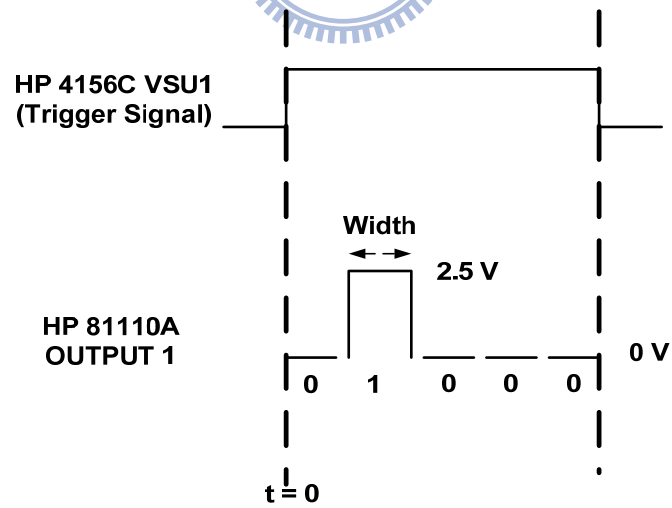


Fig. 2.3 The timing diagram of the triggered pattern mode method during (a) program and (b) erase operation.

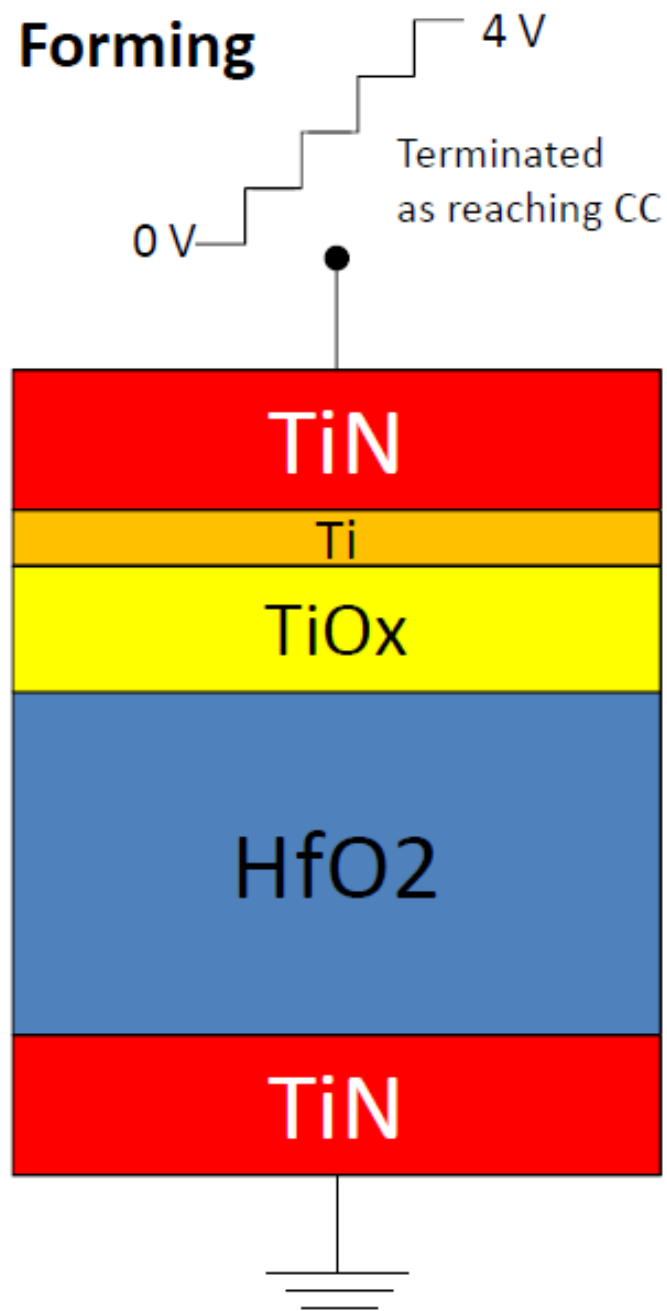


Fig. 2.4 The cross section of transition metal oxide based resistive switching memory during forming process.

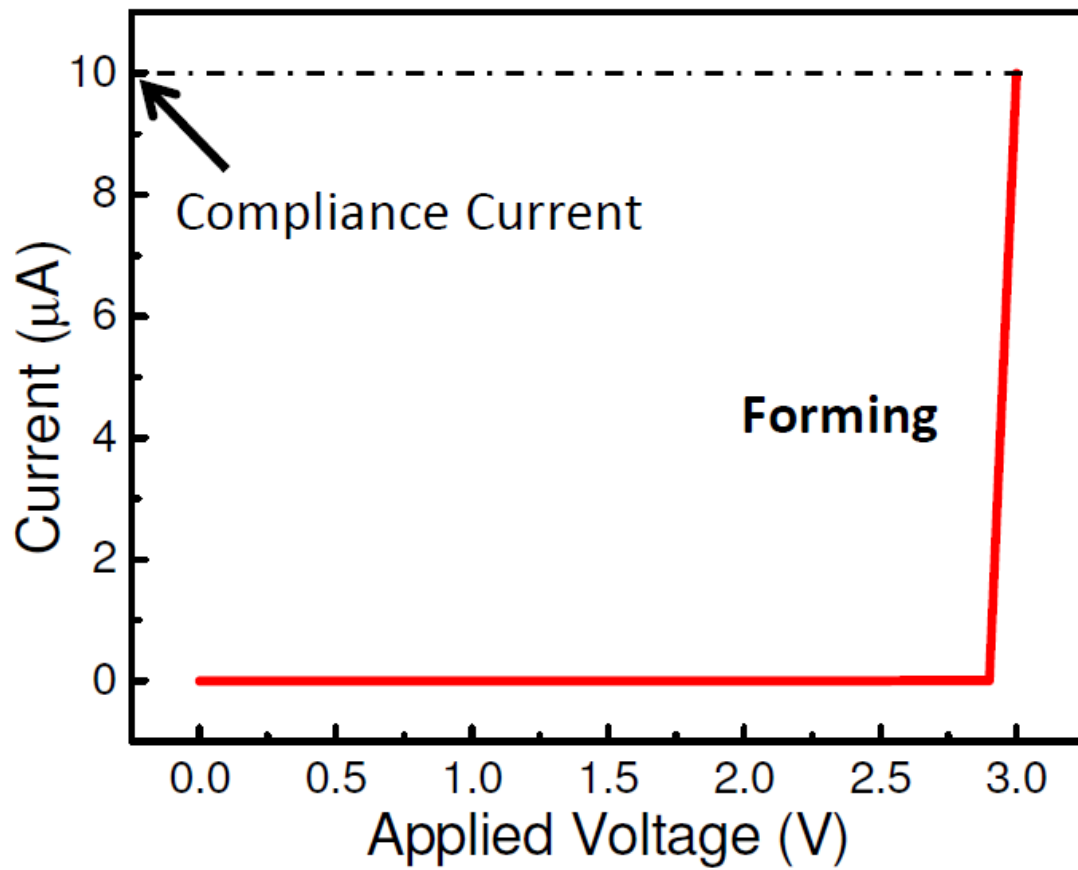
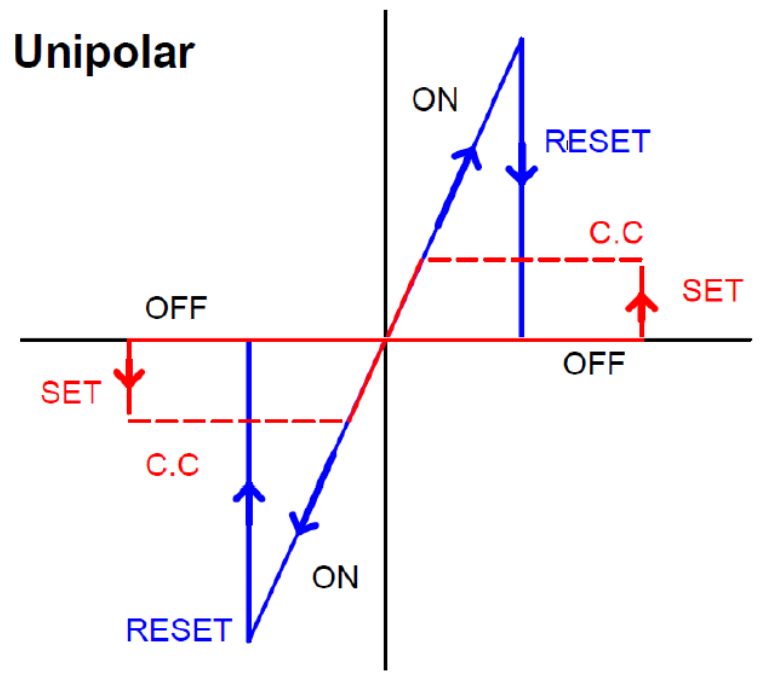
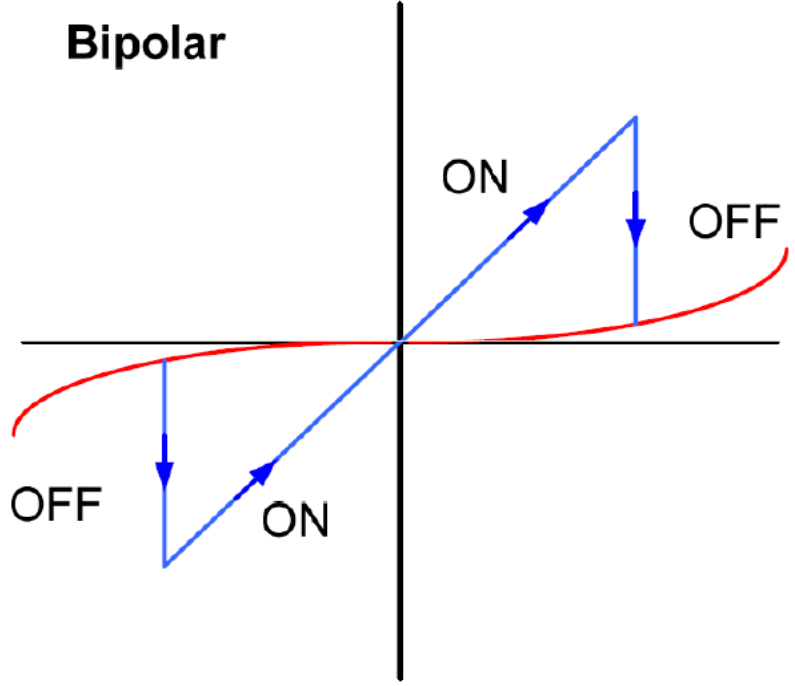


Fig. 2.5 Forming: The predominant step before resistive switching operation.



(a)



(b)

Fig. 2.6 Two terminologies of RRAM. (a) unipoalr (b) bipolar.

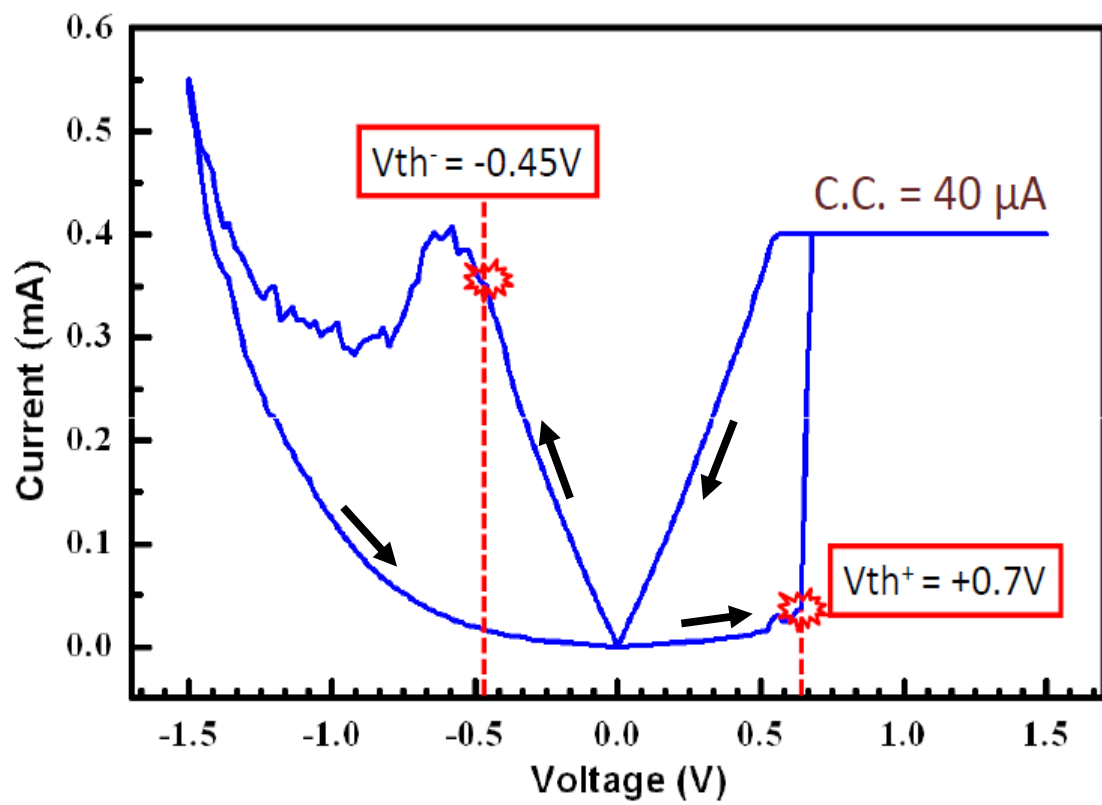


Fig. 2.7 Basic characteristics of the test RRAM cells in this thesis.

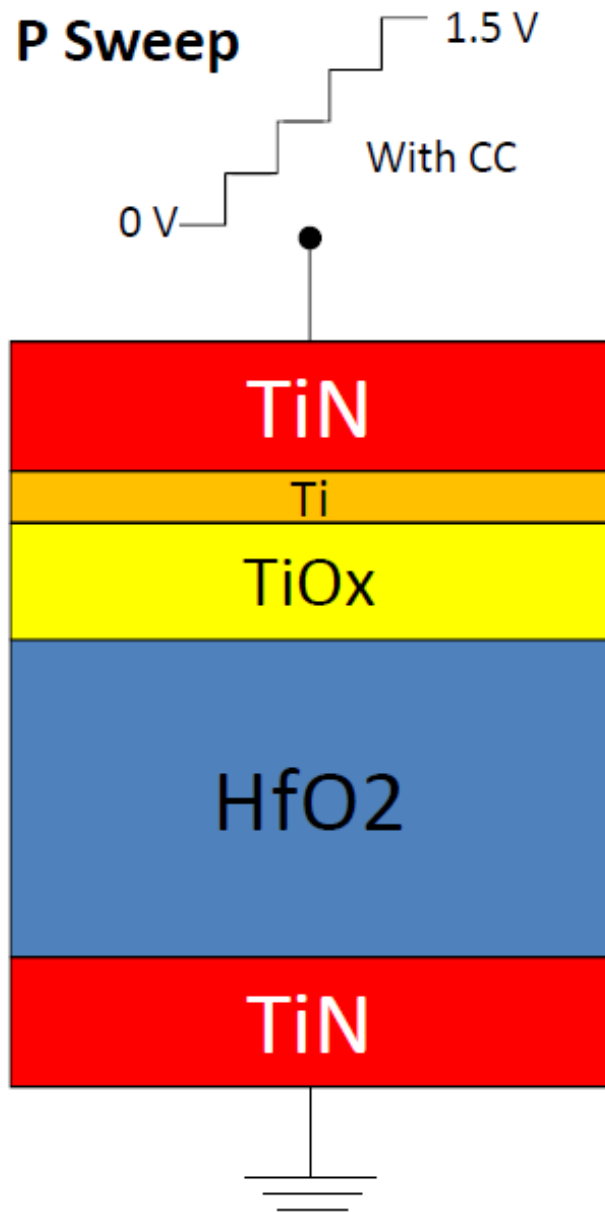


Fig. 2.8 Illustration for positive sweep operation.

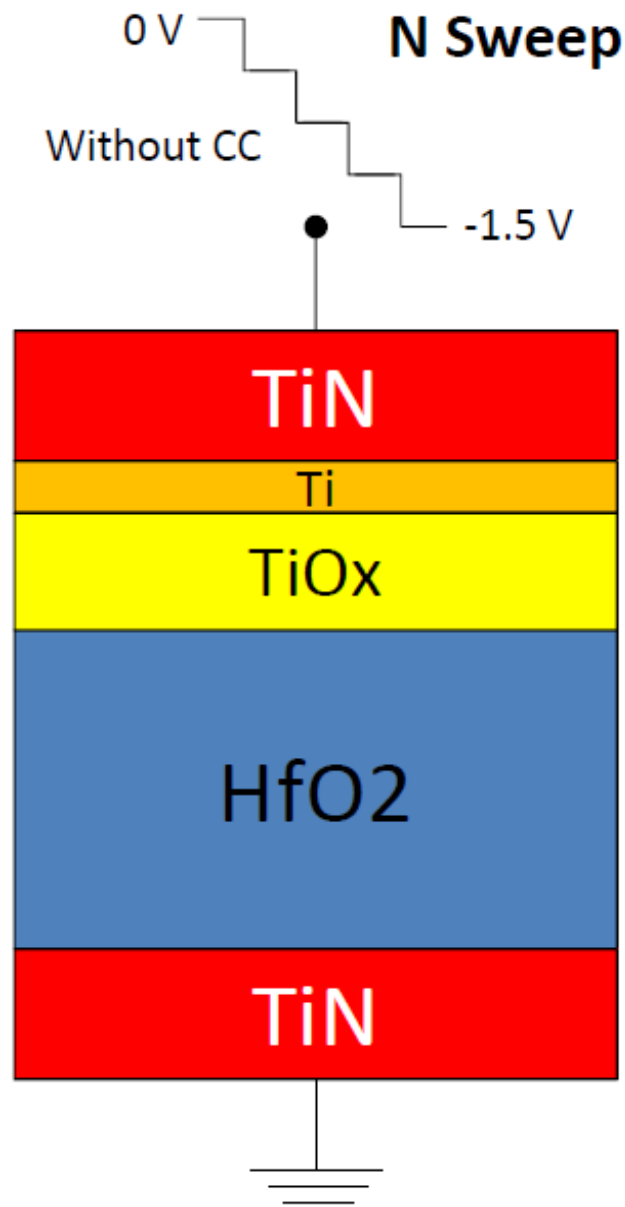


Fig. 2.9 Illustration for negative sweep operation.

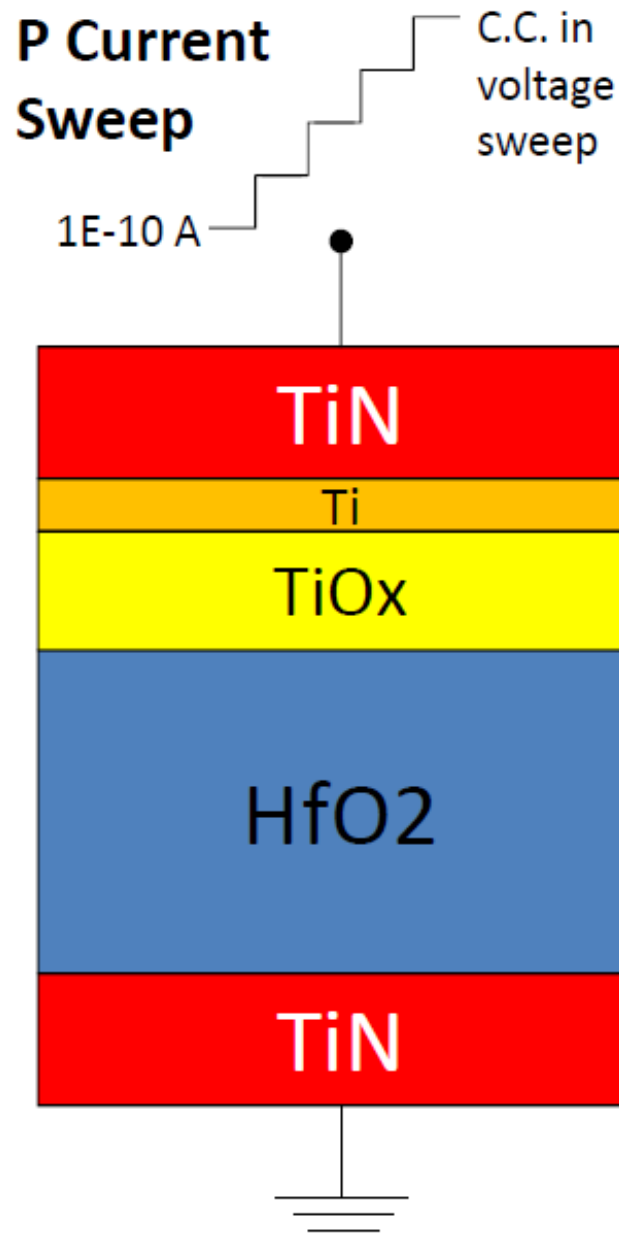


Fig. 2.10 Illustration for positive current sweep

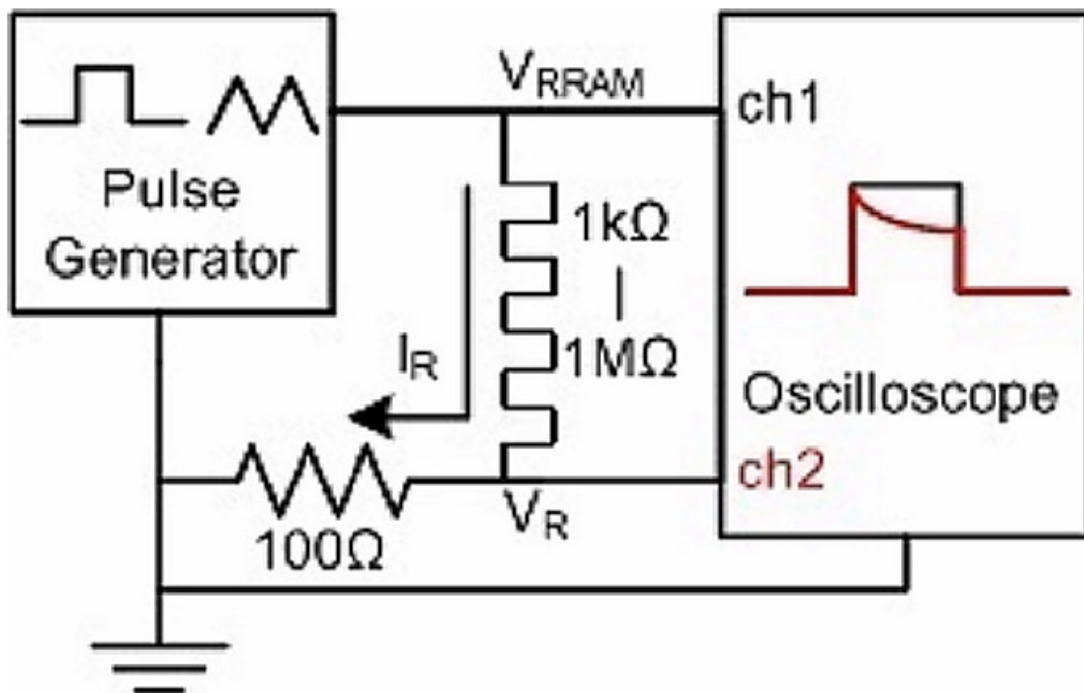


Fig. 2.11 Measurement setup for series resistor sensing method.

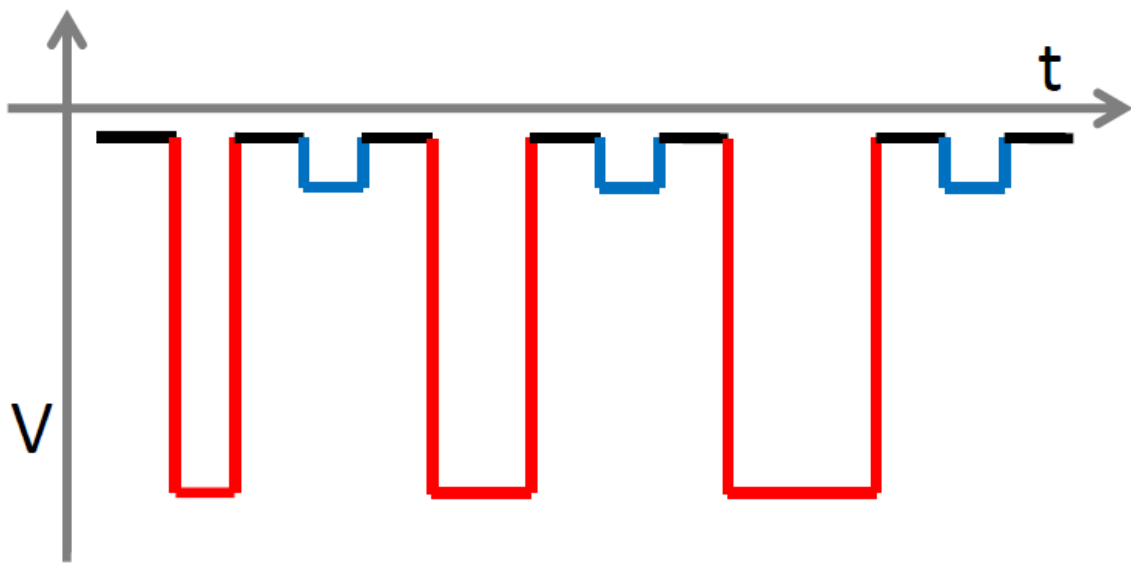


Fig. 2.12 Continuous pulses measurement: The red pulse is used for RESET, and the blue lines indicate a small read voltage after each time-varying RESET pulses.

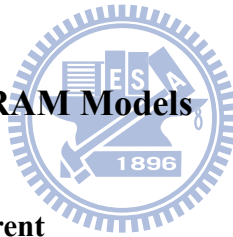
Chapter 3

Physical Model of Transition Metal Oxide Based RRAM

3.1 Introduction

There are three parts in this chapter. First in Chapter 3.2, we discuss all reported RRAM models about their validity. Then, we propose a possible universal model to include all RRAM phenomena. We utilized WKB approximation to quantitatively describe the tunneling model that we proposed, and finally, we will show the simulation result with real experimental data to verify our model.

3.2 Discussion on Known RRAM Models



3.2.1 Space Charge Limited Current

A number of literatures refer RRAM current to be the so-called “space-charge-limited current”, abbreviated as SCLC, due to the special nonlinear current characteristic of RRAM [3.1, 3.2]. According to Fig. 3.1 [3.2], we can clearly tell that when applied voltage is small, RRAM current is proportional to the applied voltage, just like an ohmic resistor. As the applied voltage increases, the current-voltage relation then follows a square law. This behavior is similar to the theory of SCLC, which contains both linear and square law of applied voltages [3.3]. There are three equations used in SCLC theory :

1、 In the mobility region (Mott-Gurney law)

$$J = \frac{9\epsilon_s \mu V^2}{8L^3} \quad (3.1)$$

2、 In the velocity saturation region

$$J = \frac{2\epsilon_s v_s V}{L^2} \quad (3.2)$$

3、 In the velocity saturation region

$$J = \frac{4\epsilon_s}{9L^2} \left(\frac{2q}{m^*} \right)^{1/2} V^{3/2} \quad (3.3)$$

The space charge is determined by both the doping concentrations and the free-carrier concentrations. When the injected carrier is larger than its equilibrium value as well as the doping concentration, the space-charge effect is said to occur [3.3]. In semiconductor, the carrier velocity is proportional to the electric field under low electric field, and saturated under high field. According to this, we should expect a square law at low applied voltage and a linear law at high applied voltage, which contradicts the RRAM measurement result. Beyond this, we can see the current increase more rapidly beyond the square law region, where SCLC theory fails obviously. Based on these contradictions, we can say that SCLC is not a good model for RRAM current behavior.

3.2.2 Schottky Barrier Thermionic Emission

Another reported RRAM current characteristic is Schottky barrier thermionic emission, which is also based on measured current-voltage characteristic. As shown in Fig. 3.2, the RRAM current is actually proportional to the exponential of the square root of applied voltage [3.4]. To understand the origin of this relation, we have to first realize the fundamental of the theory. The current characteristic of Schottky barrier thermionic emission is shown below [3.5]:

$$J = A^{**} T^2 \exp \left[-\frac{q \left(\phi_{B0} - \sqrt{q E_i / 4 \pi \epsilon_i} \right)}{kT} \right] \left[\exp \left(\frac{q V_f}{kT} \right) - 1 \right] \quad (3.4)$$

$$A^{**} = \frac{f_p f_Q}{1 + (f_p f_Q v_R / v_D)} \frac{4 \pi q m^* k^2}{h^3} \quad (3.5)$$

The square-root law comes from the E_i term in equation (3.4), which means the electric field inside the insulator. First of all, the thermionic emission is a diode-like behavior. That is to say, when the applied voltage is forward biased, the current will exponentially increase with applied voltage. This opposes to the RRAM current characteristic, which shows reverse bias characteristic for both positive and negative applied voltage.

The supporters of Schottky barrier thermionic emission refer the RRAM switching to the change of Schottky barrier height. In their works, the barrier height is extracted by fitting current characteristic with the formula above. However, a more accurate method is done by temperature experiments. Our result, as shown in Fig. 3.3, and another paper [3.6] show that the Schottky barrier height does not change in different high resistance states. Also, the RRAM current seems to be rather insensitive to temperature [3.7, 3.8]. As a result, we can certainly say RRAM current cannot be explained by Schottky barrier thermionic emission.

3.2.3 Frenkle-Poole Transport

One of the conduction mechanisms through an insulator is controlled by inter-trap tunneling, which can be described by Frenkle-Poole transport. In Frenkle-Poole transport, the electron enters the trap site first by tunneling, and then leaves by thermionic emission. The current characteristic of Frenkle-Poole transport is described by the following equation [3.5]:

$$J \propto E_i \exp \left[-\frac{q \left(\phi_B - \sqrt{qE_i / \pi \epsilon_i} \right)}{kT} \right]. \quad (3.6)$$

Nevertheless, this equation fits only the pre-forming current of RRAM [3.9]. A possible explanation is that this theory is adaptable when the trap density is low. But the conduction filament is actually a bundle of dislocations composed of extremely localized traps [3.10]. These dislocations form a high conductance passage for electron transport instead of using thermionic emission.

3.2.4 Coupled Ionic Drift and Electronics

The first adapted RRAM switching mechanism is described by the ion motion under applied electric field [3.11], but the device size then is of the order of millimeter. Recently, the HP research group proposed a modified coupled ionic drift and electronics model in *Nature* to explain RRAM memristive characteristic [3.12]. The main idea is illustrated in Fig. 3.4 and the current model is described by:

$$i(t) = \frac{1}{R_{ON} w(t) + R_{OFF} (1 - w(t))} v(t) \quad (3.7)$$

and

$$w(t) = \mu_v \frac{R_{ON}}{D^2} q(t) \quad (3.8)$$

There are some assumptions made in this model. One of them is the ion mobility which is independent of applied electric field. This assumption is unrealistic for modern nano-scale device. Another one is assuming that there is not any threshold to initiating ionic motion. According to this assumption, the RRAM will eventually change state as long as the bias is applied for enough time. This is contradicted to every known RRAM measurement result, which always exhibits a certain threshold voltage both in SET and RESET operation. The threshold is important for a memory device since it can avoid

disturbance during read or programming of the other cells. Third, the ion motion is assumed to be controlled only by electric field intensity without considering the polarity. The result will make the switching behavior similar in both SET and RESET processes. However, the basic characteristic shown in Fig. 2.7 indicated that SET and RESET process obviously show asymmetric behaviors. In summary, for large scale device, RRAM behavior can be well explained by ionic motion, but for nano-scale device, we must develop some new models since quantum mechanics may play a significant role in electron transport.

3.3 Theory of Tunneling Model

3.3.1 Introduction

In order to effectively improve RRAM performance, it is crucial to find out an exact model for RRAM switching mechanism. In previous section, we already deliberated that none of the existing model can fully explain all experimental phenomena of RRAM. Still some of the concepts in those models are worthy of reference. First, the exponential relationship between the current and the square root of applied voltage in both Schottky barrier thermionic emission and Frenkel-Poole transport models is a key. We also found this characteristic under small applied voltage, as shown in Fig. 3.5. The origin of this relation comes from image force induced barrier lowering [3.13]. This characteristic suggests there is indeed a barrier hindering electron transport. We have already shown that barrier height doesn't change for different states, so we may assume that it is the barrier "width" which is changing. This hypothesis seems reasonable because the conduction filament length will extend or shrink as ionized oxygen vacancies moves under applied electric field and thus the distance between the filament and the electrode will change. The depletion region near the interface forms a nano-scale tunneling barrier which is the origin of RRAM current and resistance switching.

In order to verify our tunneling barrier width model, we adopted a simple semi-quantum simulation method called WKB approximation [3.14] to describe RRAM

current behavior. We found it successfully fits experimental data and is very useful to further describe all problems which cannot be explained by other models.

3.3.2 Formulae and Parameters for Simulation

Since the cross section of a single conduction filament is normally few nm^2 , which is relatively small compared to total electrode area (up to μm^2), so we consider only one dimension potential barrier and assume the conduction filament is a cylinder with 4 nm^2 cross section, as shown in Fig. 3.6. The tunnel barrier width “d” is the only variable in the following equations.

According to WKB approximation, the tunneling probability is defined as :

$$P = \exp\left(-\frac{2}{\hbar} \int_0^d \sqrt{2m^* q |E - V|} dx\right) \quad (3.9)$$

where m^* is the effective of the dielectric, $|E - V|$ is the absolute difference between electron kinetic energy, and potential barrier. The potential barrier is defined by the conduction band energy difference between the electrode or trap level of conduction filament and the depleted dielectric, which is initially constant. However, in the last section, we already mentioned we have to include image force induced barrier lowering to satisfy RRAM current characteristic. So, the energy difference now becomes a distance- and voltage-dependent equation as below:

$$|E - V| = \phi_i - \frac{q^2}{16\pi\epsilon_i x} - q \frac{V_i}{d} x \quad (3.10)$$

where ϕ_i , ϵ_i , and V_i are the initial barrier height, dielectric constant, and voltage drop of the dielectric layer. The integration now can be done as long as the constants are known.

At first, we took the parameters of hafnium oxide for simulation but the result was

inconsistent with real measurement data. However, it has been published that the formation energy of titanium oxide is lower than hafnium oxide [3.15]. Therefore, we assumed the tunneling dielectric layer is actually titanium oxide and took the parameters of titanium oxide to perform the simulation again. The result was surprisingly good. This result is a great revolution. It means the dielectric material is not the only factor that affects RRAM performance, the choice of electrode material is also a great issue. Fig. 3.7 (a) illustrates possible schemes in LRS and HRS. According to the motion of oxygen ion, a new titanium oxide layer should be formed near the bottom interface. There is also a titanium oxide layer initially formed right after titanium sputtering, but the area of the top layer is much larger than the bottom layer. In order to satisfy the charge conservation, the total charge used in redox reaction is the same for both SET and RESET process. Therefore, if the charge densities of both layers are equal, the width variation of the bottom layer must be greater than the top layer. That is to say, it is the bottom titanium oxide that controls the RRAM resistance switching. Fig. 3.7 (b) shows the band diagram along the conduction path. Assuming the top layer does not share the applied voltage, we can thus drive the equation as given below based on Gauss's law:

$$V_i = V_{TiOx} = \frac{V_A}{1 + \frac{\epsilon_{TiOx} d_{HfO2}}{\epsilon_{HfO2} d_{TiOx}}} \quad (3.11)$$

where V_A is the applied voltage. Table 3.1 includes all the parameters we used in the simulation [3.16-3.19]. One thing is noticeable that the barrier height and effective mass used for positive and negative bias conditions are different, indicating different conduction band characteristics between electrode and the conduction filament.

3.3.3 Analytical RRAM Low-Field Current Model

Although the integration mentioned above can be numerically done to fit any measured RRAM current characteristic, it is hard to describe RRAM behaviors in this form. We need an analytical formula for further discussion. If the barrier width is large

enough so that the barrier distortion can be seen as effective barrier height lowering, we can simplify the integration and multiply it by a pre-factor [3.20]:

$$I_{RRAM} = \frac{Aq^2}{16\pi^2\hbar\varepsilon_{TiOx}\phi_i'} \cdot \frac{V_A}{d_{TiOx}} \exp \left[-\frac{4\sqrt{2qm^*}(\phi_i')^{3/2}d_{TiOx}}{3\hbar|V_{TiOx}|} \left[1 - \left(1 - \frac{|V_{TiOx}|}{\phi_i'} \right)^{3/2} \right] \right] \quad (3.12)$$

where A is the conduction filament cross section and ϕ_i' is the effective barrier height defined as:

$$\phi_i' = \phi_i - \sqrt{\frac{qV_{TiOx}}{4\pi\varepsilon_{TiOx}d_{TiOx}}} \quad (3.13)$$

Equation (3.11) can be further reduced if the voltage drop on titanium oxide is much smaller than the initial barrier height, the exponential term will become voltage-independent, i.e.,

$$I_{RRAM} = \frac{Aq^2}{16\pi^2\hbar\varepsilon_{TiOx}\phi_i'} \cdot \frac{V_A}{d_{TiOx}} \exp \left[-\frac{2\sqrt{2qm^*}\phi_i'}{\hbar} d_{TiOx} \right] \\ \propto \frac{1}{d_{TiOx}} \exp \left[-\frac{2\sqrt{2qm^*}\phi_i'}{\hbar} d_{TiOx} \right] \quad (3.14)$$

Equation (3.13) is exactly the formula of direct tunneling through a constant barrier height. Based on equation (3.12), we can transform the RRAM current state which is measured by specific read voltage (usually 0.1V) into the effective barrier width.

3.4 Simulation Result and Discussion

Figure 3.8 shows the simulation result with real experimental data and the effective tunneling barrier width are shown in the legend. The maximum sweep voltage is $\pm 0.3V$

to avoid resistance switching, and this condition also meets the requirement of low field assumption in our model. Fig. 3.9 shows the relation between read resistance and RESET voltage. The resistance first grows proportional to the RESET voltage, and then exponentially. This behavior can be fully understood by equation (3.13). If we set the applied voltage as a constant, the resistance will be:

$$R_{RRAM} \propto d_{TiOx} \exp \left[\frac{2\sqrt{2qm^* \phi_i}}{\hbar} d_{TiOx} \right] \quad (3.15)$$

As the tunneling barrier width is small, the resistance is proportional to it. When the width further increases, then the exponential term dominates. However, combining equation (3.14) with Fig. 3.9 gives the following interesting relation:

$$d_{TiOx} \propto V_{RESET} \quad (3.16)$$

This relation implies there is a critical electric field to initialize ionic drift and RESET process. As long as the width grows enough to make the electric field less than the critical value, the RESET process will eventually stop. The extracted critical electric field is about 1.2MV/cm.

The tunneling model also helps us to understand why temperature makes little effect on RRAM current. Since the temperature only affects the average kinetic energy of electrons by $3kT/2$, it makes finite effect on the effective barrier height, which is inside a square root. The temperature-insensitive characteristic makes RRAM a good memory even under extreme environment.

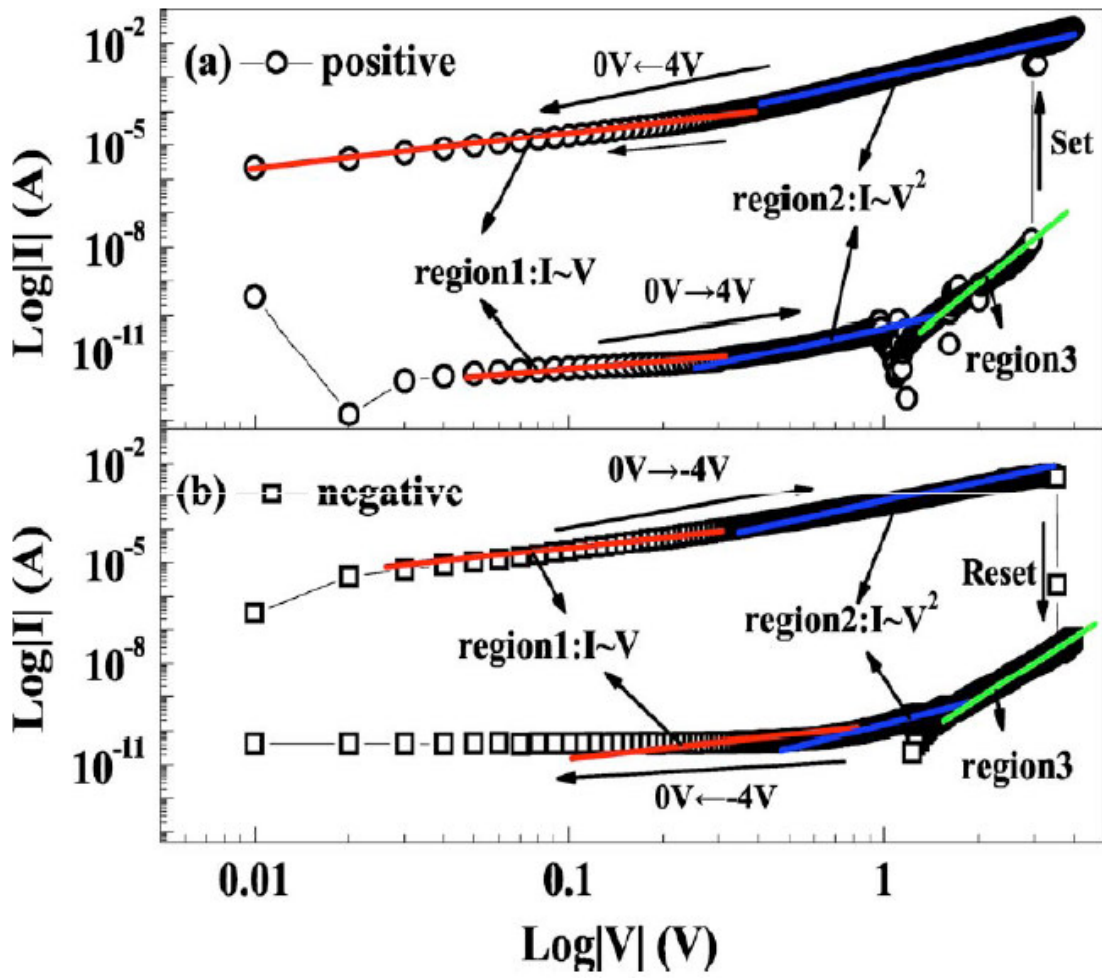


Fig. 3.1 SCLC model: The red line indicates the Linear relation. The blue line indicates the Square law region.

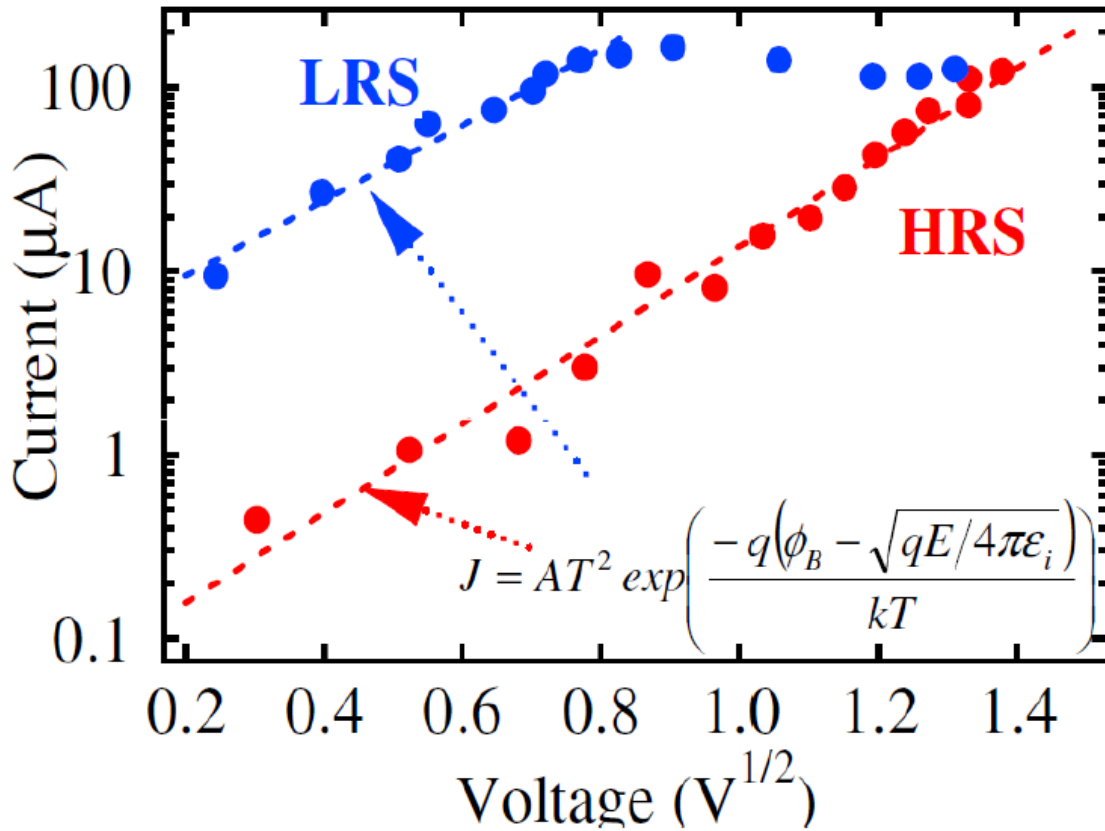
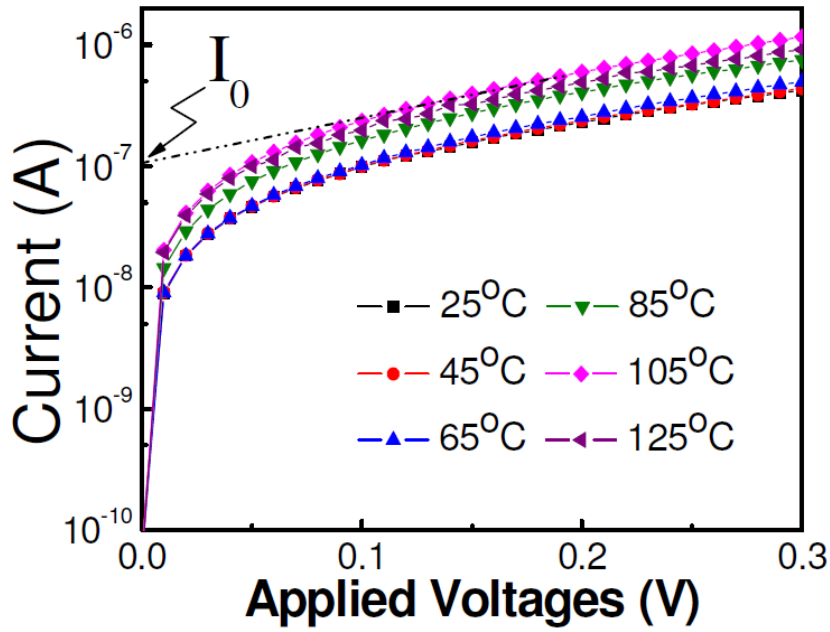
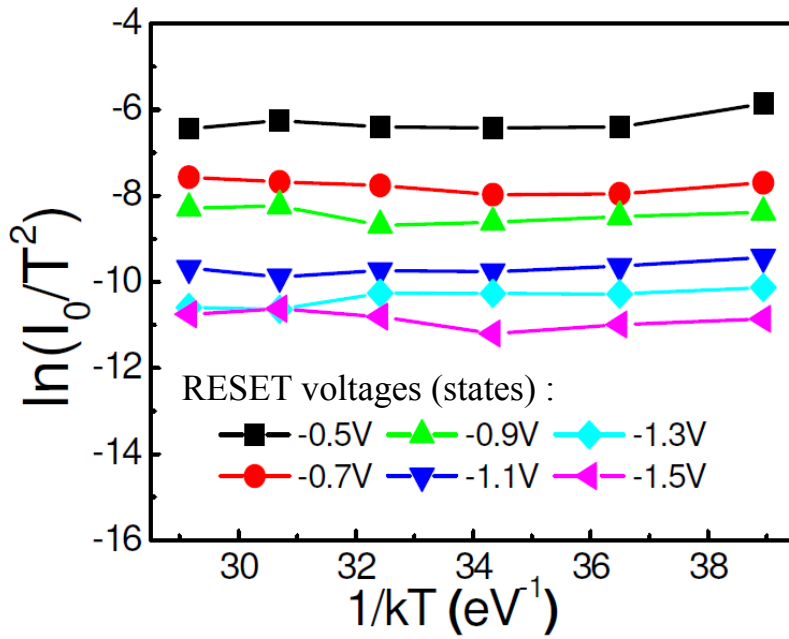


Fig. 3.2 Schottky barrier thermionic emission: This figure indicates the current seems to be proportional to the exponential of the square root of voltage.

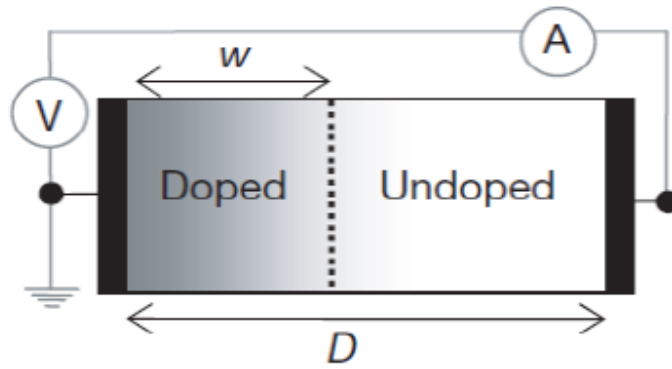


(a)



(b)

Fig. 3.3 Temperature experiments. In (a), the slopes of each curve don't vary with temperature. In (b), it shows the barrier height is very small and doesn't change for different resistance state.



Undoped:



Doped:

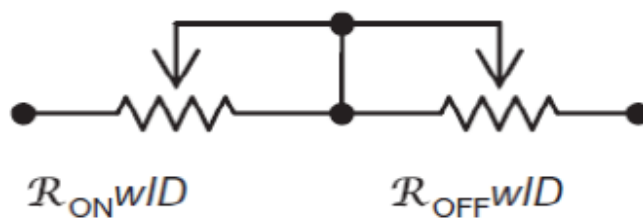


Fig. 3.4 Illustration for coupled ionic and electronic model. This model combines ionic drift and a series connection between high and low doping concentration regions.

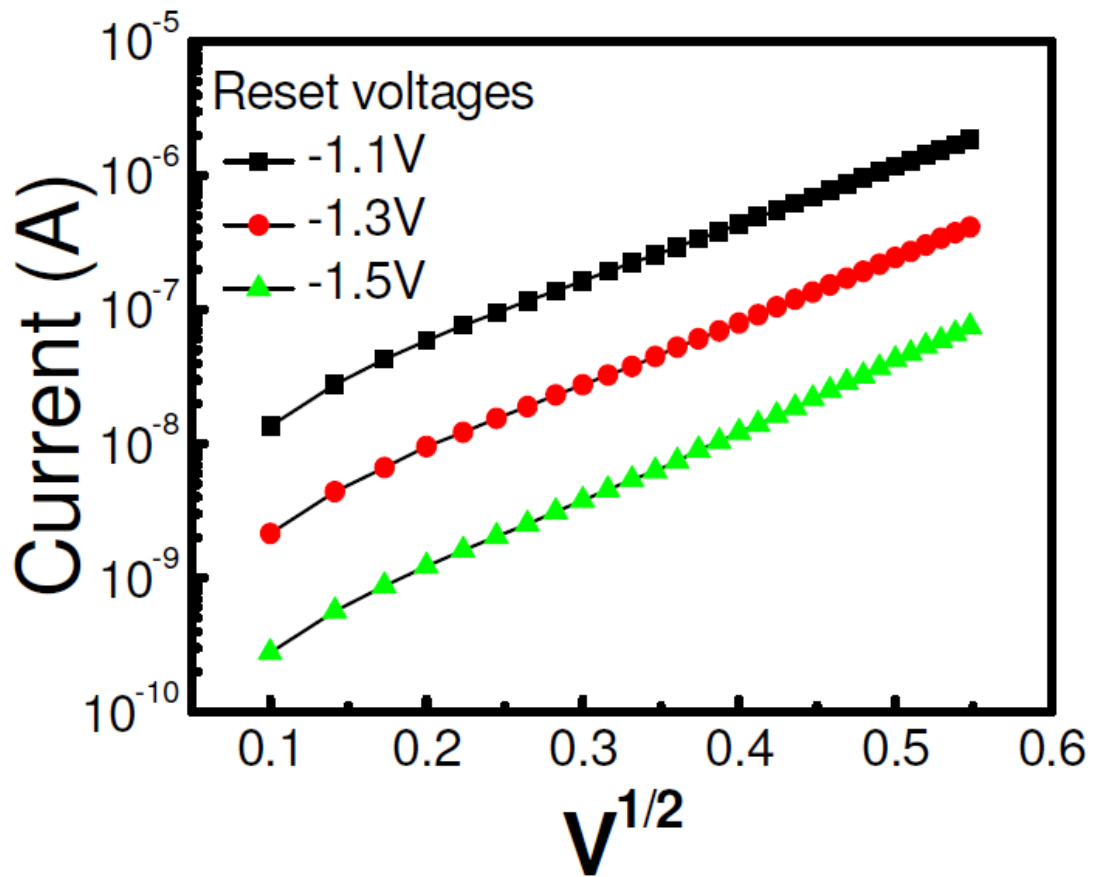
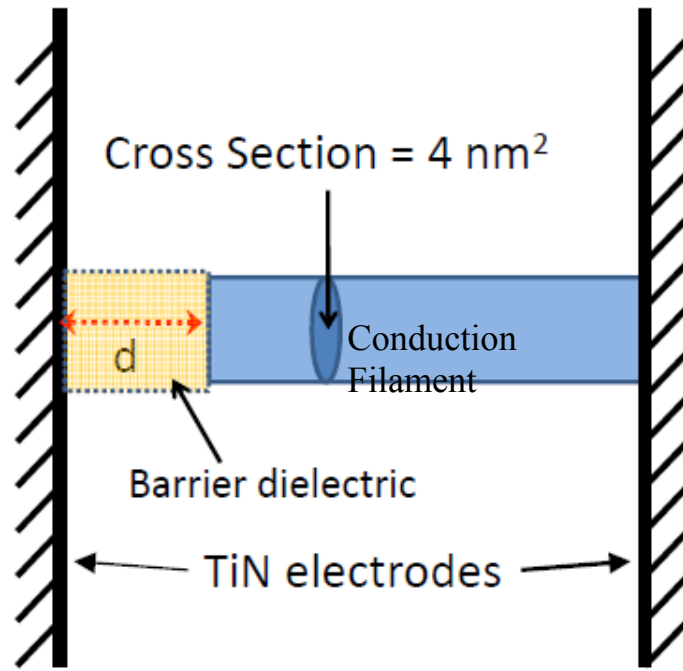
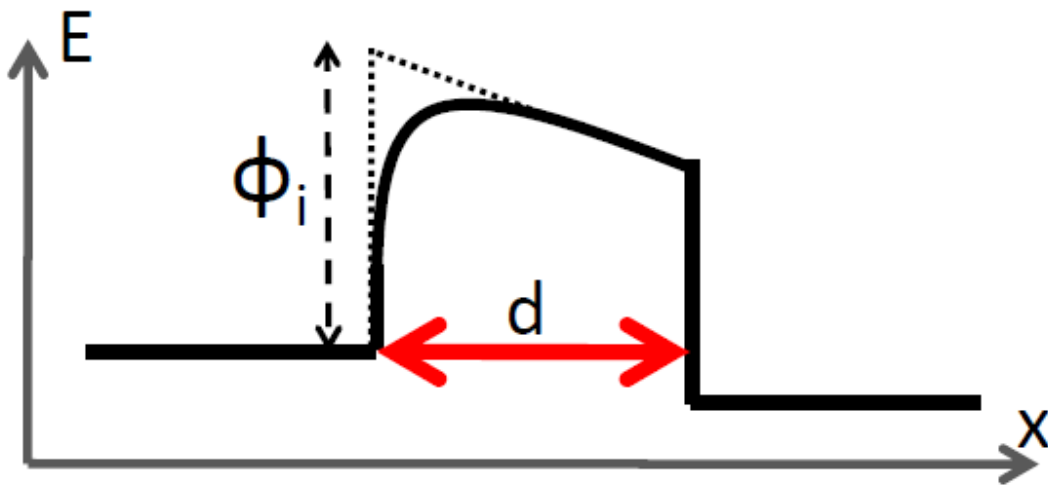


Fig. 3.5 Small voltage sweep. Our measurement also shows linear relation.

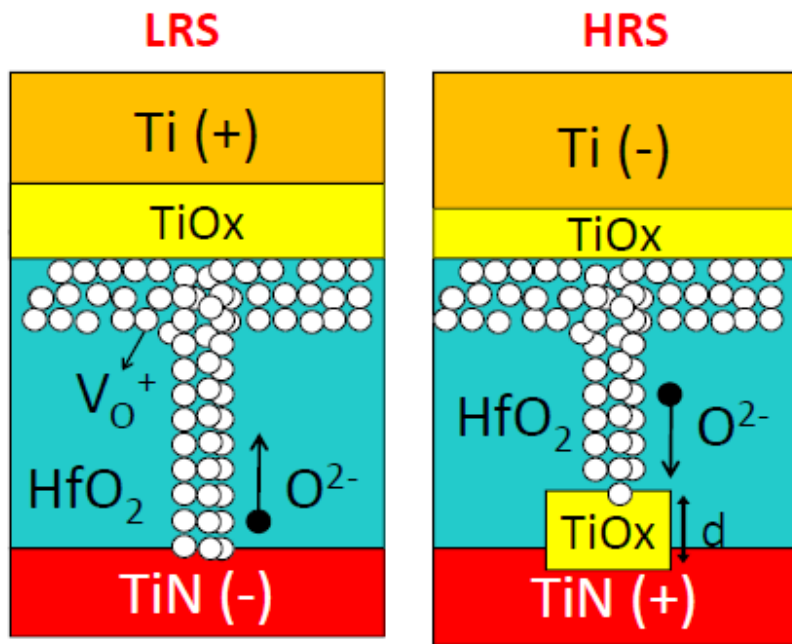


(a)

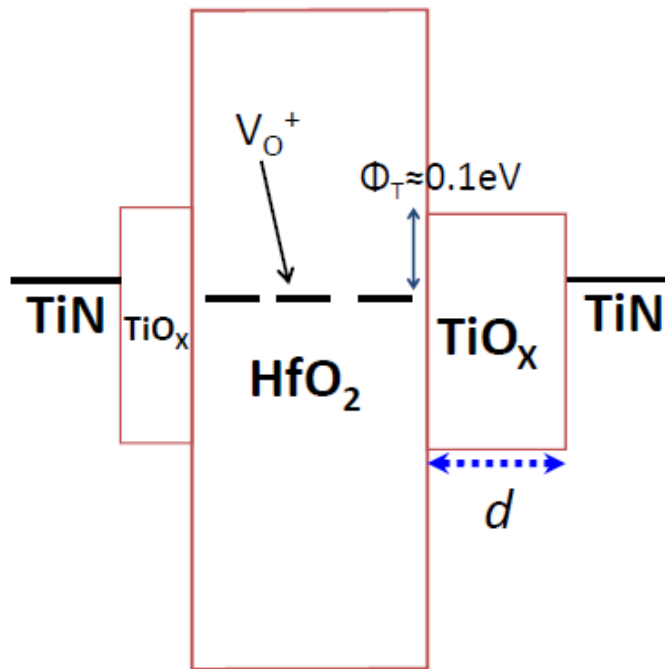


(b)

Fig. 3.6 Simulation Conditions: (a) The proposed tunnel width varying model. (b) The barrier profile used for simulation. The barrier distortion is due to image force induced barrier lowering.



(a)



(b)

Fig. 3.7 (a) Possible schemes in RRAM for LRS and HRS. (b) The band diagram of RRAM in HRS.

Parameters	Values
HfO ₂ dielectric constant	25
TiO _x dielectric constant	46
Initial barrier height (positive bias)	0.074eV
Effective mass in TiO _x (positive bias)	13m ₀
Initial barrier height (negative bias)	0.09eV
Effective mass in TiO _x (negative bias)	9.6m ₀

Table. 3.1 Device parameters used in simulation.

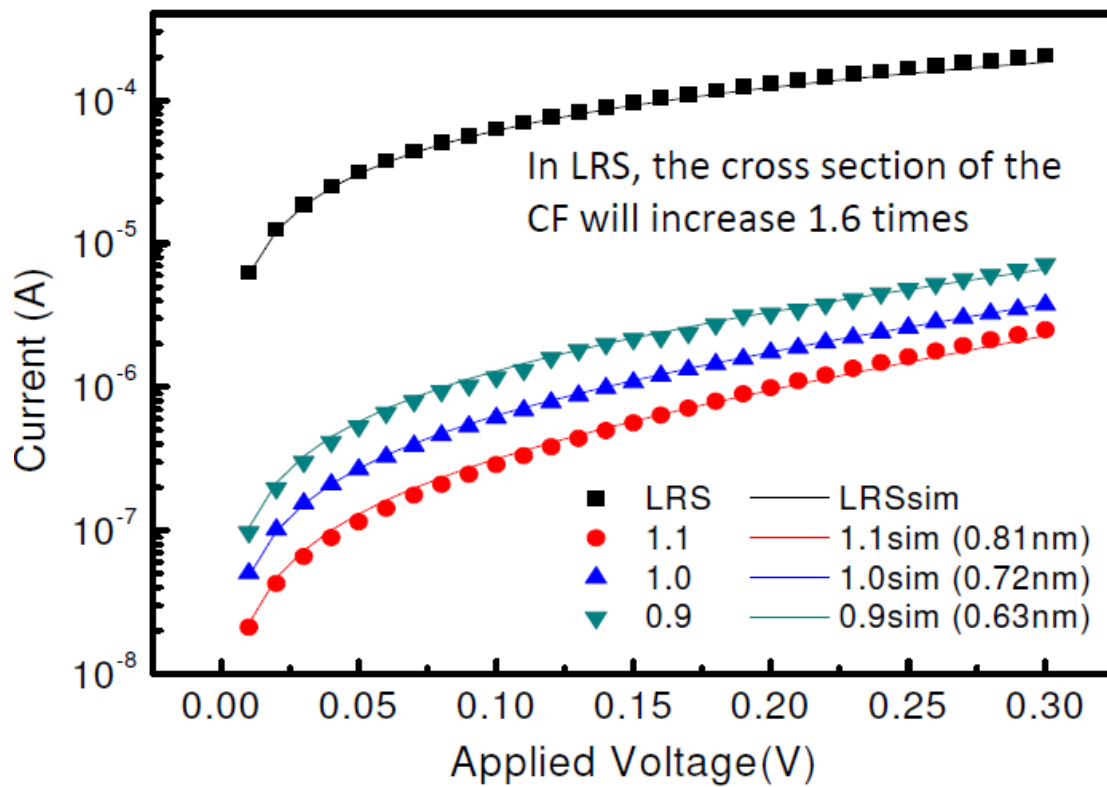


Fig. 3.8 Simulation results. The dots are measurement data, and the lines are simulations. Simulation shows the LRS cross section increases 1.6 times.

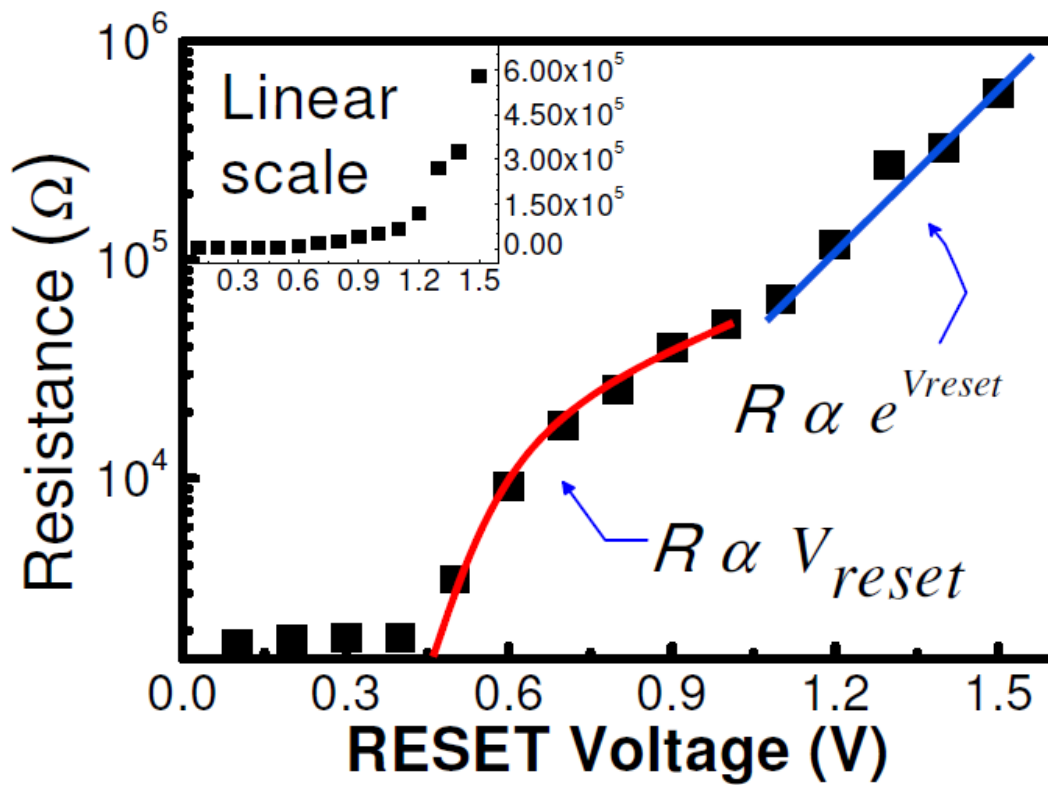


Fig. 3.9 The relation between multi-level resistance states and the RESET voltages.

Chapter 4

Switching Time Behavior of RRAM

4.1 Introduction

In this chapter, we discuss the transient switching mechanism of RRAM on the basis of single conduction filament and tunneling model. First, we demonstrate the measurement result using the continuous pulse method mentioned in Chapter 2. We found interesting behaviors during RRAM switching and thus we propose a series of models. These models provide a good reference for improving RRAM switching time.

4.2 Transient Measurement



Figure 4.1 shows the transient measurement result by continuous pulse method. We show only RESET process since SET process finishes in 100ns, which is beyond our test station resolution limit. The physical origin causing the difference between SET and RESET switching mechanism will be discussed in the next chapter.

We can clearly see there are three phases during RESET switching process, which is demonstrated in Fig. 4.2. First, it remains in LRS for a certain time. Second, the width increases linearly with logarithmic time, and finally it saturates to a certain level. The switching time is therefore defined by the total time of the first and second phases. To improve the speed of RRAM switching, it is important to find out the origin of these two

phases. The third phase has reached dynamic equilibrium, so it shall be connective with DC measurement.

4.3 Discussion

4.3.1 Phase I – Ionic Transport Region

In Fig. 4.1, we found the duration of “Phase I” decreases exponentially as the RESET voltage increases linearly. The duration of “Phase I” is determined by how fast the oxygen ion confined in the electrode reaches the conduction filament. Obviously, the ion drift velocity is no longer linear with electric field as in bulk material. Some literatures also reported under a strong electric field, the ion migration activation energy can be greatly lowered [4.1-4.3]. A simple rigid point-ion model has been proposed to explain this nonlinear ionic motion, illustrated in Fig. 4.3 [4.3-4.5]. Here we assume the positive ions are fixed and periodically distributed. The period is “a” and activation energy is “ U_A ”. The mobile negative ions have to conquer the potential barrier to migrate into the nearest site. The applied electric field deform the potential well and change the potential barriers by $\pm qEa/2$, positive for the barrier opposite to migration direction and vice versa. The average velocity thus can be described by:

$$v \approx fae^{-\frac{U_A}{k_B T}} \sinh\left(\frac{qEa}{2k_B T}\right) \quad (4.1)$$

where f is the frequency ion attempts to escape from the well. The velocity can be rewrite into a classical form:

$$v = \begin{cases} \mu E & E \ll E_0 \\ \mu E_0 e^{E/E_0} & E \sim E_0 \end{cases} \quad (4.2)$$

where $E_0 = 2k_B T / qa$ is the characteristic critical field, which is typically about 1MV/cm.

The low field mobility is redefined by:

$$\mu \approx \frac{qfa^2}{k_B T} \exp\left(-\frac{U_A}{k_B T}\right) \quad (4.3)$$

According to equation (4.2), the ion migration time can be derived:

$$T_{migration} = \frac{d_0}{v} = \frac{d_0}{\mu E_0 \exp\left(V/d_0 E_0\right)} \quad (4.4)$$



where d_0 is the LRS tunnel barrier width. In accordance with equation (4.4), as the applied RESET voltage increases, the ion migration will decrease exponentially, which is consistent with measurement result. To improve ion migration, one should increase the ion mobility by choosing a lower potential material.

4.3.2 Phase II – Redox Reaction Region

“Phase II” shows a linear increment of tunnel barrier width with logarithmic time. Since during “Phase I”, plenty of ions migrate through the tunnel barrier and reach the tip of conduction filament, we can then assume the ion concentration no more dominates the reaction. Alternatively, the redox reaction speed becomes the main issue in this phase.

The redox reaction contributes to a partial amount of the measured currents. However, the portion is very small and hard for extraction. In order to qualitatively describe the behavior in “Phase II”, we assume a perfect condition that all tunnel current contribute to reaction. The concept is schematically illustrated in Fig. 4.4. The total charge need for shrinking the conduction filament a distance of dx is:

$$NA dx = I(t) dt = I(x) dx = I_0 x^{-1} \exp(-\gamma x) dx \quad (4.5)$$

where $I_0 \exp(-\gamma x)$ is the a simplified form of our analytical model mentioned in Chapter 3.3.3. Integration both side and we get:

$$T_{reaction} \approx \frac{NA}{I_0 \gamma} d \exp(\gamma d) \quad (4.6)$$

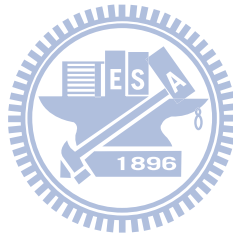


According to equation (4.6), we find it happens to match with the experimental measurement. Although the full contribution assumption is not rational, we can absorb the ratio into the constants on the RHS of equation (4.6). In order to improve reaction speed, one can choose a small γ material, which can be achieved by lower effective mass. A smaller barrier height material also helps due to $I_0 \gamma$ together gives an reciprocal of square root of barrier height.

Another thing worth mentioning is the slope of each “Phase II” curve, which is increasing along with RESET voltage. This behavior can be explained by the magnitude of I_0 in equation (4.6), which is proportional to applied voltage.

4.3.3 Phase III – Saturation Region

After the fast transition in “Phase II”, each curve enters the third region with a rather slower incremental rate. We found that each curve finally separated by a constant value, which is consistent with our DC measurement result: $d \propto V_{RESET}$. In this region, the incremental speed is insensitive to applied voltage. We speculate this is due to the residual ions surrounding the conduction filament. These ions reach the conduction filament by diffusion which is irrelevant to applied voltage.



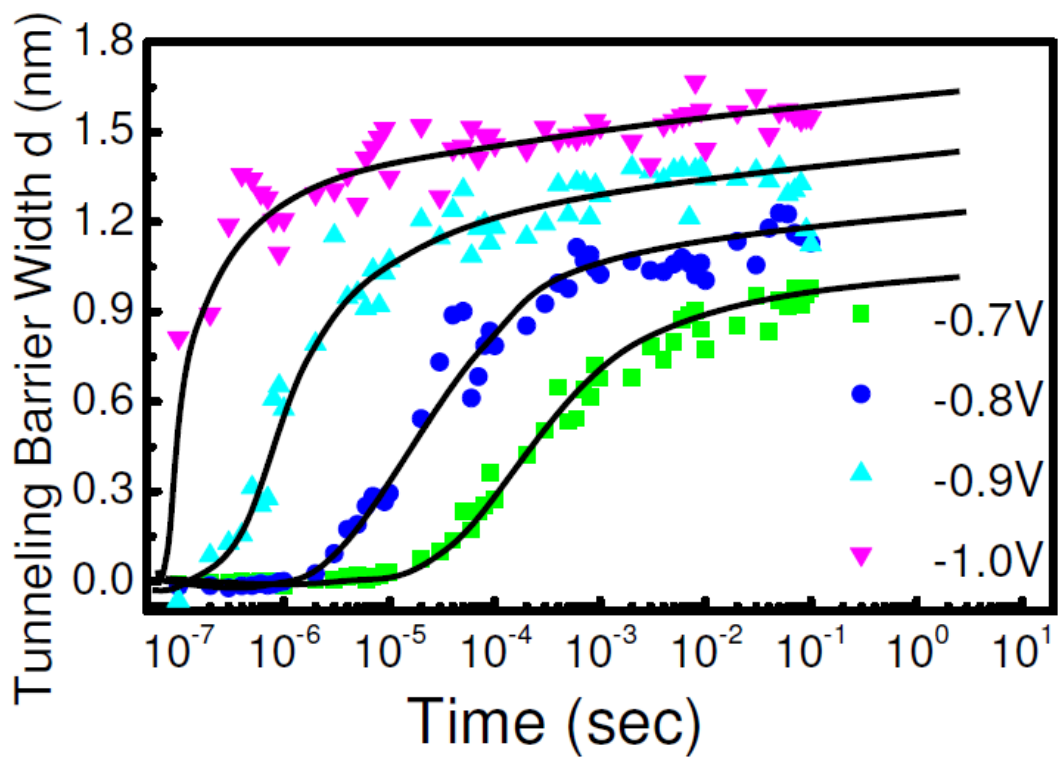


Fig. 4.1 Transient tunneling barrier width variation measured by continuous pulses method.

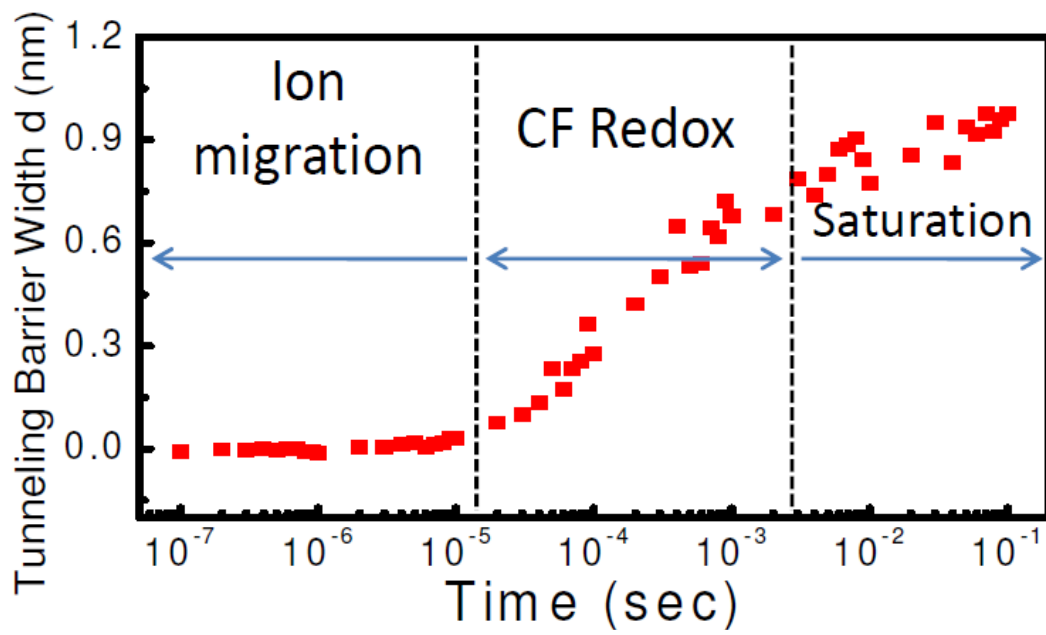


Fig. 4.2 Magnified examination of the curves shown in Fig. 4.1. There are three phases during the RESET process.

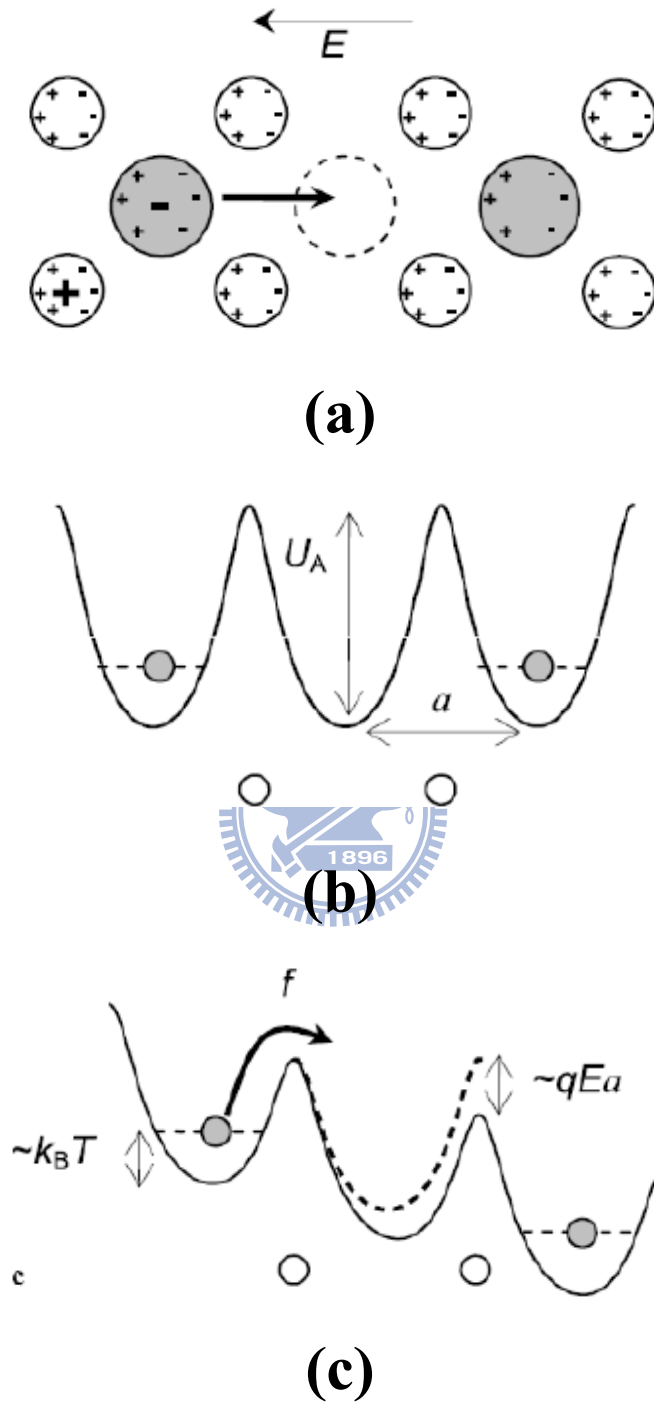


Fig. 4.3 Schematically illustration exponential ionic drift. (a) The mobile negative ions move under electric field. The positive fixed ions create periodic potential barriers. The barrier profiles (b) without and (c) with electric field are also shown.

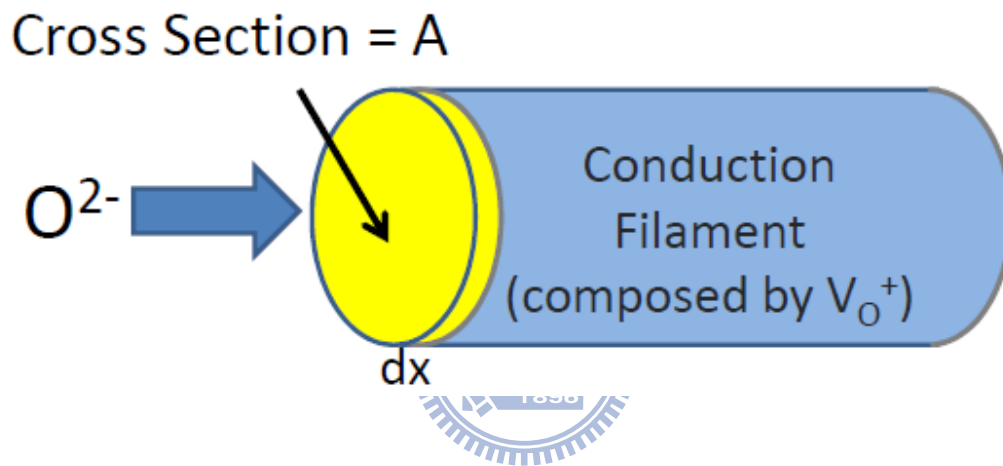


Fig. 4.4 Redox reaction control model. The charge density is N , which is assumed to be uniform throughout the conduction filament. The yellow region represents a small portion of oxygen vacancies to be annihilated by incoming oxygen ions.

Chapter 5

Applications as a Memristor

5.1 Introduction

The functional form of memristor is the relation between charge and magnetic flux, $d\phi = Mdq$. But if this relation is linear; That is to say, M is a constant; it is just identical to a traditional linear resistor. What we are interested is the nonlinear relation, in which M is also a function of q . The RRAM device is smaller than traditional transistor, and because it is a back-end process, it can be easily integrated into existing CMOS fabrication without consuming additional area, which is a great lure for circuit designers. Therefore, it is extremely important to construct a systematic model for RRAM memristive characteristic. The research group of HP in 2008 proposed a diode/resistor model to explain the origin of RRAM hysteresis loop [5.1]. Further in 2009, they proposed a physical model coupling ionic motion and electron transport for simulation [5.2] and a mathematical approach to meet real RRAM transient behavior [5.3]. However, the simulation results are just formally similar to real current-voltage characteristic, but cannot physically explain well some of the phenomena in RRAM switching, such as asymmetric SET/RESET switching rate [5.3], exponential dependence between switching time and reset voltage [5.4], and the temperature effect [5.5].

In previous chapters, we have solved all problems above by using our new tunneling barrier width model. In this chapter, we will also try to discuss RRAM memristive characteristics by this model and evaluate the feasibility of RRAM memristor.

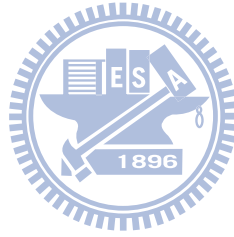
5.2 Experimental RRAM Memristive Characteristic

In the following experiments, we use the series sensing resistor method to measure RRAM transient current. Fig. 5.1 shows the typical current-voltage hysteresis loop for RRAM. The current is measured when we input sinusoidal voltage signal. One can see that changing input signal frequency has significant impact on HRS, which shows great switching time asymmetry between SET and RESET process. In fact, the SET switching time is just few hundred nano-second, while RESET switching time ranges from μ s to ms, depending on applied voltage and required HRS level, as shown in Fig. 5.2. Based on memristor theory, the current-voltage relation has to satisfy the equations as below:

$$v_M(t) = M(q)i_M(t) \quad (5.1)$$

where

$$M(q) = d\varphi(q)/dq \quad (5.2)$$

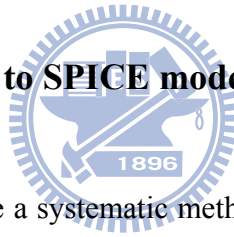


The memristance M , which has the same unit as resistance, must be nonlinear for different time interval, so that one can regard such device as a memristor. Otherwise, it returns to linear resistor as mentioned above. The SET process is too fast to measure the resistance transition accurately, and the transition is unstoppable until it reaches final state. Because the switching time is beyond measurement limit, the measured memristance will be a constant and it cannot be recognized as a memristor. However, the RESET process shows rather good memristive characteristic. Fig. 5.3 reveals transient changing of RRAM current under different RESET voltage. The current decreased several order during switching, but it is rather slow compared to SET process.

5.3 Discussion on Asymmetric Behavior

Figure 5.4 (a) illustrates the band diagram near the bottom interface during SET process. After applying a positive voltage, the distance between electrode and conduction filament shrink and thus the electric field increases. The increasing electric field accelerates ion migration speed, and so does the filament lengthening speed. It turns out that SET process is a **positive feedback** loop once activated, and the final state is controlled by how much your compliance current is [5.6]. On the other hand, shown in Fig. 5.4 (b), the RESET process is a **negative feedback**, since the final states will saturate to certain levels given sufficient time for switching.

5.4 Mathematical Approach to SPICE model



Based on Fig. 5.3, we can use a systematic method to generate charge-flux relation, as shown in Fig. 5.5. The result is shown in Fig. 5.6. The “charge” here equals to the total charge supplied by electrodes. It contains both charges directly tunnel through the barrier and the charges used for redox reaction. As time goes by, the tunnel current may decrease and therefore decrease the charge accumulation rate, as well as the slope of charge-flux plot. Simultaneously, the chemical reaction reaches equilibrium and eventually the charge accumulation will completely come from constant tunnel current, the slope of charge-flux relation also enter constant region. The flux here does not relate to magnetism, it is an alternative representation to show how voltage and time both affect RRAM memristive characteristic.

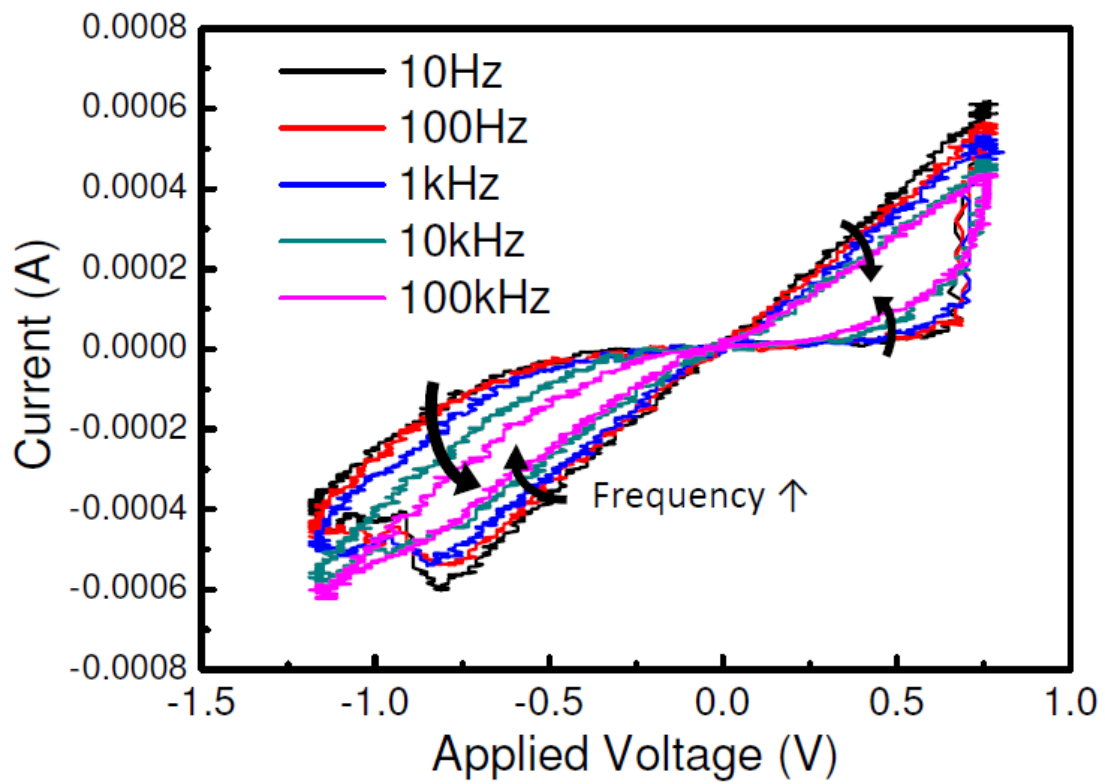
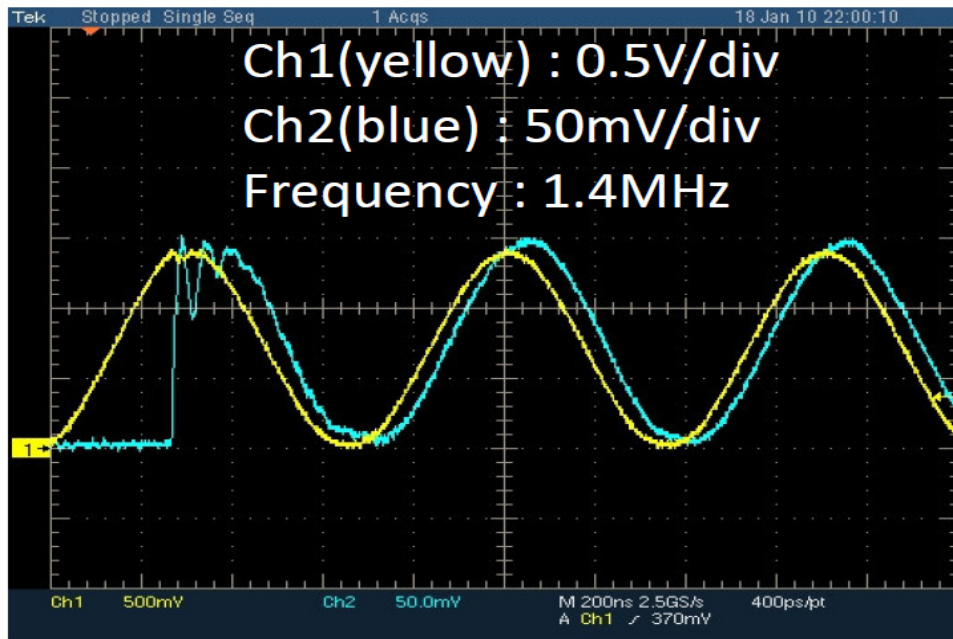
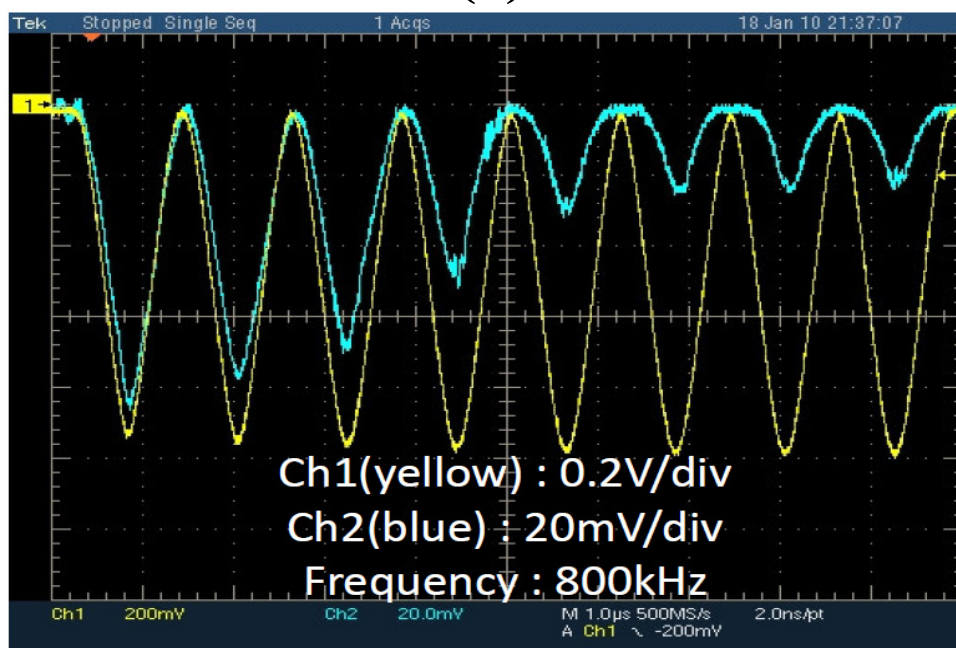


Fig. 5.1 The current output with a sinusoidal voltage input at different frequencies. The higher frequency input makes RRAM harder to switch and thus less hysteresis.



(a)



(b)

Fig. 5.2 The oscilloscope output. The unipolar sine wave forces RRAM to switch (a) simultaneously in SET process and (b) progressively in RESET process.

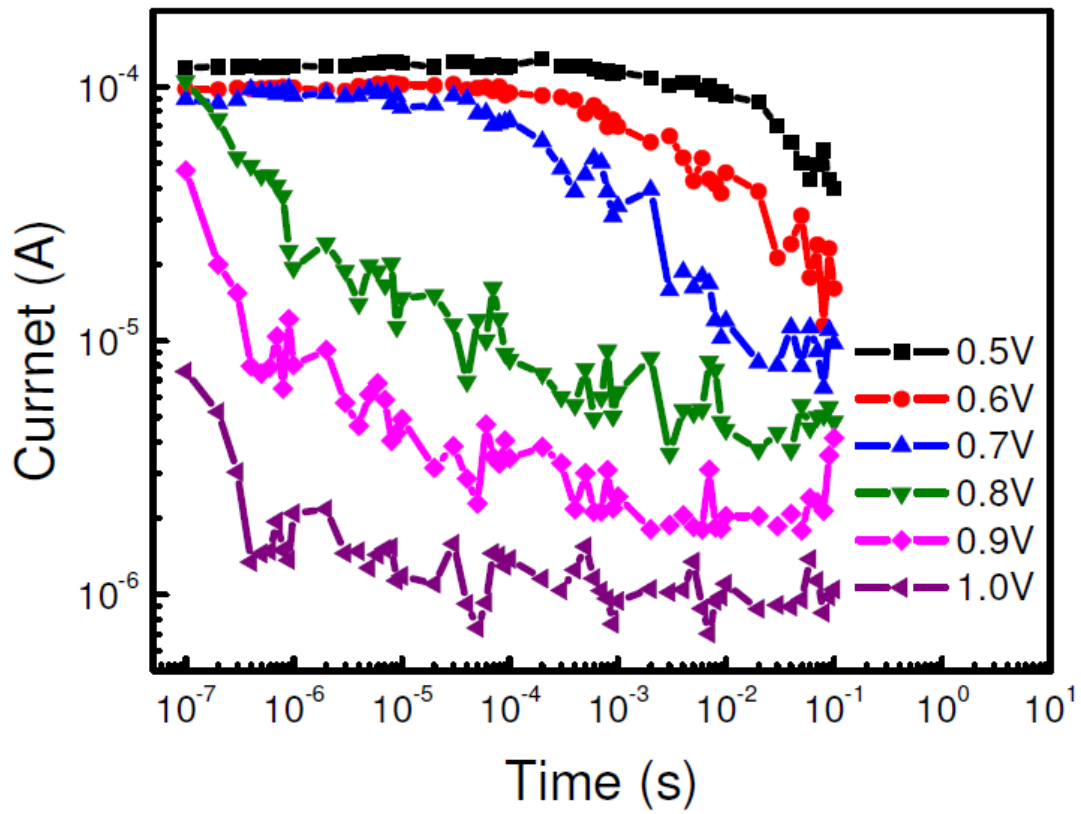


Fig. 5.3 Transient current changing with time during RESET process.

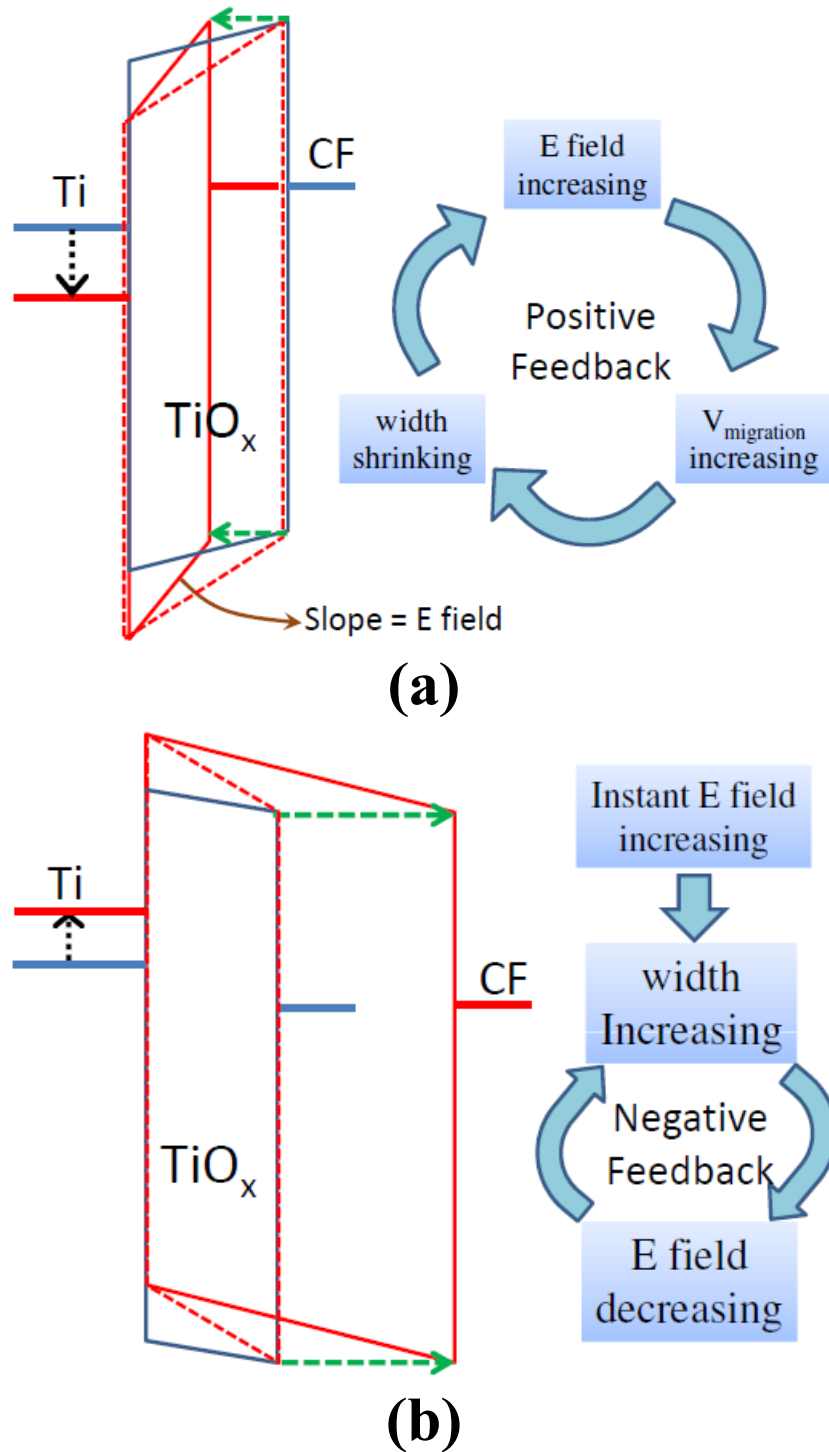


Fig. 5.4 Different switching mechanisms for (a) SET and (b) RESET processes. The blue one is the before-threshold status, the red dash one is the upon-threshold status, and the red solid one is the equilibrated status.

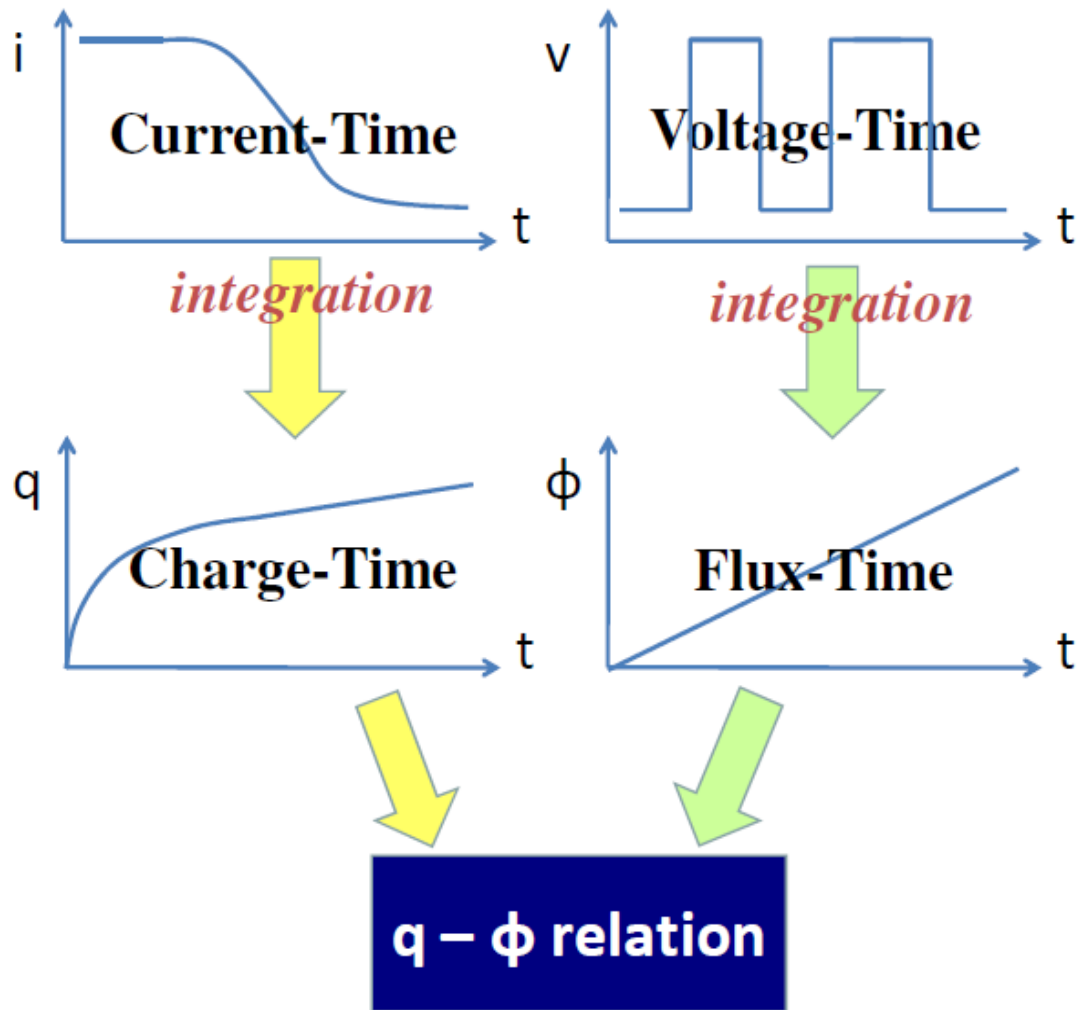


Fig. 5.5 Derivation of charge-flux relation by integration method.

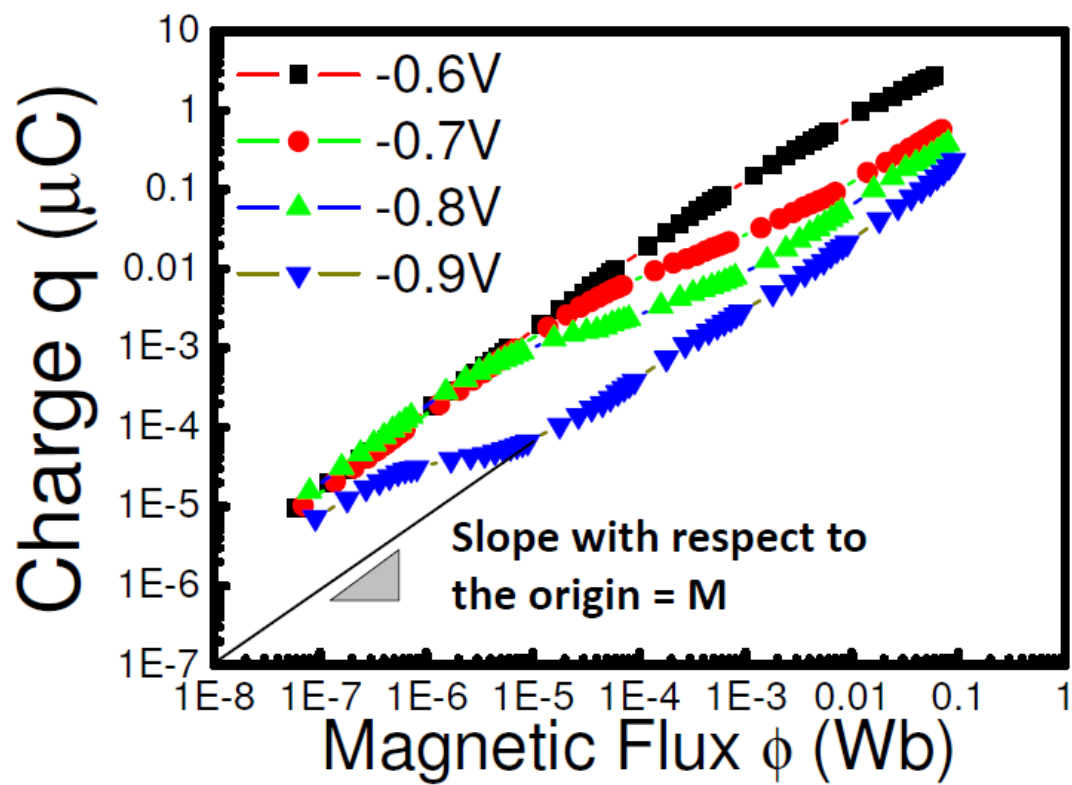



Fig. 5.6 Derived charge-flux relation for different RESET voltages. The slope to the origin for each point represents the instant meristance M .

Chapter 6

Conclusion

In this thesis, we have investigated RRAM switching behaviors and proposed a new tunneling barrier width model to fully explain all RRAM switching properties, including current characteristic before switching, temperature effect, origin of multi-level storage, and on/off ratio. By applying WKB approximation, we can perfectly fit the experimental current data with simulation results. We also derive a simple and analytical formula, which is similar to traditional direct tunneling model. The formula parameters provide a performance improvement standard for future RRAM researches.



The transient switching behavior is also important for RRAM high speed applications. We have examined RRAM transient switching behavior by sensing its barrier width variation and found their three-phase rule. Two new models are proposed to individually explain the first two phases: ion transport phase and redox reaction phase. The third saturation phase verifies our DC measurement result. These models could greatly help in improving switching speed with lower RESET voltage and power.

Finally, the RRAM memristive characteristics have been examined. We found that only RESET region is suitable for memristor application, since the SET process is an unstoppable positive feedback, and the RESET process is a self-equilibrated negative feedback. Based on experimental data, we can characterize the charge-flux relation of RRAM memristor by a simple approach, which can be applied to SPICE simulator.

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