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電子工程學系 電子研究所碩士班

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二位元分離式閘極氮化矽快閃式記憶體之漏電機制探討

The Investigation of Charge Loss Mechanism in Dual-Bit Split-Gate SONOS Flash Memory

研 究 生 ：何永涵

指導教授 ：莊紹勳 博士

中華民國 九十九 年 七 月

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研 究 生：何永涵　　Student : Yung-Hang Ho

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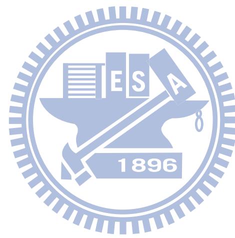
摘要

利用缺陷捕抓電荷之記憶體元件對於其尺寸之微縮是很有利的。在本篇論文中，我們提出一種二位元分離式閘極氮化矽快閃式記憶體。在最佳化之電壓操作下，利用源極注入(SSI)之寫入以及帶對帶電洞入射(BTBHH)抹除，相較於傳統式氮化矽快閃式記憶體，此種快閃式記憶體可以達成較高寫入速度、低功率消耗以及低位元間之干擾，然而保留著傳統式氮化矽快閃式記憶體之特性。

資料漏失是氮化矽快閃式記憶體最為重要之可靠度議題。水平向與垂直方向之電荷漏失機制已被提出且爭論，因為對於傳統式氮化矽快閃式記憶體，水平方向和垂直方向之電荷漏失幾乎不可能分離出來。在此論文中，我們提出了對分離式閘極氮化矽快閃式記憶體減少電荷流失的方法。藉由改變分離式閘極氮化矽快閃式記憶體之上閘極之長度或在抹除操作時之隱藏閘極施加一小電壓，水平方向和垂直方向之電荷漏失即可被分離出來。我們可以觀察到，水平方向之資料漏失是由於電子和電洞間之分佈差異所導致，且最長之上閘極元件之電荷流失是最短上閘極元件之電荷流失的兩倍。

最後，我們提出一種基底瞬時熱電洞射入之抹除方式可以完整的消除儲存的電子並且造成低電子電洞之差異分佈，而導致低橫向資料流失。因為橫向之資

料流失被抑制，此時可以觀察到資料流失與上閘極長度是無相關的並且可以防止電壓區間在10年的生存期間縮小對於二位元分離式閘極氮化矽快閃式記憶體。



The Investigation of Charge Loss Mechanism in Dual-Bit Split-Gate SONOS Flash Memory

Student：Yung-Hang Ho　　　　　　　Advisor：Dr. Steve S. Chung

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

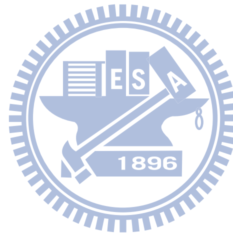
ABSTRACT

Devices based on charge trapping are a promising solution for flash memory scaling. In this study, a dual-bit split-gate SONOS flash memory has been proposed. Under the optimized bias operation, the split-gate structure device by utilizing source-side injection (SSI) programming and band-to-band hot hole injection (BTBHHI) erasing can achieve high program speed, low power consumption and low interference caused by the other bit while preserving the same performance of the conventional NROM device.

The charge loss in nitride based charge trapping memory has been a major reliability issue. The charge loss mechanisms have been published and uncertain whether the leakage path is along the lateral or vertical direction, since it is impossible to separate the two directions loss for conventional structure. In this paper, a new approach to reduce the charge loss in a split-gate SONOS memory has been proposed. By altering the word-gate length of the split-gate structure SONOS or by applying a small bias at the control-gate under erasing, the electron or hole distribution can be

varied, and the lateral and vertical retention loss can be split off. It was observed that the lateral retention loss is caused by the misalignment between the distribution of electron and hole. The retention loss of the longest word-gate device is about two times larger than the shortest device ones caused by lateral retention loss.

Finally, substrate transient hot hole (STHH) injection erasing scheme has been demonstrated to fully eliminate the electrons throughout the entire channel and achieve low electron and hole misalignment, inducing low lateral data retention loss. Since the lateral retention loss has been suppressed, the retention loss is independent of the word-gate length with time and avoids window closure for the 10-year lifetime after the program/erase cycling in split-gate structure SONOS cells.



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Chapter 1

Introduction

1.1 The Motivation of This Work

Flash memories today are still mostly based on the storage of charges in the poly-silicon floating-gate (FG) of a MOS transistor. Since the storage medium is conductive, the device is subject to stress induced leakage current (SILC) because of traps accumulated in the bottom oxide during cycling. Thus, the scaling of bottom oxide below 8 nm is almost prohibited because of important charge loss after the cycling [1].

An alternative solution is to replace the floating-gate storage element by a non-conductive one, such as a nitride trapping layer [2]. This indeed makes the device much robust toward SILC, which explains the renewed interest for SONOS type flash memories. Nitride read only memory (NROM) cell is one of the most mature nitride based cells technologies [3]. This device is locally programmed by a channel hot electron injection (CHEI) and erased by a band-to-band tunneling hot-hole injection (BBTHHI), which allows the storage of two physically separated bits close to each junction and to use a thicker bottom oxide.

However, NROM device has following inherent disadvantages: (1) The channel length scaling is limited because the lateral distributions of the charges have to be well separated to avoid any interference between the bit and the punch-through effect by sufficient drain voltage larger than 3.2V. (2) High power consumption associated

with CHEI and write disturbance due to the high drain voltage, and (3) The retention is strongly degraded after cycling. The repeated programming of each bit relies on a delicate overlap of the injected electrons and holes distributions, which is degraded as program/erase cycling proceeds. This can be followed by a drift and recombination of remaining charges after cycling. Besides, hot holes can be easily trapped in the bottom oxide during the erase operation, creating a path for vertical charge loss [4].

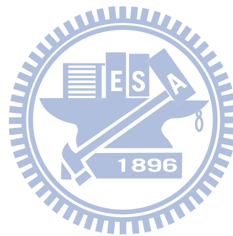
Here, the dual-bit split-gate SONOS is presented in this paper solves most NROM drawbacks while preserving the same performance, at the expense of a slightly more complicated processing. This structure allows separating both bit locations by a nitride layer, and prevents the charges from merging. The two bits are also addressed by separate gates, which remove the second bit effect. Furthermore, source-side injection can be used for programming. This mechanism is more efficient than CHEI, reducing the power consumption [4-6].

In this thesis, the characteristics and mechanisms of split gate SONOS will be discussed. Next, the retention loss mechanism will be investigated by using the split gate SONOS with different gate length. Then, an erase scheme called Substrate Transient Hot Hole Injection (STHHI) will be demonstrate to achieve low retention loss by suppressing the lateral retention loss [7-8]. Finally, we will draw a conclusion of this thesis.

1.2 Organization of the Thesis

The organization of this thesis consists of six chapters. After a brief introduction in Chapter 1, we will introduce the experimental devices and experimental setup in

Chapter 2, which includes the operating schemes, the program and erase schemes and the measuring method for charge pumping. In chapter 3, we will show the physical mechanism and the basic characteristics of the dual-bit split-gate SONOS. In Chapter 4, we will discuss the misalignment and retention loss model for conventional SONOS. In Chapter 5, we discuss the retention mechanism for split-gate SONOS by altering the word-gate length of the devices and demonstrate an erasing scheme for split-gate SONOS to achieve low retention loss. Finally, the conclusions will be presented in chapter 6.



Chapter 2
Device fabrication and Equipment Setup

2.1 Introduction

This chapter is divided into four sections. First of all, both split-gate SONOS and the conventional SONOS cells used in this study will be described. Second, the instruments setup and the experimental techniques to accurately control these instruments are illustrated. Third, we will discuss the programming and erasing schemes of these cells. Finally, charge pumping measurement technique setup used in this study will be demonstrated.

2.2 Device Fabrication

Figure 2.1 is the schematic diagram illustrating of forming the split-gate SONOS. As shown in Fig. 2.1(a), a substrate is provided, and a P well is formed in the substrate. Then, a plurality of control gate structure is formed on the P well. Each control-gate structure from bottom to top includes a gate insulating layer, a control gate oxide (65Å), and a cap nitride layer. As shown in Fig. 2.1(b), a silicon oxide layer (not shown), a nitride layer (not shown) is deposited on the substrate and control gate structure, and an etching back process is then performed to form a plurality of sacrificial spacers alongside each control gate structure. Meanwhile, a plurality of opening is formed between any two adjacent sacrificial spacers to expose the P well. Afterward, an implantation process is performed via each opening to form a plurality of N doped regions, serving as buried bit line, in the P well. As shown in Fig. 2.1(c), the sacrificial spacers alongside each control gate structure are removed. Then, a

composite dielectric layer is formed on the P well, the control-gate structure, and the N doped regions. In this embodiment, the composite dielectric layer is an ONO tri-layer dielectric including a bottom oxide layer (60Å), a nitride layer (90Å), and a top oxide layer (90Å). As shown in Fig. 2.1(d), a conductive layer is entirely deposited on the composite dielectric layer, and a photolithography and etching process is performed to define a plurality of parallel word line, which are perpendicular to the control-gate structure, as shown in Fig. 2.1(e) [9]. The SEM image and the 2D-TCAD simulation structure of dual-bit split-gate SONOS are shown in Fig. 2.2 (a) and Fig. 2.2 (b). The gate width is 0.2um, and the channel length is 0.18um under control-gate and three different word-length(L_{WG}) splits (0.13um, 0.12um, 0.10um) under word-gate.

The conventional SONOS device used in this study is first grown by thermal oxidation with thicknesses of 50 Å. Next, a layer of 60 Å LPCVD nitride film is grown. Finally, the LPCVD blocking oxide is grown with thickness of 50 Å. (W/L=0.7/0.26 um)

2.3 Equipment Setup

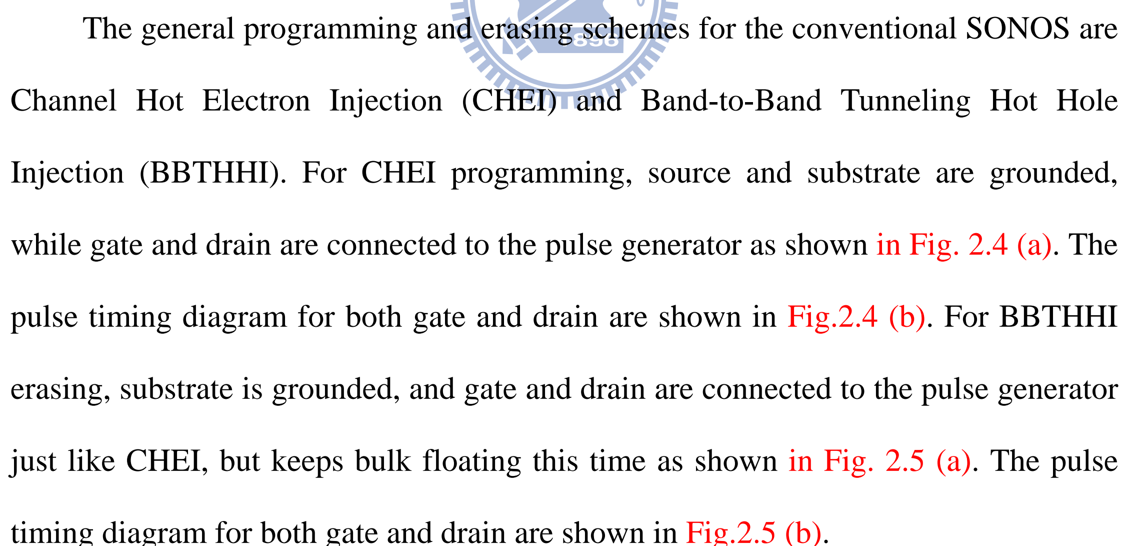
The experimental setup for the I-V and transient characteristics measurement of SONOS is illustrated in Fig. 2.3. Based on the PC controlled instrument environment via HP-IB (GP-IB, IEEE-488 Standard) interface, the complicated and long-term characterization procedures during analyzing the intrinsic and degradation behaviors in SONOS cells can be easily achieved. As shown in Fig. 2.2, the characterization apparatus with semiconductor parameter analyzer (HP 4156C), dual channels pulse generator (HP 8110A), low leakage switch mainframe (HP E5250A), and a probe

station provides an adequate capability for measuring the device I-V characteristics and executing the SONOS cell program/erase operation.

Source-monitor units (SMU) and provided the high current resolution to 10^{-15}A range facilitates the gate current measurement, sub-threshold characteristics extraction, and the saturation drain current measurement. The HP E5250A equipped with a 10-input (6 SMU ports and 4 AUX ports) × 12-output switching matrix, switches the signals from the HP 4156C and the HP 8110A to device under test (DUT) in probe station, automatically. In addition, the HT-Basic are used as the program languages to achieve the personal computer (PC) control of these measurement instruments.

2.4 Programming and Erasing Setup

The general programming and erasing schemes for the conventional SONOS are Channel Hot Electron Injection (CHEI) and Band-to-Band Tunneling Hot Hole Injection (BBTHHI). For CHEI programming, source and substrate are grounded, while gate and drain are connected to the pulse generator as shown in Fig. 2.4 (a). The pulse timing diagram for both gate and drain are shown in Fig.2.4 (b). For BBTHHI erasing, substrate is grounded, and gate and drain are connected to the pulse generator just like CHEI, but keeps bulk floating this time as shown in Fig. 2.5 (a). The pulse timing diagram for both gate and drain are shown in Fig.2.5 (b).



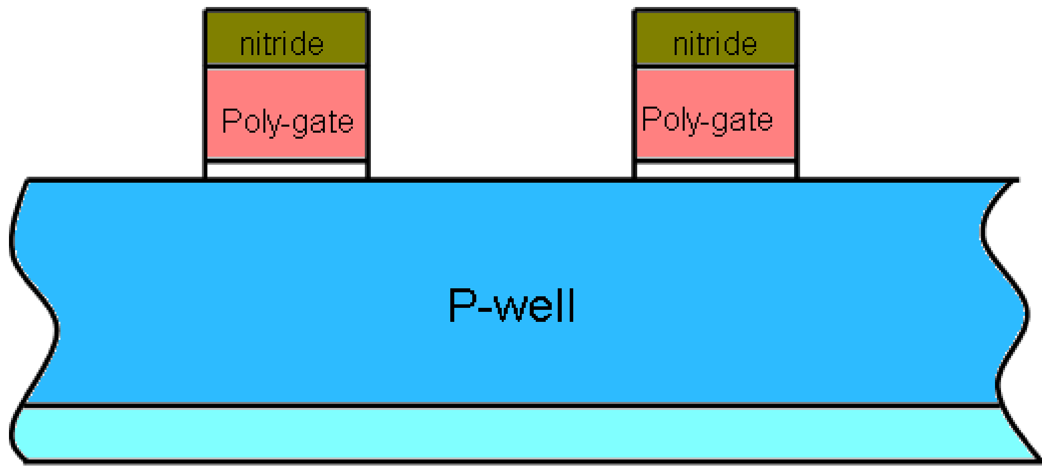
Another erase scheme called Substrate Transient Hot Hole Injection (STHHI) is also used in this study. For STHHI, source and drain keep floating and gate is grounded, while only substrate is connected to the pulse generator as shown in Fig. 2.6 (a). The pulse timing diagram for both gate and drain are shown in Fig.2.6 (b).

The operation mechanism and relevant measurement of STHHI will be discussed after this chapter.

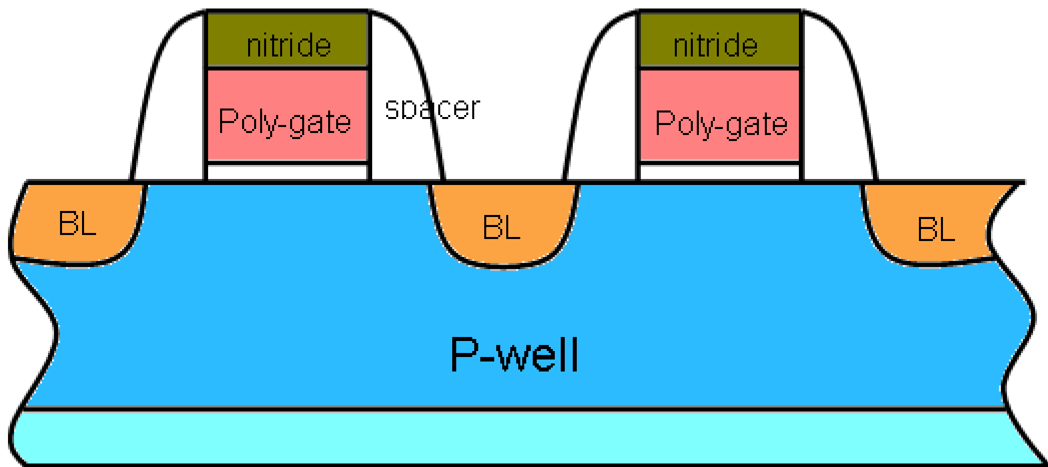
Dual-bit split-gate SONOS operates as conventional does, but adding a control-gate bias in the middle of the cell. The control-gate keeps a small constant bias for programming, while floating for erasing. And the other terminals are just the same as conventional operation.

2.5 Charge Pumping Measurement Technique Setup

The charge pumping measurement technique setup is shown in Fig. 2.6, which we called fixed based charge pumping, but with some method unlikely the traditional one. The pulse generator is connected to the gate, and with the substrate and drain connecting to the HP4156C, while source is kept floating. Fig. 2.7 (a) shows the pulse series type sending out from the pulse generator used by this setup. By using this setup, we can measure the charge pumping current from drain. If one wants to measure the charge pumping from drain (/source), we should connect the HP4156C with them and open the source (/drain) to get the information of the charge pumping current. The second scheme for charge pumping measurement technique setup is shown in Fig. 2.7 once again. However, the pulse series type is different this time. As shown in Fig. 2.7 (b), we used likely the traditional fixed top charge pumping pulse series to do our measurement.



(a)



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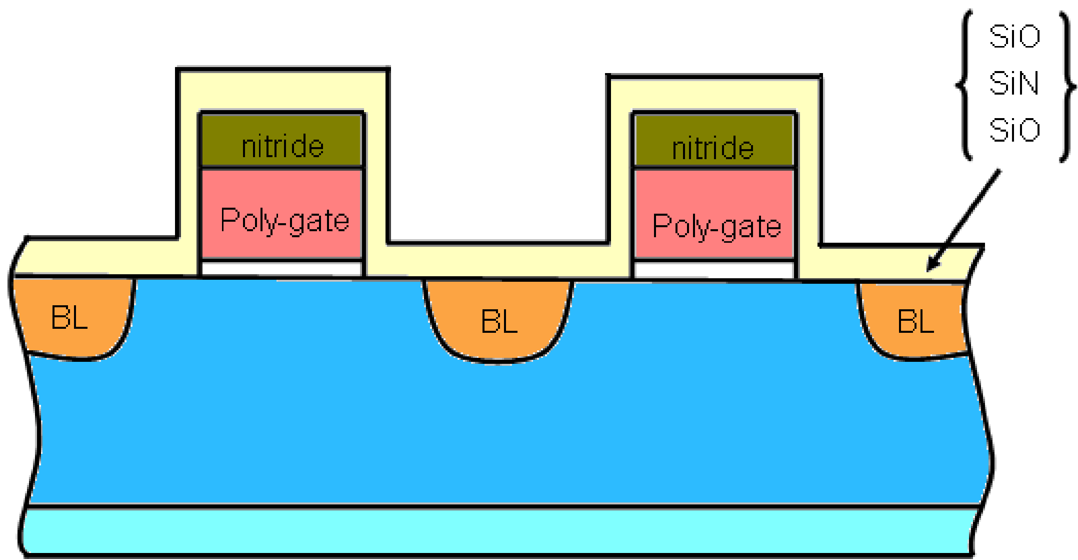
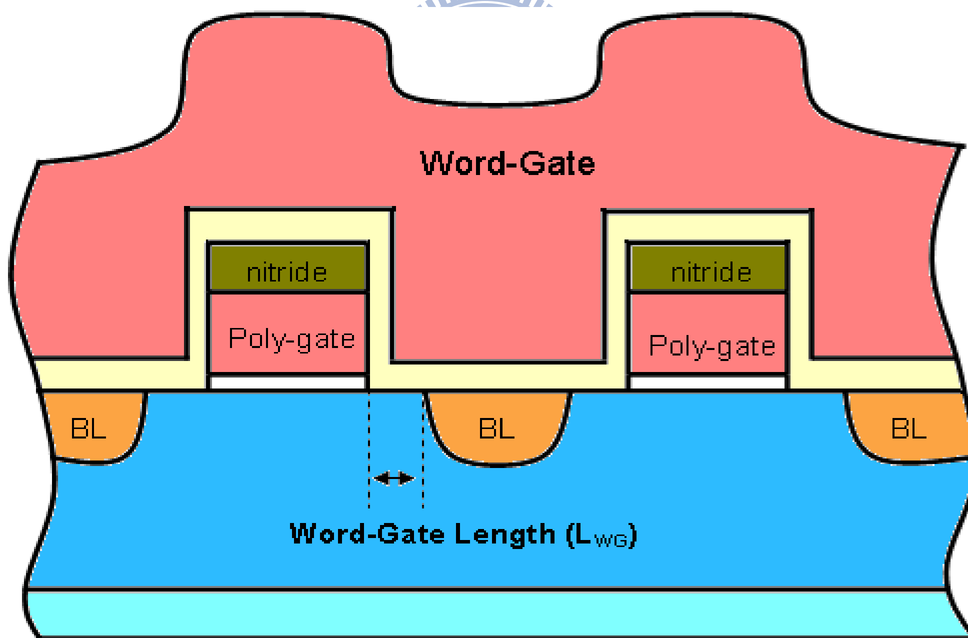


(a)



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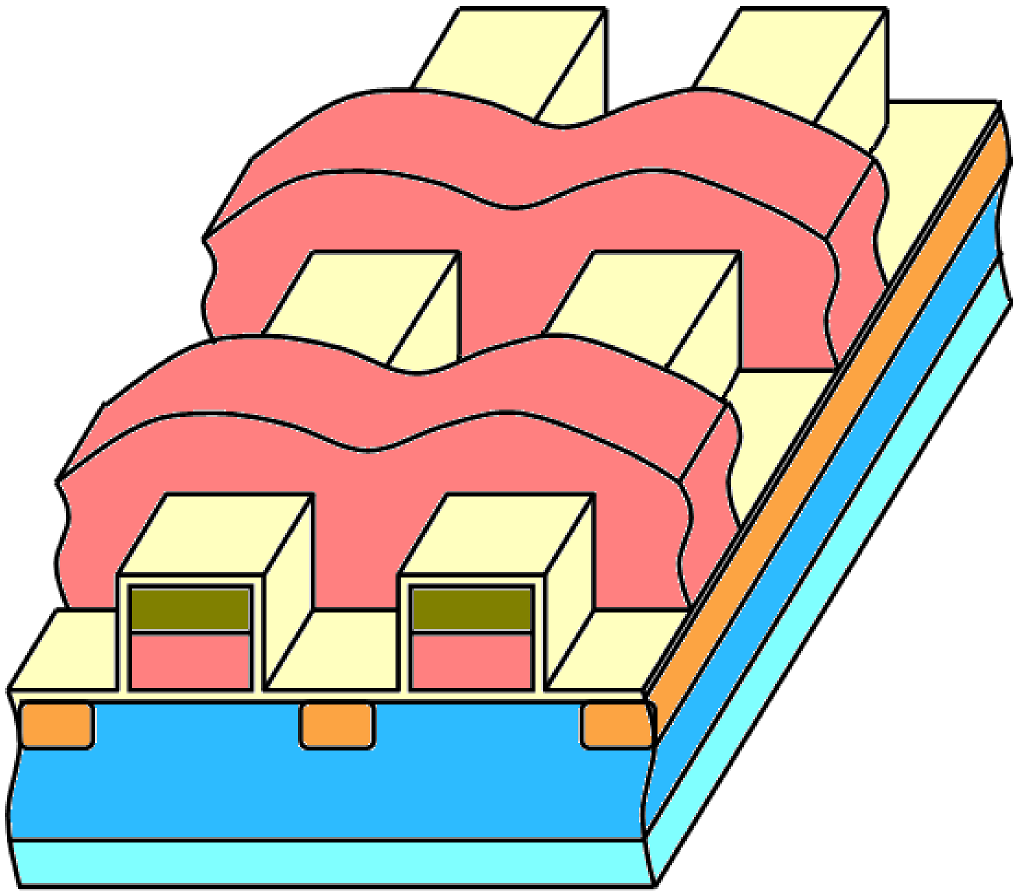
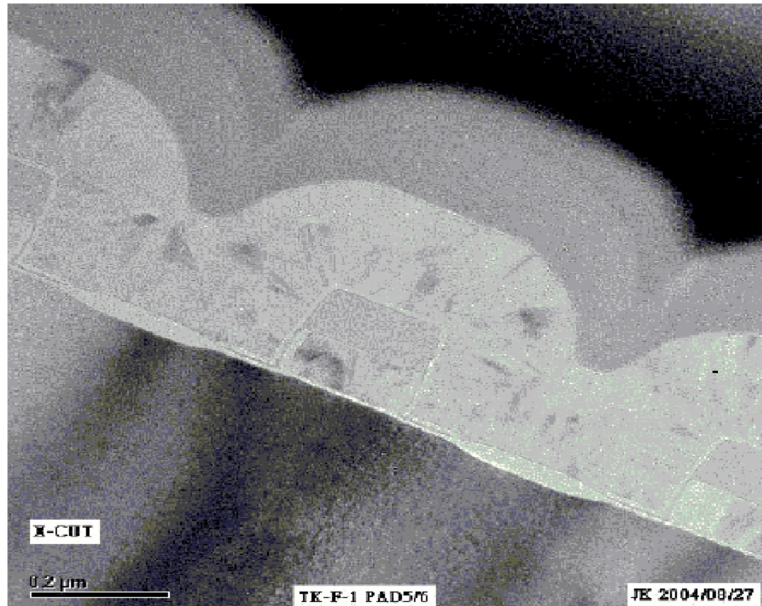
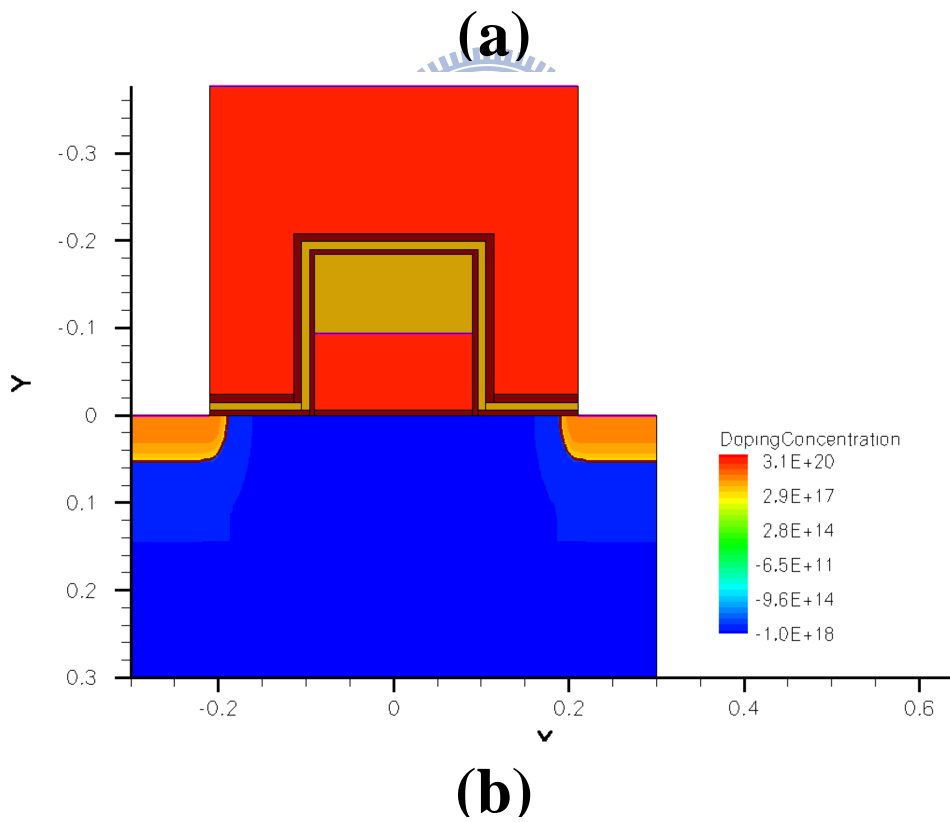


(e)

Fig. 2.1 The schematic diagram illustrating of forming the dual-bit split-gate SONOS.



(a)



(b)

Fig. 2.2 The SEM image (a) and the simulation structure (b) of the dual-bit split-gate SONOS.

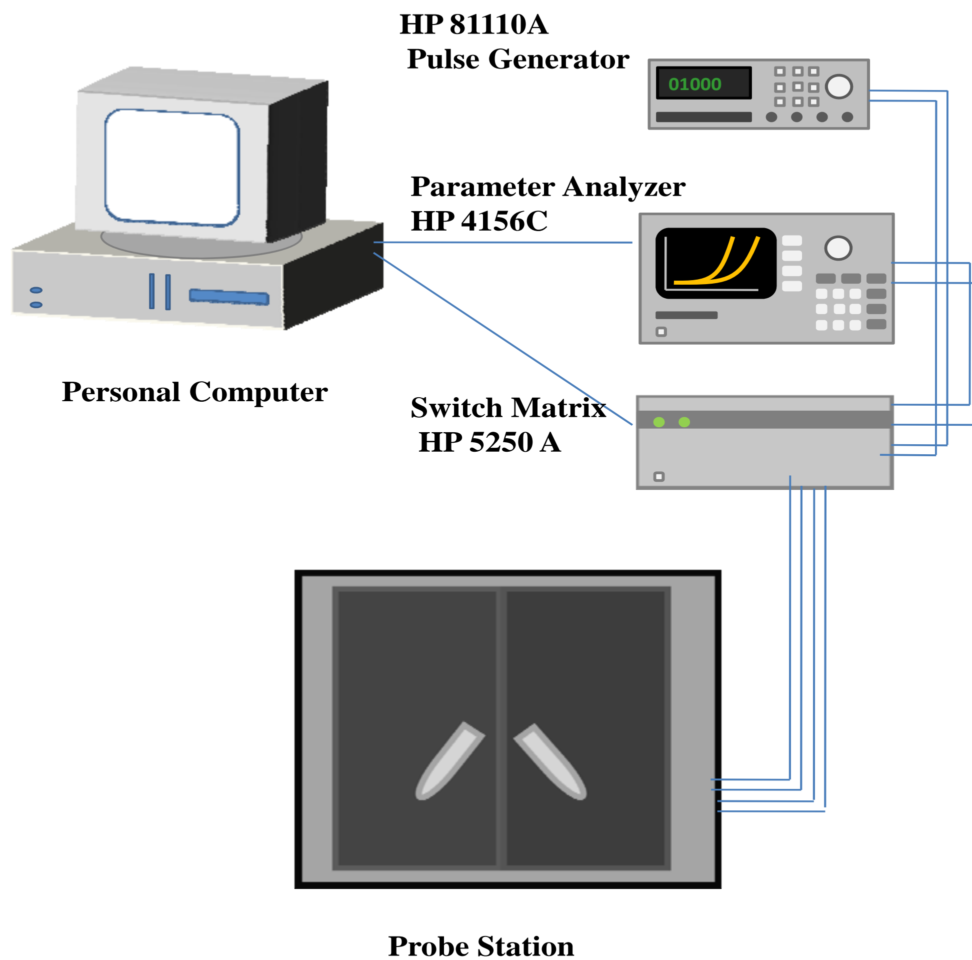
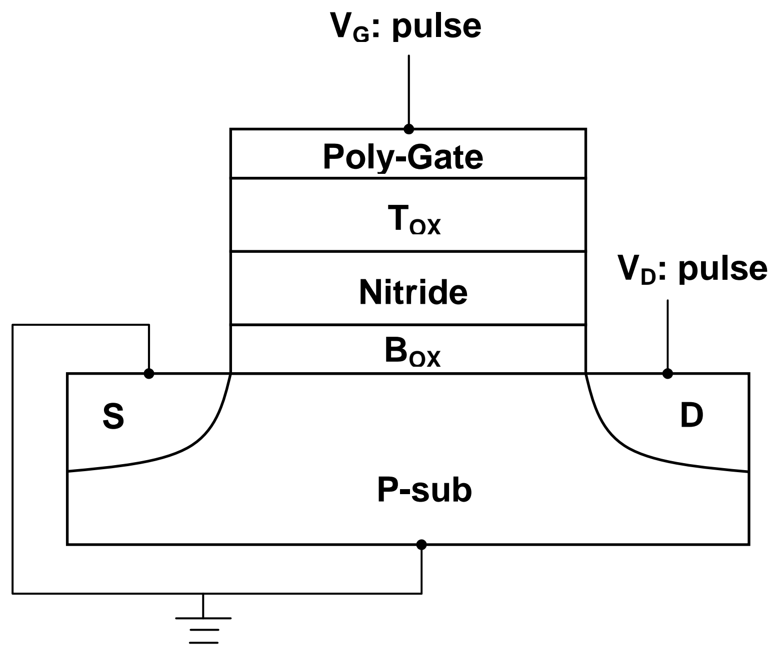
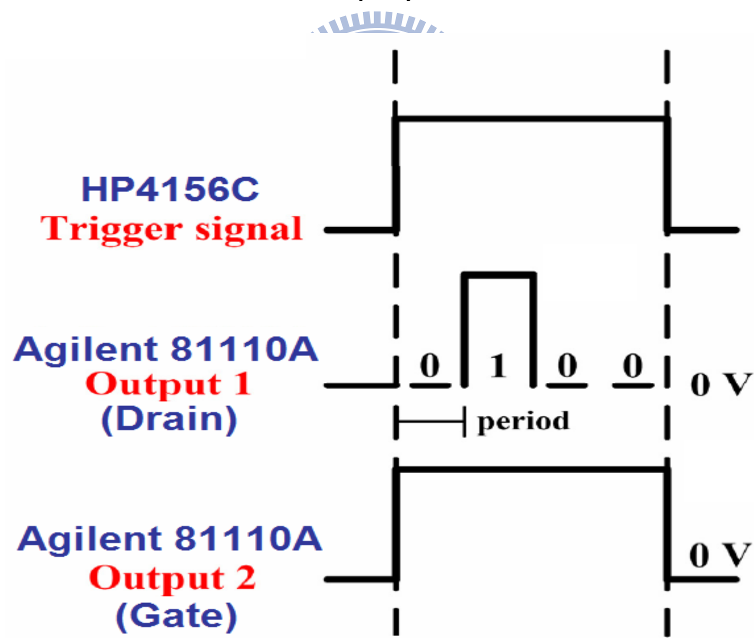


Fig. 2.3 The experimental setup of the current-voltage and the transient characteristics measurement. An automatic controlled characterization system is setup based on the PC controlled instrument environment.

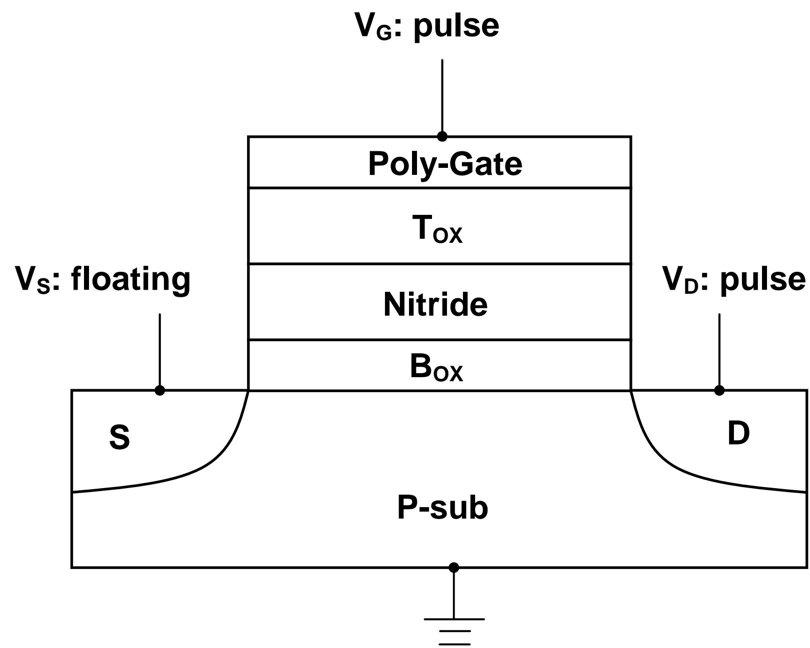


(a)



(b)

Fig. 2.4 The operation scheme (a) and time diagram (b) for CHEI programming.



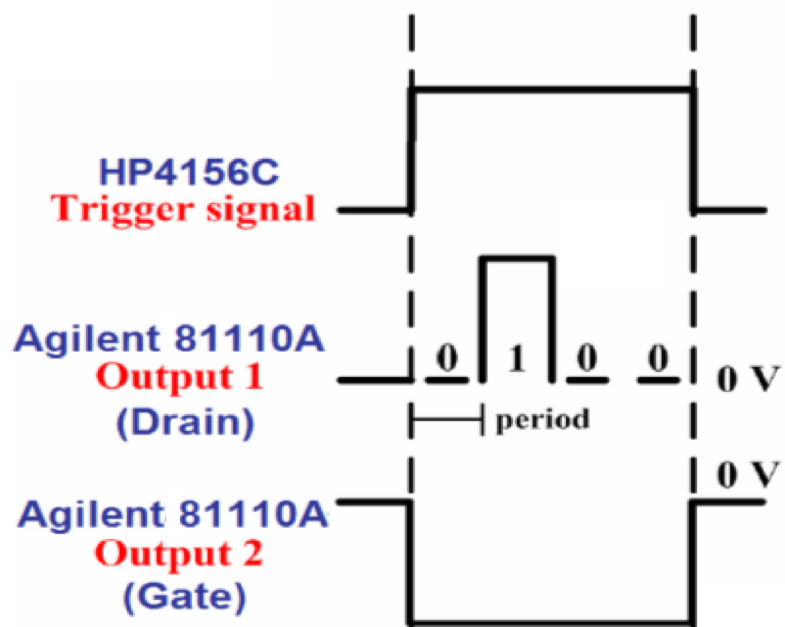
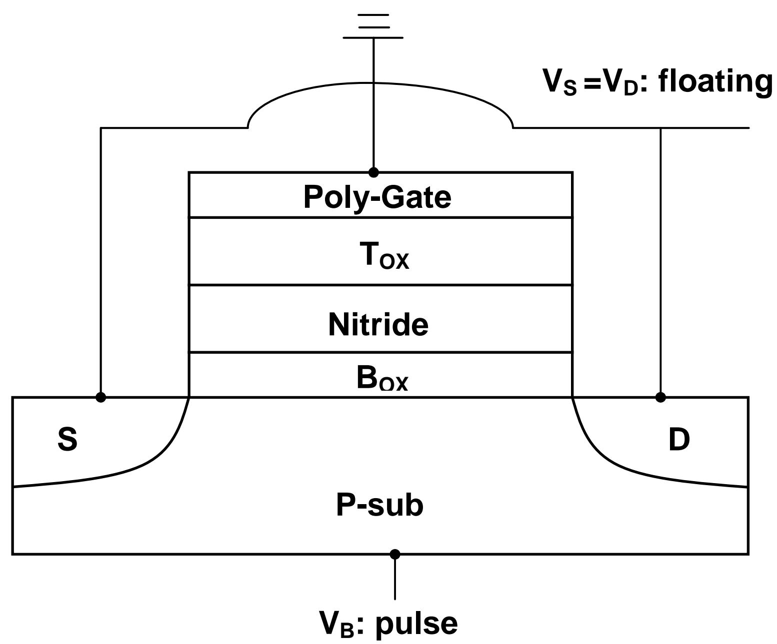
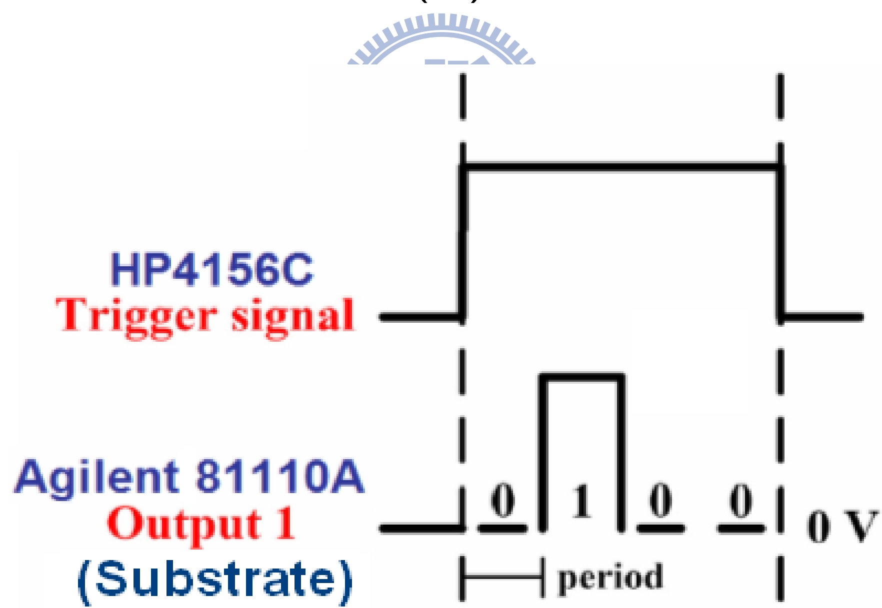


Fig. 2.5 The operation scheme (a) and time diagram (b) for BBTHHI erasing.

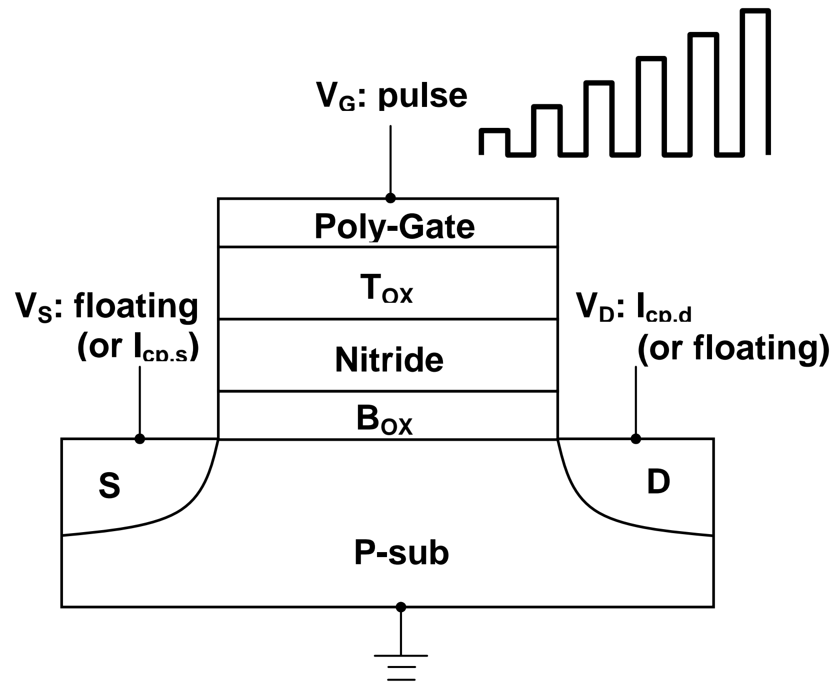


(a)

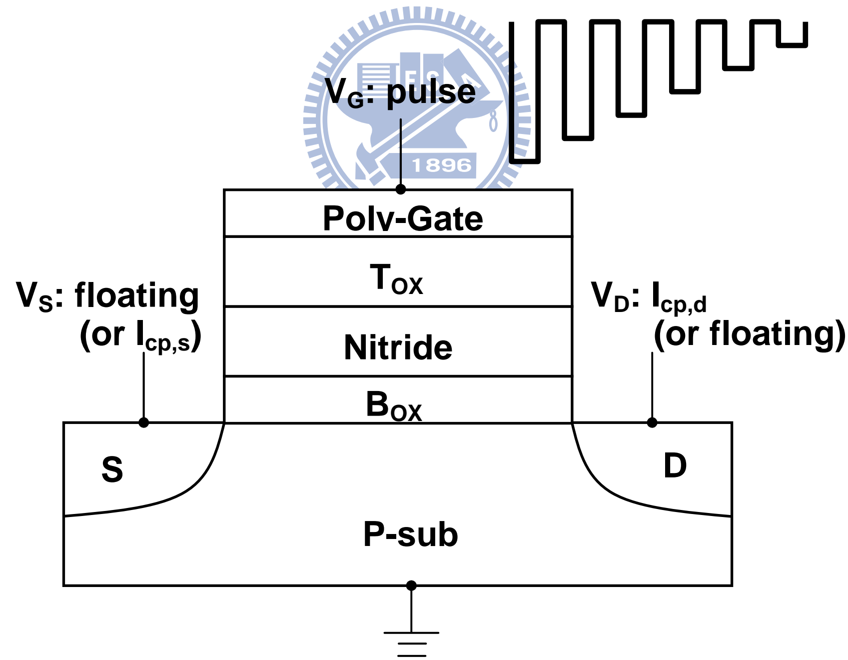


(b)

Fig. 2.6 The operation scheme (a) and time diagram (b) for STHHI erasing.



(a)



(b)

Fig. 2.7 The operation scheme for charge pumping with fixed base pulse series sketch (a) and fixed top sketch (b).

Chapter 3

Basic Characteristics of Dual-Bit Split-Gate SONOS

3.1 Introduction

In this chapter, first, we will introduce the basic physical mechanism of split-gate SONOS and find the optimized bias condition for both programming and erasing. Then, some reliability issues for non-cycled cell, such as gate disturbance, drain disturbance, second bit effect, and one shot retention will be discussed in this chapter.

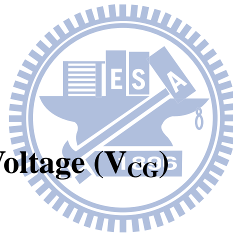
3.2 Basic Mechanism and Optimized Bias Condition of Split-Gate SONOS

3.2.1 Source Side Injection Programming

Channel hot electron injection has been widely used as a programming mechanism in flash memory. Based on Lucky-Electron model, the programming efficiency of flash memory is evaluated with the gate current or the substrate current as the figure of merit. Source side injection has a higher programming efficiency than drain-side programming by using-split gate structure to achieve high CHE generation and optimal electron collection at the same time. As shown in Fig. 3.1, under the programming condition, the word-gate is biased at a higher potential than the drain. The inversion layer formed in the word-gate channel acts like a virtual drain. A large channel potential drop formed at the gap between control-gate and word-gate such

that the channel electrons are accelerated in this gap region and become hot enough to inject into the ONO layer underneath the word-gate as shown in Fig. 3.2 [5, 10-11].

The drain current as a function of the control-gate voltage (V_{CG}) for the word-gate voltage (V_{WG}) of 10V is shown in Fig. 3.3. The parameter was the drain voltage (V_D) varied from 0.5V to 2V. This bias condition makes the channel resistance beneath the word-gate negligible small. Thus, the programming current was limited by the control-gate and is could be estimated to be 0.3uA in Fig. 3.3. Fig. 3.4 compares the drain current versus drain voltage curve between split-gate SONOS and conventional SONOS. It was found that the drain current for split-gate SONOS by using SSI is about 100~1000 times lower than conventional SONOS by using CHEI [4-5].



3.2.2 Optimized Control-Gate Voltage (V_{CG})

Figure 3.5 shows the simulated and measured result with different control-gate bias under programming. It shows the property bell-shape with respect to the V_{CG}. In split-gate SONOS memory device, the control-gate can limit the programming current, as mentioned above. This programming characteristic indicates that the control-gate can dominate not only the programming current but also the programming properties. When a large voltage than the threshold voltage against the channel beneath the control-gate is applied to the control-gate, the potential beneath the control gate is dropped down due to the effect of the drain voltage. This potential drop induces a fall in the lateral electric field, which is a derivative of the potential, in the gap between control-gate and word-gate. This cause only a small shift in the threshold voltage brought on the electron injection, even though a large drain current flows in the

channel. However, when a smaller voltage then threshold voltage of the control-gate is applied to the control-gate, the drain voltage does not induce a potential drop beneath the control-gate. This indicates that the drain voltage does not induce the drop of the lateral electric field in the gap. Instead the electric field formed at the gap is high enough to inject electron, however, the control-gate shuts off the programming current. Thus, electron can not be injected, even though a high electric field is formed at the gap. Therefore, to achieve high efficiency programming operation, both the programming current and the electric field must be obtained by applying the bias condition appropriately [5-6, 10].

3.2.3 Optimized Drain Voltage (V_D)

Figure 3.6 shows the simulated and measured result with different drain bias under programming. The shift in the threshold voltage was saturated against increases in the drain voltage. In the simulation result, drain voltage of over 3V does not affect the electric field at the gap except for increases the electric field at the junction. Therefore, it is no use by adding a too large voltage at junction but a proper voltage can achieve the same efficient as large drain voltage does [5-6].

3.2.4 Programming, Erasing Transient and Readout

Figure 3.7 shows the programming (V_{WG}= 9V, 10V, 11V V_D= 4V V_{CG}= 0.9V V_S= V_B= 0V) and erasing (V_{WG}= -5V V_D= 6V V_{CG}= V_B= 0V) transient for multi-level cell application with each threshold voltage step of 1V. Fig. 3.8 shows the drain current versus gate voltage for the spit-gate SONOS at initial state and three different programmed states. Fig. 3.9 shows also the drain current versus gate voltage but under

different read bias conditions. It was found that, if the read voltage is not large enough (o.1V), there is no threshold voltage difference between forward read and reverse read, since the program charge can not be completely depleted or the surface potential can not be pull down. Therefore, a large reverse read voltage (1.8V) is needed for readout for this type of memory cell to suppress the potential barrier, causing a local DIBL effect that screen out the potential barrier [4-5, 12-13]. The suggestion of programming, erasing and readout bias condition is shown in table 1.1.

3.3 Reliability for Non-Cycled Split-Gate SONOS

3.3.1 Second bit Effect

Figure 3.10 shows the second bit effect of the dual-bit split-gate SONOS. It was found that the left and right bit will not interfere with the other bit, since the two storage bit position is already separated by the control-gate. And the readout voltage of 1.8V is large enough to screen out the potential barrier [13].

3.3.2 Gate and Drain Disturbance

Fig. 3.11 and Fig. 3.12 show the gate and drain disturbance of the split-gate SONOS respectively. During programming and erasing, the selected row (column) applies to a word-gate (drain) voltage. Therefore, non-selected cell will suffer from gate (drain) disturbance as shown in Fig. 3.11 (a) and Fig. 3.12 (a). Fig. 3.11 (b) and Fig. 12 (b) show that it needs a large enough word-gate voltage and long enough stress time to make disturbance. It is impossible for non-selected cell to suffer from gate or drain disturbance during programming and erasing operation [5].

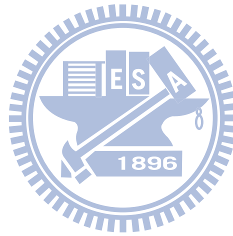
3.3.3 Another Erasing Method (Positive BBTHHI Erase)

There is another erase method like drain disturbance for split-gate SONOS. However, the erase speed for drain disturbance in Fig. 12 is too slow. Fig. 13 shows the contour plots of the potential distribution around the gap between the gates at the drain voltage of 6V. The voltage of the control-gate was small (0.9V) in Fig13 (a) and large (6V) in Fig13 (b). The potential for holes beneath the region where the electrons were trapped was lower than that around the region. It means that most of holes generated at the drain flow toward not only the substrate but also the electron trapped region. By comparing with Fig13 (a) and Fig13 (b), the potential induced by the voltage applied to the control-gate tend to spread beneath the gap by applying the higher voltage of the control-gate. This spread potential makes a path where hot holes generated at the drain region moving toward the substrate narrower than the path without the bias to the control-gate. This introduces more hot holes move toward the region where electrons are trapped than toward the substrate. Therefore, the larger positive voltage is applied to the control-gate, the more effectively the erasing operation using hot holes can be achieved without a negative bias [5].

Figure 14 shows the positive bias erasing transient with different positive bias applying to the control gate. For small positive control-gate bias (3V), most of the holes are flowing to the substrate. While large positive control-gate bias (6V), the holes are flowing into the nitride layer to achieve more efficient erase operation. However, large control-gate bias positive BBHH erase still need more time to complete the erasing operation than general negative BBHH erase. The reason will be explained in chapter 5.

3.3.4 Retention Loss

Figure 15 shows the retention loss at program state for fresh and cycled cell. It was found that there is no loss for fresh cell but not for cycled cell. It is because after cycling, the bottom oxide is heavily damaged and a large amount of holes accumulate near junction causing both vertical and lateral retention loss, which will be discussed in the following chapters in detail.



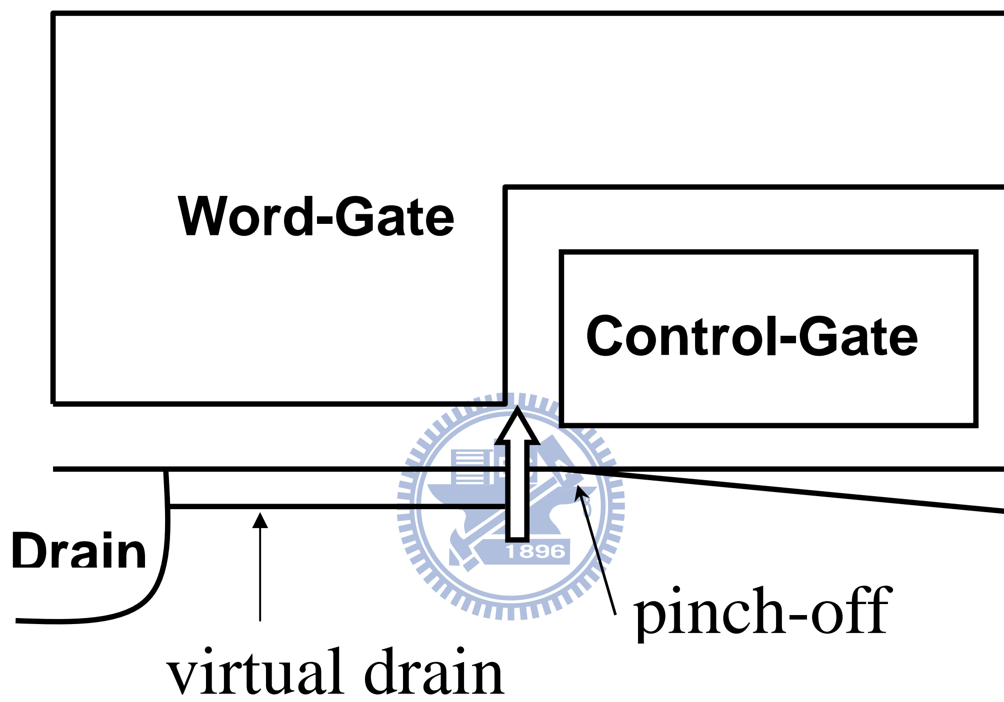
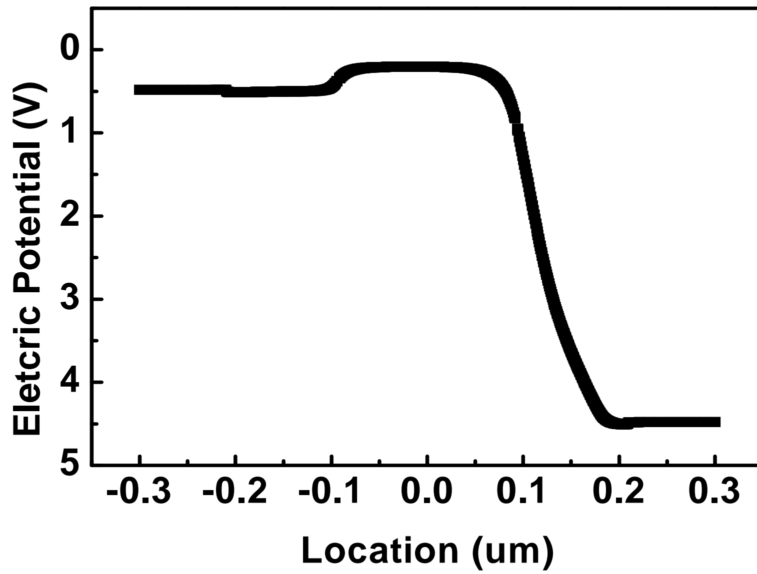
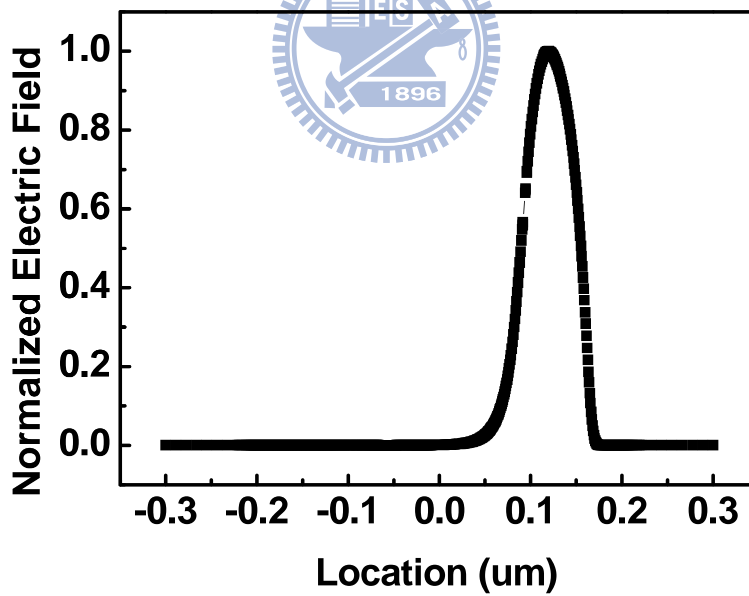


Fig. 3.1 Schematic illustration of source-side injection for split-gate structure SONOS flash memory.



(a)



(b)

Fig. 3.2 The electric potential (a) and the normalized electric temperature (b) for split-gate SONOS during programming.

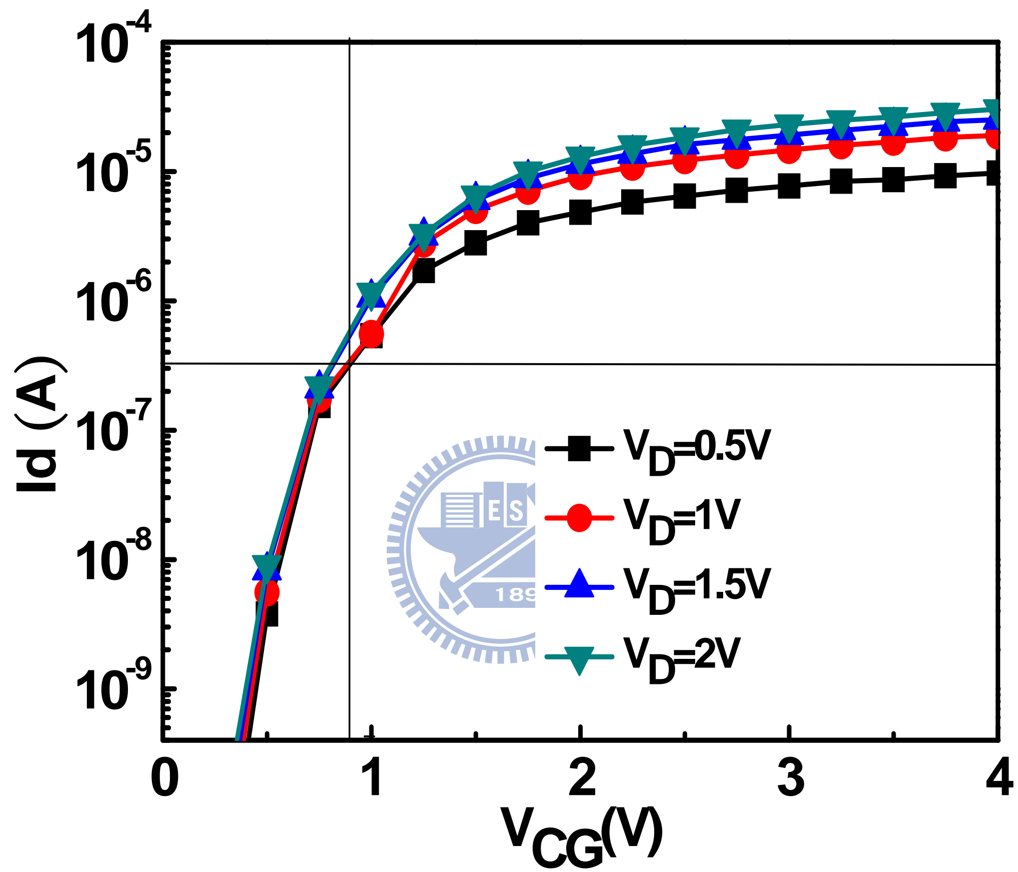


Fig. 3.3 The drain current versus control-gate voltage with various drain voltage.

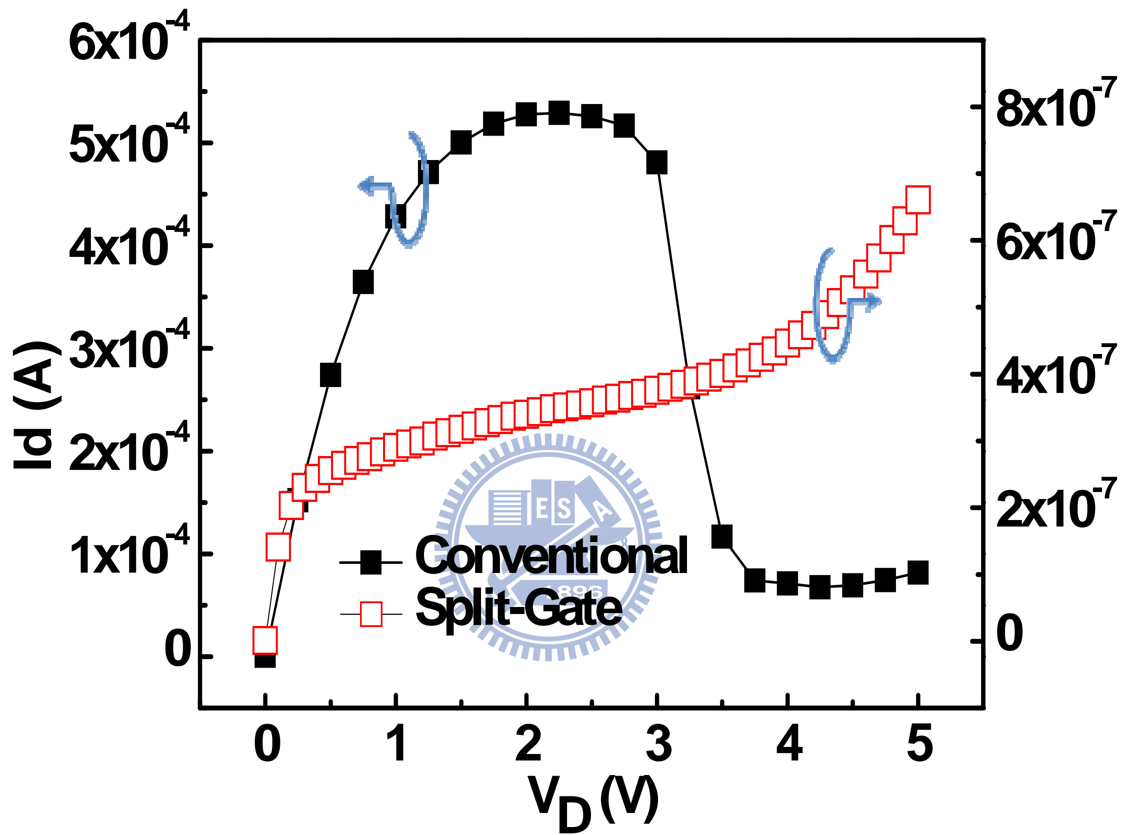
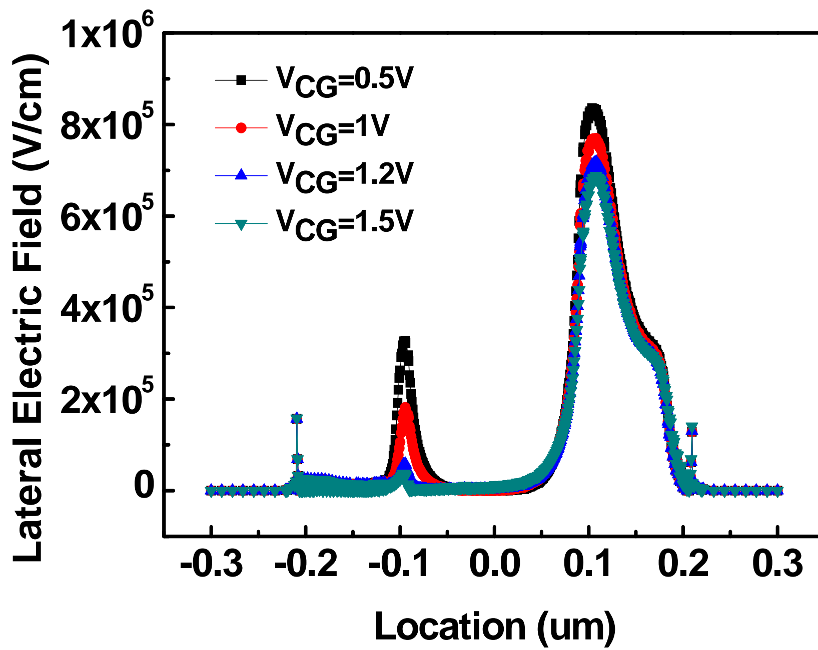
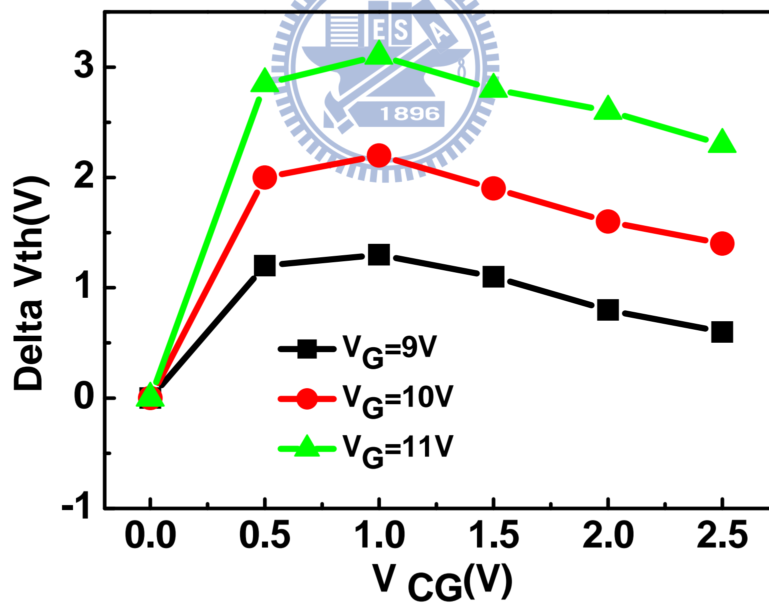


Fig. 3.4 The drain current versus drain voltage of conventional SONOS (red) and split-gate SONOS (black).

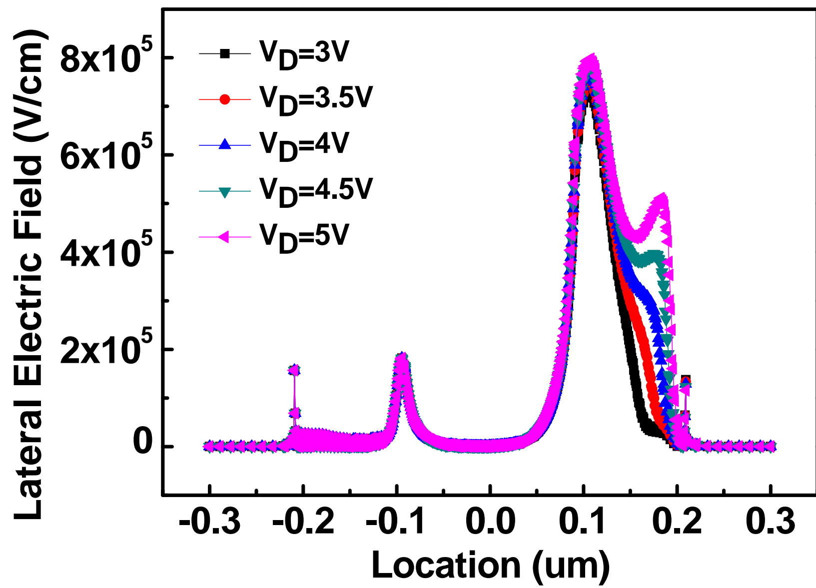


(a)

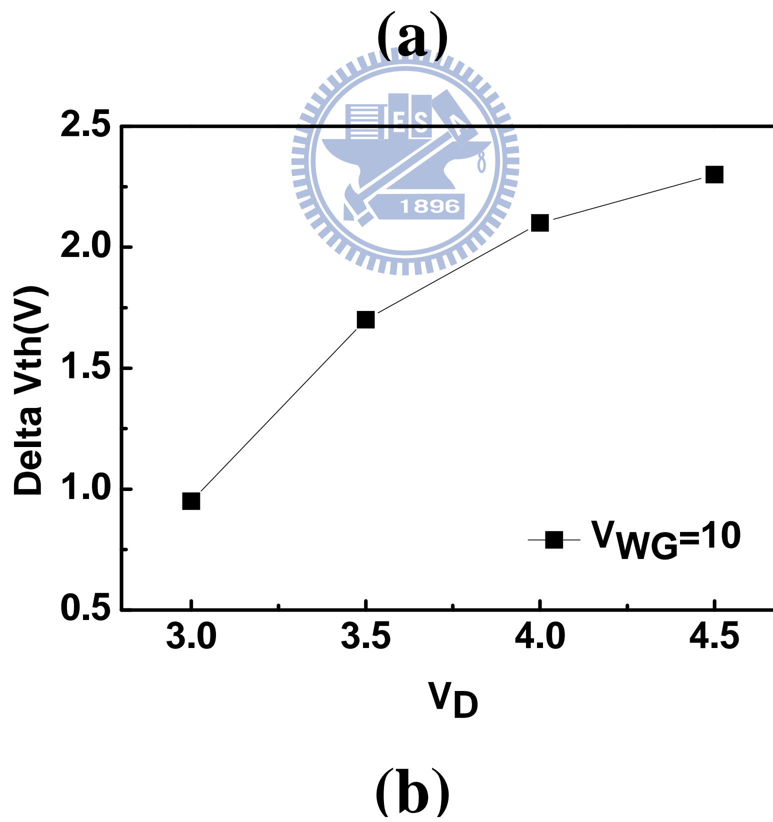


(b)

Fig. 3.5 Simulated lateral electric field versus lateral position under (a) different control-gate voltage and (b) measured programming window versus control-gate voltage.



(a)



(b)

Fig. 3.6 Simulated lateral electric field versus lateral position under (a) different drain voltage and (b) measured programming window versus drain voltage.

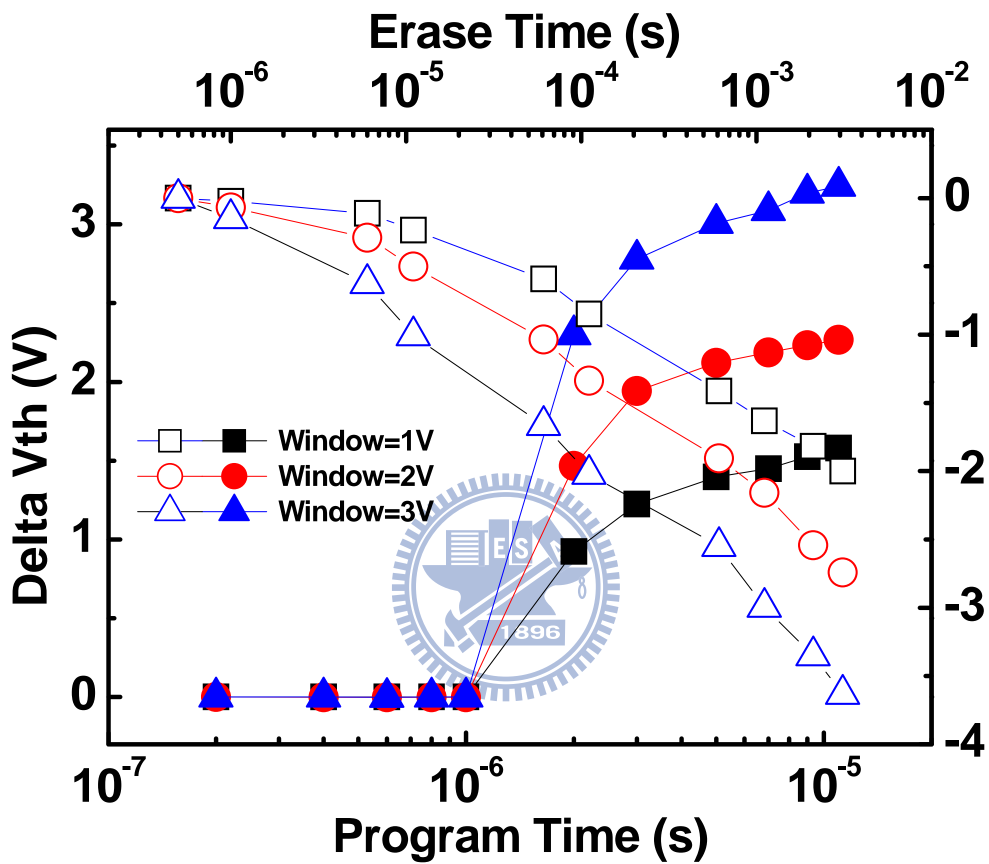


Fig. 3.7 The programming and erasing transient for split-gate SONOS with multi-level cell application.

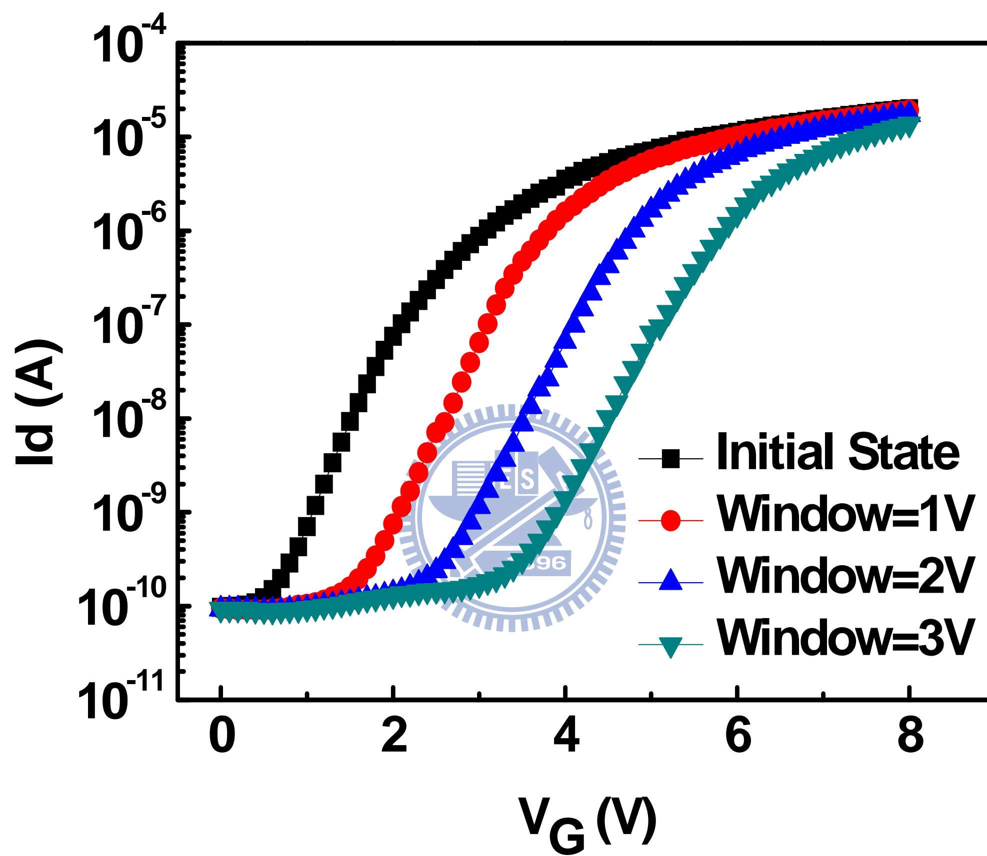


Fig. 3.8 The drain current versus gate voltage for split-gate SONOS with multi-level application.

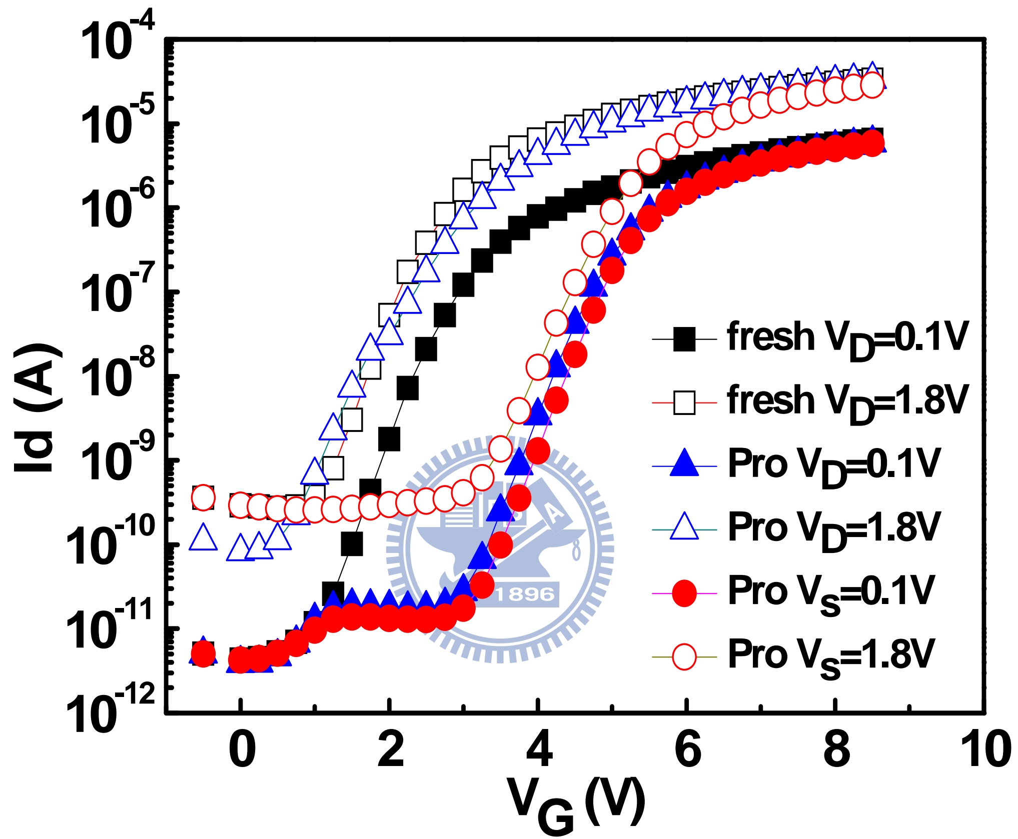


Fig. 3.9 The drain current versus gate voltage under forward read (open) and reverse read (void) for dual-bit split-gate SONOS.

	SSI	BBHH	STHH	Read
V_G	*9/10/11*	*-5*	0	Sweep
V_{CG}	0.9	floating	floating	2.1
V_D	*4*	*6*	floating	0
V_S	0	floating	floating	1.8
V_B	0	0	*10-2*	0

Table 1.1 Suggest bias conditions for dual-bit split-gate SONOS cell operation.

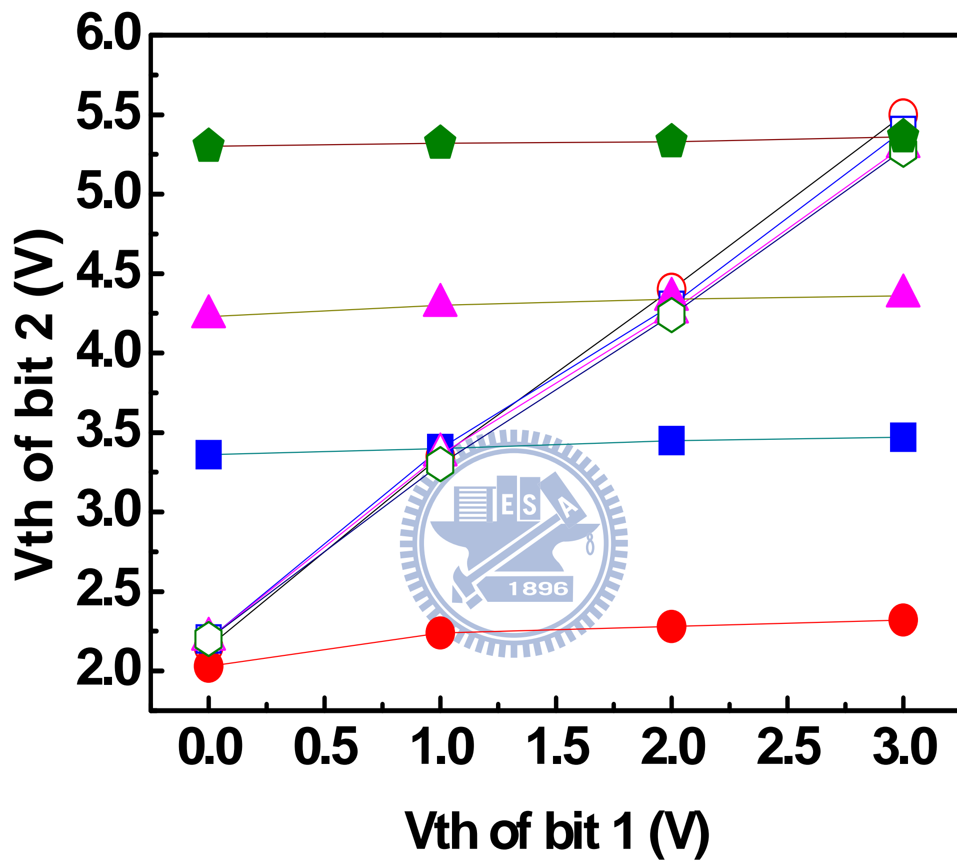
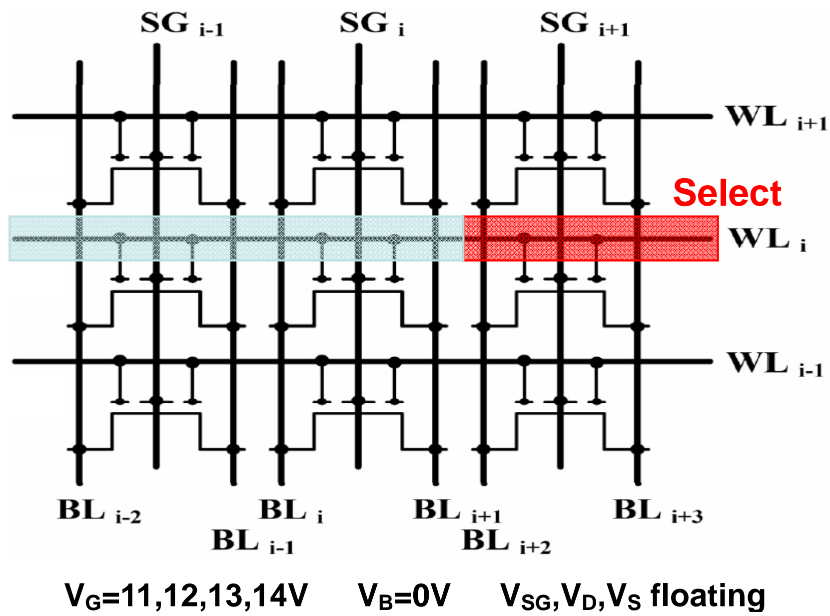
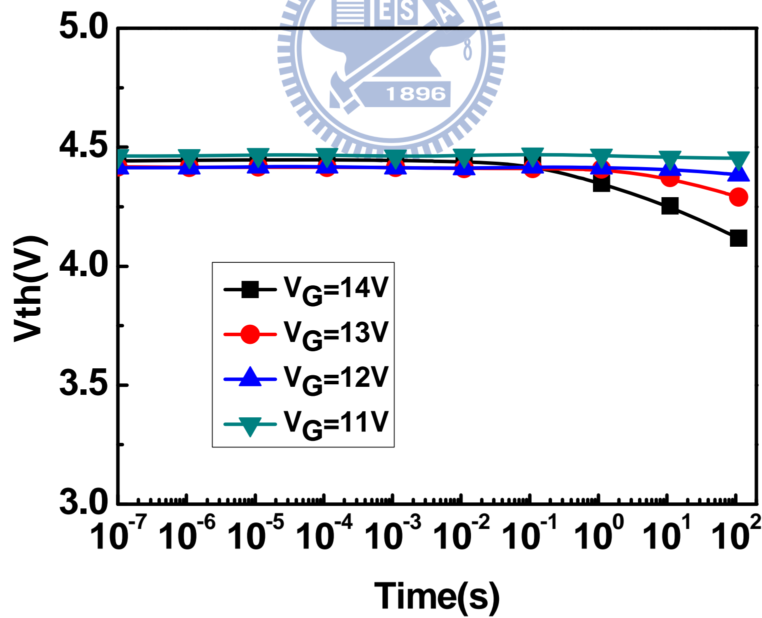


Fig. 3.10 The second-bit effect measurement for dual-bit split-gate SONOS.

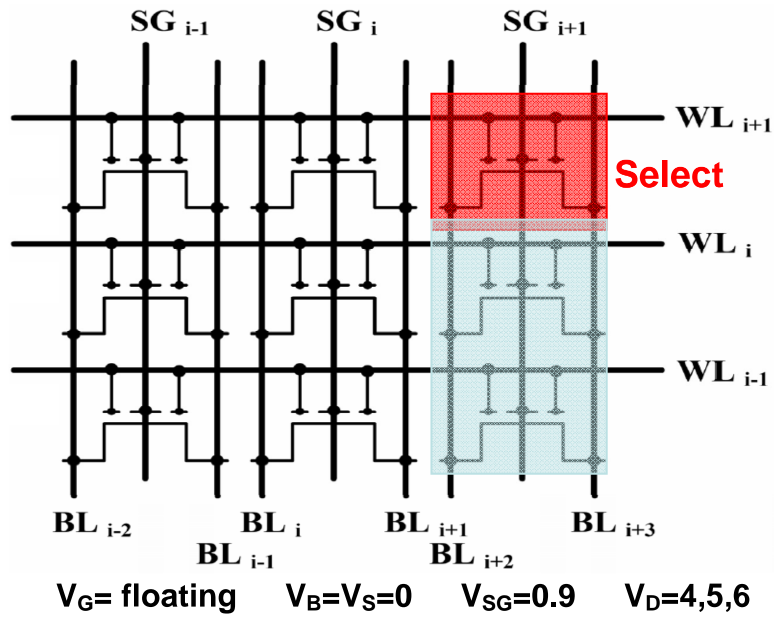


(a)

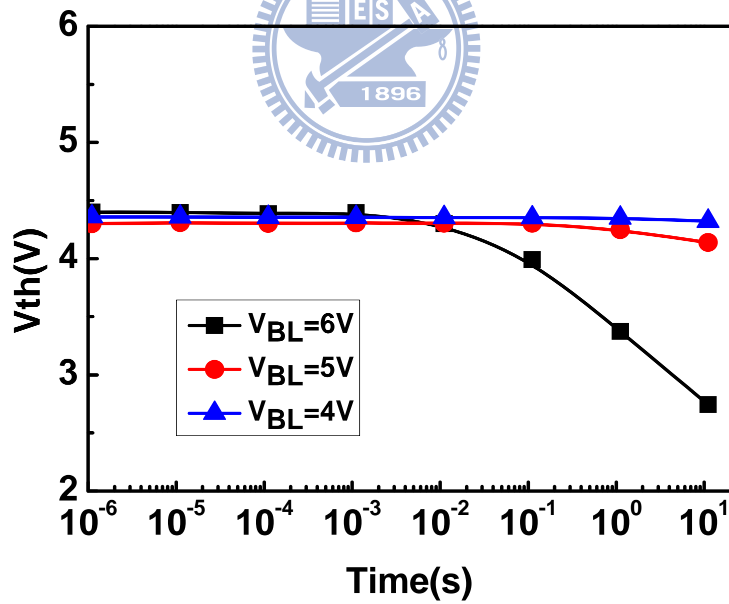


(b)

Fig. 3.11 Illustration of gate disturbance (a) and the measured gate disturbance (b) for split-gate SONOS.

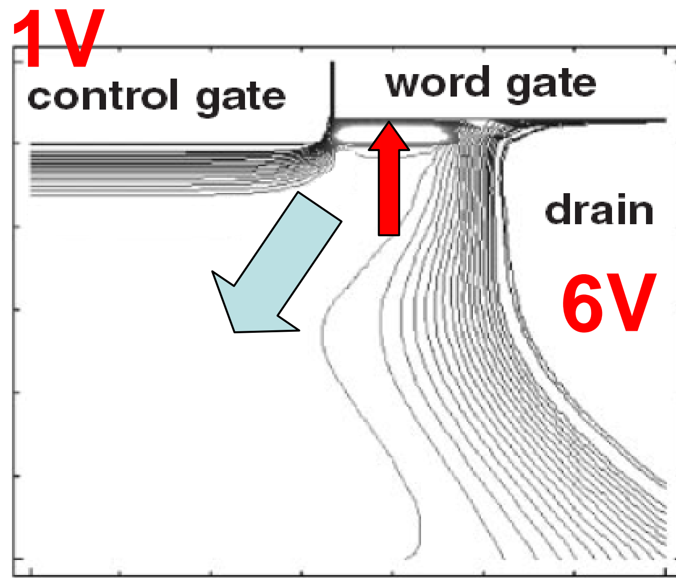


(a)

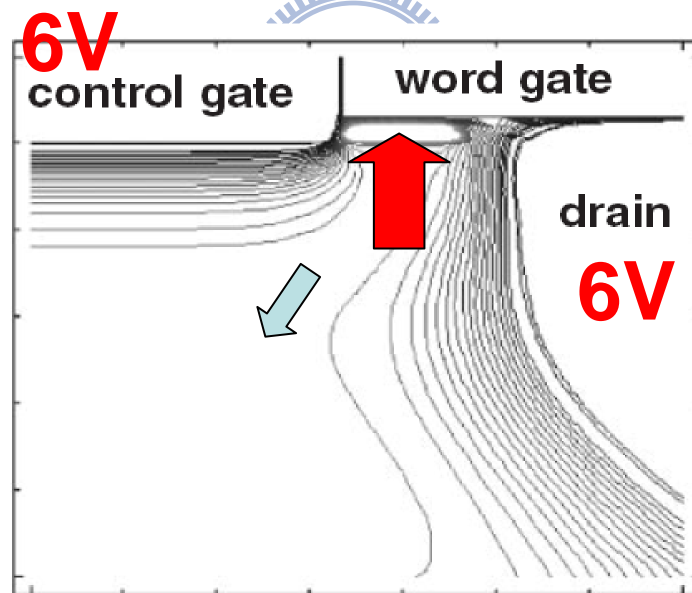


(b)

Fig. 3.12 Illustration of drain disturbance (a) and the measured drain disturbance (b) for split-gate SONOS.

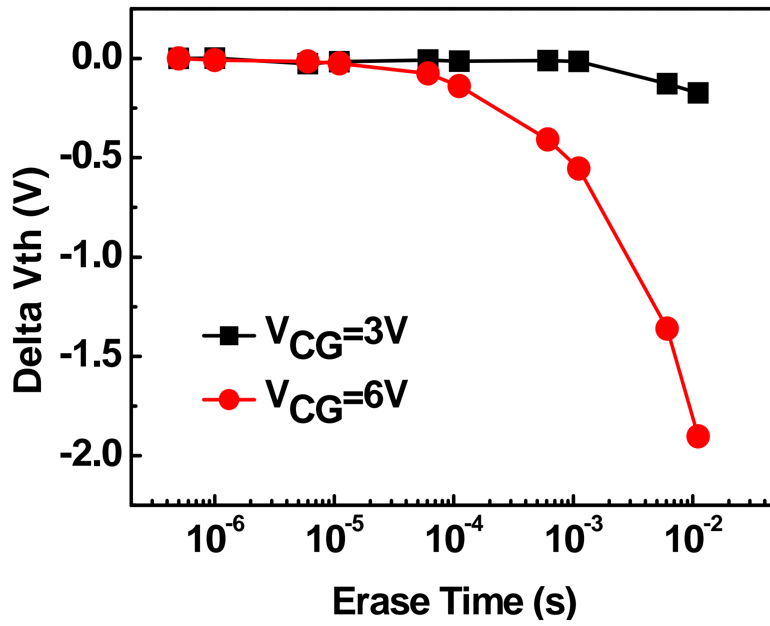


(a)

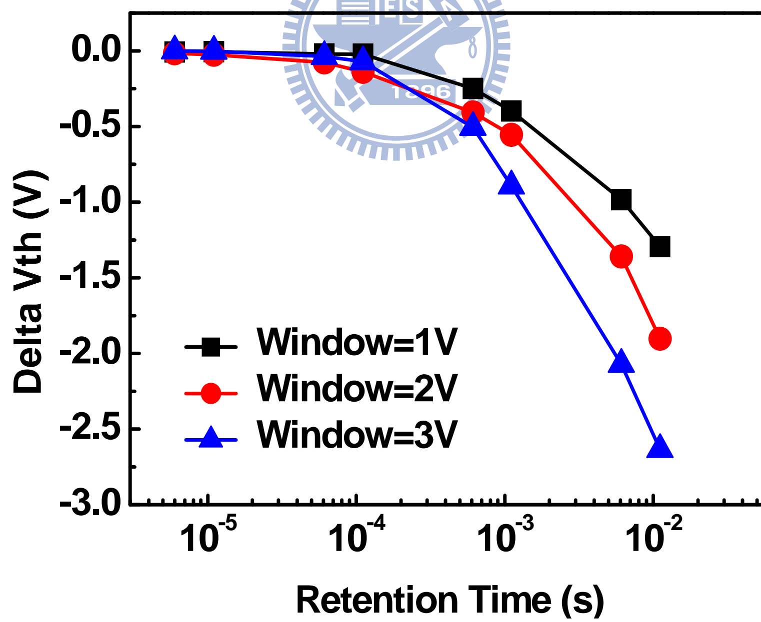


(b)

Fig. 3.13 Illustrate Contour plot of potential distribution around gap between gates for a small control-gate voltage (a) and a large control-gate voltage (b).



(a)



(b)

Fig. 3.14 The positive erasing transient with different control-gate voltage (a) and different programming window (b).

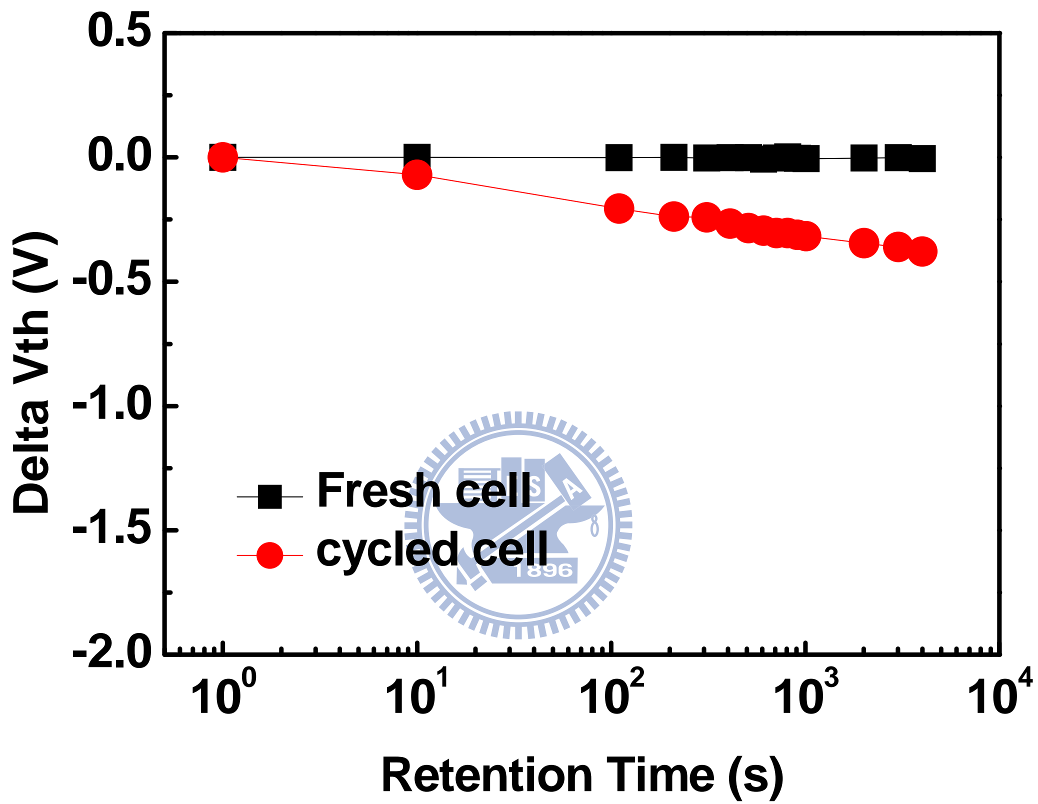


Fig. 3.15 The retention loss measurement for one shot fresh cell (red) and 10^4 P/E (black) at 85C.

Chapter 4

Misalignment of Distributions and Retention Loss Mechanisms for Conventional SONOS

4.1 Introduction

In this chapter, we will discuss the misalignment between the distribution of electrons and holes and the retention mechanisms for conventional SONSO flash memory. First, we discuss the mismatch distribution by using floating S/D charge pumping method. Next, we still use charge pumping method to analyze holes migration in the nitride storage layer. Finally, we explain both vertical and lateral retention loss mechanisms.

4.2 Principle of Charge Profile by Charge Pumping Method

4.2.1 Principle of Charge Pumping Method

The charge pumping method has been widely used for hot-carrier-related reliability characterization in MOSFETs. During a typical charge pumping measurement, a pulse string is applied to the gate terminal of a MOSFET while the substrate current (commonly called the "charge pumping current") is monitored. Since this current is a result of the recombination of majority carriers (coming from the substrate when the gate is biased between flat-band and accumulation) with the trapped minority carriers at the interface (coming from the source/drain when the gate

is biased to inversion), to first order the charge pumping current (I_{cp}) is nonzero only if the high level (V_h) and the base level (V_b) of the gate pulses cover both the threshold voltage and the flat-band voltage [14-15].

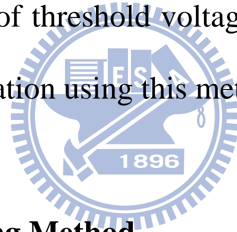
Unlike the conventional charge pumping (CP) method, the other two basic ways of charge pumping test to attain the profile scheme are demonstrated. First one is the fixed base CP (fixed base level and varying the top level) method with one side of drain (or source) floating and the other one is the fixed top CP (fixed top level and varying the base level) method with also one side of drain (or source) floating, which are defined as FV_b and FV_h, respectively.

In FV_b CP method, the setup is shown in Fig. 2.5 (a) in chapter 2, the gate is applied with a pulse string, as shown in Fig. 2.5 (b), and the I_{cp} can be measured from drain or source side with source or drain floating respectively. When measuring the charge pumping current $I_{cp,d}$ from the drain side, the minority carrier only contributed from the drain side and vice versa with $I_{cp,s}$. Therefore, we can obtain more precious information about the drain and source side from $I_{cp,d}$ and $I_{cp,s}$. By combining these two currents, we can profile the asymmetrical threshold voltage along the channel for both virgin and programmed cells [16-17].

4.2.2 Fixed Base Charge Pumping Method

Figure 4.1 (a) illustrates the threshold voltage profile of a programmed nitride storage memory cell, which contains a narrow threshold voltage peak near the drain side. Four regions are marked in this figure, and they are consistent with the I_{cp} curve tested from FV_b CP method in Fig. 4.1 (b). Fig. 4.1 (b) corresponds to the drain or

source junction area in Fig. 4.1 (a). After programming, localized trapped charges enhance the threshold voltage near drain side, which forms the asymmetrical threshold voltage profile in Fig. 4.1 (a). Therefore, the $I_{cp,d}$ and $I_{cp,s}$ curves shift toward the right, which corresponds to the regions B and C in Fig. 4.1 (b). The difference between curves B and C indicates the location and profile of the injected charges. As Fig. 4.1 (b) shows, the injection is closer to the drain side. It needs to be pointed out that I_{cp} keeps shifting rightward in region D, indicating a threshold voltage peak here. Moreover, $I_{cp,d}$ and $I_{cp,s}$ overlap in this region, which means the minority carrier coming from drain or source is passing through the peak region under the channel. For this reason, the equivalent interface traps are sensed and contribute the same $I_{cp,d}$ and $I_{cp,s}$. Thus, in FV_b CP method, data obtained in region D cannot be used to extract the exact profile of threshold voltage in large current region. We can, however, extract the accurate location using this method.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4.2.3 Fixed Top Charge Pumping Method

On the other hand, the equipment setup is similar to FV_b CP method instead of the gate pulse string which is fixed on a constant level upon the threshold voltage. In contrast, the I_{cp} curve shift caused by the threshold voltage peak, takes place in the low current region and has higher precision in FV_h CP method. Fig. 4.2 (a) illustrates I_{cp} test with FV_h CP method in logarithmic scale. Correspondently, region B, C and D in Fig. 4.2 (a) and Fig. 4.1 (b) also can be seen herein. I_{cp} in region D can be used to extract the accurate profile of narrow threshold voltage peak due to its low testing current. However, V_h is set larger than the highest threshold voltage along the whole channel, and I_{cp} current tested from drain and source are identical. FV_h CP method can only extract the width and value of narrow threshold voltage peak but cannot be used

to identify the location.

4.3 Misalignment Between Electron and Hole Distribution

Fig. 4.3 shows the measured charge pumping curve for both program state Fig. 4.3 (a) and erase state 4.3 (b) after 1 and 10k P/E cycles. For program state, after the first program operation, the program charges are injected into the nitride layer near the junction, therefore, the charge pumping curve tested from drain raise up late because of a high local threshold voltage near the drain. However, after thousands of P/E cycles, the curve tested from source raise up late than tested from drain, which is totally contrary to the initial state. It is because after large numbers of PE cycles, the misalignment distribution of electron and hole makes a large amount of holes accumulation near the drain, inducing the local threshold voltage lowering near the junction. Fig. 4.4 shows the charge pumping measurement for the program state after different numbers of P/E cycles. The leftward shift of curves indicates the accumulation of holes near the junction.

While for erase state, after first erase operation, the charge pumping curves tested from drain and source are the same curve, since there is no program charge in the channel. But after hundreds or thousands of P/E cycles operation, the two curves are split off as increasing the number of P/E cycles. It is because the misalignment makes the electrons accumulation in the channel, which can not be recombined by the hot holes.

Both electrons and holes accumulation in the channel will change the drain current flowing path and the electric field in the channel, resulting in the impact

ionization position move toward in to the channel, making the mismatch more serious. Fig. 4.5 shows the forward read threshold voltage measurement for various drain voltages. The saturation level of the curve is increasing with the number of cycles, which indicates the accumulation of electron far from the drain. It needs a larger drain voltage to completely deplete the program charge [18-22].

4.4 Hole Migration

In order to investigate the behavior of large amount of holes near the drain as discuss above. A fresh cell is initially over-erased. The charge pumping result is shown in Fig. 4.6 (a). The generated interface traps during erase are negligible since the Icp at V_h=5V is almost unchanged. Because a considerable amount of holes are injected into the nitride layer after erase, a leftward shift of the low V_h portion (for V_h<3.8V) of the Icp characteristic is observed. The cell is then baked at 125C. The up sift of the Icp curve indicates the hole above the drain spread out into the channel. A leftward than rightward sift of Icp curve with baking time can be observed, however, the gate induced drain leakage current (GIDL) shift rightward as baking time increasing as shown in Fig 4.6 (b). Hence, the holes distribution can roughly be deduced as shown in Fig. 4.6 (c). The peak of the hole distribution should be in the drain as black curve. As the hole spread out, the distribution of hole become to the red than green curve, and result in the local threshold voltage at the end of drain increase first than decrease [23].

Therefore, a large amount of holes accumulate in the drain edge caused by mismatch might induce a retention loss issue due to hole migration in the nitride layer.

4.5 Retention Loss Mechanisms

4.4.1 Retention Loss Mechanisms for Conventional SONOS

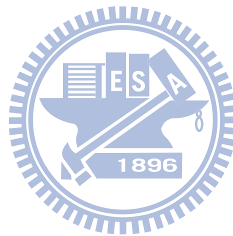
Two main model types have been published to explain the retention mechanism. The first model explains the retention loss by lateral redistribution of charge as discuss above. During cycling, both holes and electrons accumulate in the nitride layer due to mismatch between the distributions resulting from the program and erase operation. The holes are de-trapped by thermal activation in the nitride layer and move toward the electron before recombining [21, 24-26].

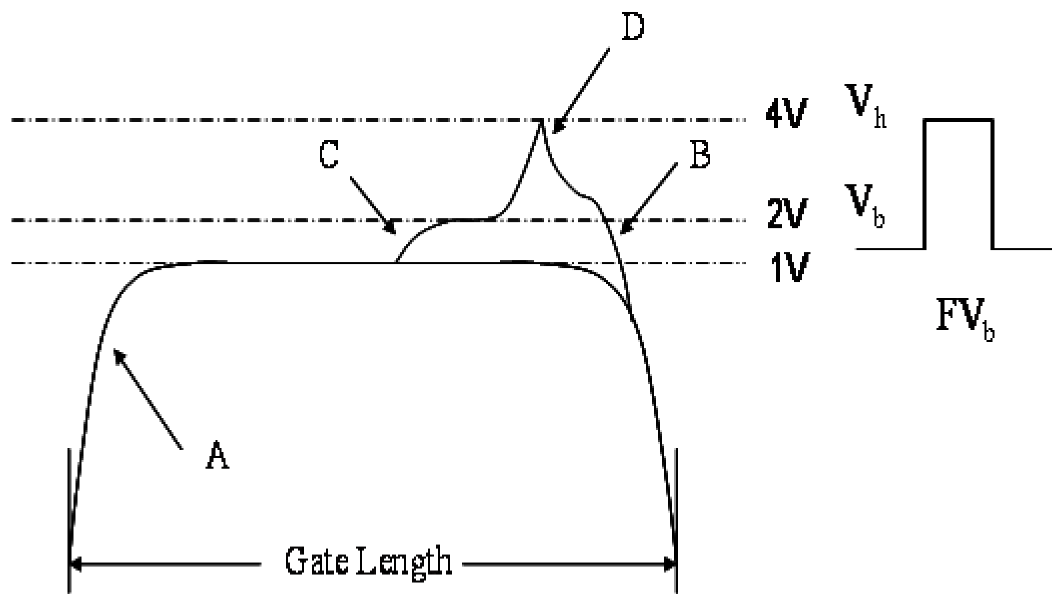
The second model of retention is the vertical loss of charge through the bottom oxide. During cycling, the bottom oxide is progressively degraded by successive programming and erasing operation, which allows a trap assist tunneling through the bottom oxide [26-28]. Fig. 4.7 explains the generation of trap sites in the bottom oxide during P/E cycling and opens a vertical leakage path between the nitride layer and the substrate. Every trapped charge builds up a potential barrier for the inversion channel charges. After the loss of one of the trapped charge, an additional percolation path can be generated and therefore a higher drain current will flow as shown in Fig. 4.8 [29-30].

4.4.2 Retention Loss Mechanisms for Split-Gate SONOS

Different from conventional SONOS by using drain side CHEI programming, the misalignment is much more important for split-gate SONOS by utilizing source side injection programming as shown in Fig. 4.9. Fortunately, the split-gate SONOS

can adjust the word-gate length to improve the mismatch and suppress the lateral retention loss, which we will discuss in the next chapter. However, the vertical direction retention loss is inevitable. Fig. 4.10 shows the threshold voltage evolution with retention time in a fresh Fig. 4.10 (a) and in a cycled Fig. 4.10 (b) split-gate cell with different gate bias are applied. No charge loss is observed for the fresh cell, since the bottom oxide is clean for a fresh cell. While the retention loss for a cycled cell is dependant on applied gate bias caused by vertical direction retention loss.





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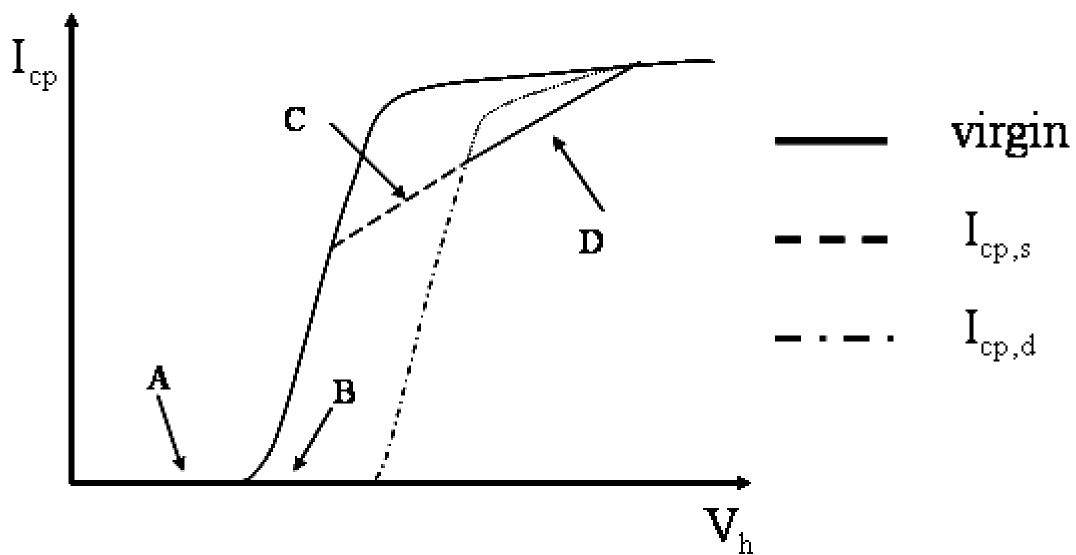
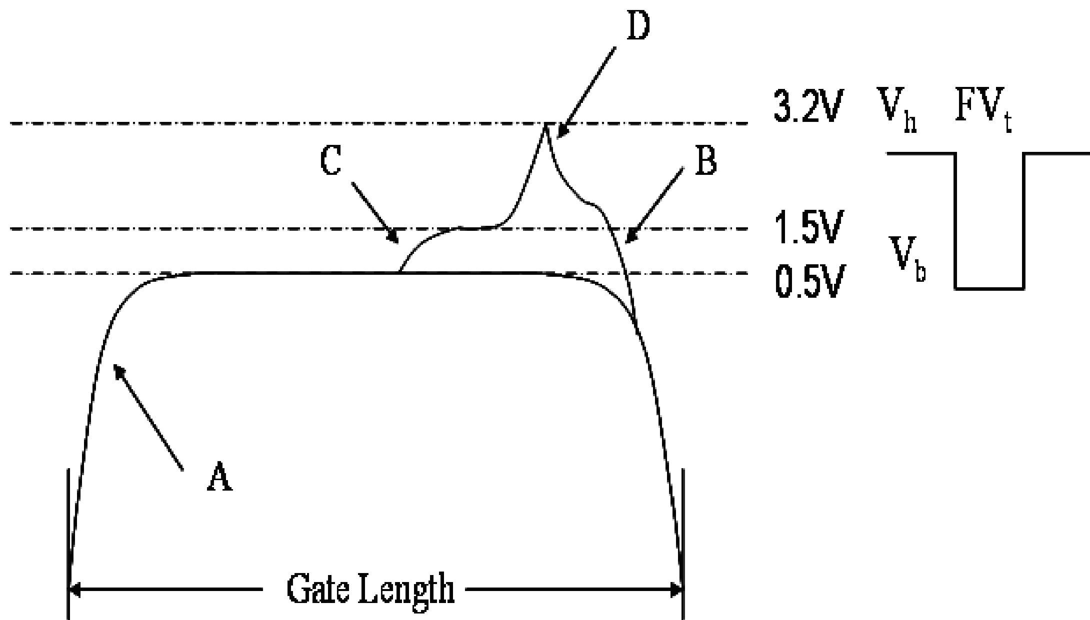
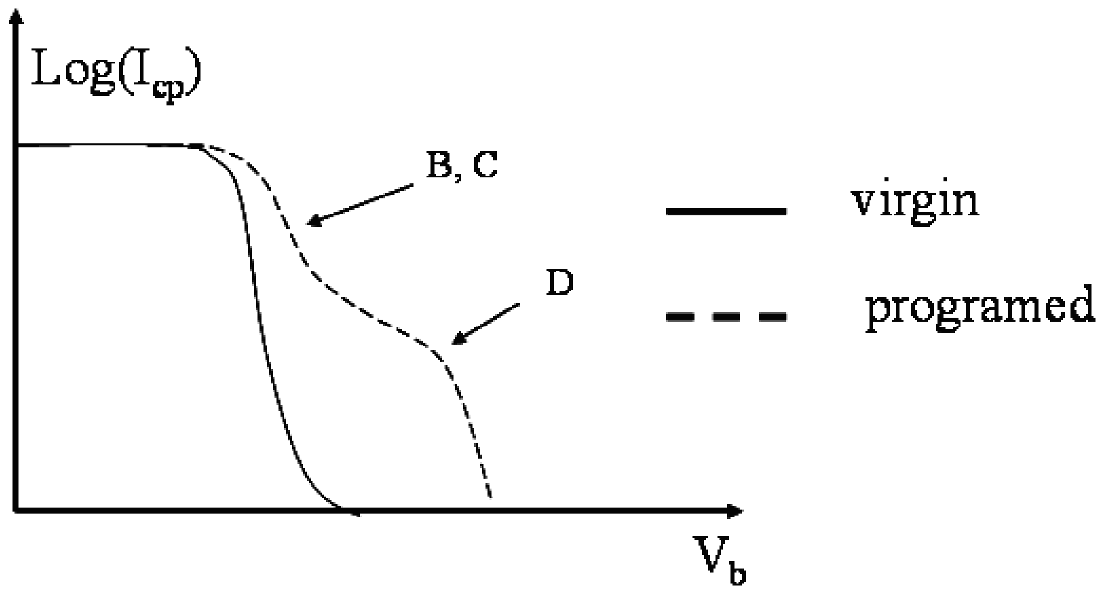


(b)

Fig. 4.1 Diagram of V_T profile in a programmed nitride storage memory cell (a) and the illustration of I_{cp} curves versus V_h before and after programming (b).

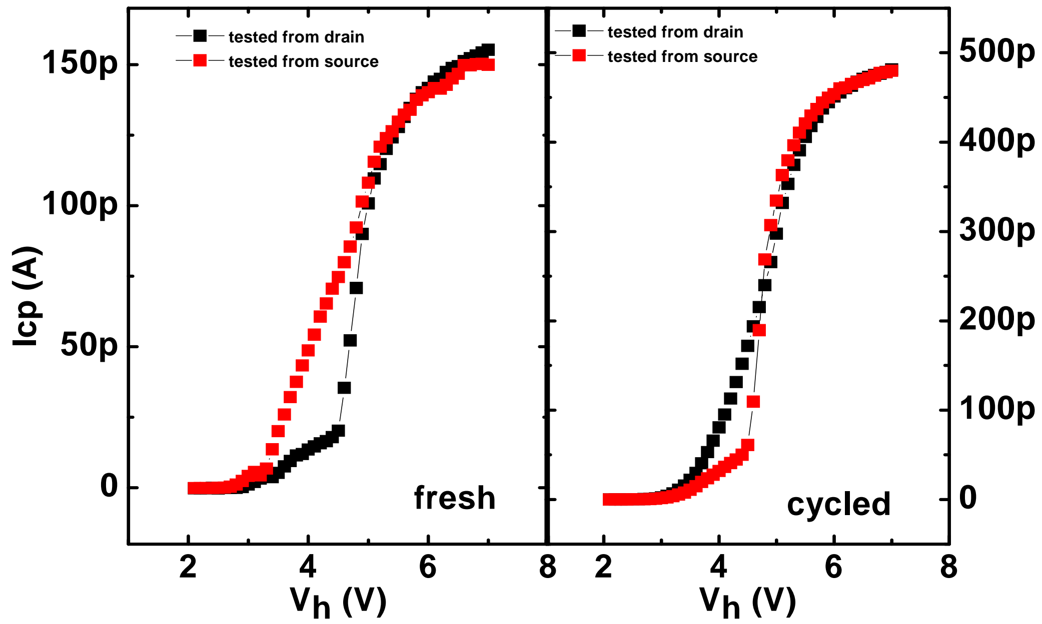


(a)

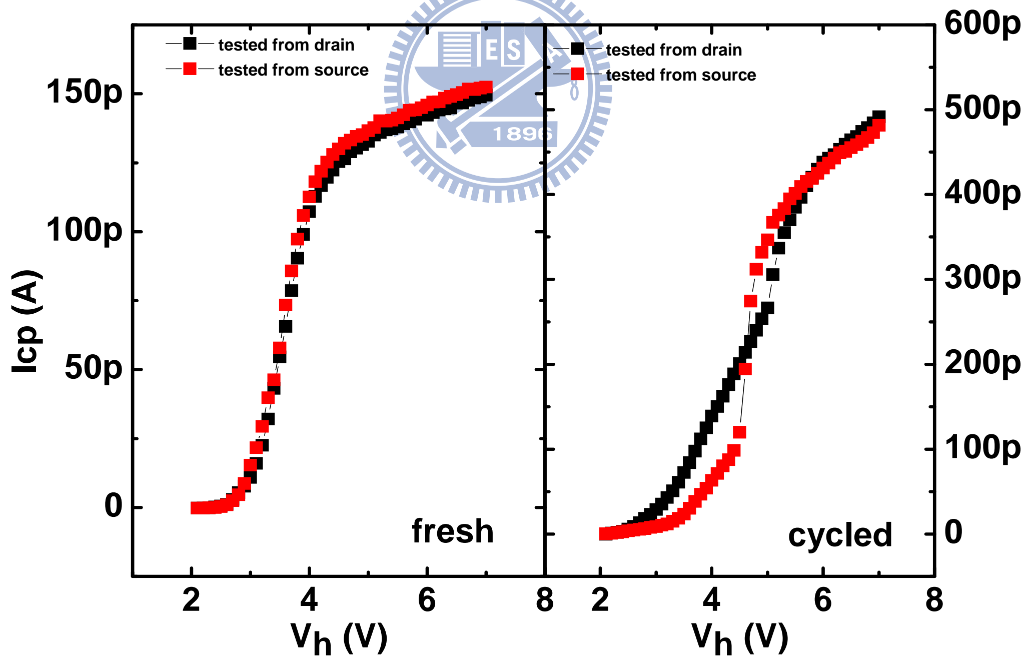


(b)

Fig. 4.2 Diagram of V_T profile in a programmed nitride storage memory cell (a) and the illustration of I_{cp} curves versus V_b before and after programming (b).



(a)



(b)

Fig. 4.3 The charge pumping current versus V_h of program state (a) and erase state (b) after 1PE cycle (left) and 10kPE cycles (right) for conventional SONOS.

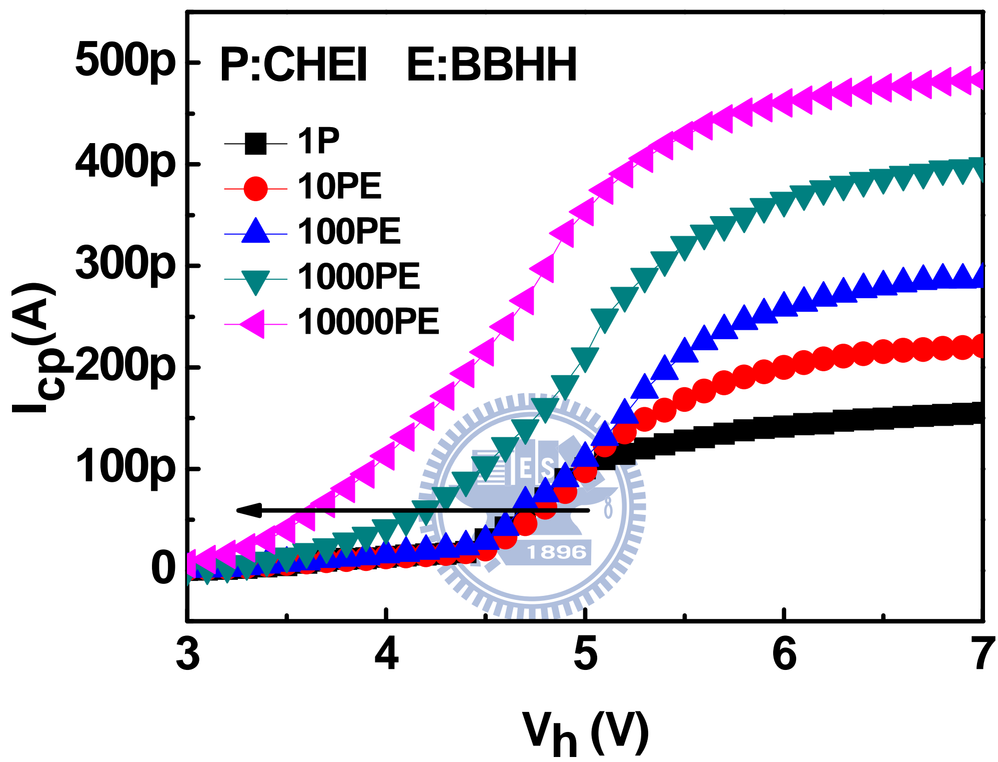
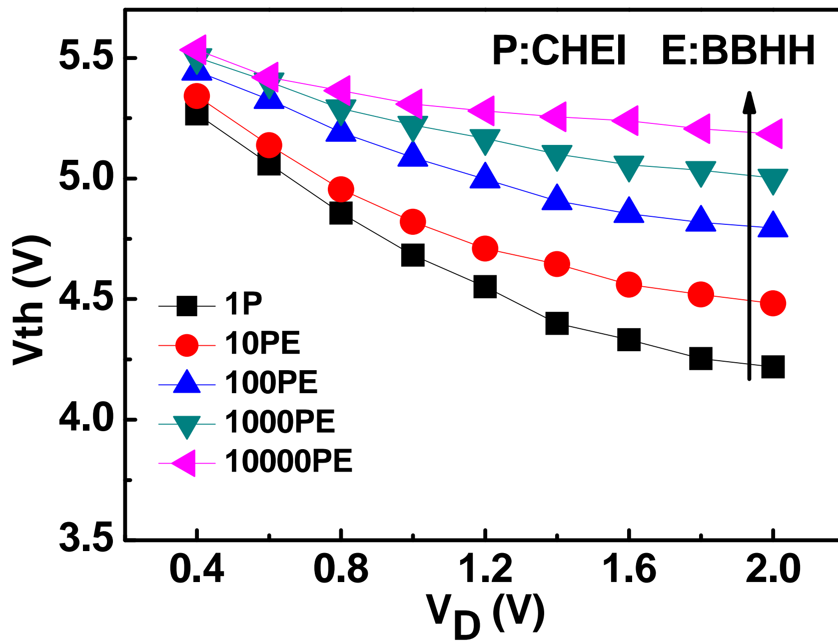
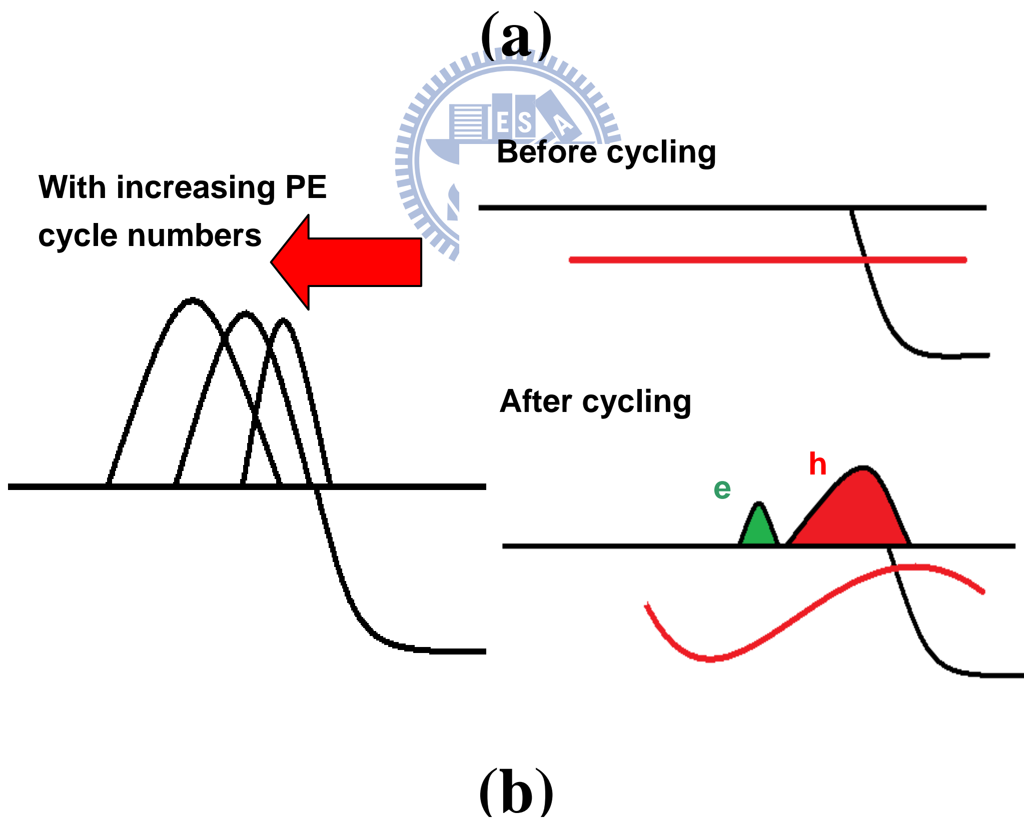


Fig. 4.4 The charge pumping current versus V_h of a programmed cell after different numbers of P/E cycles for conventional SONOS.

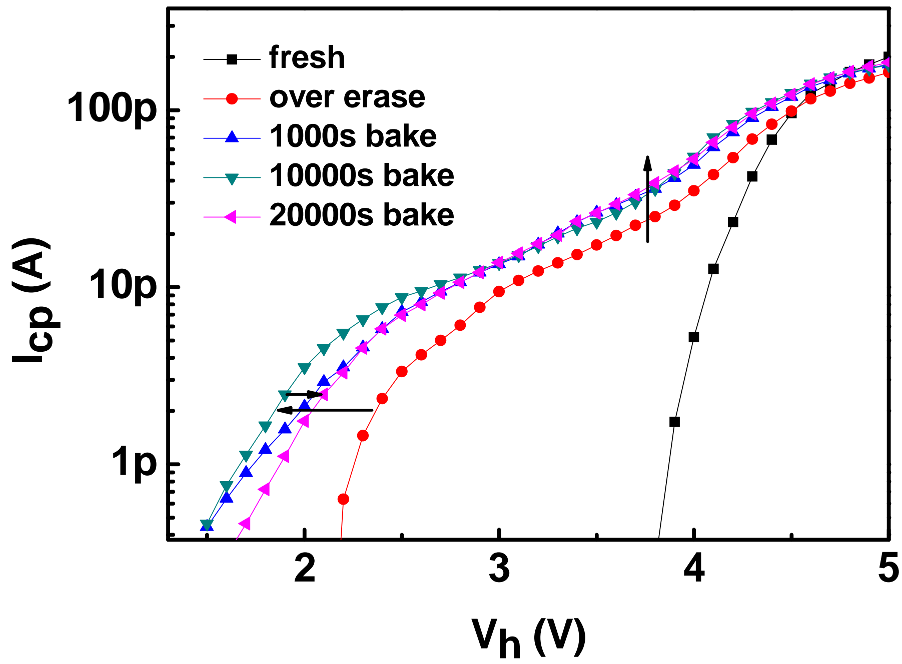


(a)

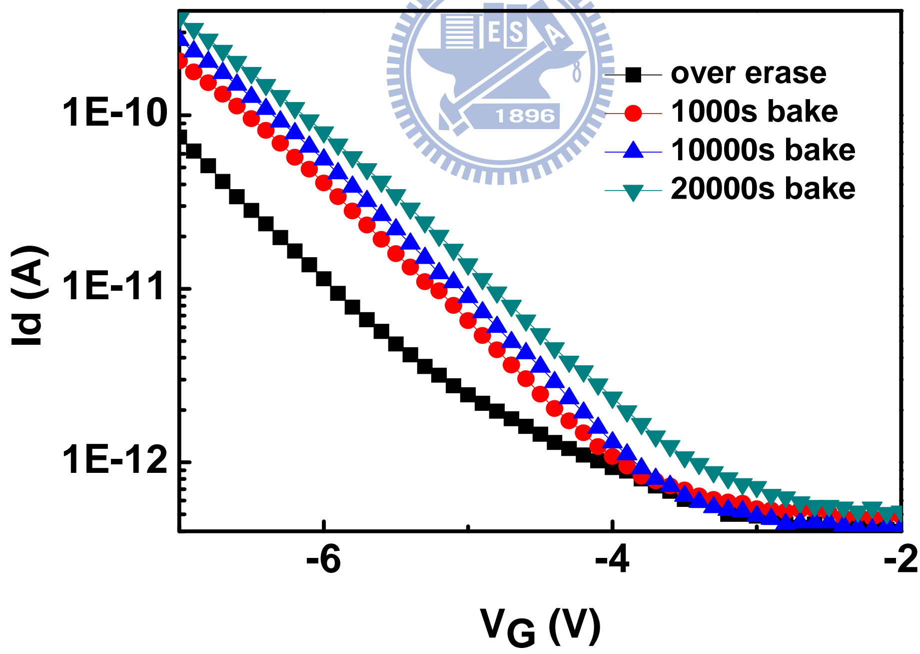


(b)

Fig. 4.5 Forward read threshold voltage for various drain voltages (a). The accumulated electrons and holes may alter the current flowing path and make the impact ionization position move into the channel (b).



(a)



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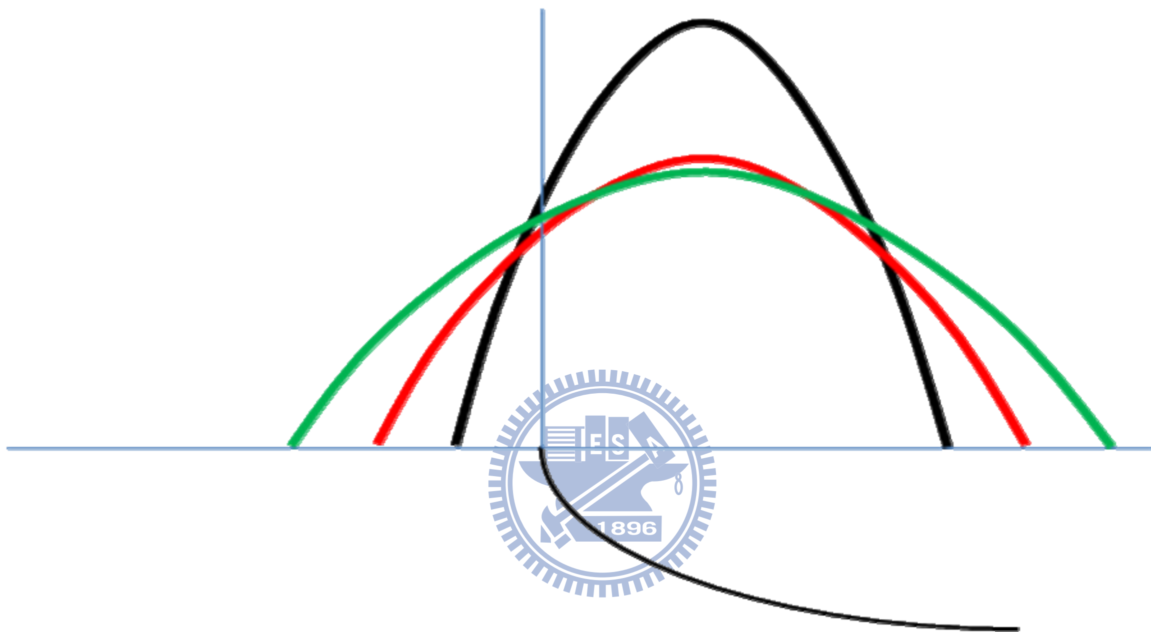


(c)

Fig. 4.6 Charge pimping characteristics (a), GIDL measurement (b) and deduced hole distribution (c) of a over-erasing fresh cell, and subsequently after bake of 20k seconds at 150C.

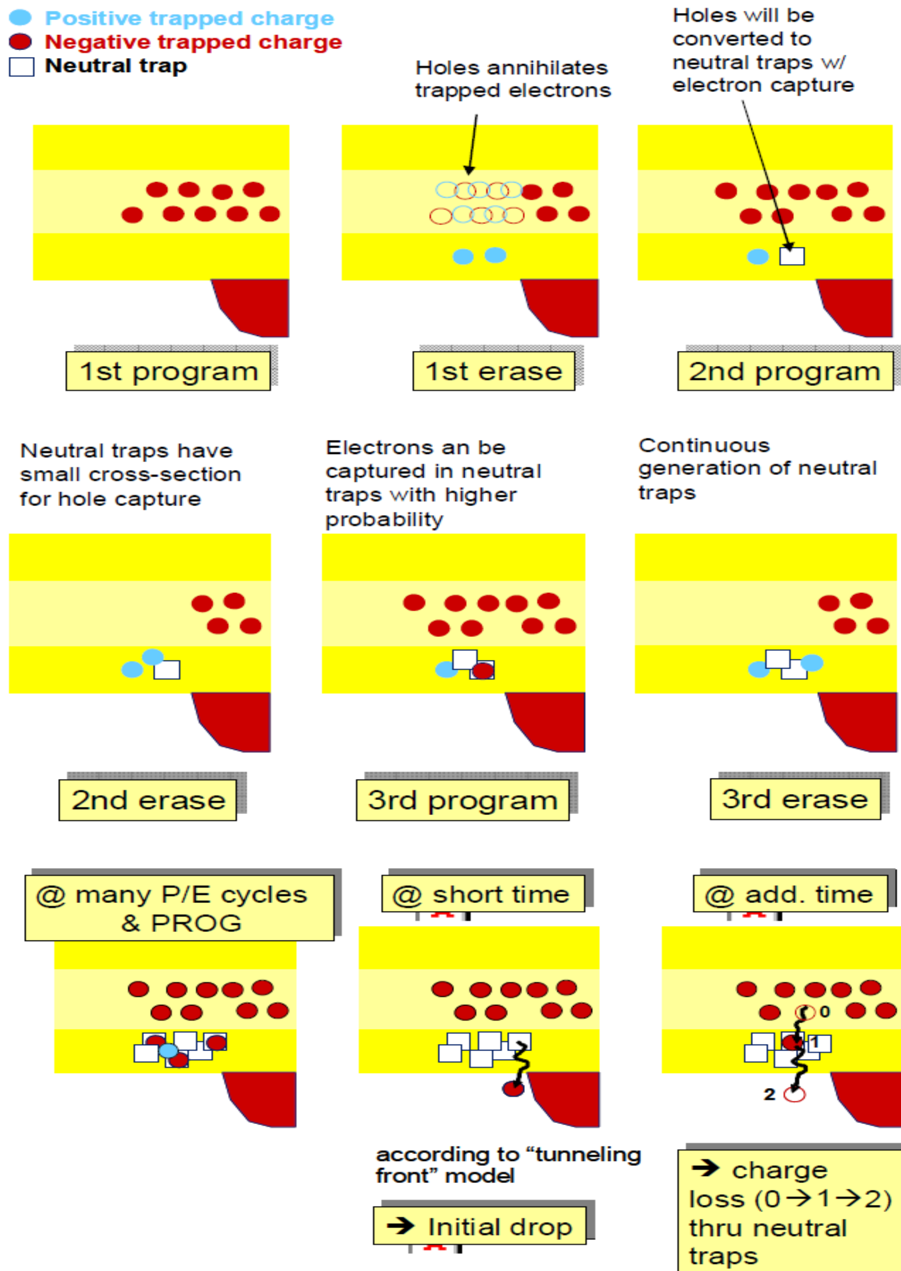
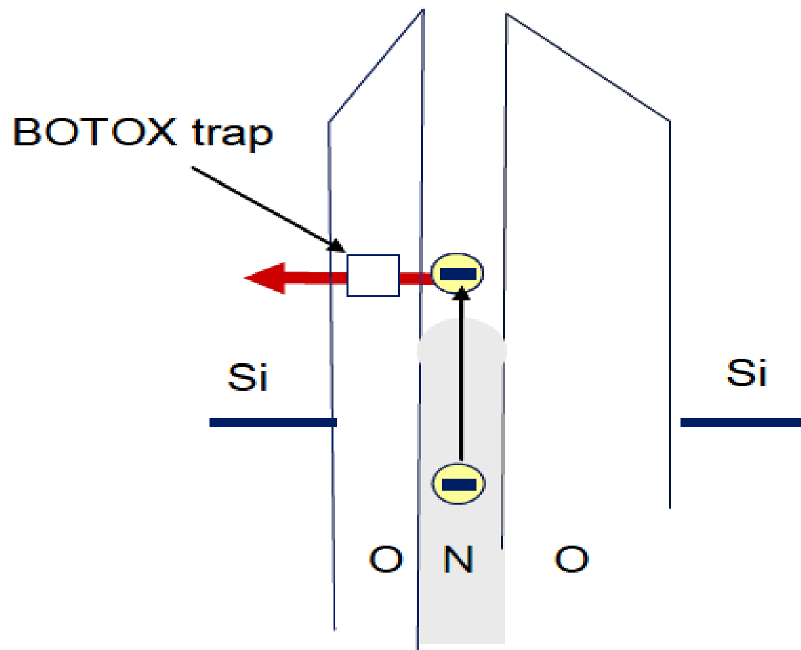
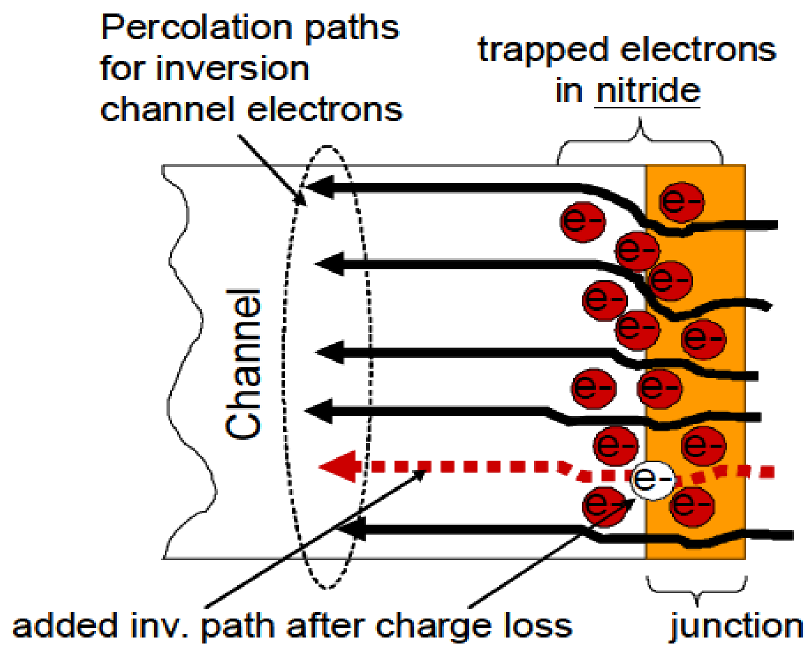


Fig. 4.7 Schematic description of neutral trap formation in the bottom oxide.



(a)



(b)

Fig. 4.8 Schematic of charge loss of thermal activated electron trapped in the nitride trough traps inside the bottom oxide (a). After loss of one of the trapped charges an additional percolation path can be generated (b).

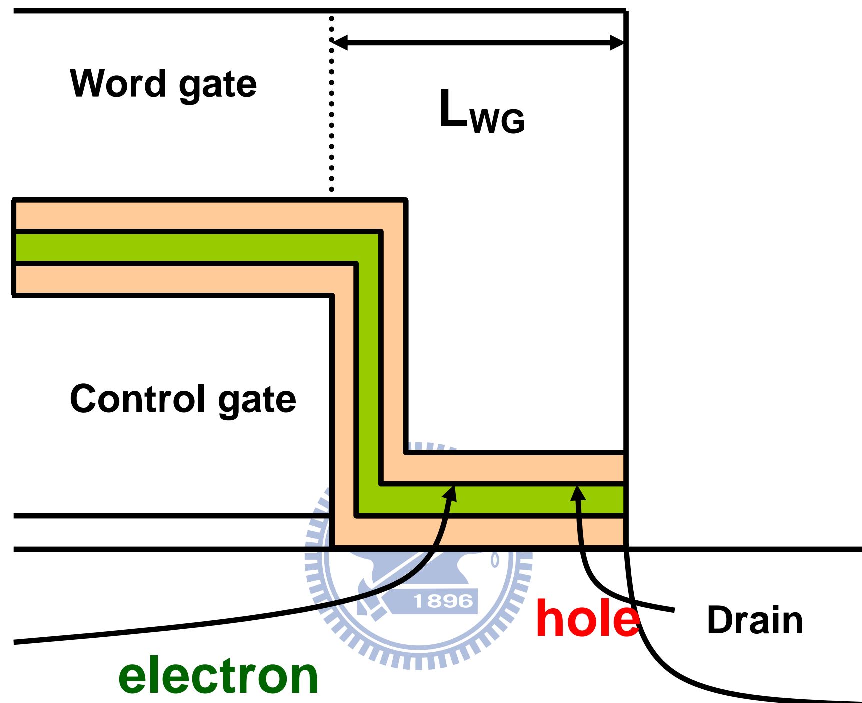
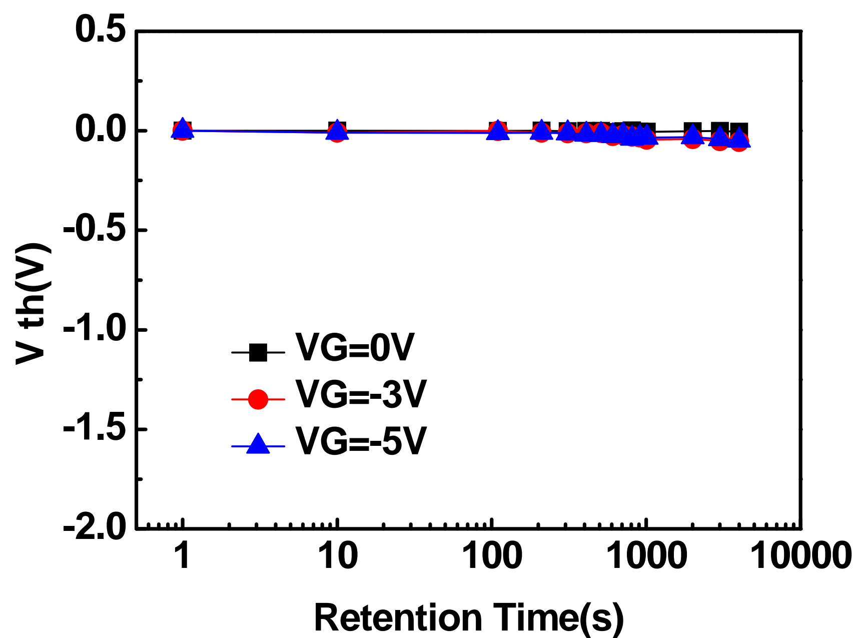
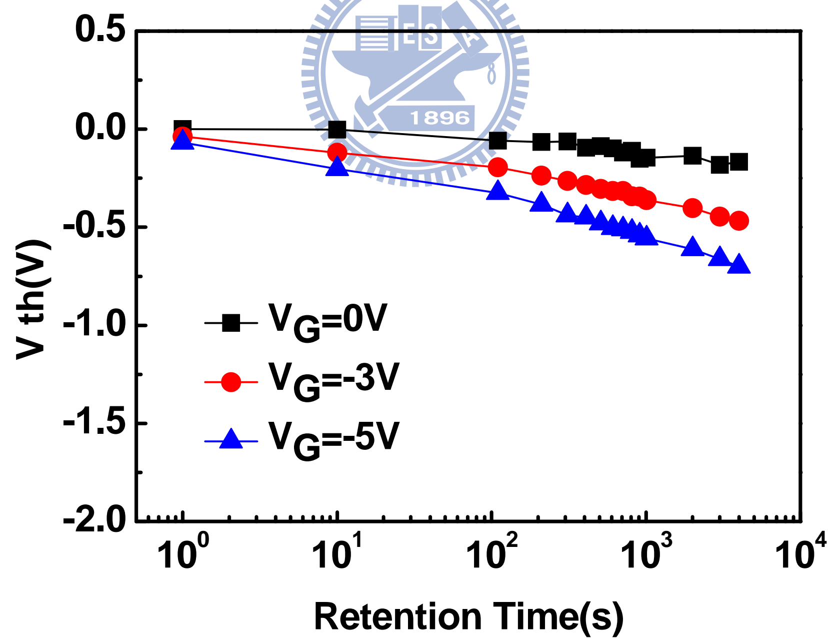


Fig. 4.9 The schematic of misalignment between SSI and BBHH for split-gate SONOS.



(a)



(b)

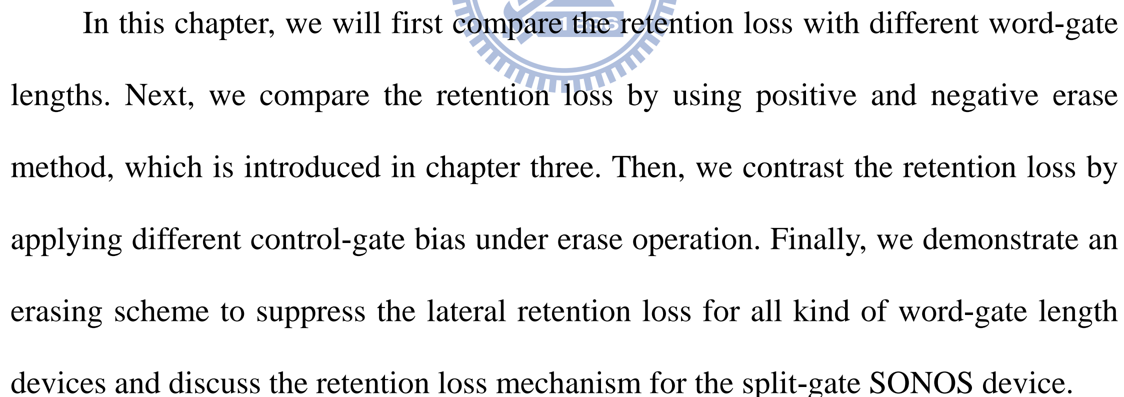
Fig. 4.10 Dependence of threshold voltage on retention time in a fresh cell (a) and a 10k PE cell (b). The gate bias is 0V, -3V and -5V.

Chapter 5

Retention Loss Mechanism and Methods to Suppress Lateral Retention Loss for Split-Gate SONOS

5.1 Introduction

Different from conventional SONOS, the split-gate SONOS can adjust the word-gate length (sacrifice spacer length) or the control-gate bias under the erase operation to reduce the misalignment and suppress the lateral retention loss. By comparing the split-gate SONOS with different word-gate length, we can separate the vertical and lateral retention loss, which can not be achieved in conventional SONOS.



In this chapter, we will first compare the retention loss with different word-gate lengths. Next, we compare the retention loss by using positive and negative erase method, which is introduced in chapter three. Then, we contrast the retention loss by applying different control-gate bias under erase operation. Finally, we demonstrate an erasing scheme to suppress the lateral retention loss for all kind of word-gate length devices and discuss the retention loss mechanism for the split-gate SONOS device.

5.2 Retention Loss with Different Word-Gate Length

Fig. 5.1 shows the programming and erasing transient for word-gate length L_{WG}=0.13, 0.12 and 0.10 um. It was found that the programming transient is independent of the word-gate length, while the erasing transient is dependent of word-gate length. The shorter length of the word-gate length is, the faster the eraseing

operation does. It is because the shorter word-gate length device makes the injected electron more close to the junction. Thus, a shorter word-gate length is favorable for the compensation of electron by hole. Fig. 5.2 shows the V_{GIDL} versus $V_{channel}$ for the split-gate SONOS with different word-gate lengths. Since the GIDL current is sensitive to the charge above the junction, we can use this method to compare the injected electron distributions. In Fig. 5.2 (b), the shorter word-gate length device has larger slope, since the program charge is injected more close to the junction than long word-gate length device [4, 31-33]. It is worth noting that under GIDL measurement, the drain pulse is applied of 3V to suppress another impact ionization in the junction, which has been discussed in chapter three.

Fig. 5.3 shows the endurance of the three devices. An important increase of erase state threshold voltage is observed, and the situation becomes better for shorter word-gate length device because of the different injection point of electrons and holes. While for the program state, the threshold voltage has only a little decreasing at first than increasing at last. The incensing of program state threshold voltage is also induced by misalignment, but the decreasing of threshold voltage is cause by interface degradation and non-uniform nitride charge distribution [34]. Fig. 5.4 shows the drain curve versus gate voltage for program state and erase state after different P/E cycles. It was found that the sub-threshold swing is strongly degraded after large number of successive programming and erasing operation for program state, resulting from the generation of interface state near the junction and resulting in decreasing of the threshold voltage. However, for erase state, the sub-threshold swing has only a little difference. It is because the "local inversion" region induced by excess holes in the nitride, shadowing the interface state as shown in Fig 5.5. Fig. 5.6 (a) shows the erase transient before and after cycling, and the erase efficiency is degraded throughout

cycling for long word-gate device. It is due to hole accumulated in the nitride, or in the bottom oxide at the drain side, that cause a repulsive effect to the injection of holes in the next cycling as shown in Fig. 5.6 (b).

Since we utilize the same programming and erasing condition for all three devices during cycling, we can assume the bottom oxide are equally damaged. Then, the program state retention loss between two devices is caused by lateral retention loss as shown in Fig. 5.7. It can be said that, vertical retention loss should dominate the total retention loss, however, under a large misalignment situation, the lateral retention loss will give an other non-negligible loss portion. For erase state, the retention loss first increase than decrease a little. The increasing of threshold voltage is cause by drift of holes jump out from bottom oxide into substrate, while the decreasing of the threshold is cause by lateral redistribution of holes in the nitride layer. The larger misalignment between electrons and holes distributions, the more serious of holes drift and lateral move can be observed.

5.3 Retention loss with different Control-Gate Bias

5.3.1 Positive Erase Versus Negative Erase

Fig. 5.8 shows the endurance between the negative and positive erasing scheme. Although the large positive control-gate bias can narrower the potential contour to make the hot hole injecting into the nitride layer, it will repulse the positive charge moving away from the control-gate and make the misalignment more serious. It is the reason why the positive erase efficiency is lower than negative erase, resulting in slower retention transient as discussed in chapter three.

5.3.2 Negative Erase with Adding a Control-Gate Bias

Therefore, we can change the holes distribution by using negative erase but adding a small control-gate bias instead of floating it. Fig. 5.9 shows the erase transient with applying different control-gate bias. A small negative control-gate bias can attract the holes close to the control-gate to make a faster erasing operation, on the contrary, a small positive control-gate bias may repulse the hot holes away from the control-gate to make a slower erasing operation [32]. Fig. 5.10 and Fig 5.11 show the endurance and retention. The misalignment of electrons and holes distribution can be improved by adding a small negative bias and degrade by adding a small positive bias. The lateral retention loss can be split off again, which verifies the lateral retention is caused by misalignment distribution of electrons and holes.

All in all, the spilt-gate SONOS is very flexible for adjusting the electrons and holes distributions, no meter by altering the word-gate length or by adding different control-gate bias.

5.4 An Erasing Scheme to Suppress Lateral Retention Loss

5.4.1 The mechanism of STHH Erase

Here, we propose an erase scheme to suppress the lateral retention loss. The set up is shown in Fig 2.6. The gate is grounded, and the source and drain are kept floating while apply a pulse to the substrate. The mechanism of this erasing scheme is shown in Fig. 5.12. At time T1, the substrate is at V_{base} and a built in voltage between drain and substrate. At time T2, the pulse applies the substrate to V_{top} and still a built

in voltage between drain and substrate. As time goes from T2 to T3, the substrate bias immediately back to V_{base}, while the floating drain can not catch up but slowly back to the initial position. Therefore, a large band banding occurs at the time from T2 to T3 and generates hot holes to achieve erasing operation. Although the applied pulse width can be micro-second or less, the real erasing time is the time for floating drain move from V_{top}-V_{bi} to V_{base}-V_{bi}. Therefore, we call this erase scheme Substrate Transient Hot Hole erase [7-8, 35].

Fig. 5.13 shows the time versus voltage tested from substrate and drain during erasing at the same V_{top}=9V but different V_{base}. The lager V_{base} –V_{top} induces large voltage drop to generate more hot holes. In Fig. 5.13, we can observe that the breakdown voltage of the p-n junction is about 7V, that is, the largest voltage drop is 7V. Fig 5.13 (a) is the case that allows 7V of drop, and the erase window is about 2.2V. However, the erase window in Fig 5.13 (b) is 2.8V with the same voltage drop of 7V. It is because the V_{base} induces an electric field, making the hole more easily to inject into the nitride layer. Although the larger V_{base} induces the stronger electric field and makes hole easily to jump into the nitride layer, the large V_{base} could reduces the voltage drop and reduces the erase window as shown in Fig 5.13 (c).

Fig. 5.14 shows the erasing window versus pulse width and pulse counts. Since the real erasing time is the RC time constant, the erase window has no relation with the pulse width. Fig. 5.15 shows erase window versus various of V_{base} and V_{top}. At V_{base} =0V, the four V_{top} cases drop the same voltage of 7V, and have the same erase window. At V_{base} =1V, the window can not increase in the case of V_{top}=8V because of the lowing of votage drop. The erase window increases for the other three cases caused by building an electric field to enhance the hole injecting into the nitride. At

V_{base} =2V, the enhancement of electric field become more stronger to make hole injecting into nitride. However, the voltage drop is decreasing to decrease the erase window for V_{top}=8V and 9V cases. The same result happens to V_{base} =3V or higher. All in all, the three important components determine the erase efficient: the voltage drop, the electric filed builds by V_{base} and the RC time constant.

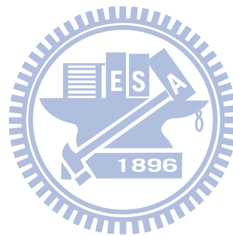
5.4.2 STHH Erase for Conventional SONOS

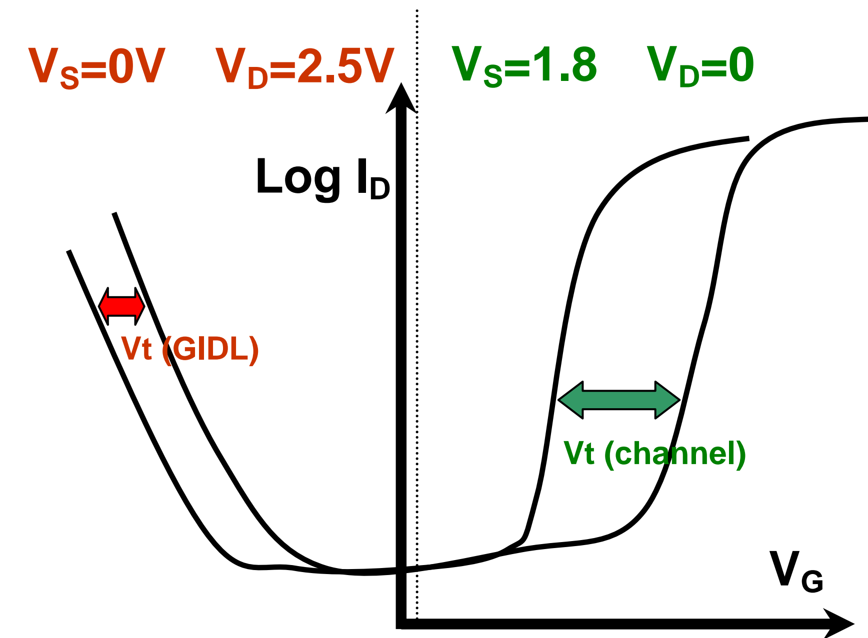
Fig. 5.16 shows the charge pumping measurement for conventional SONOS using CHEI programming and STHH erasing before and after cycling as discussed in chapter four. It was found that the curve does not change their position before and after cycling, which indicates less holes accumulation as shown in Fig 5.17 compared to Fig 4.4. Fig 5.18 shows the forward read threshold voltage of a programming cell after P/E cycle. The curves only have a little shift indicates less electrons accumulation in the channel. A great match between electrons and holes distributions can be achieve by utilizing the STHH erasing scheme to completely erase the program charges in the nitride layer. The interface state can also be calculated by using Fig. 4.4 and Fig 5.17. A small number of STHH will be generate is observed.

5.4.3 STHH Erase for Split-Gate SONOS

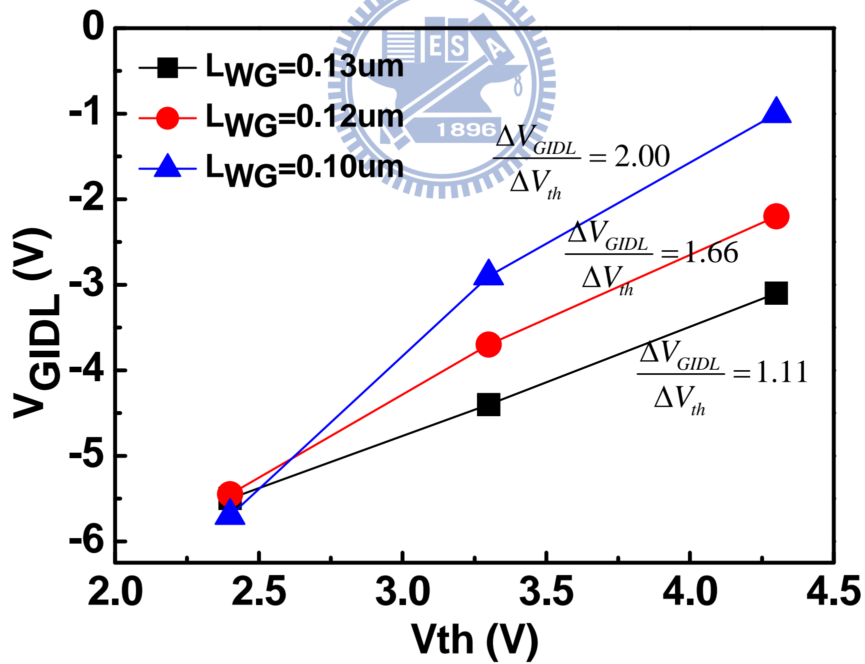
Fig. 5.20 shows the endurance of the split-gate SONOS with different word-gate length by using STHH erasing scheme. The erase state threshold voltage is almost independent of word-gate length because the STHH erasing scheme has a widely distribution to erase the charge a little far away from junction. Fig 5.21 shows the retention loss for both program state and erase state. No matter program state or erase

state, both of them are independent of word-gate length because of a good match between electrons and holes. For program state, no split off between two curves indicates the suppression of the lateral retention loss. And because of low misalignment between electrons and holes, the remaining hole in the bottom oxide is low, too. Therefore, a small hole drift and lateral redistribution can be observed in the retention loss of erase state.





(a)



(b)

Fig. 5.1 Schematic for Vt(channel) and Vt(GIDL) (a) and the measured Vt_{GIDL} versus $Vt_{channel}$ with different word-gate length of split-gate SONOS (b).

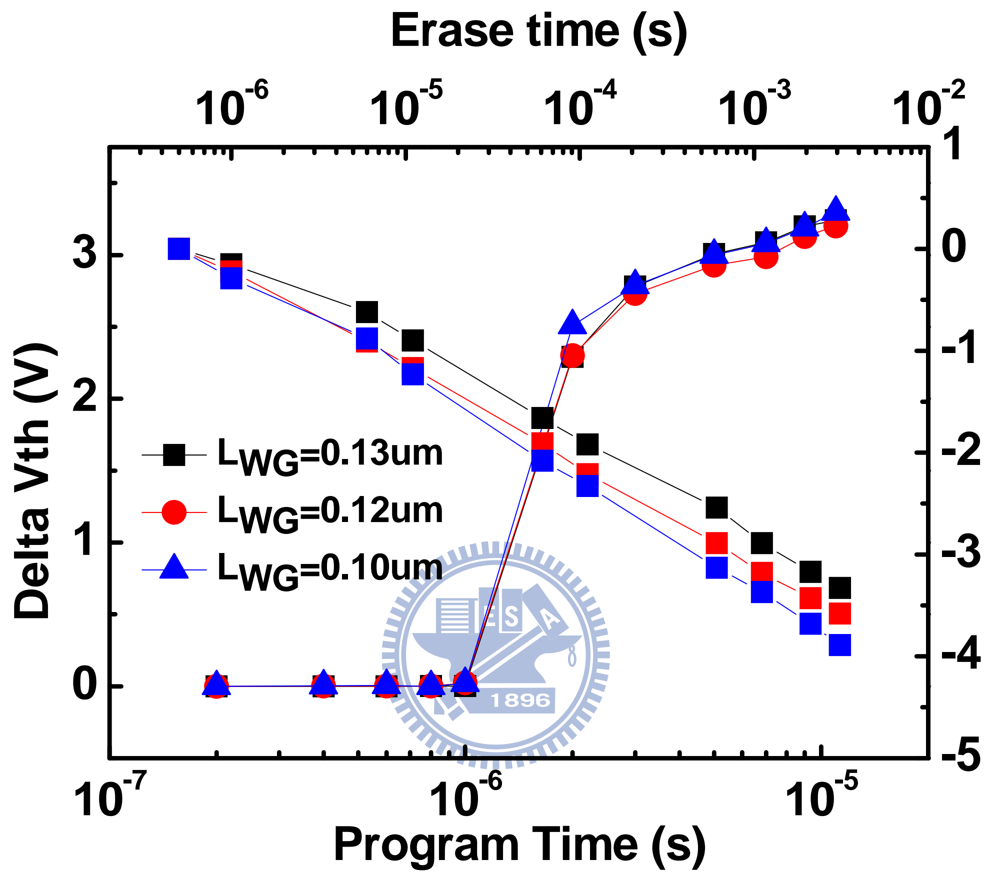


Fig. 5.2 The programming and erasing transient of split-gate SONOS with different word-gate length.

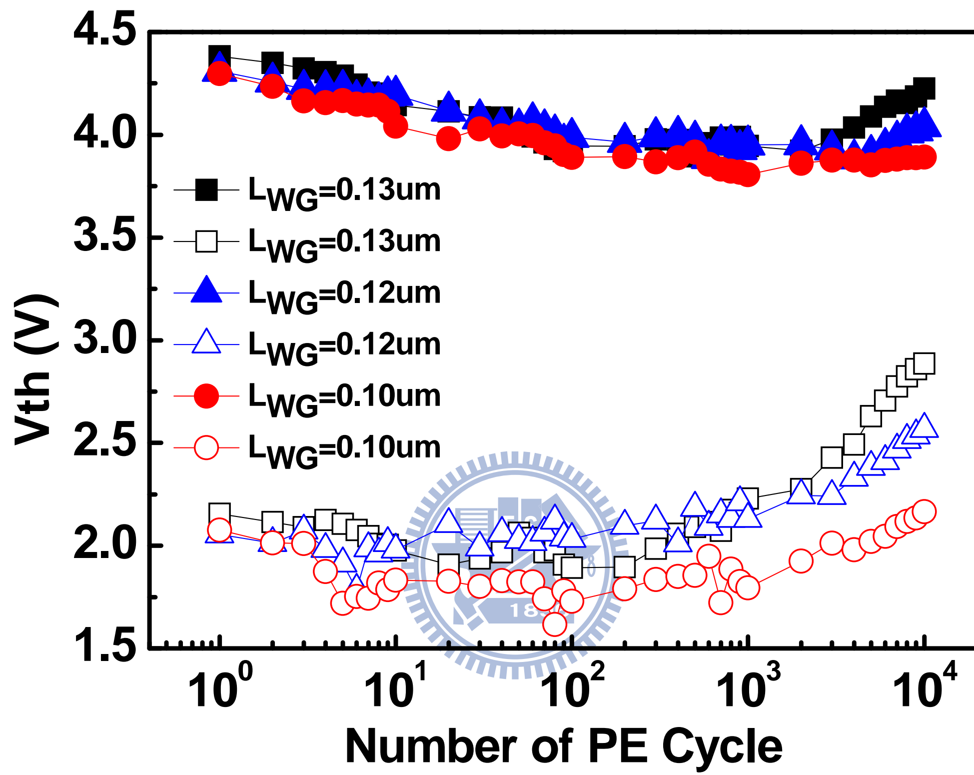
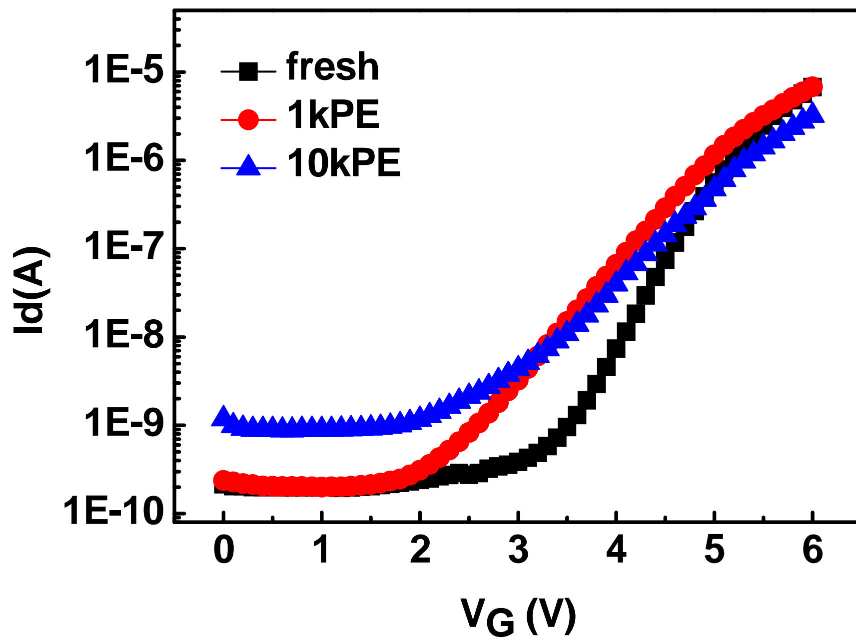


Fig. 5.3 Endurance of split-gate SONOS with different word-gate length.



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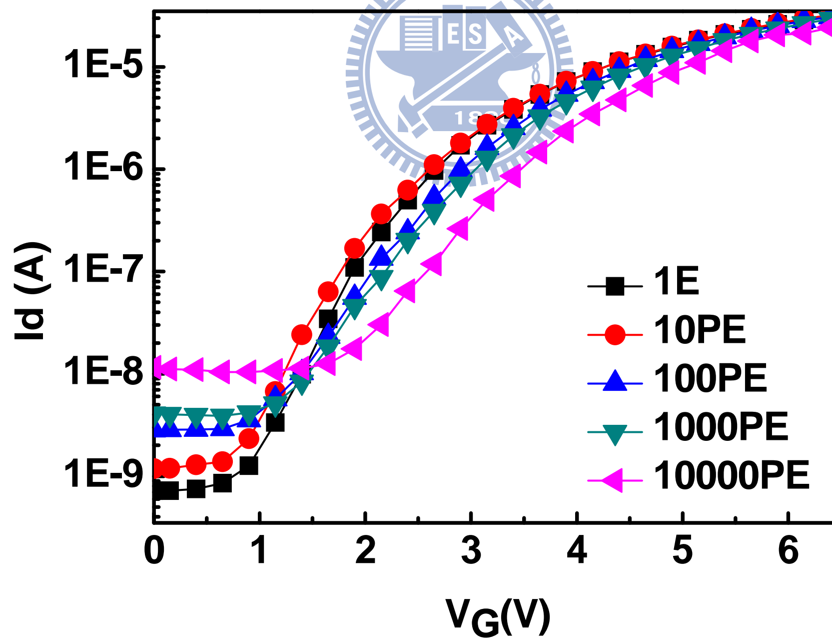


(b)

Fig. 5.4 The drain current versus gate voltage at program state (a) and erase state (b) for split-gate SONOS.

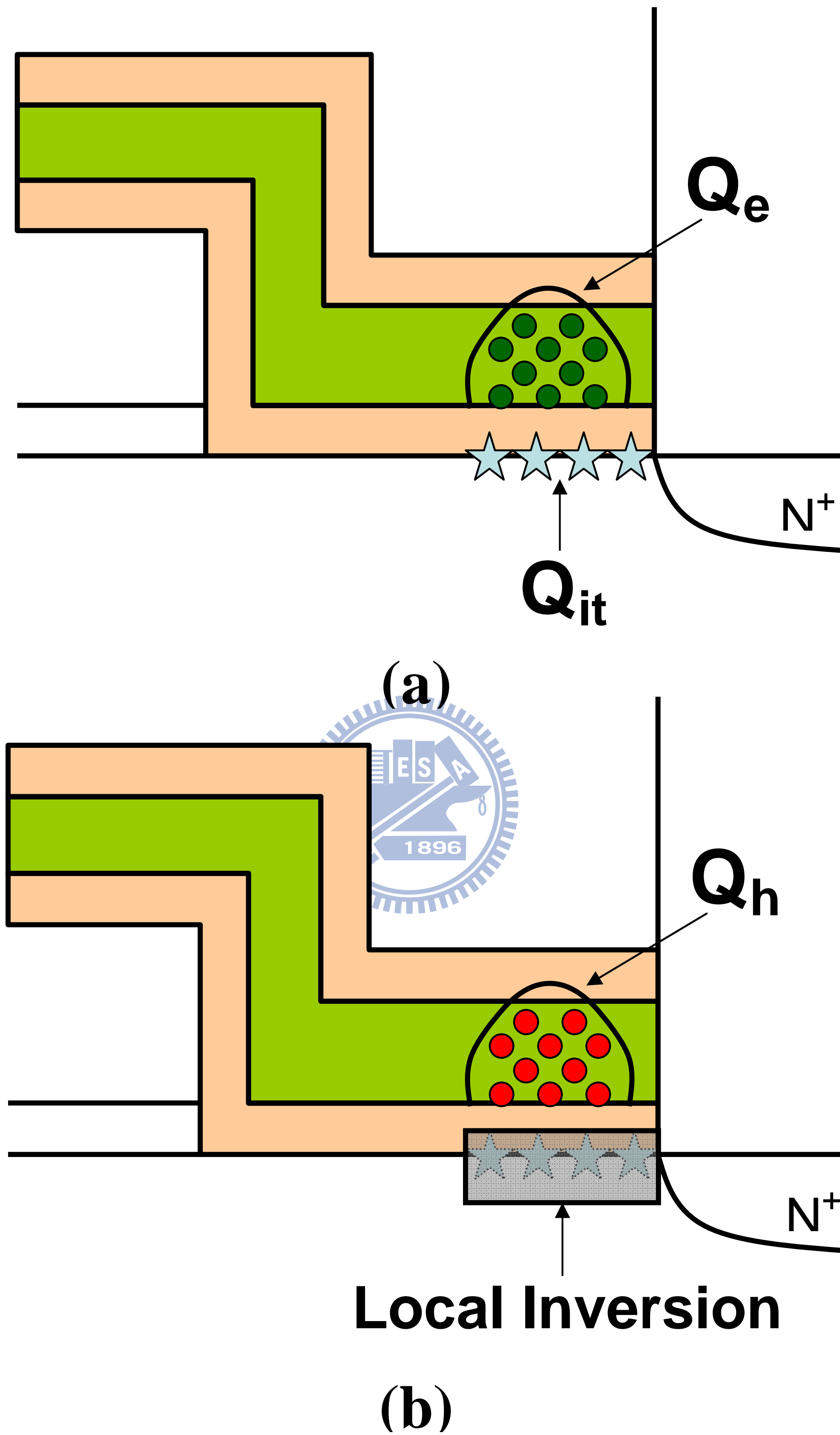
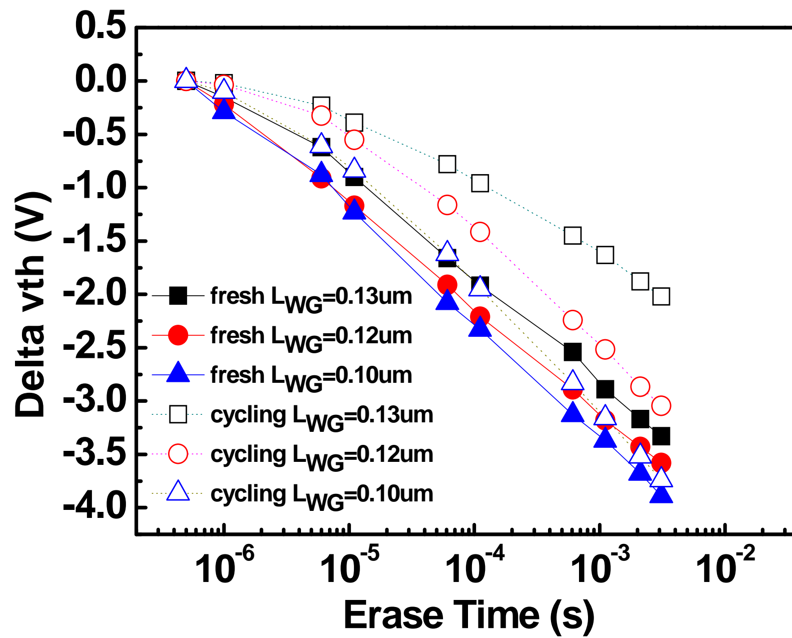
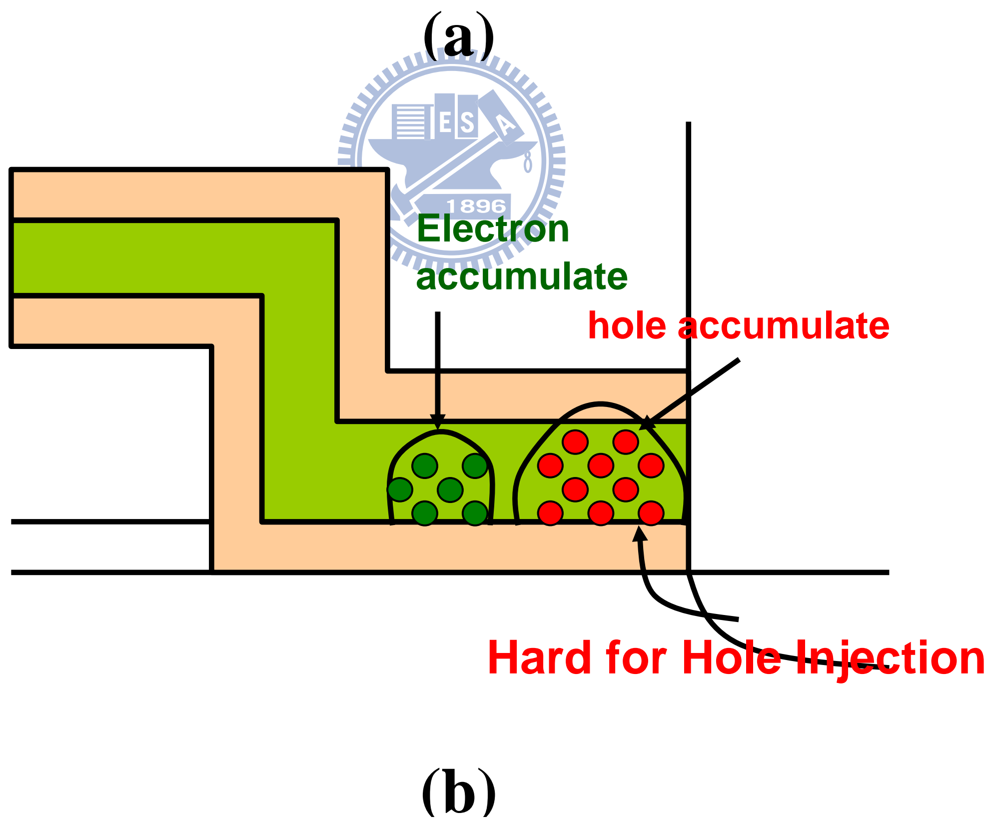


Fig. 5.5 Illustration of electrons, holes and interface state charge in cycled device being read at program state (a) and erase state (b).



(a)



(b)

Fig. 5.6 The erasing transient for fresh cell (void) and 10k cycled cell (open) (a), and the illustration for hole to inject after cycling (b).

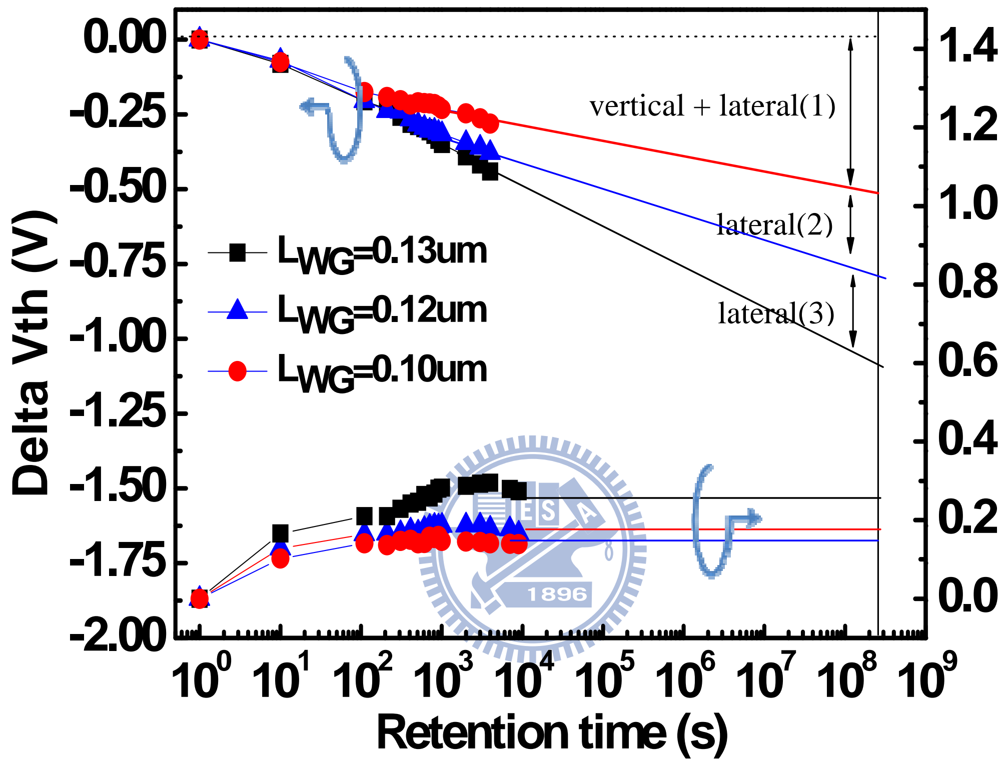


Fig. 5.7 Retention loss for split-gate SONOS with different word-gate lengths at 85C.

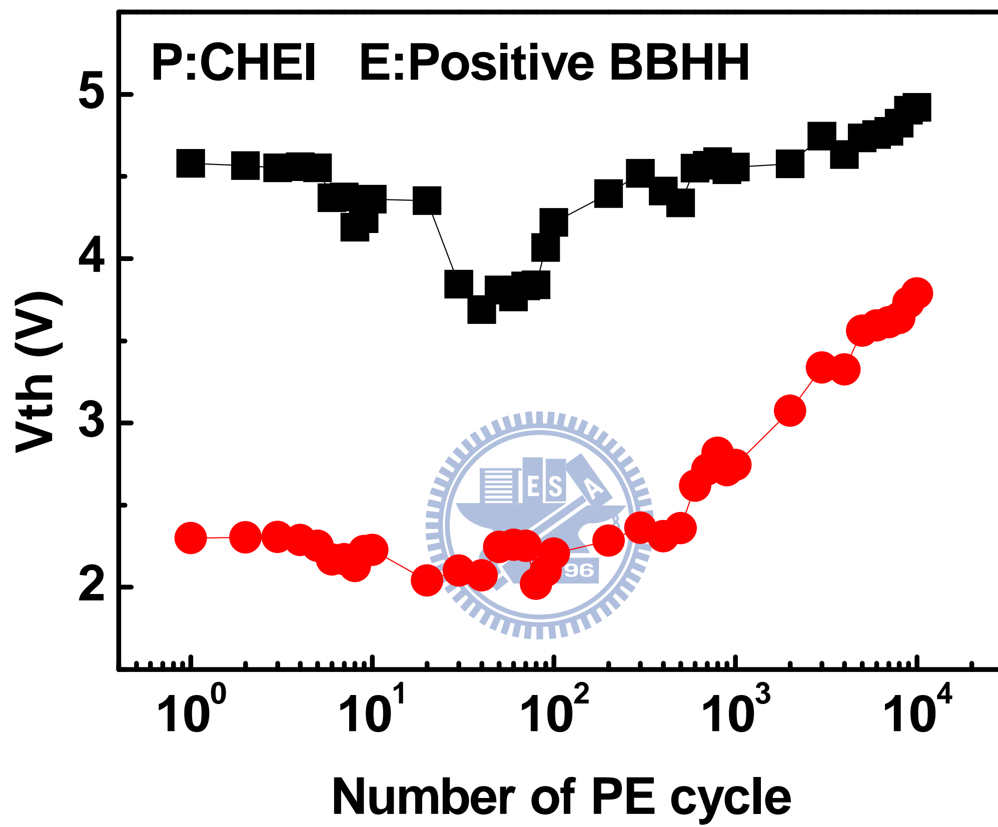
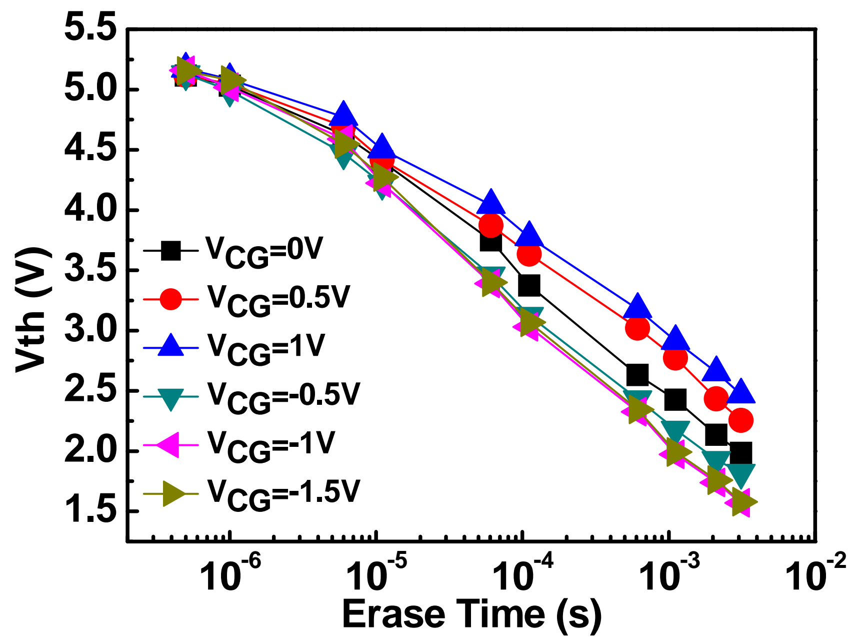
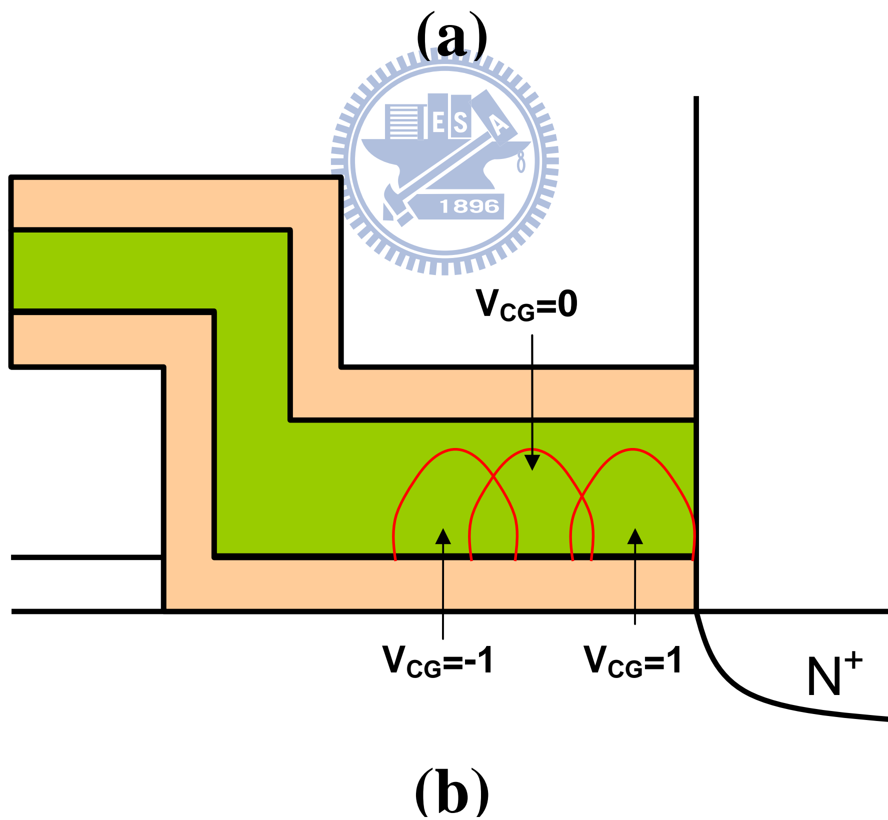


Fig. 5.8 Endurance for split-gate SONOS using positive BBHH erasing.



(a)



(b)

Fig. 5.9 The erasing transient with different control-gate voltage (a), and the schematic diagram for the misalignment with different control-gate voltage (b).

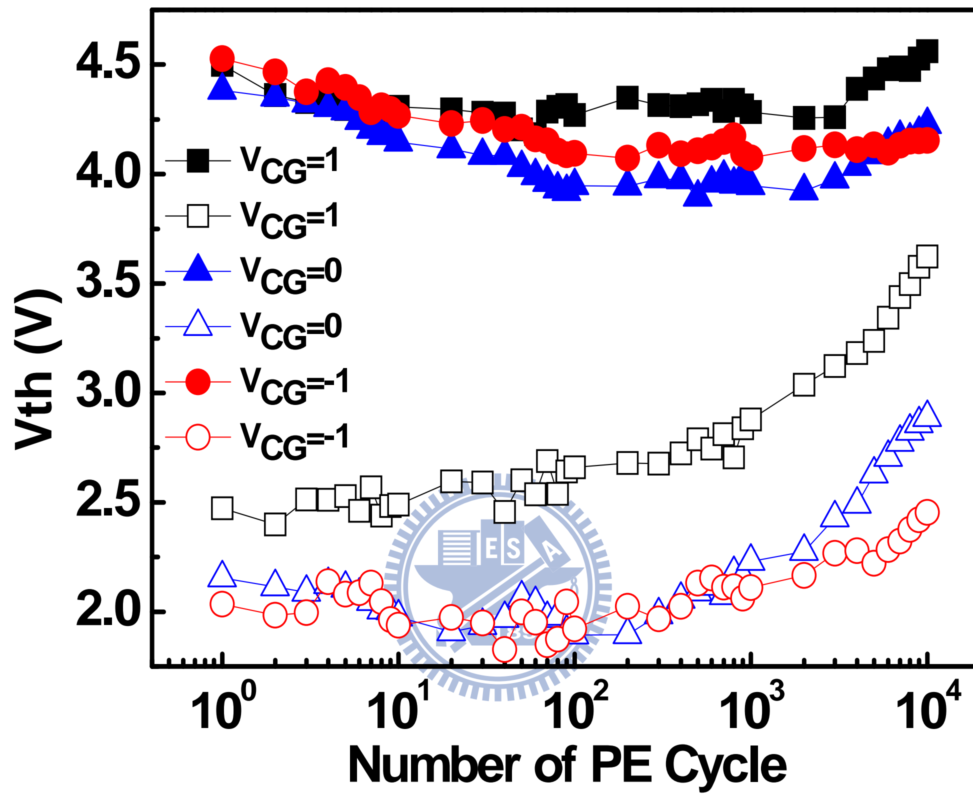


Fig. 5.10 Endurance for split-gate SONOS with different control-gate voltages during erasing.

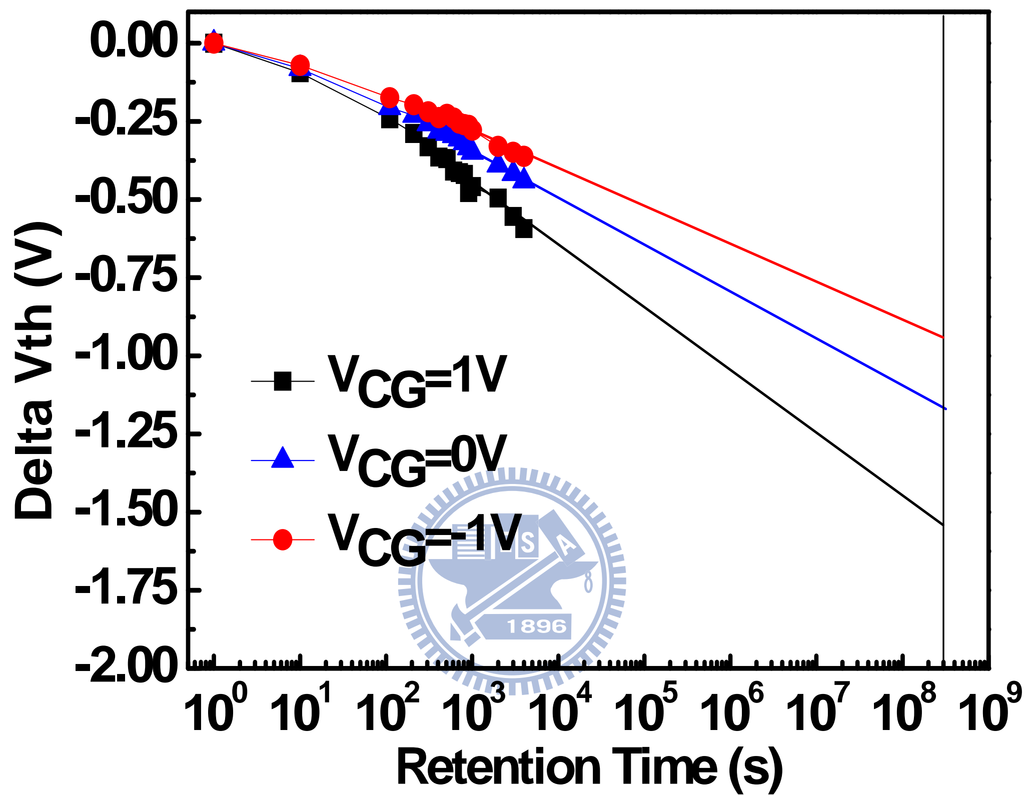
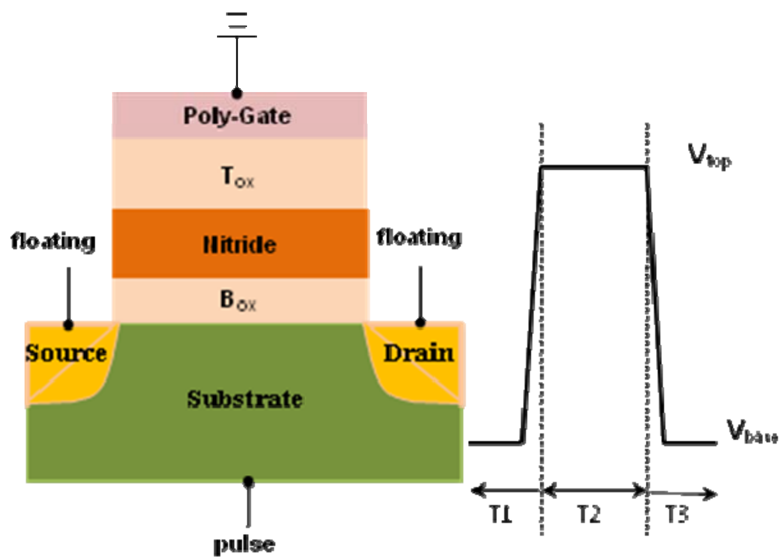
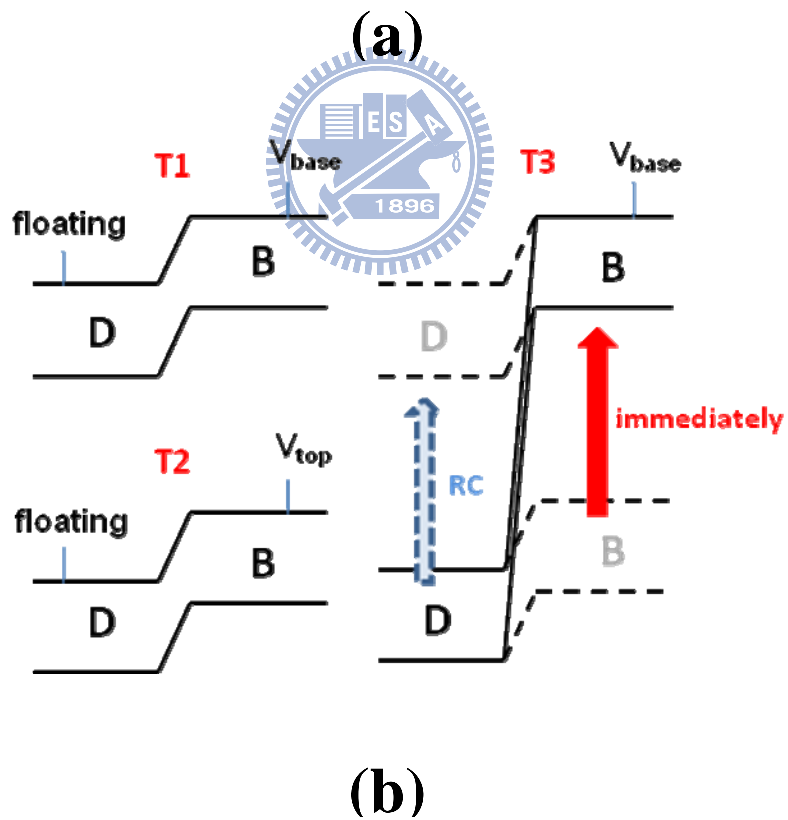


Fig. 5.11 Retention loss for split-gate SONOS with different control-gate voltages during erasing at 85C.

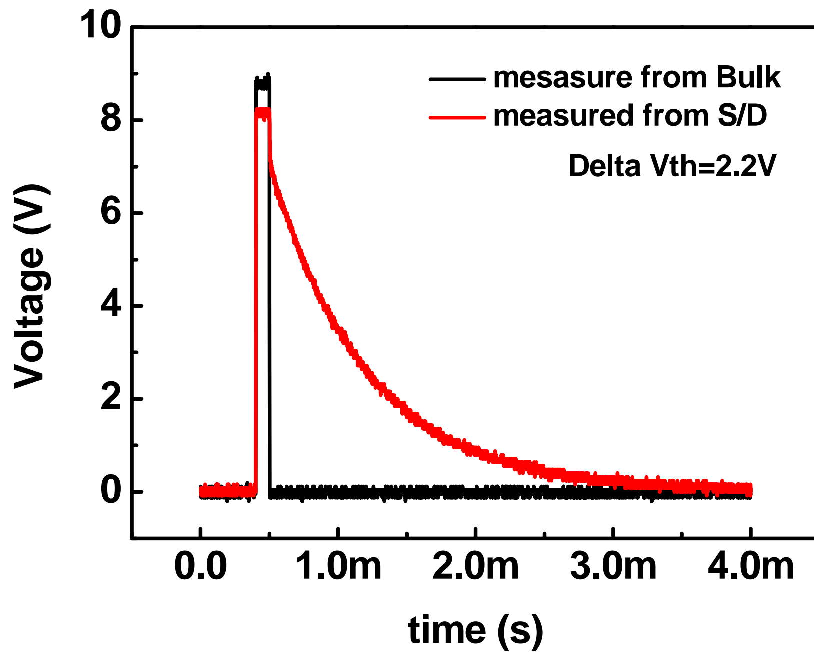


(a)

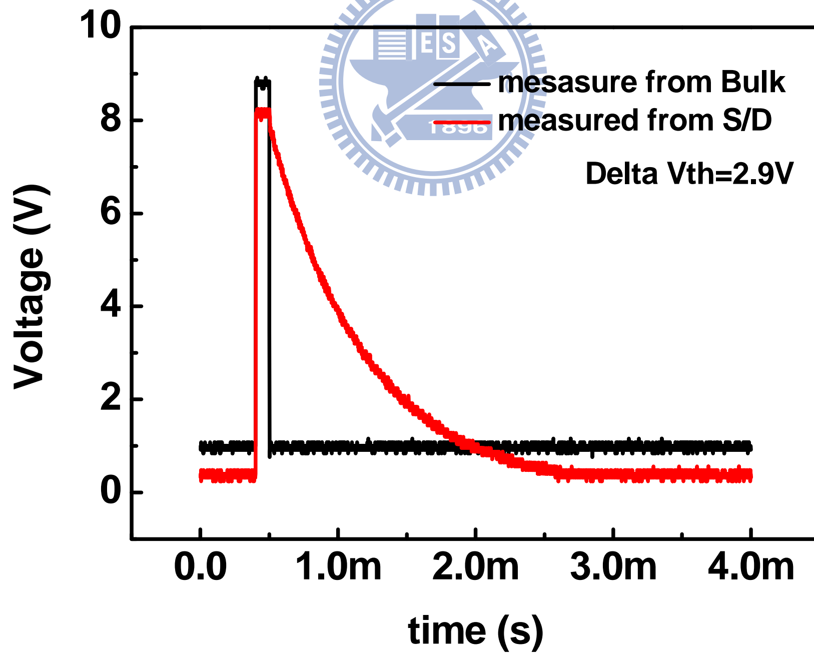


(b)

Fig. 5.12 Experiment set up and timing diagram for STHH erasing, and its band diagram transient during erasing.



(a)



(b)

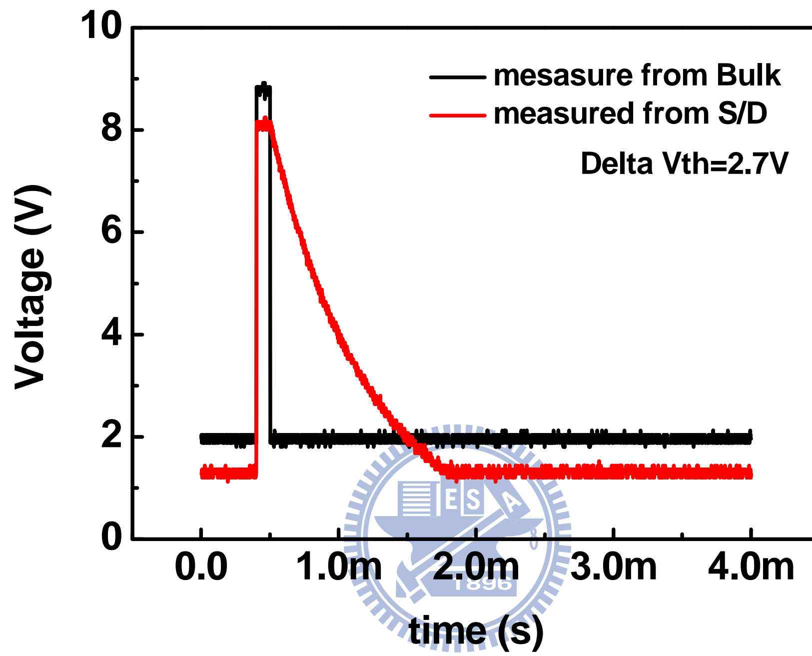
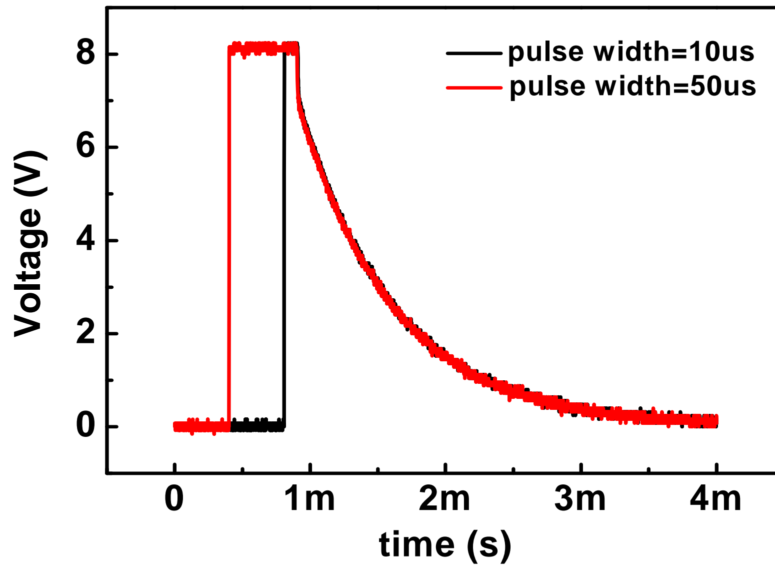
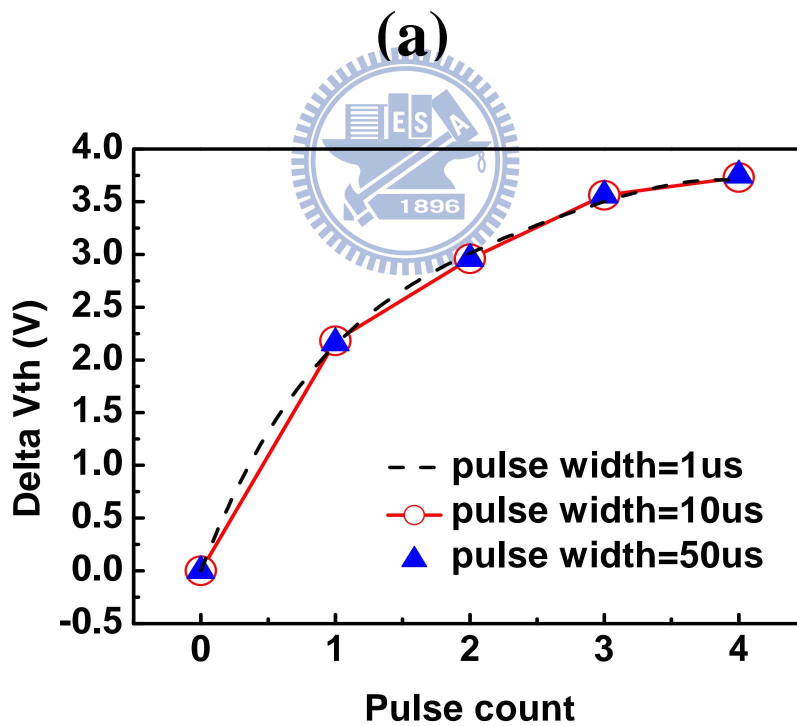


Fig. 5.13 The oscilloscope trace of the amplitude of the voltage tested from drain (red) and substrate (black) for the case of V_{base} =0V (a) V_{base} =1V (b) V_{base} =2V (c) with the same V_{top}=9V.



(a)



(b)

Fig. 5.14 The oscilloscope trace of the amplitude of the voltage tested from drain with pulse width of 50us (red) and 10us (black) (a), and the erasing window versus different pulse counts and widths (b).

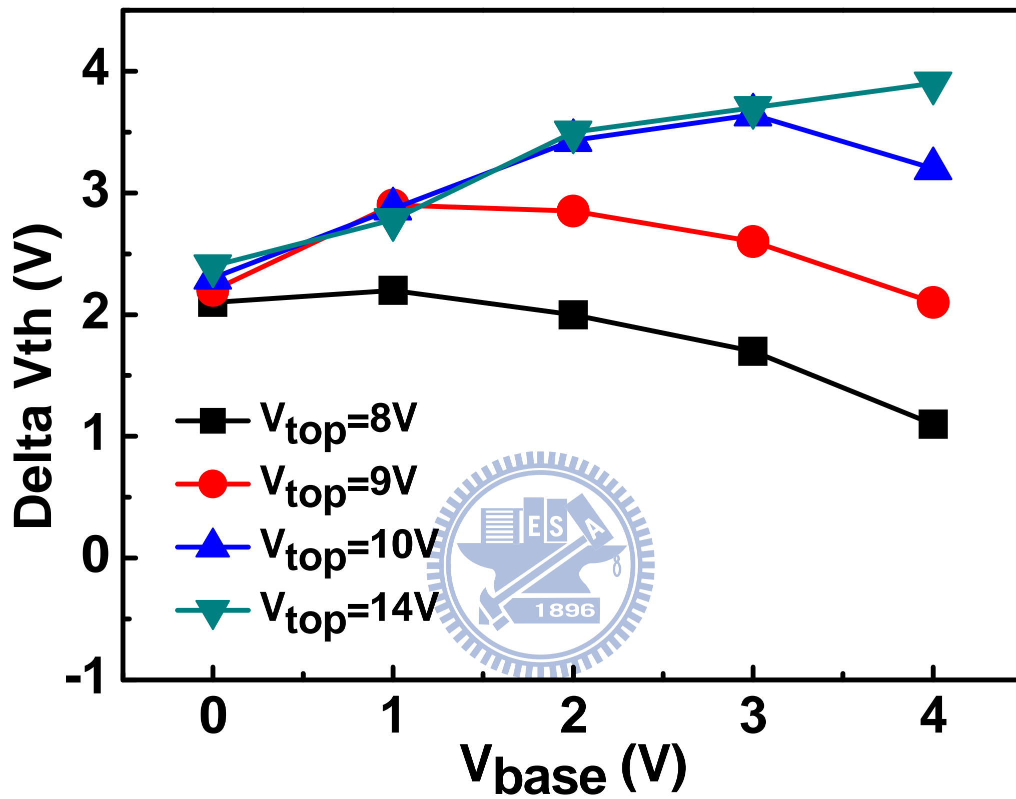


Fig. 5.15 The threshold voltage shift with varying V_{base} and V_{top}.

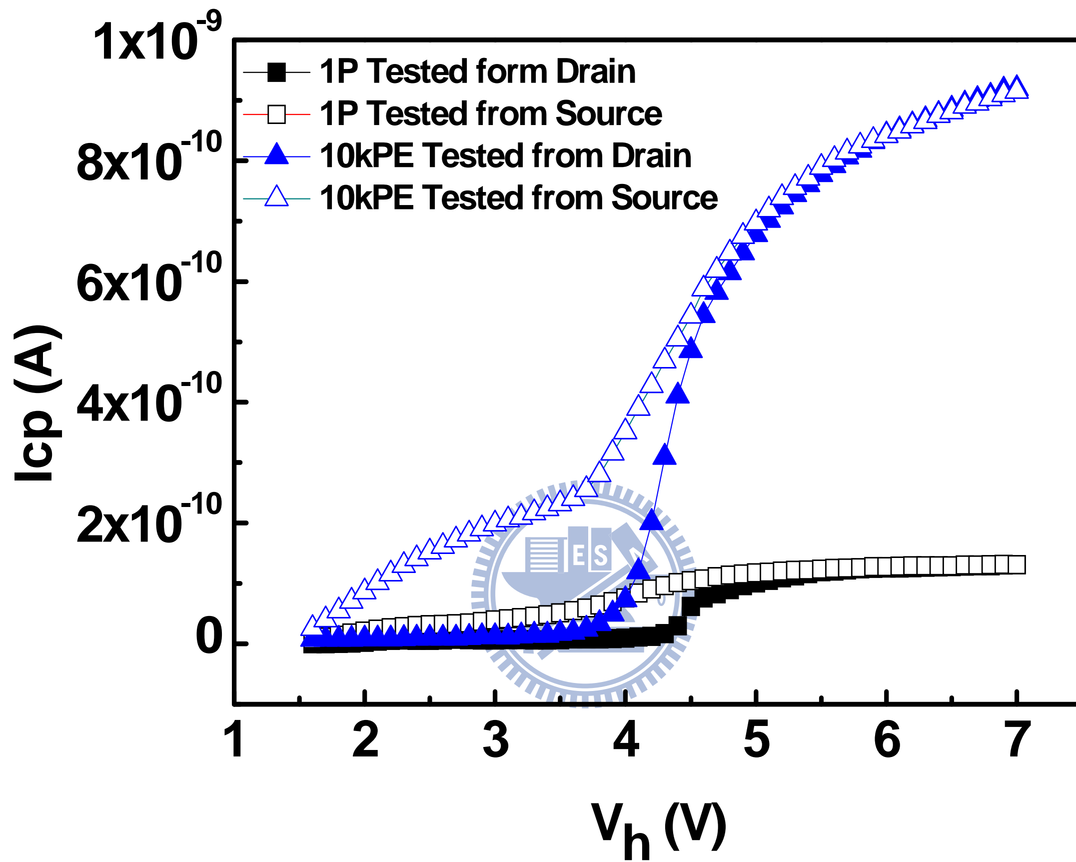


Fig. 5.16 The charge pumping current versus V_h of fresh cell (black) and 10k cycled cell (b) for conventional SONOS using STHH erasing scheme.

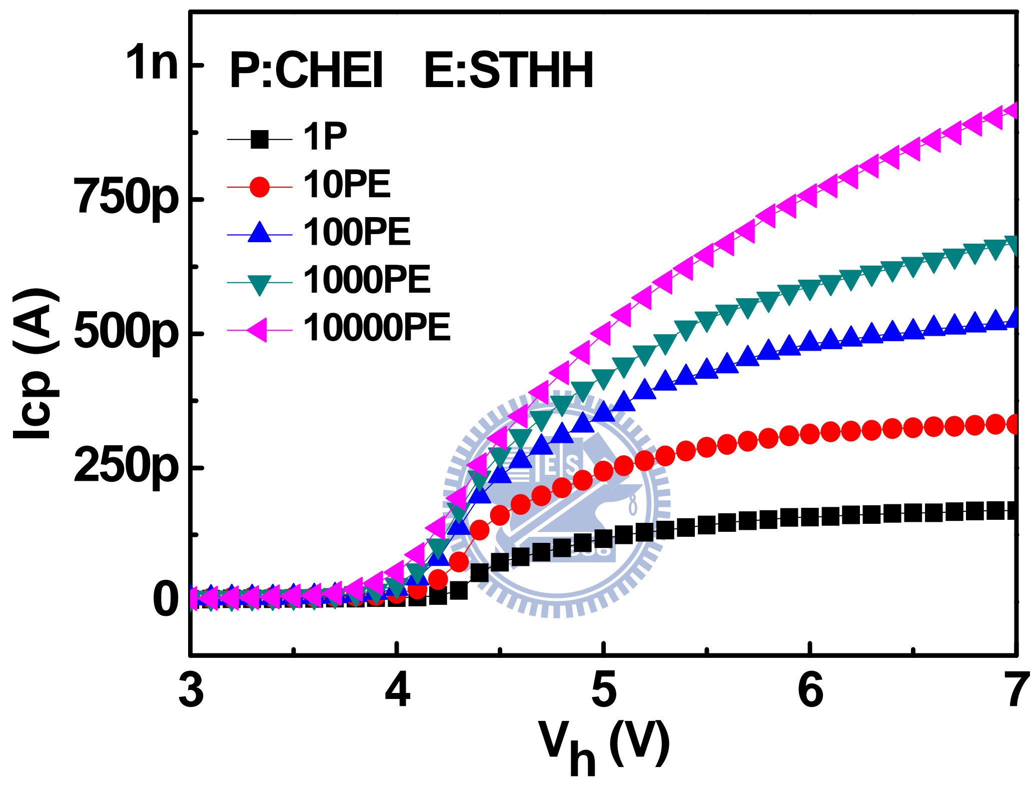


Fig. 5.17 The charge pumping current versus V_h of a programmed cell after different numbers of P/E cycles for conventional SONOS using STHH erasing scheme.

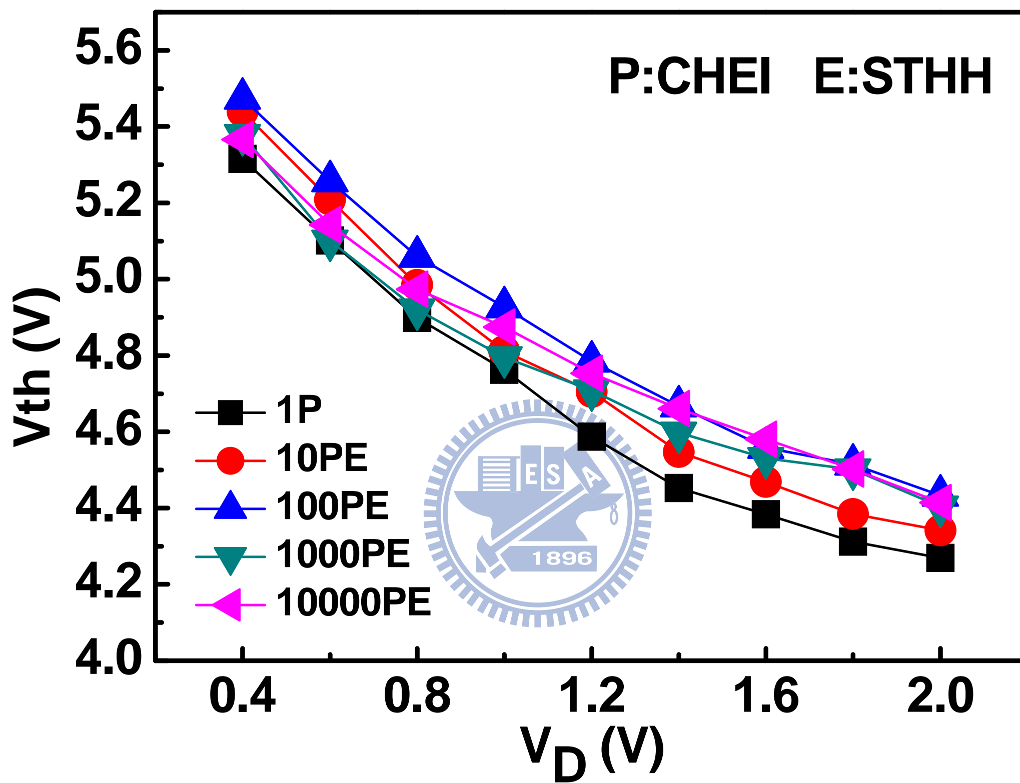


Fig. 5.18 Forward read threshold voltage for various drain voltages for conventional SONOS using STHH erasing scheme.

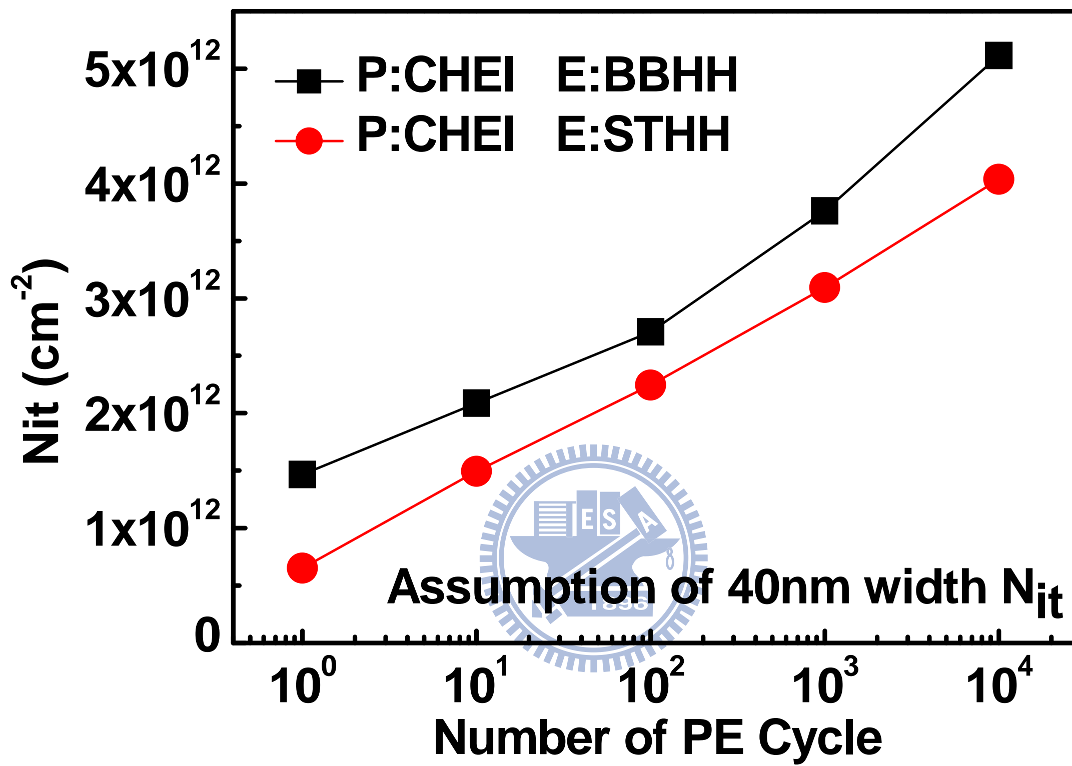


Fig. 5.19 Evolution of Dit with the number of P/E cycles endured by the device by using BBHH erase (black) and STHH (red).

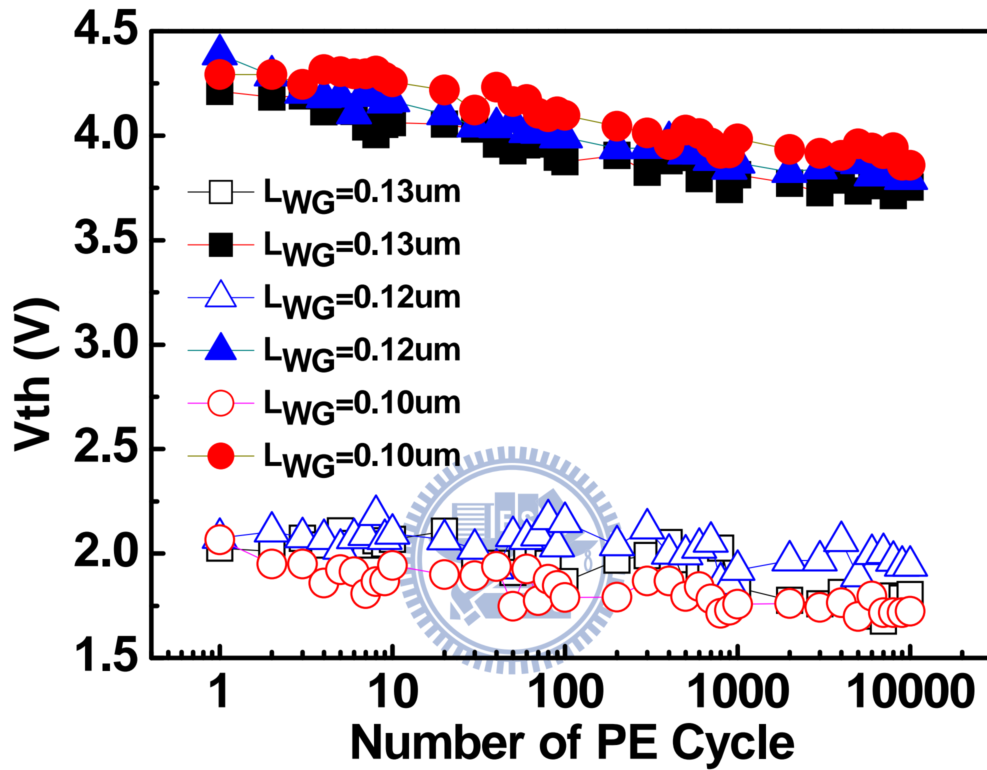


Fig. 5.20 Endurance for split-gate SONOS with different word-gate lengths by using STHH erasing scheme.

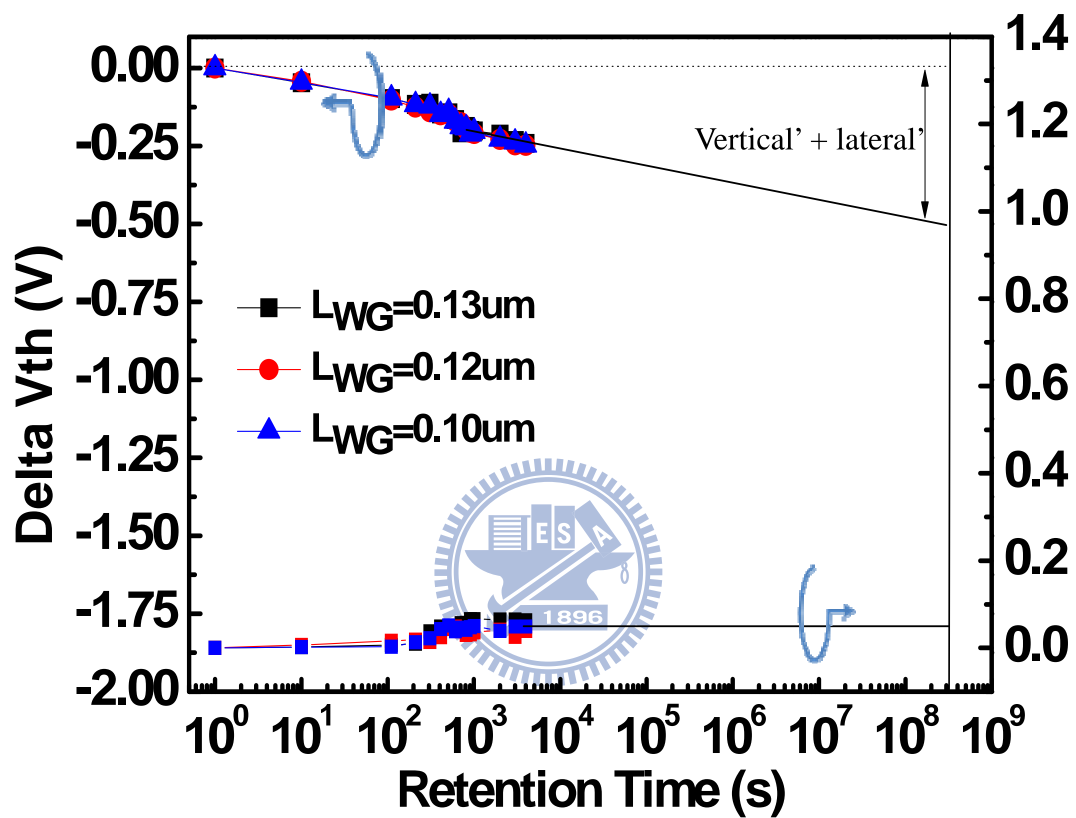


Fig. 5.21 Retention loss for split-gate SONOS with different word-gate lengths by using STHH erasing scheme at 85C.

Chapter 6

Summary and Conclusion

In this study, a very promising solution for near future flash memory has been proposed. The dual-bit split-gate SONOS allows high density thanks to dual-bit or multi-level/cell storage, and is easily scalable with the bit areas which are physically isolated. The performances are comparable to NROM, but with much lower power consumption because of the use of a more efficient programming mechanism. Most important of all, the split-gate SONOS can improve the misalignment between distributions by adjusting the word-gate length or the control-gate bias condition.

Retention loss mechanism for split-gate SONOS includes both vertical and lateral directions. The best way to improve the vertical retention loss is to make a better quality of bottom oxide, which has no relation to split-gate structure. However, the lateral retention loss is caused by the mismatch of distribution, which can be easily improved by adjusting the word-gate length or the control-gate bias condition of a split-gate structure.

Finally, the substrate transient hot hole erasing scheme is proposed to suppress the misalignment of distributions and improve the lateral retention loss. The charge retention loss mechanism can be said that the vertical retention loss should dominate the total loss, however, under a large misalignment situation, the lateral retention loss will give a non-negligible loss for nitride-based localized trapping memory cell.

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