國立交通大學

電子工程學系 電子研究所

博 士 論 文

具有高介電係數閘極介電層之薄膜電晶體製作及特性研究

Fabrication and Characterization of Thin-Film Transistors With High-κ Gate Dielectrics

研 究 生：鄧 至 剛

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摘 要

在本論文中提出整合高介電係數閘極介電層製程，來改善低溫複晶矽薄膜電晶體以及有機五環素薄膜電晶體的特性。首先提出具有高介電係數氧化鐠閘極介電層的低溫固相再結晶複晶矽薄膜電晶體，並且在施行固相再結晶退火前，對非晶化矽薄膜進行氮離子植入。結果顯示，在一定濃度的氮離子植入非晶化矽情況下，能夠在固相再結晶的退火過程中，修補晶粒邊界的缺陷態位，進而大幅改善低溫複晶矽薄膜電晶體元件的電性，而且此氮離子修補技術亦可在低溫複晶矽薄膜裡形成較強的矽-氮鍵結，來取代一般較弱的矽-矽鍵結和矽-氫鍵結，來增進元件對熱載子效應的免疫力。另一方面，使用具有高介電係數的氧化鐠閘極介電層，能夠在相同的等效氧化層厚度下，得到較大的閘極電容密度，加強電晶體閘極的控制能力，使複晶矽通道區產生更多的少數載子，迅速填滿補晶粒邊界的缺陷態位，以致於能大幅地改善薄膜電晶體的臨界電壓、次臨界斜率等電性。第二部分，對於有機五環素薄膜電晶體，我們也整合具有高介電係數的氧化鑭釔閘極介電層，預期得到良好的電性結果。結果顯示，高介電係數的氧化鑭釔的閘極介電層，具有高的閘極電容密度和低的閘極漏電流，能夠讓有機薄膜電晶體的五環素通道，在飽和累積工作區間的操作下，成功誘導產生更多的累積載子，來大幅降低有機薄膜電晶體的操作電壓至兩伏特內。因此，整合高介電係數閘極介電層的薄膜電晶體，將會符合往後顯示器科技的發展趨勢，適合在高速元件或低電壓操作電路的應用。

Fabrication and Characterization of Thin-Film Transistors With High-κ Gate Dielectrics

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Abstract

In this thesis, we integrate high dielectric constant (high-κ) materials as gate dielectrics to improve the electrical performances of the low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) and the pentacene-based organic TFT (OTFT). First, we study the LTPS TFT with a high-κ praseodymium oxide (Pr_2O_3) gate dielectric and incorporating with nitrogen implantation before solid-phase crystallization (SPC) annealing. Nitrogen atoms with appropriate dosages of 5×10^{12} cm^{-2} implanted into amorphous silicon (α-Si) film could passivate the trap states in grain and in grain boundaries during SPC annealing and greatly improve electrical performances. This nitrogen modification could form the strong Si-N bonds in place of the weak Si-Si and Si-H bonds to enhance the immunity against hot-carrier stress. Besides, using Pr_2O_3 as a gate insulator could obtain a thin equivalent-oxide thickness (EOT) of 8 nm and a high gate capacitance density of 432 nF/cm^2 with well gate controllability, compared to conventional tetraethoxylsilane (TEOS) oxide. Because the poly-Si channel could induce more minority carriers to quickly fill up trap states in grain boundaries, the threshold voltage and the subthreshold swing of the LTPS TFT could be greatly improved by integrating high-κ gate dielectrics. Second, we also demonstrated the pentacene-based OTFT with a high-κ lanthanum-yttrium oxide ($LaYO_X$) gate dielectric to

achieve high-performance characteristics. The results show that the 30-nm $LaYO_X$ film as the gate insulator of the OTFT device exhibits a high capacitance density of approximate 410 nF/cm^2 and a low leakage current below 20 nA/cm^2 biased at –4 V. It could induce more accumulation charges in the pentacene channel layer to obtain good device performances, such as a low threshold voltage of 1.25 V, a low subthreshold swing of 265 mV/Dec., and a field-effect mobility of 0.22 $cm^2/V\text{-}s$, under the 2-V low-voltage operation. Therefore, these TFT devices with high-κ gate dielectrics integration are suitable for high-speed or low-voltage electronic applications in flat panel display (FDP) field in the near future.

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At last, I would show my deepest appreciation to my wonderful family. With their continuous love and support, my research work has a perfect ending, and it is dedicated to my beloved parents, Mr. Guang-Cyuan Deng and Mrs. Jin-Mei Huang.

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CHAPTER 1

INTRODUCTION

Over the past ten years, flat panel displays (FPDs) have became frequent features to provide any instantaneous information in our daily lives, for examples, mobile phones, personal digital assistants (PDAs), notebooks, desktop computer monitors, televisions (TVs) etc, as shown in Fig. 1-1. They replace traditionally heavy cathode ray tube (CRT) and develop toward thin short in portable device or large-scale display. Today, the business of the display industry and its derivative marketing are significantly growing up and gradually catching up those of the semiconductor industry and the automobile industry. For high definition (HD), high quality, portable, power saving, and low-cost considerations, the fabrications of FPD technology must make new breakthroughs to satisfy human being's pursing. One of the breakthroughs is to improve the electrical performance of the thin-film transistor (TFT) device with a higher driving capability. A TFT device with a higher driving capability could use a smaller device dimension to drive liquid crystal (LC) in active matrix region, hence achieving a higher aperture ratio (AR) and a higher definition. Besides, it also could be directly embedded functional and control circuits by in-situ fabricated active-matrix TFT devices on peripheral panel without extra tap-automated-bounding (TAB) integrated-circuit (IC) to reduce the cost of the backend process on FPD.

Table 1-1 shows the roadmap proposed by Nakajima of Sony Corporation for integrating the circuit system into FPD to realize system-on-glass (SOG) or system-on-panel (SOP) concept [1]. By using the index of low-temperature polycrystalline silicon (LTPS) technology, the mobility is enhanced from 50 cm^2/V-s to 200 cm^2/V-s, the design rule of the channel length is shrunk from 3.5 μm to 1 μm, and the threshold voltage is decreased from 2 V to 0.5 V. Because of the improvement of TFT device performance, many kinds of integrated circuit

function on panel could migrate from analog driving circuits in 1st generation, digital-to-analog converter (DAC) circuits in 2nd generation, interface signal control circuits in 3rd generation, and finally to central processing unit (CPU) and memory circuits in 4th generation. In the near future, the FPD is not only for displaying information but also for increasing added value of digital and mobile products with high performance. Although these prototypes have been announced by lots of international FPD companies, they still need a period of time appearing in production line. Hence, how to improve electrical performance of a unit TFT device has became a research emphasis.

Although pursing high performance of LTPS TFT device drives new technologies in FPD field, not all electronics require such high performance devices. Some devices, however, such as electrical papers or electrical clothes, only have to cover large area without high resolution consideration, and they should be produced with extremely low-cost or disposable, as shown in Fig. 1-2. Hence, relatively cheap organic materials are more applicable to flexible surfaces rather than to rigid materials as traditional TFT displays. These special applications, such as large area coverage, mechanical robustness, flexible, lightweight, low-power consumption, and low-temperature production, are taken into account rather than intrinsic performance. Besides, an organic TFT (OTFT) device is usually used as a switching device to drive organic light-emitting diode (OLED) on panel [2], which is an active component emitting light unlike passive component of liquid crystal (LC). Unfortunately, today organic displays have a sluggish response time to limit display ability due to a low saturation carrier mobility of 0.1 to 1 cm^2/V-s for OTFT. To provide a sufficient driving capacity of OTFT, the large-area device layout must be drawn with sacrificing aspect ratio or the OTFT is operated under higher voltage with power consumption. Therefore, improving performance of OTFT must be also an important topic on an active-matrix organic light-emitting diode (AM-OLED) display [3].

Both LTPS TFT and OTFT devices are all need to improve their performance. Fig. 1-3

summarizes various ways to improve the performance of TFT device, where takes an n-type LTPS TFT for example. On purpose to decrease grain boundary trap states in polycrystalline silicon (poly-Si) film, the solid-phase crystallization (SPC) method and the excimer laser annealing (ELA) technology [4] are developed to re-crystallize from an α-Si film to enlarge grain size. In recently years, to further improve the characteristics of poly-Si similar to those of single crystalline silicon, the sequential lateral solidification excimer laser annealing (SLS) [5] and the selectively enlarging laser crystallization (SELAX) [6] are proposed to realize on display products. However, the grain boundaries still exist in the active channel of TFT even if the grain size of poly-Si has been enlarged by a re-crystallization technology. To passivate these trap states in grain boundaries, the hydrogen plasma [7] and the ammonia plasma [8] treatments are processed during inter-metal dielectric depositing in today FPD industry. The grain boundaries also have opportunity to appear near the drain side junction of LTPS TFT. To avoid the kink effect [9] and the gate induce drain leakage (GIDL) current [10], the LTPS TFT device with a lightly-doped-drain (LDD) structure [11] is often used to solve the electrical stability in industry. In academic, many device structures to lower the electric field near drain side are also reported to improve the electrical stability [12]. With the increase of panel size, the parasitic resistance and the parasitic capacitor must be considered to maintain the speed of signal transportation. Therefore, the copper gates for interconnection [13] as well as the low-κ materials for inter-metal dielectric [14] have been studied and introduced into large-size panel production.

As previous mentioned on the index of SOP technology, the circuit on panel is designed toward power-saving applications, which means the operational voltage should be continuously lowered with the same driving current of LTPS TFT. Especially on the irregular number of grain boundaries in poly-Si channel, although using LTPS process could enlarge poly-grain size to improve the device performance, it usually accompanies a random device-to-device variation, which is not suitable for circuit design [15]. Therefore, except for

improving the device performance, the gate controllability to active channel of LTPS TFT seems more important. In ref. [16], integrating high-κ gate dielectric into LTPS TFT could increase gate capacitance density and obtain a thin equivalent-oxide thickness (EOT) with good gate controllability. Compared to LTPS TFT with an oxide gate insulator, that with a high-κ gate dielectric could induce more minority carriers to quickly fill up the grain boundary trap states in active channel region. Therefore, LTPS TFT with a high-κ gate insulator has larger on/off current ratio, lower subthreshold swing, and lower threshold voltage. Furthermore, as the channel length scales down, the fluctuation of threshold voltage caused by the variation on the number of grain boundaries and the threshold voltage roll-off property corresponding to the short channel effect could be well controlled due to higher gate controllability to minimize the body effect in the channel region. Therefore, developing high-κ dielectric into LTPS TFTs is a mainstream technology in FPD field in the near future.

For an organic TFT (OTFT) device, the ways to improve performance are also summarized in Fig. 1-4. First, because the stability of OTFT is affected by environmental gas, the polymer passivation layers are proposed to spin coating on the active channel layer to improve the reliability of organic device [17], [18]. Besides, improving the contact between the electrodes and the active organic layer by minimizing their work-function mismatch could help majority carriers inject into the active channel to improve the device performance [19], [20]. Fig. 1-5 shows various organic materials with a higher carrier mobility compared with polycrystalline silicon are also developed. [21]. If the interface status between the inorganic oxide insulator and the organic channel layer is treated from hydrophilic to hydrophobic by interface modification [22]-[24], the organic molecules would be grown and aligned with each other to enhance grain size corresponding to the raise of carrier mobility.

Finally, incorporating a suitable high-κ material to increase the gate capacitance density of OTFT could also improve device characteristics. The major motivation to find silicon oxide alternatives is significantly reducing the operational voltage of OTFT. In fact, while the

saturation carrier mobility of organic semiconductors have approached or surpassed that of amorphous silicon (α-Si), OTFT generally is operated under a very large source-drain or source-gate bias, typically greater than 30 V to 50 V [25]. It results in excessive power consumption, which is not suitable for organic electronic circuits. Therefore, using high-κ materials as gate dielectrics could induce more accumulation charges in the active channel layer of OTFT under the same electric field (gate and drain voltages) corresponding to the improvement of the channel mobility, compared with using low-κ silicon dioxide.

In this thesis, we propose integrating high-κ materials as gate dielectrics to improve the electrical performance of low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) and pentacene-based organic TFTs (OTFTs), and we hope both of them are suitable for high-speed or low-voltage electronic applications. This thesis organizes as following. Chapter 1 presents the introduction of FPDs concept and the motivation why we need to integrate high-κ gate dielectrics for thin-film transistor (TFT), including LTPS TFT and organic TFT (OTFT). Chapter 2 gives the general backgrounds on active-matrix liquid crystal display (AMLCD), history of TFT, organic semiconductor materials, and solid-phase crystallization technology. All of this knowledge would be used for discussion in chapter 4. The high-κ dielectric materials could be used in complementary-metal-oxide-semiconductor (CMOS) devices and TFT devices are also reviewed. Besides, the current equations of LTPS TFT and OTFT are derived. Chapter 3 shows the detail fabrication processes of LTPS TFTs and OTFTs with high-κ gate insulators, and the physical analysis techniques as well as the electrical measurement methods used to characterize device performances are included. Chapter 4 devotes into two main categories, which contain the characteristics of the LTPS praseodymium oxide (Pr_2O_3) TFTs with various nitrogen dosages and those of the OTFT with lanthanum-yttrium oxide ($LaYO_X$). Their electrical performances are investigated to verify the benefits on integrating high-κ gate dielectrics. Finally, chapter 5 concludes this research work and gives the suggestions for future work.

Fig. 1-1. The applications of flat panel displays (FPDs) in our daily lives.

Table 1-1. The roadmap of system integration trend of FPD provided by Sony Corporation [1].

Time	Before 2000	2000–2002	2003–2005	After 2005
Generation	1st	2nd	3rd	4th
System integration	V driver & analog sample hold	4 bit DAC 6 bit selector low current DCDC converter	Completely integrated RGB interface high current power circuit leading to single power supply	Multibit frame memory high speed interface sensor signal processor
Interface	Analog (Special format)	Digital (Special format)	Digital (Standard 18 bit RGB parallel)	Digital (CPU or RGB Serial)
Application	Digital video camera Digital still camera	PDA Mobile phone	PDA Mobile Phone	Advanced mobile terminal
Mobility	50 $cm^2/V\,s$	50 $cm^2/V\,s$	100 $cm^2/V\,s$	200 $cm^2/V\,s$
V_{th}	2 V	2 V	1 V	0.5 V
Design rule	3.5 μm	3.5 μm	2.0–3.0 μm	1.0 μm

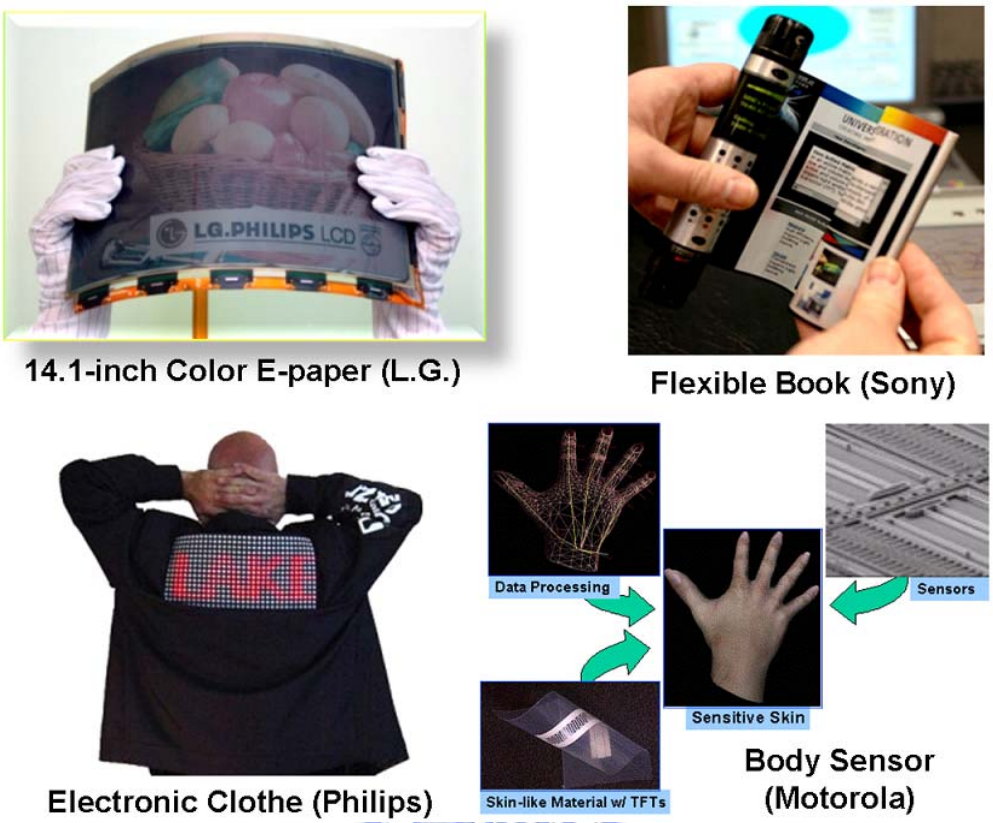


Fig. 1-2. The applications of organic thin-film transistor (OTFT) on flexible electronics.

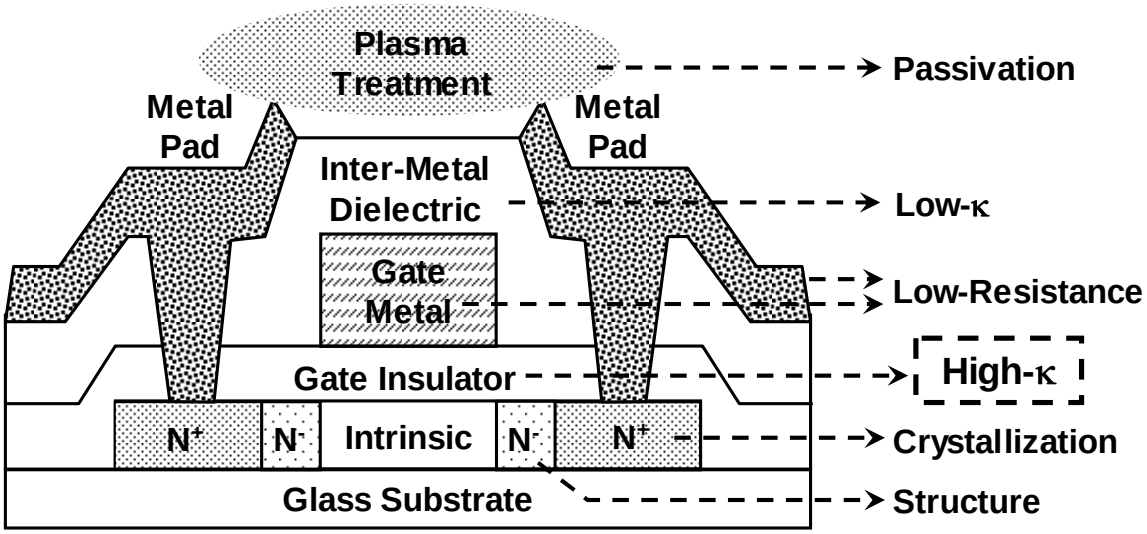


Fig. 1-3. The methods to improve characteristics of low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT).

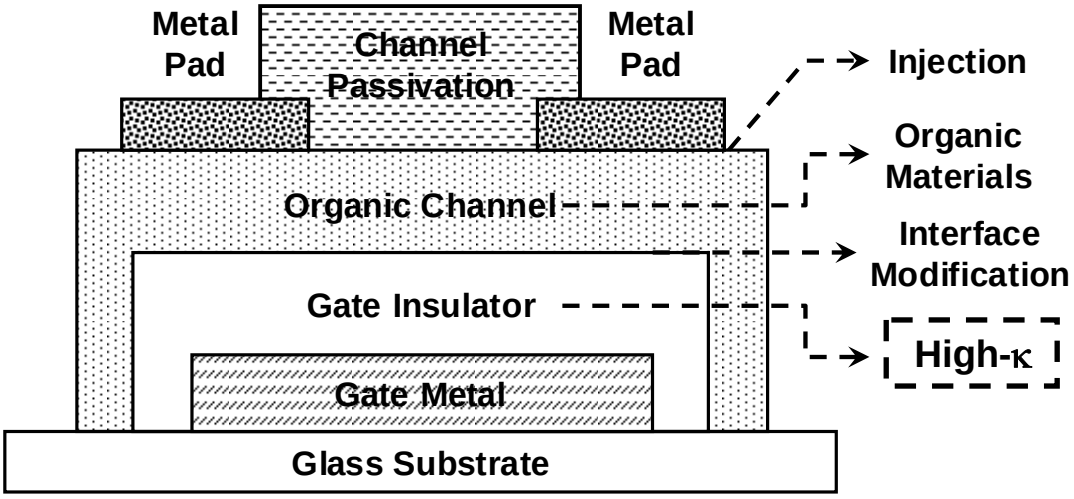


Fig. 1-4. The methods to improve characteristics of organic thin-film transistor (OTFT).

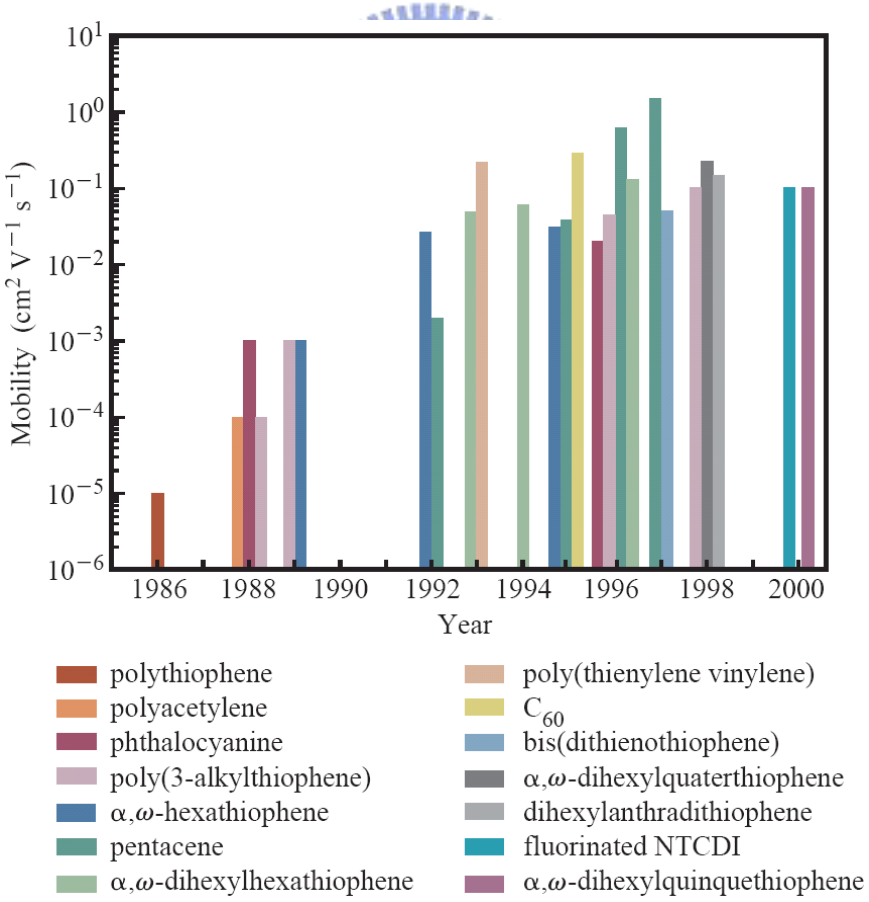


Fig. 1-5. Organic materials used as active channel layers for organic thin-film transistors (OTFTs) [21].

CHAPTER 2

GENERAL BACKGROUND AND LITERATURES REVIEW

In this chapter, we first give a brief introduction on the active-matrix liquid crystal display (AMLCD) where the thin-film transistors (TFTs) as the switching devices or the controlled devices are fabricated. Second, a history for manufacturing TFT devices is described from the first TFT device to the low-temperature polycrystalline silicon (LTPS) TFT and the organic TFT (OTFT). The section 2.3 presents a review on some kinds of organic semiconductor materials used for OTFT and their conduction mechanisms. In the subsequent section 2.4, the principle of solid-phase crystallization (SPC) method as well as several modified SPC methods to improve device performance are described and explained here. Section 2.5 gives a brief comparison of various high-κ materials, especially on the properties of the lanthanum series materials, such as praseodymium oxide (Pr_2O_3) and lanthanum-yttrium oxide ($LaYO_X$). Moreover, the advantages for incorporating these high-κ dielectrics in TFTs and in OTFTs are also illustrated in this section. And then, the retrospective reviews on LTPS TFT and OTFT with high-κ gate dielectrics are shown in section 2.6. Finally, the current equations of these TFT devices used in the following chapters are derived in section 2.7.

2.1 ACTIVE-MATRIX LIQUID CRYSTAL DISPLAY TECHNOLOGY

Thin-film transistors (TFTs) are commonly utilized as pixel-switching elements in active-matrix liquid crystal display (AMLCD). Fig. 2-1 shows the cross-sectional view of the unit pixel in an AMLCD [26]. Basically, the unit pixel in AMLCD consists of three main parts, a thin-film transistor (TFT), a liquid crystal (LC), and two polarizers on outer top and bottom

glasses. The liquid crystal (LC), a group of rod-shaped polymer molecules, is confined between two glass plates separated by a spacer, and it would be forced by the orientation alignment layers either into 90° or 270°. The outer surfaces of two glass plates are coated with linear polarizers whose polar orientations are mutually perpendicular. When the unpolarized light travels through this AMLCD system, it is linearly polarized by the first polarizer, and subsequently the polarization plane of light could be rotated by the twisted LC molecules. This rotation enables the light to pass the second polarizer, which is perpendicular to the first polarizer. Hence, the AMLCD system is transparent in non-activated state. Besides, the inner surface of glass substrate contains patterned pixel electrodes made by a transparent conductor of indium-tin oxide (ITO). When an output voltage of switching TFT device is applied on the pixel electrode, the LC molecules would be aligned parallel to the electric field and perpendicular to the surface of the glass substrate. Therefore, the light polarization is not rotated anymore, and the crossed-polarization filters would result in blocking light, appeared to black in this unit pixel. Grey levels could be obtained with the partial alignment of liquid crystal (LC) molecules by applying various voltage levels on the pixel electrode. The red, green, and blue color filters are implemented on the front glass for individual pixels of full-color display.

The first matrix concept on liquid crystal display (LCD) was proposed by *Lechner et al*. [27] in 1971. This equivalent circuitry of active matrix concept is drawn in Fig. 2-2. Each crossing region surrounded by row line and column line is located a thin-film transistor (TFT) and a pixel capacitor (C_p). The pixel capacitor represents both the capacitances of liquid crystal and additional storage capacitor. The data driver and the scan driver, the peripheral circuitry generally fabricated by complementary-metal-oxide-semiconductor (CMOS) process, control the gate voltage and the drain voltage of each thin-film transistor, respectively. The scan driver controls the gate addressing, and its alternate sweeping depends on how much frame rate we need. The data driver inputs the information of video signals by various voltage

levels stored on the pixel capacitor (C_p). Various amounts of charges in the pixel capacitor related to the polarization of liquid crystal (LC) result in the various grey levels we see on the active-matrix liquid crystal display (AMLCD).

2.2 HISTORY OF THIN-FILM TRANSISTORS

The first n-type thin-film transistor (TFT) was fabricated by P. K. Weimer at RCA laboratory in 1962 [28]. He used the thin film of microcrystalline cadmium sulfide (CdS), the insulator of silicon monoxide, and the electrodes of autumn (Au) to form CdS TFT with a top-gate staggered structure on glass substrate, as shown in Fig. 2-3. All of these materials in this device were deposited by utilizing electron-beam evaporation through shadow masks. In 1964, P. K. Weimer also reported a p-type TFT with a tellurium (Te) active channel with the same structure [29]. Although the active channel of polycrystalline CdS or Te has a high mobility characteristic, the other electrical properties are influenced by grain size, stoichiometry, high interface states, and even sensitive to ambient gas. Therefore, in 1979, *LeComber et al*., first introduced the radio-frequency (RF) sputtered amorphous silicon (α-Si) as the active channel material of TFT device [30], as shown in Fig. 2-4. With the process progressing, in 1986, *Funada et al*., of Sharp fabricated the TFT with a tri-layer inverted-staggered structure contained a back-channel insulating layer, an etch-stopper layer, an active layer, and a source/drain contact layer which those layers are all deposited by a plasma-enhanced chemical vapor deposition (PECVD) system [31]. With this tri-layer inverted-staggered structure, it is easy not only to make the good contact with the back-channel approach but also to control the OFF-state current with the shading-light bottom-gate electrode. It becomes the standard structure of amorphous silicon (α-Si) TFT in modern active-matrix liquid crystal display (AMLCD) technology [32], as shown in Fig. 2-5. In following years, based on α-Si technology, many kinds of electronic products equipped

with AMLCD panels are commercialized, such as LCD monitors, notebooks, and the state of the art: super large size TFT-LCD TV of 108 inches fabricated by Sharp with its 7-th generation production line in 2007.

Because the mobility of amorphous silicon (α-Si) TFT was too low with an approximate value of 0.2 to 1 cm^2/V-s, in 1980, *Funada et al*., of IBM reported the first high-temperature polycrystalline silicon (poly-Si) TFT with a high mobility of 50 cm^2/V-s fabricated on quartz substrate [33], but it could not be fabricated on glass substrates due to the temperature limitation. Afterwards, many researches [34], [35] focused on how to use a low-temperature process to fabricate top-gate poly-Si TFTs on glass substrate, as shown in Fig. 2-6. In 1991, *Little et al*., of Seiko-Epson first developed a low-temperature polycrystalline silicon (LTPS) TFT on glass substrate by using solid-phase crystallization at 600 °C, whose mobility was close to that on quartz substrate [36]. Further, various crystallization technologies were developed to improve the device performance, for examples, metal induced crystallization [37], [38] and laser crystallization [39], [40]. With these advanced crystallization technologies, the LTPS TFT device with a high mobility was not only used as the switching element with a larger aspect ratio (AR) in unit pixel, but also made as the device in periphery driving circuit and in control circuit around the panel, as shown in Fig. 2-2. Currently, by combining the laser crystallization technology, the LTPS TFTs have been used in small-to-mid size panel products, such as digital camera or cellular phone, for high delicate pixel, high definition, and portable and low-power electronics applications.

In previous section, pursing high performance of TFT device drives new technologies used in FPD field. However, not all electronics require high performance. Some devices, for examples, detectors, electrical papers, or electrical clothes, only have to cover large area, no need to high definition, and must be produced with extremely low cost or disposable. Some devices have to integrate with personal information on a plastic substrate, such as smart cards or identification tags. For these special applications, large area coverage, mechanical

robustness, and cheap and low-temperature production, are the most important consideration rather than intrinsic performance. Therefore, the cheaper organic semiconductors with similar mobility to the amorphous silicon (α-Si) have been attracted much attention recently.

Various organic semiconductors have been studied since the early 1950s [41], but their characteristics were poor and low reproducible. The electrical conduction of the polymer-based polyacetylene was first reported by *Chiang et al*. in 1977 [42]. A few years later, *Ebisawa et al.*, fabricated the first polymer-based transistor with a polyacetylene (CHx) channel in 1983 [43]. Owing to the thermal and mechanical fragility of the organic materials, the inverted-staggered structure and the inverted coplanar structure are most frequently used structures in the organic-based TFTs field, as shown in Figs. 2-7(a) and 2-7(b), respectively [44]. Nowadays, all organic semiconductors are conjugated organic materials with single and double carbon bonds alternated along whole molecule backbone. Based on the molecular weight, the organic semiconductors roughly have two classifications as (1) conjugated polymers and (2) small molecules or short conjugated oligomers [45]. Among these organic semiconductors, the oligomers pentacene ($C_{22}H_{14}$) has the highest mobility. Recently, the saturation mobility of the pentacene-based thin-film transistor with a 400-nm thermal gate oxide on heavily doped silicon substrate was progressive to 1 cm^2/V-s [46], [47], whose characteristics are shown in Fig. 2-8. However, such device needs high operational voltage so that it could not be used for low-power circuit applications.

2.3 ORGANIC SEMICONDUCTOR MATERIALS

In conjugated organic materials, single and double bonds alternate along whole molecule backbone. It means that all π orbitals of the carbon atoms participates to either a double bond or a single bond from a sort of continuous π bond delocalized along the whole molecule. The hybridization of the π orbital results in splitting of the energy levels and forming a sort of the

Highest-Occupied-Molecular-Orbit (HOMO) analogous to the valence band of conventional inorganic semiconductor. Besides, the anti-bonging π* orbitals, with their higher energy, constitute the Lowest-Unoccupied-Molecular-Orbit (LUMO) like the conduction band of inorganic semiconductor. The energy band diagrams of oligo-thiophenes and poly-thiophenes are also the function of the number of conjugated units [48], as shown in Fig. 2-9.

On the contrary, the transport from one molecule to another is much more difficult due to a small energetic coupling between molecules held by a weak Van der Waals force about 10 kcal/mol [49]. Generally, the inter-molecular transport could not be described with the conventional band theory, but it could be described as the phonon assisted carrier hopping between the localized states of organic molecules. Accordingly, unlike the case of the phonon scattering for conventional inorganic semiconductor [45], the mobility (μ_m) of these organic molecules increases with temperature following an exponential form as

$$\mu_m = \mu_{m,0} \exp\left[-\left(\frac{T_0}{T}\right)^{1/\alpha}\right] \tag{2-1}$$

, where α is an integer ranging from 1 to 4, T is temperature, and T_0 and $\mu_{m,0}$ are fitting constant. However, concerning the higher ordered organic materials, the explanation for inter-molecular conduction by hopping process may face some controversy [45].

Depending on the arrangement of molecules and the nature of majority charge carriers, organic semiconductors could be either p-type or n-type materials. Several commonly used organic and polymer semiconductor materials with reliable performance characteristics for thin-film device are shown in Fig. 2-10 [21]. Pentacene ($C_{22}H_{14}$) and regioregular poly(3-hexylthiophene) (P3HT) have been extensively researched and commonly used for p-type material in most organic TFT devices. However, n-type materials are also required for special applications, such as organic light emitting diodes (OLED) or organic-based complementary-metal-oxide-semiconductor (O-CMOS), including N,N'-bis(n-octyl)--dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2), and hexadecafluoro-

-phthalocyanine ($F_{16}CuPc$). In our study, pentacene, as a member of oligomers, consists of five aligned and condensed benzene rings is used to demonstrate our organic TFT with high-κ dielectric.

2.4 SOLID-PHASE CRYSTALLIZATION TECHNOLOGY

As-deposited polycrystalline silicon (poly-Si) film as an active channel layer generally exhibits small grain size resulting in inferior characteristics of low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT). In poly-Si film, most of defects in grain boundaries would act as scattering centers or midgap trap states to degrade carrier transport properties and to increase off-state leakage current in LTPS TFT [50]. Consequently, a low-cost solid-phase crystallization (SPC) process is developed to re-crystallize poly-Si film from amorphous silicon (α-Si) film and it could obtain larger grain size to minimize grain boundaries in active channel layer corresponding to the improvement of ploy-Si quality [51]. A small amount of scattering centers and trap states in active channel layer result in a higher carrier mobility in LTPS TFT. In our work, therefore, we use SPC method to demonstrate the LTPS high-κ TFT with various nitrogen dosages.

Given sufficient energy to overcome initial energy barrier, amorphous silicon (α-Si), a thermodynamically metastable phase, has a driving force to transform toward polycrystalline phase. After the α-Si film is deposited, the traditional SPC process spends several hours (> 20hrs) for completely converting the α-Si film to the poly-Si film at a low temperature of 600 °C. The grains are generally elliptical in shape due to preferential growth in <112> direction, and dendritic due to the formation of twin along (111) boundaries, as shown in Fig. 2-11 [52]. Besides, as the cross-sectional view of TEM in Fig. 2-12 [53], the traditional SPC process is an interface-nucleation scheme generating lots of nucleation sites at the amorphous silicon/underlayer (α-Si/SiO_2) interface as a function of annealing time. It also results in many

grain boundaries in re-crystallized poly-Si film, in spite of less than those in amorphous silicon (α-Si) film [54].

In order to improve the microstructure of poly-Si film, the modified solid-phase crystallization (SPC) methods with surface-nucleation scheme are proposed by introducing oxygen dopants at the amorphous silicon/buffer oxide layer (α-Si/SiO_2) interface to suppress grain nucleation starting at this interface [55], [56]. It initially nucleates at another preferable nucleation site on the top free surface of α-Si film to gain a larger grain size of poly-Si film. In order to further decrease the trap states in grain boundaries, the hydrogen plasma [7] or the ammonia plasma [8] passivation is treated after the LTPS TFT is finished. However, the hydrogenated poly-Si TFTs suffer from a serious instability issue due to the easily broken of weak Si-H bonds under electrical stress [57]. To find stronger and more stable bonds, such as S-F bond or Si-N bond, to replace the Si-H bonds in passivation process, the fluorine implantation [58], the carbon tetrafluoride (CF_4) plasma treatment [59], and the nitrous oxide (N_2O) plasma treatment [60] are processed on the active channel layer after the SPC process is completed. Furthermore, the low-temperature SPC activation with implanted fluorine ions is also proposed [61] to improve the electrical characteristics and the reliability of LTPS TFTs. According to these previous reports, we could conclude that the stronger bonds formed in the poly-Si film and at poly-Si/gate insulator could significantly improve performance and reliability of device. Therefore, in our study, we propose the LTPS TFT with nitrogen incorporation during SPC process to form the stronger Si-N bonds and to passivate the trap states in poly-Si grains and in grain boundaries. We expect such device has better electrical stress immunity.

2.5 THE PROPERTIES OF HIGH-κ MATERIALS

Today, searching potentially alternative high-κ materials as gate insulators has attracted much attention in complementary-metal-oxide-semiconductor (CMOS) technology. Through the publications of well-known international journals and conferences, as shown in Fig. 2-13, the research trend gradually changes from binary oxides to ternary oxides as well as from hafnium-based dielectrics to lanthanide oxides. Besides, the new dielectric must satisfy some criteria, including large energy bandgap (E_G) and high dielectric constant (κ) value. The capacitor fabricated by using dielectric material with a large energy bandgap and a high dielectric constant value could obtain a low leakage current and a large capacitance density, respectively. However, the dielectric constant and the bandgap of high-κ dielectric materials are usually trade-off. Fig. 2-14 shows the energy bandgap of several candidate oxides for gate dielectric as a function of the dielectric constant [62], [63]. The most promising dielectric in terms of the figure of merit (FOM) is given by the product of the energy bandgap and the dielectric constant. Therefore, we choose the materials with energy the bandgap larger than 5 eV and the dielectric constant larger than 20 as gate dielectrics, as shown in the oblique-line region of Fig. 2-14, including hafnium-based oxide, zirconium-based oxide, and lanthanide-based oxide.

Lanthanide oxides are possible candidates of gate dielectrics to replace the hafnium-based oxide in the next generation [64]. Lanthanide oxides have good thermal stability in contacting with silicon [65], and the most of their dielectric constant values are large enough. For example, the lanthanum oxide (La_2O_3) as a gate dielectric has been reported a high dielectric constant value up to 27 [66]. The energy bandgap (E_G) and the conduction band offset relative to silicon (ΔE_{CB}) of the lanthanide oxides also meet the requirements for gate dielectrics, being $E_G \sim 4$ to 6 eV and $\Delta E_{CB} > 2$ eV, respectively [67], [68]. Fig. 2-15

shows the energy bandgaps of various lanthanide oxides. Except for the E_G of the cerium oxide (CeO_2) smaller than 2.5 eV, the other lanthanide oxides have a E_G larger than 4 eV [67], [68]. Therefore, in this study, we choose praseodymium oxide (Pr_2O_3) and lanthanum-yttrium oxide ($LaYO_X$) as our gate dielectrics for integrating into LTPS TFT and organic TFT, respectively. The reasons why we choose these two lanthanide oxides as the gate insulators are shown in next subsection.

2.5-1 Characteristics of Praseodymium Oxide

Praseodymium oxide, a rare earth metal oxide, has been used for microelectronic applications so far. The praseodymium oxide have three various crystallographic structures, which PO_2 exhibits the cubic calcium fluoride structure with C1-type, and Pr_2O_3 crystallizes in the manganese oxide structures with D 5_3 type and D 5_2 type [69], [70]. The D 5_3 type structure is based on the calcium fluoride structure where a quarter of the oxygen atoms are removed from specific lattice sites. It has been reported that the Pr_2O_3 with hexagonal lanthanum oxide structure of D 5_2 type is suitable for epitaxy on Si (100) substrate only [69].

The melting point and the boiling point of praseodymium oxide (Pr_2O_3) are 2183 °C and 3760 °C, respectively [70]. Praseodymium oxide (Pr_2O_3) as the gate dielectric on Si substrate has a dielectric constant up to 31, deposited by molecular beam epitaxy (MBE) equipped with electron-beam evaporator [71]. As to the deposition of praseodymium oxide (Pr_2O_3) film, the studies on pulsed-laser deposition (PLD) method [72], [73] and metallorganic chemical vapor deposition (MOCVD) method [74] are also reported. The symmetrical valance and conduction band offsets relative to silicon (ΔE_{VB} and ΔE_{CB}) of praseodymium oxide measured by X-ray photoelectric spectroscopy (XPS) valence band spectrum and Fowler-Nordheim plot are all larger than 1.2 eV, respectively [75]. Due to the middle bandgap of 4.0 eV and the large formation energy of −12900 kJ/mole [70], the praseodymium oxide (Pr_2O_3) should be more stable and popular for its application on Si substrate. Particularly, the praseodymium oxide

(Pr_2O_3) film exhibits a leakage current densities 10^4 times lower than the hafnium oxide (HfO_2) film and the zirconium oxide (ZrO_2) film at the same equivalent oxide thickness (EOT) of 1.4 nm [76]. Moreover, *Osten et al.*, also reported that the praseodymium oxide film is compatible with conventional COMS processes, and demonstrated that it is no need to re-engineer the manufacturing procedures [76].

2.5-2 Characteristics of Lanthanum-Yttrium Oxide

In 2001, *W. Zhu et al.*, reported that incorporating some aluminum atoms into hafnium oxide (HfO_2) film (about 30 %) could increase the crystallization temperature up to 1000 °C, and it also could decrease the gate leakage current due to the increase of thermal stability on Si substrate [77]. Due to the smaller dielectric constant value of aluminum-doped hafnium oxide ($HfAlO_X$) (around 15), the lanthanum-doped hafnium oxide ($HfLaO_X$) was proposed by *Y. Yamamoto et al.*, with a high dielectric constant value around 25 [78]. The $HfLaO_X$ film has a wide bandgap around 5.5 eV and a good thermal stability with amorphous phase to 1000 °C so that its leakage current is very small. Even though the lanthanum oxide (La_2O_3) film is easy absorbent to become lanthanum hydroxide to degrade its dielectric constant value, the lanthanum-doped hafnium oxide film could solve this moisture absorption problem. Following, *K. Kita et al.*, also reported on the yttrium-doped hafnium oxide ($HfYO_X$) film (only need about 4 % yttrium) [79], which not only increases the thermal stability of hafnium oxide (HfO_2) but also increases the dielectric constant by the structural phase transformation from monoclinic phase to cubic phase. The atom induced a smaller molar volume (V_m) or with a large polarizability (α_m) could be chosen for doping source into high-κ dielectric [79]. The yttrium (Y) atom just conforms to these two criteria [79]. Besides, yttrium oxide (Y_2O_3) is also a high-κ dielectric material with a good thermal stability on silicon. Therefore, the high-κ lanthanum-yttrium oxide ($LaYO_X$) film is proposed to solve the moisture absorption problem of lanthanum oxide and to increase the dielectric constant value to 29 with 40-to-60 % yttrium

doped concentration [80]. This $LaYO_X$ film is deposited by radio-frequency (RF) co-sputtering of L_2O_3 and Y_2O_3 targets. The bandgap of $LaYO_X$ film with 50 % yttrium doping is also larger than 5.5 eV, and the leakage current and the hysteresis are lower than those of other reports under the same equivalent oxide thickness (EOT) [81].

2.6 REVIEW ON HIGH-κ MATERIALS USED IN THIN-FILM TRANSISTORS

In CMOS technology, for matching scaling rule to improve device performance, especially on driving capability, the gate capacitance density (C_{ins}) is continuously enlarged by using various high-κ materials with high dielectric constant values. On the other hand, in academic studies, the solid-phase crystallization (SPC) poly-Si TFT device also gradually incorporates the high-κ materials process to gain its benefits on device performance. The equivalent oxide thickness (EOT) of high-κ gate insulator could be thinner than that of the traditional tetraethoxylsilane (TEOS) gate insulator under the same physical thickness. Due to the same reason for using high-κ materials in CMOS technology, the high-κ poly-Si TFT also could increase the gate capacitance density to induce more inversion charge carriers in channel region. Therefore, the poly-Si TFT with high-κ dielectric could improve its gate controllability due to the driving capability enhancement. Several high-κ materials, including ONO stack oxide [82], nitrous oxide (N_2O) [83], tantalum pentoxide (Ta_2O_5) [84], aluminum oxide (Al_2O_3) [85], lanthanum-aluminum oxide ($LaAlO_3$) [86], and hafnium oxide (HfO_2) [16], are proposed to replace the conventional TEOS oxide served as gate insulators for the poly-Si TFTs. The comparison on electrical characteristics of LTPS poly-Si TFTs with various gate insulators are summarized in Table 2-1. Unfortunately, implementing ONO stack oxide, nitrous oxide (N_2O), and aluminum oxide (Al_2O_3) in LTPS TFTs could not effectively improve the device performance due to their low dielectric constant values. The tantalum

pentoxide (Ta_2O_5) with a narrow energy bandgap, especially on its smaller conduction bandgap offset relative to silicon (ΔE_{CB}), is not suitable for n-type LTPS TFTs application due to the gate leakage current issue. By the way, in Table 2-1, the LTPS TFT with hafnium oxide (HfO_2) gate dielectric has the smallest threshold voltage (V_{TH}) of 0.3 V. The reason is that its channel width is 100 nm approximate to the thickness of active channel of 50 nm so that its operation mode is like Fin-FET device with well gate controllability. Besides, the 30-min ammonia (NH_3) plasma treatment is also contributed to passivate the trap states in the grain boundaries and interface of this LTPS TFT with a hafnium oxide (HfO_2) gate dielectric.

Furthermore, OTFT with a low mobility and a high operation voltage, compared to LTPS TFT, is more necessary to introduce the high-κ dielectric process to improve the device performance. The mobility of pentacene-based OTFT increases linearly with the increase of electric field (E) and charge density in channel layer (Q_S), but eventually saturates, as shown in Fig. 2-16 [25]. Q_S is a function of the accumulated carriers concentration in channel layer. Except for thermal oxide (SiO_2), gate dielectrics with high-κ materials could induce more charge density in channel layer (Q_S) under the same electric field (gate and drain voltages) corresponding to the channel mobility (μ). Table 2-2 shows the comparison on electrical characteristics of pentacene-based OTFTs with various gate dielectrics, including thermal oxide (SiO_2) [25], barium zirconate titanate (BZT) [25], gadolinium oxide (Gd_2O_3) [87], tantalum pentoxide (Ta_2O_5) [88], lanthanum-aluminum oxide ($LaAlO_3$) [89], titanium oxide (TiO_2) [90], manganese-doped barium strontium titanate (Mn-BST) [91], and titanium-silicon oxide (TiSiO) [92]. We can see that the mobility of pentacene-based OTFTs without interface modification from hydrophilic to hydrophobic [22]-[24] is within 0.1 to 0.4 cm^2/V-s. When the gate capacitance density (C_{ins}) is increased, the operational voltage and the threshold voltage (V_{TH}) could be decreased, particularly on the highest C_{ins} fabricated by titanium oxide (TiO_2) [90]. By the way, the pentacene-based OTFTs using lanthanum-aluminum oxide ($LaAlO_3$) has the best mobility. The reason is that introducing lanthanum (La^{3+}) with ionic

bond nature and as the same valence as that of aluminum (Al^{3+}) reduce the dangling bonds caused by Al^{3+} so that improve the mobility and hysteresis [89]. Therefore, in our work, we use the same kind of lanthanum-yttrium oxide ($LaYO_X$) as the gate insulator processed in pentance-based OTFT.

2.7 CURRENT EQUATIONS OF THIN-FILM TRANSISTORS

2.7-1 Drain Current Equations in Linear and Saturation Regions

In this section, we formulate a general drain current for thin-film transistor by using gradual channel approximation (GCA) model [93], which the variation of the electrical field along the channel is much less than that along the corresponding variation perpendicular to channel. Hence, the inversion charges density (Q_{inv}) could be simplified to the 1-D form of Possion's equation, as shown in Fig. 2-17 [93]. The current-voltage characteristic of the thin-film transistor could be calculated by estimating the elemental resistance dR and the elemental segment dy of the conducting channel given by

$$dV = I_{DS}dR = I_{DS}\frac{dy}{W\mu_{EF}|Q_{inv}(y)|} \tag{2-2}$$

, where W is the channel width and μ_{EF} is the field-effect mobility. And then, integrating Eq. (2-2) from source ($V=0$ at $y=0$) to drain ($V=V_{DS}$ at y=L), the drain current could be expressed as

$$\int_0^L I_{DS}dy = \mu_{FE}W\int_0^{V_{DS}}|Q_{inv}|dV \quad \rightarrow \quad I_{DS} = \mu_{FE}\frac{W}{L}\int_0^{V_{DS}}|Q_{inv}|dV\ . \tag{2-3}$$

Following, we use the charge-sheet approximation model [94], which assumes that the inversion charges (Q_{inv}) are located at the silicon surface as a sheet of charges with no potential dropping or band bending across the inversion layer, to derive drain current as

$$Q_{inv} = Q_S - Q_{dep} = -C_{ins}\left(V_{GS} - V_{fb} - 2\psi_B - V\right) + \sqrt{2\varepsilon_{Si}qN_B\left(2\psi_B + V\right)} \tag{2-4}$$

, where Q_S is the total surface charge density, Q_{dep} is the depletion charge density, V_{fb} is the flat band voltage, the surface potential ψ_S is pinned at $\psi_S = 2\psi_B + V(y)$, C_{ins} is the gate capacitance density of insulator layer, ε_{Si} is the dielectric constant of silicon, and N_B is the effective channel dpoant in active channel of the thin-film transistor. Substituting Eq. (2-4) into Eq. (2-3) and carrying out the integration, the drain current (I_{DS}) could be presented by

$$I_{DS} = \mu_{FE}\frac{W}{L}\int_0^{V_{DS}} |Q_{inv}|dV = \mu_{FE}C_{ins}\frac{W}{L}\left\{(V_{GS}-V_{TH})V_{DS} - \frac{m}{2}{V_{DS}}^2\right\} \quad (2\text{-}5)$$

, where the body-effect coefficient m and the threshold voltage V_{TH} are

$$m = 1 + \frac{\sqrt{\varepsilon_{Si}qN_B/4\psi_B}}{C_{ins}} \text{ and } V_{TH} = V_{fb} + 2\psi_B + \frac{\sqrt{4\varepsilon_{Si}qN_B\psi_B}}{C_{ins}}\text{, respectively.} \quad (2\text{-}6)$$

When the device works in saturation region, the I_{DS} is independent on V_{DS}, which means

$$\frac{dI_{DS}}{dV_{DS}} = (V_{GS}-V_{TH}) - mV_{DS} = 0 \rightarrow V_{DS} = V_{DS,sat} = \left(\frac{V_{GS}-V_{TH}}{m}\right). \quad (2\text{-}7)$$

Substituting Eq. (2-7) into Eq. (2-5), the saturation current $I_{DS,sat}$ could be written as

$$I_{DS,sat} = \mu_{FE,sat}C_{ins}\frac{W}{L}\frac{(V_{GS}-V_{TH,sat})^2}{2m} \quad (2\text{-}8)$$

In $m = 1$ case, the Eq. (2-5) and Eq. (2-8) could be simplified by

$$I_{DS,lin} = \mu_{FE,lin}C_{ins}\frac{W}{L}\left\{(V_{GS}-V_{TH,lin})V_{DS} - \frac{1}{2}{V_{DS}}^2\right\} \quad \text{for linear operation} \quad (2\text{-}9)$$

and

$$I_{DS,sat} = \frac{1}{2}\mu_{FE,sat}C_{ins}\frac{W}{L}(V_{GS}-V_{TH,sat})^2 \quad \text{for saturation operation, respectively.} \quad (2\text{-}10)$$

2.7-2 Drain Current Equations in Subthreshold Region

To derive the subthreshold current, we start at solving Poisson's equation in the surface region of semiconductor, whose detail band diagram and potential of p-type silicon are summarized in Fig. 2-18 [93]. The Poisson's equation in this band diagram could be

re-written as

$$\frac{d^2\psi}{d^2x} = -\frac{d\xi_{Si}}{dx} = -\frac{q}{\varepsilon_{Si}}\left[N_B\left(\exp\left(\frac{-q\psi}{k_BT}\right)-1\right)-\frac{n_i^{\,2}}{N_B}\left(\exp\left(\frac{q\psi}{k_BT}\right)-1\right)\right] \tag{2-11}$$

, where ψ is the potential in silicon, ξ_{Si} is the electric field in silicon, and k_B is the Boltzmann constant. At $x=0$, let $\psi=\psi_S$ (surface potential). Based on the Gauss's law, the total charge density ($|Q_S|$) is

$$|Q_S| = |Q_{acc}| + |Q_{dep}| + |Q_{inv}| = -\varepsilon_{Si}\xi_{Si} = \varepsilon_{Si}\int\frac{d^2\psi}{d^2x}\left(\frac{d\psi}{dx}dx\right). \tag{2-12}$$

Substitute Eq. (2-11) into Eq. (2-12) and arrange the $|Q_S|$ as

$$|Q_S| = \sqrt{2\varepsilon_{Si}k_BTN_B}\left\{\left(\exp\left(-\frac{q\psi_s}{k_BT}\right)-\left(-\frac{q\psi_s}{k_BT}\right)-1\right)+\left(\frac{n_i}{N_B}\right)^2\left(\exp\left(\frac{q\psi_s}{k_BT}\right)-\left(\frac{q\psi_s}{k_BT}\right)-1\right)\right\}^{1/2}. \tag{2-13}$$

In substhreshold operation, we only consider the inversion charge density (Q_{inv}) in channel region, and the last significant terms of Eq. (2-13) could be re-written as

$$Q_{inv} = \sqrt{\frac{\varepsilon_{Si}qN_B}{2\psi_S}}\frac{k_BT}{q}\left(\frac{n_i}{N_B}\right)^2\exp\left(\frac{q(\psi_S-V)}{k_BT}\right) \tag{2-14}$$

, where the $(\psi_S - V)$ term is considered as the influence of drain voltage on active channel. Substituting Q_{inv} of Eq. (2-14) into Eq. (2-3), and carrying out the integration, the drain current in the subthreshold region ($I_{DS,SUB}$) could be presented by

$$I_{DS,SUB} = \mu_{FE}\frac{W}{L}\int_0^{V_{DS}}|Q_{inv}|dV = \mu_{FE}C_{ins}\frac{W}{L}\sqrt{\frac{q\varepsilon_{Si}N_B}{2\psi_S}}\left(\frac{k_BT}{q}\right)^2\left(\frac{n_i}{N_B}\right)^2\exp\left(\frac{q\psi_S}{k_BT}\right). \tag{2-15}$$

2.7-3 Drain Current Equations of Organic Thin-Film Transistors

Most organic thin-film transistors operate in the accumulation region, where the gate voltage is polarized positively (negatively) versus the n-type (p-type) substrate. Because organic thin-film transistor operates in accumulation region, we only take account in the

accumulation charges density (Q_{acc}) and the free carrier density (Q_0) in organic channel layer, where

$$|Q_0| = qn_0 d_s \quad \text{and} \quad |Q_S| = C_{ins}\left[V_{GS} - V_{fb} - V(y)\right] \sim |Q_{acc}|. \tag{2-16}$$

In Eq. (2-16), n_0 is the density of free carriers at equilibrium, d_s is the thickness of the semiconductor, C_{ins} is the gate capacitance density, V_{fb} is the flat band voltage, and $V(y)$ is accounted as the drain influence. Because the organic thin-film transistor works in accumulation mode, $Q_S(y)$ and Q_0, the total charges in channel, have identical sign neglecting the ohmic drop in channel. Hence, the drain current in linear region (in $V_{DS} < V_{GS}$) could be obtained from gradual channel approximation (GCA) model

$$dV = I_{DS,lin} dR = I_{DS,lin} \frac{dy}{W \mu_{EF,lin} |Q_S(y) + Q_0|}. \tag{2-17}$$

Substituting Eq. (2-16) and Eq. (2-17) into Eq. (2-3), we can obtain

$$I_{DS,lin} = \mu_{FE,lin} \frac{W}{L} C_{ins} \left[\left(V_{GS} - V_{TH,lin}\right) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2-18}$$

, where $V_{TH,lin}$ is the threshold voltage in linear region and could be written as

$$V_{TH,lin} = V_{fb} + \frac{qn_0 d_s}{C_{ins}}. \tag{2-19}$$

However, when $V_{DS} > V_{GS}$, the accumulation layer near drain changes to a depletion layer, as shown in Fig. 2-19 [95]. In depletion region, there is no free carrier at semiconductor/insulator interface. Thus, the integrating term of free carriers Q_0 in Eq. (2-16) should be modified as

$$|Q_0| = qn_0 \left[d_s - W(y) \right] \tag{2-20}$$

, where $W(y)$ is the depletion width near the drain region. And, the depletion width could be solved by the voltage drop equation as

$$V_{GS}-V_{fb}-V(y)=V_{OX}+V_{Semi}=\frac{qN_BW(y)}{C_{ins}}+\frac{qN_BW^2(y)}{2\varepsilon_{Semi}}\sim V_{GS}-V(y) \tag{2-21}$$

, where N_B is the dopant concentration and ε_{Semi} is the dielectric constant of the organic semiconductor. Then, the depletion width near drain $W(y)$ could be solved as

$$W(y)=\frac{\varepsilon_{Semi}}{C_{ins}}\left[\sqrt{1+\frac{2C_{ins}{}^2\left[V_{GS}-V(y)\right]}{qN_B}}-1\right]. \tag{2-22}$$

Hence, substituting Eq. (2-22) and Eq. (2-20) into Eq. (2-3), and the drain current in saturation region ($V_{DS}>V_{GS}$) could be expressed as

$$\begin{aligned}I_{DS,sat}&=\mu_{FE,sat}\frac{W}{L}C_{ins}\int_0^{V_{GS}}\left[V_{GS}-V_{TH,sat}-V\right]dV+\mu_{FE,sat}\frac{W}{L}qn_0\int_0^{V_{dsat}}\left[d_s-W(y)\right]dV\\&=\mu_{FE,sat}\frac{W}{L}C_{ins}\int_0^{V_{GS}}\left[V_{GS}-V_{TH,sat}-V\right]dV\\&\quad+\mu_{FE,sat}\frac{W}{L}\frac{q^2n_0N_B}{\varepsilon_{Semi}}\int_0^{d_s}(d_s-W)\left(W+\frac{\varepsilon_{Semi}}{C_{ins}}\right)dW\\&=\mu_{FE,sat}\frac{W}{L}\left[C_{ins}\left(\frac{V_{GS}{}^2}{2}-V_{GS}V_{TH,sat}\right)+\frac{q^2n_0N_B}{\varepsilon_{Semi}}\frac{d_s{}^3}{6}\left(1+3\frac{C_{Semi}}{C_{ins}}\right)\right].\end{aligned} \tag{2-23}$$

Because the organic thin-film transistor has a thin semiconductor layer, $C_{Semi}>>C_{ins}$, where C_{Semi} is the depletion capacitance density of $\frac{\varepsilon_{Semi}}{d_s}$. Assuming $N_B=n_0$ yields $\frac{qN_Bd_s}{C_{ins}}=V_{TH,sat}$, and the Eq. (2-23) could be made as

$$\begin{aligned}I_{DS,sat}&=\frac{1}{2}\mu_{FE,sat}\frac{W}{L}C_{ins}\left(V_{GS}{}^2-2V_{GS}V_{TH,sat}+V_{TH,sat}\frac{qN_Bd_s}{C_i}\right)\\&=\frac{1}{2}\mu_{FE,sat}\frac{W}{L}C_{ins}\left(V_{GS}-V_{TH,sat}\right)^2.\end{aligned} \tag{2-24}$$

This formula is the saturation drain current of the organic thin-film transistor.

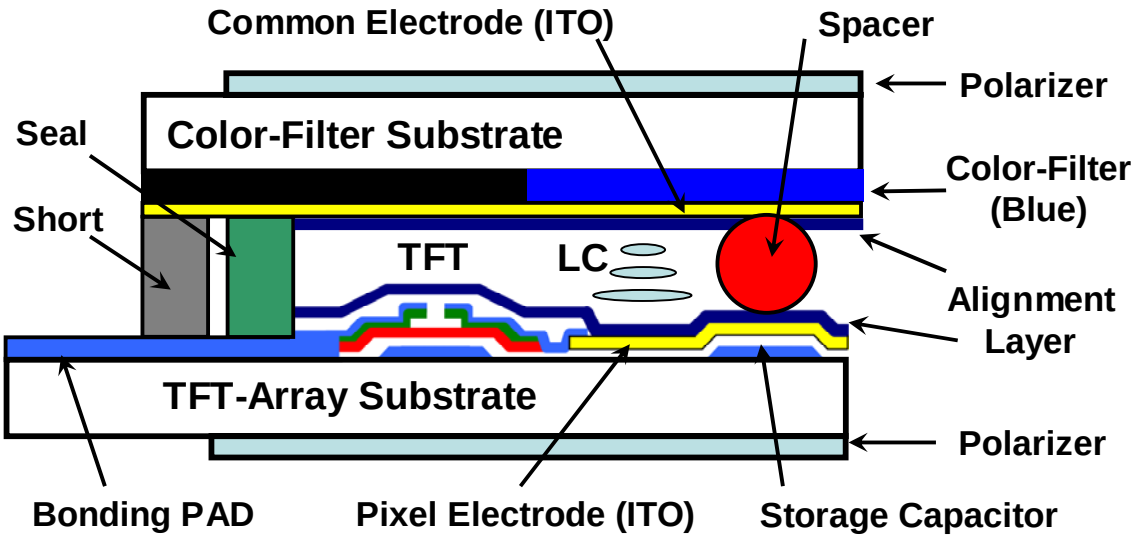


Fig. 2-1. Cross-sectional view of a unit pixel in active-matrix liquid crystal display (AMLCD) [26].

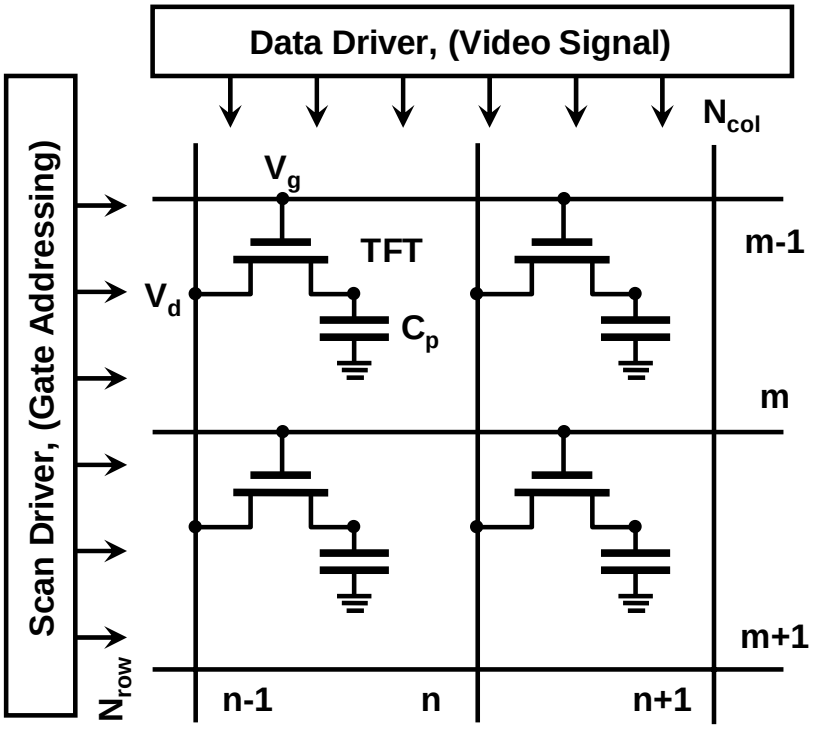


Fig. 2-2. The equivalent circuitry for the addressing matrix of an AMLCD [27].

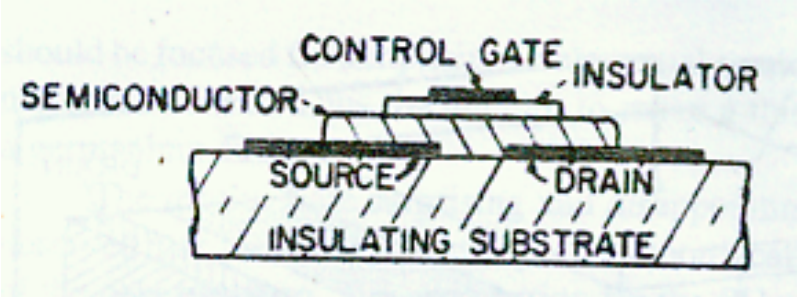


Fig. 2-3. Schematic diagram of Weimer's CdS TFT with top-gate staggered structure [28].

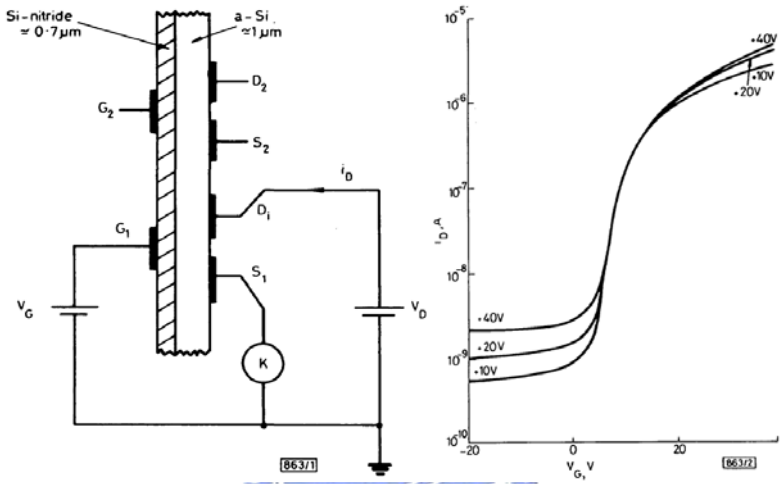


Fig. 2-4. Schematic diagram of LeComber's amorphous silicon (α-Si) TFT structure and its transfer characteristics [30].

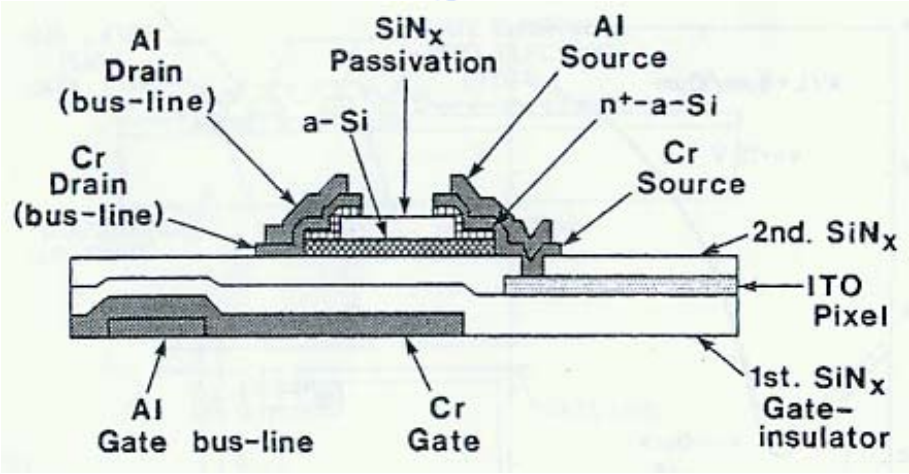


Fig. 2-5. Schematic cross section of an α-Si TFT with the "etch-stopper" layer and the in-situ tri-layer [32].

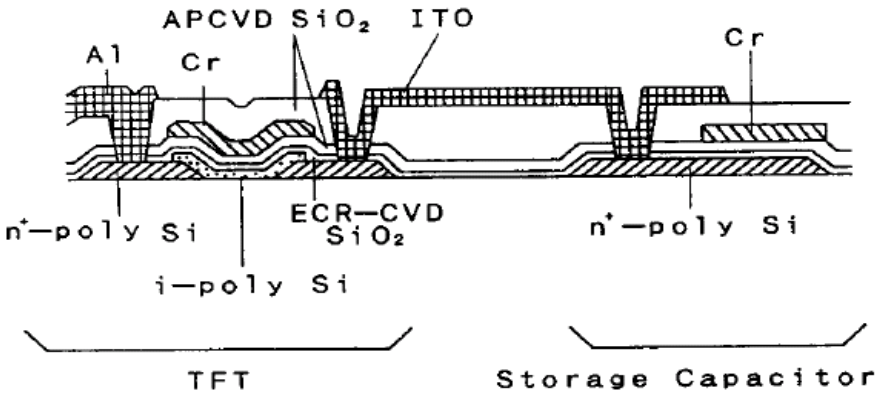


Fig. 2-6. Schematic cross section of a top-gate low-temperature polysilicon TFT with a storage capacitor [34].

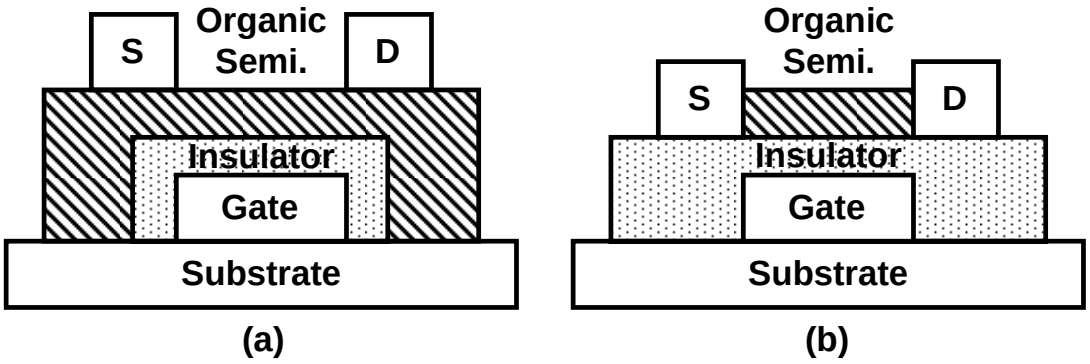


Fig. 2-7. Schematic of the geometries frequently used in organic thin-film transistors with (a) inverted-staggered structure, and (b) inverted-coplanar structure [44].

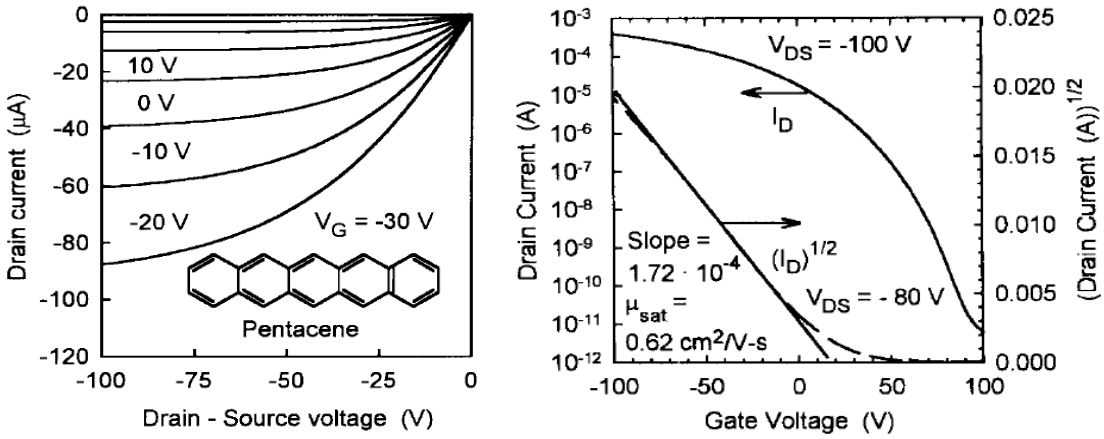


Fig. 2-8. The output characteristic and the transfer characteristic of the pentacene-based organic thin-film transistor with a high saturation mobility of 0.62 cm^2/V-s [46].

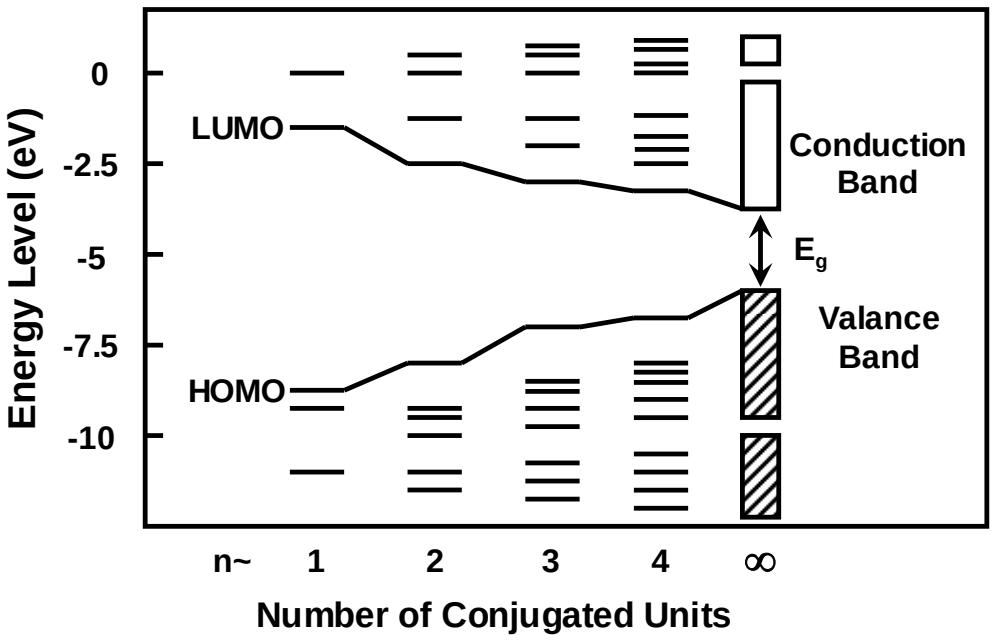


Fig. 2-9. The energy levels of oligo-thiophenes and poly-thiophenes as a function of the number of conjugated units [48].

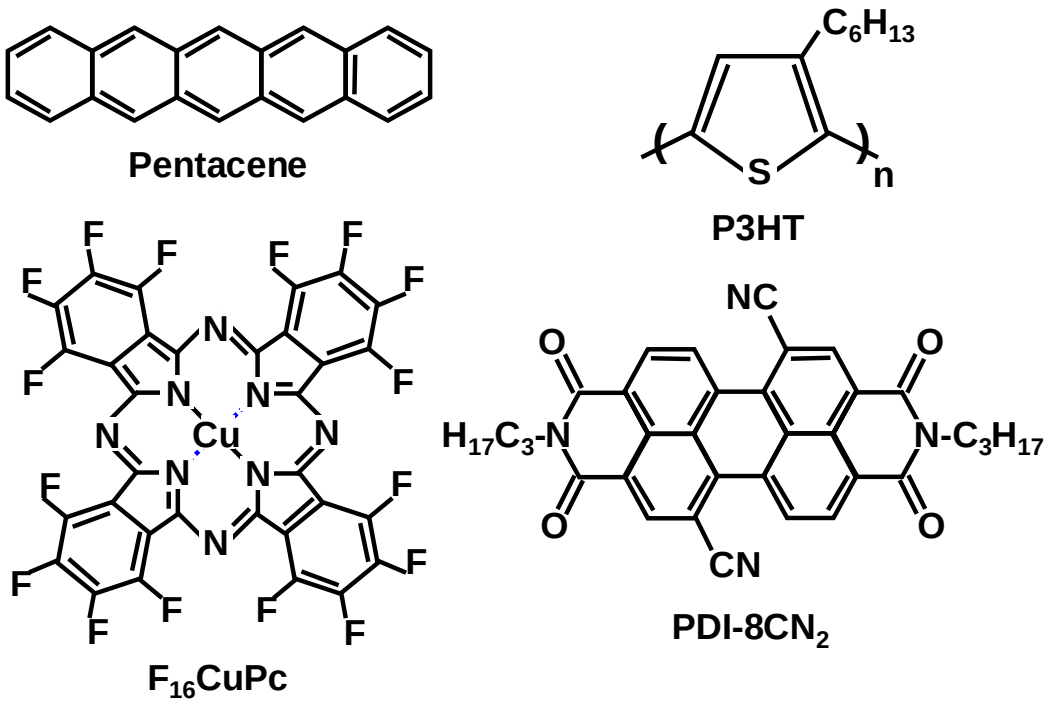


Fig. 2-10. Commonly used high-performance organic and polymer semiconductor materials [21].

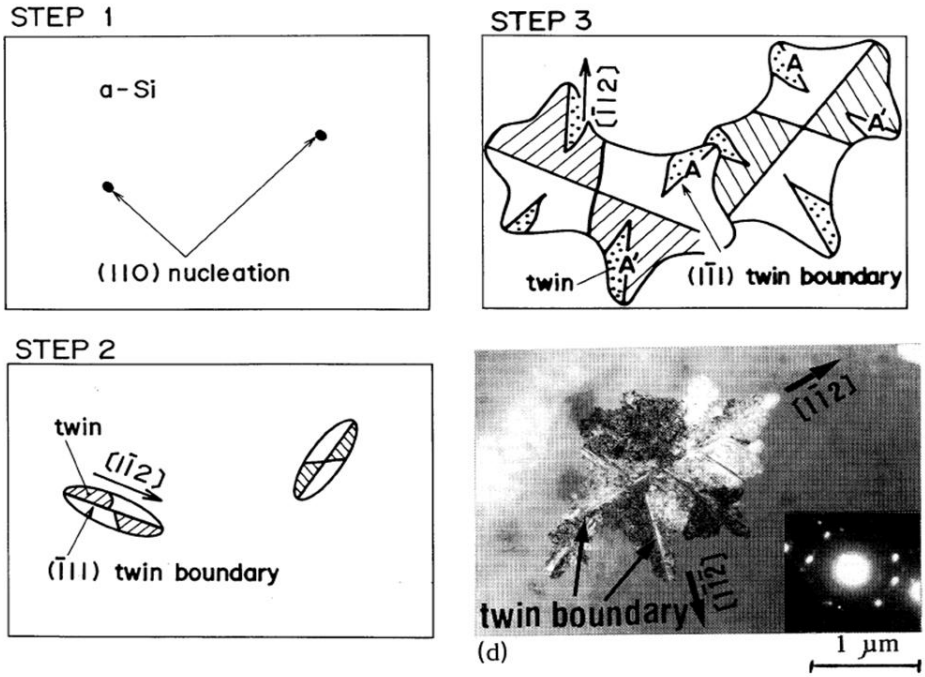


Fig. 2-11. Schematic of the re-crystallization mechanism for solid phase growth of amorphous silicon (α-Si) [52].

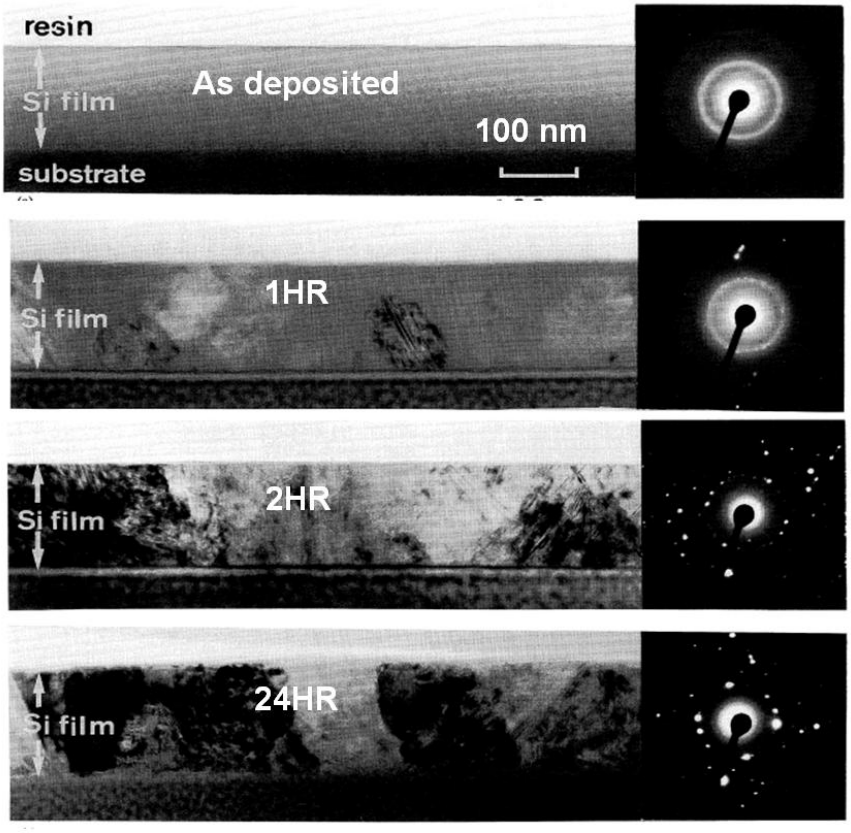


Fig. 2-12. TEM micrographs for amorphous silicon (α-Si) film as a function of annealing time, such as as-deposited, 1HR, 2HR, and 24HR [53].

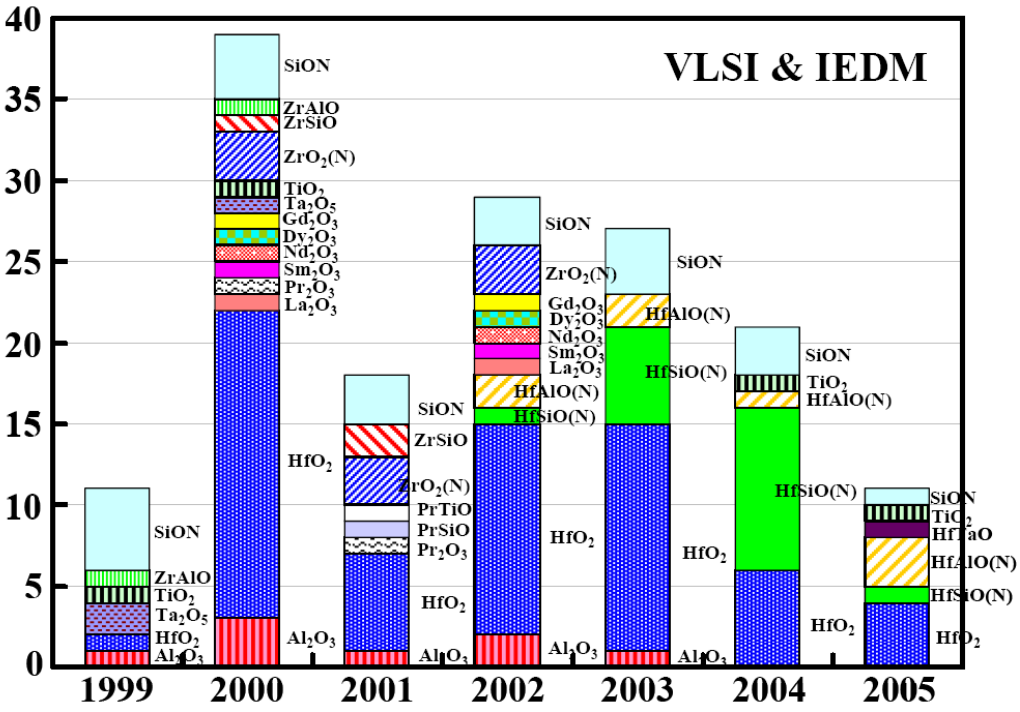


Fig. 2-13. Summarized alternative high-κ gate dielectric materials reported in VLSI Symposium and IEDM from 1999 to 2005.

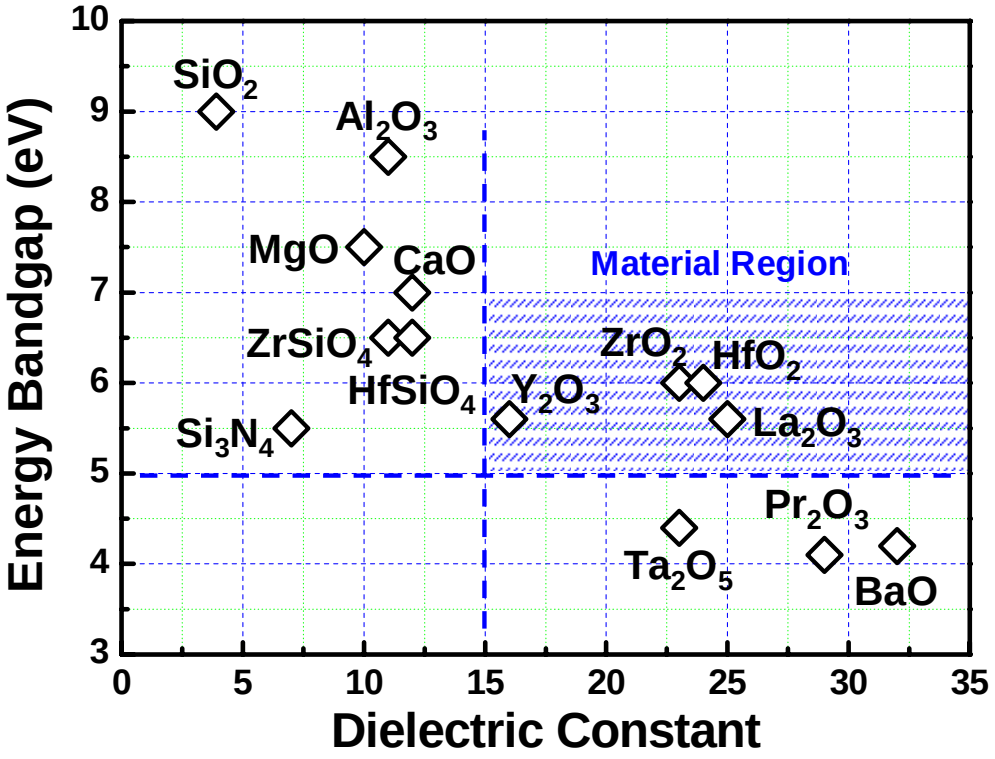


Fig. 2-14. Energy bandgap versus dielectric constant plots for candidate gate insulators [62], [63].

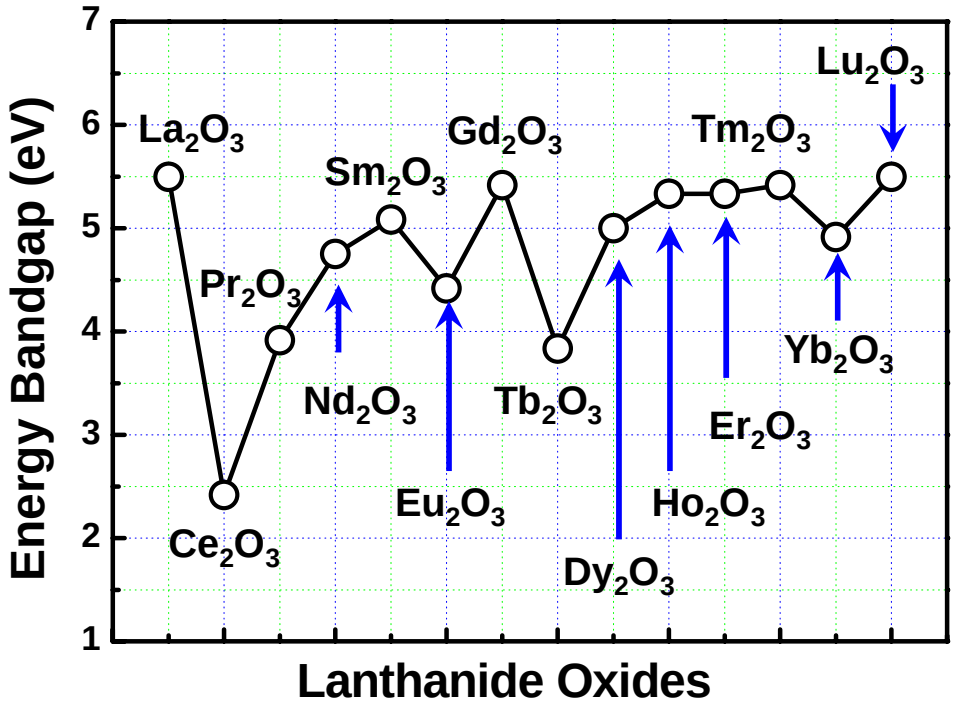


Fig. 2-15. Energy bandgap versus various lanthanide oxides [67], [68].

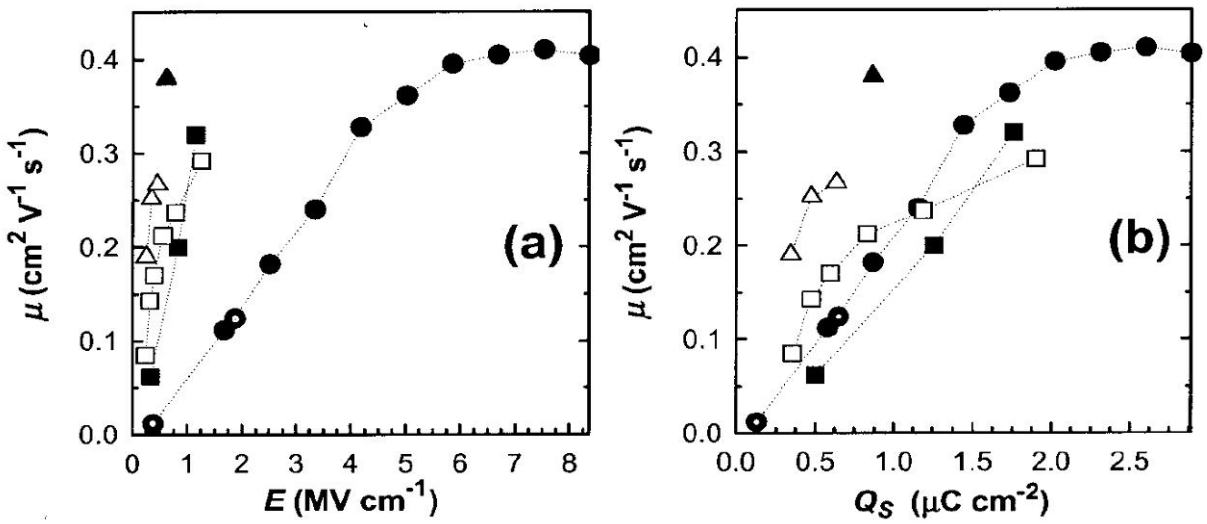


Fig. 2-16. Dependence of mobility (μ) on gate electric field (E). (b) Dependence of channel mobility (μ) on charge density (Q_S). Black or white sample correspond to channel mobility (μ) calculated from gate sweep or drain sweep, respectively. 500 nm SiO_2 with gate sweeps (o); 120 nm SiO_2 with gate sweeps (•); 82 nm BST with drain sweeps (♠); 90 nm BST with gate sweeps (Δ); 122 nm BZT with drain sweeps (■); 128 nm BZT with gate sweeps (□) [25].

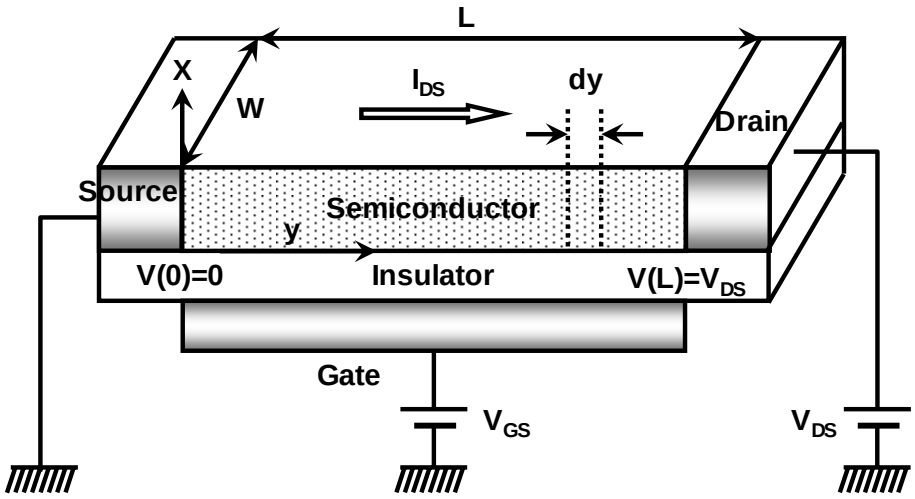


Fig. 2-17. Schematic view of a thin-film transistor (TFT) under gate and drain biases [93].

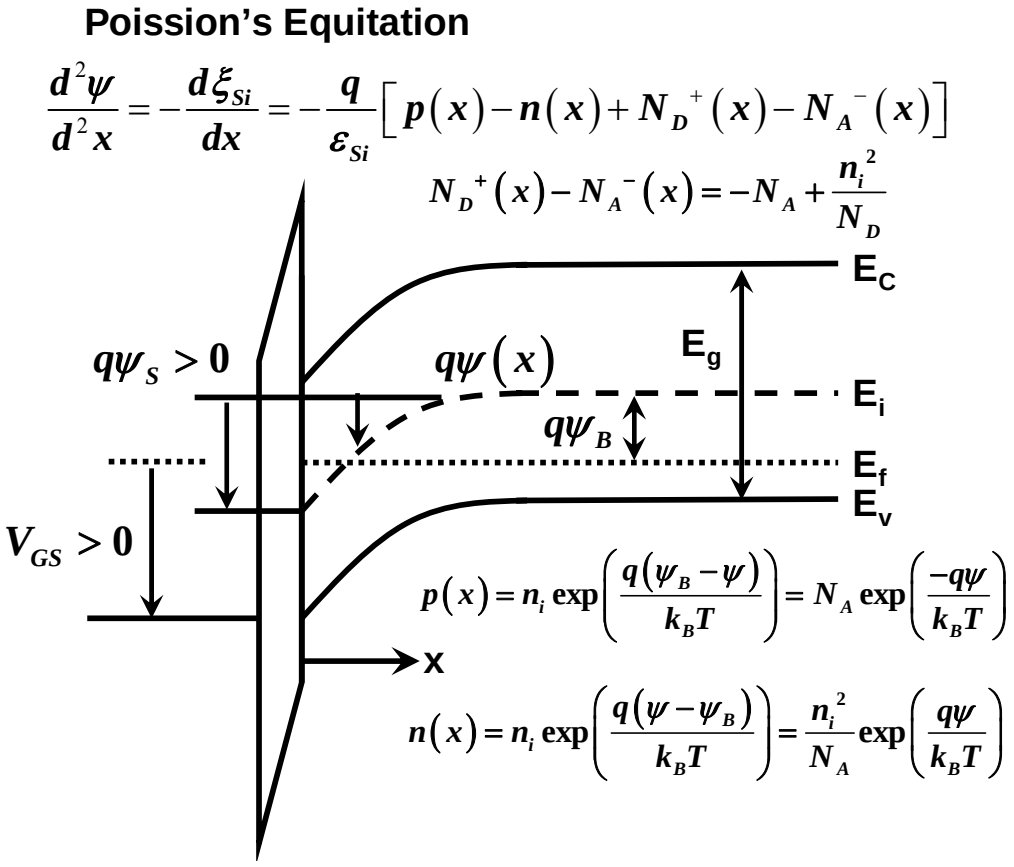


Fig. 2-18. The energy bandgap diagram of the metal-insulator-semiconductor (MIS) structure under gate bias [93].

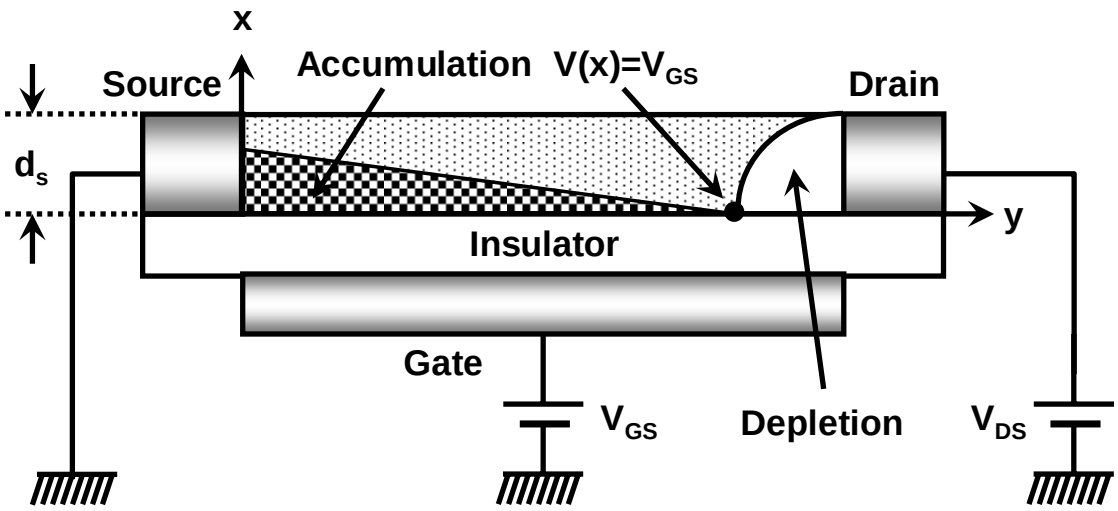


Fig. 2-19. Schematic view of an organic thin-film transistor (OTFT) working in accumulation region under high drain bias [95].

Table 2-1. Comparison on electrical characteristics of SPC poly-Si TFTs with various gate dielectrics, including TEOS oxide, ONO stack oxide, nitrous oxide (N_2O), aluminum oxide (Al_2O_3), lanthanum-aluminum oxide ($LaAlO_3$), and hafnium oxide (HfO_2).

SPC TFT with Various Dielectrics	40 nm TEOS [60]	22 nm ONO [82]	21 nm N_2O [83]	50 nm Al_2O_3 [85]	50 nm $LaAlO_3$ [86]	27.7 nm HfO_2 [16]
EOT	40 nm	----	----	20 nm	8.7 nm	7.3 nm
W/L (mm)	50/10	40/10	50/10	200/3	100/4	0.1/1
V_{TH} (V)	5.14	4.75	4.75	3*	1.2	0.3 **
μ_{FE} (cm^2/V-s)	12.4	4.6	26.8	47*	40	39 **
S.S. (mV/Dec.)	1970	642	410	440*	310	280 **
I_{ON}/I_{OFF} (10^6)	0.24	0.95	1.72	0.3*	6.3	9.7 **

* $Si_{0.85}Ge0_{0.15}$ TFT with Al_2O_3 dielectric ** NH_3 plasma passivation for 30 min

Table 2-2. Comparison on electrical characteristics of pentacene-based organic TFTs with various gate dielectrics, including silicon oxide (SiO_2), barium zirconate titanate (BZT), gadolinium oxide (Gd_2O_3), tantalum pentoxide (Ta_2O_5), lanthanum-aluminum oxide ($LaAlO_3$), titanium oxide (TiO_2), Mn-doped barium strontium titanate (Mn-BST), and titanium-silicon oxide (TiSiO).

	D (nm)	C_{ins} (nF/cm^2)	$\mu_{FE,sat}$ (cm^2/V-s)	I_{ON}/I_{OFF}	*S.S.* (mV/Dec.)	V_{TH} (V)
SiO_2 [25]	100	6.9	0.12	$3x10^5$	1785	–18 V @ V_D = –50 V
BZT [25]	122	125	0.38	$3x10^5$	300	–2 V @ V_D = –5 V
Gd_2O_3 [87]	280	125	0.1	10^3	300	–3.5 V @ V_D = –8 V
Ta_2O_5 [88]	45	334	0.32	10^4	500	–0.8 V @ V_D = –5 V
$LaAlO_3$ [89]	330	402	1.4	10^7	---	–15 V @ V_D = –40 V
TiO_2 [90]	280	676	0.15	$3.5x10^6$	170	–0.34 V @ V_D = –1 V
Mn-BST [91]	200	106	0.32	$4x10^2$	7000	–1 V @ V_D = –4 V
TiSiO [92]	73	125	0.14	$3x10^6$	140	–2.9 V @ V_D = –10 V

CHAPTER 3

FABRICATION AND CHARACTERIZATION METHODS

In this chapter, the detail fabrication steps of the low-temperature polysilicon (LTPS) thin-film transistors (TFTs) and the pentacene-based organic thin-film transistors (OTFTs) with high dielectric constant (high-κ) gate insulators are described. The praseodymium oxide (Pr_2O_3) film is used for LTPS TFTs. Besides, for pentacene-based OTFTs, the lanthanum-yttrium oxide ($LaYO_X$) film is chosen. The physical analysis techniques as well as the electrical measurement methods used to characterize both LTPS TFTs and OTFTs are also included and presented in this chapter.

3.1 FABRICATION OF LOW-TEMPERATURE POLYCRYSTALLINE SILICON PRASEODYMIUM OXIDE THIN-FILM TRANSISTORS WITH VARIOUS NITROGEN DOSAGES

The main fabrication steps of the low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) with a praseodymium oxide (Pr_2O_3) dielectric were summarized below and shown in Fig. 3-1. In modern liquid crystal display (LCD) industry, the amorphous silicon (α-Si) TFTs or the LTPS TFTs were fabricated on glass substrate as the switching devices in array cells. In our study, the 500-nm thermal oxide grown on 6-inch silicon wafer by using a horizontal furnace was used to simulate the glass substrate of active matrix liquid crystal display (AMLCD). And then, an undoped α-Si film with 50-nm thickness was deposited on the 500-nm thermal oxide by using a low-pressure chemical vapor deposition (LPCVD) system in silane (SiH_4) ambient with a pressure of 350 mtorr at 560 °C. In addition,

before silicon oxidation, chemical vapor deposition (CVD), and high-κ deposition in this work, all samples were cleaned by using the traditional RCA process to remove any contamination, native oxide, and atomic scale roughness [96].

To explore the nitrogen effect on the re-crystallization, the nitrogen atoms with various dosages of zero (control sample), 5×10^{12} cm^{-2}, and 5×10^{13} cm^{-2}, were implanted into the 50-nm α-Si film with an ion implantation energy of 10 keV, as presented in Fig. 3-1(a). The implantation energy of nitrogen atoms was set by 10 keV with a projected range about 25 nm to induce significant influence overall 50-nm α-Si film. After nitrogen implantation, the conventional solid-phase crystallization (SPC) annealing was processed at 600 °C for 24 hrs in nitrogen ambient to crystallize α-Si film into polycrystalline silicon (poly-Si) film. Such as traditional SPC annealing with the maximum process temperature limited at 600 °C was widely used to recrystallize amorphous silicon (α-Si) film due to its low-production cost and good grain-size uniformity.

Subsequently, the active regions of LTPS TFTs were lithographically patterned and then etched by using a transformer-coupled-plasma (TCP) dry etcher with a chlorine-based gas. The edge of the active region must be formed an inclined and trapezoid shape because the latter high-κ gate insulator was deposited by using a physical vapor deposition (PVD) method, for its consideration to poor step coverage. Therefore, the exposure dosage and the focus offset should be fine trimmed to exposure the photoresist pattern in a trapezoid shape, and afterward the edge of the active region could become in a trapezoid shape during an anisotropic dry etching process. After removing residue photoresist and performing RCA cleaning process on the poly-Si film, the high-κ praseodymium oxide (Pr_2O_3) was deposited as the gate insulator by using an electron-beam evaporation system. The working pressure and the deposition rate were controlled within 5×10^{-5} torr and 0.05 nm/sec, respectively. In order to improve the quality of gate insulator, the praseodymium oxide as the gate dielectric was subjected to a rapid thermal annealing (RTA) process at 600 °C for 1 minute in oxygen

ambient, as shown in Fig. 3-1(b).

After the gate dielectric formation, a 200-nm tantalum nitride (TaN) film was deposited in $N_2/(Ar+N_2)$ = 5 % ambient at 600 mtorr with a DC power of 500 watt by using a reactive sputter system. Such refractory TaN metal with a resistance to acid-and-oxidation was applicable to gate electrode of thin-film transistor. Next, the TaN metal gate with a thickness of 200 nm was also defined by using a transformer-coupled-plasma (TCP) etcher with a chlorine-based gas, and it could be completely etched within 1 minute. However, the etching rates of the praseodymium oxide layer and I-line photoresist were approximate 0.1 nm/sec and 3 nm/sec, respectively, so that the I-line photoresist with 800-nm thickness could not protect the TaN metal gate if the 42-nm Pr_2O_3 dielectric was completely removed. Therefore, such dry etching process was capable of stopping on the praseodymium oxide layer while the TaN gate was completely removed, and we took account of the other etching process to remove this Pr_2O_3 dielectric for the following interconnection.

As displayed in Fig. 3-1(c), phosphorus atoms were self-aligned implanted through the praseodymium oxide layer into the 50-nm poly-Si film with the dosage and the energy of 5×10^{15} cm^{-2} and 90 keV, respectively, to form the source and drain regions of LTPS TFTs. And then, the phosphorus dopants in source and drain regions were activated by using a rapid thermal annealing (RTA) process at 600 °C for 1 minute in nitrogen ambient. Afterwards, the 300-nm tetraethoxylsilane (TEOS) oxide film used as an inter-layer dielectric (ILD) layer was deposited by using a plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C. Because the praseodymium oxide could not be effectively etched by using a dry etching process, the contact holes were opened by a two-step contact etching process for interconnection, as illustrated in Fig. 3-1(d). Firstly, the 300-nm ILD passivation layer on the source and drain regions was removed by using a wet etching process with a buffered oxide etch (BOE) solution or a dry etching process with a fluorine-based gas. Secondly, the mixed solution of H_3PO_4: HNO_3: CH_3COOH: H_2O = 50: 2: 10: 9 heated to 60 °C was used to

dissolve the praseodymium oxide film with a high etching selectivity to the ILD passivation layer, the TaN gate metal, and the source and drain regions of poly-Si film. Consequently, the praseodymium oxide film could be completely removed by an over etching. In fact, in this wet etching procedure, the lanthanide-series metal oxides, such as terbium oxide (Tb_2O_3) or dysprosium oxide (Dy_2O_3), could be removed by this mixed solution with a stable etching rate of 0.4 ~ 0.5 nm/sec, except for lanthanum oxide (La_2O_3). The etching rate of the lanthanum oxide by using this mixed solution was so quick (larger than 200 nm/sec) that the gate dielectric of the La_2O_3 film would be etched over through the channel region of the transistor device. Accordingly, this mixed solution should be diluted or changed with the other recipes for etching La_2O_3 film.

After the contact holes were opened by this two-step wet etching process, the 500-nm aluminum (Al) film was deposited at 600 mtorr with a DC power of 1500 watt by using a reactive sputter system. Finally, the aluminum pads were lithographically patterned, and subsequently etched by using a TCP metal etcher, and then the nitrogenous poly-Si TFTs with the (Pr_2O_3) gate dielectric were accomplished, as indicated in Fig. 3-1(e). For comparison, the control Pr_2O_3 poly-Si TFT without nitrogen implantation (D_N = 0) was also prepared by the same process flow. In addition, note that all Pr_2O_3 poly-Si TFTs had no extra plasma treatment to passivate the trap states in active channel [7], [8] in this work. In order to verify the electrical properties of the praseodymium oxide (Pr_2O_3) film, the Pr_2O_3 metal-insulator-silicon (MIS) capacitors were also fabricated together with the same LTPS TFTs process, including the deposition and the annealing of the high-κ dielectric. For the Pr_2O_3 MIS capacitor fabrication, a shadow mask was used to define the top TaN electrode in a circle pattern with a radius of 220 μm. The bottom aluminum electrode was also deposited after the native oxide on the backside substrate was wiped out by using a buffered oxide etching (BOE) solution.

3.2 FABRICATION OF PENTACENE-BASED ORGANIC THIN-FILM TRANSISTORS WITH LANTHANUM-YTTRIUM OXIDE

Figs. 3-2(a) and 3-2(b) showed the schematic top view and its cross section along the AA' line of the fabricated bottom-gate-top-contact pentacene-based organic thin-film transistor (OTFT) with the gate insulator of high-κ lanthanum-yttrium oxide ($LaYO_X$), respectively. In this OTFT work, all pattern regions were defined by the shadow masks, and the process steps corresponding to their shadow masks were shown in Fig. 3-3. In Fig. 3-3(a), the 500-nm thermal oxide was grown on a 4-inch silicon wafer as a buffer layer to simulate a glass substrate or a flexible substrate where OTFT devices were fabricated. And then, the tantalum nitride (TaN) with a 50-nm thickness was deposited on the oxide/silicon substrate as the bottom-gate electrode, through the shadow mask 1, by using a reactive sputtering system. Here, the sputter condition was the same as that on the metal gate process of LTPS TFT. Following, the bottom TaN electrode was treated with ammonia (NH_3) plasma at 200 mtorr with a RF power of 100 watts for 10 minutes. Because the following high-κ dielectric was directly deposited on the bottom TaN electrode, its surface characteristics could be improved to inhibit oxidation and to reduce leakage current by such ammonia (NH_3) plasma treatment [97], [98].

After the gate electrode formation, the shadow mask 2 was aligned to the TaN pattern on substrate, as shown in Fig. 3-3(b), and it defined the region where the gate insulator should be deposited. Therefore, no high-κ dielectric film was deposited on the bottom gate pad, and the extra etching step was unnecessary to open contact for interconnection. The 30-nm lanthanum-yttrium oxide ($LaYO_X$) thin film was deposited as a gate insulator by using an electron-beam evaporation method. The working pressure and the deposition rate were controlled within 5×10^{-5} torr and 0.06 nm/sec, respectively. Subsequently, the gate insulator

of lanthanum-yttrium oxide was annealed at 300 °C in oxygen ambient for 30 minutes to improve its film quality.

Next, the pentacene provided from Aldrich Chemical Company without purification (nearly 98 % purity) was deposited on the gate insulator through the shadow mask 3 by using a thermal evaporation method, as shown in Fig. 3-3(c). It was well known that the deposition pressure, the deposition rate, and the deposition temperature were three critical parameters to the quality of organic pentacene film [99]-[101]. The substrate was heated to 70 °C during the pentacene deposition at a pressure around 3×10^{-6} torr. The thickness of the deposited pentacene film was about 50 nm with a deposition rate of 0.05 nm/sec, monitored by a quartz crystal oscillator. Such deposition condition could significantly decrease the thermal dislocation of pentacene molecules. Moreover, no organic/insulator interface modification [22]-[24] was executed on the insulator surface of the bottom-gate OTFT in this work.

In order to form the ohmic contact, the aurum (Au) metal with a high work function about 5.1 eV, near to the valance band of pentacene crystals, was commonly chosen for the top source/drain electrodes of p-type OTFT device to provide a better injection junction [19], [20]. The top source/drain electrodes were also deposited on the pentacene layer by using a thermal evaporation method, and they were defined by the shadow mask 4, as shown in Fig. 3-3(d). The evaporation pressure and the deposition rate of aurum were 3×10^{-6} torr and 0.05 ~ 0.1 nm/sec, respectively. The channel width (W) and the channel length (L) of the pentacene-based OTFT devices defined by the width and the spacing of the top source/drain electrodes were 1000 μm and 120 μm, respectively. Besides, the Au/$LaYO_X$/TaN metal-insulator-metal (MIM) capacitors were in-situ fabricated with the pentacene-based OTFT device to verify the high-κ LaYOx dielectric properties, as shown in Fig. 3-4. The capacitor area was 200×200 μm^2 defined by the top Au electrode, and the bottom TaN electrodes of the OTFT and the MIM capacitor shared together.

3.3 THERMAL EVAPORATION AND ELECTRON-BEAM EVAPORATION

There are two physical vapor deposition (PVD) ways to deposit the high-κ dielectrics, including evaporation and sputtering methods [102], [103]. Although the sputtering method is a normal processing in industry, the targets of high-κ dielectric and precious materials used in sputter system are too expensive for the consideration to our budget and flexible research. Therefore, we choose the evaporation method to use cheaper granule sources for depositing our high-κ dielectrics, the pentacene channel film, and the precious metal aurum (Au) in this experiment. The evaporation method is that the granule source in tungsten crucible or boat is heated to its melting point to evaporation and then its evaporating molecules would diffuse onto the deposited substrate in a vacuum chamber, as shown in Fig. 3-5(a). The chamber during evaporation procedure must be controlled at a high vacuum pressure (about $10^{-3} \sim 10^{-7}$ torr) to create a long mean free path neglecting the collision among evaporating molecules. The fine uniformity and quality of the deposition film could be obtained because the scattering of the evaporating molecules is small in a high vacuum condition. There are two evaporation systems in our laboratory, the thermal evaporation system and the electron-beam evaporation system, as shown in Figs. 3-5(a) and 3-5(b), respectively.

The thermal evaporation system directly applies a low voltage with a high current on the tungsten boat, and it heats the evaporated source in a vacuum condition to achieve the deposition process. However, the thermal evaporation method could not effectively control its evaporation rate due to the nonuniform heating of the evaporated source in the tungsten boat with a large heating area. Besides, the thermal evaporation method could not apply for lots of materials with high melting points, either. Consequently, the pentacene and the precious metal aurum Au with low melting points of 300 °C and 1064 °C, respectively [104] so that the

thermal evaporation system is suitable for their thin-film deposition. By the way, the holder where is put the deposited substrates is heated to 70 °C for decreasing the thermal dislocation of the pentacene thin-film during depositing [101].

On the other hand, the high-κ dielectrics, the praseodymium oxide (Pr_2O_3) and the lanthanum-yttrium oxide ($LaYO_X$), are deposited by using an electron-beam evaporation system. The electron-beam evaporation system, as shown in Fig. 3-5(b), is using an electron beam with a high energy to evaporate the granule source onto the deposited substrate. Such electron beam emitting from an electron gun in a high vacuum condition could be controlled by the magnetic force to focus it on a small area of the granule source. When a high-energy electron-beam bombards the granule source in the tungsten crucible, its kinetics energy could be translated to the heat energy on a small area, and then be used to melt the granule source to evaporation. Therefore, the electron-beam evaporation method could be applied for the material with a high melting point, and it could well control the deposition rate and the thickness of the deposition film.

In fact, all metal oxides in lanthanides system have hygroscopicity, especially on lanthanum oxide (La_2O_3) [105], [106]. Thus, we preserve these granules, the evaporation materials of lanthanum-yttrium oxide and praseodymium oxide (Pr_2O_3), in a vacuum chamber with a pressure around 10^{-2} torr in normal time. In the beginning of the Pr_2O_3 evaporation process, the low electron emission current must be sustained in a period of time to eliminate the hydroxide on the granules surface of praseodymium oxide. Because much dust (not pure Pr_2O_3 molecules) would be easily evaporated and taken away by a cryopump, the pressure abruptly increases near to 10^{-4} torr in this pre-evaporation condition. The pressure sensor is set close to the beginning of vacuum path. Therefore, the better time to open shutter is when the working pressure comes back to a stable condition below 5×10^{-5} torr. The electron-beam current in this work is set 20 mA with a deposition rate of 0.05 nm/s monitored by a quartz crystal oscillator. On the other hand, although the lanthanum-yttrium oxide ($LaYO_X$) has a

good resistance to moisture [106], we also follow this procedure to obtain a good quality of deposition dielectric. Finally, for the consideration to poor step coverage, the thickness of the gate insulators deposited by using an electron-beam evaporation method is designed closely to that of the poly-Si channel film or the bottom TaN metal gate to avoid the edge leakage.

3.4 DEVICE MEASUREMENT AND PARAMETER EXTRACTION

An automatic measurement system combined a personal computer (PC), Agilent-4156 semiconductor parameter analyzer, Agilent-4285 precision LCR meter, Agilent E5250A low leakage switch mainframe, and a probe station is used to measure I-V and C-V characteristics of fabricated capacitors and thin-film transistors. The metal-insulator-silicon (MIS) and metal-insulator-metal (MIM) capacitors are fabricated to measure their leakage current, dielectric constant values, and breakdown properties. The electrical parameters of thin-film transistors, for examples on the threshold voltage (V_{TH}), the field-effect mobility (μ_{FE}), and the subthreshold swing (*S.S.*), are also extracted to estimate the benefits of integrating high-κ dielectric or nitrogen incorporation.

According to the TFT theory derived in the chapter 2, the drain current in linear regime ($I_{DS,lin}$) could be approximated as the following equation

$$I_{DS,lin} = \mu_{FE,lin} C_{ins} \frac{W}{L}\left[\left(V_{GS} - V_{TH,lin}\right)V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right] \tag{2-9}$$

, where C_{ins} is the gate capacitance density of the insulator layer, W is the channel width, L is the channel length, V_{GS} is the gate-source voltage, and V_{DS} is the drain-source voltage. In the linear regime, $V_{DS} < V_{GS} - V_{TH,lin}$, and the drain current ($I_{DS,lin}$) could be described as

$$I_{DS,lin} = \mu_{FE,lin} C_{ins} \frac{W}{L}\left(V_{GS} - V_{TH,lin}\right)V_{DS} \tag{3-1}$$

Thus, the transconductance (G_m) in the linear regime is given by

$$G_m = \frac{\partial I_{DS,lin}}{\partial V_{GS}} = \mu_{FE,lin} C_{ins} \frac{W}{L} V_{DS} \tag{3-2}$$

Therefore, the field-effect mobility in the linear regime ($\mu_{FE,lin}$) could be obtained as

$$\mu_{FE,lin} = \frac{L}{W} \frac{1}{C_{ins}} \frac{1}{V_{DS}} G_m \Big|_{V_{DS} \sim 0.1V} \tag{3-3}$$

, where the drain-source voltage (V_{DS}) is usually set at 0.1 V. Because the inversion carriers in the active channel layer could be easily drained out with enough high carrier mobility at low drain bias, we calculate the field-effect mobility in the linear regime ($\mu_{FE,lin}$) for low-temperature polycrystalline silicon (LTPS) TFT device. The transfer curve of LTPS TFT device, drain current ($I_{DS,lin}$) versus gate-source voltage (V_{GS}), is measured at V_{DS} = 0.1 V, and then $\mu_{FE,lin}$ could be obtained by using Eq. (3-3).

For extraction convenience, the threshold voltage (V_{TH}) is defined as the gate voltage required a normalized drain current of $I_{DS,N} = (W/L) \times$ 100 nA at V_{DS} = 0.1 V. The ON/OFF current ratio ($I_{ON,\,max}/I_{OFF,\,min}$) and the subthreshold swing (*S.S.*) present the switching and the gate-controlled capabilities of TFT device, respectively. In this work, the ON/OFF current ratio of LTPS TFT device is defined as that ratio of the maximum on-state current to the minimum off-state current at V_{DS} = 1 V. The subthreshold swing is measured at the inverse of the maximum slope in the plot of drain current (in denary logarithm) versus gate-source voltage (V_{GS}). All device parameters extracted from the transfer characteristic plot are displayed in Fig. 3-6 and their detail derivations are shown below.

By integrating the depletion charges (Q_{dep}) in active channel with the charge-sheet approximation [94] in chapter 2, the subthreshold current ($I_{DS,SUB}$) in the subthreshold region (at a small V_{DS} ~ 0.1 V) could be derived as the following equation

$$I_{DS,SUB} = \mu_{FE} C_{ins} \frac{W}{L} \sqrt{\frac{q\varepsilon_{Si} N_B}{2\psi_S}} \left(\frac{k_B T}{q}\right)^2 \left(\frac{n_i}{N_B}\right)^2 \exp\left(\frac{q\psi_S}{k_B T}\right) \tag{2-15}$$

, where the surface potential ψ_S could be expressed in terms of V_{GS}

$$V_{GS} = V_{fb} + \psi_S + \frac{\sqrt{2\varepsilon_{Si} q N_B \psi_S}}{C_{ins}}. \tag{3-4}$$

Considering $\psi_S \sim 2\psi_B$ in the subthreshold region, the Eq. (3-4) could be expand to the square-root term around $2\psi_B$ as

$$V_{GS} = V_{fb} + 2\psi_B + \frac{\sqrt{4\varepsilon_{Si} q N_B \psi_B}}{C_{ins}} + \left(1 + \frac{\sqrt{\varepsilon_{Si} q N_B / 4\psi_S}}{C_{ins}}\right)\left(\psi_S - 2\psi_B\right) = V_{TH} + m\left(\psi_S - 2\psi_B\right) \tag{3-5}$$

, where the body-effect coefficient m is

$$m = 1 + \frac{\sqrt{\varepsilon_{Si} q N_B / 4\psi_S}}{C_{ins}} = 1 + \frac{C_{dep}}{C_{ins}} \tag{3-6}$$

and C_{dep} is the depletion capacitance density. Substituting Eq. (3-6) into Eq. (2-15) yields the subthreshold current as a function of V_{GS}

$$I_{DS,SUB} = \mu_{FE} C_{ins} \frac{W}{L}(m-1)\left(\frac{k_B T}{q}\right)^2 \exp\left(\frac{q\left(V_{GS} - V_{TH}\right)\psi_S}{m k_B T}\right). \tag{3-7}$$

Consequently, the subthreshold swing (*S.S.*) could be presented as the following equation

$$S.S. = \left[\frac{d \log_{10} I_{DS,SUB}}{dV_{GS}}\right]^{-1} = 2.3\frac{m k_B T}{q} = 2.3\frac{k_B T}{q}\left(1 + \frac{C_{dep}}{C_{ins}}\right). \tag{3-8}$$

Consider the effective interface trap-state densities $N_{it} = qC_{it}$ and substituting it into Eq. (3-8), the subthreshold swing (*S.S.*) neglected the depletion charges ($Q_{dep} = q \times C_{dep}$) could be rewritten as

$$S.S. = \left[\frac{d \log_{10} I_{DS,SUB}}{dV_{GS}}\right]^{-1} = 2.3\frac{k_B T}{q}\left(1 + \frac{C_{dep} + C_{it}}{C_{ins}}\right) \sim 2.3\frac{k_B T}{q}\left(1 + \frac{qN_{it}}{C_{ins}}\right). \tag{3-9}$$

Therefore, the maximum interface states density ($N_{SS,max}$) presents the interface quality between the gate dielectric and the active channel layer of TFT device could be calculated from the *S.S.* without the depletion capacitance as

$$N_{SS,\max} = \left[\frac{S.S.}{2.3} \left(\frac{q}{k_B T} \right) - 1 \right] \left(\frac{C_{OX}}{q} \right). \tag{3-10}$$

In pentacene-based organic TFT device case, because its inversion carriers in the active channel could not be easily drained out the device with a low carrier mobility at a low drain bias, its parameters are usually extracted in the saturation regime ($V_{DS} > V_{GS} - V_{TH}$) as

$$I_{DS,sat} = \frac{1}{2} \mu_{FE,sat} C_{ins} \frac{W}{L} \left(V_{GS} - V_{TH,sat} \right)^2. \tag{2-24}$$

The Eq. (2-24) could be transposed by V_{GS} as

$$V_{GS} = V_{TH,sat} + \sqrt{2 I_{DS,sat}} \sqrt{\frac{L}{\mu_{FE,sat} C_{ins} W}}. \tag{3-11}$$

Hence, the threshold voltage ($V_{TH,sat}$) could be determined from the maximum slope in the square-root plot ($I_{DS}^{1/2}$–V_{GS}) of the transfer characteristic, and we fit a straight line to the $I_{DS}^{1/2}$–V_{GS} curve at the point extrapolated to I_{DS} = 0. Following, substitute the obtained V_{TH} from Eq. (3-11) back into Eq. (2-24), and then the field-effect mobility in the saturation regime ($\mu_{FE,sat}$) of the organic TFT device could be obtained as

$$\mu_{FE,sat} = 2 I_{DS,sat} \frac{L}{C_{ins} W} \frac{1}{\left(V_{GS} - V_{TH,sat} \right)^2}. \tag{3-12}$$

Strictly speaking, the Eq. (3-12) is valid only when the saturation mobility is constant. In fact, $\mu_{FE,sat}$ is dependent on the gate-source bias (V_{GS}). The Eq. 3-12 is only used to estimate an approximate value for the field-effect mobility calculation on organic TFT devices.

3.5 MATERIAL ANALYSIS

The X-ray diffraction (XRD) experiments (RU-H3R, Rigaku, Japan) are performed by using a Dmmax-B diffractometer with a 0.02-degree beam divergence at 30 keV and 30 mA with Cu-Kα radiation. The X-ray diffraction is a powerful non-destructive technique for characterizing crystalline materials. It provides information on structures, phases, preferred crystal orientations (textures), and other structural parameters, such as average grain size, crystallinity, strain, and crystal defects. The peaks of X-ray diffraction are produced by the constructive interference of the monochromatic beam scattered from each set of lattice planes at specific angles. The intensity of every peak is determined by the atomic decoration within the lattice planes. Consequently, the X-ray diffraction pattern is the fingerprint of the periodic atomic arrangements in a given material. In this work, we use this XRD system to analyze the crystallinity of the pentacene film deposited on gate insulator.

The cross section of the fabricated samples could be observed by using a transmission electron microscope (TEM). The principle of TEM is similar to that of optical microscope. In TEM, observation is made in an ultra high vacuum condition, where an electron beam is focused onto the sample by using electromagnetic lenses. Because the wavelength of the electron beam is less than that of visible spectra, the resolution of TEM is higher than that of the conventional optical microscope. In this work, the deposited high-κ dielectric is prepared by using a focus ion beam (FIB) system with the model Nova 200 of FEI Company, and then it is transferred to JEOL JME-3000F TEM system for observing its thickness.

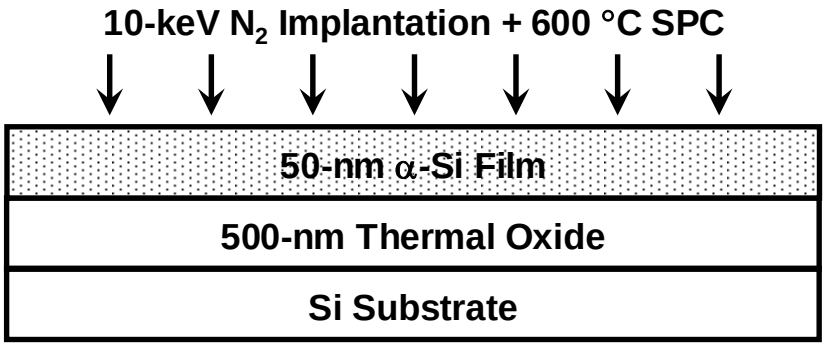
The Auger electron spectroscopy (AES) (Microlab 350, Thermal VG Scientific Company, England) is used to analyze the composition of our deposited high-κ dielectrics, praseodymium oxide (Pr_2O_3) and lanthanum-yttrium oxide ($LaYO_X$). The X-ray photoelectron spectroscopy (XPS), also known as the electron spectroscopy for chemical analysis (ESCA),

is a quantitative spectroscopic technique to measure elemental composition, empirical formula, chemical state, and electronic state of elements existed within a material. Samples would irradiate with X-ray, and their emitted photoelectrons with kinetic energy (KE) are detected. The measured kinetic energy (KE) is given by

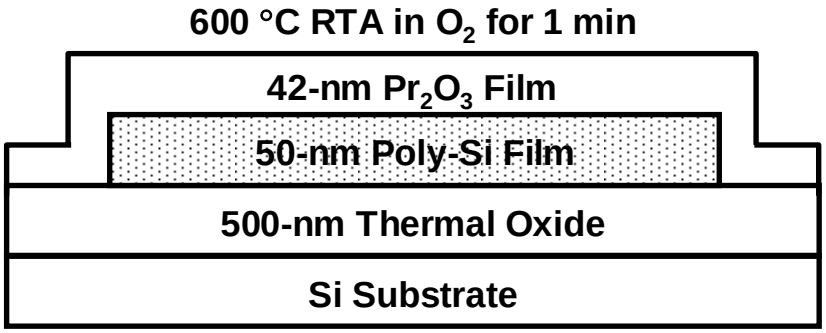
$$KE = h\nu - BE - \phi_S \tag{3-13}$$

, where $h\nu$ is the photon energy, BE is the binding energy of the atomic orbital where electron generates, and ϕ_S is the spectrometer work function. The binding energy is the minimum energy to break the chemical bond inherent in each bond of the measured molecule. Thus, the binding states could be identified by the positions of the binding energies where the peaks appear. In the case that the peak position is different from the expected positions, the chemical bond states are discussed the amount of shifting to the higher or the lower energy side.

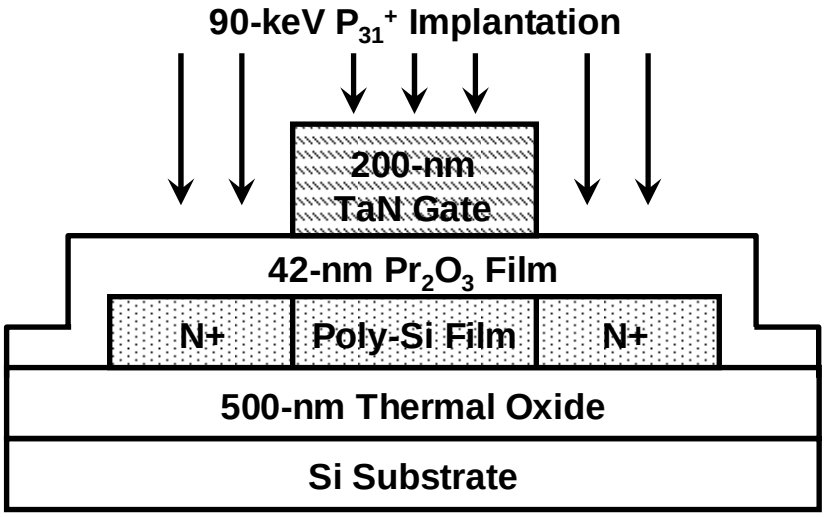
Atomic force microscopy (AFM) (Dimension 5000, Veeco, USA) is used to study the surface morphology with a molecular or atomic resolution. The principle could be described as the force acting on the scanning tip via detecting the deflection of the moving cantilever. The interaction force between the scanning tip and the sample surface is the essential parameter to determine AFM scanning mode. By decreasing the gap between the scanning tip and the sample surface, the interaction force can change from attractive force to repulsive force. With further reducing the gap, the repulsive force can dramatically increase due to the Pauli exclusion principle and become the dominant interaction. With varying the interaction force, the cantilever deflects in different ways to bend upward, downward, or twisted. In this study, we use the tapping mode to explore the surface morphology of the pentacene film on gate insulator.



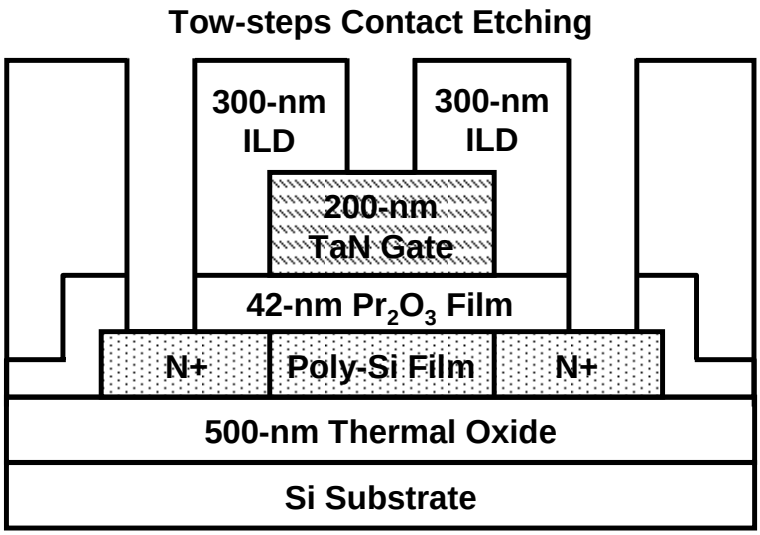
(a) Thermal oxidation, α-Si deposition, nitrogen implantation, and SPC annealing.



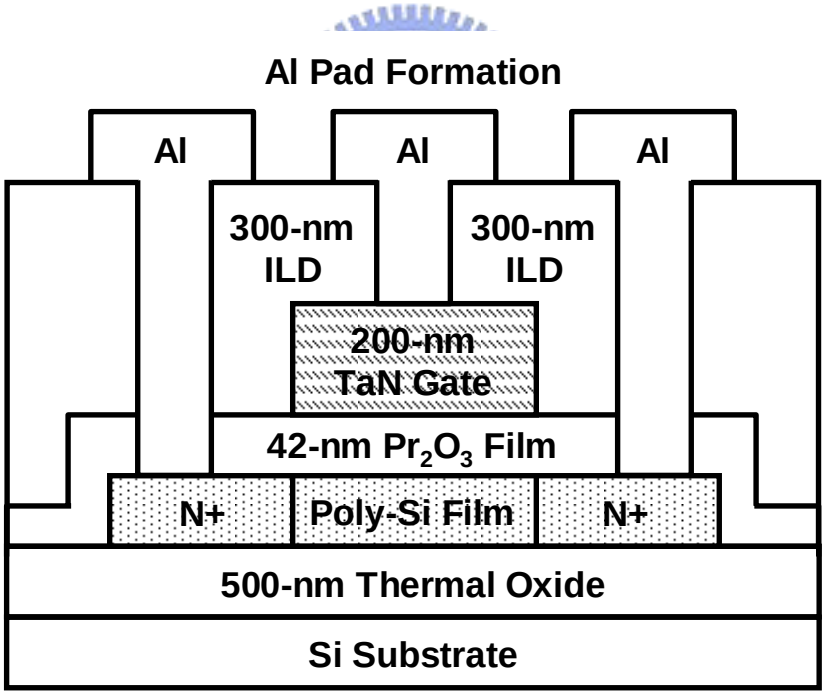
(b) Active region patterning, Pr_2O_3 deposition, and Pr_2O_3 annealing.



(c) TaN gate deposition and patterning, and then self-align implantation and activation.

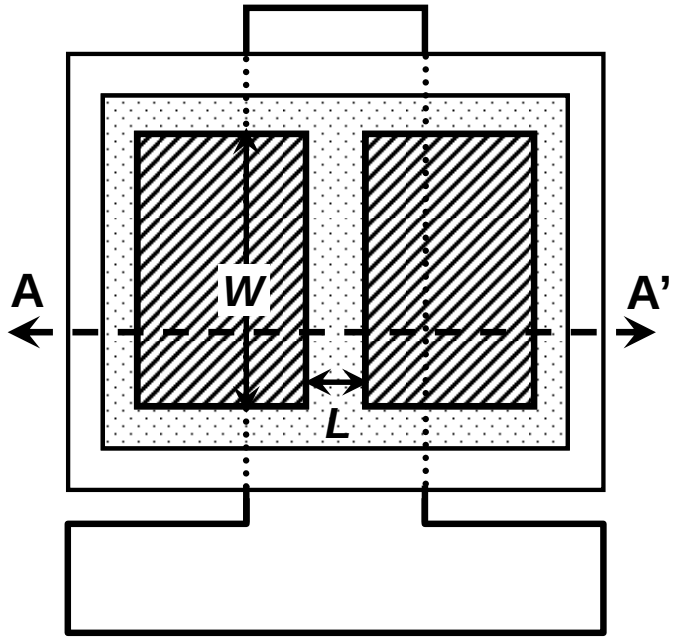


(d) ILD deposition and contact hole opening.

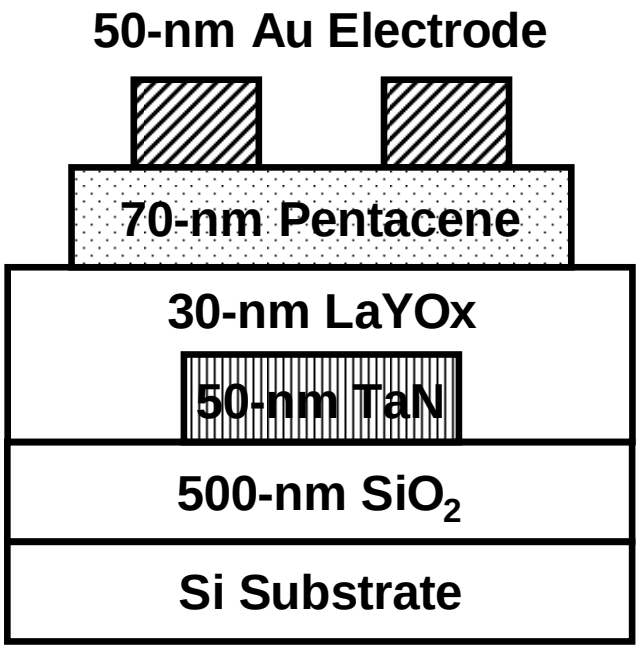


(e) Al deposition and patterning.

Fig. 3-1. The main process steps of the Pr_2O_3 poly-Si TFT with nitrogen-implanted poly-Si film.

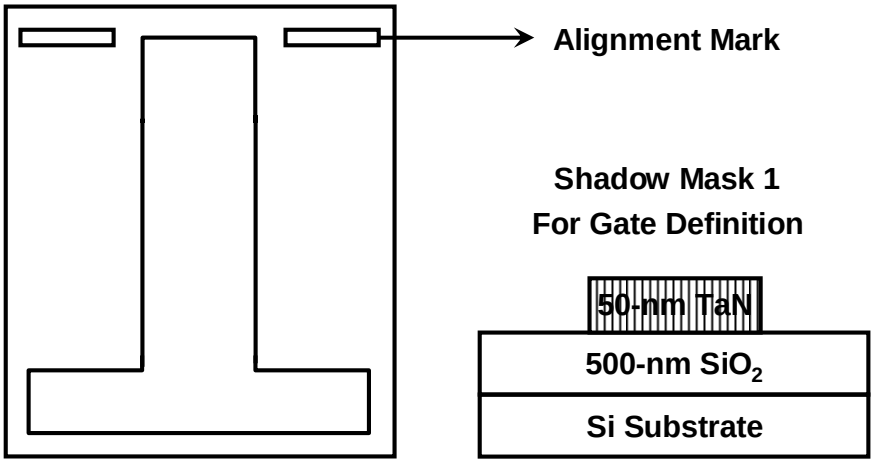


(a)

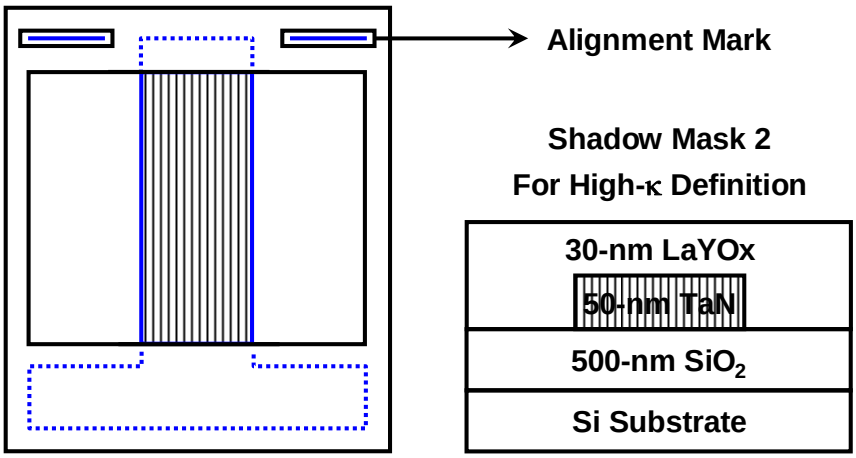


(b)

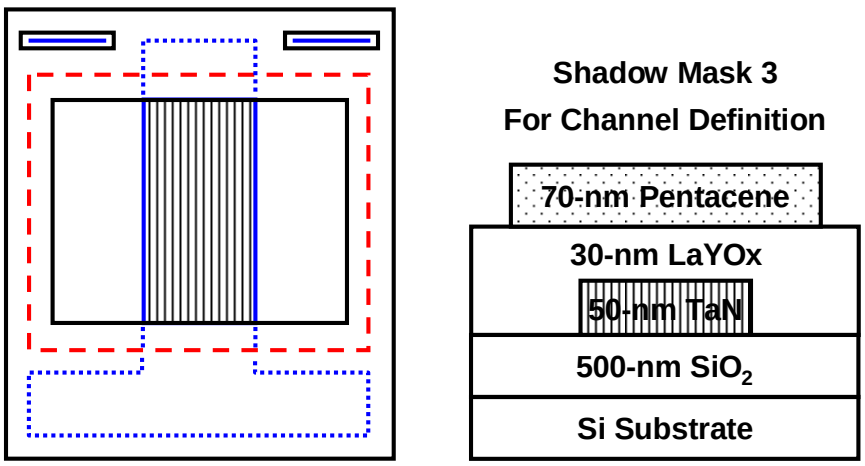
Fig. 3-2. (a) The top view of the fabricated pentacene-based organic thin-film transistor (OTFT). (b) The cross-sectional structure of the pentacene OTFT with high-κ $LaYO_X$ gate insulator along AA' dashed line in (a).



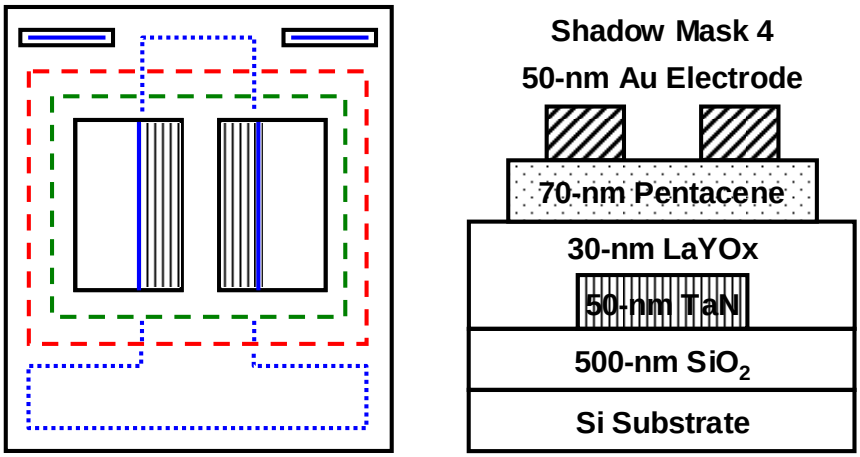
(a) Shadow mask 1 for TaN gate deposition.



(b) Shadow mask 2 with the TaN pattern alignment for high-κ $LaYO_X$ deposition.



(c) Shadow mask 3 with the TaN pattern alignment for pentacene deposition.



(d) Shadow mask 4 with the TaN pattern alignment for Au electrode deposition.

Fig. 3-3. The schematic view of the shadow masks corresponding to their process for pentacene-based OTFT fabrication.

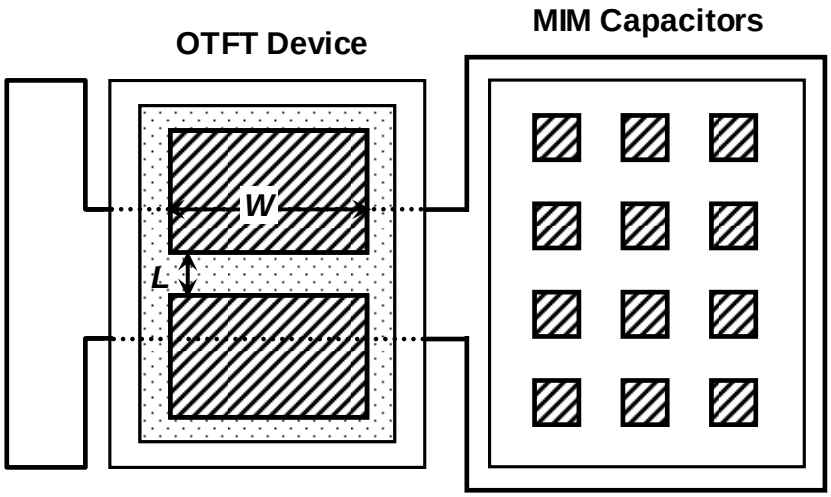


Fig. 3-4. The schematic view of the Au/$LaYO_X$/TaN metal-insulator-metal (MIM) capacitors in-situ fabricated with OTFT device.

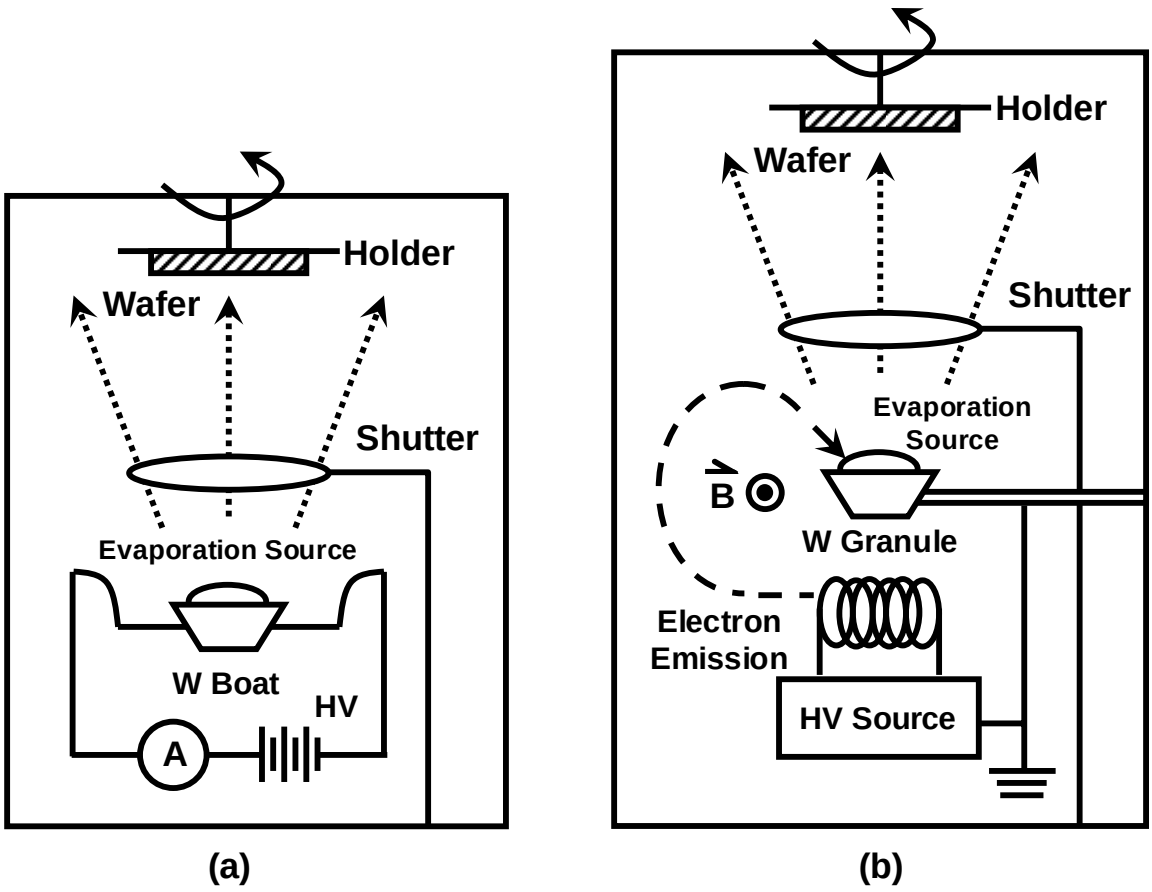


Fig. 3-5. The schematic views of (a) the thermal evaporation system, and (b) the electron-beam evaporation system.

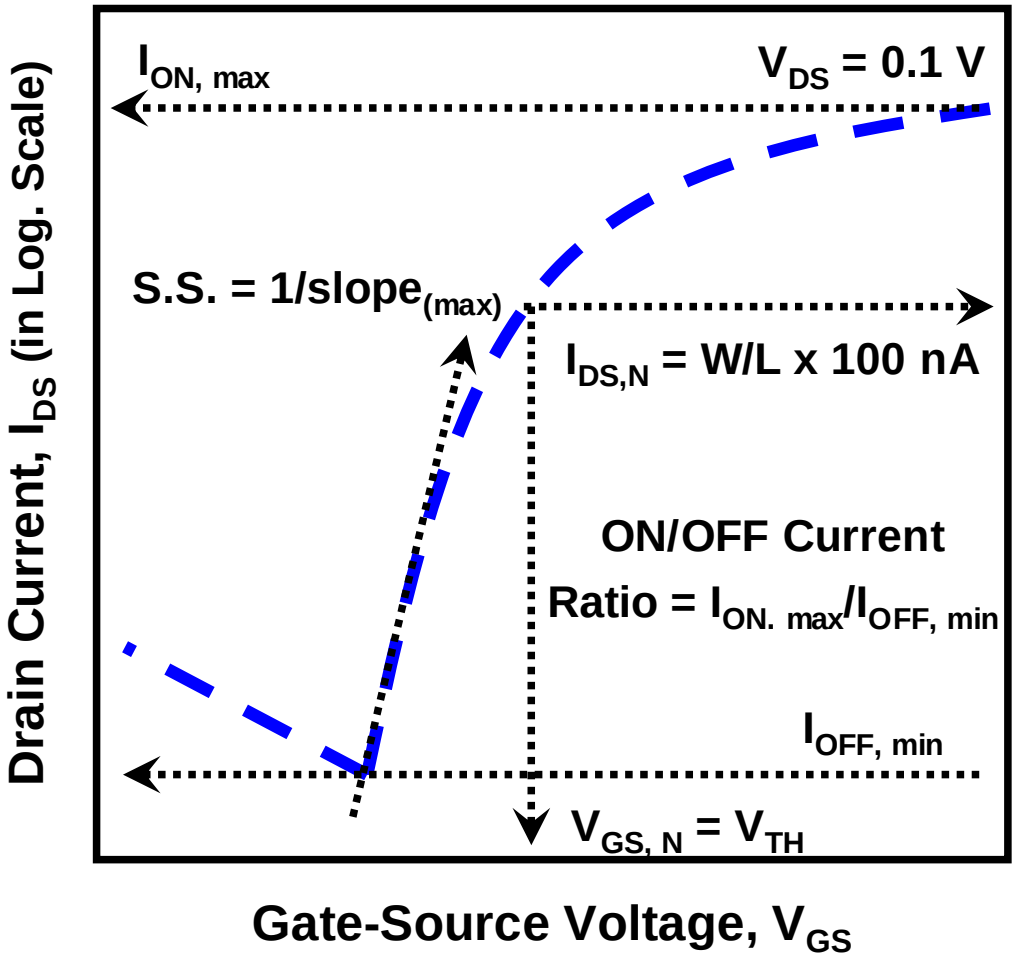


Fig. 3-6. The device parameters, including threshold voltage (V_{TH}), subthreshold swing (*S.S*), and ON/OFF current ratio, extracted from the transfer characteristic plot.

CHAPTER 4

RESULTS AND DISCUSSION

This chapter divides into two main categories, which contain the characteristics of the low-temperature polycrystalline silicon (LTPS) praseodymium oxide (Pr_2O_3) thin-film transistors (TFTs) with various nitrogen dosages and those of the organic thin-film transistor (OTFT) with a lanthanum-yttrium oxide ($LaYO_X$) gate insulator. The quality of the high-κ dielectric films is examined by using the metal-insulator-silicon (MIS) and the metal-insulator-metal (MIM) capacitors, including the measurements of the capacitance-voltage (*C*-*V*) curves and the current density-voltage (*J*-*V*) curves. The composition of these two high-κ gate dielectrics, Pr_2O_3 film and $LaYO_X$ film, is presented by using the X-ray photoelectron spectroscopy (XPS) analysis. In terms of the analysis on the electrical parameters, for examples on the threshold voltage (V_{TH}), the field-effect mobility (μ_{FE}), and the subthreshold swing (*S.S.*), the benefits of integrating high-κ dielectrics into these two kinds of thin-film transistors are discussed. Moreover, the effects on various nitrogen dosages in polycrystalline silicon film subjected to conventional solid phase crystallization (SPC) annealing are also investigated by using the hot-carrier stress testing on the LTPS TFTs with the Pr_2O_3 gate dielectric.

4.1 PROPERTIES OF LOW-TEMPERATURE POLYCRYSTALLINE SILICON PRASEODYMIUM OXIDE THIN-FILM TRANSISTORS WITH VARIOUS NITROGEN DOSAGES

4.1-1 Characteristics of Pr_2O_3 MIS Capacitors

Firstly, the thickness of the deposited Pr_2O_3 gate insulator is determined by the cross-sectional transmission electron microscope (TEM) image of the gate structure of the fabricated LTPS TFT, as shown in the left inset of Fig. 4-1. The thickness of the praseodymium oxide (Pr_2O_3) gate dielectric is about 42 nm after a rapid-thermal-annealing (RTA) treatment in oxygen ambient, and the thickness of polycrystalline silicon (poly-Si) channel layer is around 50 nm. The current density of the 42-nm Pr_2O_3 gate dielectric on p-type silicon substrate has a huge increase to 1 μA/cm^2 under a negative bias over the electric field of 3 MV/cm. Applying the negative bias on the TaN electrode means the electrons injection from the gate to the substrate. When applying a positive bias, which is minority carriers (electrons) injection from the silicon substrate to top metal, the current density was below 1 μA/cm^2 until the breakdown larger than 7 MV/cm.

Fig. 4-1 shows the typical capacitance-voltage (*C*–*V*) characteristic of the praseodymium oxide (Pr_2O_3) metal-insulator-silicon (MIS) capacitor at 1 MHz from –4 V to 4 V. The accumulation capacitance density (C_{acc}) is 432 nF/cm^2 at the applied voltage of V_{APP} = –4 V. According to the TEM image of the 42-nm thickness of the Pr_2O_3 dielectric on the polycrystalline silicon (poly-Si) film, the equivalent-oxide thickness (EOT) and the effective dielectric constant value (κ) extracted are 8 nm and 25, respectively, from the accumulation capacitance density. Here, the praseodymium silicate formed an interfacial layer between the praseodymium oxide film and the poly-Si film has been included into EOT and κ calculation.

By the way, the hysteresis of the C–V curves is about 30 mV after 100-times –4-to-4 V sweeping, and its value could be neglected. The praseodymium oxide seems a good candidate for the gate dielectric application since the Pr_2O_3 MIS capacitor represents a high capacitance density and a low leakage current. Therefore, it could be expected that the poly-Si TFT with the Pr_2O_3 gate dielectric has a well gate controllability resulting in better electrical characteristics, compared to that with conventional plasma TEOS oxide as gate dielectric.

The chemical composition of the Pr_2O_3 gate dielectric film on silicon substrate is determined by an X-ray photoelectron spectroscopy (XPS) analysis. The XPS spectra of Pr 3d and O 1s core level spectral regions are shown in Fig. 4-2. The Pr 3d signals of the Pr_2O_3 film consist of the binding energy splitting of the $3d_{3/2}$ and the $3d_{5/2}$ spin-orbit doublets. The main Pr 3d XPS peak is centered at 953.6 eV and its spin-orbit component is also separated at 933.2 eV. The binding energy and the spin-orbit component associated with the present Pr_2O_3 features are in agreement with the XPS reference book [107]. It reveals that the Pr_2O_3 phase formation on silicon substrate is the same as that on in-situ fabricated LTPS TFTs. Besides, the shape of O 1s is also shown in the inset of Fig. 4-2. The XPS peak of O 1s core level spectral at higher binding energy of 530.1 eV could be regarded as the Pr-O bonding. A broad signal existed at the lower binding energy of 533 eV is attributed to the overlap of various components associated with oxide and hydroxide on the surface of Pr_2O_3 film.

4.1-2 Characteristics of Pr_2O_3 Poly-Si TFTs With Nitrogen Implantation

Fig. 4-3 shows the transfer characteristics (I_{DS}–V_{GS}) of the Pr_2O_3 polycrystalline silicon (poly-Si) TFTs with various nitrogen dosages (D_N) of zero (control sample), 5×10^{12} cm^{-2}, and 5×10^{13} cm^{-2}, measured in linear regime at V_{DS} = 0.1 V. The channel length (L) and the channel width (W) of the Pr_2O_3 poly-Si TFT are 10 μm and 5 μm, respectively. When the implanted nitrogen dosage increases to 5×10^{12} cm^{-2}, the electrical performances of the Pr_2O_3

poly-Si TFT could be improved, including the decrease of the threshold voltage (V_{TH}) and the increase of the transconductance (G_m), compared to those of the control sample ($D_N = 0\,cm^{-2}$). The subthreshold swings (*S.S.*) of these Pr_2O_3 poly-Si TFTs defined by the Eq. (3-8) seem no change with various nitrogen dosages.

As the papers reported on [108]-[110], the interface trap states and the grain boundary trap states dominate the electrical characteristics of poly-Si TFT. The deep trap states in the grain boundaries and in the interface mainly affect on the threshold voltage. Besides, the tail states in the interface states and in the grain boundaries mainly contribute to the degradation of the transconductance. The subthreshold swing mainly depends on the deep interface trap states and on the bulk states in intra-grain defects. These relationships between trap states and device parameters of LTPS TFT are summarized in Table 4-1. Compared with Table 4-1 and Fig. 4-3, such the same subthreshold swings of three TFT devices indicate that their interface trap states at the Pr_2O_3 gate dielectric/poly-Si channel interface are not changed with various nitrogen dosages. Further, the transconductance and the threshold voltage of three TFT devices are fluctuated with various nitrogen dosages. Therefore, the electrical improvement of the Pr_2O_3 poly-Si TFT by incorporating nitrogen could be attributed to the reduction of the grain boundary trap states within the poly-Si film during conventional solid-phase crystallization (SPC) annealing. However, when the nitrogen dosage increases to $5 \times 10^{13}\,cm^{-2}$, the electrical characteristics of the Pr_2O_3 poly-Si TFT would be degraded with larger threshold voltage and smaller transconductance. The overdose of nitrogen implantation ($D_N = 5 \times 10^{13}\,cm^{-2}$) in amorphous silicon (α-Si) film would obstruct α-Si film crystallized to poly-Si film, compared to that without nitrogen implantation (control sample). Therefore, the drain current of the Pr_2O_3 poly-Si TFT without large-size poly-Si grains is decreased.

Fig. 4-4 compares the transfer characteristics (I_{DS}–V_{GS}) of the Pr_2O_3 poly-Si TFTs with the nitrogen dosages of $0\,cm^{-2}$ and $5 \times 10^{12}\,cm^{-2}$ under $V_{DS} = 0.1$ V and 1 V. The inserted table summarizes the electrical parameters of these two devices. The electrical characteristics of the

control Pr_2O_3 poly-Si TFTs without nitrogen dosage is inferior to those with a nitrogen dosage of 5×10^{12} cm^{-2}. The threshold voltage (V_{TH}) and the field-effect mobility (μ_{FE}) could be significantly improved from 2.15 to 1.9 V and from 34 to 47.4 cm^2/V-s, respectively. In addition, both the subthreshold swings (*S.S.*) and the ON/OFF current ratios of them are almost the same with the values about 242 mV/dec and over the sixth power of ten, respectively. Besides, the gate-induced drain leakage (GIDL) current [111], [112] at V_{DS} = 1 V and V_{GS} = 0 V also could be suppressed by a half-order magnitude by using the nitrogen implantation with a suitable dosage of 5×10^{12} cm^{-2}. As well-known, the GIDL current of poly-Si TFTs is an off-state leakage current which is generated from the field-enhanced emission through the trap states and then resulted in the traps assisted band-to-band tunneling current near the drain junction under a high drain field. Implanting a moderate dosage of nitrogen atoms into the amorphous silicon film could effectively passivate the trap states at grain boundaries during SPC annealing. Therefore, the Pr_2O_3 poly-Si TFT with implanting a moderate nitrogen dosage of 5×10^{12} cm^{-2} has less grain boundary trap states in its poly-Si channel than the control sample so that the GIDL current could be reduced, especially under a high drain-voltage operation.

The output characteristics (I_{DS}–V_{DS}) of the Pr_2O_3 poly-Si TFTs with nitrogen dosages of zero and 5×10^{12} cm^{-2} are shown in Fig. 4-5. The driving current of the Pr_2O_3 poly-Si TFT with a nitrogen dosage of 5×10^{12} cm^{-2} has about 40 % improvement at V_{GS} = 4 V, compared to that of the control sample. The pervious studies [16], [82]-[86] have been reported that the poly-Si TFT with a high-κ gate dielectric exhibited a high gate capacitance density could induce more charge carriers and quickly fill the trap states in poly-Si channel to improve device electrical characteristics due to the well gate controllability. However, in this work, using the nitrogen implantation technique in the Pr_2O_3 poly-Si TFTs would further passivate these grain boundary trap states in poly-Si channel film and improve the device performance.

The electrical reliability on the Pr_2O_3 poly-Si TFTs with and without the nitrogen

implantation is investigated in Fig. 4-6. All devices are biased at V_{GS} = V_{DS} = 4 V, under a hot-carrier stress condition. The degradation of the drain current (I_{DS}) is defined as $\Delta I_{DS}/I_{DS,0}$, where the $\Delta I_{DS} = I_{DS,S} - I_{DS,0}$, $I_{DS,0}$ is the initial drain current, and $I_{DS,S}$ is the drain current for each stress time. The I_{DS} degradation of the Pr_2O_3 poly-Si TFT with a nitrogen dosages (D_N) of 5×10^{12} cm^{-2} is about 5 % after 1000-s hot-carrier stress, which is superior to that without nitrogen implantation (control sample). The I_{DS} degradation of the control sample is saturated to −70 % after 200-s hot-carrier stress. It has been reported that the hot-carrier stress easily breaks the weak Si-Si bonds and Si-H bonds (with the bonding energy of 70 kcal/mol [113]) to generate the interface states and the grain boundary trap states in poly-Si film [108], [109]. If the appropriate nitrogen atoms are implanted into α-Si film during solid phase crystallization (SPC) annealing, the stronger Si-N bonds with a higher bonding energy of 81 kcal/mol [113] would replace the weak Si-Si and Si-H bonds to excellent hot-carrier endurance. It is noted that the Pr_2O_3 poly-Si TFT with a nitrogen dosage of 5×10^{12} cm^{-2}, even under a higher stress current (see Fig. 4-3), has a better hot-carrier stress immunity than that without nitrogen implantation. On the other hand, as to the Pr_2O_3 poly-Si TFT with a nitrogen dosage of 5×10^{13} cm^{-2}, its I_{ON} degradation is saturated at −50 % after 400-s hot-carrier stress, which seems better than that of the control sample (D_N = 0 cm^{-2}). This reason could be attributed to that the overdose of nitrogen implantation would restrict α-Si film crystallization and result in the inferior electrical characteristics of the Pr_2O_3 poly-Si TFT, as shown in Fig. 4-3. The hot-carrier stress degradation on TFT device with a nitrogen dosage of 5×10^{13} cm^{-2} is more alleviative than control sample under the same stress bias. In a brief summary, the Pr_2O_3 poly-Si TFT with applicable nitrogen incorporation in poly-Si channel has a better immunity on the hot-carrier stress, compared to the control sample.

Table 4-2 compares all electrical parameters of the SPC poly-Si TFTs with various gate dielectrics, including TEOS oxide [60], aluminum oxide (Al_2O_3) [85], lanthanum-aluminum oxide ($LaAlO_3$) [86], and praseodymium oxide (Pr_2O_3). The subthreshold swing of the poly-Si

TFTs with high-κ dielectrics has a gradual improvement from 1.97 V to 0.24 V, compared to that with the TEOS dielectric [60]. A large gate capacitance density (C_{ins}) could induce more inversion charges to minimize the effect on depletion charges and interface charges, as shown in Eq. 3-8.

$$S.S. = \left[\frac{d \log_{10} I_{DS,SUB}}{dV_{GS}} \right]^{-1} = 2.3 \frac{mk_BT}{q} = 2.3 \frac{k_BT}{q} \left(1 + \frac{C_{dep} + C_{it}}{C_{ins}} \right). \quad (3\text{-}8)$$

The body-effect coefficient m could be smaller by large gate capacitance density (C_{ins}). The better switching characteristic, corresponding to the good threshold swing, makes the smaller threshold voltage at the same turn-on current condition. Besides, the reason why the poly-$Si_{0.85}Ge_{0.15}$ TFT with an Al_2O_3 gate dielectric has a higher mobility of 47 cm^2/V-s is that the poly-$Si_{0.85}Ge_{0.15}$ film with a narrow energy bandgap easily induces more carrier charges in its channel [85]. However, the narrow energy bandgap also induces a large leakage current so that the ON/OFF current ratio (I_{ON}/I_{OFF}) of the poly-$Si_{0.85}Ge_{0.15}$ TFT is not large as the other samples. The control sample (D_N = 0 cm^{-2}) in this work has the same characteristics compared to the $LaAlO_3$ poly-Si TFT, expect the threshold voltage. In ref. [86], the authors integrate the aluminum metal gate with a low work function value into their $LaAlO_3$ poly-Si TFT, but the aluminum (Al) metal gate is deposited after the dopant activation is complete. In this work, we use the refractory metal of TaN as the metal gate, which could sustain an activation temperature of 600 °C to achieve the self-align implantation process. However, the work function of the TaN metal is around 4.5 eV higher than that of the Al metal of around 4 eV. Therefore, our threshold voltage of the control sample is slightly larger than that of the $LaAlO_3$ poly-Si TFT. In this work, the LTPS TFTs with 42-nm Pr_2O_3 gate dielectric has an equivalent-oxide thickness (EOT) of 8 nm. Because of the roughness of poly-Si and the fast deposition rate of TEOS oxide, the conventional LTPS TFTs with 8-nm TEOS gate dielectric is difficult to fabricate and it would cause large gate leakage current during operation. Finally,

as regards the Pr_2O_3 poly-Si TFTs with various nitrogen dosages, their threshold swings are controlled within 300 mV, which verify the well gate controllability due to the integration of the high-κ gate dielectric process. The Pr_2O_3 poly-Si TFT with an overdose nitrogen implantation has a poor crystallization on poly-Si channel film so that its mobility, threshold voltage, and ON/OFF current ratio are inferior to those of the other two devices in this work.

4.1-3 Summary

High-performance low-temperature polycrystalline silicon (LTPS) TFTs integrated nitrogen implantation and praseodymium oxide (Pr_2O_3) gate dielectric are demonstrated in this section. High gate capacitance density (~ 432 nF/cm^2) and high breakdown electrical field (> 3 MV/cm) are introduced by using the MIS capacitor with a 42-nm Pr_2O_3 gate dielectric and the TaN gate metal. The electrical characteristics of the poly-Si TFT with a Pr_2O_3 gate dielectric could be improved without additional plasma treatment due to the well gate controllability, for example, over six-order magnitudes of the ON/OFF ratio. Moreover, the threshold voltage (V_{TH}) and the field-effect mobility (μ_{FE}) of the Pr_2O_3 poly-Si TFT with a nitrogen dosage of 5×10^{12} cm^{-2} progress to 1.9 V and 47.4 cm^2/V-s, respectively. Based on the hot-carrier stress testing, we know that implanting nitrogen atoms in poly-Si film could form the stronger Si-N bonds during SPC annealing and passivate the trap states in poly grains and in grain boundaries. Therefore, the proposed Pr_2O_3 poly-Si TFT with suitable nitrogen incorporation would be a promising candidate for matrix devices and high-speed driving circuit applications in the near future.

4.2 PROPERTIES OF PENTACEBE-BASED ORGANIC THIN-FILM TRANSISTORS WITH LANTHANUM-YTTRIUM OXIDE

4.2-1 Characteristics of $LaYO_X$ MIM Capacitor

In order to verify the electrical properties of the lanthanum-yttrium oxide ($LaYO_X$) film, the capacitance-voltage (*C*–*V*) characteristic and the current density (*J*–*V*) curve are measured by using the Au/$LaYO_X$/TaN metal-insulator-metal (MIM) capacitor, as shown in Fig. 4-7. The area of this MIM capacitor is defined by a shadow mask in a square pattern of 200 × 200 μm^2. The capacitance density is measured from –5 V to 5 V sweeping at 100 kHz. The MIM capacitor with a 30-nm $LaYO_X$ insulator has a high capacitance density of 420 nF/cm^2 and a low leakage current density of 1 $\mu A/cm^2$ under the applied voltage of 5 V on the aurum (Au) electrode. It also shows a small tunability of 2 % variation from 0 V to –5 V, insuring the voltage independence on capacitance density and making more predictable for organic thin-film transistor (OTFT) operation. In terms of the capacitance-voltage calculation, the equivalent-oxide thickness (EOT) and the effective dielectric constant value (κ) of the 30-nm $LaYO_X$ gate dielectric on tantalum nitride (TaN) electrode are around 8.2 nm and 14.2 at the applied voltage of –4 V, respectively. The previous studies have been reported that the 5-nm $LaYO_X$ thin film with 40-to-60 % yttrium doped concentration annealed at 600 °C has a high κ value of 29 [80], [81], [105], [106]. The dielectric constant value of our nonstoichiometric $LaYO_X$ thin film is lower than that of the previous reports because the high-κ $LaYO_X$ film is annealed at a low temperature of 300 °C in this work.

Two distinct behaviors in the *J*–*V* plot are observed, where the leakage current density keeps lower than 2×10^{-8} A/cm^2 in the low voltage region (below 3 V) but rapidly increases in the high voltage region (above 3 V). It is well known that the former region could be ascribed to the dielectric relaxation [115] and the latter region is to the Poole-Frenkel emission from

the TaN electrode, [116]. Therefore, it could be expected that the pentacene-based OTFT with a high-κ dielectric of $LaYO_X$ gate insulator has a low gate leakage current and a well gate controllability resulting in better electrical characteristics, compared to that with thermal or sputtering gate oxide [25], [88] without interface modification. Because the work function of TaN electrode with ammonia plasma treatment (~ 4.6 eV) is smaller than that of Au electrode (~ 5 eV), the leakage current density under bottom-injection condition where the positive bias is applied on Au electrode, is higher than that under top-injection condition. Such high capacitance density and low leakage current density of Au/$LaYO_X$/TaN MIM capacitor represent that the high-κ $LaYO_X$ thin film, even subjected to a low-temperature annealing at 300 °C, is still a good candidate for gate dielectric application.

4.2-2 Characteristics of Pentacene Layer

Fig. 4-8 provides the information on the crystallinity and the surface morphology of the pentacene channel layer strongly dependent on the surface condition of the substrate material. These glancing-incidence X-ray diffraction (GI-XRD) peaks of the deposited pentacene layer correspond to (hkl) equal to (001), (002), (003), and (004), respectively [87], [101]. It indicates a well-oriented film with a c-axis perpendicular of the pentacene layer on the lanthanum-yttrium oxide ($LaYO_X$) film. The main XRD peak of the $LaYO_X$ film located at 29.7° with a hexagonal phase corresponding to (002) [80] and that of the TaN film located at 35.4° with a face-center cubic phase corresponding to (111) [97] are not shown in Fig. 4-8. The GIXRD peaks of the pentacene layer present an average crystalline quality of the channel layer deposited on the $LaYO_X$/TaN gate structure without organic/insulator interface modification [22]-[24]. The atomic force microscopy (AFM) image of the pentacene layer deposited on the $LaYO_X$/TaN layers is also shown in the inset of Fig. 4-8. The pentacene layer on the $LaYO_X$ film also performs a good surface roughness and a dendrite grains to achieve

an acceptable quality channel in OTFT. As a result, in this work, the crystalline quality and the surface roughness of the deposited pentacene channel layer on the $LaYO_X$/TaN gate structure are compatible with the other reports [87], [101]. Therefore, if there is any electrical improvement on our proposed pentacene-based OTFT, it could be attributed to the benefit by using the high-κ gate dielectric of the lanthanum-yttrium oxide film.

4.2-3 Characteristics of Organic TFTs With $LaYO_X$ Gate Insulator

Fig. 4-9 reveals the transfer characteristics (I_{DS}–V_{GS}) and its square root plot ($I_{DS}^{1/2}$–V_{GS}) of the pentacene-based OTFT with a high-κ dielectric of the lanthanum-yttrium oxide ($LaYO_X$) gate insulator measured at V_{DS} = –2 V. The data points are spaced to 0.01 V to ensure a good accuracy during measurement. The resolution setting and the noise are set 10 pA and smaller than 100 fA, respectively. The curves are typical for the pantacene-based OTFT working in accumulation mode. The threshold voltage (V_{TH}) of the pentacene-based OTFT with a high-κ dielectric of $LaYO_X$ gate insulator estimated from the x-axis intercept of the $I_{DS}^{1/2}$–V_{GS} plot at V_{GS} = –2 V is nearly –1.25 V, which is a dramatically decreased value compared to that with silicon-oxide based insulator [25]. According to the standard OTFT theory in Chapter 3, the field-effect mobility in saturation regime ($\mu_{FE,sat}$) could be calculated from the following equation

$$\mu_{FE,sat} = 2I_{DS,sat}\frac{L}{C_{ins}W}\frac{1}{\left(V_{GS}-V_{TH,sat}\right)^2} \tag{3-21}$$

, where the C_{ins} is the gate capacitance density of the insulator layer. The C_{ins} is 410 nF/cm^2 obtained from the Au/$LaYO_X$/TaN MIM capacitor measured at the applied voltage of –4 V on Au electrode. The saturation drain current ($I_{DS,sat}$) of this high-κ $LaYO_X$ OTFT with a dimension of W/L = 1000 μm/120 μm is 0.21 μA measured at V_{GS} = V_{DS} = –2 V. Therefore, we figure that the $\mu_{FE,sat}$ is approximately 0.22 cm^2/V-s, which is the hole mobility in the

pentacene channel under saturation operation. By means of the high-κ lanthanum-yttrium oxide ($LaYO_X$) insulator with a large gate capacitance density (C_{ins}), the higher concentration carriers could be accumulated in the pentacene channel at the same gate voltage and the Fermi level moves toward the band edge. The trapping states located in the grain boundaries are filled, and consequently the injection carriers are free to move with the microscopic mobility associated with carriers in the delocalized states, which is described in the chapter 2. Thus, integrating high-κ dielectrics into OTFTs lowers the operational voltages.

The ON/OFF current ratio is almost 3.3×10^3 by the definition of the maximum $I_{DS,sat}$ over the minimum $I_{DS,sat}$, when the V_{GS} is scanning between 0 V and –2 V under V_{DS} = –2 V. The subthreshold swing (*S.S.*) should be as low as possible since it represents the interface quality corresponding to the switching capability to turn from the off-state to the on-state. In this work, the subthreshold swing (*S.S.*) is 265 mV/Dec., which could be expressed as

$$S.S. = \left[\frac{d \log_{10} I_{DS,SUB}}{dV_{GS}} \right]^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dep} + C_{it}}{C_{ins}} \right) \sim 2.3 \frac{kT}{q} \left(1 + \frac{qN_{SS,\max}}{C_{ins}} \right). \quad (3.9)$$

where the C_{dep} and the C_{it} are the depletion capacitance density of the pentacene film and the capacitance density corresponding to the interface trap states, respectively. Because the pantacene-based OTFTs works in accumulation mode, the depletion charges ($Q_{dep} = q \times C_{dep}$) could be neglected. As a result in Eq. 3-9, the maximum trap states density ($N_{SS,\max} = C_{it} / q$) could be calculated by a value of 8.8×10^{12} eV^{-1}-cm^{-2}, which is an applicable value compared with the other reports [87], [101]. If the interface status between the inorganic oxide insulator and the pentacene layer is treated from hydrophilic to hydrophobic, the pentacene molecules would be grown and aligned with each other. Thus, the maximum trap states density ($N_{SS,\max}$) also could be further minimized. The 1,1,1,3,3,3-hexamethyldisilazane (HMDS) [117], the polymethylmethacrylate (PMMA) [118], and the octadecyltrichlorosilane (OTS) [119], are the organic polymer materials usually used for this interface modification. Since the large gate capacitance density (C_{ins}) of the high-κ $LaYO_X$ insulator in pantacene-based OTFT devices

could induce more accumulation charges to minimize the effects on the interface states, a lower subthreshold swing (*S.S.*) could be achieved to increase the switching speed under smaller operational voltages. This result is consistent with Eq. 3-9.

The hysteresis phenomenon is often observed in OTFTs with the high-κ dielectric but unavoidable while the gate voltage sweeping [120], [121]. In this work, a little hysteresis is also observed in this pentacene-based OTFT with a high-κ dielectric of $LaYO_X$ gate insulator but it is still under an acceptable value, while the saturation drain current ($I_{DS,sat}$) scans from V_{GS} = 0 V to –2 V, as shown in Fig. 4-9. The transfer characteristic curve is shift to the positive direction when the gate voltage (V_{GS}) is sweeping direction from 0 V to –2 V and then back from –2 V to 0 V. It is dominated by long-lifetime deep electron traps at pentacene and high-κ dielectric interface. Initially in the OFF-to-ON sweeping, the negative charges are accumulated in the channel and filled up the electron traps under V_{GS} = 0 V and V_{DS} = –2 V. When V_{GS} sweeps toward negative, more holes are induced to balance the stored negative charges. The ON-to-OFF scanning, on the contrary, starts to the hole accumulation and no stored negative charges, resulting in a little larger threshold voltage of this OTFT [121].

The off-state current larger than the gate leakage current (I_G) under V_{GS} > –0.5 V could be attributed to the impurity levels generated from the structural isomers of pentacene assisted conduction [87], [101]. The OFF-state leakage current between drain and source could be reduced by simply using the purified pentacene source rather than the 97 % purity of the pentacene [101]. The maximum gate leakage current of the pentacene-based OTFT with a high-κ dielectric of $LaYO_X$ gate insulator is about 200 pA at V_{GS} = V_{DS} = –2 V, resulting from the gate-to-source leakage. In order to ensure the shadow masks have a good manual alignment, the overlap area of the gate-to-source region or the gate-to-drain region is designed by 1000 μm × 1000 μm, where one of the 1000 μm represents the length of the channel width, as shown in Fig. 3-3(d). From the leakage current calculation on the Au/ $LaYO_X$/TaN MIM capacitor with the same overlap area under the applied voltage of 2 V, the value is close to

100 pA and it is decreased with the decrease of the applied gate voltage. Therefore, if the overlap area is reduced by using a machinery alignment, the extra gate leakage current in saturation regime could be reduced as well as the power saving of the OTFT under operation is achieved. Finally, Fig. 4-10 shows the output characteristic (I_{DS}–V_{DS}) of the pentacene-based OTFT with a high-κ dielectric of $LaYO_X$ gate insulator. The saturation drain current ($I_{DS,sat}$) is around 210 nA which is three-orders magnitude larger than the gate leakage current at $V_{DS} = V_{GS} = -2$ V. This result indicates a high quality of $LaYO_X$ gate dielectric on the pentacene-based OTFT even processed in low-temperature condition.

Table 4-3 compares all electrical parameters of the pentacene-based organic TFTs (OTFTs) with various gate dielectrics, including silicon oxide (SiO_2) [25], barium zirconate titanate (BZT) [25], tantalum pentoxide (Ta_2O_5) [88], titanium oxide (TiO_2) [90], and lanthanum-yttrium oxide ($LaYO_X$). In this work, we use the thinnest dielectric thickness (D) of the $LaYO_X$ gate insulator to obtain a large gate capacitance density (C_{ins}), compared to the other high-κ dielectric materials. The subthreshold swing (*S.S.*) and the operational voltages are dramatically decreased with the enlargement of the gate capacitance density. Besides, these saturation field-effect motilities ($\mu_{FE,sat}$) show less dependence on the gate capacitance densities with values around 0.1 ~ 0.4 cm^2/V-s in this comparison table. That is because their saturation field-effect motilities are calculated from various operational voltages (V_D), corresponding to the charge density (Q_S), as shown in Fig. 2-16. However, the ON/OFF current ratio of the $LaYO_X$ OTFT in this work is not good compared to the other reports [25], [88], [90]. Two possible reasons we summarize below. First, the channel length (L) and the channel width (W) of the fabricated $LaYO_X$ OTFT in this work are 120 μm and 1000 μm, respectively, confirmed by the optical microscope. If the dimension ratio of W/L is increased by the reduction of the channel length (L) compared to the other reports, the drain current as well as the ON/OFF current ratio could be increased. Second, the operational voltages, V_{GS} and V_{DS}, are close to the threshold voltage of the $LaYO_X$ OTFT so that the overdrive term

(V_{GS}–V_{TH}) in Eq. 2-24 is small. When the operational voltage is increased to 3 V, its $LaYO_X$ OTFT is subjected to a stress-induced damage on channel layer and gate insulator, and the I-V characteristics would be shifted and degradation. That is why we set the safety operational voltage of 2 V in this work. The benefit of enlarging the gate capacitance density to obtain a high driving capability seems not fully display due to the smaller operational voltages. Therefore, if the thickness of the gate dielectric is twice increasing to 60 nm, the operational voltages could be slightly increased at the same threshold voltage condition. As long as we fine tune the gate capacitance density (C_{ins}) and the overdrive (V_{GS}–V_{TH}), the driving current as well as the ON/OFF current ratio could be further increased.

4.2-4 Summary

In this section, we demonstrate a pentacene-based organic thin-film transistor (OTFT) with a gate dielectric of high-κ lanthanum-yttrium oxide ($LaYO_X$) insulator processed at a low temperature of 300 °C. The Au/30-nm $LaYO_X$/TaN MIM capacitor has a high capacitance density of 410 nF/cm^2 and a low leakage current below 20 nA/cm^2 biased at –4 V. The pentacene-based OTFT with a high gate capacitance could induce more accumulation charges and result in good electrical characteristics under low drain-and-gate voltage operation. This device exhibits good electrical characteristics, such as a low subthreshold swing of 265 mV/Dec., a small threshold voltage of –1.25 V, a ON/OFF current ratio of 3.3×10^3, and especially on a low gate leakage current smaller than 200 pA under $V_{DS} = V_{GS} = -2$ V. Therefore, the $LaYO_X$ organic thin-film transistor could work under low-voltage operation, compatible with portable or low-power electronic applications.

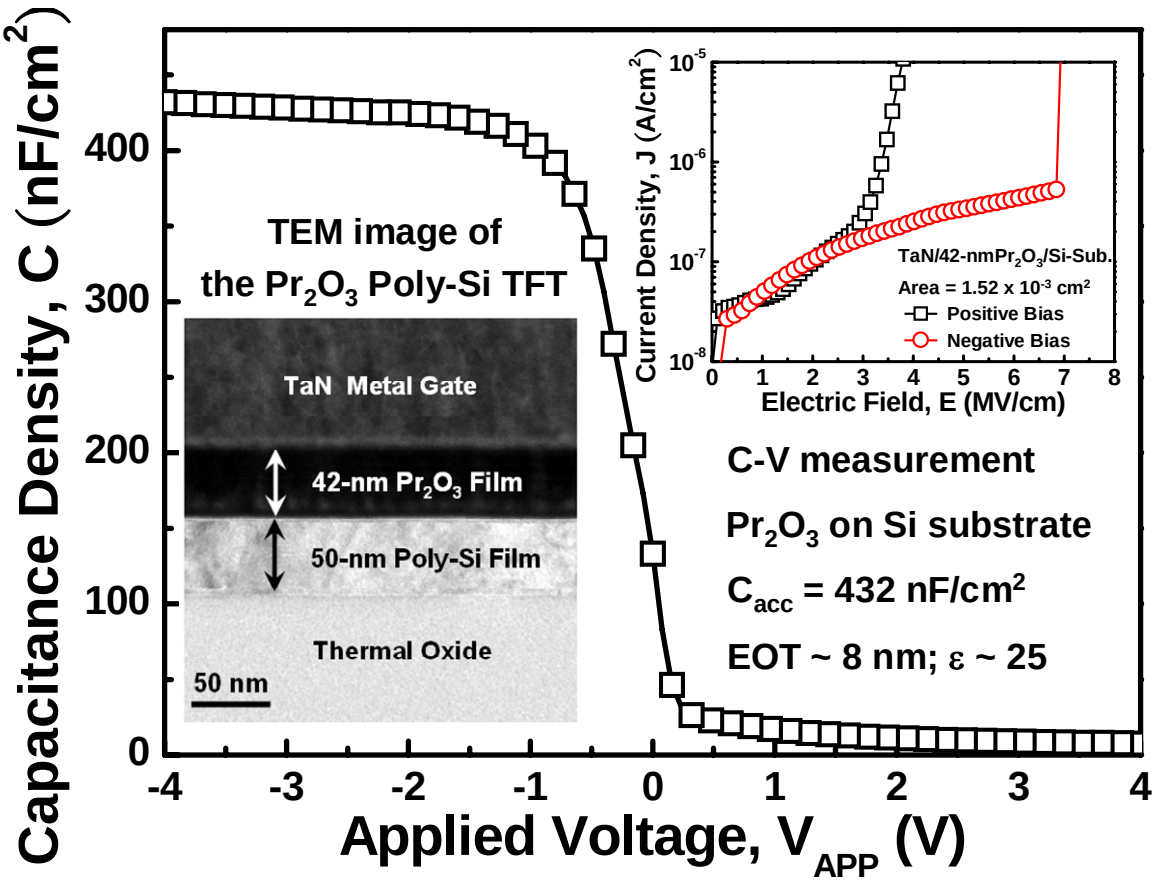


Fig. 4-1. The C-V characteristic and the leakage current density of the Pr_2O_3 film on Si substrate. The insert is the cross-sectional TEM image of the proposed Pr_2O_3 poly-Si TFT.

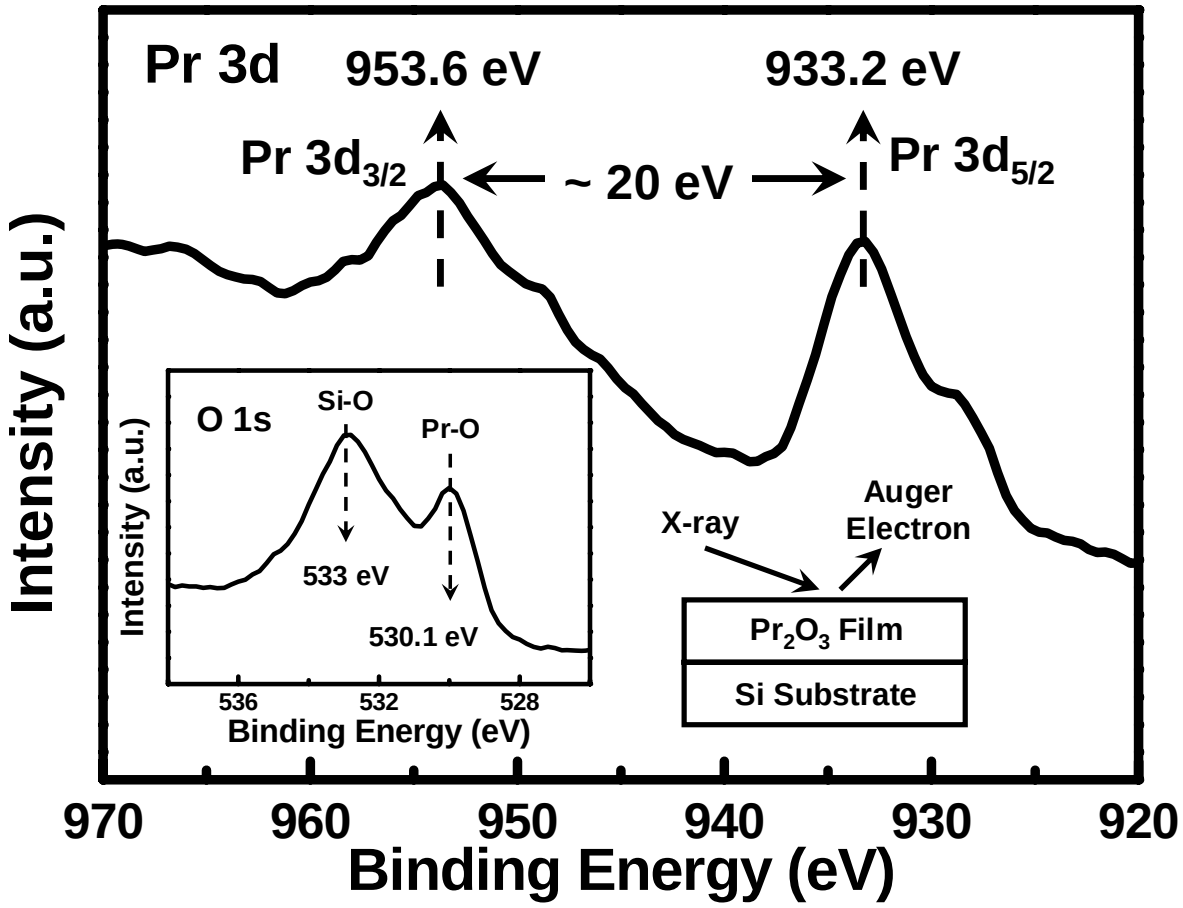


Fig. 4-2. The XPS spectra of Pr 3d and O 1s core level for the Pr_2O_3 gate insulator on Si substrate.

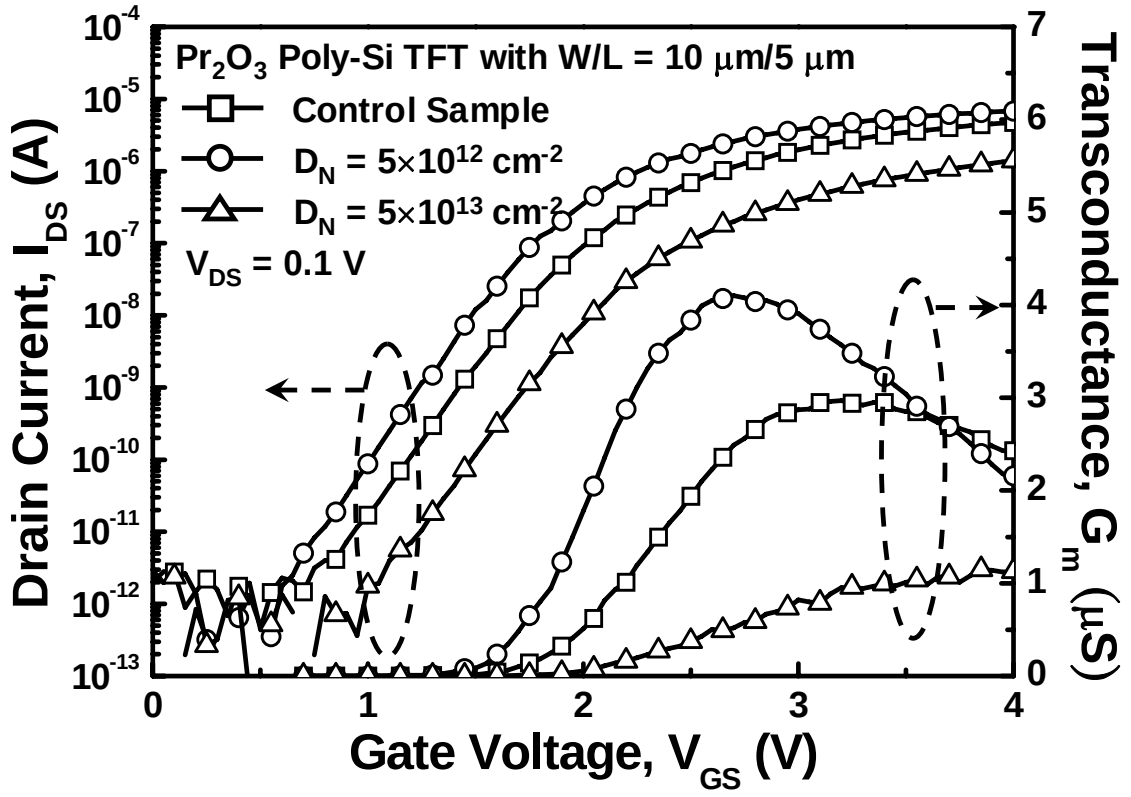


Fig. 4-3. The transfer characteristics of the Pr_2O_3 poly-Si TFTs with various nitrogen dosages of zero (control sample), 5×10^{12} cm^{-2}, and 5×10^{13} cm^{-2} under $V_{DS} = 0.1$ V.

.

Table 4-1 The relationships between trap states and device parameters of LTPS TFTs

	Main influences on trap states
Transconductance (G_m)	Interface states Tail states in grain boundaries
Threshold Voltage (V_{TH})	Injection charges into gate insulator Deep interface states Deep states in the grain boundaries
Substhreshold Swing (*S.S.*)	Deep intra-grain defects Deep interface states

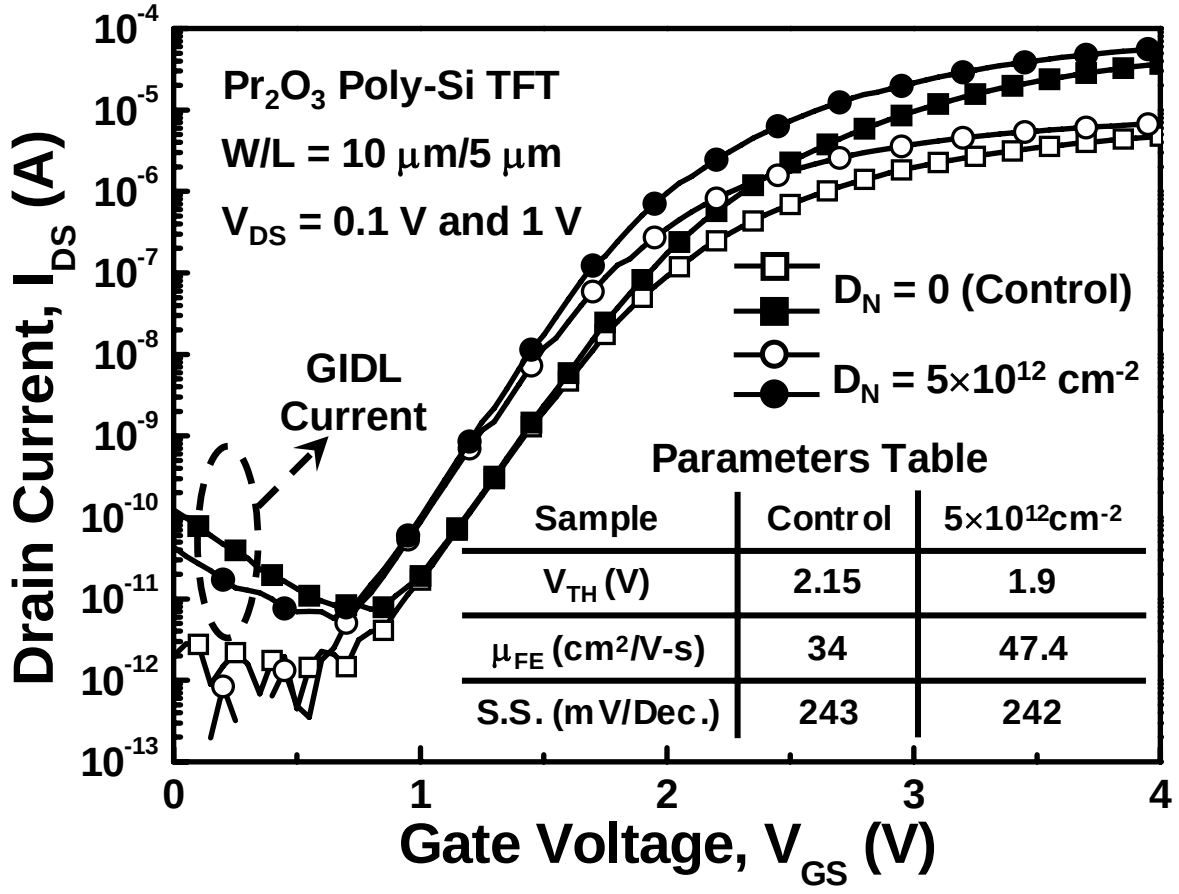


Fig. 4-4. The transfer characteristics (I_{DS}–V_{GS}) of the Pr_2O_3 poly-Si TFTs with nitrogen dosages of zero and 5×10^{12} cm^{-2} under V_{DS} = 0.1 V and 1 V. The inset is the table of the electrical parameters.

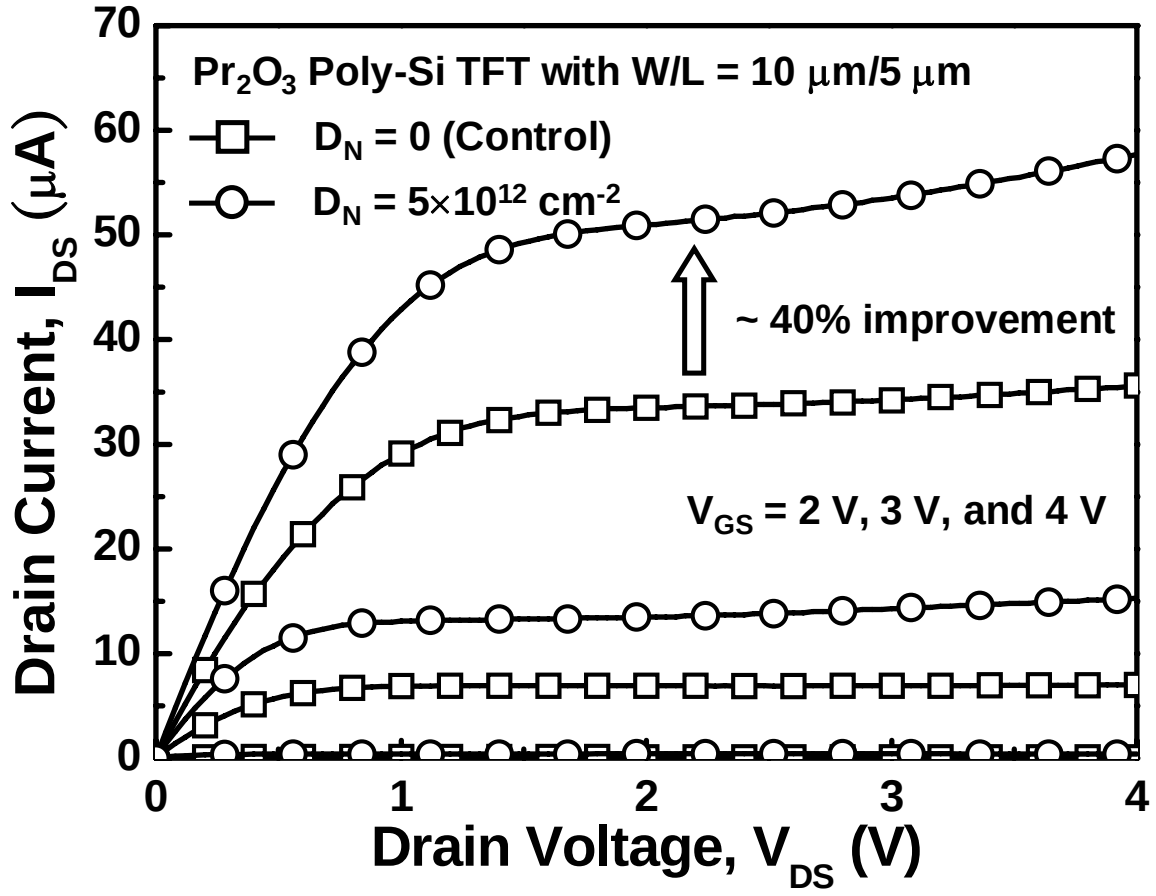


Fig. 4-5. The output characteristics (I_{DS}–V_{DS}) of the Pr_2O_3 poly-Si TFTs with nitrogen dosages of 0 cm^{-2} and 5×10^{12} cm^{-2}.

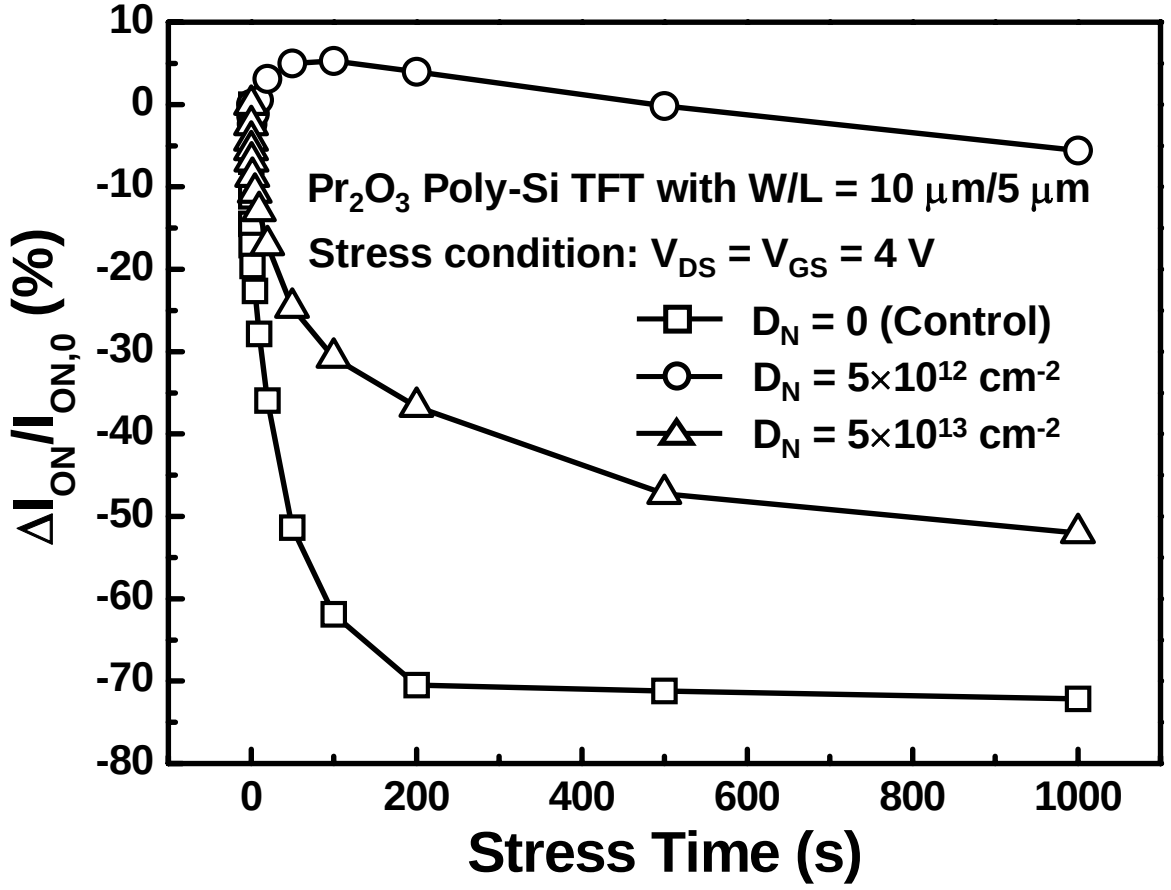


Fig. 4-6. The drain current degradation for the Pr_2O_3 poly-Si TFTs with and without nitrogen implantation under hot-carrier stress condition.

Table 4-2. Comparison on electrical parameters of SPC poly-Si TFTs with various gate dielectrics, including TEOS oxide, aluminum oxide (Al_2O_3), lanthanum--aluminum oxide ($LaAlO_3$), and praseodymium oxide (Pr_2O_3)

SPC TFT with Various Dielectrics	40 nm TEOS [60]	50 nm Al_2O_3 [85]	50 nm $LaAlO_3$ [86]	42 nm Pr_2O_3 (D_N=0cm^{-2}) [This Work]	42 nm Pr_2O_3 (D_N=5E12cm^{-2}) [This Work]	42 nm Pr_2O_3 (D_N=5E13cm^{-2}) [This Work]
EOT	40 nm	20 nm	8.7 nm	8 nm	8 nm	8 nm
W/L (mm)	50/10	200/3	100/4	10/5	10/5	10/5
V_{TH} (V)	5.14	3*	1.2	2.15	1.9	2.61
μ_{FE} (cm^2/V-s)	12.4	47*	40	34	47.4	10.2
S.S. (mV/Dec.)	1970	440*	310	243	242	275
I_{ON}/I_{OFF} (10^6)	0.24	0.3*	6.3	6.8**	9.73**	1.99**

* $Si_{0.85}Ge0_{0.15}$ TFT with Al_2O_3 dielectric ** I_{OFF} is set 800 fA at V_{DS} = 0.1 V

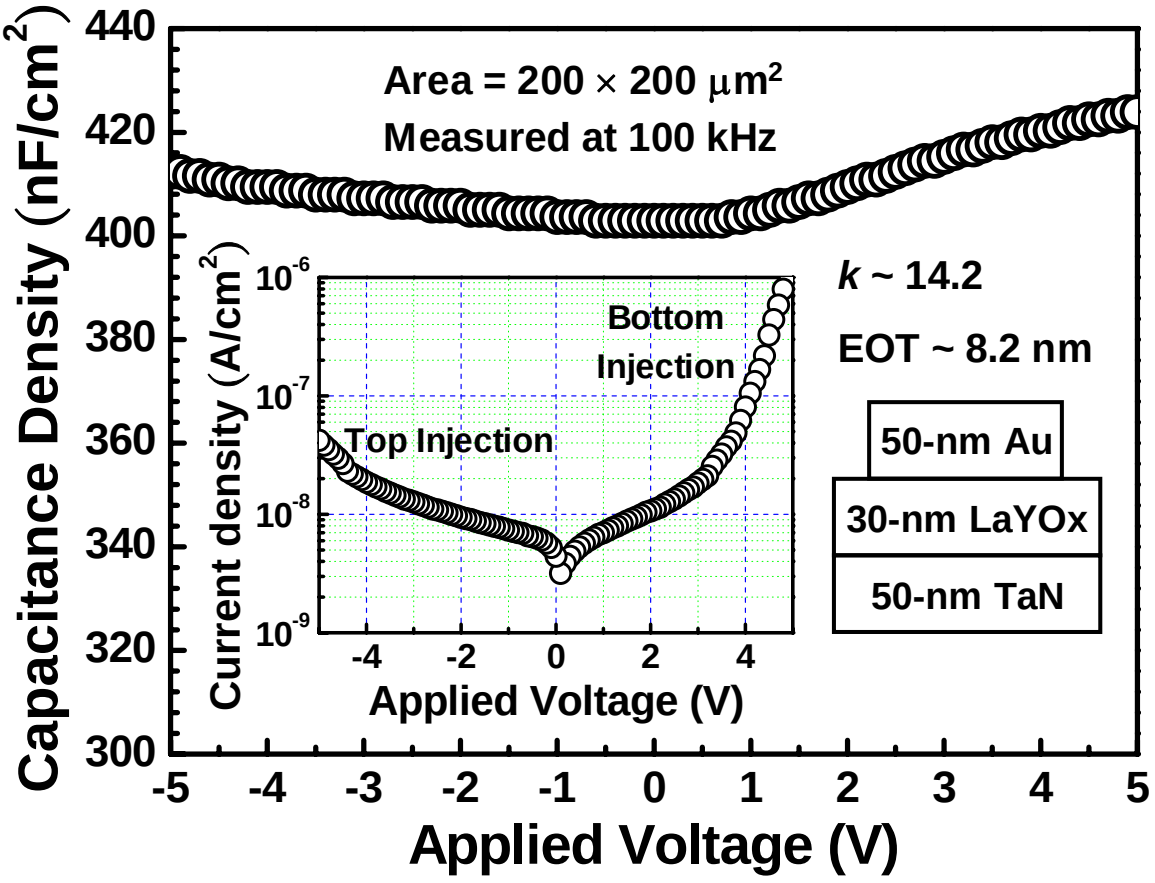


Fig. 4-7. The capacitance-voltage (C–V) and the current density-voltage (J–V) characteristics of the Au/$LaYO_X$/TaN MIM capacitor.

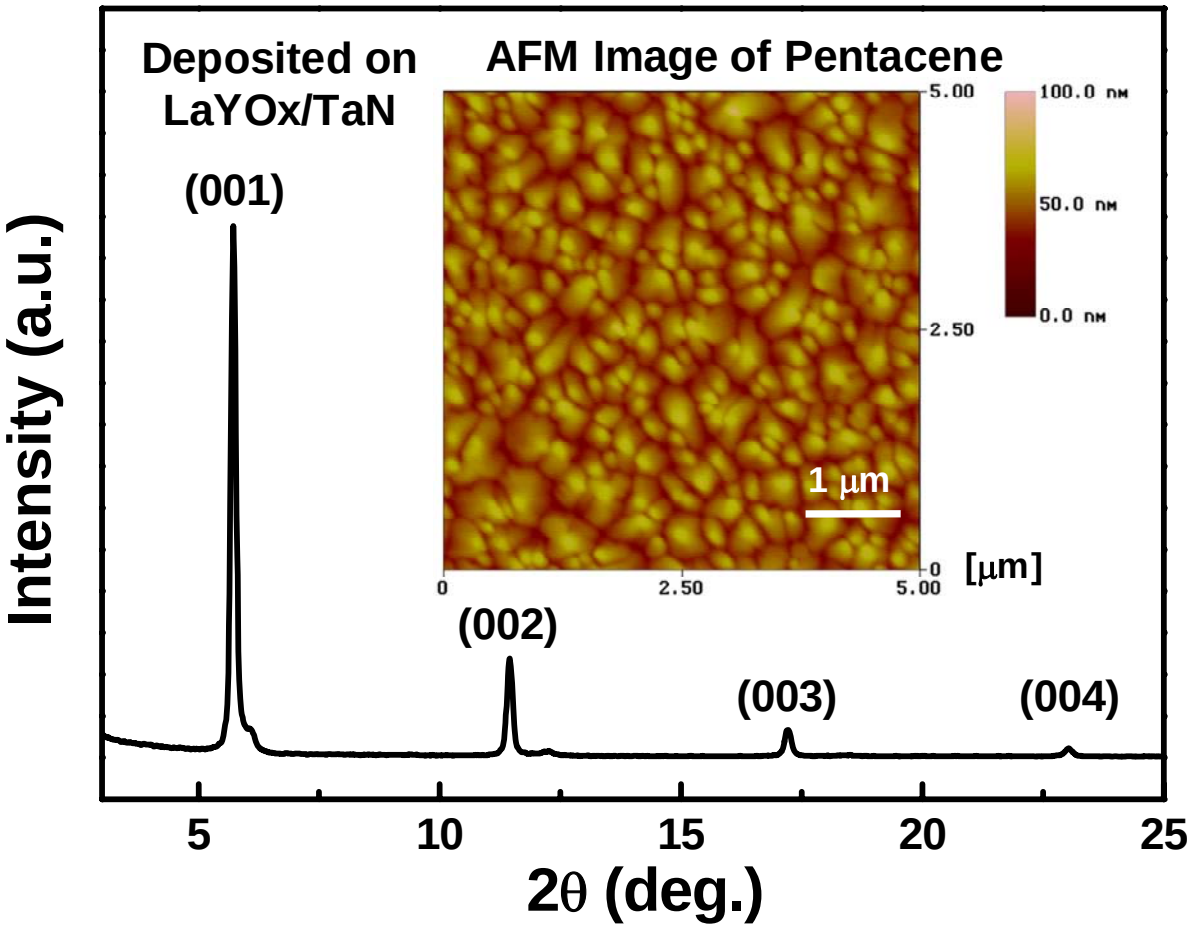


Fig. 4-8. The glancing-incidence X-ray diffraction (GI-XRD) spectra and the atomic force microscopy (AFM) image (inset) of pentacene channel layer deposited on the $LaYO_X$/TaN gate structure.

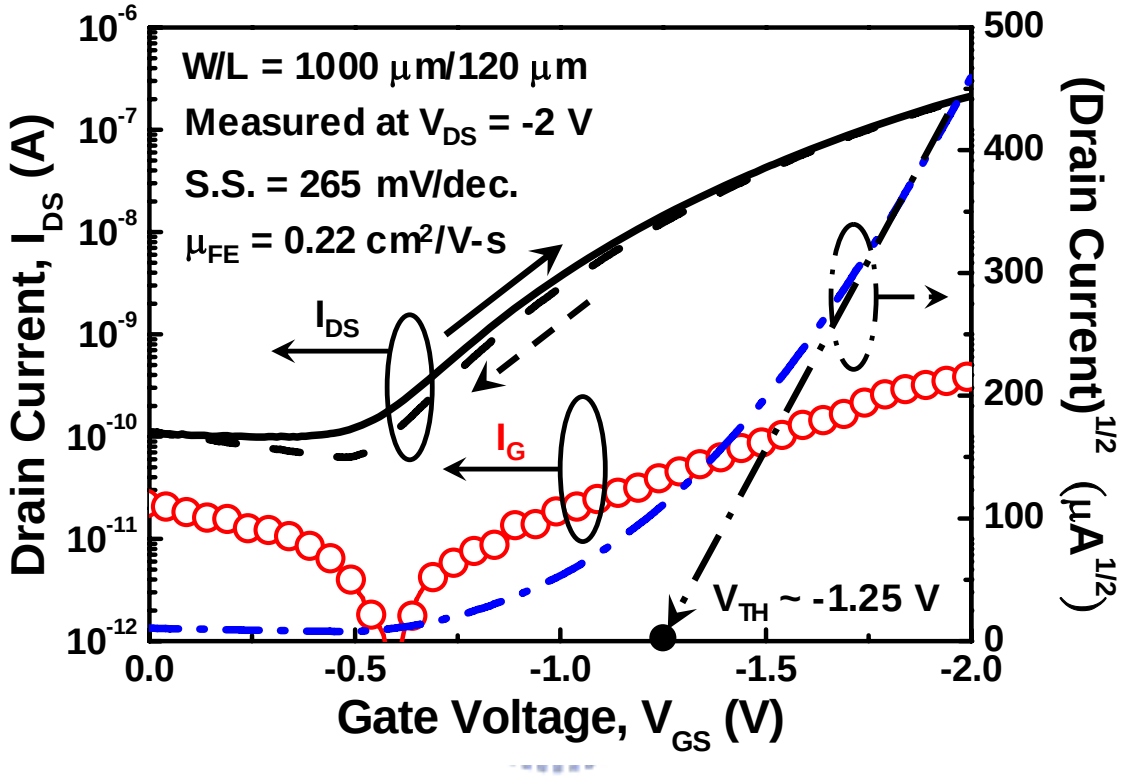


Fig. 4-9. Transfer characteristics (I_{DS}–V_{GS}) and its square root plot ($I_{DS}^{1/2}$–V_{GS}) of the pentacene-based organic thin-film transistor with a high-κ dielectric of $LaYO_X$ gate insulator at V_{DS} = –2 V.

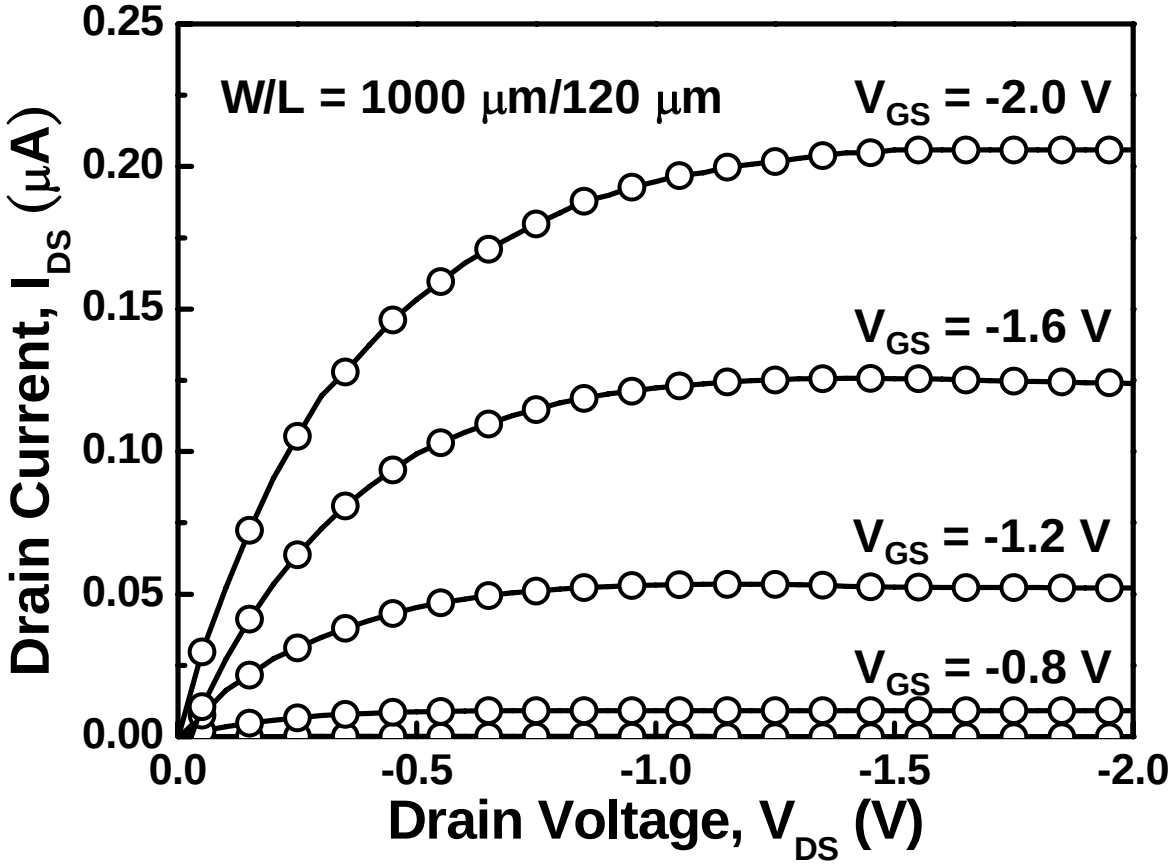


Fig. 4-10. The output characteristics (I_{DS}–V_{DS}) of the pentacene-based organic thin-film transistor with a high-κ dielectric of $LaYO_X$ gate insulator.

Table 4-3. Comparison on electrical parameters of the pentacene-based organic TFTs with various gate dielectrics, including silicon oxide (SiO_2), barium zirconate titanate (BZT), tantalum pentoxide (Ta_2O_5), titanium oxide (TiO_2), and lanthanum--yttrium oxide (LaYOx).

	W/L (μm/μm)	*D* (nm)	C_{ins} (nF/cm^2)	$\mu_{FE,sat}$ (cm^2/V-s)	I_{ON}/I_{OFF}	*S.S.* (mV/Dec.)	V_{TH} (V)
SiO_2 [25]	1500/83	100	6.9	0.12	3x10^5	1785	–18 V @ V_D = –50 V
BZT [25]	1500/83	122	125	0.38	3x10^5	300	–2 V @ V_D = –5 V
Ta_2O_5 [88]	500/170	300	50	0.32	10^4	500	–0.8 V @ V_D = –5 V
TiO_2 [90]	2000/25	280	676	0.15	3.5x10^6	170	–0.34 V @ V_D = –1 V
LaYOx [This Work]	1000/120	30	410	0.22	3.3x10^3	256	–1.25 V @ V_D = –2 V

CHAPTER 5

CONCLUSION AND FUTURE PROSPECTS

5.1 CONCLUSION

In this thesis, we integrate high-κ materials as gate dielectrics, the praseodymium oxide (Pr_2O_3) and the lanthanum-yttrium oxide ($LaYO_X$), to improve the electrical performance of low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) and pentacene-based organic TFT (OTFT), respectively. The 42-nm Pr_2O_3 gate dielectric shows a high capacitance density of 432 nF/cm^2 and a high breakdown electrical field larger than 3 MV/cm. The LTPS TFT with 42-nm Pr_2O_3 gate dielectric has a good gate controllability to minimize the body effect, which means it could induce more minority carriers to quickly fill up the grain boundary trap states in active channel region under operation. Therefore, the threshold voltage (V_{TH}) and the subthreshold swing (*S.S.*) of the LTPS TFTs with a Pr_2O_3 gate dielectric could be improved compared to those with a TEOS gate insulator. Moreover, with moderate dosages of nitrogen implantation before solid-phase crystallization (SPC) annealing, the threshold voltage (V_{TH}) and the field-effect mobility (μ_{FE}) of LTPS TFT could further progress because implanting nitrogen atom could passivate trap states in intra-grains. Further, it could form the stronger Si-N bond to enhance the immunity against hot-carrier stress. On the other hand a 30-nm $LaYO_X$ gate insulator also has a high capacitance density of 410 nF/cm^2 and a low leakage current below 20 nA/cm^2 biased at –4 V. The pentacene-based OTFT with a high-κ 30-nm $LaYO_X$ gate dielectric could induce more accumulation charges (Q_{acc}) to enhance the saturation field-effect mobility ($\mu_{FE,sat}$) to 0.22 cm^2/V-s. This device also exhibits good electrical characteristics, such as a low subthreshold swing of 265 mV/Dec., a

small threshold voltage of −1.25 V, a ON/OFF current ratio of 3.3×10^3, and especially on a low gate leakage current smaller than 200 pA under the operational voltage of −2 V. Therefore, by integrating a Pr_2O_3 high-κ dielectric and crystallizing a α-Si layer with nitrogen implantation, the electrical performance of LTPS TFT device is suitable for high-speed and low-power circuits design in near future. The organic TFT with $LaYO_X$ gate insulator has been greatly reduced the operational voltage, which could reduce the power consumption for active-matrix organic light-emitting diode (AM-OLED) display or flexible electronic applications.

5.2 FUTURE PROSPECTS

In this work, we use electron-beam evaporation system to deposit the high-κ gate dielectrics because of our budget and flexible research consideration. But, in flat panel display (FPD) industry, electron-beam evaporation is not a suitable process for large size panel fabrication. The thin-film deposition process of LTPS TFTs in industry is usually unitizing plasma enhanced chemical vapor deposition (PECVD) system or reactive sputter system. The praseodymium (Pr) target with oxygen reaction by sputter system could be used to deposit the high-κ dielectric on active channel layer of LTPS TFT. Furthermore, the praseodymium oxide thin film could be formed by using a thermal decomposition of praseodymium complex, such as $Pr_2(CO_3)_3 \cdot 8H_2O$ **[122]** or $Pr(NO_3)_3 \cdot 6H_2O$ **[123]**. Such sol-gel process with spin-coating high-κ dielectric layer on active channel layer of LTPS TFT is more suitable for large size panel fabrication. On the other hand, the sol-gel method is also easy applying on OTFT process. The precursor of the $LaYO_X$ could be spun on the large area of panel or sprayed in allocated active region of OTFT. The industry usually uses ink-jet method to define device area of OTFT without lithography, which is compatible with sol-gel method of high-κ dielectric. Therefore, no matter LTPS TFT or OTFT, the sol-gel method provides a convenient

way to deposit the high-κ dielectrics, and it is worthy to develop in the industry process.

In this work, we use the $LaYO_X$ dielectric with large bandgap (E_g) as the insulator of OTFT device to reduce gate leakage current. Besides, the high-κ $LaYO_X$ film has been proposed to solve the moisture absorption problem [80]. The OTFT also need the passivation layer on active channel layer because the organic channel layer is easily affected by environmental condition. Therefore, if the anti-absorbent $LaYO_X$ film is use as the passivation layer onto organic active channel to isolate outside moisture; the reliability of OTFT could be improved. The more electrical tests on OTFT could be performed without absorbent limitation. On the other hand, the $LaYO_X$ film with large E_g is also a suitable gate dielectric for n-type and p-type LTPS TFT devices. Because the maximum process temperature is controlled within 600 °C, the $LaYO_X$ film has structural phase transformation to increase κ-value to 29 [81]. The thicker physical thickness under the same EOT could be fabricated, and the reliability of LTPS TFT device is also improved.

As the mention in chapter 2, the saturation field-effect mobility ($\mu_{FE,sat}$) of OTFT is dependent on the operational voltages (drain and gate voltages). In fact, the 2-V operational voltage for the OTFT with 30-nm $LaYO_X$ gate insulator is a safety voltage with a little hysteresis and enough driving current. As the thickness of the high-κ gate insulator is increased, the higher drain voltage could be applied on OTFT without stress degradation and help drain out the accumulation charges in active channel to enhance the saturation field-effect mobility. To maintain the same accumulation charges (Q_{acc}) in active channel, the gate voltage (V_{GS}) must be increased with the decreased gate capacitance density (C_{ins}). However, the gate and drain voltages could not be increased with the same ratio because the limitation of breakdown voltage at the drain side, which depends on the addition of these two applied voltages. Therefore, the OTFTs with various thickness of the high-κ gate insulator could be fabricated, and the relationships among the saturation field-effect mobility, the drain voltage, and the gate voltage could be established to model the electrical characteristics of

OTFTs.

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Publication List

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