Chap.1 Introduction

In recent years, many efforts exploit the applications comprising frequency frontier above 60 GHz. Signal frequencies at W band are possessed of high spatial resolution, the resulting compact size , and small antenna dimensions. In addition, the fog and cloud penetration properties of W band make those attractive in commercial applications.

The increasing demand for intelligent transportation system (ITS) has raised the necessity to realize on-vehicle collision avoidance radar. The 77GHz band has been specifically defined for automotive applications in Japan, the US and Europe as a common world wide frequency for that purpose. The circuit components on the radar front end are quiet difficult and expensive because the working frequency of forward-looking automotive radar is 77GHz.

Fig.1-1 shows the system block diagram of proposed 77 GHz RF front end. In the transmitter, the 38.5 GHz signal is amplified by a power amplifier and then multiplied by a frequency doubler to provide an output signal at 77 GHz. In the receiver, the received RF signal is amplifier by a low noise amplifier and then down converted by a subharmonic mixer, which is pumped by LO coupled from 38.5 GHz signal of the transmitter. Therefore, frequency doubler and subharmonic are key components in the proposed RF front end system.

In the chapter 2, two different subharmonic mixer topologies are presented. One adopts antiparallel diode pairs and the other employs an ultra broadband ring to achieve harmonic mixing response. Both circuits utilize coplanar waveguide (CPW) technology on a ceramic substrate.

In the chapter 3, two different frequency doublers are presented. Schottky diodes and HEMT can be used as nonlinear devices to generate harmonics. Single ended topology is utilized in both circuits. The single diode and HEMT doublers are fabricated using hybrid MIC (Microwave Integrated Circuit) and MMIC (Monolithic Microwave Integrated Circuit) process.

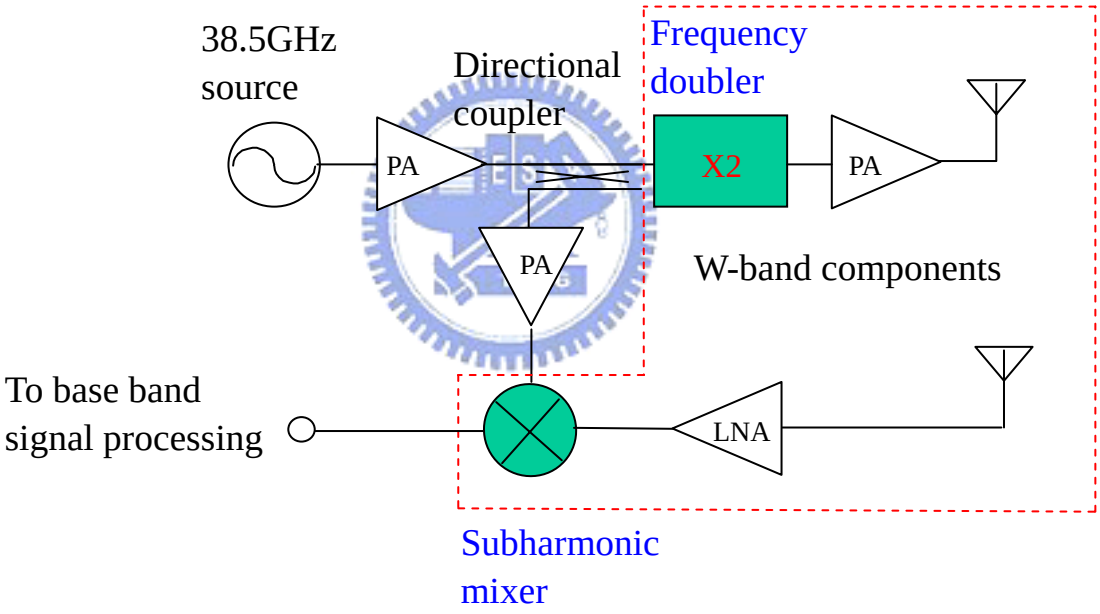


Fig.1-1 The proposed 77 GHz RF frond end system block

Chap.2 W band Subharmonic Mixer

2-1 Introduction

It is a significant challenge to downconverting a received signal from high frequencies for the microwave circuit designer. For fundamental mixing operation, mixers typically have a minimum local oscillator (LO) power below which the frequency-conversion performance degrades drastically. At millimeter wave frequencies, it may be difficult or impossible to meet these power requirements with an integrated oscillator. In addition, LOs with sufficient output power at millimeter-wave often incorporate physically large and expensive waveguide resonators.

Subharmonic mixing provides a solution to overcome the above difficulties. Subharmonic mixing operation use a mixer that is pumped at half the LO frequency, and to mix the RF signal with the second harmonic of the junction's conductance waveform. The benefit of this approach is that it allows the use of a LO at a relatively low frequency at which the output power and phase noise performance may be superior to that which is available at the fundamental frequency. Besides, subharmonic mixing is also provided with the inherent RF to LO isolation. In receiver applications, this isolation is vital in order to minimize the radiation of LO power from the RF port. [1-4]

Two different subharmonic mixer configurations, antiparallel diode pair and rat-race ring subharmonic mixer, will be presented in this chapter,. The design methodology will be described in details as follows.

2-2 Antiparallel Diode Pair Subharmonic Mixer

Subharmonic mixers using antiparallel diode pair have been successfully implemented in millimeter wave applications. Furthermore, antiparallel diode pair mixers are attractive due to the inherent RF to LO isolation, self protection against large peak inverse voltage burnout and lower noise figure through suppression of local oscillator sideband. In the thesis, this design methodology was utilized up to W band.

2-2-1 Harmonic Mixing Theory

Antiparallel diode configuration is the most widely implemented subharmonic mixer topology [4]. This consists of a pair of diodes in parallel with polarity reversed to one another. The analysis involves graphic and numeric illustration.

I. Graphic illustration:

Fig. 2-1 shows the waveform of current and conductance while diode is pumped by a large LO signal. The conductance can be easily presented in the form of Fourier series as:

$$g(t) = \sum_{n=-\infty}^{\infty} g_n e^{jn\omega_{LO}t} \tag{2.1}$$

Consequently, the diode will generate RF harmonics if RF signal is applied. The RF voltage can be expressed as:

$$V_{RF} = \sum_{m=-\infty}^{\infty} v_m e^{jm\omega_{RF}t} \tag{2.2}$$

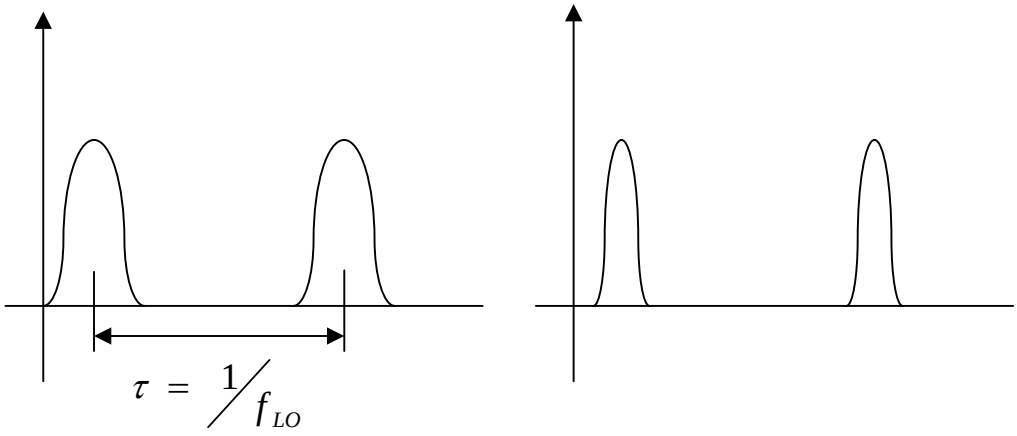


Fig. 2-1 The waveform of LO pump current and conductance

i(t)

Hence, the small signal current of the diode which consists of RF and *g(t)* can be expressed as:

$$i_d = V_{RF} g(t) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} g_n v_m e^{j(m\omega_{RF} + n\omega_{LO})t} \tag{2.3}$$

This current includes IF signal and all the mixing products of RF and LO. IF signal can be obtained by means of adequate circuit design to suppress redundant harmonics.

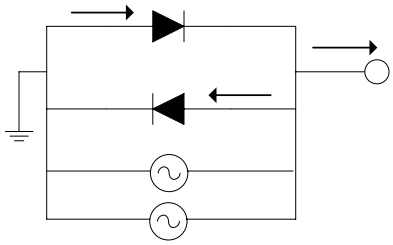
Fig.2-2 shows the current and voltage flow of antiparallel diode pair. The figure displays that the currents of LO and RF have a period difference of $\tau_{LO}/2$ and $\tau_{RF}/2$, respectively. Take the current of D1 as reference current, and the all the currents can be expressed as follows:

$$i_1 = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} g_n v_m e^{j(m\omega_{RF} + n\omega_{LO})t} \tag{2.4}$$

$$i_2 = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} g_n v_m e^{j(m\omega_{RF} + n\omega_{LO})t} e^{jm\omega_{RF}(\frac{\tau_{RF}}{2})} e^{jn\omega_{LO}(\frac{\tau_{LO}}{2})} \tag{2.5}$$

$$i_2 = i_1 \cdot e^{jn\pi} \cdot e^{jm\pi} = i_1 \cdot (-1)^{n+m} \tag{2.6}$$

$$i_{IF} = i_2 - i_1 = \left[(-1)^{n+m} - 1\right] \cdot i_1 \tag{2.7}$$



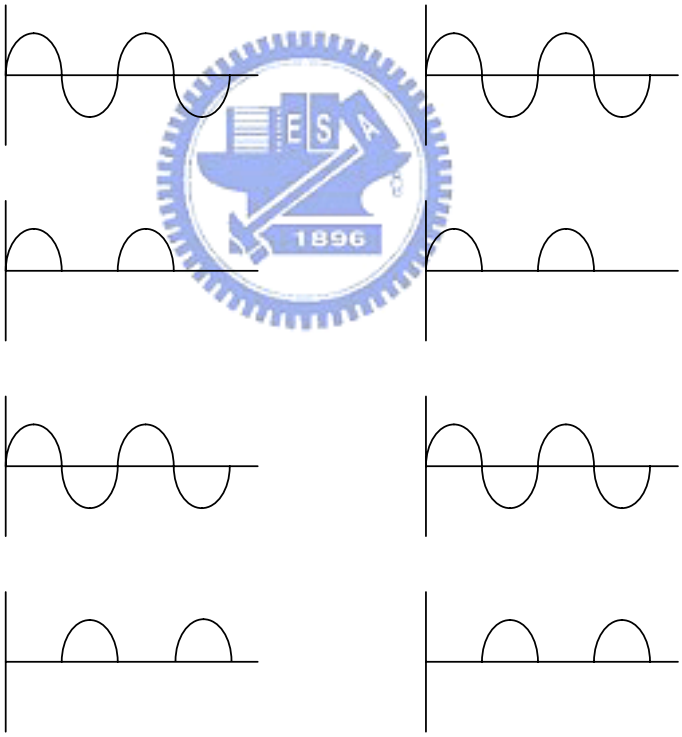


Fig. 2-2 Voltage and current flow chart of antiparallel diode pair

From the above expression, IF signal does not exist when n=1、m=－1 (LO－RF) and n=－1、m=1 (RF－LO). On the contrary, the output IF current only exist when

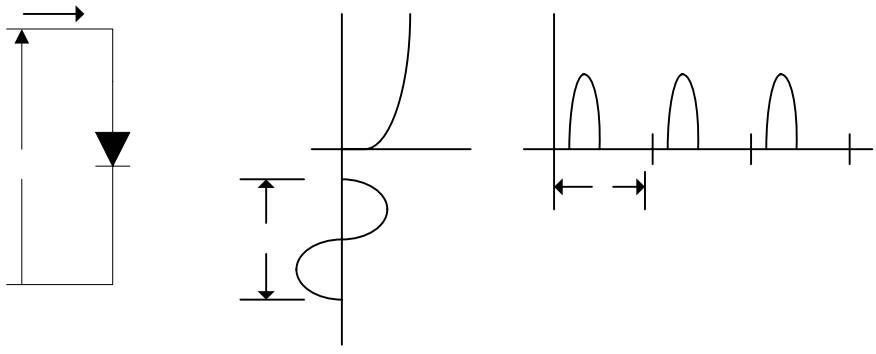
$m+n$ is an odd integer；i.e., $m+n$ = 1, 3, 5. . . . This phenomenon reveals that fundamental and other odd harmonic mixing products of the antiparallel diode pair are suppressed inherently.

II. Numeric illustration [5]:

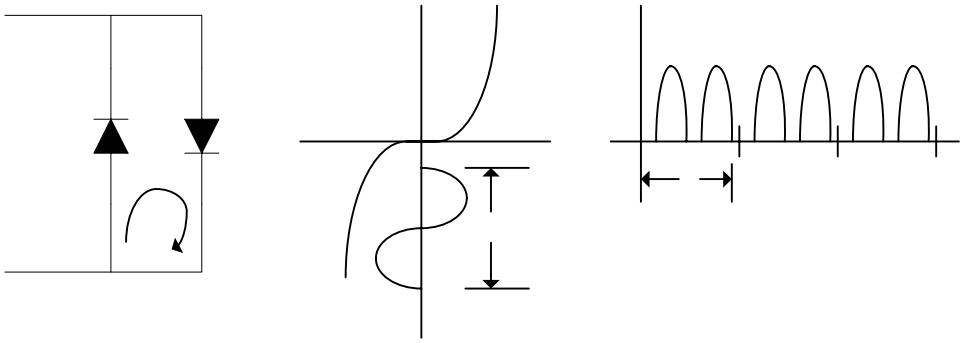
Fig.2-3(a) shows a conventional single diode mixer, the applied voltage waveform should be:

$$V = V_{LO}\sin\omega_{LO}t + V_{RF}\sin\omega_{RF}t \qquad (2.8)$$

which results in the diode current having all frequencies $mf_{RF}\pm nf_{LO}$. It will be demonstrated in this section that the total current of the antiparallel diode pair shown in Fig.2-3(b) contains only frequencies for which $m+n$ is an odd integer. All even harmonics, i.e., the terms in which $m+n$ is an even integer, fundamental mixing products ($\omega_{RF}\pm\omega_{LO}$), and the DC term exist only within the diode loop.



(a)



(b)

Fig 2-3 Mixer circuit (a) single diode mixer (b) antiparallel diode pair mixer

The instantaneous currents through the diodes i_1 and i_2 in the Fig.2-3(b) may be expressed as:

$$i_1 = -i_{RF}(e^{-\alpha V} - 1) \tag{2.9}$$

$$i_2 = i_{RF}(e^{\alpha V} - 1) \tag{2.10}$$

where α is the diode slope parameter. The differential conductance for each diode may be written as:

$$g_1 = \frac{di_1}{dV} = \alpha i_{RF} e^{-\alpha V} \tag{2.11}$$

and

$$g_2 = \frac{di_2}{dV} = \alpha i_{RF} e^{\alpha V} \tag{2.12}$$

The sum of the individual differential conductance is simply the composite time varying differential conductance g.

$$g = g_1 + g_2 = \alpha i_{RF}(e^{\alpha V} + e^{-\alpha V}) = 2\alpha i_{RF}\cosh \alpha V \tag{2.13}$$

The above expression exhibits that g has even symmetry with V, and double the number of conductance pulses per LO cycle with comparison to a single diode as illustrated in Fig.2-3(a) and (b).

For the usual case, V may be substituted

$$V = V_{LO}\cos \omega_{LO} t \tag{2.14}$$

into Equ.(2.13) with the following result

$$g = 2\alpha i_{RF}\cosh(\alpha V_{LO}\cos \omega_{LO} t) \tag{2.15}$$

Equ.(1.15) may be expended in the following series:

$$\begin{aligned} g = 2\alpha i_{RF}[&I_0(\alpha V_{LO}) + 2I_2(\alpha V_{LO})\cos 2\omega_{LO} t + \\ &+ 2I_4(\alpha V_{LO})\cos 4\omega_{LO} t + \cdots] \end{aligned} \tag{2.16}$$

where $I_n(\alpha V_{\mathrm{LO}})$ are modified Bessel functions of the second kind. Examination of the expression, the conductance components consists of a DC term plus even harmonics of the LO frequency, ω_{LO}. For the applied voltage, Equ.(2.8), the current may be expressed as:

$$i = g(V_{LO}\sin \omega_{LO} t + V_{RF}\sin \omega_{RF} t) \tag{2.17}$$

$$\begin{aligned} i = &A\cos \omega_{LO} t + B\cos \omega_{RF} t + C\cos 3\omega_{LO} t + D\cos 5\omega_{LO} t \\ &+ E\cos(2\omega_{LO} + \omega_{RF})t + F\cos(2\omega_{LO} - \omega_{RF})t \\ &+ G\cos(4\omega_{LO} + \omega_{RF})t + F\cos(4\omega_{LO} - \omega_{RF})t + \cdots \end{aligned} \tag{2.18}$$

Equ.(2.18) reveals that the total current only contains frequency terms $mf_{\mathrm{RF}} \pm nf_{\mathrm{LO}}$ where $m+n$ is an odd integer.

In the diode loop, the current i_c is indicated in the Fig.2-3(b).This circulating current is composed of the individual current i_1 and i_2 whose polarity are opposite. From Fig2-3 (b), one can mathematically describe this circulating current as

$$i_c = (i_2 - i_1)/2 = i_{RF}(\cosh \alpha V - 1) \tag{2.19}$$

Substituting Equ.(2.8) into the expansion for the hyperbolic cosine yields

$$\begin{aligned} i_c &= i_{RF}\left[1 + \frac{(V_{LO}\cos\omega_{LO}t + V_{RF}\cos\omega_{RF}t)^2}{2!} + \cdots - 1\right] \\ &= \frac{i_{RF}}{2}\begin{bmatrix} {V_{LO}}^2\cos^2\omega_{LO}t + {V_{RF}}^2\cos^2\omega_{RF}t + \\ 2V_{LO}V_{RF}\cos\omega_{LO}t\cos\omega_{RF}t + \cdots \end{bmatrix} \\ &= \frac{i_{RF}}{2}\left\{\begin{matrix} \frac{{V_{LO}}^2 + {V_{RF}}^2}{2} + \frac{{V_{LO}}^2}{2}\cos 2\omega_{LO}t + \frac{{V_{RF}}^2}{2}\cdot\cos 2\omega_{RF} \\ + V_{LO}V_{RF}\cdot[\cos(\omega_{LO} - \omega_{RF})t + \cos(\omega_{LO} + \omega_{RF})t] + \cdots \end{matrix}\right\} \end{aligned} \tag{2.20}$$

The above expression exhibits that the circulating current only contains frequencies $mf_{RF} \pm nf_{LO}$, where $m+n$ is an even integer.

Thus, the numeric analysis demonstrates that the antiparallel diode pair has the advantage of suppressing fundamental and other odd harmonic mixing products as well as even harmonics of the LO. These above-mentioned results accords with those from graphic illustration.

From above analysis, harmonic mixers employing antiparallel diode configuration could be operated at the fourth harmonic of the LO. In such mixers, the mixing products near the second harmonic must be terminated to achieve better conversion loss performance [1].

2-2-2 Circuit Design

The schematic of antiparallel diode pair subharmonic mixer is shown in Fig.2-4. The circuit is designed to mainly operate at RF frequency of 77 GHz, IF frequency of 500 MHz. In Fig.2-4, the circuit consists of five major portions, including antiparallel diode pairs, short stub, open stub, RF bandpass filter, and lowpass filter.

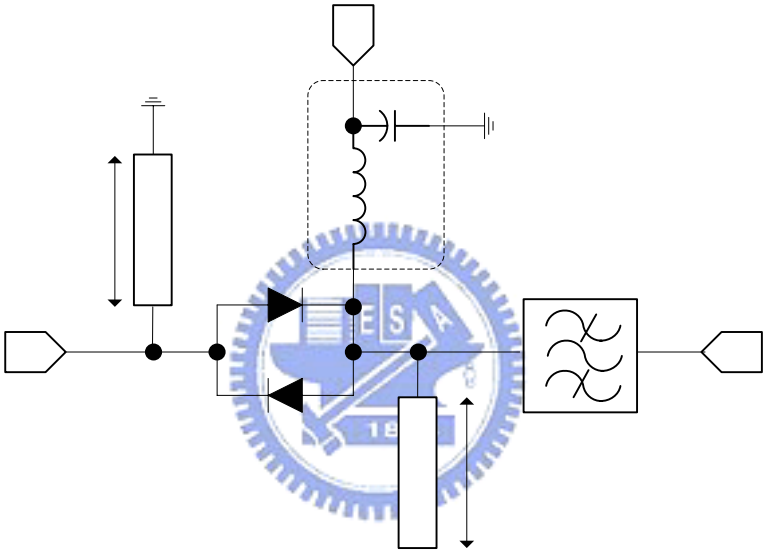
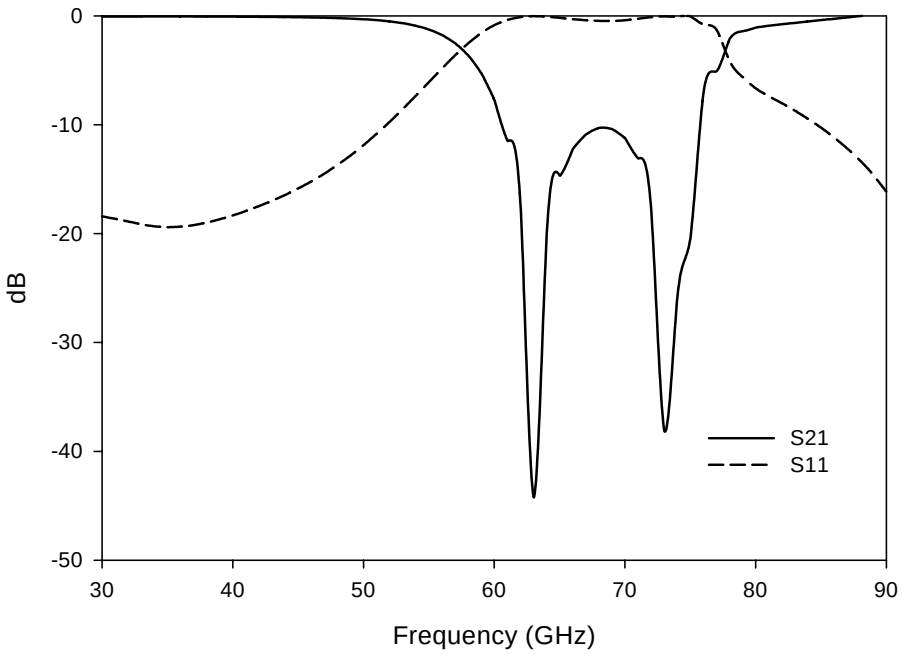


Fig.2-4 Schematic of antiparallel diode pair subharmonic mixer

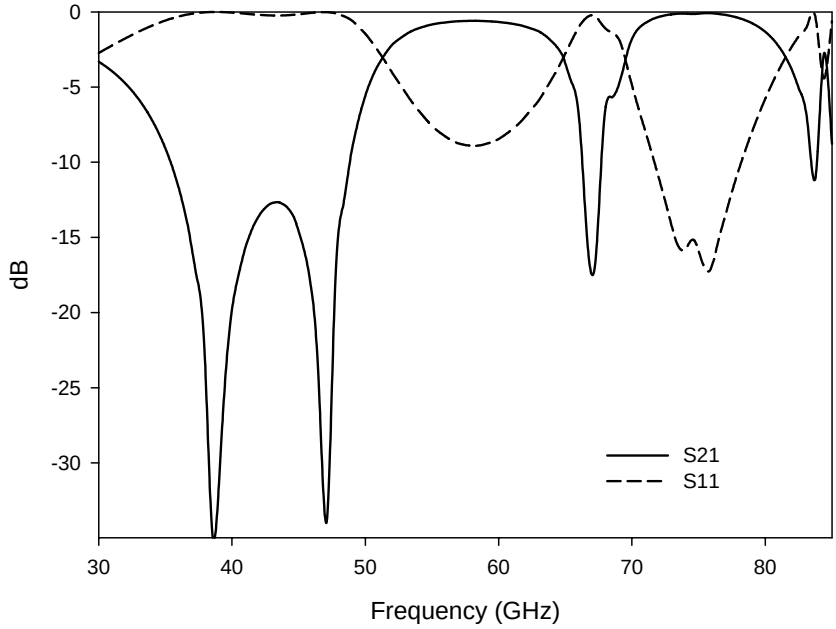
From the section 2-2-1, the antiparallel diode pairs revels that all LO's even harmonic currents can be canceled at RF and LO end. Thus, the LO's even harmonic signal is eliminated inherently at both RF and LO ports as long as the diodes are identical. The $\lambda_{LO}/4$ open stub grounds the LO signal on the right-hand side of the diodes, providing the LO signal with a return path. The RF signal is approximately two times that of the LO. Therefore, the $\lambda_{LO}/4$ open stub is about one wavelength of the RF signal and appears as an open circuit to the RF signal at the right-hand side of

the diodes. Similarly, The $\lambda_{LO}/4$ short stub appears as an open circuit at the LO frequency, and provides a return path for RF and IF.

The open and short stubs are arranged in opposite orientation to increase distance between them to reduce mutual coupling. Furthermore, the stubs must be placed as closed to pads of the diode pairs as possible. This placement provides better signal rejection of the idler signals. However, the discontinuous effects between pads and stubs have to be taken into account in simulation. Fig.2-5 shows the EM simulated results of the short and open stubs. In Fig.2-5(a), the S21 is close to 0 dB in the frequency of 30 GHz to 45 GHz, and less then -10 dB in the frequency of 60 to 77 GHz. In Fig.2-5(b), the S21 is better than -3 dB in the frequency of 70 GHz to 80 GHz, and less than -15 dB in the frequency of 37 GHz to 48 GHz.



(a)

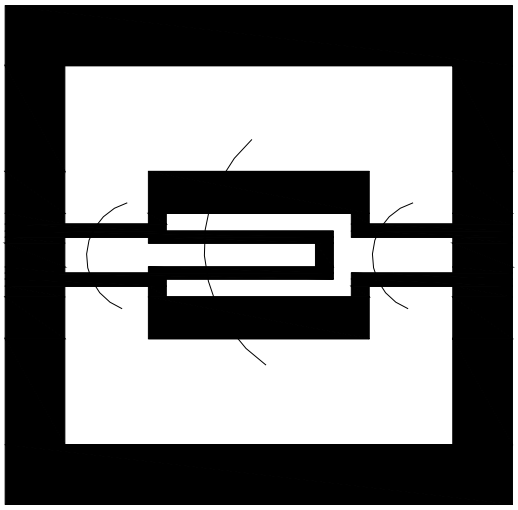


(b)

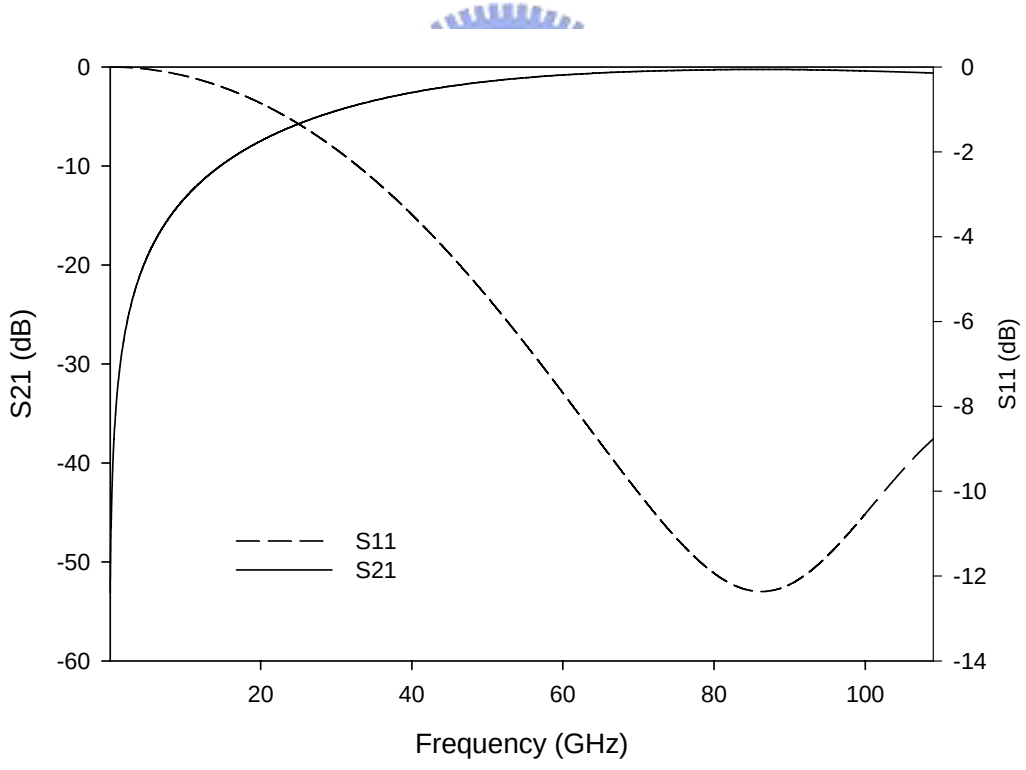
Fig.2-5 The simulated results of FCPW (a) short and (b) open stubs

The IF signal is extracted from the RF side of the diode pair. Therefore, the RF bandpass filter is essential to prevent IF leakage to the RF port. The RF bandpass filter utilizes CPW series open-circuited structure. The series open-circuited structure behaves not only as RF bandpass filter, but also DC block as well [6]. Bonding wires are required for keeping its proper propagation mode. The circuit layout and EM simulated response are depicted in Fig.2-6. The simulation result reveals that the RF bandpass filter provide good rejection below 2GHz.

The lowpass filter is formed by two bonding wire inductors and one chip capacitor. The capacitance value is 1 pF and inductance value is about 2.28 nH. This third order LPF has cut off frequency of 3.6 GHz. Using the bonding wire as the inductor is due to its very high self-resonant frequency to keep high rejection rate of the LPF at LO and RF frequencies.



(a)



(b)

Fig.2-6 (a) Layout and (b) simulated results of bandpass filter

2-3 Ring Subharmonic Mixer

Fundamental mixer incorporating a ring (rat race) hybrid is one of the most common types of mixers. However, ring mixer usually suffers the limitation of bandwidth because the conventional ring hybrid has only 15% bandwidth. In this thesis, a modified ring with an ideal phase inverter is adopted in the mixer circuit design to achieve harmonic mixing operation.

2-3-1 Harmonic Mixing Theory

Fig.2-7 (a) shows the basic configuration of ring mixers. The configuration consists of a 180 degree hybrid and two diodes. An IF filter is necessary to provide IF current return.

The RF and LO are applied to a pair of mutually isolated ports. RF and LO signals are fed to sum and delta ports respectively. The diode current flow waveform is depicted in Fig. 2-7 (b). The analysis can be derived as bellow:

The LO and RF signals are fed to the delta and sum ports of the hybrid, and the diodes is arranged in reverse direction. It reveals that the LO current of D1 is equal to that of D2, the RF current has have a period difference of $\tau_{RF}/2$ between D1 and D2.

$$i_{1LO} = i_{2LO} \tag{2.20}$$

$$i_{2RF} = i_{1RF} e^{jm\omega_{RF}\left(\frac{\tau_{RF}}{2}\right)} \tag{2.21}$$

Take the current of D1 as reference current, and each diode current could be presented in Fourier series as follows:

$$i_1 = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} g_n v_m e^{j(m\omega_{RF} + n\omega_{LO})t} \tag{2.22}$$

$$i_2 = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} g_n v_m e^{j(m\omega_{RF}+n\omega_{LO})t} e^{jm\omega_{RF}(\frac{\tau_{RF}}{2})} \tag{2.23}$$

After combining the above equations, the total currents, i.e. IF current, could be expressed as:

$$i_2 = i_1 \cdot e^{jm\pi} = i_1 \cdot (1)^n (-1)^m \tag{2.24}$$

$$i_{IF} = i_2 - i_1 = [1^n (-1)^m - 1] \cdot i_1 \tag{2.25}$$

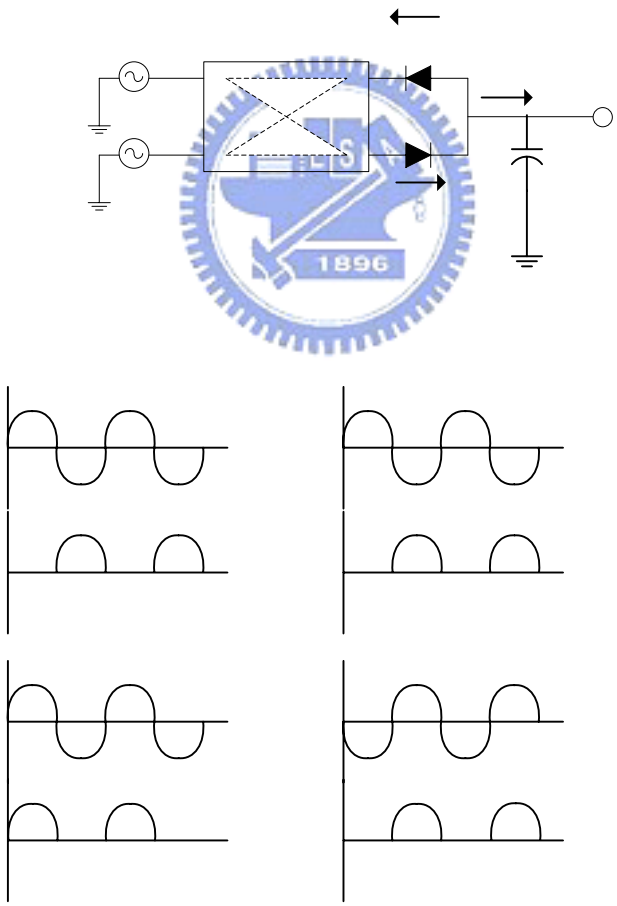


Fig.2-7 (a) ring mixer architecture (b) voltage and current flow chart

For subharmonic mixing operation, the desired IF signal frequency is the subtraction between fundamental and second harmonic of RF and LO frequency respectively, which means (m, n) = (1,-2) or (m, n) = (-1, 2). For fundamental mixing operation, the index (m, n) is (1,-1) or (-1, 1). However, if replacing subharmonic and fundamental mixing index into Equ.(2.25), the IF current will be obtained identical value. This exhibits that IF current consists of fundamental and subharmonic mixing products. Therefore, a low pass filter is necessary to eliminate the fundamental mixing products.

2-3-2 Circuit Design

Ring mixers are rarely used for harmonic mixing operation because the bandwidth of conventional hybrid is narrowband. In subharmonic mixer circuits, the bandwidth of the employed hybrid must cover an octave frequency band since the RF frequency is approximately two times of LO. The conventional ring coupler comprises four arms. One of the ring arms contains a 180 degree phase shifter, which is formed by a half wavelength line section, traditionally. Chang proposed a novel broadband ring coupler to achieve 120 % bandwidth [7]. The novel broadband ring coupler has been successfully applied to realize Ka band singly balanced mixer [8]. In this work, the mixer circuit adopts this ring structure to meet the bandwidth requirement.

Fig.2-8 shows the schematic of ring subharmonic mixer. The subharmonic mixer consists of a ring coupler, two diodes and a low pass filter formed by bonding wires and a capacitor. The ring coupler employs the broadband twist-line phase inverter, which is implemented by bonding two wires to cross the signal strip and ground strip of the FCPW line. An ultra-broadband response could be achieved by using this phase inverter rather than half wavelength line section of conventional ring couplers.

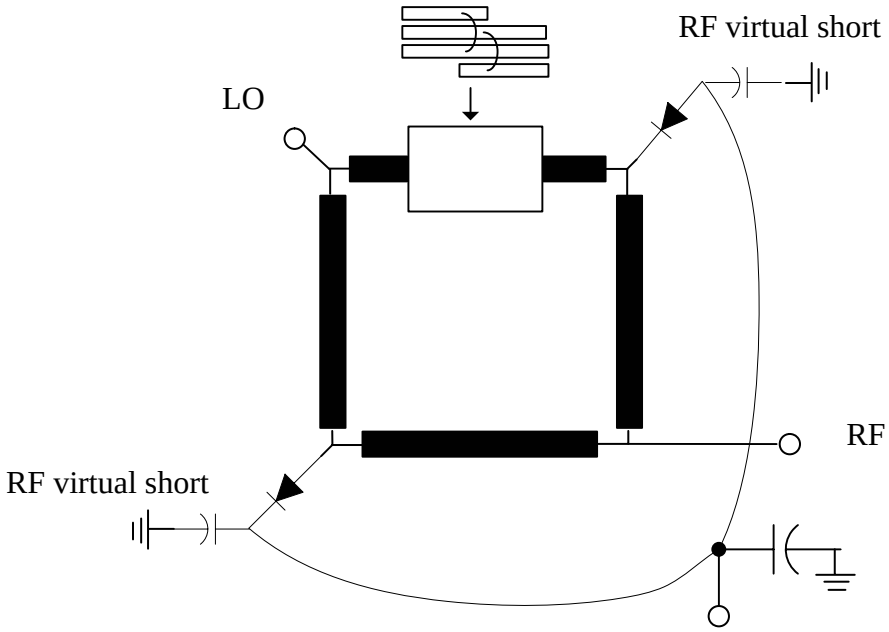


Fig.2-8 Schematic of ring subharmonic mixer

The measured performance exhibits that the ultra-broadband ring coupler has return loss below -10 dB and isolation below -15 dB from 35 GHz to 103 GHz [6]. The bandwidth of the ultra-broadband ring is broad enough for subharmonic mixing applications.

IF signal is extracted from the diode ends instead of the ring coupler. This arrangement makes the IF blocking filters (or dc blocks) unnecessary in the RF and LO ports. A low pass filter realized by two bonding wires connected between two diodes and a grounded capacitor passes IF signal and rejects other undesired signals. RF virtual short circuits connected to the diode end are essential to block IF signal leakage to ground and compensate the parasitic effect of the diode's lead.

2-4 Implementation and Measurement

2-4-1 Implementation

The antiparallel diode pair and ring subharmonic mixer are implemented using coplanar waveguide (CPW) technology. The CPW is a uniplanar structure allowing both shunt and series connection of circuit elements, and simple ground-plane connections without the need for backside metallization or the associated via holes. The CPW transmission line has several advantages for implementation, including low dispersion, low line attenuation, lower radiation loss for odd mode operation, and flexibility in designing line dimensions for a particular characteristic impedance.

Most published works on subharmonic mixer at 77GHz are using MMIC technology [1-3]. The MMIC circuits still need hybrid circuit chip-carrier-board to connect them together to form the whole radar. At 77GHz, the subharmonic mixer is one of the circuits that are possibly implemented by hybrid circuit technology. The hybrid circuit mixer should be much cheaper than MMIC subharmonic mixer because it can be fabricated on the same MMIC chip-carrier-board. The 77GHz radar front-end uses alumina (Al_2O_3) substrate as chip-carrier-board and CPW as interconnecting transmission lines is a very good combination. The CPW on alumina substrate shows very good wave guiding performance at 77 GHz. Moreover, the CPW is a very good chip-mounting environment especially at higher mm-wave frequencies because it is easy to access to the ground plane of the FCPW transmission line. We use the CPW to implement the subharmonic mixer in order to match other chip-connecting transmission lines on the chip-carrier-board.

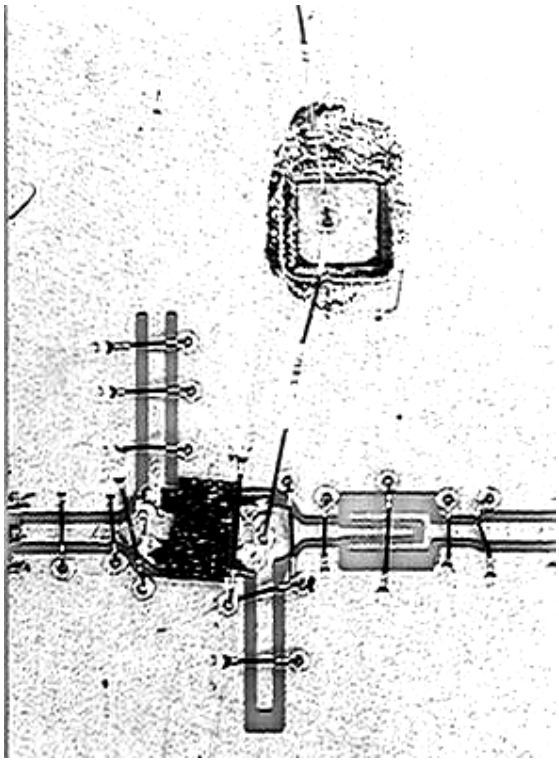
Determining a proper diode for mixer circuits is significant due to pursuit of good performance and minimizing cost. At lower frequencies, a low cost

epoxy-package diode is adequate for mixer design. However, a beamlead diode is more appropriate at higher frequencies. A beamlead diode is a chip that has integral gold ribbons, which are formed in the diode fabrication process. Beamlead diodes conform to the requirements of a small, low parasitic component having ribbon leads

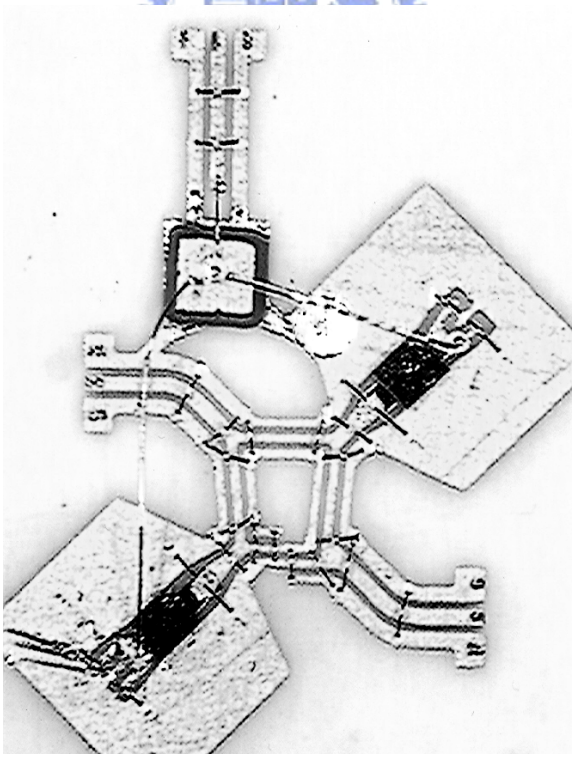
. Series resistance and junction capacitance are the most important diode parameters that strongly affect mixer performance. Low series resistance and low junction capacitance are required for the operation at high frequencies. This implies the use of a semiconductor with high carrier mobility and saturation velocity. Most Schottky diodes are realized on a silicon (Si) or gallium arsenide (GaAs) semiconductor. GaAs devices have higher electron mobility than silicon. Hence, the conversion loss performance of GaAs devices is superior to that of silicon ones for high frequency application.

Two different GaAs beamlead Schottky barrier diodes are adopted for antiparallel diode pair. The commercial diodes used in the antiparallel diode pair and ring subharmonic mixer are M/ACOM MA4E2037 and Agilent HSCH-9101. M/ACOM MA4E2037 has the junction capacitance (Cj) of 0.02pF and series resistance (Rs) of 4-7 Ohm, while Agilent HSCH-9101 has the Cj of 0.04 pF and (Rs) of 6 Ohm.

The chip capacitors used in both mixer circuits are Dielectric Lab's 1pF ceramic chip. The circuit is fabricated on a 15 mil thick alumina (Al_2O_3) substrate whose dielectric constant is 9.8. The circuit size of the antiparallel diode pair and ring mixer are 2.6 mm × 6 mm and 2.87 mm × 3.66 mm respectively.



(a)



(b)

Fig.2-9 The photograph of (a) antiparallel diode pair (b) ring subharmonic mixer

2-4-2 Measurement Results

The subharmonic mixer is measured by a probe station. The millimeter wave source is HP83650 with W band waveguide source head. The output of the RF source is calibrated by a waveguide power meter. The LO is provided by another HP83650 source with a medium power amplifier. The IF signal is measured by a spectrum analyzer where the power reading of the spectrum analyzer is calibrated.

The measured conversion loss versus RF frequency at the LO power corresponding to the minimum conversion loss when the IF frequency is fixed at 500 MHz is shown for the both mixer configuration in Fig.2-10 and Fig.2-11. The performance at 77 GHz will be specified due to the working frequency of forward-looking automotive radar application.

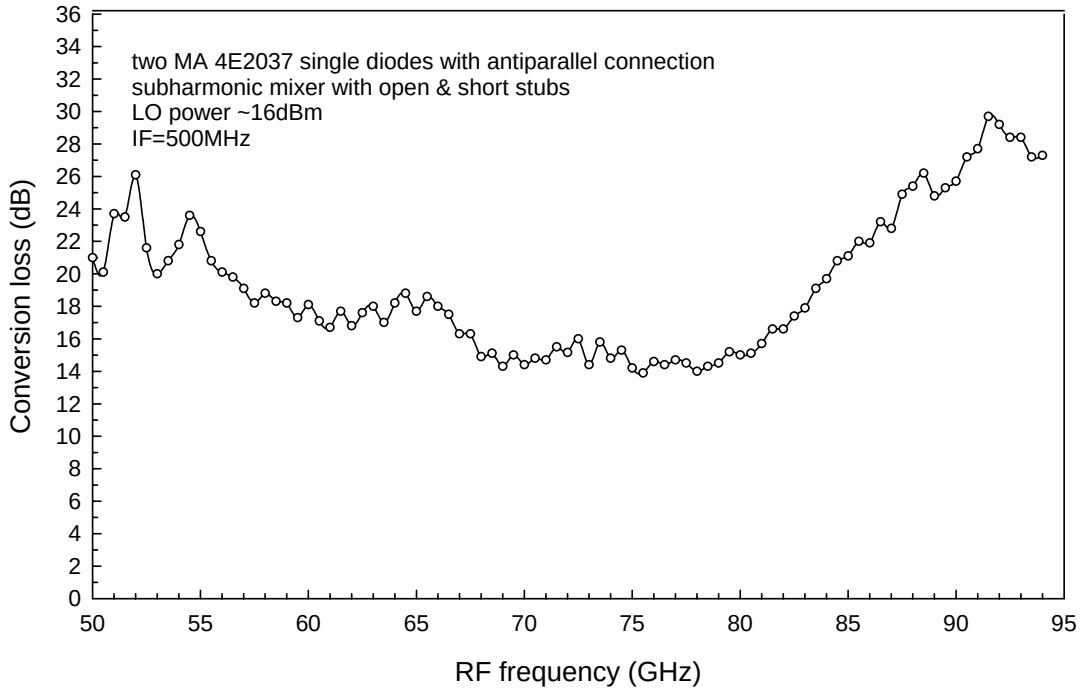
Fig.2-10 (a) shows the measured conversion loss of antiparallel diode mixer using two M/ACOM MA4E2037 diodes with a LO drive level of approximate 16 dBm. The minimum conversion loss is 14 dB at 78 GHz, and the conversion loss at 77 GHz is 14.7 dB. The measured conversion loss remains around 15 dB from 68 GHz to 81 GHz. Fig.2-10 (b) shows the measured conversion loss of antiparallel diode pair mixer using two Agilent HSCS9101 diodes with a LO drive level of approximate 19 dBm. The minimum conversion loss is 14.8dB at 67GHz, and the conversion loss at 77GHz is 24.5 dB. The measured conversion loss remains below 20dB from 64GHz to 75GHz. The measured results exhibit that the use of M/ACOM MA4E2037 has better conversion loss than the use of Agilent HSCH9101 since the junction capacitance of Agilent HSCH9101 is lager than that of MA 4E2037.

Fig.2-11 (a) shows the measured conversion loss of ring mixer using two M/ACOM MA4E2037 diodes with a LO drive level of 12 to 15 dBm. The minimum

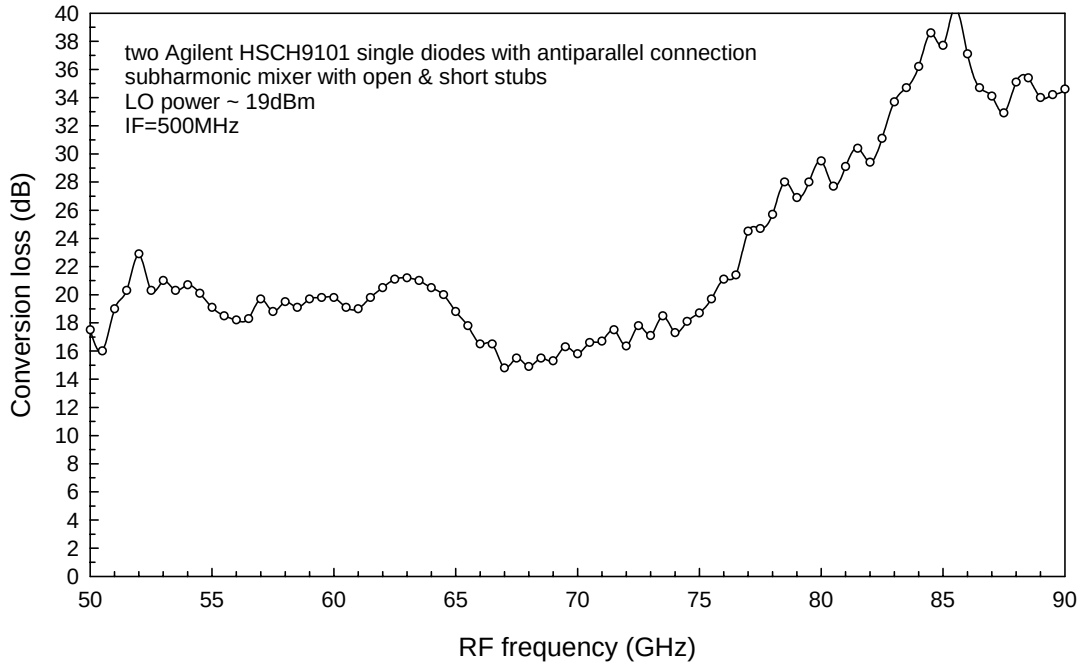
conversion loss is 12.8 dB at 95 GHz, and the conversion loss at 77 GHz is 15.7 dB. The measured conversion loss remains below 17 dB from 51.5 GHz to 95.5 GHz and about 15 dB from 70 GHz to 95 GHz. Fig.2-11 (b) shows the measured conversion loss of ring mixer using two Agilent HSCH9101 diodes with a LO drive level of 12 to 15 dBm. The minimum conversion loss is 14.1 dB at 74 GHz, and the conversion loss at 77 GHz is 16.7 dB. The measured conversion loss remains below 17 dB from 58.5 GHz to 79.5 GHz, 80.5 GHz to 90 GHz. The measured results exhibit that the use of M/ACOM MA4E2037 has slightly better conversion loss than the use of Agilent HSCH9101 since the junction capacitance of Agilent HSCH9101 is lager than that of M/ACOM MA 4E2037.

The quarter wavelength open and short stubs employed in the antiparallel diode pair mixer design suffer from the limitation of bandwidth. This phenomenon indicates that the bandwidth of ring mixer is more broadband than that of antiparallel diode pair mixer, which also can be verified from the measured performance shown in Fig.2-10 and Fig.2-11.

As shown in the measured results, antiparallel diode pair mixer has much more performed variation than ring mixer does when using two different commercial diodes. The performance of antiparallel diode pair is entirely determined by the selection of diodes. However, the performance of balance circuits mainly depends on the employed hybrid circuits. This makes that the conversion loss only degrades slightly when using Agilent HSCH9101 in the ring mixer circuits.

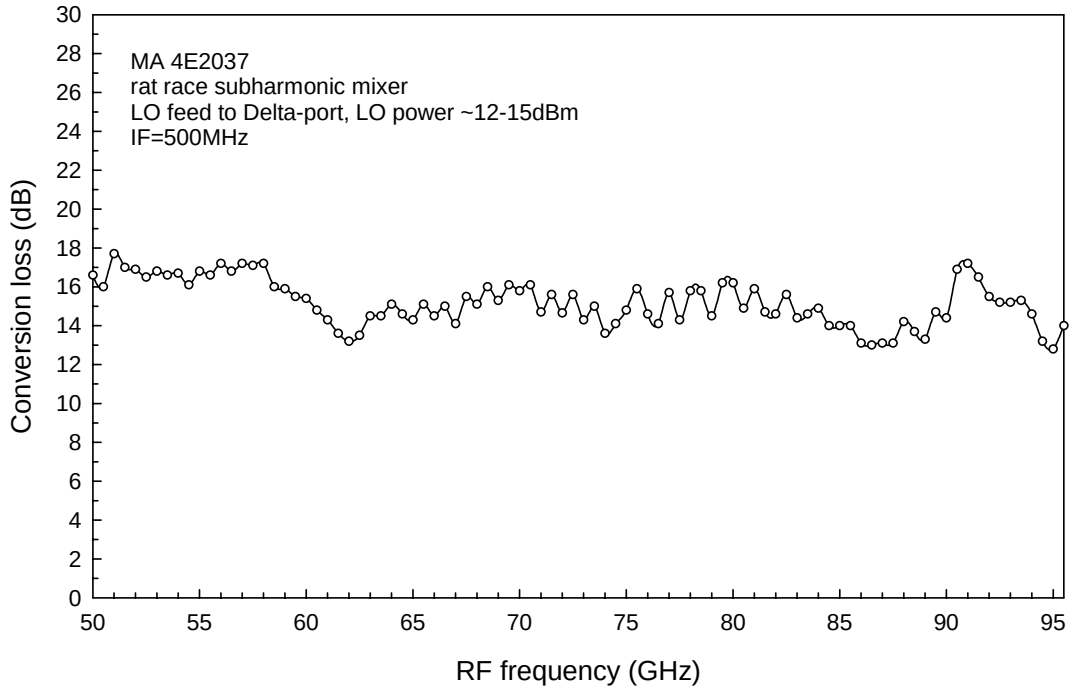


(a)

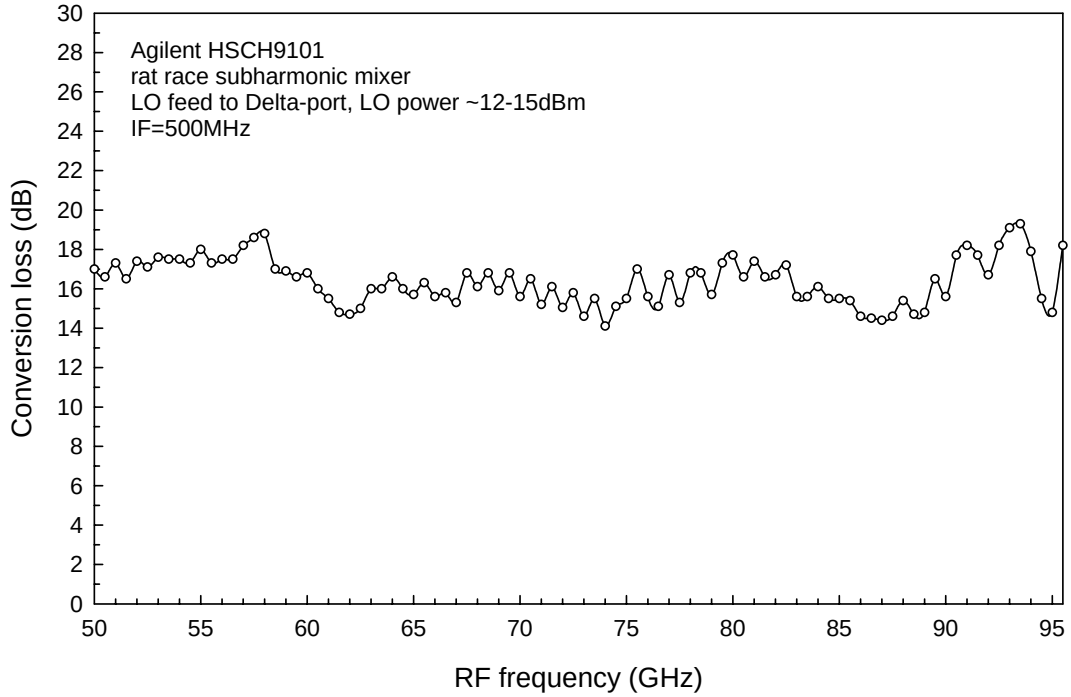


(b)

Fig.2-10 The measured conversion loss of antiparallel diode pair subharmonic mixer using (a) M/ACOM MA 4E2037 and (b) Agilient HSCH9101



(a)



(b)

Fig.2-11 The measured conversion loss of ring subharmonic mixer using (a) M/ACOM MA 4E2037 and (b) Agilient HSCH9101

Chap.3 38.5/77 GHz Frequency Doubler

3-1 Introduction

As mentioned in the chapter 1, on-vehicle collision avoidance radar is essential in the intelligent transportation system (ITS). Local oscillator sources with low phase noise are required in the forward-looking automotive radar. Signal sources can be achieved by either a fundamental 77 GHz oscillator or multiplication from a lower frequency source. The use of frequency multiplication has several advantages over than the direct design of millimeter wave frequency oscillators. Sources incorporating frequency doublers provide more reliability and accuracy than an equivalent millimeter wave frequency oscillator does. Moreover, the phase noise performance could be improved because of allowing the use of a superior technology for the lower frequency oscillators. This enables frequency doublers become more attractive in W band systems.

It is well known that frequency multiplication could be achieved by any nonlinear devices which can generate harmonics. In the diode frequency multiplier design, varactors, step-recovery diodes (SRDs) and Schottky-barrier diodes are most used nonlinear devices to generate harmonics. Varactors and SRDs circuits are reactive multipliers that make use of the diode's nonlinear capacitance characteristic. Varactors and SRDs frequency multipliers are provided with decent efficiency, low noise, but inherently narrowband. Schottky-barrier diodes (resistive diodes) frequency multipliers suffer from poor conversion loss performance, but can be made broadband if well designed. Moreover, reactive multipliers are difficult to optimize because of sensitivity of slight mistuning. In contrast, resistive multipliers are relatively easy to develop and are not nearly as sensitive [9].

HEMT (High Electron Mobility Transistor)-based frequency doublers provide more benefits compared to diode-based frequency doublers. Typically, HEMT-based frequency doublers usually consume less dc power; dissipate less heat, and better conversion loss. Moreover, small-signal FETs usually achieve better conversion gain over broad bandwidths while maintaining good DC-RF efficiency at low power level when used as frequency doublers. In contrast, diode-based frequency doublers exhibit loss [9-12].

Most published works [11-14] adopt balanced type structure to realize FET frequency doublers. Balanced type FET doublers are provided with good fundamental frequency and odd harmonics suppression and compact size, but suffer from poor conversion loss, circuit complexity and lack of balun with decent performance. Here, single-ended structure employing quarter wavelength open stubs as reflector networks is utilized to design doublers. Single-ended HEMT doublers have the advantages of better conversion loss and simple circuit topology [15].

Diode and HEMT frequency doublers are manufactured using hybrid MIC (Microwave Integrated Circuit) and MMIC (Monolithic Microwave Integrated Circuit) technologies respectively. The ceramic used for hybrid MIC circuit is alumina (Al_2O_3). The MMIC chip was fabricated using commercial available 0.15 μm GaInAs low noise pHEMT foundry service provided by WIN Semiconductor Inc.

3-2 Single Diode Frequency Doubler

Diode frequency multipliers include reactive and resistive ones, as mentioned in the previous section. Compared to reactive multipliers, resistive multipliers are significantly less efficient and limited in output power. Therefore, it is not practical to generate harmonics grater than the second for resistive diode multipliers. However, resistive multipliers have one advantage of broad bandwidth over reactive multipliers since resistive devices are inherently broadband. In this section, two configurations of Schottky barrier diode doubler will be presented and discussed.

3-2-1 Diode Frequency Multiplication Analysis

Fig.3-1 shows the simplified model of a single diode resistive frequency doubler. The model consists of an ideal diode and two ideal parallel resonant circuits. These resonators provide open circuits at resonance and short circuits at all other frequencies. These resonators represent the frequency selective parts of the matching circuits in a practical doubler. In this manner, voltage components at only fundamental and second harmonic frequency exist across diode, and only fundamental and second harmonic current circulate in the input and output respectively due to the resonators.

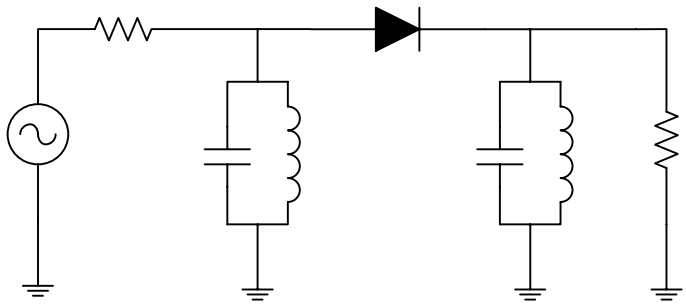


Fig.3-1 The simplified model of a resistive diode frequency doubler

A single diode frequency doubler is operated by applying a relatively large amplitude sinusoidal voltage, to the diode plus load circuit represented in Fig.3-1. The harmonic components increase as increasing applied voltage and their amplitudes tend to saturate to a constant value. The diode conducts current to the load during the positive cycle of the applied voltage. On the negative cycle, there is no current flowing in the circuit since the voltage across the diode is lower than the thermal voltage. Fig.3-2 depicts the voltage and current waveforms in the single diode doubler.

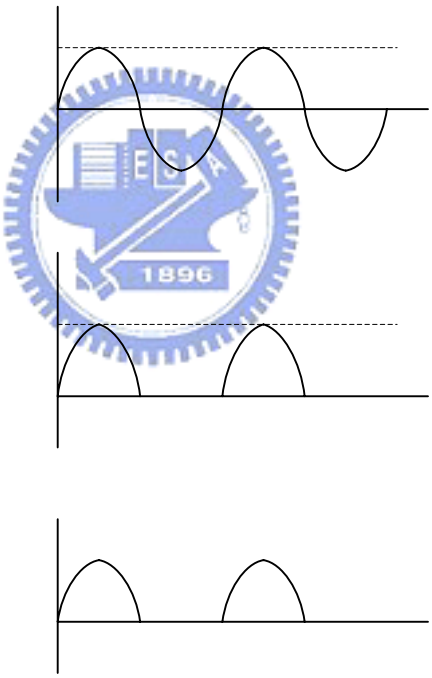


Fig. 3-2 Voltage and current waveforms in the single diode doubler

As shown in Fig.3-2, the current waveform could be adequately approximated as a series of half cosine pulse. It is apparent that half wave sinusoidal waveform is rich in even harmonics. A series of half wave rectified cosine wave can be represented in

Fourier series. From Fourier analysis, the dc component of the diode current is:

$$I_{dc} = \frac{1}{T}\int_{t_0}^{t_0+T} i(t)dt = \frac{I_{\max}}{\pi}\sin\frac{\pi}{2} = \frac{I_{\max}}{\pi} \qquad (3.1)$$

and the peak value of the fundamental current component is

$$I_1 = \frac{I_{\max}}{2} = 0.5I_{\max} \qquad (3.2)$$

and the nth harmonic current component is

$$I_n = \frac{I}{\pi}\left[\frac{\sin(1-n)\frac{\pi}{2}}{(1-n)} + \frac{\sin(1+n)\frac{\pi}{2}}{(1+n)}\right] \quad \text{for n>1} \qquad (3.3)$$

It is worth noting that the second harmonic component of diode current in the frequency doubler designs. Substituting n=2 into Equ.(3.3) yields

$$I_2 = \frac{2}{3\pi}I_{\max} \approx 0.212I_{\max} \qquad (3.4)$$

The second harmonic can be selected by adequate filtering.

Many studies indicate that resistive multipliers suffer from the limitation of efficiency. Page [10] demonstrated that the optimum efficiency of a resistive multiplier is never greater than $1/n^2$, where n is the harmonic number. For example, doubler must have at least 6 dB conversion loss. Mass [9] proved that the minimum conversion loss of a resistive doubler is only 8.8dB, even if the parasitic series resistance is zero. In practical circuits, doublers rarely have conversion loss below about 10dB.

3-2-2 Circuit Design

The single diode multiplier is the most simply constructed topologies of diode multipliers. The single diode multiplier depends heavily on filters to suppress fundamental frequency signal, while the fundamental frequency signal is inherently rejected in balanced circuits. However, the cost of two or four diodes makes balance multipliers prohibitive. Therefore, the single diode multiplier is suitable for the low cost application.

Fig.3-3 shows the schematic of frequency doubler with single series-mounted diode. Stubs of quarter wavelength at fundamental frequency provide appropriate filtering. A quarter wavelength short stub of fundamental frequency at the input side of the diode, which is equivalent to half wavelength of second harmonic frequency, provides an RF ground at 77 GHz to prevent output signals generated by the diode nonlinearity from traveling backward. Similarly, a quarter wavelength open stub of fundamental frequency at the output side of the diode grounds fundamental frequency signal.

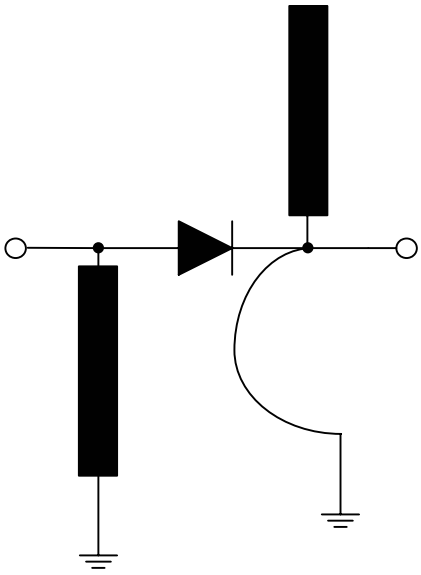
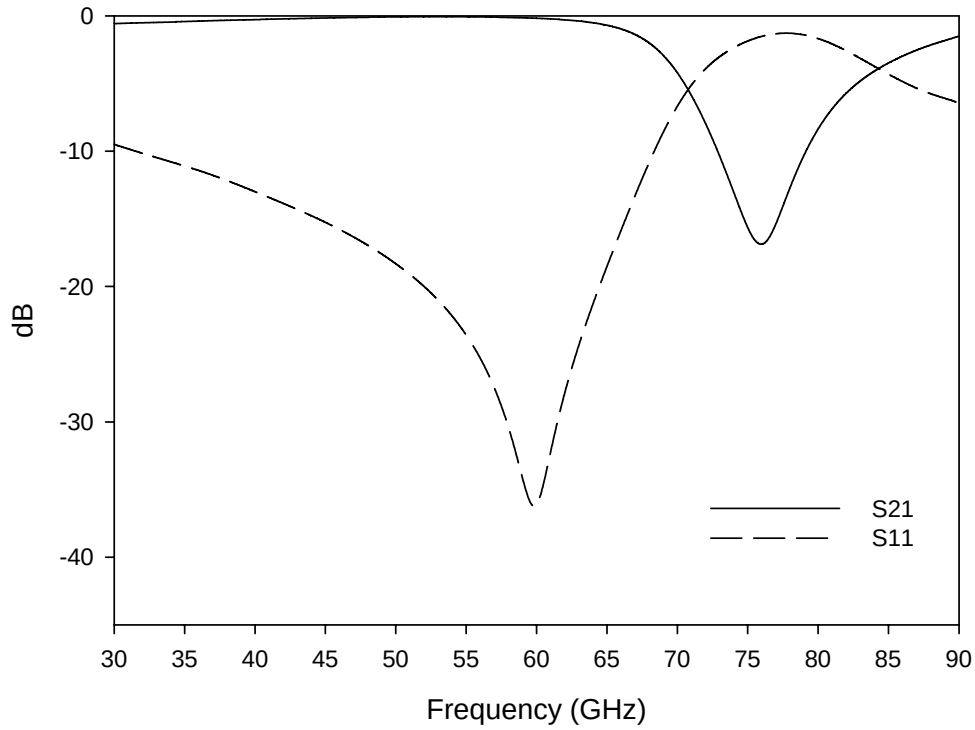


Fig.3-3 Resistive doubler with single series-mounted diode

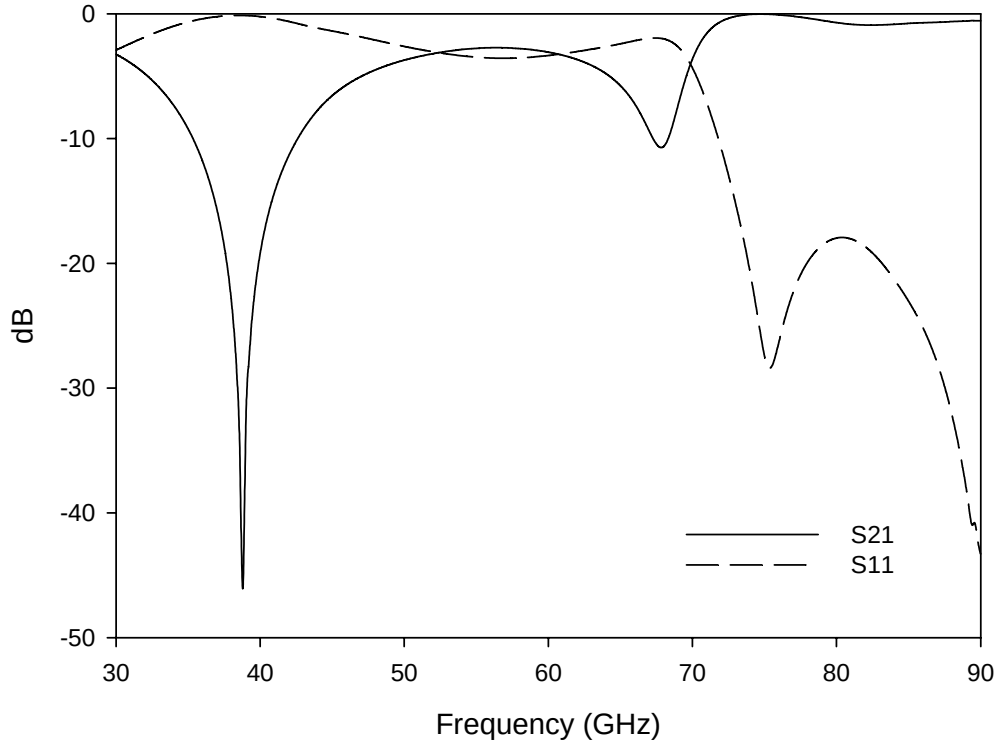
The open and short stubs in the single diode doubler circuit should be arranged in opposite orientation to avoid mutual coupling. Moreover, for best fundamental frequency rejection, these stubs are very close to the pads for mounting diodes. Fig.3-4 shows the EM simulated results of FCPW short and open stubs including junction effects between stubs and pads for mounting diodes. As shown in the figure, the short stub provides more than 15 dB rejection at 77 GHz, while the open stub provides more than 40 dB at 38.5 GHz.

In the single series-connected diode circuit, a dc current return path is needed. As shown in Fig.3-3 (a), an inductor formed by a bonding wire near the open stub provides a dc ground.

Diode selection of resistive doublers is identical to that of mixers. The junction capacitance and the series resistance of a Schottky diode should be as low as possible. However, reducing junction capacitance usually accompanies with increasing series resistance in the design of Schottky diodes. The lower diode junction capacitance leads to higher cut-off frequency but degrades power handling ability since larger diodes can handle higher power. The higher series resistance results in higher conversion loss.



(a)



(b)

Fig.3-4 Simulated results of FCPW (a) short and (b) open stubs

3-3 HEMT Frequency Doubler

The most significant disadvantage of diode frequency multipliers is that the diodes are passive elements. Circuits that use passive devices are lossy. Therefore, frequency multipliers employing active devices, such as FETs and bipolar transistor, could have better efficiency. In this section, a single-ended HEMT frequency doubler will be presented and discussed.

3-3-1 FET Frequency Multiplication Theory

In the general frequency doubler circuit design, the gate bias voltage is applied equal to or less than the turn on voltage, V_t. Consequently, the output signal conducts in pulse whose shape is approximately a rectified or half cosine. The duty cycle of the pulses is equal or less than 50 percent as $V_g \leqq V_t$.

Fig.3-5 depicts the voltage and current waveform of the ideal FET used as frequency doubler. As shown in Fig.3-1(b), the drain voltage varies between $V_{ds,max}$ and $V_{ds,min}$. $V_{ds,min}$ is the value of the drain voltage at the knee of the drain IV curve when the gate voltage is applied maximum value, $V_{g,max}$. V_{dd} and V_{gg} indicate dc drain and gate voltage, and are halfway between their maximum and minimum value. Assume that the input gate voltage shown in Fig.3-1(a) is $V_0\cos(\omega t)+V_{gg}$, where V_0 is the amplitude that has a value of half of the deference between $V_{g,max}$ and $V_{g,min}$. The waveform of the output drain current shown in Fig.3-1(c) reveals in the form of rectified cosine since drain current conducts only when input gate voltage is large than turn on voltage. The drain current has peak value Imax, and the current waveforms have the time duration t_0. The time duration is equal or less than half of the period of the excitation, T. If the drain current reaches peak value at the point t=0, the drain current can be represented in Fourier series form as:

$$I_d(t) = I_0 + I_1\cos(\omega t) + I_2\cos(2\omega t) + I_3\cos(3\omega t) + \cdots \tag{2.1}$$

where

$$I_0 = I_{\max}\frac{2t_0}{\pi T} \tag{2.2}$$

$$I_n = I_{\max}\frac{4t_0}{\pi T}\left|\frac{\cos(n\pi t_0/T)}{1-(2nt_0/T)^2}\right| \quad \text{when } n \geqq 1 \tag{2.3}$$

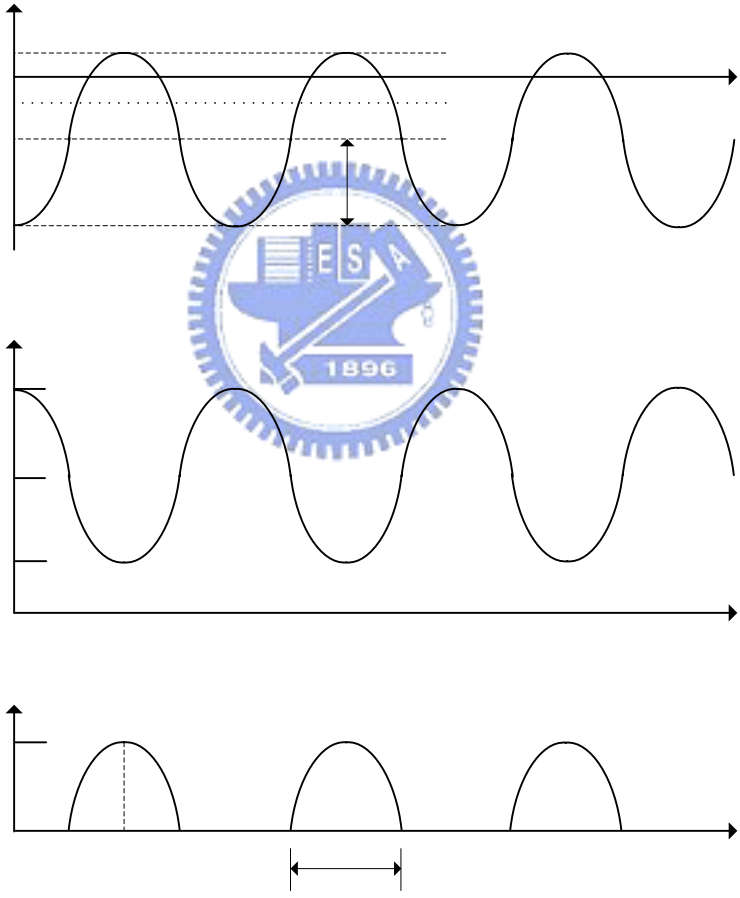


Fig.3-5 Voltage and current waveform in the ideal FET

From Equ.(2.1), the drain current consists of infinite harmonics. It reveals that nth harmonic current I_n could be determined by selecting t_0/T. Fig.3-6 exhibits a plot of I_n/I_{max} as a function of t_0/T when n=1 through n=4. As shown in figure, each of these harmonic current reaches maximum value when $t_0/T \leqq 0.5$. It would appear that the optimum value of In could be achieved by adjusting V_{gg}, so that $I_d(t)$ has the desired period conduction t_0.

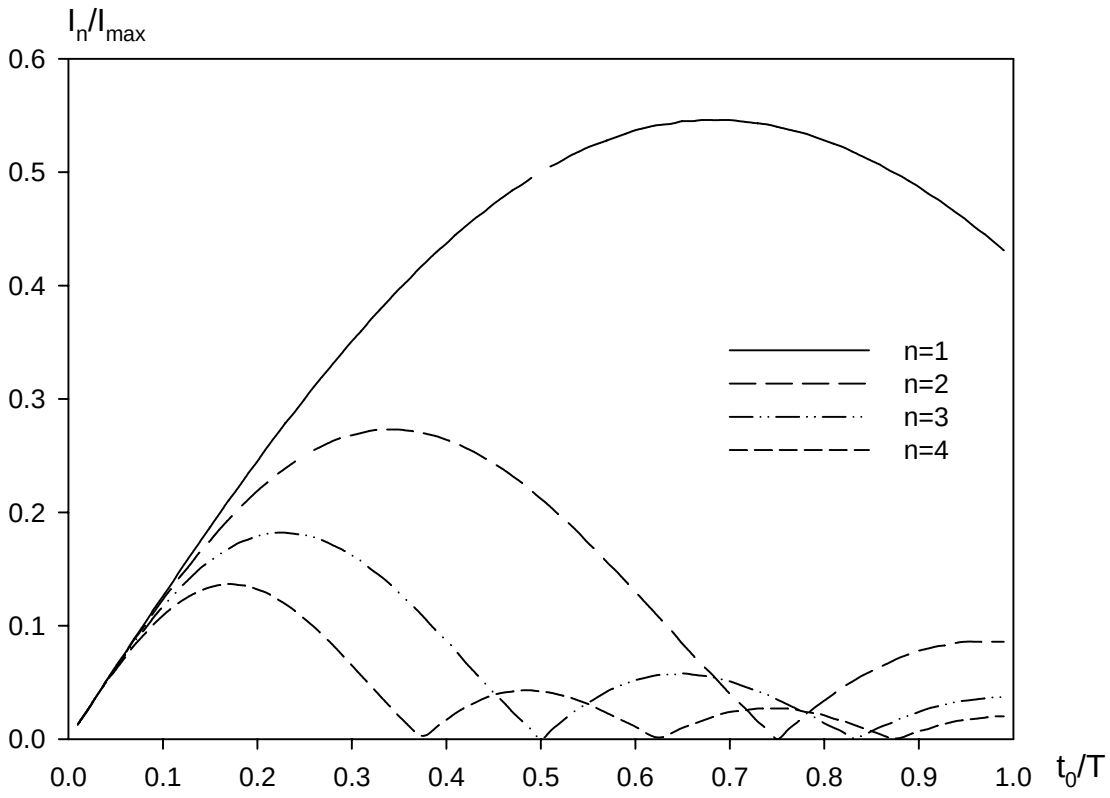


Fig.3-6 Harmonic drain current components

As depicted in Fig.3-6, the second harmonic of drain current could achieve maximum value by selecting $t_0/T=0.37$. The relation between t_0/T and conduction angle could be expressed as:

$$t_0 / T = \theta / 2\pi \qquad (2.4)$$

However, the conduction angle can be obtained from gate input voltage waveform shown in Fig.3-1(a):

$$\theta = 2\cos^{-1}\left(\frac{V_T - V_{gg}}{V_0}\right) = 2\cos^{-1}\left(\frac{2V_T - V_{g,\max} - V_{g,\min}}{V_{g,\max} - V_{g,\min}}\right) \quad (2.5)$$

From above equations, it is concluded that the efficiency and output power of nth harmonic are determined not only by drain and gate bias voltage, but also amplitude of input signal. A shorter duty cycle, which is necessary for higher harmonics, requires more negative gate voltage, Vgg, and greater RF input power [14].

3-3-2 Circuit design

At lower frequency, bipolar transistors work well as frequency multiplier. The low frequency gain of bipolar transistors is higher than that of FETs. Moreover, the nonlinearity of the base-to-emitter capacitance in bipolar transistors is much stronger than the nonlinearity of the gate-to-source capacitance in FETs. However, HEMT devices are more preferable for millimeter-wave applications.

Fig.3-7 depicts the circuit schematic of the frequency doubler. The frequency doubler is designed using microstrip lines on a 100 μm thick GaAs substrate. The HEMT device with 0.15 μm T-gates and 2×75 μm geometries, which achieves an extrinsic cut-off frequency (f_T) of 85 GHz, is adopted in the frequency doubler circuit.

As discussed in previous section, harmonic generation is heavily influenced by bias point of a FET. Frequency doublers can be biased to operate in class A or B regime. Class B doublers are biased at $V_{gg}=V_p$ and channel conducts in pulse having a duty cycle of 50%. However, class A doublers are biased at Vgg=0 and provided with higher drain current. It has been concluded from previous studies [13, 14, 16, 17] that class A doublers provide good conversion loss while class B doublers have better DC

to RF efficiency and output power.

The objective of input network is to pass the fundamental frequency component to the gate of the HEMT, while suppressing other harmonic components. Similarly, the output network rejects the fundamental and other undesired harmonic components, while passing the second harmonic component in the doubler design. In addition, the input network should be designed such that it reflects the second harmonic component back into the gate at the proper phase angle to interfere constructively for optimum conversion loss. Likewise, the output network is designed such that it reflects fundamental signal properly phased into the drain of the HEMT [18]. As shown in Fig.3-7, the input and output networks consist of shunt quarter-wavelength stubs at 38 GHz and 77 GHz, two filters served as DC blocks, and transmission lines($\Theta_1$and Θ_2) between device and shunt stubs, to meet the mentioned criteria.

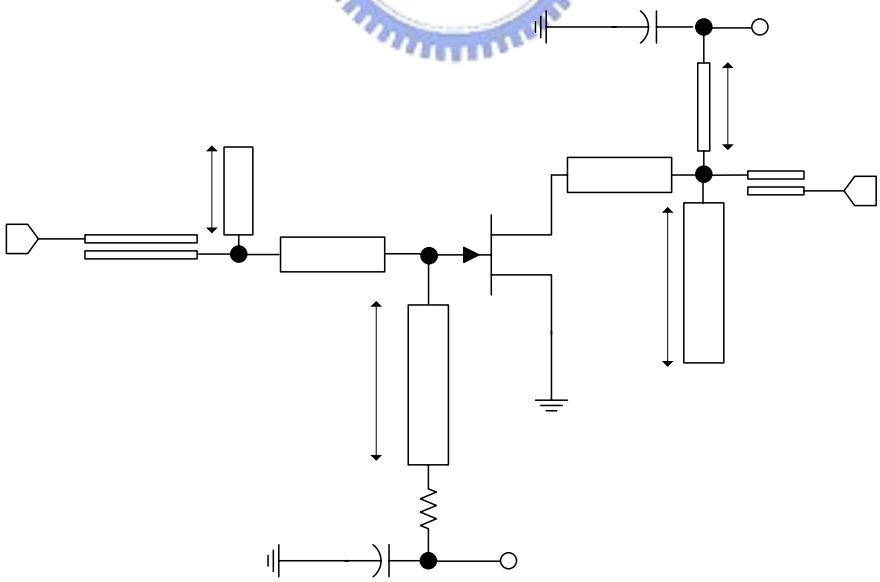


Fig.3-7 The schematic of the frequency doubler circuit

In the input network, a short-circuit stub with quarter wavelength at fundamental frequency connects the gate of the HEMT. The gate short-circuit quarter-wave stub not only passes the fundamental frequency signal and suppresses the other harmonic signal, but also serves as gate bias line. The gate bias line adds large decoupling capacitors and a 10 Ω thin film resistor to stabilize the circuit at very low frequencies. In the output network, an open-circuit stub with quarter wavelength at fundamental frequency is connected that pass the second harmonic signal and reject the fundamental signals. In both input and output networks, two bandpass filters formed by coupled-line DC blocks reinforce the filtering out-band signal performance.

Open-circuit stubs with quarter wavelength at second harmonic and fundamental frequencies in the input and output networks respectively, which is at a distance of Θ_1 and Θ_2 from the device, provides proper phase for reflecting signals back into the device from the input and output networks. In this manner, the mixing components of fundamental and harmonic signals will be degraded, and the desired harmonic signal will be enhanced, consequently [18]. The optimal conversion loss could be achieved by chosen Θ_1 and Θ_2 as 74^0 and 47^0 at second harmonic and fundamental frequency respectively. The values of Θ_1 and Θ_2 are determined by harmonic balance simulation results.

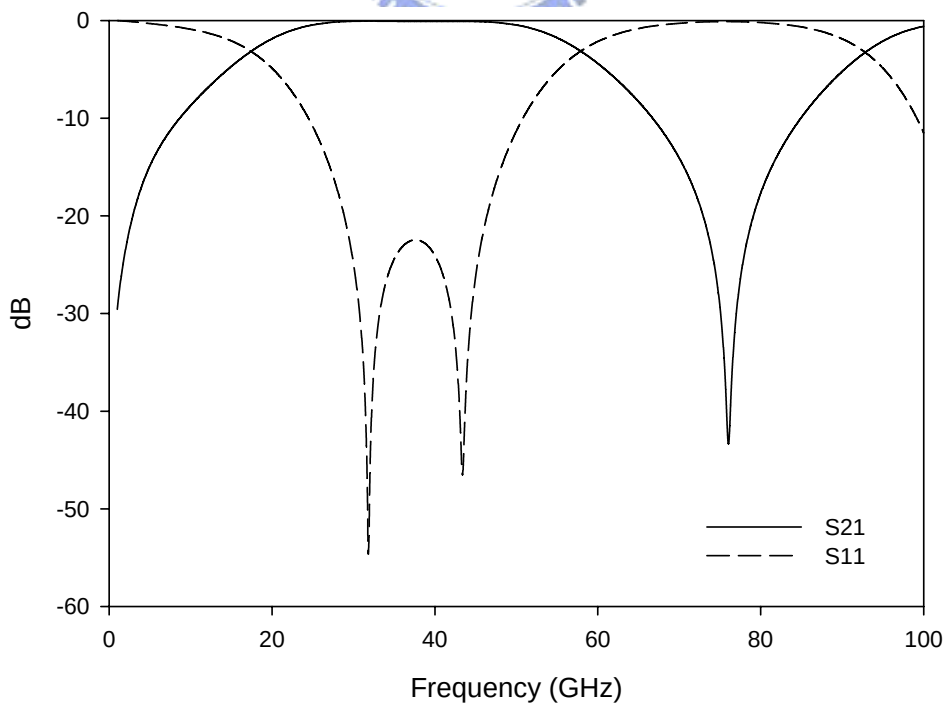
The best conversion loss could be obtained by adjusting the fundamental frequency termination, i.e. the distance between the FET's drain terminal and the short circuit reference plane of the open stub, Θ_2. However, the technique may have the expense of reducing stability margin. Rauscher [19] stated that the conversion gain heavily depends on the fundamental frequency drain termination. This method is slightly like using positive feedback in amplifier design and oscillation may occur at a

moderate length. Furthermore, the maximum output power is not largely affected by this termination.

3-3-3 Simulation

The frequency doubler is designed using a harmonic balance simulator from Agilent Advanced Design System. For the simulation of the transistor, a large signal nonlinear HEMT model [20, 21] has been employed. In addition, a full wave EM simulator, Sonnet, is utilized for passive components of the circuit to eliminate the uncertainties due to quasi-static models. The bias condition of $V_{gg} = 0$ V is selected to make the FET provide higher drain current for optimal conversion loss.

Fig.3-8 shows the EM simulation results of 38.5 GHz and 77 GHz filters respectively. As shown in the figure, the insertion loss is close to 0 dB and the return loss is less than 20 dB in the desired pass band of the both filters. This improves the filtering and suppressing performance of the circuit input and output.



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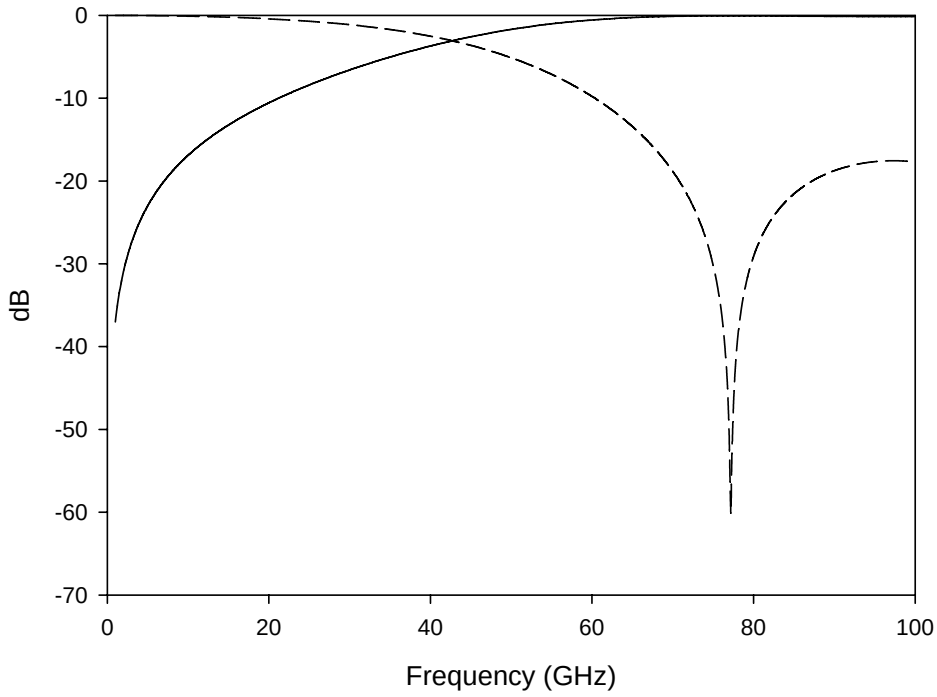


(b)

Fig.3-8 Simulated results of (a) 38.5GHz and (b) 77GHz filters

Fig.3-9, Fig.3-10 and Fig.3-11 show the simulated results from harmonic balance simulator. Fig.3-9 depicts the simulation result of conversion loss. The simulation appears that conversion loss is 4.5 dB around 77 GHz and less than 10 dB from 66 GHz to 90 GHz with an input power of 12 dBm. Fig.3-10 displays the simulated output power of fundamental, second and third harmonic signals, while input power is 12dBm. As shown in the figure, the fundamental and third harmonic components are suppressed below -20 dBm and -7 dBm, while the second harmonic signals achieves 7.6 dBm around 38.5 GHz. Fig.3-11 reveals the simulation of the conversion loss and output with different input power at the output frequency of 77 GHz. The conversion loss is below 10 dB when input power is large than 4 dBm. The output power exceeds 0 dBm when input power is larger than 6.5 dBm.

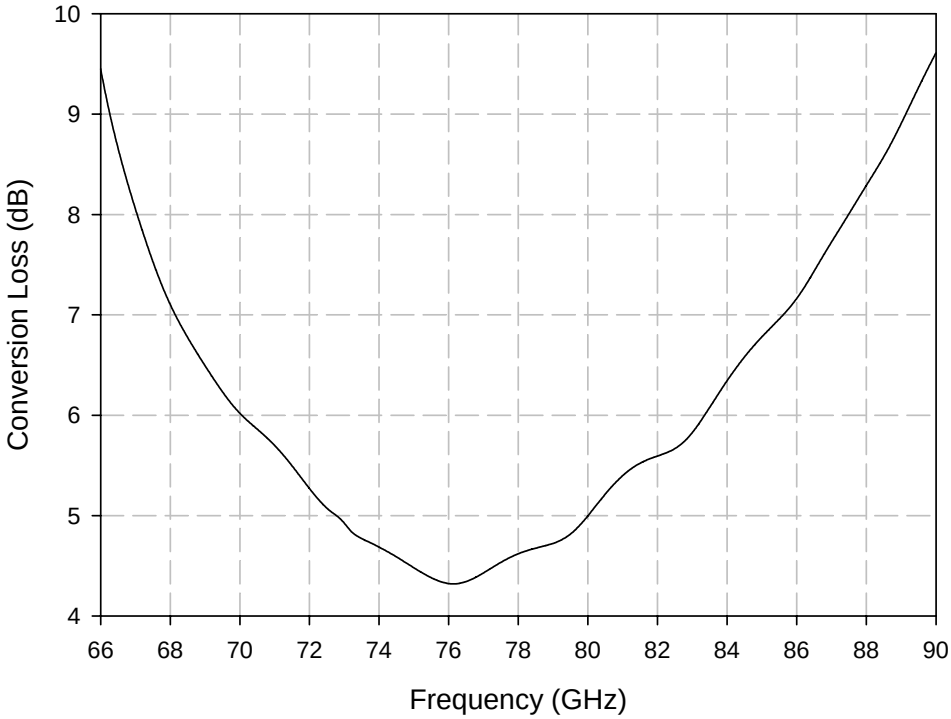


Fig.3-9 Simulated result of conversion loss (dB) V.S output frequency

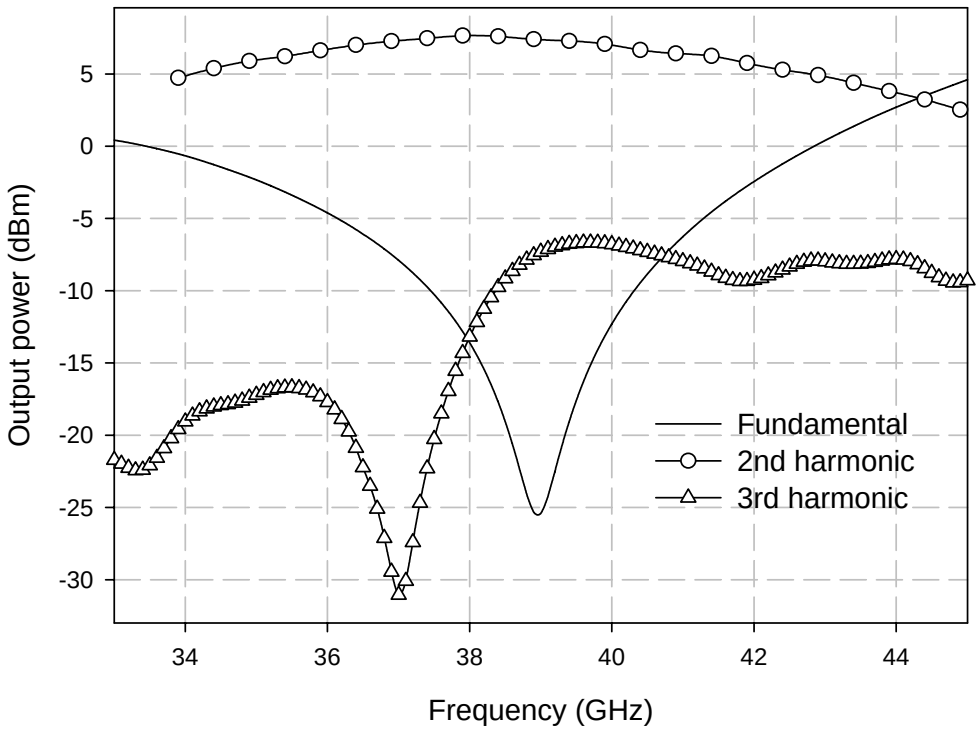


Fig.3-10. Output power simulation of fundamental, 2nd and 3rd harmonic

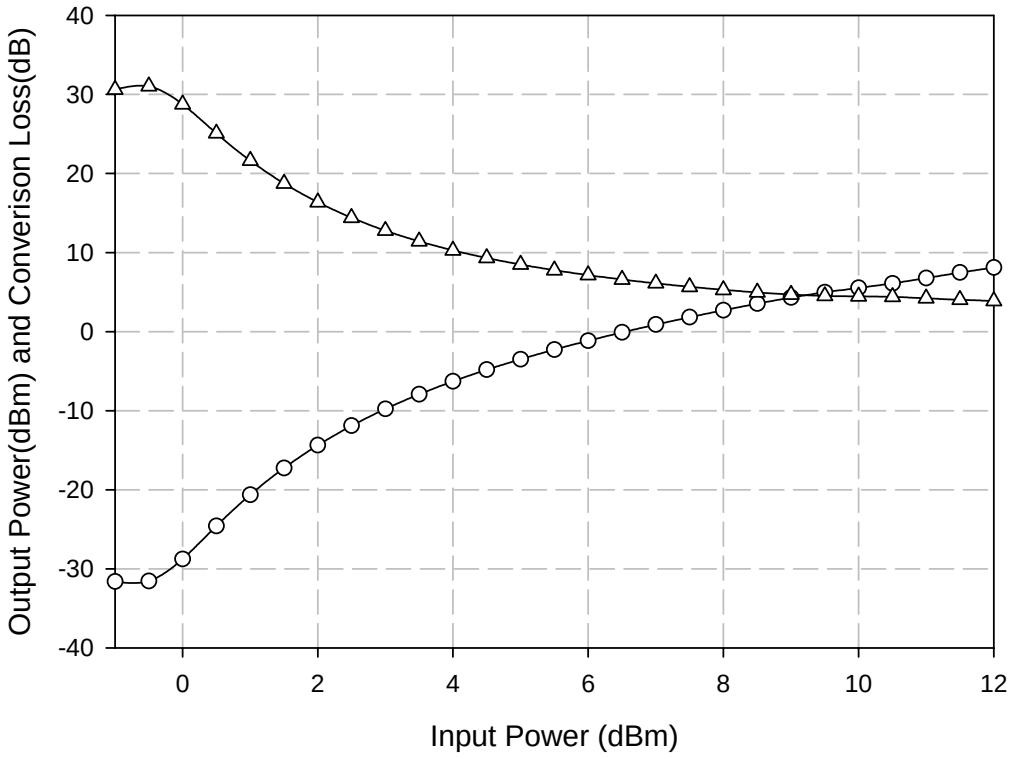


Fig.3-11. Simulation of conversion loss (dB) and output power (dBm) V.S. Pin (dBm)

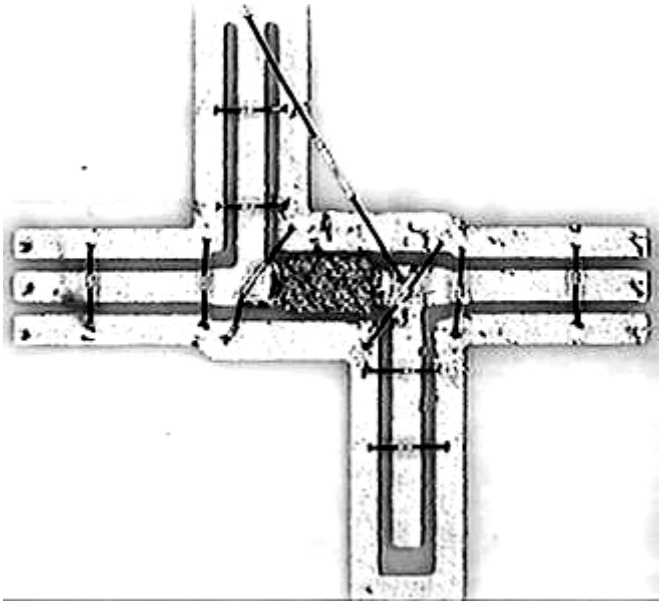
3-4 Implementation and Measurement

3-4-1 Implementation

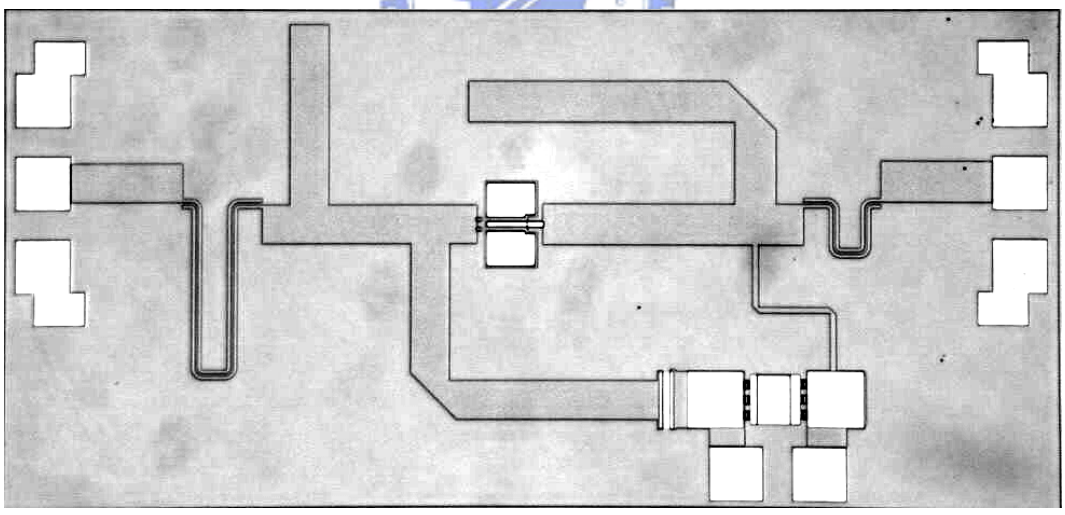
The single diode doubler was fabricated using CPW technology on a 25 mil thick alumina (Al_2O_3) substrate whose dielectric constant is 9.8. The benefit of CPW technology for hybrid MIC (microwave integrated circuit) has mentioned in section 2-3-1. The Schottky barrier diode adopted in the single diode doubler circuit is commercial M/ACOM MA4E2037, which has the junction capacitance (Cj) of 0.02 pF and series resistance (Rs) of 4-7 Ohm.

The HEMT frequency doubler was design using microstrip lines on a 100 μm thick GaAs substrate whose dielectric constant is 12.9. The MMIC fabrication process was provided by WIN Semiconductor Inc. Compared to hybrid MIC, MMIC has the advantages of smaller size, multifunctionality, higher reliability and lower parasitic effects. This makes the performance of MMIC should be superior to that of hybrid MIC. The mentioned characteristics yield MMIC more attractive in millimeter wave applications. However, the debugging and tuning mechanism in fabricated MMICs is relatively poor with comparison of hybrid MICs.

The circuit and die photograph of the single diode and HEMT frequency doublers is shown in Fig.3-12. The circuit size of the single diode doubler is 2.06 mm × 1.97 mm. The chip size of the HEMT doubler is 1 mm × 2 mm.



(a)



(b)

Fig.3-12 Photograph of (a) the single diode and (b) HEMT frequency doublers

3-4-2 Measurement Results

The frequency doublers were measured using by a probe station. An HP83650 synthesizer together with an HP83050 amplifier provides the fundamental frequency signal. The output power is measured by a W-band waveguide power sensor since the output frequency is higher than 50GHz. Using a waveguide power sensor can eliminate the fundamental signal leaked to the output because its frequency is far below the waveguide cutoff frequency. The losses of all cables and probes were calibrated out.

Because of the lack of precise nonlinear model of the commercial Schottky diode, MA4E2037, the output load has not been optimized for maximum power transfer at the second harmonic. Fig.3-13 shows the measured conversion loss versus output frequency of the single diode frequency doubler at input power of 12.5-18.6dBm. The measured results exhibits that the optimum conversion loss is 12.8 dB at 75GHz, while the conversion loss at 77 GHz is 14.2 dB. The measured conversion loss remains below 15 dB from 74 GHz to 77.5 GHz. The bandwidth is limited due to the use of quarter wavelength stubs in the doubler circuit design. A resistive doubler incorporating wideband filters could have broadband response.

Fig.3-14 shows the measured output power, conversion loss and fundamental leakage power versus output frequency of the HEMT frequency doubler at an input power of 12 dBm. The measurements were performed with a drain voltage of 3 V and a gate voltage of 0 V, which corresponds to the Idss condition. The HEMT frequency doubler achieves a minimum conversion loss of 5.96 dB and a maximum output power of 6.04 dBm at 77 GHz. The conversion loss and output power remains below 10 dB and larger than 0 dBm respectively from 69 GHz to 83 GHz. The fundamental leakage power at 77 GHz is -7.3 dBm, which corresponds to an isolation of 19.3 dB.

Fig.3-15 shows the measured output power and conversion loss versus input power at 77 GHz. As shown in the figure, the output power exceeds 0 dBm as input power is large than 6 dBm, and the conversion loss remains below 10 dB as input power is larger than 2 dBm. In the small signal operation, the HEMT doubler might have conversion gain if input and output circuits are well matched.

From measured results of both circuits, HEMT doubler obviously achieves better conversion loss compared to single diode doubler. However, single ended HEMT doubler suffers from fundamental leakages since HEMT is an amplifying device after all. Some studies [9, 21] indicate that an additional open stub of quarter wavelength at fundamental frequency in the output can provide better fundamental rejection for single ended device circuits.

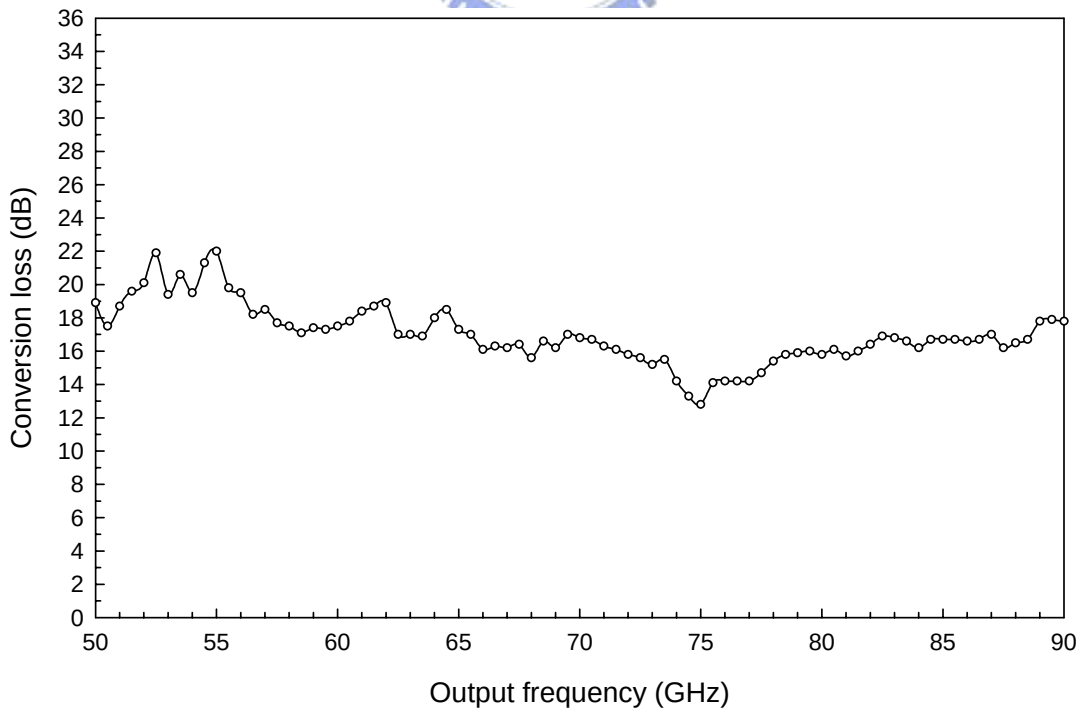


Fig.3-13 The measured conversion loss of single diode frequency doubler

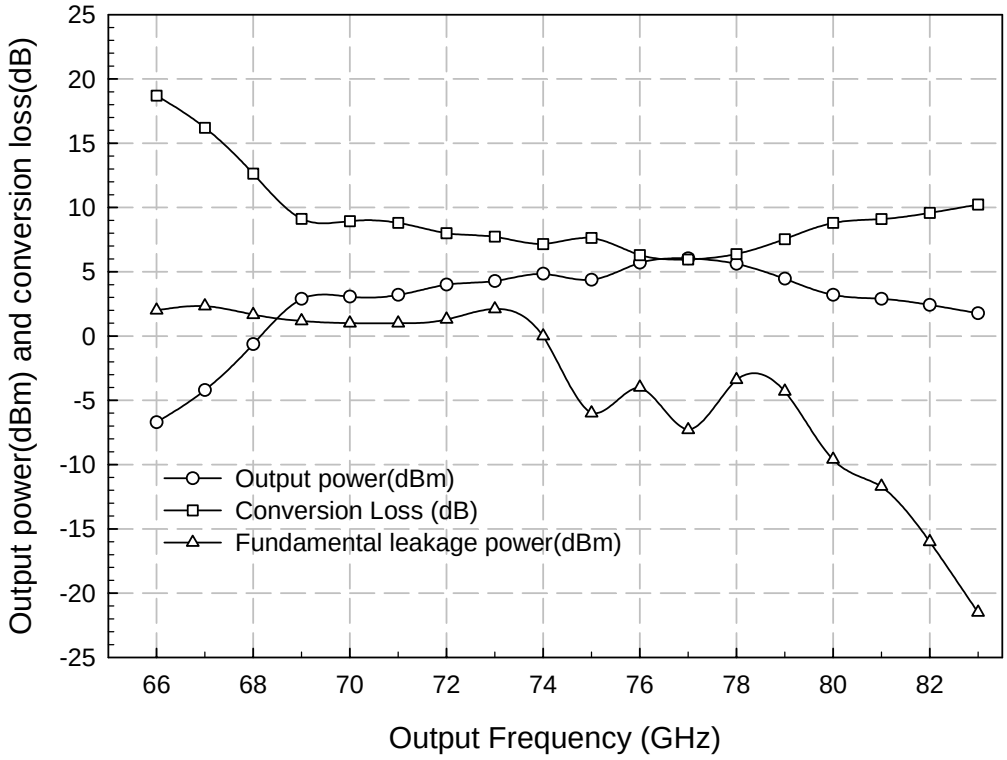


Fig.3-14 The measured output power (dBm), conversion loss (dB), and fundamental leakage power (dBm) versus output frequency (GHz)

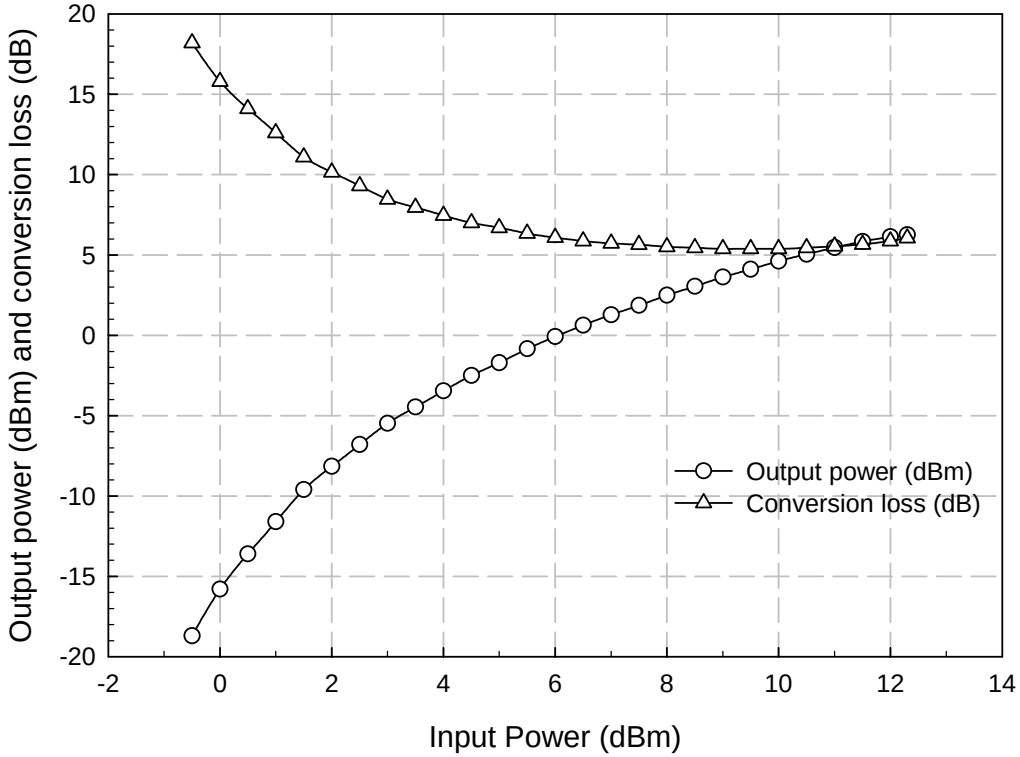


Fig.3-15 The measured output power (dBm) and conversion loss (dB) versus input power at 77GHz

Chap.4 Conclusion

The thesis proposes subharmonic mixers and frequency doublers for automotive radar application whose frequency frontier is 77 GHz. In addition, design methodologies and implementation techniques have been also widely discussed and described.

For the subharmonic mixer design, antiparallel diode pair configuration is most used to generate subharmonic mixing response. The subharmonic mixer incorporating antiparallel diode pair usually has the bandwidth limitation due to the use of quarter wavelength stubs. From measured results of mounting two different diodes, it is obvious that lower junction capacitance is essential in high frequency operation. The subharmonic mixer incorporating a rat-race ring has much more broad bandwidth response due to the use a ultra wideband hybrid circuit. The performance of balance circuits is determined by employed hybrid circuits.

For the frequency doubler design, diodes and transistors can be used as nonlinear device to generate harmonics. Single diode frequency is the simplest topology, but has the bandwidth limitation due to the use of quarter wavelength stubs for filtering unwanted signals. Furthermore, in this thesis, single diode doubler is apparently low efficiency because the circuit adopts resistive device, Schottky barrier diode, rather than varactors. The HEMT frequency doubler is clearly much efficient than passive doubler. In the HEMT frequency doubler design, the optimal conversion loss could be obtained by adjusting the length between drain of HEMT and the fundamental termination. The HEMT frequency doubler in the thesis adopts single end topology, which has a major problem of fundamental frequency leakage at the output. It is more difficult to filter the output of an active doubler than a passive one because FET

amplifies the applied fundamental frequency excitation. Balance doublers may solve the fundamental leakage problem. However, balance circuits not only employ a hybrid circuit occupying large areas for MMIC circuit but also consume much dc power due do the use of two transistors. The topology selection between single ended and balanced types is determined by efficiency, fundamental leakage, circuit complexity and dc power consumption trade-off.

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