國立交通大學

光電工程研究所

碩士論文

以溶液製程製作鋯銦鋅氧化物半導體薄膜電晶體

Solution-Processed ZrInZnO

Semiconductor for Thin Film Transistors

研究生：鍾亞衛

指導教授：陳方中 博士

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中文摘要

本研究選用鋯銦鋅氧化物(ZrInZnO)為薄膜電晶體的主動層，不同於以往使用濺鍍的方式，而是以溶液製程的方式旋轉塗佈在矽-二氧化矽基板上當做主動層，並以鋁當作電極材料，研究其元件特性。當 Zr 的含量增加時，關閉電流也會隨之下降。當 ZrInZnO 的比例為 Zr: In: Zn = 0.1: 5: 5 時，場效遷移率為 $3.8 \text{cm}^2/\text{Vs}$，開關電流比大約為 10^7，截止電壓為 0.44V，次臨界擺幅為 0.42 V/dec。在壓力測試中，ZIZO 在 10 伏特的偏壓下一段時間後，截止電壓的漂移亦能保持穩定。 ZIZO 薄膜結晶為非晶型，Zr 原子能有效地控制氧空缺和提供自由電子。XPS 證明當 Zr 含量增加時，氧原子 1s 的鍵結峰值減少，此即為氧空缺數量減少的證據。除此之外，我們還發現添加氫氧化鈉(NaOH)能使 ZIZO 的薄膜更加穩定並且加速 ZIZO 的結晶化反應，減少元件的製作時間。

Solution-Processed ZrInZnO Semiconductor for Oxide Thin Film Transistors

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Abstract

Solution-processed ZrInZnO (ZIZO) semiconductors have been fabricated as the channel material for thin film transistors (TFTs). As the amount of Zr content increased, the off current decreased. The ZIZO TFTs fabrication with the ratio of Zr: In: Zn = 0.1: 5: 5 exhibited a field effect mobility of 3.8 cm^2/Vs, an on-off ratio of ~10^7, a threshold voltage (V_{th}) of 0.44 V and the subthreshold swing of 0.42 V/dec. The threshold voltage also became stable under the bias stress. We found that the ZIZO thin film was amorphous. However, when pre-annealing temperature increased, the degree of micro-crystallization was improved. We interred that the Zr effectively controlled the oxygen vacancies and supplied the concentration of free electron. X-ray photoelectron spectroscopy verified that the oxygen 1s peak decreased with the Zr increasing content. Therefore, it proved that oxygen vacancies decreased with adding the Zr. In addition, we found that adding NaOH could make the ZIZO thin film more stable and accelerate the chemical sol-gel reaction. Overall the device performance is almost comparable with that of the device made by conventional cosputtering methods.

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Chapter 1

Introduction

1.1   Preface

Thin film transistors (TFTs) have been widely employed as the pixel-driving elements for flat panel displays (FPDs), such as active-matrix liquid-crystal display (AMLCDs) [1] and active matrix organic light-emitting diodes (AMOLEDs) [2]. There are two factors affecting the performance of active matrix TFTs backplanes: the individual pixels and the interconnection lines. Normally, an active matrix TFTs backplane is composed of an array of pixels connected with vertical and horizontal programming lines. From Fig. 1-1, it shows the schematic of the active matrix. Scan lines are connected to gates of switching TFTs of the pixels, data lines are used to drive TFTs sources, and drains are connected to the liquid crystal (LC). Fig. 1-2 shows the cross section of a pixel in a TFT LCD. Each pixel includes TFTs devices, polarizer, color filter, spacer, alignment layer and liquid crystal, etc.

TFTs devices can be divided into three types by the crystal structure of the active layer: amorphous state, polycrystalline state and crystalline state as shown in Fig. 1-3. The field effect mobility of amorphous silicon (a-Si) is lower than poly-crystal silicon (poly-Si) due to its messy amorphous state. In practical applications, due to the grain boundary, poly-Si TFTs are suitable for the small size

flat panel display. On the other hand, the a-Si TFTs are often applied in large size flat panel display on account of its mature manufacture and low fabrication cost. There are two disadvantages of a-Si including visible light sensitivity and low field-effect mobility, which reduce the pixel aperture ratio and driving ability.

Besides, a new electronics is emerging for applications which cannot be fabricated by silicon metal oxide semiconductor (MOS) technology. Recently, metal oxide semiconductor based TFTs have attracted much attention for future applications such as flexible and transparent displays [3, 4, 5]. This is due to their unique electrical and optical properties which are transparent in visible light, deposition at low process temperature, and high field effect mobility. In particular, we can control the resistivity of metal oxide semiconductors through controlling the oxygen partial pressure [6].
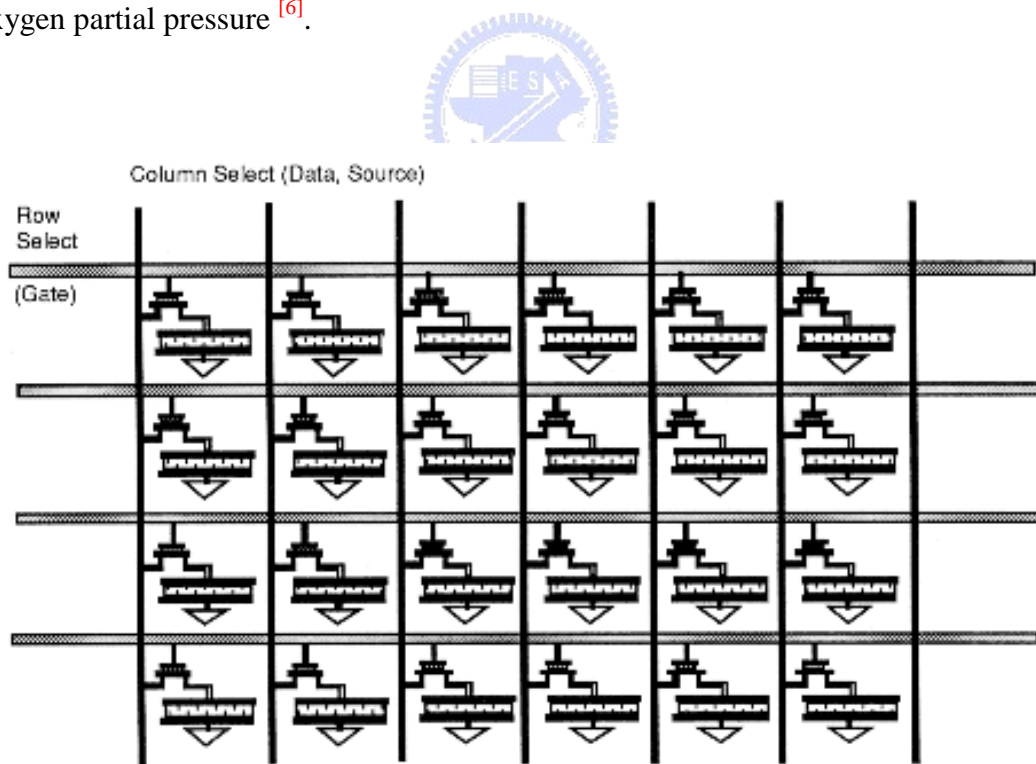
Figure 1.1   Schematic of an active matrix display layout.

[Adapted from http://www.wtec.org/loyola/dsply_jp/c5_s2.htm]

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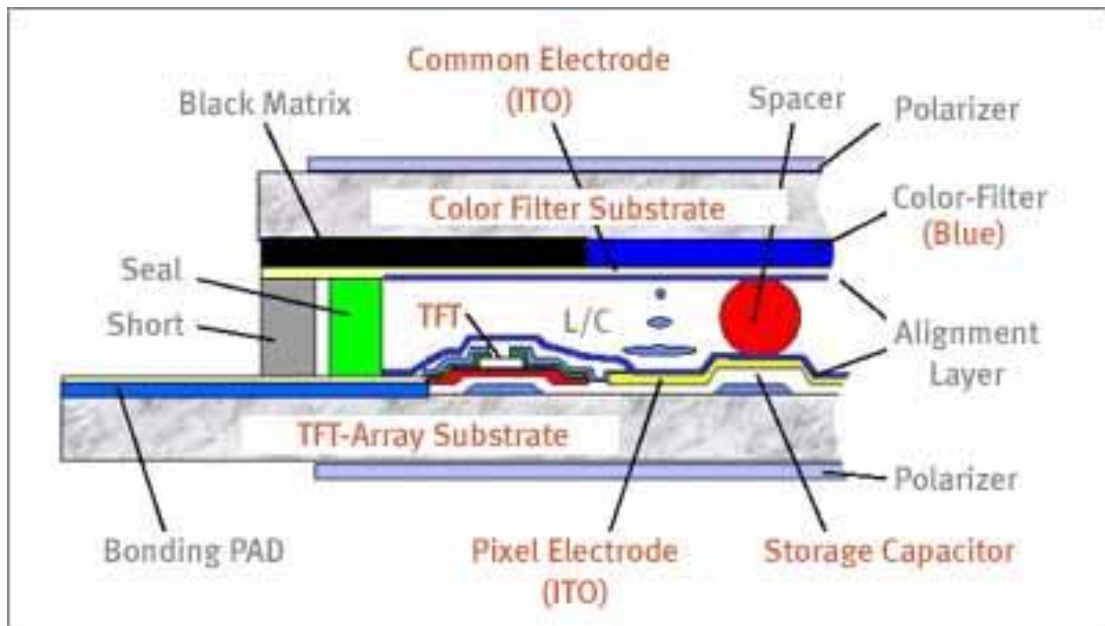
Figure 1.2   Cross section of a pixel in a TFT LCD.

[Adapted from http://digitalworld-mirror.blogspot.com/2008_09_01_archive.html]

Crystalline   Polycrystalline   Amorphous
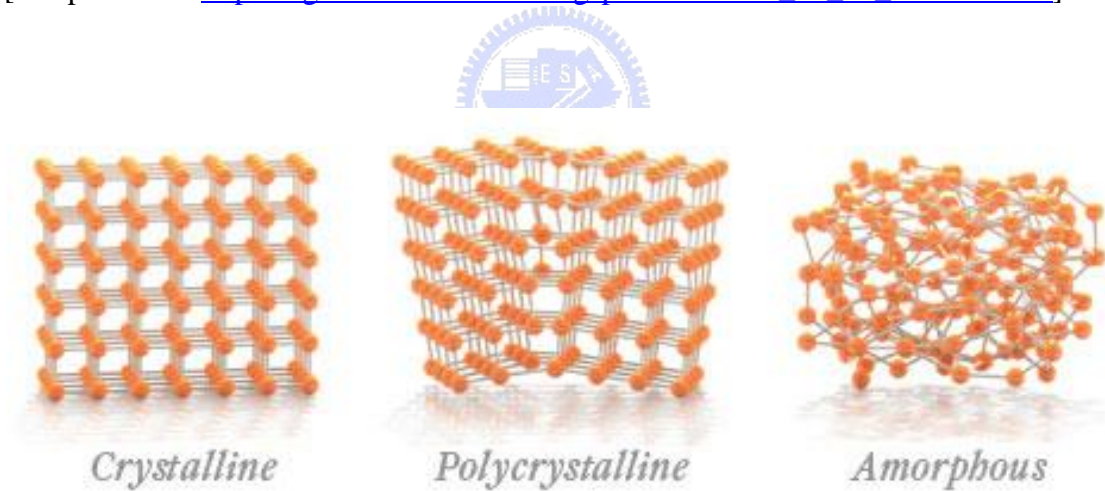
Figure 1.3   The structure of the active layer.

[Adapted from

http://spectrum.ieee.org/semiconductors/materials/thin-fast-and-flexible-semiconduct

ors/0]

1.2　　Oxide Thin Film Transistors

The thin film metal oxide materials like SnO_2, In_2O_3, ZnO, CdO and their alloys have many advantages such as visible light transparency and high electrical conductivity [7]. Especially, indium tin oxide (ITO) is well known to the display industry. These metal oxide materials can also have semi-conductive properties to be used as the active layer of TFTs [8].

In recent years, these metal oxide TFTs have been reported to exhibit field effect mobility above 10 cm^2/Vs even in the amorphous state, which is more than one order of magnitude compared to that of the traditional a-Si TFTs [9, 10]. The mobility of a-Si:H TFTs is limited to around 1 cm^2/Vs which is associated with the intrinsic nature of the chemical bonding. Fig. 1-4 (a) illustrates average carrier transport paths in covalent semiconductors such as a-Si:H which consists of sp^3 orbitals with strong directivity. The bond angle fluctuation significantly alters the electronic levels, causing the high density traps deep of tail-states. In contrast, metal oxide semiconductors contained post transition metal cations with the $(n-1)d^{10}ns^0$ electron configuration, where n ≥ 5, leading to a large mobility (**>** 10 cm^2/Vs) [4]. Fig. 1-4 (b) illustrates the carrier transport path in metal oxide semiconductors which are composed of spatially spread ns orbital with an isotropic shape, where the ns orbital overlap among the neighbouring orbital directly. The isotropic of the ns orbital is insensitive to the disorder structure which intrinsically exists in amorphous materials that can avoid significant degradation of transport properties [11]. This feature shows why the field effect mobility of amorphous metal oxide semiconductors is similar to the corresponding crystalline phase, even under the room temperature deposition process. The amorphous metal oxide semiconductor based TFTs can be one of the promising candidates for the increase in the size of the flat panel display because of

their high mobility and good uniformity.

Zinc oxide (ZnO) is a conventional metal oxide semiconductor which is polycrystalline state in nature even at room temperature. The grain boundaries of such metal oxides affect device properties, uniformity and stability over large areas. The ZnO-based semiconductors such as In-Zn-O, Zn-Sn-O and In-Ga-Zn-O can be amorphous state at room temperature and have been proposed as the active layer in TFTs [12, 13, 14]. These amorphous ZnO-based TFTs overcome the drawbacks of a-Si:H and poly-Si TFTs in flat panel displays.
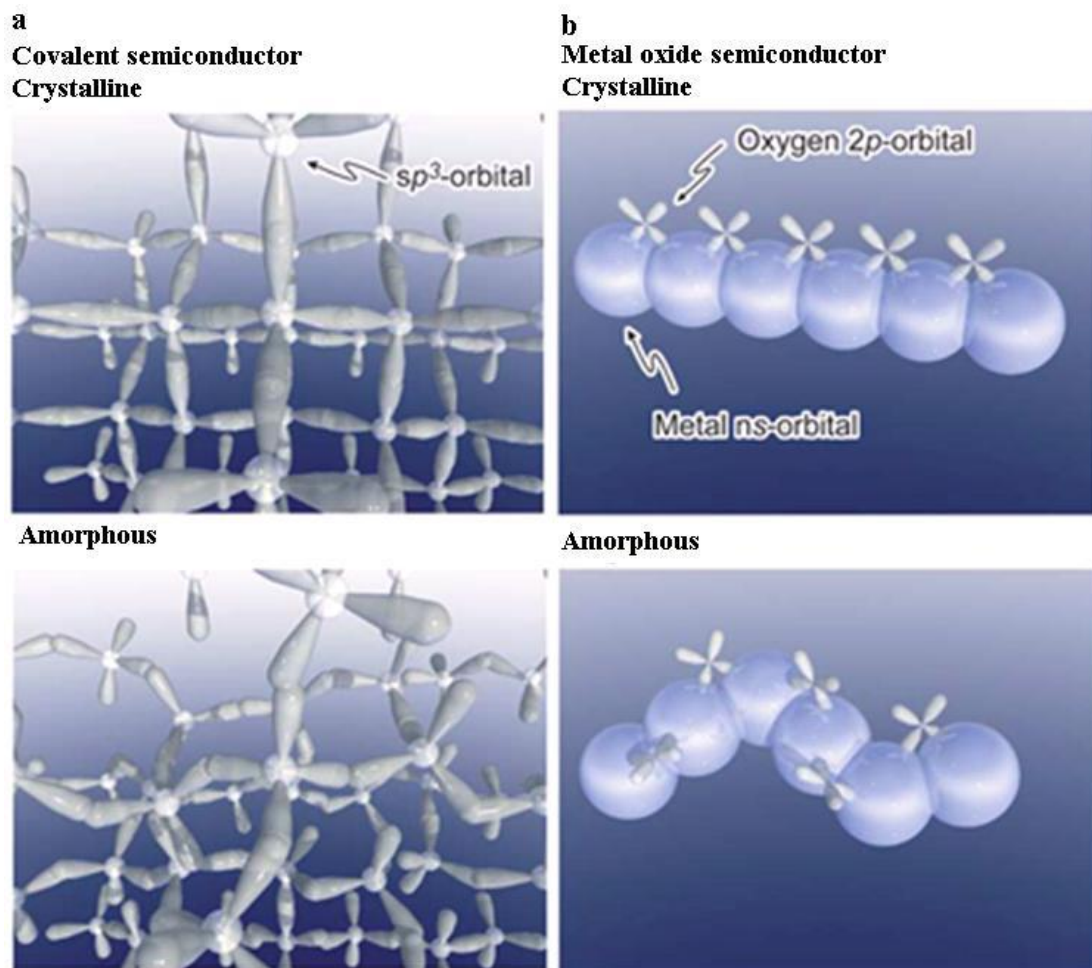
Figure 1.4   Schematic orbital drawing of electron pathway in (a) covalent semiconductors and (b) metal oxide semiconductors, respectively.

1.3   N-type Material of ZIZO

Metal-oxide materials have a wide semiconductor band gap (>3eV). The intrinsic property of the metal-oxide materials seems to behave as an insulator. Most metal-oxide materials are n-type materials. When metal-oxide TFTs were fabricated, the oxygen atoms in the material were decreased so that the oxygen vacancies were induced. Therefore, the original metals bonded oxygen atoms would produce free electrons. One oxygen vacancy will generate two free electrons.

In this study, we presented a solution-processed ZrInZnO (ZIZO) semiconductor, which is used as the active layer of the TFTs. The process involves the blending of $ZrOCl_2 \cdot 8H_2O$, $In(NO_3)_3 \cdot xH_2O$, and $Zn(CH_3COO)_2 \cdot 2H_2O$ in 2-methoxyethanol. The role of Zr atoms in the ZIZO system is to control the amount of oxygen vacancies. The number of oxygen vacancies decrease with increasing the Zr content. Moreover, the ZIZO TFTs exhibits long-term stability under bias stress conditions. The device performance is almost comparable with that of the device made by conventional cosputtering methods [15].

1.4   Motivation

Nowadays, there have been many reports of high performance TFTs with oxide semiconductors, including ZnO [16-18], InZnO (IZO) [19-21], InGaZnO (IGZO) [22-26] as the channel materials. The electrical characteristics have been significantly improved since Hosono and coworkers reported the usage of amorphous IGZO as a channel material using physical-vapor-deposition techniques [27]. Furthermore, the formation of solution-processed oxide semiconductor has also been investigated. The solution process has a lot of advantages such as low-cost, fast processing, and simplicity.

Sol-gel processing is widely used because of its relative simplicity and potential application in printed device fabrication. In the sol-gel process, the conductivity of multicomponent oxide films can be controlled by incorporating charge-controlling cations. These cations can control the amount of oxygen vacancies that supply free electrons in the multicomponent oxide thin films because of their high oxygen affinity [28, 29].

However, the large amount of gallium in the IGZO system has disadvantages due to its toxicity and high cost. Some groups suggested using different oxide materials, such as Sc [30] and La [31] carrier suppressors. We investigated the carrier suppressor effect by incorporating Zr into the sol-gel based InZnO system. The high stability is attributed to the lower electron negativity of Zr (1.4) than oxygen (3.4).

1.5   Thesis Organization

This thesis is organized as followings. In this chapter, the background of this study is described briefly; in the following chapter, we have introduced the basic knowledge of field-effect transistors. The useful methods of analysis are also presented in this part. The experimental details are shown in the third chapter and the procedures of the fabrication of TFTs, including surface treatments and thin-film spin-coating are illustrated. Apart from the device fabrication, the analysis methods are also particularly taken into account. In chapter 4, there are discussions for devices with the different ratio and the pre-annealing temperature. Further, the surface states of the active layer thin film was investigated by using atomic force microscopy (AFM), X-ray diffraction (XRD) measurement, UV/Visible measurement and X-ray photoelectron spectroscopy (XPS) techniques. Finally, conclusions are remarked in the last chapter.

Chapter 2

Review and Principle

2.1　Structures of Thin Film Transistors

According to the different position of source and drain, OTFTs can be classified to two common device structures: top-contact which also is called the inverted staggered type [Figure 2.1 (a)].and bottom-contact which is also called the inverted coplanar type TFTs [Figure 2.1 (b)].
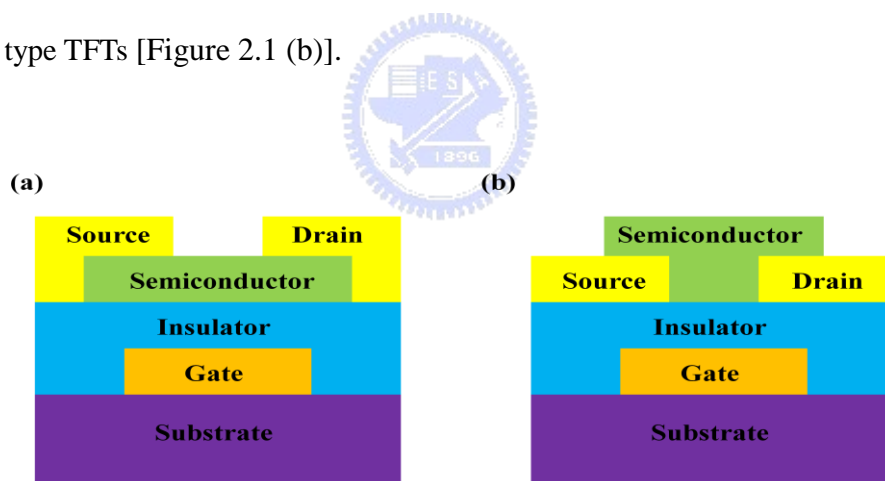
Figure 2.1　　　The basic TFT structure (a) Top contact (b) Bottom contact.

2.2 The Operation of Thin Film Transistors

The TFTs can be divided into two parts: n-type and p-type channel, according to the type of transported charges in the semiconductor. The majority carriers are electrons in the n-type channel. On the other hand, the majority carriers are holes in p-type channel. The TFTs can also be classified into two parts: the depletion-mode and the enhancement-mode, based on whether drain current flows through TFTs when no voltage is applied to gate electrode. For the enhancement-mode TFTs, only leakage current flows through the TFTs without applying the gate voltage and the device is off. For the depletion-mode TFTs, the drain current flows through the TFTs without applying the gate voltage and the device is on. If trying to turn off the depletion-mode TFTs with n-type channel, the gate electrode will be biased negatively with respect to the grounded source electrode.

The energy band diagrams and the schematics of TFTs operation in an n-type accumulation mode as shown in Figs. 2-2 and 2-3 are introduced to explain the three operation modes of TFTs. When no gate voltage is applied, the semiconductor is in an equilibrium state. After a negative bias is applied on the gate electrode, the delocalized electrons in the channel are repelled from the semiconductor/gate insulator interface. The effect creates a depletion region of positive charge, as indicated by the positive curvature in the conduction band and the valance band near the insulator as shown in Fig. 2-2 (b). This result conducts the depletion region of carriers as shown in Fig. 2-3 (b). The higher bias on the gate electrode, the larger depletion the region expands. Finally, all of the semiconductor layer will be depleted. When a positive gate bias is applied, delocalized electrons in the channel are attracted to the semiconductor/gate insulator interface, and creating electron accumulation at the interface. The outcome can be indicated by the negative curvature in the

conduction band and valance band near the insulator as shown in Fig. 2-2 (c). Then, the accumulation region is formed as shown in Fig. 2-3 (c). These accumulated electrons at the semiconductor/insulator interface provide a current conduction path and form the channel.
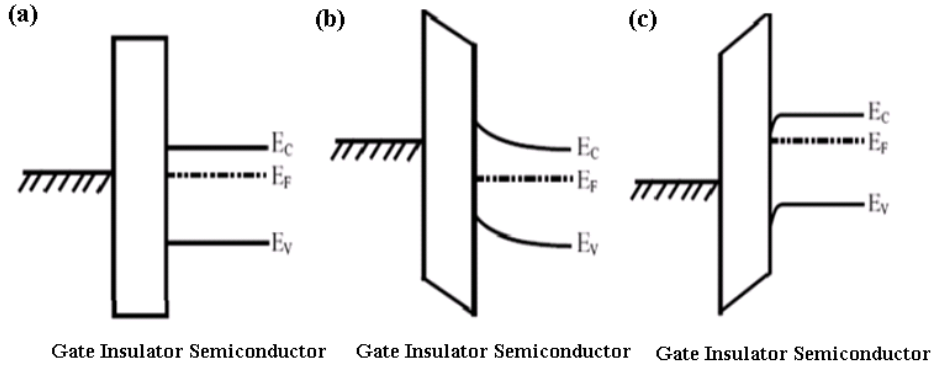
Figure 2.2   The semiconductor energy band diagram when (a) unbiased, (b) negative gate voltage bias, and (c) positive gate voltage bias, respectively.
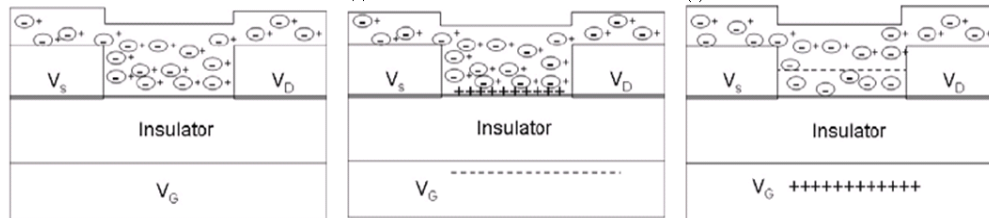
Figure 2-3   Schematic of TFTs operation in accumulation mode: (a) unbiased, (b) negative gate voltage bias, and (c) positive gate voltage bias, respectively.

The quantities of charges accumulated in the active layer are proportional to the gate bias and the capacitance of the insulator. In fact, the deep traps have to be filled firstly at interfacial states, and then induce extra mobile charges. In other words, the V_{GS} have to be biased higher than the threshold voltage (V_{Th}). So V_{GS}-V_{Th} is the effective driving voltage to accumulate more mobile charge carriers. The interfacial potential can be created an internal voltage at the semiconductor interface upon the insulator at zero gate bias and thus cause accumulation of additional charges (mobile or immobile) in the channel so that a obvious turn-on voltage shift is exhibited in the transfer characteristics [32,33].
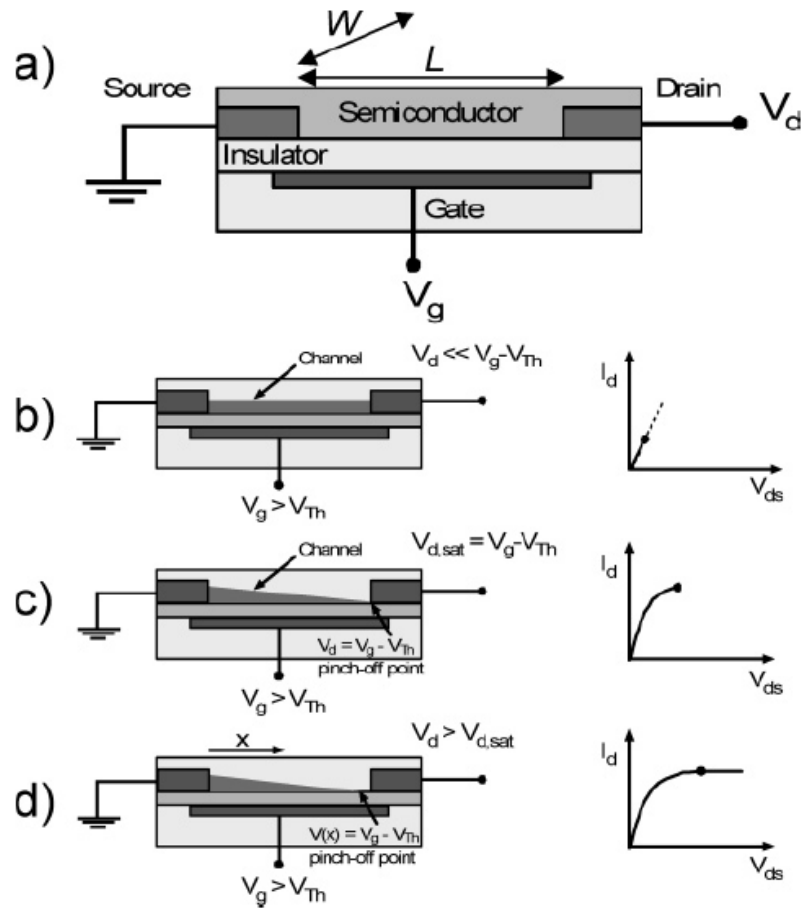
Figure 2.4   Carrier concentration diagram of TFT and associated current-voltage characteristics.

Figure 2.5 illustrates the basic operating modes and associated current-voltage characteristics. When drain-to-source voltage is zero, the charge carrier concentration in the transistor channel is uniform. Therefore, a linear slope of charge density can be observed when a small source-drain voltage is applied. In the linear regime, the quantities of charges flowed in the active layer are proportional to the gate bias. From the source [$V_{(X=0)}$ = 0 V] to the drain electrode [$V_{(X=L)}$ = V_{DS}], the potential $V(x)$ within the channel increases linearly. When V_{DS} = V_{GS} - V_{TH}, the channel becomes pinched- off. A depletion region is formed near the drain electrode because the voltage difference between the local potential $V(x)$ and the gate voltage is lower than the threshold voltage. Now only a space-charge-limited saturation current can flow across this region. Applying a higher drain-to-source voltage, it pushed the pinch point slightly toward the source. Eventually, in common situations, the channel length is much longer than the width of this depletion part, and the higher drain voltage would not lead to an additional drain current.

2.3 The Parameters Extraction of TFTs

There are two electrical characteristics curves. The one plot is I_D - V_D transfer characteristics as shown in Figure 2.6. The I_D versus V_D relation is measured under the constant V_G and sweeping V_D. There are two modes which are the linear and saturation modes in the I_D - V_D curves. The TFT is operated in the linear mode when the drain voltage is smaller than the voltage V_G - V_{Th}, and the transistor behaves like a resistance. When the drain voltage is applied larger than V_G - V_{Th}, the TFT is operated in saturation mode. In saturation mode, the drain current is controlled by the gate bias. The other plot is I_D - V_G transfer characteristics [34,35] as shown in Figure 2.7. From the I_D − V_G curve, we can extract several parameters like the mobility, threshold

voltage, subthreshold swing, and on-off ratio. Although the transportation mechanism is different between the organic materials and inorganic materials, the transfer characteristics are similar. Now we introduce a formula as the following section:

First, from Ohm's law, we know

$$\frac{I_D}{tW} = \sigma \frac{V_D}{L} \qquad (2\text{-}1)$$

, where σ is the conductivity, W is the channel width, L is the channel length , and t is the thickness of charged layer in the channel.

$$I_{d,lin} = \frac{W\mu C_i}{L}(V_g - V_{Th} - \frac{V_d}{2})V_d \qquad\qquad I_{d,Sat} = \frac{W\mu C_i}{2L}(V_g - V_{Th})^2$$

Linear region   **Saturation region**

$V_g = -50\ V$

$V_g = -40\ V$

$V_g = -30\ V$

$V_g > V_{Th}$

$V_g < V_{Th}$

$I_d\ [\mu A]$

$V_d\ [V]$

-100, -80, -60, -40, -20, 0

0, -10, -20, -30, -40, -50
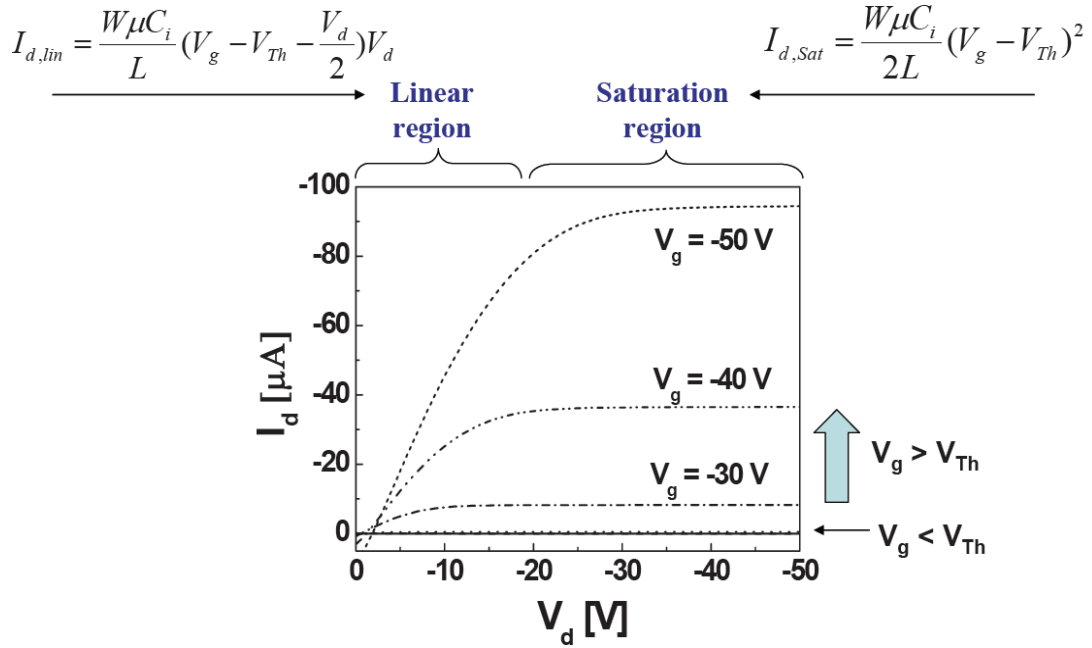
Figure 2.5   The I_D-V_D transfer characteristics of a n-type TFT.
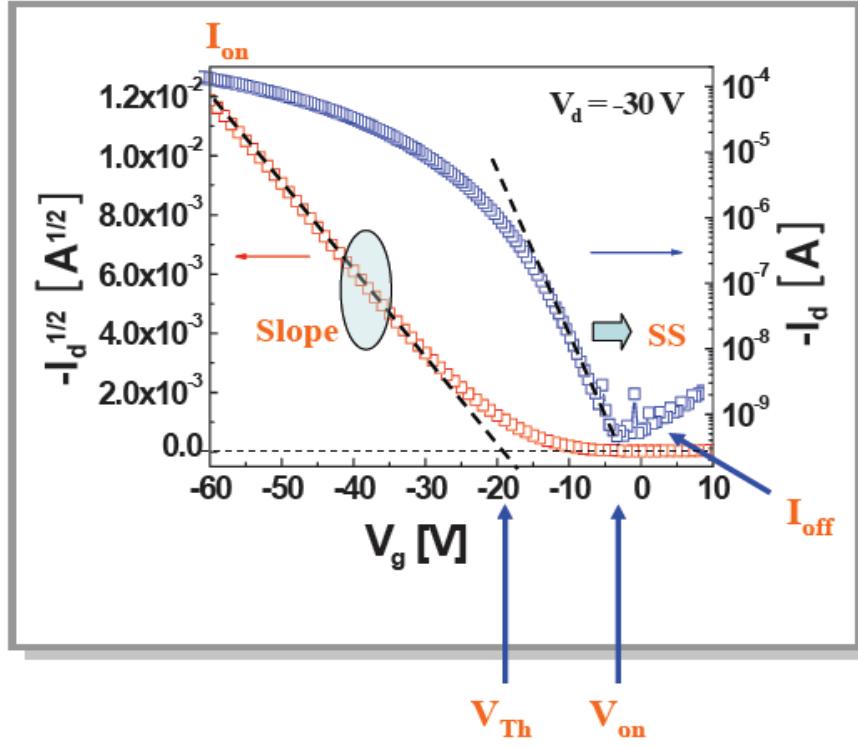
Figure 2.6   The I_D-V_G transfer characteristics of a p-typeTFT.

The equation 2-1can be rewritten as:

$$I_D = \frac{W}{L}(n_{ind}et)\mu V_D \qquad (2\text{-}2)$$

, where n_{ind} is the number density of induced charges in the channel and μ is the carrier mobility.

We assume the average value of induced charges is

$$n_{ind} = C_i\left(V_G - V_{Th} - \frac{V_D}{2}\right) \qquad (2\text{-}3)$$

Then we can substitute equation 2-3 into equation 2-2, and obtain:

$$I_D = \frac{W}{L}C_i\mu\left[(V_G - V_{Th})V_D - \frac{1}{2}V_D{}^2\right] \qquad (2\text{-}4)$$

The equation 2-4 is the typical linear regime equation.

When $V_D > V_G - V_{Th}$, the TFT is operated in a saturation regime and the equation 2-4 will be become:

$$I_D = \frac{W}{2L} C_i \mu_{sat} (V_G - V_{Th})^2 \qquad (2\text{-}5)$$

, where μ_{sat} is the carrier mobility in the saturated region, and the μ_{sat} is usually higher.

The mobility μ can be calculated by differentiating the square root of I_D in saturation mode as:

$$\frac{\partial\sqrt{|I_D|}}{\partial V_G} = \sqrt{\frac{WC_i\mu}{2L}} \qquad (2\text{-}6)$$

In the figure 2.7, the slop and threshold voltage can be measured from the $I_D^{0.5}$ – V_G curves.

The subthreshold swing (S.S.) is a parameter to determine the switch speed of a transistor. It can be calculated by the following equation 2-7.

$$S.S = \frac{\partial V_G}{\partial \log|I_D|} \qquad (2\text{-}7)$$

The dimension of subthreshold swing is V/decade. The subthreshold swing gives the degree of the switch property of a transistor.

Chapter 3

Experimental and Analysis Methods

3.1   Preface

The top-contact structure was chosen to fabricate the TFTs in this study The structure of the top-contact TFT is shown in Figure 2.1a.

3.1.1   Preparation of Substrates

We use heavily doped n-type silicon wafers with thermal SiO_2 to fabricate the devices. The top SiO_2 layer was 200 nm thick, and the sheet resistance was about 0.001~0.003 ohm-cm. The capacitance per unit area in the SiO_2 layer was 14.2 nF/cm^2. The conductance of the wafers is high enough to serve as the gate electrode.

3.1.2   Cleaning of the Si/SiO$_2$ Substrate

Step 1: The substrate has washed the substrates with detergent, acetone (ACE), and isopropyl alcohol (IPA).Then they are rinsed by deionized water for 5 minutes. The detergent can take away the large particles and oil sludge.

Step 2: Put the substrates into a Teflon container and soak the substrates in DI water into an ultrasonic cleaner for 20 minutes. Then rinse the substrates by DI water for 5 minutes.

Step 3: Put the substrates into a Teflon container and soak the substrates in ACE into an ultrasonic cleaner for 20 minutes. Organic pollutants would be swept away in this step. Then rinse it again by DI water in 5 minutes.

Step 4: Put the substrates into a Teflon container and soak the substrates in IPA into an ultrasonic cleaner for 20 minutes. The residual acetone and water molecules would be taken away by IPA. Then rinse it repeatedly by DI water in 5 minutes.

Step 5 : Dry the substrates by nitrogen shower, and then these substrates were placed into an oven in 120℃ for exceed 24 hours to remove the water.

3.2   The Material

Zirconium indium zinc oxide (ZrIZO) [Figure 3.1(a)] was used as the active layer of the TFTs. It was fabricated from zirconium dichloride oxide octahydrate [$ZrOCl_2 \cdot 8H_2O$] [Figure 3.1(b)], indium nitrate pentahydrate [$In(NO_3)_3 \cdot xH_2O$] [Figure 3.1(c)], and zinc acetate dehydrate [$Zn(CH_3COO)_2 \cdot 2H_2O$] [Figure 3.1(d)] in 2-methoxyethanol [Figure 3.1(e)]. Monoethanolamine [Figure 3.1(f)] was also added because adding Monoethanolamine in the same concentration with zinc acetate dehydrate could make the solution more stable.
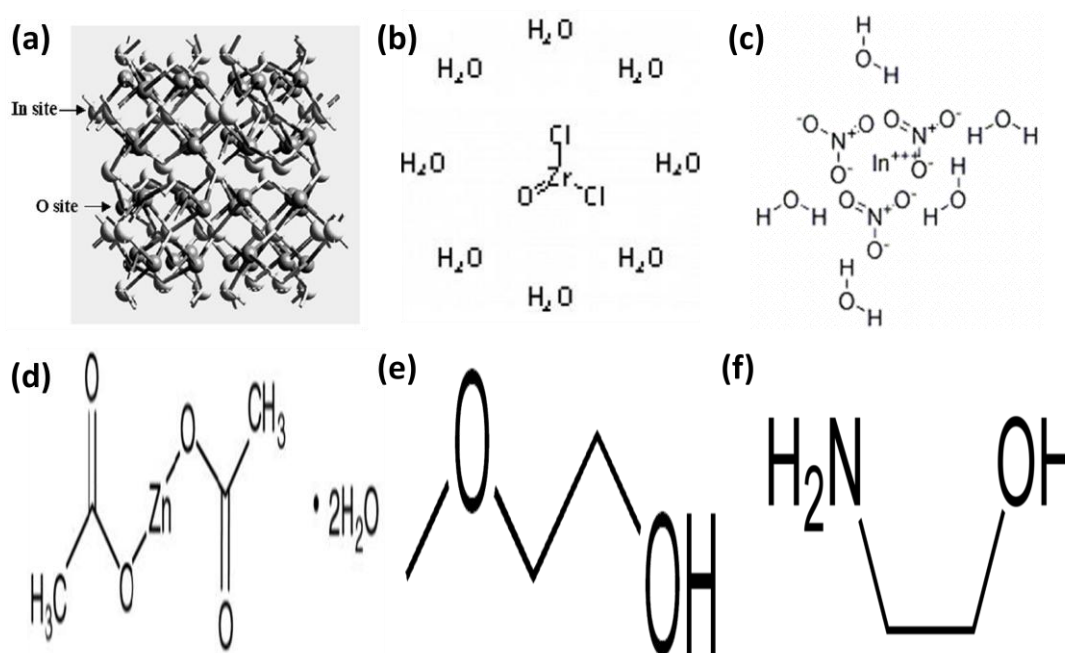
Figure 3.1   The structure of materials used in this experiment.

[(a) was adapted from Jin-Seong Park Lab [36]]

[(b) was adapted from http://www.jhyb.com.cn/goods-1680.html]

[(c) was adapted from

http://www.chemicalbook.com/ChemicalProductProperty_CN_CB2619716.htm]

[(d) was adapted from http://dailymed.nlm.nih.gov/dailymed/drugInfo.cfm?id=1081]

[(e) was adapted from http://en.wikipedia.org/wiki/File:2-Methoxyethanol.png]

[(f) was adapted from

http://en.wikipedia.org/wiki/File:Ethanolamine-2D-skeletal-B.png]

3.3 Device Fabrication Processes

3.3.1 Spin-Coating of the ZrIZO as the Active Layer

The total concentration of the metal precursors was 0.25M. Before spin-coating of the film, the ZrIZO solution was heated at 60℃ for 1 hour and then aged for more than 24 hours.

The substrates were subject to UV-Ozone treatment for 20 minutes. The ozone molecules would burn the organic contaminant on substrates, and the particles were taken away by an air flow.

The spin rate was set to 1500 r.p.m for 1 minute. The cleaned SiO2 substrates were covered with an active layer of 40 nm thick, which was prepared by spin coating of the solution of ZrIZO. After spinning, the ZrIZO films were soft baked at 300℃ for 15 minutes.

3.3.2 Evaporation of Metal Electrodes

Before the deposition of source and drain electrodes, the device was pre-annealed in air at 500℃ for 2 hours. Finally, aluminum 50nm was deposited as the source and drain electrodes by thermal evaporation under a pressure less than 5×10^{-6} torr through a shadow mask. The channel was 200 μm wide and 120 μm long.

1. Add ZrOCl$_2$ · 8H$_2$O, In(NO$_3$)$_3$ · xH$_2$O, Zn(CH$_3$COO)$_2$ · 2H$_2$O, 2-methoxyethanol, Monoethanolamine
2. Baked 60℃ for 1h and aged for more than 24 h.

1. RCA clean
2. UV-Ozone 20 minutes

1. 40-nm ZrIZO was spin-coated
2. Baked at 300 ℃ for 15 minutes and annealed at 500℃ for 2 hours.

1. 50 nm Al was evaporated on top of the semiconductor layer through the shadow mask
2. Place the device in the air.
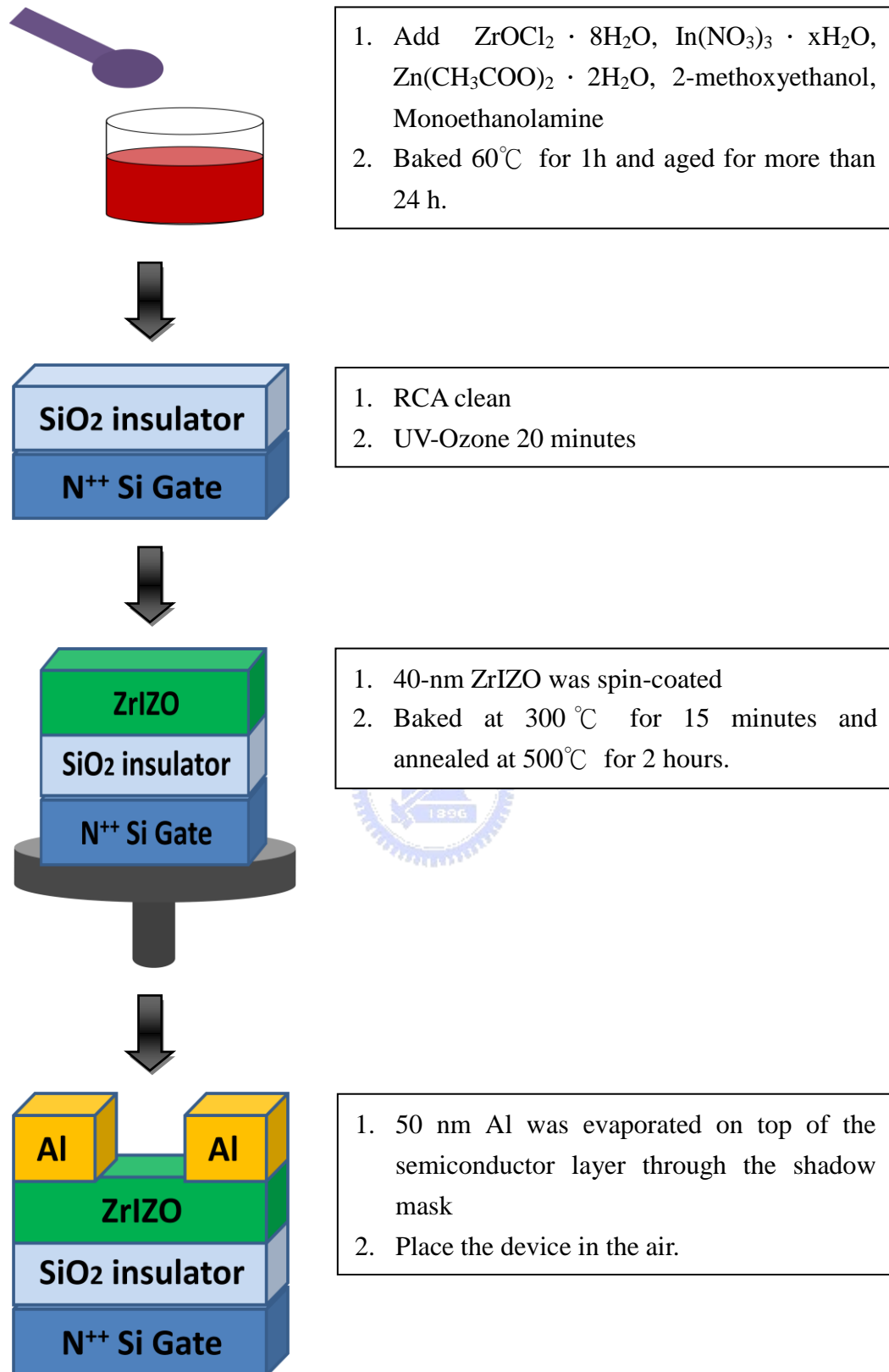
Figure 3.2   The flow chart of the device fabrication process.

3.4 Measurements and Analysis of TFTs

3.4.1 Electrical Characteristics

We measured the electrical properties of the devices by Keithley 4200 IV measurement system at room temperature. For ZrIZO devices, we applied a positive gate voltage to accumulate electrons in the channel near the semiconductor/insulator interface. In the I_D-V_D measurement, we swept the gate bias from 0 to 60Volts, and the gate voltage step was 15 V from $V_G = 0$ V to $V_G = 60$ V. Besides, in the I_D-V_G measurement, the drain bias swept from 10 to 30V, and the drain voltage step was 10 V from $V_G = 10$ V to $V_G = 30$ V.

3.4.2   Measurement of Surface Morphology

In this study, we used the atomic force microscope (AFM) to measure the surface morphology of the materials. By the interaction of the van der Waals force between the tip of the cantilever and the surface topology of the sample, the cantilever vibrates at different frequencies depending on the magnitude of the interaction. Detecting a laser beam reflected by the cantilever can sense the tiny vibration of the cantilever, the computer record these detected signals and re-construct the surface morphology of samples. The interaction force between the two atoms where one is on the tip of the cantilever and the other is on the surface of sample depends on their distance as show in Figure 3.3. Similarly, Figure3.4 illustrates the configuration of AFM. From the surface morphology, we can find the relationship between the transfer characteristic and the graining formation of the organic semiconductor.
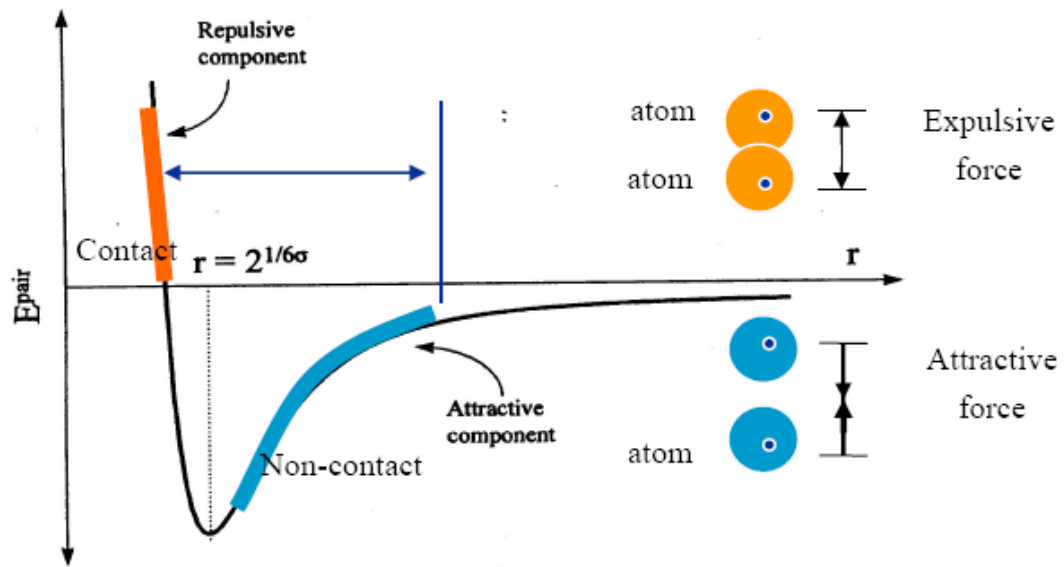
Figure 3.3   The interaction force between two atoms.
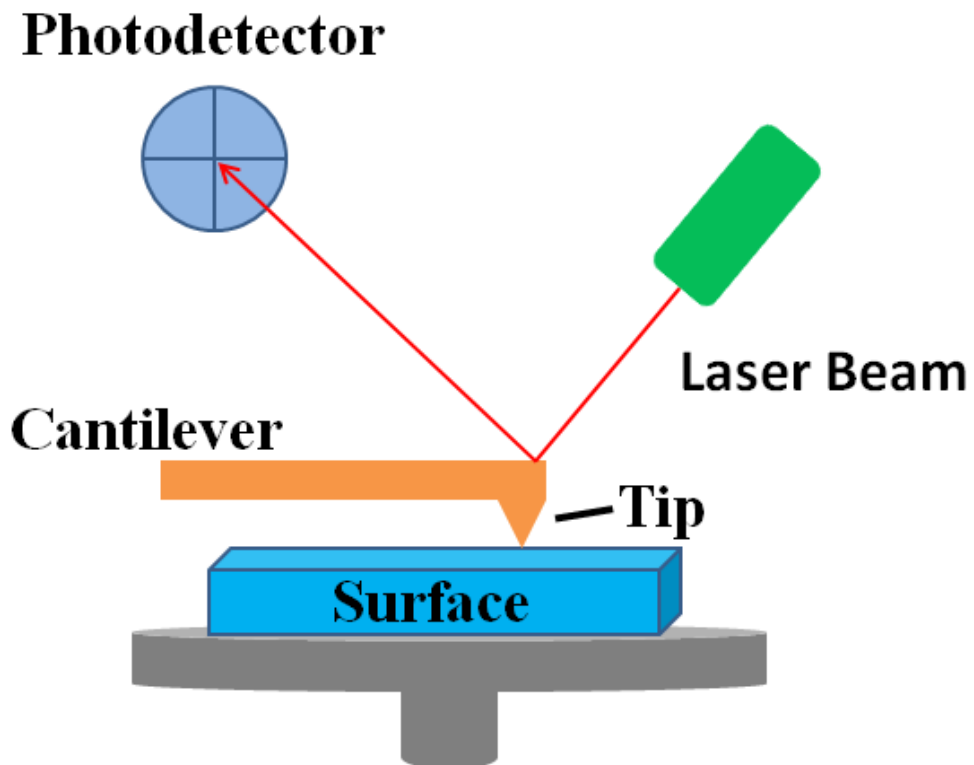
Figure 3.4   The operation of atomic force microscope.

3.4.3 X-ray Photoelectron Spectroscopy Measurement

X-ray photoelectron spectroscopy (XPS) is a widely used technique that can measure the elemental composition, the chemical state and the electron state of the elements that exist in materials. It suits to study core-level electron spectroscopy because of its high energy and short wavelength. Figure 3.5 shows the configuration of XPS. The energy (hv) of the x-ray was incident into the sample, and the core-level electron of an atom possesses exceed energy is excited. The electron possesses the kinetic energy E_k. E_k and hv are related by the following equation: $E_k = hv - E_{b-\varphi}$, φ is the energy of the material work function and E_b is the binding energy of an atom. This kind of electron is called photoelectron. In other words, by measuring the energy of the photoelectrons, we can plot photoelectron intensity versus the electron energy. From the chart, we can get the information of the material.
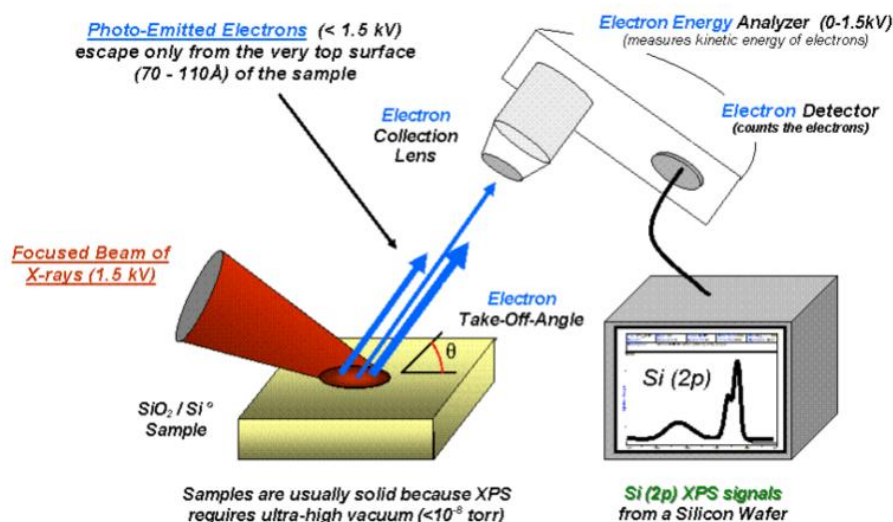
Figure 3.5 The operation of x-ray photoelectron spectroscopy.

[Adapted from http://en.wikipedia.org/wiki/X-ray_photoelectron_spectroscopy]

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3.4.4　X-ray Diffraction Measurement

High-resolution x-ray diffraction is used to characterize the thickness, and the crystallographic structure in thin epitaxial films. When x-ray is incident on the material of a regular structure, the crystalline solids reflect x-ray and produce Bragg's diffraction. The interference is constructive when the phase shift is a multiple of 2π. The relation can be indicated by the following formula: $n\lambda = 2d\sin\theta$, where n is an integer, λ is the wavelength of incident wave, d is the spacing between the planes in the atomic lattice, and θ is the angle between the incident ray and the scattering planes. These crystals, at certain specific wavelengths and incident angles, produce intense peaks of reflected radiation. In other words, we can use this information, including incident angle, peak position and intensity to construct the crystal structure.
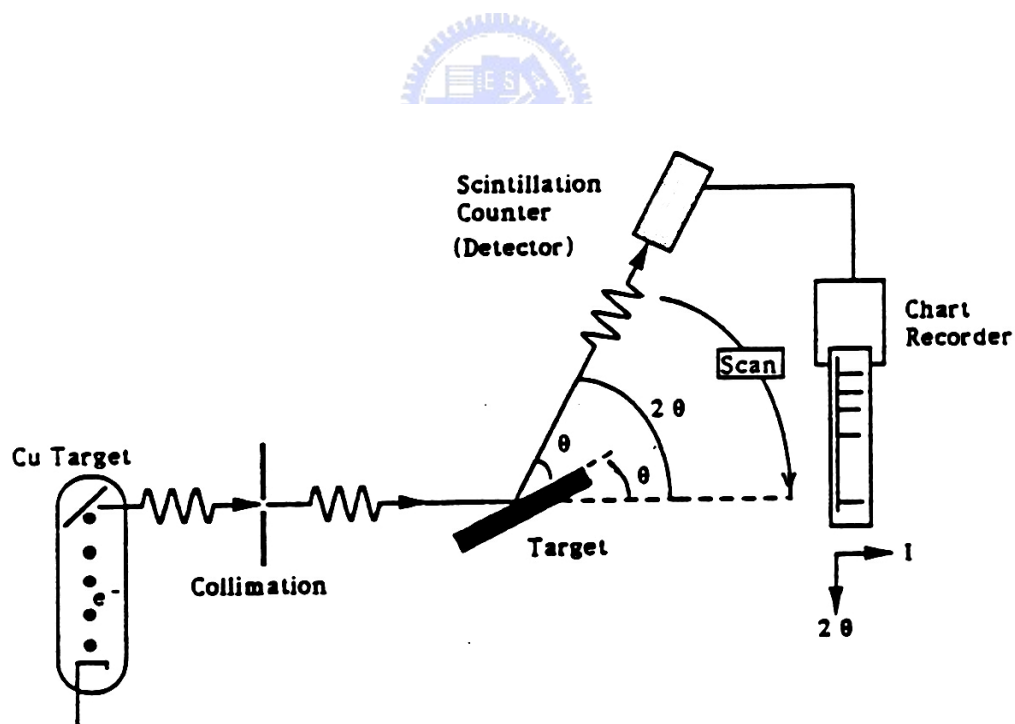
Figure 3.6　　The operation of X-ray diffraction spectroscopy.

3.4.5 UV/Visible Spectroscopy Measurement

The UV/Visible absorption of films was measured on Perkin Elmer Lambda 650. The light sources of the UV/Visible spectroscopy are provided by D_2 and W. The UV wave band is provided by D_2, and the visible light wave band by W. The absorption, A, is defined as $A = \log(I_0/I)$, where I_0 is the intensity of the incident light and I is the intensity of the transmitted light.

Chapter 4

Results and Discussion

4.1   The Effect of the Zr content

The mole ratio of Zr was varied from 0 to 1 while the In: Zn mole ratio was fixed at 5:5. (i.e., the mole ratio of ZIZO were Zr: In: Zn =0: 5: 5, 0.1: 5: 5, 0.2: 5: 5, 0.5: 5: 5, and 1: 5: 5) The variation in transfer and output characteristics of the solution-processed ZIZO TFTs with the Zr molar ratio after 8th day was described in Figure 4.1 and Table 4.1. The device exhibited typical n-channel behavior operation in the enhancement mode. As the Zr content increased, both on and off current decreased. This phenomenon was attributed to the fact that Zr acted as a carrier suppressor, like Ga and Hf. In fact, the numbers of electron carriers were reduced due to the decreased number of oxygen vacancies. We considered that this suppressing ability should be attributed to its high electron negativity (EN = 1.4). This suppressing ability is stronger than that of Ga, whose EN is equal to 1.7. And a large on-off current ratio was observed ($>10^7$). Because subthreshold swing (SS) is related to the bulk and interfacial trap states (N_t) in the TFTs, the total interfacial trap state can be calculated from the following equation:

$$N_t = \left[\frac{SS \log(e)}{\frac{kT}{q}} - 1 \right] \frac{C_i}{q} \tag{4-1}$$

, where C_i is the capacitance per unit area of the dielectric, k is the Boltzman constant, T is temperature, and q is unit charge. From equation (4-1), we can see that when the Zr content increased from 0 to 0.1, N_t decreased from 1.28×10^{13} to 5.72×10^{11}.
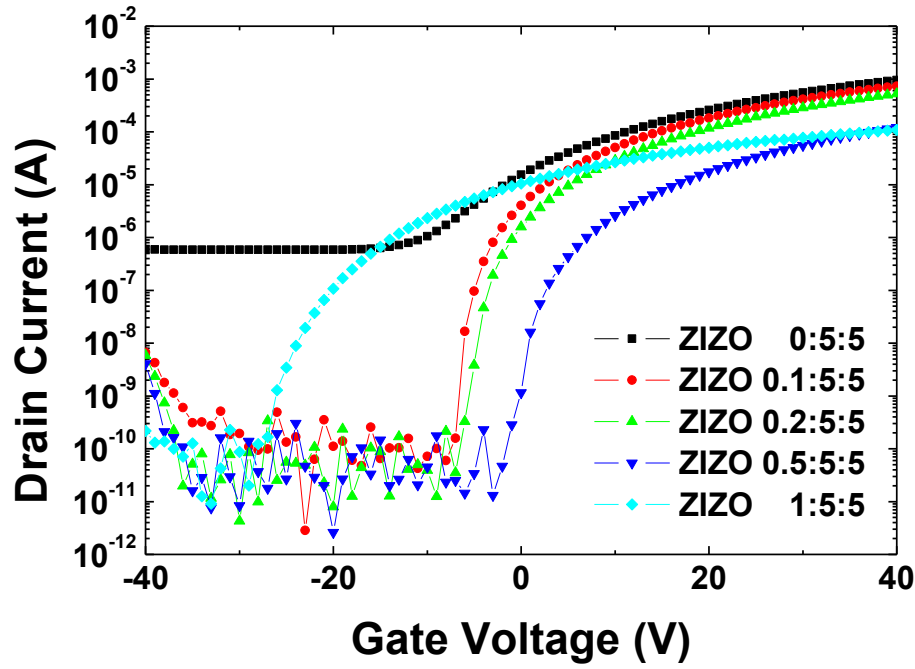
Figure 4.1 The I_D-V_G transfer characteristics of the ZIZO TFTs at $V_D = 60$ V prepared with various Zr compositions (L = 120μm and W = 200μm).

Table 4.1 Comparison of the electrical characteristics for the solution-processed ZIZO TFTs with various Zr ratio.

Zr:In:Zn mole ratio	μ (cm^2/Vs)	$I_{on\text{-}off}$	V_{Th} (V)	SS (V/dec)	N_t (cm^{-2})
0:5:5	4.55	1.63×10^3	-1.13	8.11	1.28×10^{13}
0.1:5:5	3.80	1.22×10^7	0.44	0.42	5.72×10^{11}
0.2:5:5	2.98	1.48×10^7	2.35	0.967	1.44×10^{12}
0.5:5:5	1.04	9.25×10^6	9.39	1.146	1.72×10^{12}
1:5:5	0.263	5.3×10^6	-18.34	1.277	2.01×10^{13}

From Table 4.1, the optimized condition of the ZIZO TFTs was Zr: In: Zn=0.1: 5: 5. As shown in Figure 4.2, the device exhibited a high saturation current which was higher than 10^{-3}A. The saturation field-effect mobility (μ_{FE}) and the on-off current ratio were estimated to be 3.8cm^2/Vs and ~10^7, respectively. The threshold voltage (V_{Th}) was 0.44 V. The subthreshold swing is 0.42 V/dec. Overall, the characteristics of the solution-processed ZIZO TFT are almost comparable with those of the device made by sputtering methods.
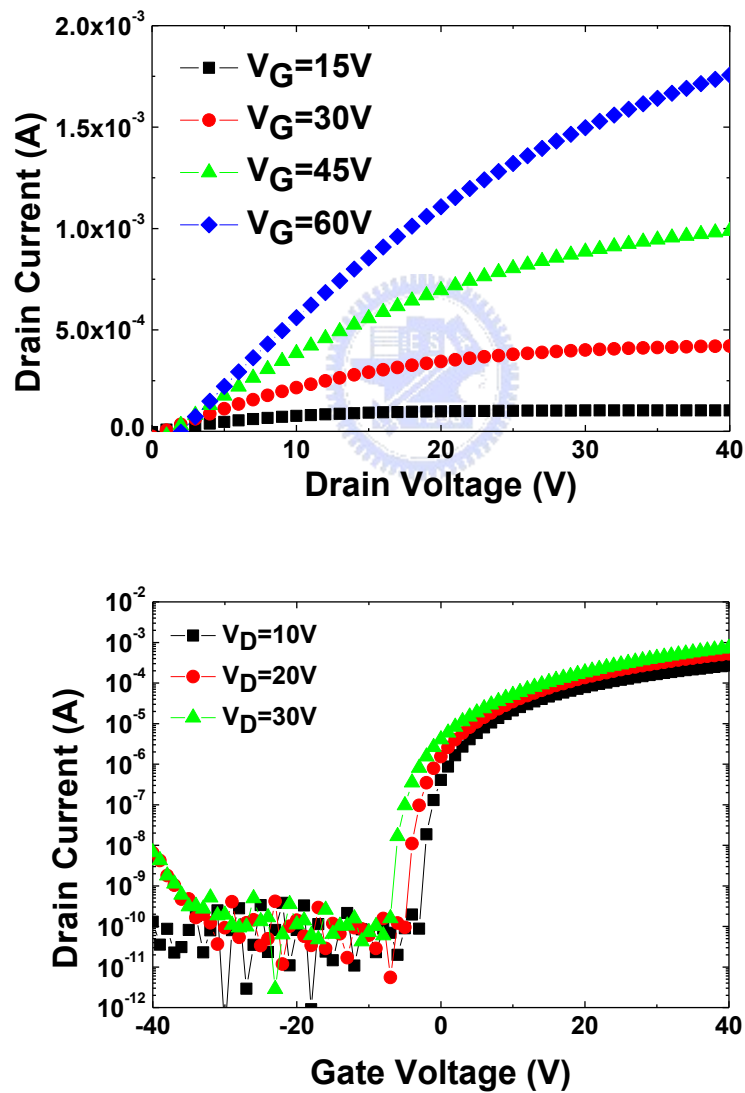
Figure 4.2 The $I_D - V_D$ and $I_D - V_G$ electrical performance of the ZIZO TFT with prepared the ratio of Zr : In : Zn = 0.1: 5: 5.

4.2 The Effect of Pre-annealing Temperature

The pre-annealing temperature was varied from 300℃ to 500℃. The variation in the transfer and output characteristics of the solution-processed ZIZO TFTs fabricated with various pre-annealing temperature is described in Figure 4.3 and Table 4.2. The device exhibited typical n-channel behavior in the enhancement mode. When the pre-annealing temperature increased, the electrical characteristics were obviously improved. When the pre-annealing temperature was higher than 400℃, the device should apparent field effect. On the contrary, when the pre-annealing temperature was below 400℃, the device only exhibited a very low current presumably due to the low crystallinity of the ZIZO thin film.
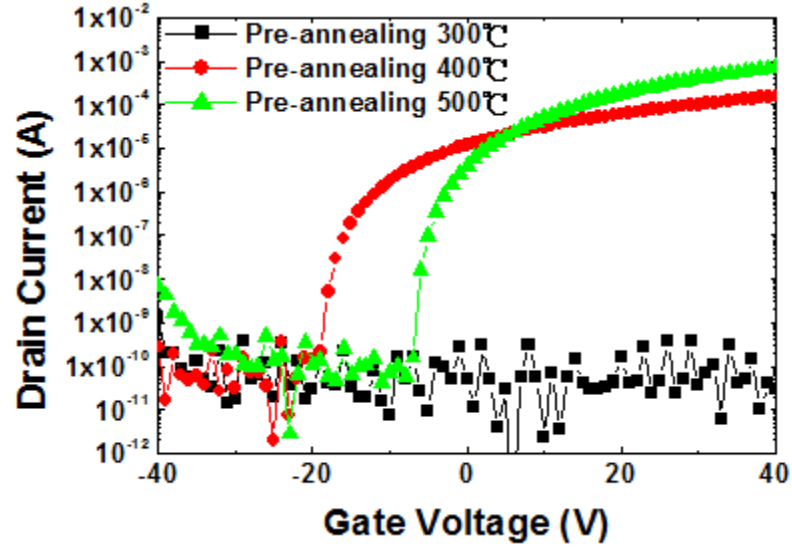
Figure 4.3   The transfer characteristics of the ZIZO TFT at $V_D = 60$ V prepared with various pre-annealing temperature (L = 120μm and W = 200μm).

Table 4.2   Comparison of the electrical characteristics for the solution-processed ZIZO TFTs fabricated with various pre-annealing temperature.

Pre-annealing Temperature	μ (cm^2/Vs)	$I_{on\text{-}off}$	V_{Th} (V)
300℃	…	…	…
400℃	0.59	3.03×10^6	-6.78
500℃	3.80	1.22×10^7	0.44

4.3 The Effect of the Adding NaOH

When the processes of solution-processed ZIZO TFT were finished, we observed from the transfer curve that the device had a high off current. We preserved the device in ambient environment in which the relativity humidity was about 60%. Figure 4.4 shows the electrical transfer performance of the device measured from the 1st day to the 15th day. We could observe that the off current remarkably decreased gradually. Similarly, we could see that the transfer performance became stable after the 8th day. We inferred that the chemical reaction had not been finished after the device was completed.

Figure 4.4 The I_D-V_G transfer characteristics of ZIZO TFT with the ratio of Zr: In: Zn = 0.5: 5: 5 at V_D = 60 V from 1st day to 15th day.

There were probably three stages during the formation of ZIZO semiconductor. According to order, the first stage was decomposition and hydrolysis. The second stage was dehydroxylation and alloying. The last stage was crystallization. In the second stage, after adding hydroxyl in the solution, such as NaOH, it could speed up the dehydroxylation reaction. Figure 4.5 and Table 4.3 showed the transfer characteristics and the parameters. After the addition of 0.03M NaOH, the electrical characteristics became stable in 9 days, suggesting that adding NaOH could accelerate the reaction effectively.
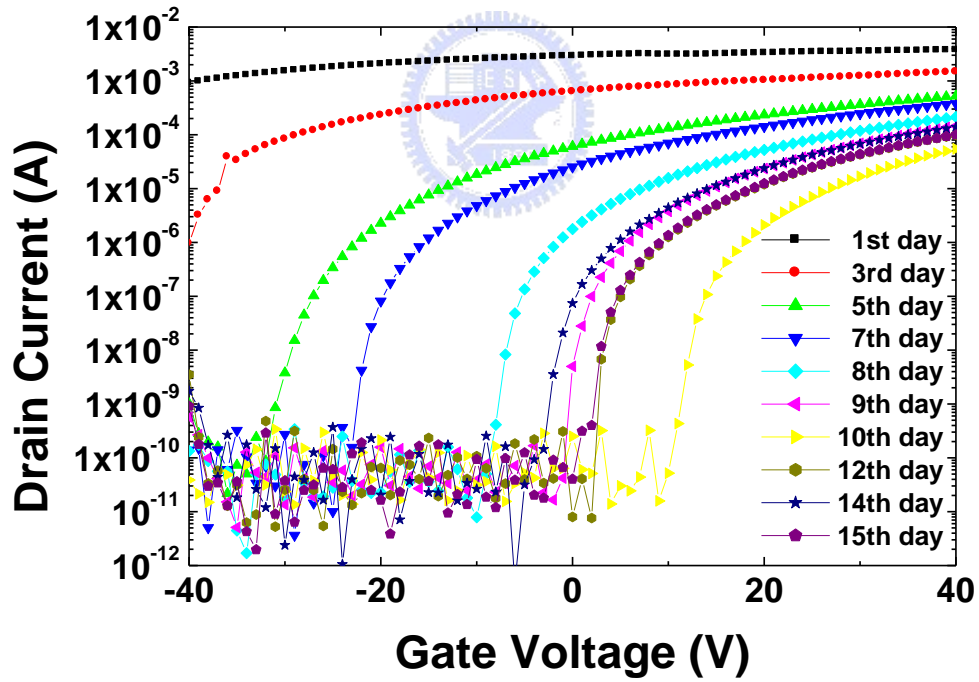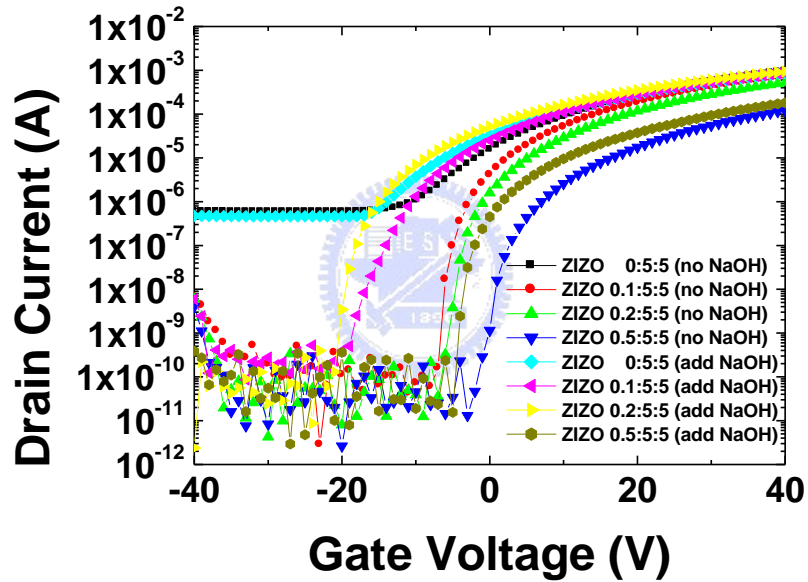

Figure 4.5   The I_D-V_G transfer characteristics of ZIZO TFT at V_D = 60 V with various pre-annealing temperature (L = 120μm and W = 200μm)

Table 4.3   Comparison of the electrical characteristics for solution-processed ZIZO TFT with different ratio with/without adding 0.03M NaOH.

	μ (cm^2/Vs)	I_{On-off}	V_{Th} (V)	Reaction day
0:5:5 (no NaOH)	4.55	1.63×10^3	-1.13	10th
0.1:5:5 (no NaOH)	3.80	1.22×10^7	0.44	10th
0.2:5:5 (no NaOH)	2.98	1.48×10^7	2.35	10th
0.5:5:5 (no NaOH)	1.04	9.25×10^6	9.39	10th
0:5:5 (add NaOH)	3.18	1.88×10^3	-6.87	1st
0.1:5:5 (add NaOH)	3.39	5.72×10^6	-5.69	1st
0.2:5:5 (add NaOH)	2.93	1.53×10^7	-10.99	1st
0.5:5:5 (add NaOH)	1.17	7.66×10^6	4.75	1st

4.4 The Bias Stress Measurement

The electrical output performance under the different bias stress was displayed in Figure 4.6. When a gate bias of 10 V was applied, we can see that the $\triangle V_{Th}$ became stable after 1×10^4 seconds. On the contrary, if a bias stress of 20V was applied, the threshold voltage shift continued to increase with time.
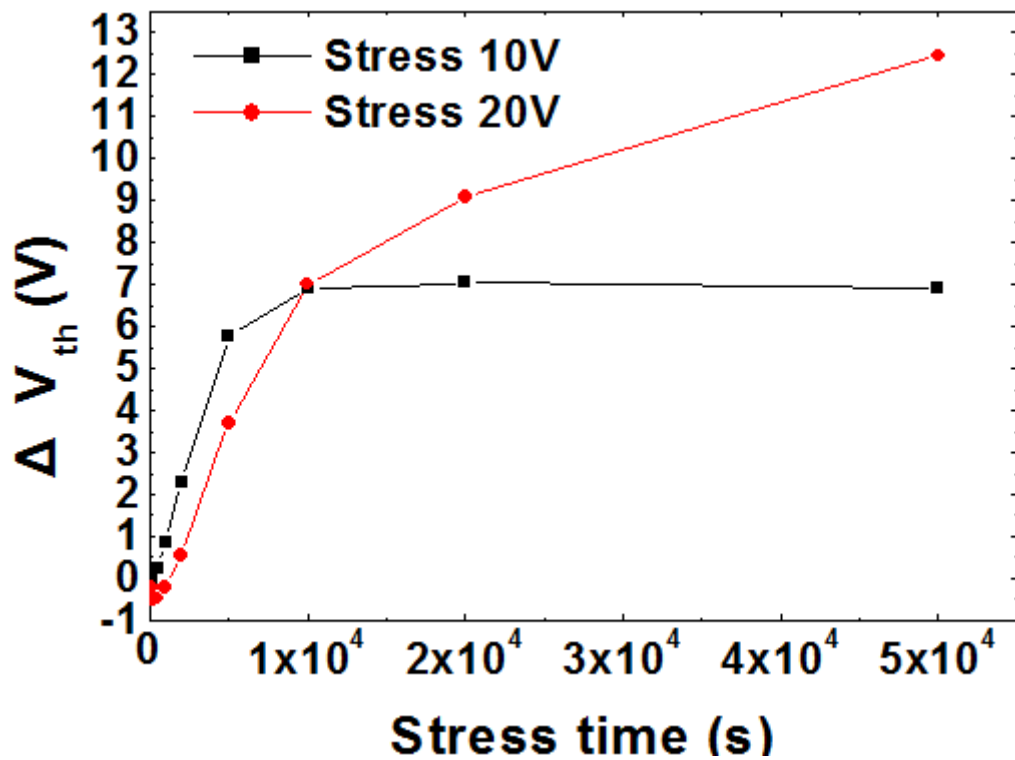
Figure 4.6   The variation of V_{Th} for the ZIZO TFTs as a function of stress time at different bias stress.

4.5　The Morphological Analysis of the Active Films

The height-mode and phase-mode images of the ZIZO films prepared with different Zr ratios were displayed in Figure 4.7. Figure 4.7(a), (c) and (e) showed the height mode images of the thin film prepared with the ratio of Zr: In: Zn = 0: 5: 5, Zr: In: Zn = 0.1: 5: 5 and Zr: In: Zn = 0.5: 5: 5, respectively, on the SiO_2 films. Similarly, Figure 4.7 (b), (d) and (f) showed the phase mode images of the thin films prepared with the ratio of Zr: In: Zn = 0: 5: 5, Zr: In: Zn = 0.1: 5: 5 and Zr: In: Zn = 0.5: 5: 5 deposited on the SiO_2 films. In the height-mode images, the films deposited with different ratios exhibit a smooth surface morphology. The surface roughnesses of the films prepared with the ratio of Zr: In: Zn = 0: 5: 5, Zr: In: Zn = 0.1: 5: 5 and Zr: In: Zn = 0.5: 5: 5 were 0.375nm, 0.396 nm and 0.325 nm, respectively. When the Zr content was increased in the film, the roughness still did not change significantly. However, in the phase mode images, we could observe many small grains on the surface. When the Zr content was increased, number of the grains was decreased gradually.

Figure 4.8 shows the height mode and phase mode images for the device annealed with different pre-annealing temperatures. When the pre-annealing temperature was increased, the roughness also increased. The roughness of the thin film prepared at 300℃, 400℃ and 500℃ was 0.233nm, 0.359nm and 0.396nm, respectively. When the pre-annealing temperature was increased, the grain size became larger, thereby improving the charge transport. Therefore, the device exhibited higher mobility.
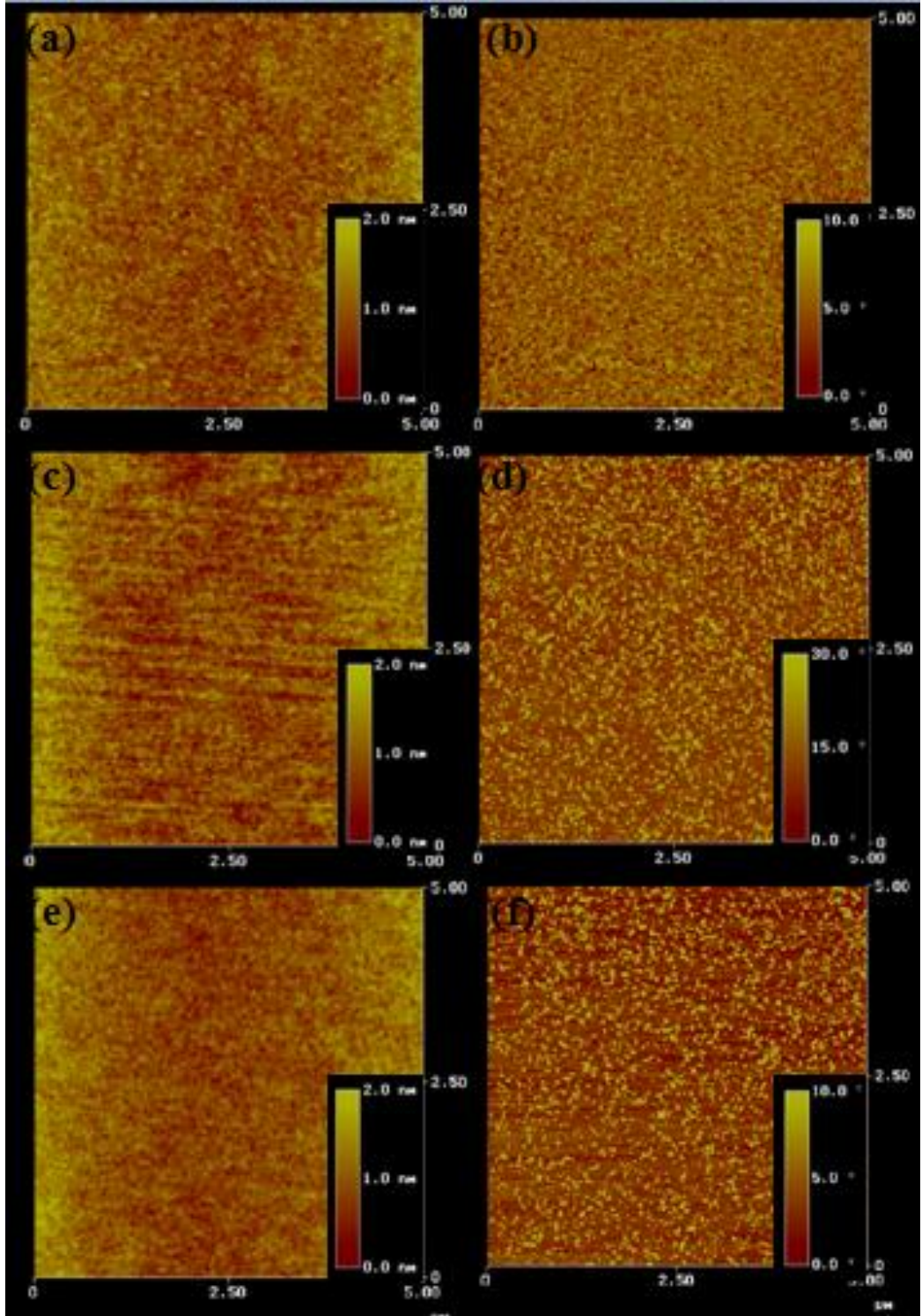
Figure 4.7 The height-mode and phase-mode images measured by AFM: (a) height mode (Zr: In : Zn = 0: 5 : 5) (b) phase mode (Zr : In : Zn = 0: 5 : 5) (c) height mode (Zr: In : Zn = 0.1 : 5 : 5) (d) phase mode (Zr : In : Zn = 0.1 : 5 : 5) (e) height mode (Zr: In : Zn = 0.5 : 5 : 5) (f) phase mode (Zr : In : Zn = 0.5 : 5 : 5)
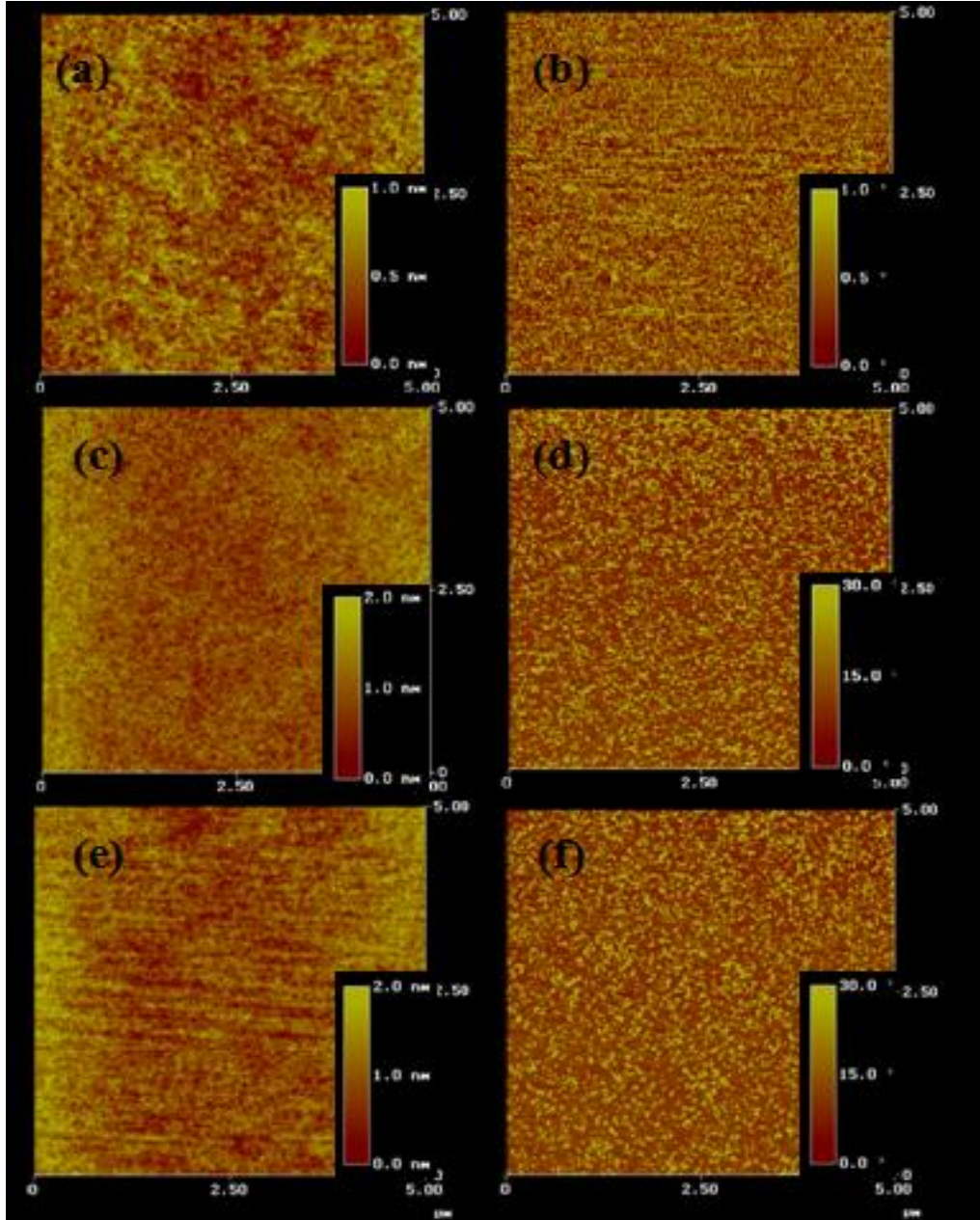
Figure 4.8 The height-mode and phase-mode images for the thin film prepared with the ratio of Zr: In : Zn = 0.1: 5 : 5 at various pre-annealing temperatures measured by AFM: (a) pre-annealing temperature: 300 ℃ (b) pre-annealing temperature: 300 ℃ (c) pre-annealing temperature: 400 ℃ (d) pre-annealing temperature: 400 ℃ (e) pre-annealing temperature: 500 ℃ (f) pre-annealing temperature: 500℃. (a)(c)(e) are height-mode images. (b)(d)(f) are phase mode images.

4.6 The Analysis of XRD Measurement

Figure 4.9 shows the x-ray diffraction (XRD) pattern of the ZIZO films deposited on SiO$_2$ surfaces. We could analysis the crystallization of the ZIZO thin films from the figure. Unfortunately, we found that no matter which conditions we used, the XRD patterns were all similar: all ZIZO films exhibited amorphous phase, suggesting that the addition of Zr atoms effectively inhibited the crystallization of InZnO.
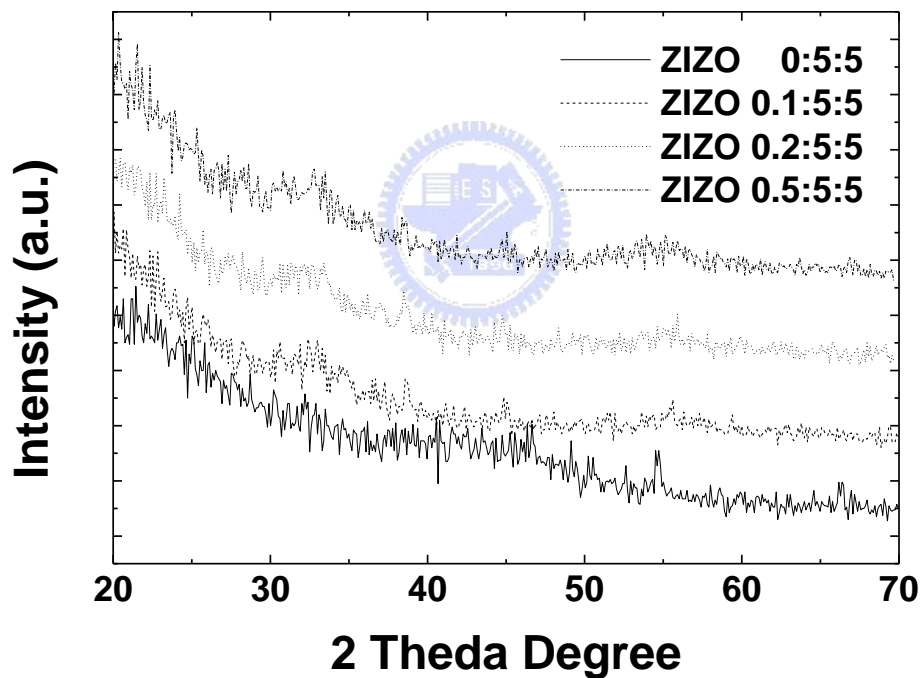
Figure 4.9   XRD patterns of the ZIZO films with different Zr contents. The devices were prepared with various conditions.

4.7 The Analysis of UV/Vis Spectroscopy Measurement

Figure 4.10 shows the transmittances of the ZIZO thin films deposited on the ITO glasses as a function of Zr content. The average transmittance of the ZIZO thin films was higher than 98% in the visible range. We also found that as the Zr content was increased, optical transmittance of the film was increased. The addition of Zr atoms probably increases of the band gap..
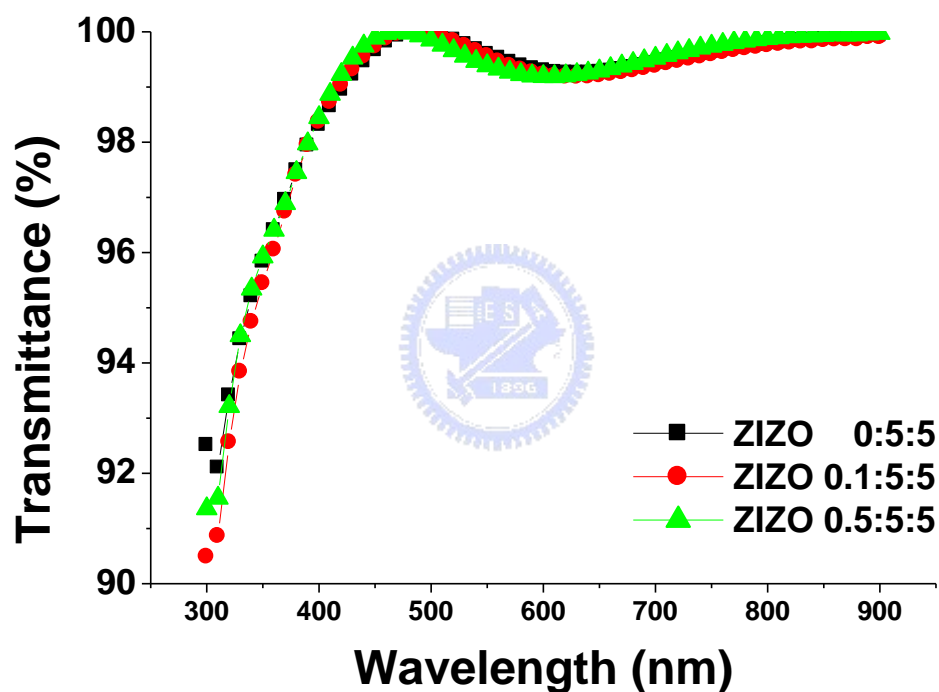
Figure 4.10 Optical transmittance spectrum of the ZIZO thin films.

Plots of $(ahv)^2$ versus absorption energy for the ZZTO thin films were shown in Figure 4.11. The optical absorption coefficient (a) and the optical energy band gap are related by the following equation:

$$ahv = C(hv - E_g)^{\frac{1}{2}}$$

where h is Planck's constant, v is the frequency of the incident photon, C is a constant for a direct transition, and a is the optical absorption coefficient. As the ratio of Zr content increased, the optical band gap increased, from 3.64 to 3.68 eV. Wide optical band gaps of thin films have large activation energies between the Fermi level (E_f) and the conduction band minimum (E_c), and thermally activated carriers were reduced according to $n = N_c \exp[-(E_c-E_f)/kT]$. The resistivity of the ZIZO thin films was consistently larger than that of the IZO thin film.
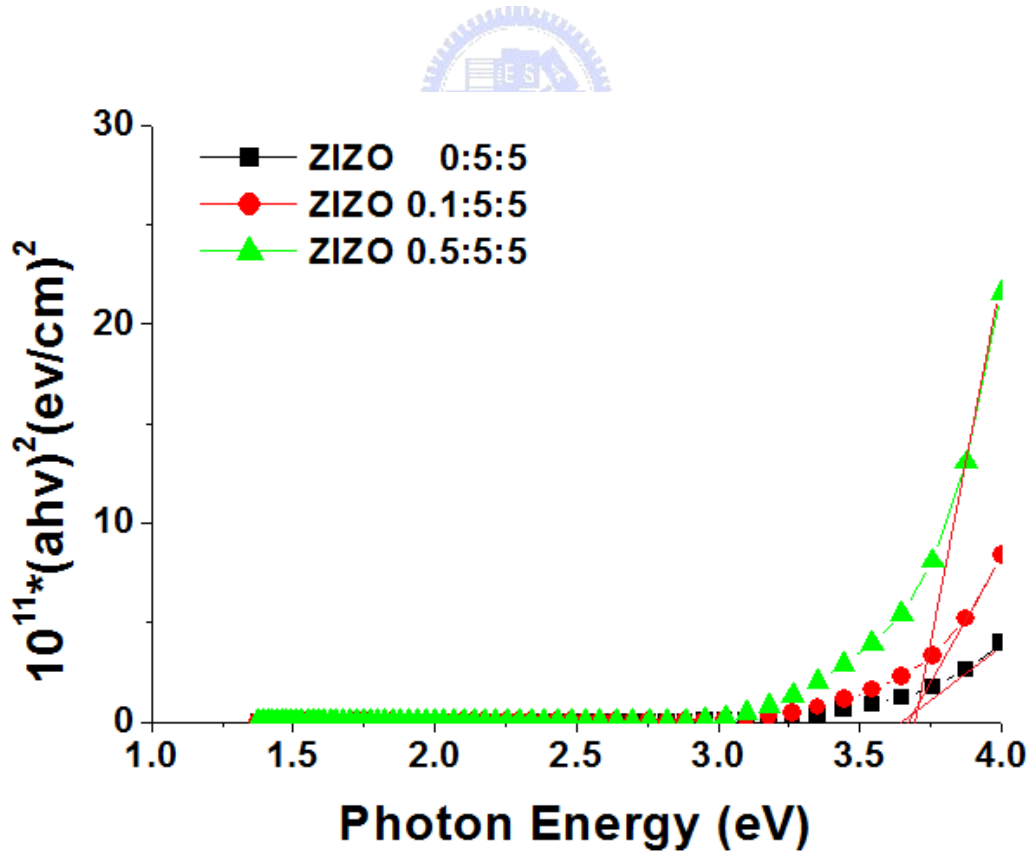
Figure 4.11   Plots of $(ahv)^2$ vs hv extracted from Figure 4.10.

4.8 The Analysis of XPS Measurement

XPS spectra of Zr, In, Zn ions with respect to the Zr content, and pre-annealing temperature was shown in the Figure 4.11. The Zr $3d_{5/2}$, In $3d_{5/2}$, Zn $2p_{3/2}$, centered at 183.4, 445.6, and 1022.8 eV, which indicated Zr-O, In-O, and Zn-O bonds, respectively.

First, we investigated the effect of the Zr content. As expected the intensity of the Zr $3d_{5/2}$ peak decreased the decreasing Zr content. The peak of Zr $3d_{5/2}$ centered at 183.4 eV was attributed to the fully oxidized zirconium. When the Zr content was decreased, it could cause a shift in the lower binding energy of In $3d_{5/2}$ and Zn $2p_{3/2}$ peaks from 445.6 and 1022.8 eV to 445.2 and 1022.2 eV, respectively.

Finally, we investigated the effect of the exposure to the atmosphere. In Figure 4.12, we observed that the binding energy of the peaks for the device prepared with the ratio of Zr: In: Zn = 0.5: 5: 5 was different than others after 2 days. According to Figure 4.4, we observed that the transfer performances became stable after 8 day. We inferred that the chemical reaction had not been completed yet. Therefore, the XPS pattern was similar to that of the device. On the other hand, after 7th day, the Zr $3d_{5/2,}$ In $3d_{5/2}$ and Zn $2p_{3/2}$ peaks shifted from 181.8, 444.2 and 1021.2 eV to 183.4, 445.6 and 1022.8 eV respectively. The shifted peaks indicated that a chemical reaction occured.

According the pattern of XPS, we calculated the real ratio of Zr: In: Zn = 0: 5: 5, 0.1: 5: 5, 0.5: 5: 5was 0: 3: 2, 1: 2: 2, 4: 11: 5, respectively.
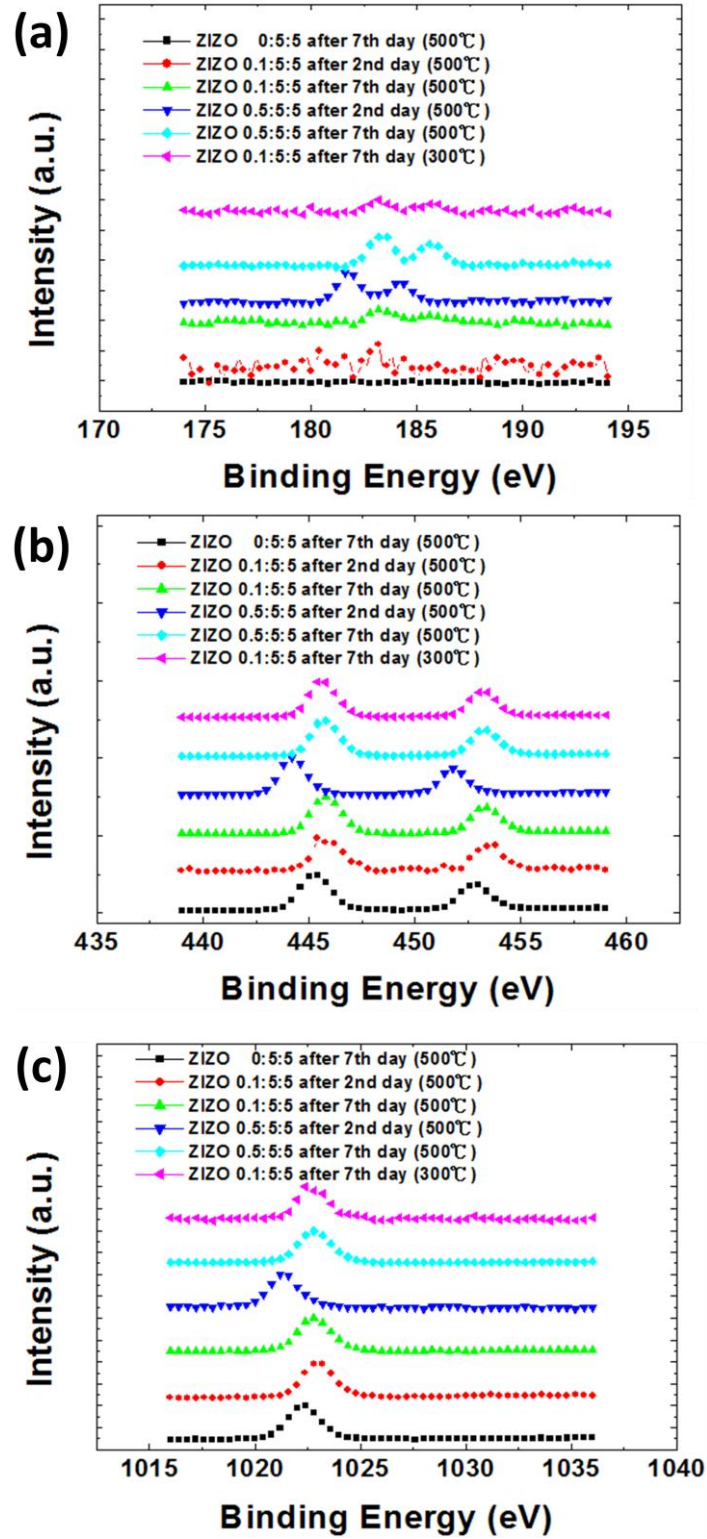
Figure 4.12   (a) Zr 3d$_{5/2}$ (b) In 3d$_{5/2}$ (c) Zn 2p$_{3/2}$ core-level XPS spectra of the ZIZO

thin films as a function of Zr content, pre-annealing temperature and day in the

atmosphere.

Figure 4.13 shows the O 1s region of the XPS spectra with respect to Zr content. The O 1s peak could be deconvoluted into two peaks centered at 531.3 and 532.9 eV, determined by Gaussian fitting. The O 1s peak could be explained with the binding state of oxygen with metals. The lower energy oxygen peaks was defined as O_I, the higher as O_{II}. O_I represented the O^{2-} ions combined with Zr, In and Zn ions in the ZIZO system. O_{II} was associated with oxygen vacancies in the ZIZO compound. O_{total} denoted the total O 1s peak area. When increasing the Zr content, the O_{II}/O_{total} value representing the ratio of oxygen vacancies gradually decreased from 0.486 to 0.289. Not only O_{II}/O_{total} but also O_{II}/O_I was decreased from 0.967 to 0.6310. Therefore, incorporating Zr reduced oxygen vacancies, indicating that Zr acted as a carrier suppressor effectively.
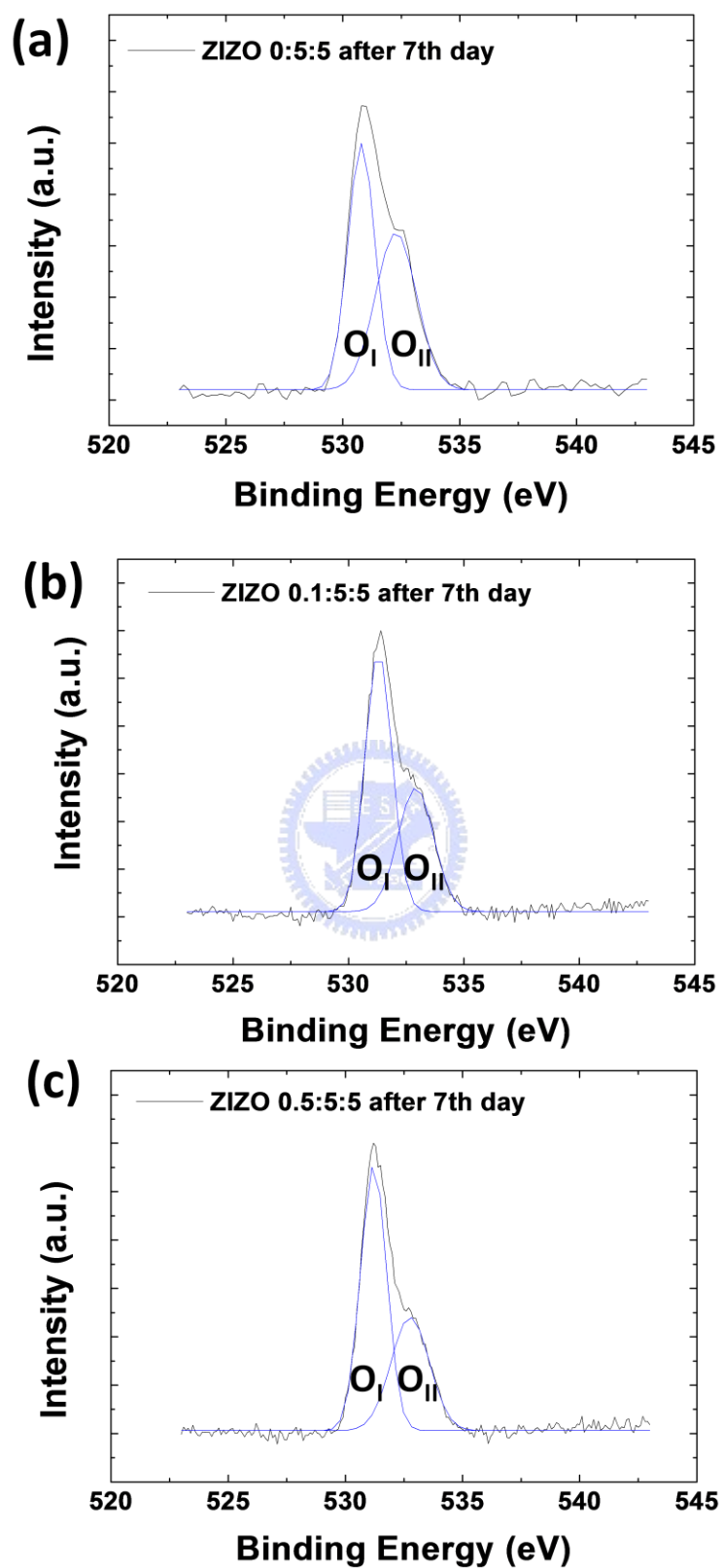
Figure 4.13   O 1s XPS spectra of the ZIZO thin films for Zr: In: Zn ratios of (a) 0:

5: 5 (b) 0.1: 5: 5 (c) 0.5: 5: 5.

Table 4.4   Variation in the area ratio of O 1s

Zr:In:Zn	Binding Energy (eV)	Ratio	Area	O_{II}/O_I
0:5:5	531.3	O_I/O_{total}	0.502	0.967
	532.9	O_{II}/O_{total}	0.486	
0.1:5:5	531.3	O_I/O_{total}	0.516	0.6337
	532.9	O_{II}/O_{total}	0.327	
0.5:5:5	531.3	O_I/O_{total}	0.458	0.6310
	532.9	O_{II}/O_{total}	0.289	

Chapter 5

Conclusion

In conclusion, we have demonstrated a solution-processable approach for manufacturing high-performance ZrInZnO (ZIZO) thin film transistors (TFTs). We studied Zr as a candidate material for carrier suppressor in the IZO systems in place of other common suppressors, such as Ga. The ZIZO TFTs exhibited a field effect mobility of 3.8 cm^2/Vs, an on-off ratio of ~10^7. The threshold voltage (V_{th}) was 0.44 V and the subthreshold swing was 0.42 V/dec. The threshold voltage became stable under the bias stress. Further, ZIZO thin film was amorphous. When the pre-annealing temperature increased, the crystallization was improved. Analysis of the O 1s peak in the XPS spectra showed decreasing the O^{2-} ions related to the variation in the concentration of oxygen vacancies which can supply free electrons. By adding NaOH, we could speed up the hydroxylation reaction. Overall the device performance is almost comparable with that of the device made by conventional cosputtering methods. Our method offers another possible way to low-cost, high-through manufacture for next generation TFTs for display applications.

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