國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

利用介面鈍化與電漿處理對原子層沉積二氧化鉿/砷化銦金氧半電容之研究

Investigation of Atomic-Layer-Deposition HfO_2/InAs Metal-Oxide-Semiconductor Capacitors with Interfacial Passivation and Plasma Treatments

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指導教授：簡昭欣 教授

中 華 民 國 一 〇 一 年 十 月

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電 子 工 程 學 系　電 子 研 究 所 碩 士 班

碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of Master of Science

In Electronics Engineering

November 2012

Hsinchu, Taiwan, Republic of China

中 華 民 國 一 〇 一 年 十 月

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摘要

在這篇論文中，首先我們研究了在原子層沉積主要高介電常數絕緣層前利用前驅物做”自我清潔”的預處理，其中有三氧化二鋁的前驅物-三甲基鋁[TMA, $Al(CH_3)_3$]，以及二氧化鉿的前驅物-四(乙基甲基氨基)鉿[$Hf(N(C_2H_5)(CH_3))_4$]。之後沉積不同的閘極介電層，分別是三氧化二鋁以及二氧化鉿，和前驅物預處理採用排列組合方式選出三種閘極介電層。並藉由二種後沉積熱過程，後沉積退火 400 度 120 秒以及 300 度 30 分鐘氫氣氮氣混合之熱退火。我們發現利用後沉積退火對於成長不同高介電常數絕緣層之砷化銦金氧半電容電性上並無明顯的趨勢，反之利用 300 度 30 分鐘氫氣氮氣混合之熱退火則大幅改善了各種高介電常數絕緣層以及絕緣層/砷化銦介面的品質。三種不同的閘極介電層各經過 300 度 30 分鐘氫氣氮氣混合之熱退火，三甲基鋁[TMA, $Al(CH_3)_3$]前驅物預處理/二氧化鉿閘極介電層擁有最佳化的電性條件，並且將此閘極介電層繼續進行下一步的電漿研究。

其次，我們研究了在原子層沉積閘極介電層中加以不同次數之氧氣電漿處理，觀察其對二氧化鉿/砷化銦金氧半電容電性之影響。我們發現當採用高次數電漿處理時，二氧化鉿/砷化銦金氧半電容在聚積、空乏、以及反轉區域有比較小的頻率分散現象，表示其對於閘極介電層以及閘極介電層/砷化銦介面的品質有較好的改善能力。再經過 300 度 30 分鐘氫氣氮氣混合之熱退火則可以進一步改善閘極介電層以及介電層/砷化銦介面的品質。

最後，我們利用建立一個閘極介電層內缺陷的模型解釋基板在操作大閘極偏壓下其費米能階附近的電子和閘極介電層內缺陷的穿隧機制。利用此模型所計算出的參數和實驗所得的多重頻率下電容-電壓與電導-電壓數據做媒合，可以定量地萃取出在閘極介電層內的缺陷密度-單位為體密度而非傳統介面捕捉缺陷密度-面密度。

Investigation of Atomic-Layer-Deposition HfO_2/InAs Metal-Oxide-Semiconductor Capacitors with Interfacial Passivation and Plasma Treatments

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ABSTRACT

In this thesis, first of all, we investigated the “self-cleaning” pretreatment before the main high-*k* dielectric in atomic-layer-deposition system, by the precursor of Al_2O_3 - trimethyl aluminum [TMA, $Al(CH_3)_3$], and the precursor of HfO2 - tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf(N(C_2H_5)(CH_3))_4$]. Then the high-*k* dielectrics, Al_2O_3 and HfO_2 with precursors trimethyl aluminum [TMA, $Al(CH_3)_3$] and tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf(N(C_2H_5)(CH_3))_4$] were chosen three gate dielectrics by the way of permutation and combination. And we applied two post-deposition thermal processes, post deposition annealing (400℃/120s) and forming gas annealing (300℃/30min.). We found that there was not clear trend for InAs MOS capacitors with different high-*k* dielectrics in post deposition annealing. However, adopting forming gas annealing, the obvious improvement on high-*k* dielectrics and high-*k* dielectric/InAs interface quality was observed. For three different gate dielectrics, all of them in forming gas annealing (300℃/30min.),

TMA/HfO_2 gate dielectric has the optimum electrical properties. Then, we utilized this dielectric to further research in plasma treatments.

Secondly, we investigated the effects on the HfO_2/InAs MOS capacitors by various numbers of times in plasma treatments during the process of atomic-layer-deposition. It is observed that there are weak frequency dispersion in the regions of accumulation, depletion, and inversion, by using higher times of plasma treatment. This represented that the ability of improving high-*k* dielectrics and high-*k* dielectric/InAs interface quality is great for high plasma density treatment. By applying forming gas annealing (300℃/30min.), the high-*k* dielectrics and high-*k* dielectric/InAs interface quality were further improved.

Finally, we built up a model to explain the tunneling mechanism between the electrons near Fermi level of the substrate and traps in the gate dielectric which is operated at high gate bias. We fitted the calculations of the model with experimental data, multi-frequency *C-V* and *G-V*, and then we could quantitatively extract the traps density in the gate dielectric, which is in unit of volume density. Unlike interface state, is in unit of areal density.

誌謝

首先，我要感謝指導教授簡昭欣教授。在這碩士班二年多的學習生涯中，給予了我極大的研究空間與機會，讓我可以順利地完成碩士學位。不僅僅只在研究方面給予支持，在待人處事方面發現老師總是嚴以律己，寬以待人，學習到了許多應對之道。老師在學術的專業上總是領先，在 meeting 討論中總是能切中其他期刊作者的優缺點，而對追求知識的渴望更是不落人後，實在是令我好生敬佩。所幸在碩士班能被老師所指導，讓我在研究的能力更躍進的一大步。

其次要感謝的是信淵學長，從我是一片空白帶起，不論帶領我做實驗、授受量測技巧、關心實驗進度等，讓我這一年多來學習到的東西太多太多。並且總是仔細地回答我所問的問題(甚至有時候還很蠢的)，即使剛開始前實驗不甚順利，但與學長相處下來學習到從實驗不順利的可能發生原因去作探討，一一將問題列出去找出答案，嚴謹性不在話下，這才是做研究嘛!還有總是具有過目不忘的能力實在是令我佩服得五體投地，改天一定要和學長請教請教。

再來想感謝的是哲偉學長，常常關心我實驗的進度，和我聊他念碩士時的心路歷程，總是能被學長開導，我們一起互相 cover 實驗的日子我會記得的。政廷學長，總是會幫我回答一些瑣事上的問題，在實驗室發生的問題第一個總是先想到學長，簡直是一本活動百科。宏基學長，在 NFC 一起努力做實驗時，總是會讓我安心做實驗，畢竟有 NFC 扛壩子撐腰，又有無限的氣場充斥著 NFC，實驗必定會安然做完！韋志學長，剛進 NFC 或 NDL 做實驗時大部分機台都有被你訓練過，你的“手順”技巧實在是太強大了。昶智學長，碩一時常問你課業上的問題，碩二也常問你實驗問題，感謝學長總是細心地教導。宇彥學長、宗佑學長，感謝學長們在其他事務上的大力協助。

一起努力的同仁們，Cookie、George、哲鎮，在做實驗的努力過程中，總是一起相互扶持，互相 cover 實驗，我們一起打拚、一起歡笑的日子我會永遠記住

的。學弟妹們，邦聖、主元、品輝、純敏，尤其是邦聖、主元，感謝你們在我最後努力過程中幫我 cover 部分實驗，讓我可以安心地做其他論文上的事，希望你們都能夠順利做完實驗如期畢業。

最後，要感謝我的父母以及家人，沒有你們的經濟和精神上支持，我根本無法完成碩士學位，謝謝你們在我冗長的學習生涯中賦予我極大的鼓勵。

林俊池

於新竹交通大學

2012 年 10 月 31 日

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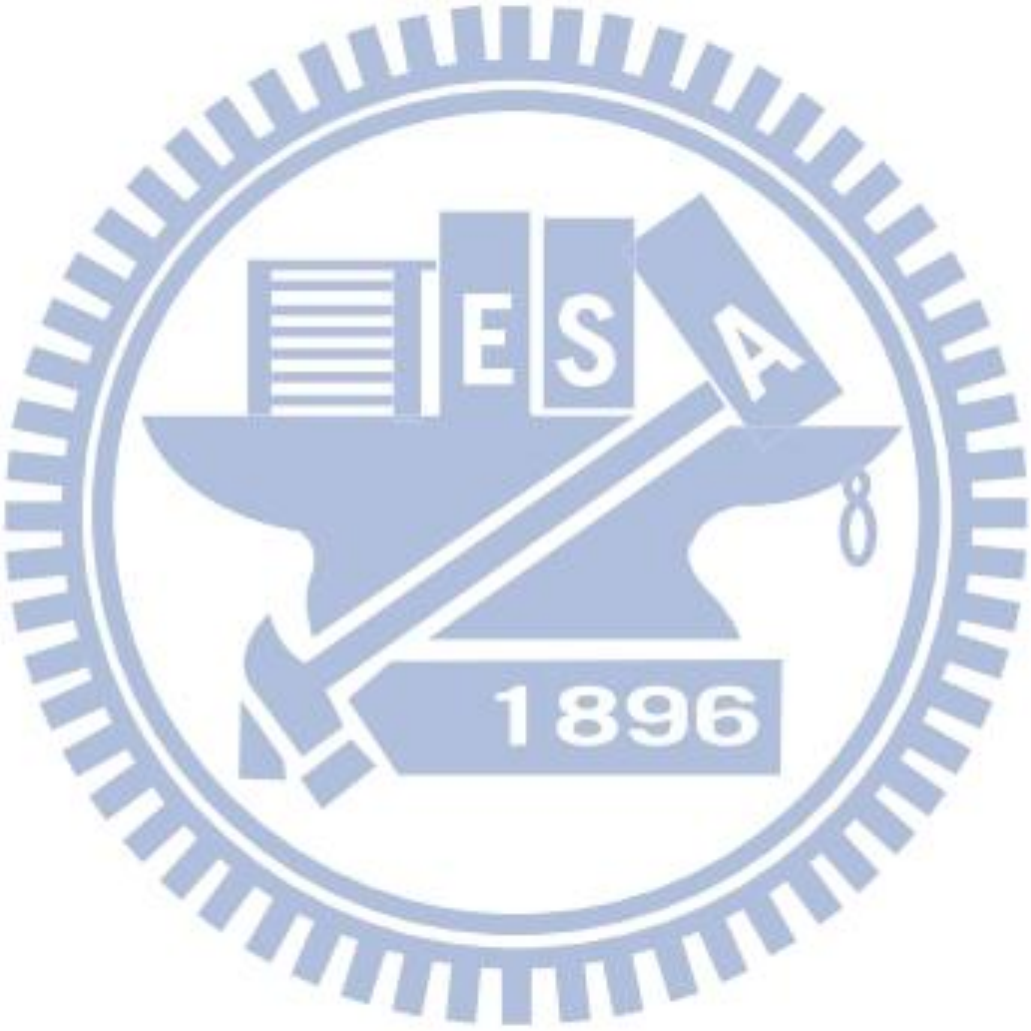

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Chapter 1

Introduction

1.1 Overview of CMOS Research Roadmap and Device Scaling Issues

Despite architectures and working principles of the metal oxide semiconductor field-effect-transistors (MOSFETs) have remained the same, the physical dimensions have been continually reduced to reduplicate the number of transistors on a chip every eighteen months according to the Moore's Law. The scaling in transistor dimensions has result in device performance enhancement over technology generations. The rapid advancement of complementary metal oxide semiconductor (CMOS) integrated circuit technologies during the past few decades has compelled the Si-based micro-electronics industry to confront several huge technological challenges and to try out some theoretical limits. Not only R. Chau, Intel Corporation, has demonstrated the scaling roadmap in the progress of the Si metal oxide semiconductor field-effect-transistors (MOSFETs), as shown in **Fig.1.1**, but M. J. Wolf, Fraunhofer IZM, even mentioned the next several scaling generation, as presented in **Fig.1.2**. It was found that within the next two generations, the lateral dimensions of the transistor will approach the physical limits and even ultimately be composed of a few atoms. Also, Moore's Law scaling can't maintain the pace of progress and packaging to enable equivalent scaling anymore.

In fact, at the early epoch of the 90-nm node, substrate engineering and uniaxial strain technologies---e.g., pseudomorphic SiGe channels grown on Si substrates for p-MOSFETs [1] and strained Si channels on the relaxed graded SiGe buffer layers for n-MOSFETs [2]---have been developed to enhance the carriers mobility in the channel. As scaling down to the 45-nm node, high-*k* materials being in place of ultra-thin conventional SiO_2 or oxynitrides are adopted as alternative gate dielectrics for leakage concerns and reliability issues. When the devices scaled down further, unfortunately, device performances are not coming up with the scaling trend, which is due to the amplification of parasitic characteristics. Therefore, numerous device structures and materials are continuously explored and proposed imperiously in an effort to alleviate the immense scaling problems and pressure required to improve device performances. In recent years, various types of non-planar tri-gate architectures, carbon nanotubes, nanowires, and high-carrier-mobility materials (Ge, III-V…) capture increasing attentions. Among above advanced researches, the practicability of integrating various prevailing high-*k* dielectrics with high-carrier-mobility substrate (or channel) is one of promising way due to the advanced progress in the development of high-k dielectrics in Si CMOS applications. Through the **Table 1.1**, we can contrast with the material properties of bulk Si, Ge, GaAs, $In_{0.53}Ga_{0.47}As$, and InAs at 300K [3]. We can find that InAs owns the much higher electron mobility (30x) than that in Si, accordingly, InAs is considered a new promising candidate to be n-channel material for high-performance logic circuit devices. However, relative to Si, Ge, GaAs, and $In_{0.53}Ga_{0.47}As$ have benefits of higher enhancements in electron velocity and mobility. Consequently, III-V materials are favorable for n-channel MOSFETs, nevertheless, Ge is suitable to be n- and p-channel MOSFETs. So far, the characteristics of the potential devices, such as Ge, [4], [5], (In)GaAs [6], and InSb [7] channels with high-*k* dielectrics either Al_2O_3 or HfO_2

incessantly demonstrated, and they even exceed the traditional Si transistors at the sub-micro-scale gate length in device performances [8]. Thus it is important to describe more details of the device challenges and process difficulties by making use of the high-carrier-mobility channels/substrates. We will discuss these themes in the following **Session 1.2**.

1.2 Device and Process Challenges and Issues in High Mobility Channels on Si Platform

As mentioned in the previous section, splendid progresses in the deposition of high-*k* materials enable renewed interest in high-carrier-mobility channels/substrates to be as a main transport channel in combination with various high-*k* dielectrics. It has been well recognized that new device engineering is essential to surmount difficulties of advanced CMOS and realizing high performance large-scale-integrated systems (LSIs) under 10-nm regime. According to the future evolution scenario of CMOS device/process technologies presented in the International Technology Roadmap for Semiconductors (ITRS) 2010 edition [9], new channel materials with enhanced carrier transport properties are extremely anticipated for further boosting driving current and resulting large-scale-integrated systems (LSIs) performances, besides the enhancements of gate stacks using high-*k* dielectrics/metal gate and the channel electrostatics control using fully-depleted SOI and multi-gate MOSFETs. Here, the high-carrier-mobility channel materials and, more indispensably, light effective mass, are preferable under quasi-ballistic transport expected in extremely-short channel regime [10]. Beginning with this viewpoint, intensive attentions have been paid to SiGe , Ge, and III-V semiconductor channels. On account of extremely high electron

mobility and light electron effective mass of Ge and III-V semiconductors such as GaAs, InGaAs, and InAs and extremely high hole mobility and light hole effective mass of Ge, Ge and III-V materials are favorable for high device performance CMOS applications.

Fig. 1.3 presents a variety of possible applications of III-V/Ge materials on Si CMOS platform [11]. The CMOS device making use of those non-Si channel materials are agreeing with the so-called More Moore approach seeking for higher driving current. There are many possible CMOS configurations currently. III-V n-channel MOSFET and Ge p-channel MOSFET can be mixed with strained-Si devices, aggressively developed so far. In addition, if III-V p-channel MOSFET or Ge n-channel MOSFET are grasped, III-V CMOS or Ge CMOS is also feasible in terms of the simplicity of the channel structures. In particular, one of the terminal CMOS structure can be a combination of III-V channel n-MOSFET and Ge channel p-MOSFET [10, 12].

In order to understand such a III-V/Ge CMOS practical to large-scale-integrated systems (LSIs), there are many technological challenges and issues to be settled for realizing III-V/Ge MOSFETs on Si substrates, which are enumerated as follows: (1) gate insulator formation with superior MOS/MIS interface quality (2) high quality III-V/Ge film formation on Si substrates (3) low resistivity source/drain formation (4) total CMOS integration [10]. These critical challenges and issues are schematically presented in **Fig. 1.4**.

CMOS family applying III-V/Ge channels on Si substrates can be crucial devices for high performance and low power advanced large-scale-integrated systems (LSIs) in the future. The critical issues and the key technologies for realizing III-V/Ge-based channel MOSFETs on Si platform have been brought up. However, there are still some critical issues to be solved. Up-to-date progresses on MOS/MIS interface

quality control technologies, the III-V/Ge thin body channel formation technologies, the channel mobility boosting technologies including surface orientation engineering and the source/drain junction technologies are causing III/V/Ge channel MOSFETs more promising for future applications to high performance and low power advanced large-scale-integrated systems (LSIs). Therefore, we can conclude that ultra-thin-body based III-V/Ge MOSFETs on Si CMOS platform can be a potential candidate as the device structure under the 15-nm technology node and beyond.

1.3 Scope and Organization of the Thesis

One promising high-carrier-mobility substrate materials, InAs, is researched in this thesis. As discussed in the previous section, it is introduced that the first challenge is how to improve the interface quality between the deposited high-*k* dielectric films and InAs substrate. So we devoted to our efforts to the diverse *in-situ.*pre-deposition treatment, and *in-situ.* O_2-plasma treatment on the physical and electrical properties of various alternative high-*k* dielectrics on InAs substrate.

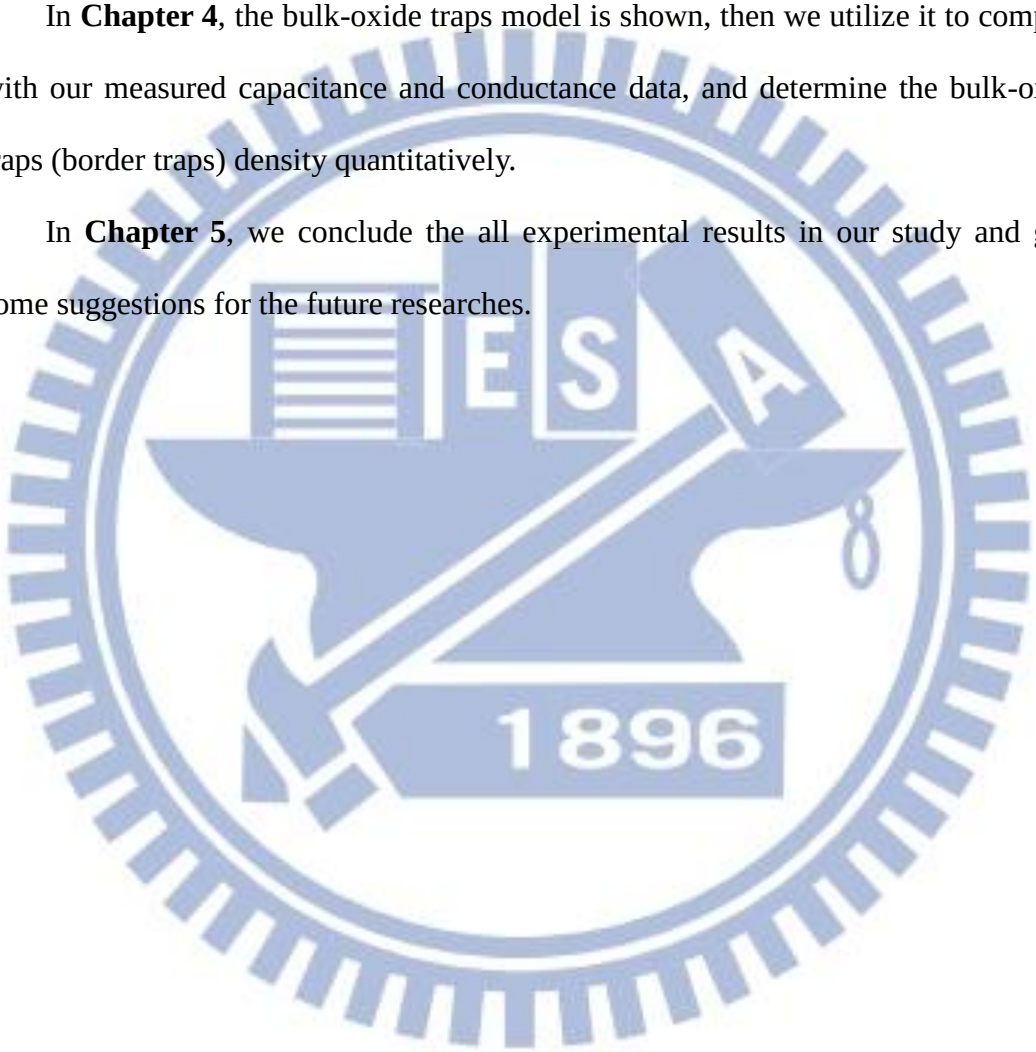
In **Chapter 1**, a concise overview of the background and motivation is described. The MOSFET scaling roadmap and possible progresses come out in the nanoscale device. Then, we discussed the significance and the process challenges/issues of high-carrier-mobility III-V/Ge CMOS on Si platform.

In **Chapter 2**, utilizing "self-cleaning" before atomic-layer-deposition process for several high-*k* dielectrics to passivate high-*k*/InAs interface is demonstrated. Then, we investigate the effects of post-deposition thermal processes, post deposition annealing and forming gas annealing on InAs MOS capacitors electrical characteristics.

In **Chapter 3**, various plasma treatments are investigated during and post atomic-layer-deposition process. We confer their influence on the electrical properties of InAs MOS capacitors. Then we apply post deposition annealing and forming gas annealing process to further examine the change of the measured electrical characteristics.

In **Chapter 4**, the bulk-oxide traps model is shown, then we utilize it to compare with our measured capacitance and conductance data, and determine the bulk-oxide traps (border traps) density quantitatively.

In **Chapter 5**, we conclude the all experimental results in our study and give some suggestions for the future researches.



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Material	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs
Lattice constant (Å)	5.431	5.646	5.653	5.869	6.058
Bandgap E_g (eV)	1.12	0.66	1.42	0.74	0.35
Intrinsic carrier concentration n_i (cm^{-3})	9.6E9	2.4E13	2.1E6	6.3E11	1.0E15
Conduction band density of states N_c (cm^{-3})	2.8E19	1.04E19	4.7E17	2.1E17	8.7E16
Valence band density of states N_v (cm^{-3})	1.04E19	6E18	9E18	7.7E18	6.6E18
Electron velocity v_e (cm/s)	2.3E7	3.1E7	4.4E7	5.8E7	7.7E7
Electron mobility μ_e (cm^2/V-s)	1350	3900	8500	12000	33000
Hole mobility μ_h (cm^2/V-s)	480	1900	400	300	460

Table 1.1 Material properties of bulk Si, Ge, GaAs, $In_{0.53}Ga_{0.47}As$, and InAs at 300K.

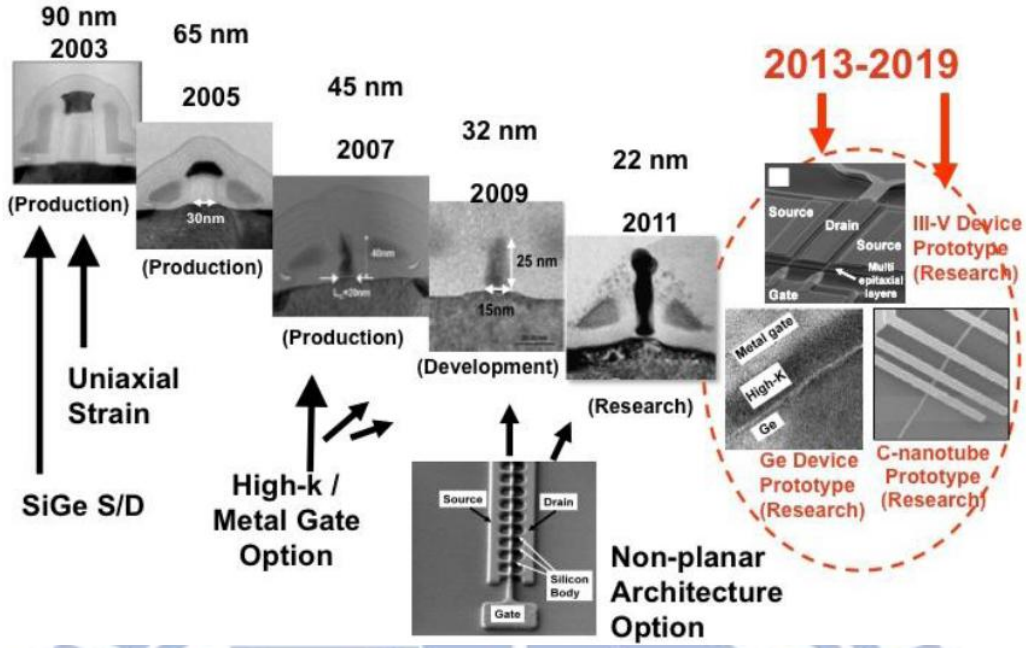

Fig. 1.1 Transistor scaling and research roadmap introduced by R. Chau, Intel Corp.

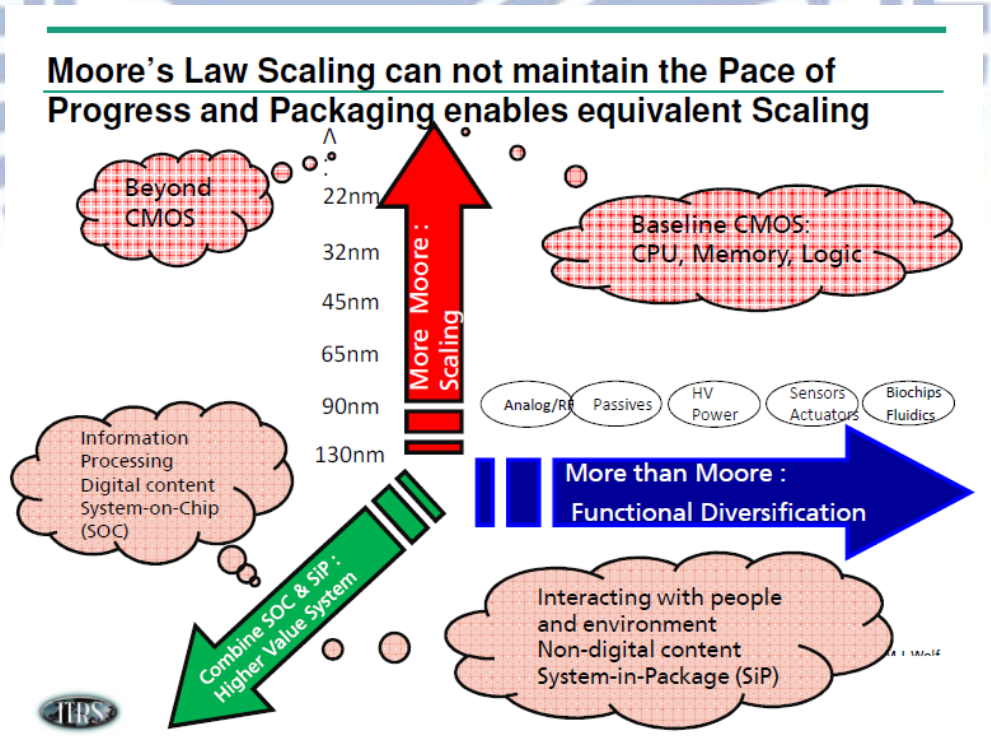

Fig. 1.2 Moore's Law can't maintain the pace of progress and packaging to enable equivalent scaling (demonstrated by M. J. Wolf, Fraunhofer IZM).

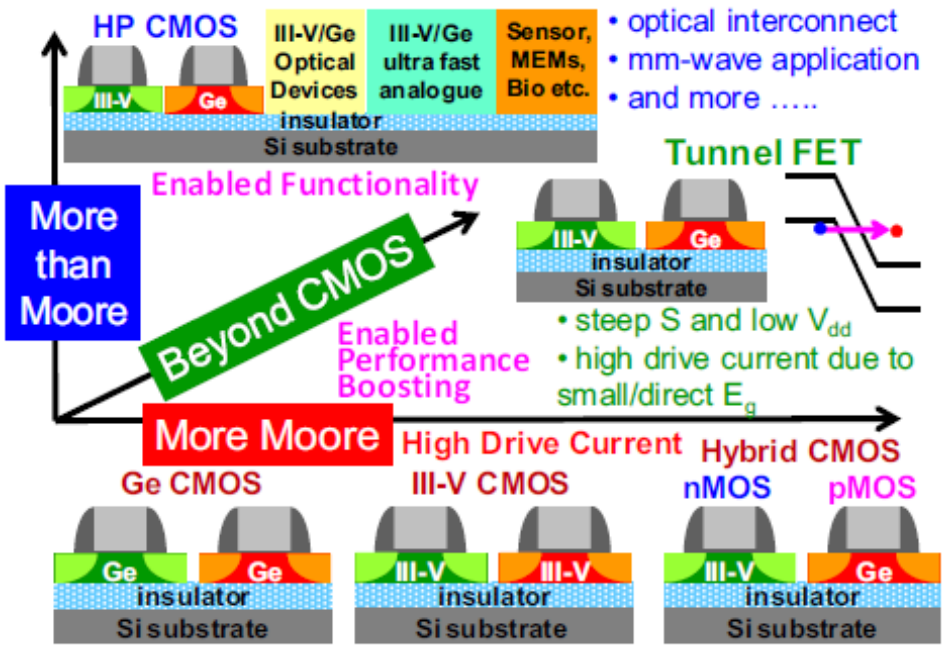

Fig. 1.3 Possible evolution scenario for III/V/Ge devices on Si platform through heterogeneous integration

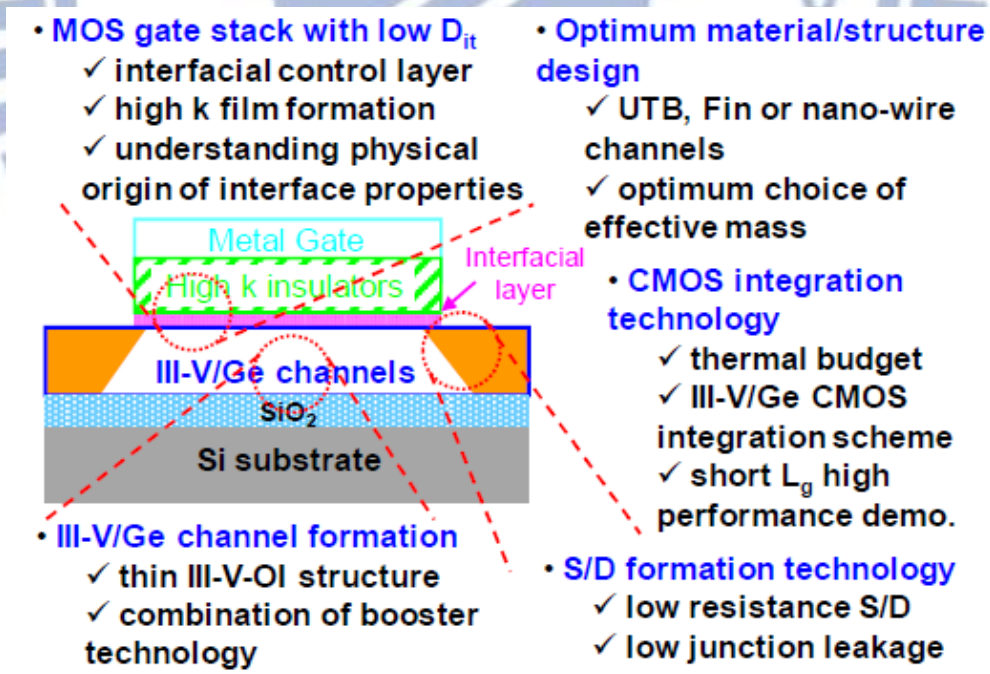

Fig. 1.4 Critical issues for III-V/Ge MOSFETs on Si platform

Chapter 2

InAs nMOSCAPs with Various Pretreatments on High-κ Dielectrics by Atomic-Layer-Deposition (ALD) System

2.1 Introduction

The rapid growth of the integrated circuit industry has been based on the continuous downscaling of complementary metal-oxide-semiconductor (CMOS) technology. However, as the channel length approach 22-nm, further scaling will become problematic. The III-V metal-oxide-semiconductor field-effect transistor (MOSFET) with high-*k* dielectric materials is one of the promising candidates for the 22-nm generation of CMOS technology or beyond. It is demonstrated that high mobility III-V channel materials have emerged as a potential solution and are under strong investigation to further enhance the device performance [1]. Among the choices of alternative channel/substrate materials, InAs remarkably possesses high electron mobility (~33000 $cm^2 V^{-1} s^{-1}$) and saturation drift velocity (~8 x 10^7 cm/s) [2]. Nevertheless, in the case of most III-V semiconductors, the lack of a high-quality interface between insulator and substrate is the main obstacle for the delayed development of InAs MOSFET. Previous efforts have been focused on reducing the effect of the native oxide on InAs surface such as by depositing Si, Ge, and Si-Ge interfacial passivation layers [3-5], ammonium sulfide passivation before oxide

deposition, and hydroxylation of the surface [6]. Late development in the deposition method of high-*k* dielectrics has opened more possibilities in this region. It has been reported that the semiconductor-dielectric interface properties have been improved for GaAs and InGaAs with low indium content [7]. Compared with the aforementioned channel/substrate materials, InAs has much higher bulk electron mobility and saturation drift velocity. Recently, the "self-cleaning" of the interfacial dielectric by trimethyl aluminum [TMA, $Al(CH_3)_3$] precursor was proposed for the atomic-layer-deposition (ALD) of oxide film on III-V semiconductors such as GaAs [8-10], InGaAs [11, 12], and InSb [13, 14]. Though there are some researches in the MOS properties of atomic-layer-deposition (ALD) high-*k* dielectric materials on InAs [15, 16], the influence of the ALD precursors on the reduction of native oxides at the InAs surface hasn't been adequately studied.

In our work, the effect of trimethyl aluminum [TMA, $Al(CH_3)_3$] precursor pre-deposition treatment in combination with Al_2O_3 is studied. We also utilize tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf(N(C_2H_5)(CH_3))_4$] precursor pre-deposition treatment in conjunction with HfO_2. Ultimately, we combine trimethyl aluminum [TMA, $Al(CH_3)_3$] precursor pre-deposition treatment with HfO_2, then discuss the pre-deposition precursor treatment on the physical and electrical characteristics of all the n-InAs MOSCAP structures.

2.2 Experimental Procedures of InAs nMOSCAPs

2.2.1 ALD-TMA/Al_2O_3 Growth and Capacitor Fabrication

(100)-oriented n-InAs substrates are prepared with doping concentration of ca. 1 x 10^{17} cm^{-3} (resistivity ca. 0.002Ω·cm). Before gate dielectric formation, all of the wafers were pre-cleaned by acetone (ACE), isopropanol (IPA), and dilute HCl (1:10) for 5, 5, 2 min., respectively, to remove the native oxide, the treated wafers were loaded into ALD chamber. *In situ* trimethyl aluminum [TMA, $Al(CH_3)_3$] precursor pretreatment was done by using 10cycles of TMA/N_2 with a period of 0.06s for a TMA pulse and 10s for a N_2 pulse. After that, the Al_2O_3 thin film (TMA/N_2/H_2O/N_2 with durations of 0.06/10/0.04/10 s) was grown over 100cycles on the bulk InAs at substrate temperature of 250℃. The wafers were kept at the temperature of 250℃ during both precursor pretreatment and dielectric deposition process. Trimethyl aluminum [TMA, $Al(CH_3)_3$] and H_2O were selected as the Al metal source and oxidant, respectively. High-purity N_2 was applied as a purging gas to remove redundant reactants. The thickness of the Al_2O_3 film estimated from the number of the growth cycles, is approximate 10nm. Then, 50/500 Å Ti/Pt was deposited using sputter system to pattern gate electrode by shadow mask, and then a 500/700/300 Å-thick Au/Ge/Ni layer was deposited as the ohmic backside contact.

Two post-deposition thermal process were examined: (i) post deposition annealing (PDA) by rapid thermal annealing (RTA) at 400℃ in a N_2 ambient for 120s and (ii) forming gas annealing (FGA) at 300℃ in a H_2/N_2 (5%) mixed ambient for 30 min.. Optical microscopy exhibited that the gate electrode area of the capacitor was ca. 4 x 10^{-4} cm^2.

The process flow and device structure are shown in **Fig. 2.1**, **Fig. 2.2**.

2.2.2 ALD-TEMAH/HfO_2 Growth and Capacitor Fabrication

(100)-oriented n-InAs substrates are prepared with doping concentration of ca. 1 x 10^{17} cm^{-3} (resistivity ca. 0.002Ω·cm). Before gate dielectric formation, all of the wafers were pre-cleaned by acetone (ACE), isopropanol (IPA), and dilute HCl (1:10) for 5, 5, 2 min., respectively, to remove the native oxide, the treated wafers were loaded into ALD chamber. *In situ* tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf(N(C_2H_5)(CH_3))_4$] precursor pre-deposition treatment was done by using 10cycles of TEMAH/N_2 with a period of 0.1s for a TEMAH pulse and 10s for a N_2 pulse. After that, the HfO_2 thin film (TEMAH/N_2/H_2O/N_2 with durations of 0.1/10/0.04/10 s) was grown over 100cycles on the bulk InAs at substrate temperature of 250℃. The wafers were kept at the temperature of 250℃ during both precursor pretreatment and dielectric deposition process. Tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf(N(C_2H_5)(CH_3))_4$] and H_2O were selected as the Hf metal source and oxidant, respectively. High-purity N_2 was applied as a purging gas to remove redundant reactants. The thickness of the HfO_2 film estimated from the number of the growth cycles, is approximate 10nm. Then, 50/500 Å Ti/Pt was deposited using sputter system to pattern gate electrode by shadow mask, and then a 500/700/300-Å-thick Au/Ge/Ni layer was deposited as the backside contact.

Two post-deposition thermal process were examined: (i) post deposition annealing (PDA) by rapid thermal annealing (RTA) at 400℃ in a N_2 ambient for 120s and (ii) forming gas annealing (FGA) at 300℃ in a H_2/N_2 (5%) mixed ambient for 30 min.. Optical microscopy exhibited that the gate electrode area of the capacitor was ca. 4 x 10^{-4} cm^2.

The process flow and device structure are shown in **Fig. 2.3**, **Fig. 2.4**.

2.2.3 ALD-TMA/HfO_2 Growth and Capacitor Fabrication

(100)-oriented n-InAs substrates are prepared with doping concentration of ca. 1 x 10^{17} cm^{-3} (resistivity ca. 0.002Ω·cm). Before gate dielectric formation, all of the wafers were pre-cleaned by acetone (ACE), isopropanol (IPA), and dilute HCl (1:10) for 5, 5, 2 min., respectively, to remove the native oxide, the treated wafers were loaded into ALD chamber. *In situ* trimethyl aluminum [TMA, $Al(CH_3)_3$] precursor pre-deposition treatment was done by using 10cycles of TMA/N_2 with a period of 0.06s for a TMA pulse and 10s for a N_2 pulse. After that, the HfO_2 thin film (TEMAH/N_2/H_2O/N_2 with durations of 0.1/10/0.04/10 s) was grown over 100cycles on the bulk InAs at substrate temperature of 250℃. The wafers were kept at the temperature of 250℃ during both precursor pretreatment and dielectric deposition process. Tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf(N(C_2H_5)(CH_3))_4$]] and H_2O were selected as the Hf metal source and oxidant, respectively. High-purity N_2 was applied as a purging gas to remove redundant reactants. The thickness of the HfO_2 film estimated from the number of the growth cycles, is approximate 10nm. Then, 50/500 Å Ti/Pt was deposited using sputter system to pattern gate electrode by shadow mask, and then a 500/700/300-Å-thick Au/Ge/Ni layer was deposited as the backside contact.

Two post-deposition thermal process were examined: (i) post deposition annealing (PDA) by rapid thermal annealing (RTA) at 400℃ in a N_2 ambient for 120s and (ii) forming gas annealing (FGA) at 300℃ in a H_2/N_2 (5%) mixed ambient for 30 min.. Optical microscopy exhibited that the gate electrode area of the capacitor was ca. 4 x 10^{-4} cm^2.

The process flow and device structure are shown in **Fig. 2.5**, **Fig. 2.6**. The cross-sectional TEM images of as-deposited Pt/Ti/TMA+HfO_2/n-InAs capacitor are shown in **Fig. 2.7**.

2.3 Capacitor Characteristics of InAs nMOSCAPs with Different Post-Deposition Thermal Processes

The capacitance-voltage and conductance-voltage characteristics of all the capacitors were measured by using HP4284A *LCR* meter at the temperature of 300K. **Fig. 2.8** displays the multi-frequency *C-V* properties, **Fig. 2.9** presents the multi-frequency *C-V* maps, and **Fig. 2.10** shows the $G/Aq_0\omega$-*V* contours, of Pt/Ti/TMA+Al_2O_3/n-InAs capacitors, w/o or w/ PDA (400℃/120s) and before or after FGA (300℃/30min.), respectively. Similarly, **Fig. 2.11**, **Fig. 2.12**, **Fig. 2.13** exhibit the multi-frequency *C-V* properties, the multi-frequency *C-V* maps, and the $G/Aq_0\omega$-*V* contours, of Pt/Ti/TEMAH+HfO_2/n-InAs capacitors, w/o or w/ PDA (400℃/120s) and before or after FGA (300℃/30min.), respectively; **Fig. 2.14**, **Fig. 2.15**, **Fig. 2.16** exhibit the multi-frequency *C-V* properties, the multi-frequency *C-V* maps, and the $G/Aq_0\omega$-*V* contours, of Pt/Ti/TMA+HfO_2/n-InAs capacitors, w/o or w/ PDA (400℃/120s) and before or after FGA (300℃/30min.), respectively.

We qualitatively define one of the capacitor characteristics through the variation of the capacitance ΔC as follows:

$$\Delta C(@V_g = 3V) = \{[C_{acc}(@100Hz) - C_{acc}(@1MHz)] / C_{acc}(@1MHz)\} \times 100\% \quad (2.1)$$

Where ΔC is the frequency dispersion of the accumulation capacitance measured in 1MHz and 100Hz for the V_g = 3V. The overview of all of the capacitors in frequency dispersion is shown in **Table. 2.1**.

2.3.1 *C-V* and *G-V* properties of InAs nMOSCAPs w/ PDA

At first, we confer the effect of applying post deposition annealing. From **Fig. 2.8 (a)(b)**, **Fig. 2.9 (a)(b)**, for TMA/Al_2O_3, comparing the as-deposited one with w/ PDA one, we find that the capacitance characteristics is similar, but the gate control of as-deposited one is better than w/ PDA one due to its smaller stretch-out curve. Then, from **Fig. 2.10 (a)(b)**, the conductance at high frequency with highly negative V_g of as-deposited one is larger than that of w/ PDA one. We suppose that the conductance at high frequency with highly negative V_g is minority carrier (hole) response (G_{inv}). Also, the conductance at low frequency with highly positive V_g of as-deposited one and w/ PDA one are both supposed to the border trap response of the high-*k* dielectrics. The frequency dispersion $\triangle C$ of as-deposited one (8.05%) is weaker than w/ PDA one (8.70%), is shown in **Table. 2.1**., which may reveal the lower number of border traps for as-deposited one.

Moreover, from **Fig. 2.11 (a)(b)**, **Fig. 2.12 (a)(b)**, for TEMAH/HfO_2 contrasting the as-deposited one with to w/ PDA one, we observe that the accumulation and inversion capacitance of as-deposited one at V_g = 3V is much larger than that of w/ PDA one, and minimum of capacitance of the two are about the same, that is to say, the gate control of the as-deposited one is much better than that of w/ PDA one. And from **Fig. 2.13 (a)(b)**, the conductance at high frequency with highly negative V_g of as-deposited one is much larger than that of w/ PDA one, and we suppose the contours shows that there is a strong interface trap response (G_{it}) with G_{inv}. In other words, the response of G_{inv} accompanying with G_{it} of as-deposited one is larger than that of w/ PDA one which is consistent with aforementioned one. We also note that there is a stronger frequency dispersion in the inversion regime of as-deposited one than that of w/ PDA one, which probably implies the higher contribution of interface traps.

However, it should be examined deeply. The frequency dispersion $\triangle C$ of as-deposited one (16.2%) is stronger than w/ PDA one (10.3%), is shown in **Table. 2.1**., which may reveal the higher number of border traps for as-deposited one.

Furthermore, from **Fig. 2.14 (a)(b)**, for TMA/HfO_2, as-deposited one in comparison with w/ PDA one, is lower in the accumulation capacitance and inversion capacitance, but the similar property of band bending transition from C_{max} to C_{min}, that is to say, the gate control of as-deposited one is better than w/ PDA one. The frequency dispersion $\triangle C$ of w/ PDA one is 11.2%, which is presented in **Table. 2.1.**.

But the effect of post deposition annealing is no obvious trend, so we resort to adopt another post-deposition thermal process --- forming gas annealing.

2.3.2 The Effect of Forming Gas Annealing on Electrical Characteristics

We applied low temperature 300℃ forming gas annealing in a H_2/N_2 (5%) mixed ambient for 30 minutes to expectably improve the high-*k* dielectric/interface quality of all the capacitors.

First of all, from **Fig. 2.8 (a)(c)**, **Fig. 2.9 (a)(c)**, although w/ FGA one is lower capacitance in the accumulation regime, but higher in the inversion regime than as-deposited one. Also, w/ FGA one exhibits a lower value of depletion capacitance C_{dep} in the depletion regime than as-deposited one, which reveals a smaller value of interface trap capacitance C_{it}, in another word, the gate control of w/ FGA one is better than as-deposited one. And then, from **Fig. 2.10 (a)(c)**, the presence of conductance signal at high frequency with negative V_g of w/ FGA one is much faster than that of w/ PDA one, and we suppose the contours shows that there is a strong inversion response G_{inv}. In other words, the larger response of G_{inv} accompanying with

quicker transition of conductance for w/ FGA one also implies that w/ FGA one has better gate control which is consistent with aforementioned one. The frequency dispersion $\triangle C$ of w/ FGA one (5.92%) is weaker than as-deposited one (8.05%), is shown in **Table. 2.1**., which may reveal the lower number of border traps for w/ FGA one.

Moreover, from **Fig. 2.11 (a)(c)**, **Fig. 2.12 (a)(c)**, w/ FGA one is lower capacitance in the accumulation regime, but about the same in the inversion regime. And, w/ FGA one shows a lower value of depletion capacitance C_{dep} in the depletion regime than as-deposited one, which reveals a smaller value of interface trap capacitance C_{it}, that is to say, the gate control of w/ FGA one is better than as-deposited one. After that, from **Fig. 2.13 (a)(c)**, the conductance at high frequency with negative V_g of w/ FGA one is smaller than that of as-deposited one, and we previously suppose the contours shows that there is interface trap response (G_{it}) with G_{inv}. So, the response of G_{inv} accompanying with G_{it} of w/ FGA one is smaller than that of as-deposited one, even the larger response of minority carrier accompanying with quicker transition of conductance for w/ FGA one also implies that w/ FGA one has better gate control which is consistent with aforementioned one. The frequency dispersion $\triangle C$ of w/ FGA one (14.2%) is weaker than as-deposited one (16.2%), is shown in **Table. 2.1**, which may reveal the lower number of border traps for w/ FGA one.

Besides, from **Fig. 2.14 (a)(c)**, w/ FGA one is still lower capacitance in the accumulation regime, but about the same in the inversion regime. As well w/ FGA one shows a lower value of depletion capacitance C_{dep} in the depletion regime than as-deposited one, which reveals a smaller value of interface trap capacitance C_{it}, in other words, the gate control of w/ FGA one is better than as-deposited one. The frequency dispersion $\triangle C$ of w/ FGA one is 8.89%, which is presented in **Table. 2.1**.

Overall, the effect of forming gas annealing may improve the performance in reducing the interface traps density and the number of border traps. The exact influence on the capacitor performances is examined later.

2.3.3 The Effect of PDA+FGA on Electrical Characteristics

Then we combine the two post-deposition thermal processes, post deposition annealing (400℃/120s) and forming gas annealing (300℃/30min.). From **Fig. 2.8(b)(d)**, **Fig. 2.9 (b)(d)**, it is observed that w/ PDA+FGA one is lower capacitance in the accumulation region, but higher in the inversion region than w/ PDA one. Also, w/ PDA+FGA one exhibits a lower value of depletion capacitance C_{dep} in the depletion region and smaller stretch-out curve than w/ PDA one, which reveals a smaller value of interface trap capacitance C_{it}, that is to say, the gate control of w/ PDA+FGA one is better than w/ PDA one. And then, from **Fig. 2.10 (b)(d)**, the presence of conductance signal at high frequency with negative V_g of w/ PDA+FGA one is much faster than that of w/ PDA one, and we suppose the contours shows that there is a strong minority carrier response. In another word, the larger response of minority carrier accompanying with quicker transition of conductance for w/ PDA+FGA one also implies that w/ PDA+FGA one has better gate control which is consistent with aforementioned one. The frequency dispersion $\triangle C$ of w/ PDA+FGA one (6.55%) is weaker than w/ PDA one (8.70%), is shown in **Table. 2.1**, which may exhibit the lower number of border traps for w/ PDA+FGA one.

In addition, from **Fig. 2.11 (b)(d)**, **Fig. 2.12 (b)(d)**, comparing w/ PDA+FGA one with w/ PDA one, is about the same capacitance in the accumulation area as well as in the inversion area. But, w/ PDA+FGA one still displays a lower value of depletion capacitance C_{dep} and smaller stretch-out curve in the depletion area than w/

PDA one, which reveals a smaller value of interface trap capacitance C_{it}, in other words, the gate control of w/ PDA+FGA one is better than w/ PDA one. And then, from **Fig. 2.13 (b)(d)**, the conductance at high frequency with highly negative V_g of w/ PDA+FGA one is approximately the same as that of w/ PDA one, and we can suppose the contours shows that the minority carrier response of w/ PDA+FGA one is around the same as that of w/ PDA one. However, quicker transition of conductance for w/ PDA+FGA one implies that w/ PDA+FGA one has better gate control which is consistent with aforementioned one. The frequency dispersion △C of w/ PDA+FGA one (9.80%) is weaker than w/ PDA one (10.3%), is shown in **Table. 2.1**., which may reveal the lower number of border traps for w/ PDA+FGA one, too.

Furthermore, from **Fig. 2.14 (b)(d)**, **Fig. 2.15 (b)(d),** w/ PDA+FGA one is still lower capacitance in the accumulation regime, but about the same in the inversion regime. Nevertheless, w/ PDA+FGA one shows a lower value of depletion capacitance C_{dep} and smaller stretch-out curve in the depletion regime than w/ PDA one, which reveals a smaller value of interface trap capacitance C_{it} as well, in other words, the gate control of w/ PDA+FGA one is better than w/ PDA one. Finally, from **Fig. 2.16 (b)(d)**, the conductance at high frequency with highly negative V_g of w/ PDA+FGA one is approximately the same as that of w/ PDA one, and we still suppose the contours shows that the G_{inv} response of w/ PDA+FGA one is around the same as that of w/ PDA one. However, quicker transition of conductance for w/ PDA+FGA one implies that w/ PDA+FGA one has better gate control which is consistent with aforementioned one. The frequency dispersion △C of w/ PDA+FGA one (10.5%) is weaker than w/ PDA one (11.2%), is shown in **Table. 2.1**, which may show the lower number of border traps for w/ PDA+FGA one, too.

In conclusion, we can resolve the effect of forming gas annealing on the electrical properties of all the capacitors, however, the influence of post deposition

annealing is comparatively unapparent. In order to acquire quantitative definition of border traps density, we resort to a distributed bulk-oxide traps model [17], [18], which is introduced in **Chapter 4**.

2.4 Comparison of Different High-κ Dielectrics on Electreical Characteristics

From **Fig. 2.17 (a)~(c)**, to compare with the introduced high-κ dielectrics, after forming gas annealing, TMA/Al_2O_3 has the weakest frequency dispersion in accumulation, depletion, and inversion regions, however, the low κ value brings about the lowest C_{max}. Although TEMAH/HfO_2 has the highest C_{max} and good ability of gate conrtrol due to its high κ value, the frequency dispersion in accumulation, depletion, and inversion regimes is the strongest. As shown in **Table. 2.2**, TMA/ HfO_2 is the optimum dielectric for our MOS device due to its not only high C_{max} and good ability of gate conrtrol due to its high κ value, but weak frequency dispersion in accumulation, depletion, and inversion bias condition.

2.5 Summary

The effect of post-deposition annealing in the condition of 400℃/120s is not clear. But forming gas annealing (300℃/30min.) is a key process to effective reduce frequency dispersion in strong accumulation and depletion regions and improve the interface quality for all the capacitors.

Overall, TMA/ HfO_2 gate dielectric owns the optimumly electrical characteristics because of its high C_{max} and weak frequency dispersion in accumulation, depletion, and inversion regimes.

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- ***Wafer preparation***

  - n(100)InAs

- ***Wafer clean***

  - acetone (5min.)

  - isopropanol (5min.)

  - HCl:H_2O=1:10 (2min.)

- ***TMA 10cyc. pretreatment***
- ***Al_2O_3 100cyc. deposited by ALD system (250˚C dep.)***
- ***PDA (400˚C/120s)***
- ***Gate electrode formation (Ti/Pt)***
- ***Backside-contact deposition (Au/Ge/Ni)***
- ***FGA (300˚C/30min.)***

Fig. 2.1 The process flow of the capacitors with different post-deposition thermal treatments.

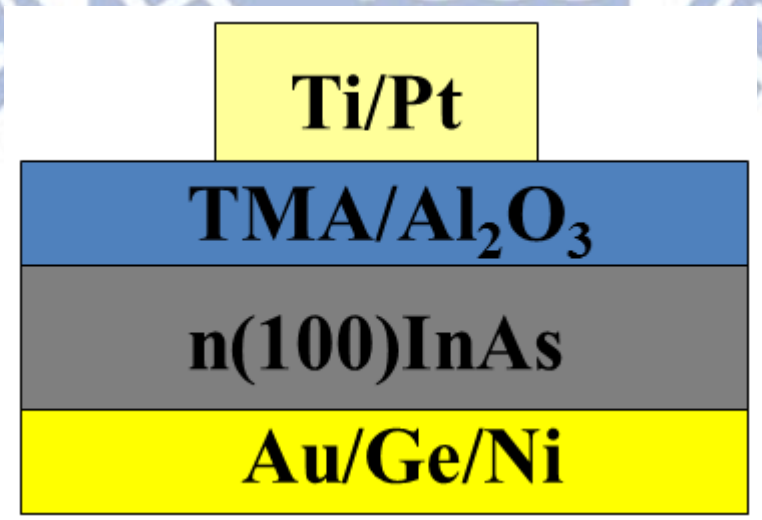


Fig. 2.2 The device structure with ALD-TMA/Al_2O_3.

- ***Wafer preparation***

  - n(100)InAs

- ***Wafer clean***

  - acetone (5min.)

  - isopropanol (5min.)

  - HCl:H_2O=1:10 (2min.)

- ***TEMAH 10cyc. pretreatment***
- ***HfO_2 100cyc. deposited by ALD system (250˚C dep.)***
- ***PDA (400˚C/120s)***
- ***Gate electrode formation (Ti/Pt)***
- ***Backside-contact deposition (Au/Ge/Ni)***
- ***FGA (300˚C/30min.)***

Fig. 2.3 The process flow of the capacitors with different post-deposition thermal treatments.

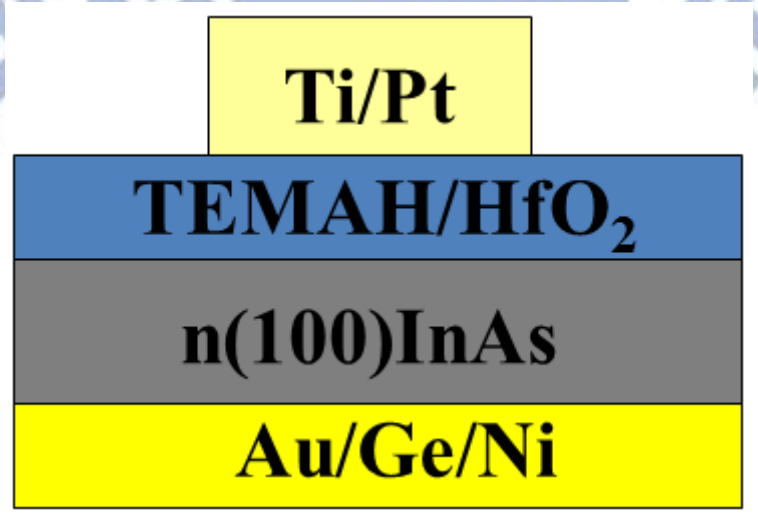


Fig. 2.4 The device structure with ALD-TEMAH/HfO_2.

- ***Wafer preparation***

  - n(100)InAs

- ***Wafer clean***

  - acetone (5min.)

  - isopropanol (5min.)

  - HCl:H_2O=1:10 (2min.)

- ***TMA 10cyc. pretreatment***
- ***HfO_2 100cyc. deposited by ALD system (250˚C dep.)***
- ***PDA (400˚C/120s)***
- ***Gate electrode formation (Ti/Pt)***
- ***Backside-contact deposition (Au/Ge/Ni)***
- ***FGA (300˚C/30min.)***

Fig. 2.5 The process flow of the capacitors with different post-deposition thermal treatments.

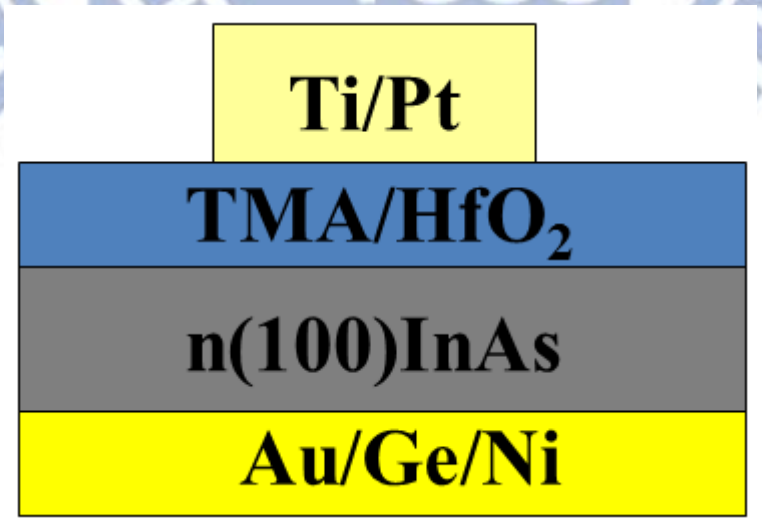
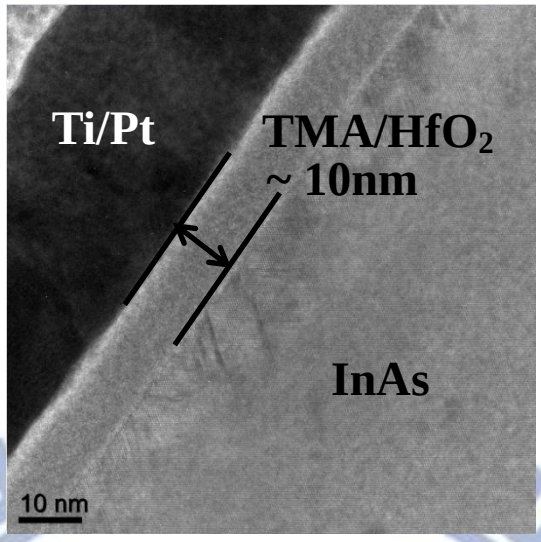
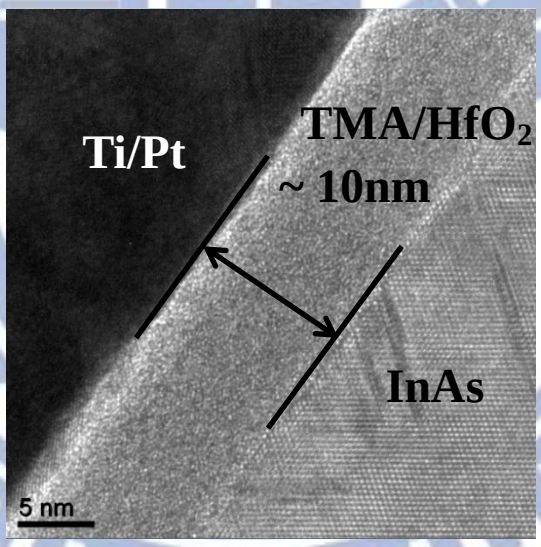


Fig. 2.6 The device structure with ALD-TMA/HfO_2.



(a)



(b)

Fig. 2.7 (a)(b) Cross-sectional TEM images of as-deposited Pt/Ti/TMA+HfO_2/n-InAs gate stack.

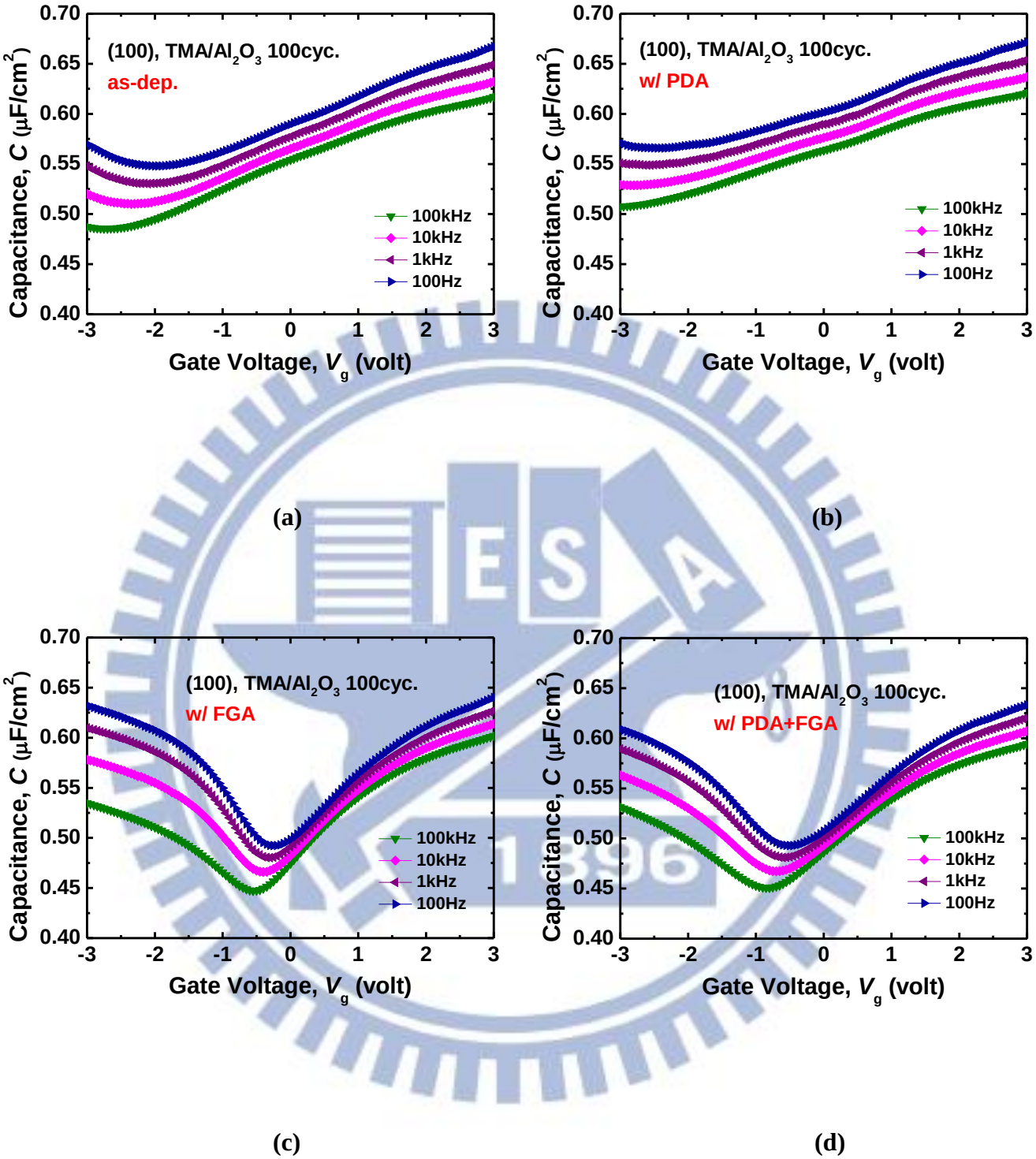


Fig. 2.8 Multi-frequency *C-V* curves of Pt/Ti/TMA+Al_2O_3/n-InAs capacitors measured in 100Hz, 1kHz, 10kHz, and 100kHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

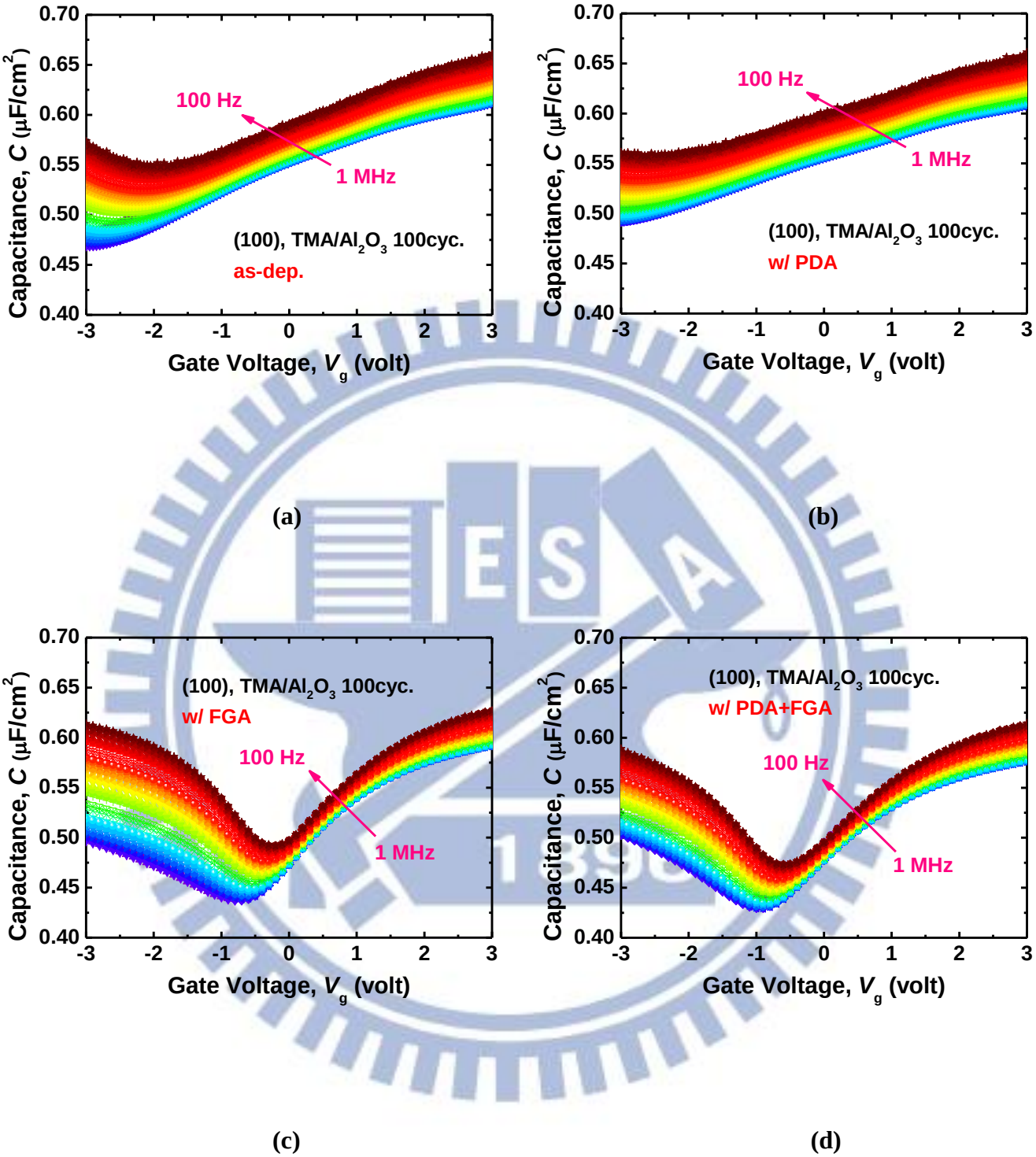


Fig. 2.9 Multi-frequency *C-V* maps of Pt/Ti/TMA+Al_2O_3/n-InAs capacitors measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

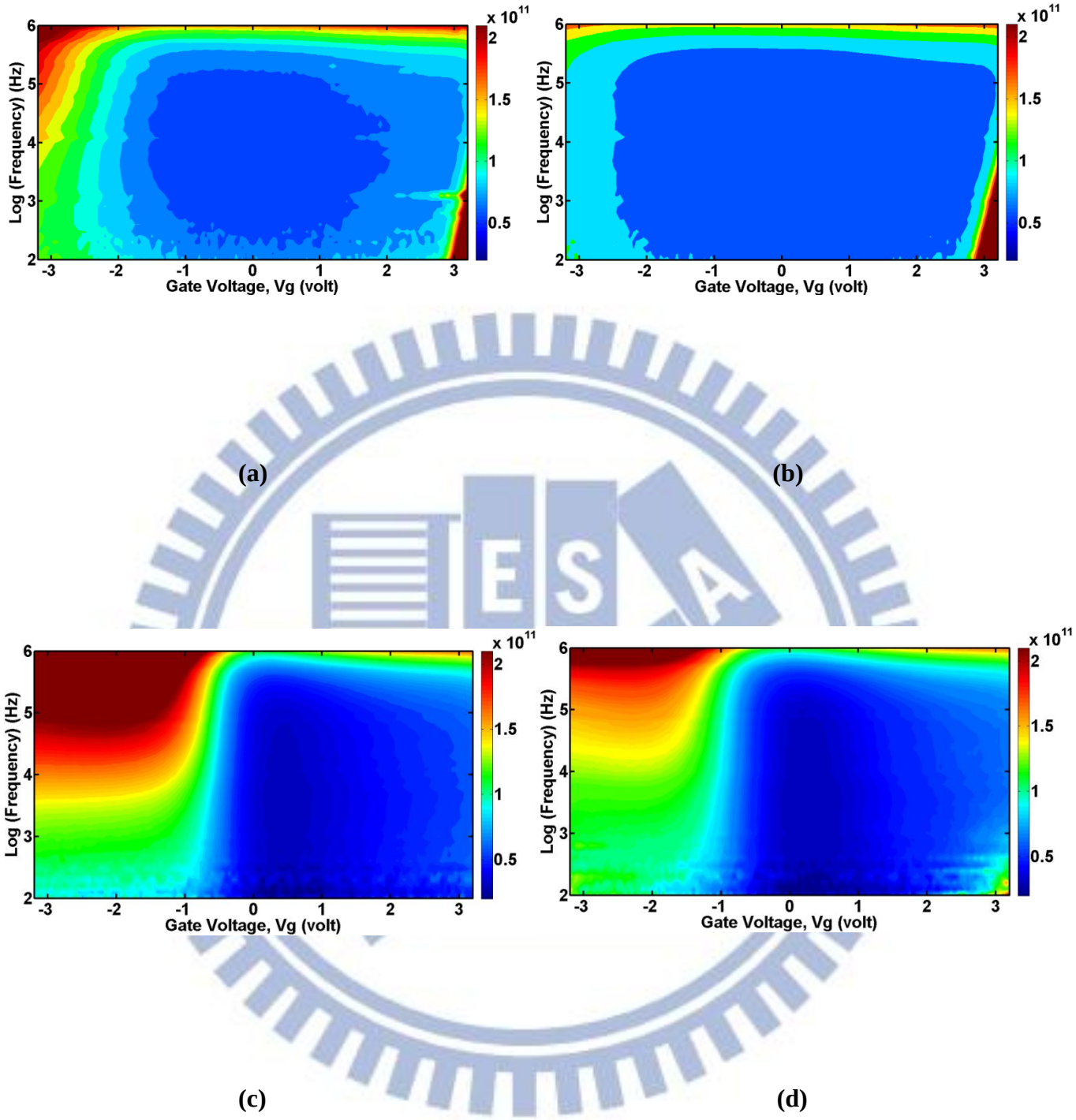


Fig. 2.10 *G/Aq₀ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of Pt/Ti/TMA+Al_2O_3/n-InAs capacitors measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

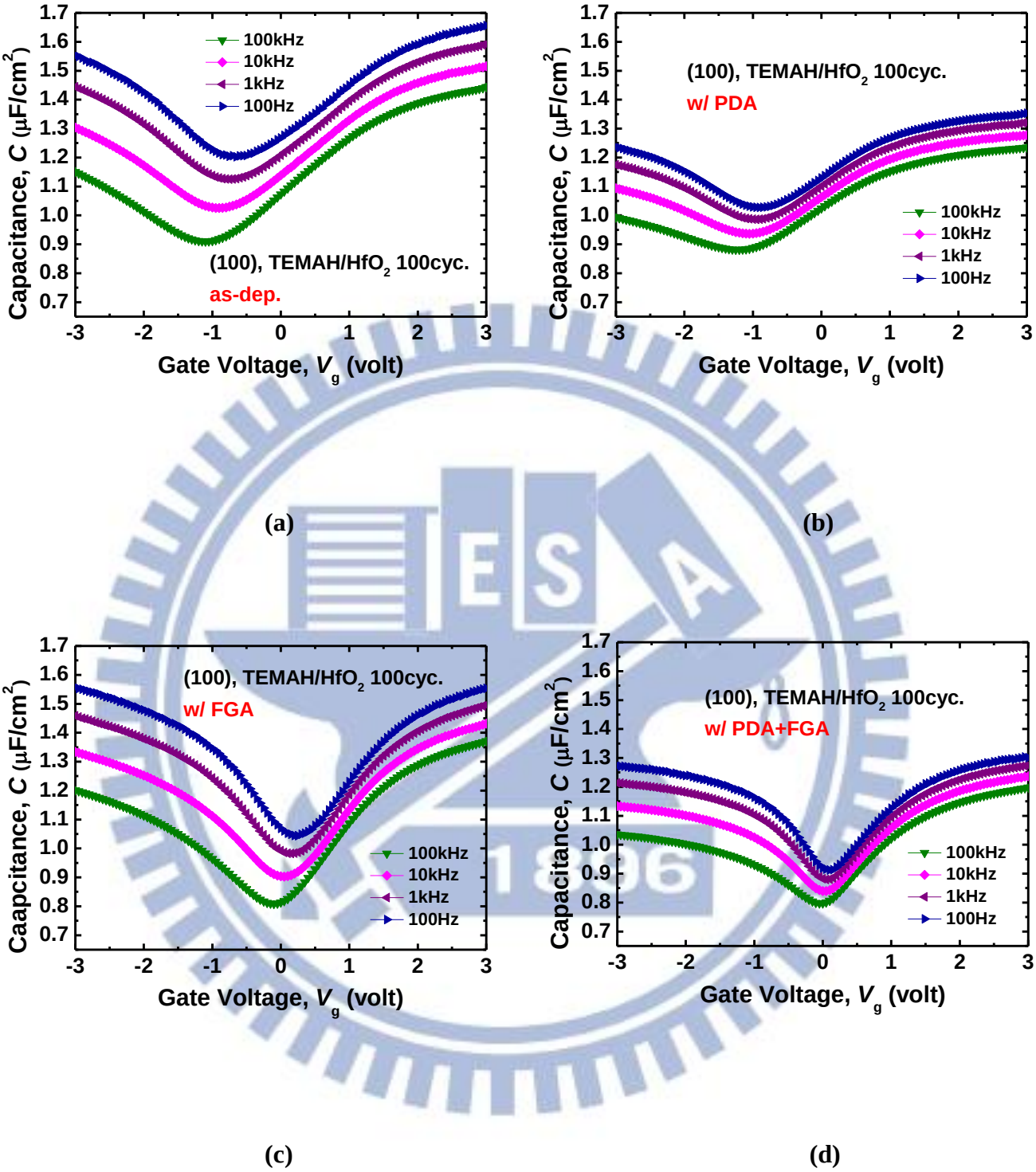


Fig. 2.11 Multi-frequency *C-V* curves of Pt/Ti/TEMAH+HfO_2/n-InAs capacitors measured in 100Hz, 1kHz, 10kHz, and 100kHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

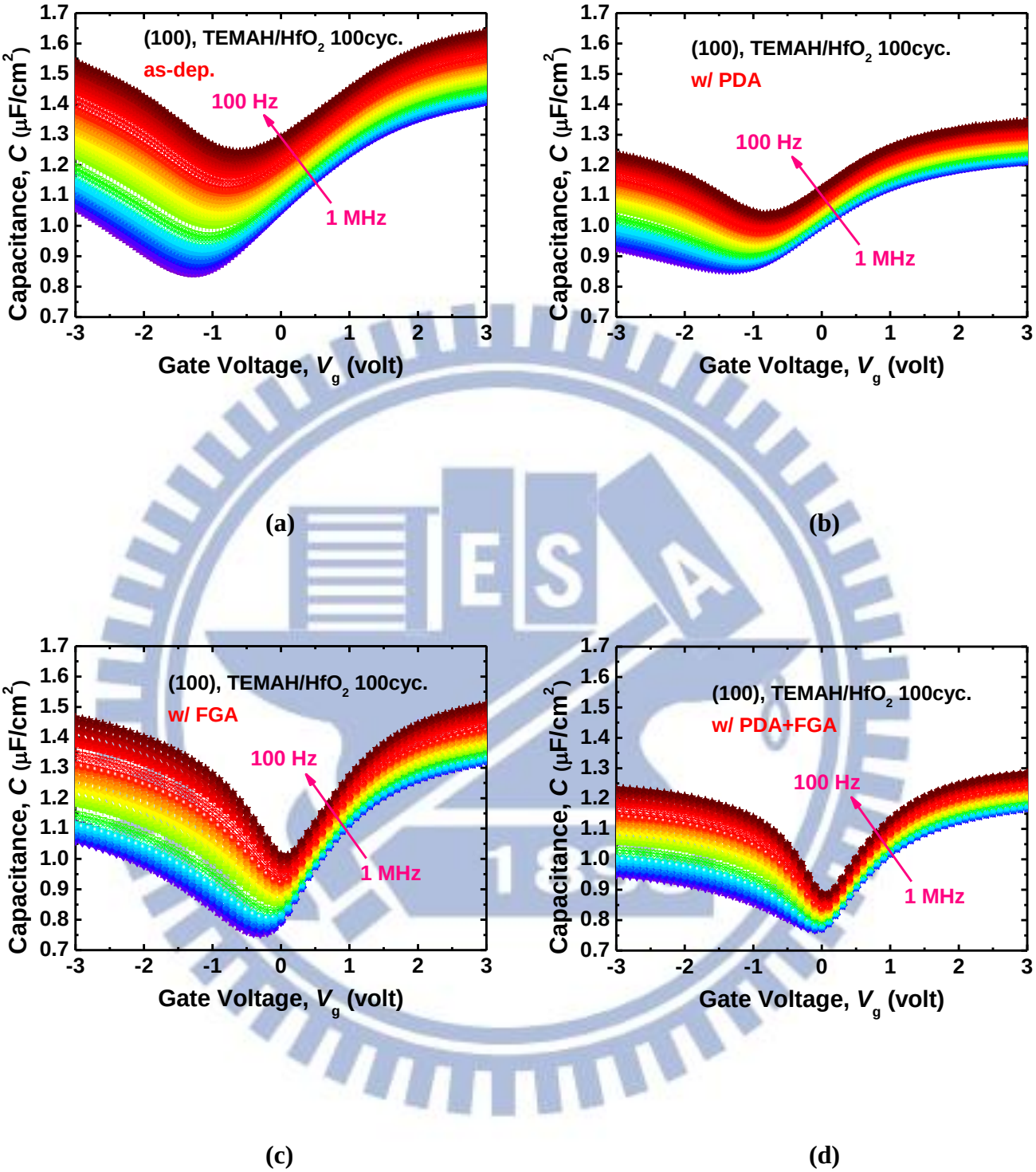


Fig. 2.12 Multi-frequency *C-V* maps of Pt/Ti/TEMAH+HfO_2/n-InAs capacitors measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

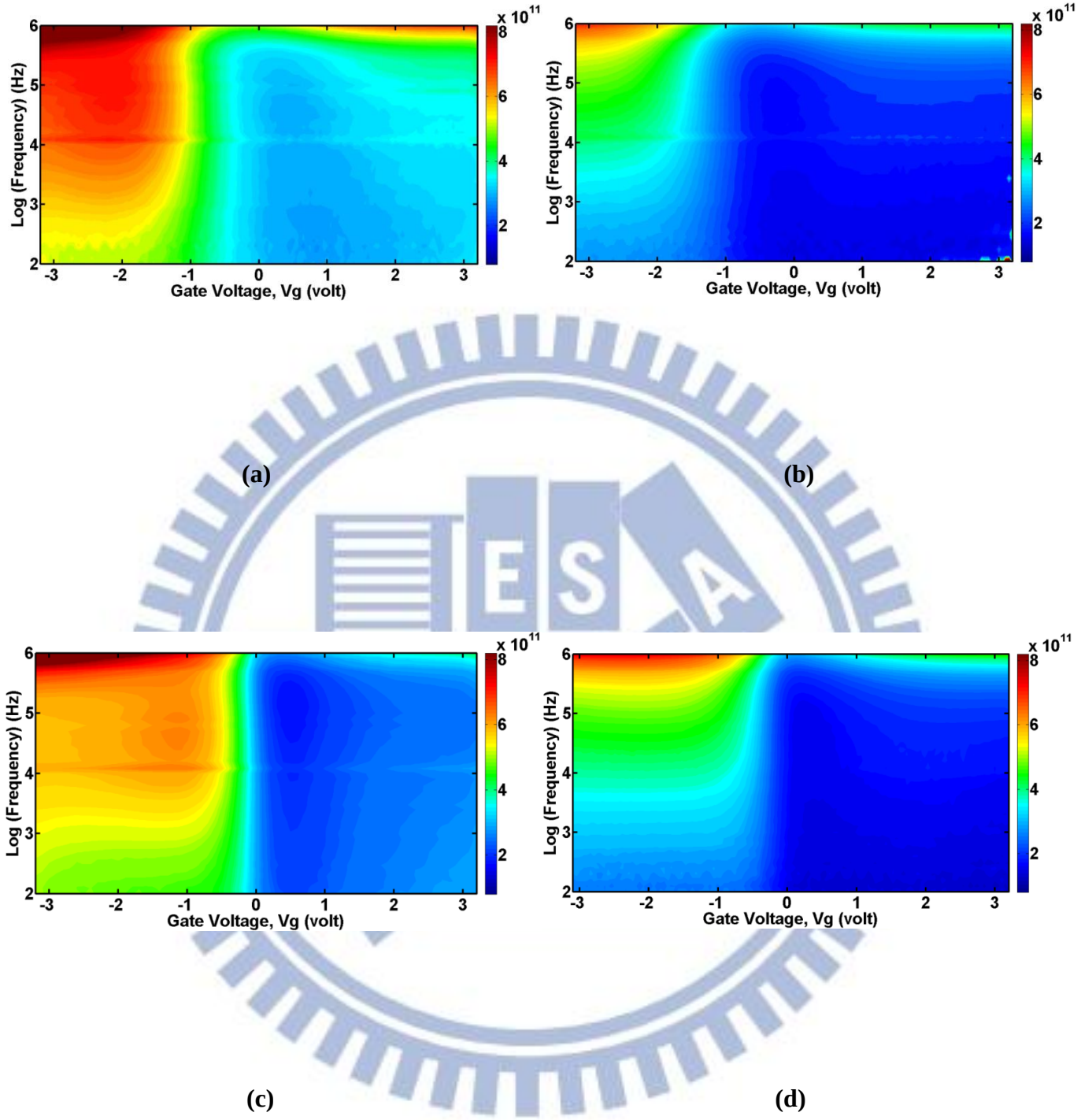


Fig. 2.13 *G/Aq₀ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of Pt/Ti/TEMAH+HfO_2/n-InAs capacitors measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

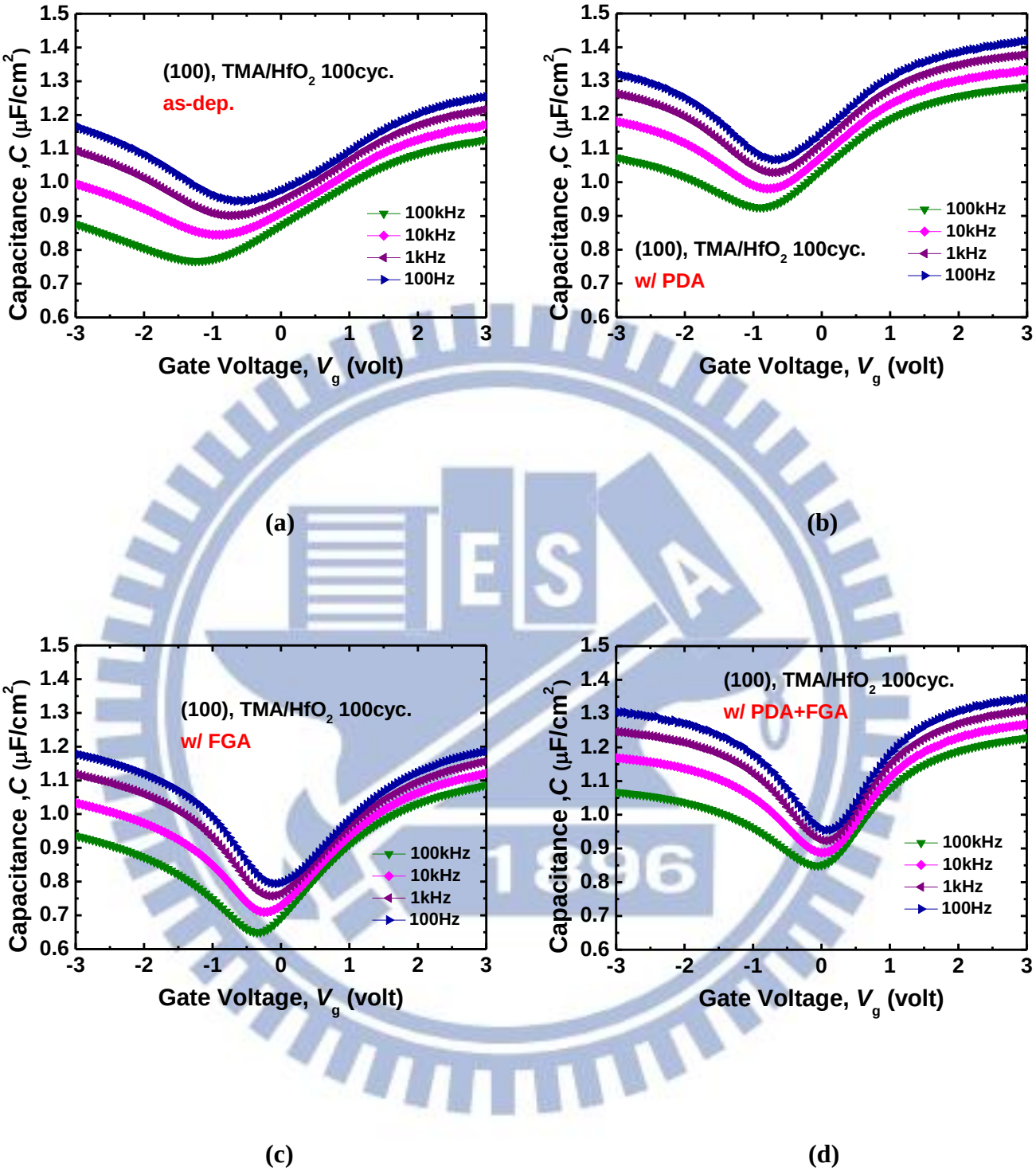


Fig. 2.14 Multi-frequency *C-V* curves of Pt/Ti/TMA+HfO_2/n-InAs capacitors measured in 100Hz, 1kHz, 10kHz, and 100kHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

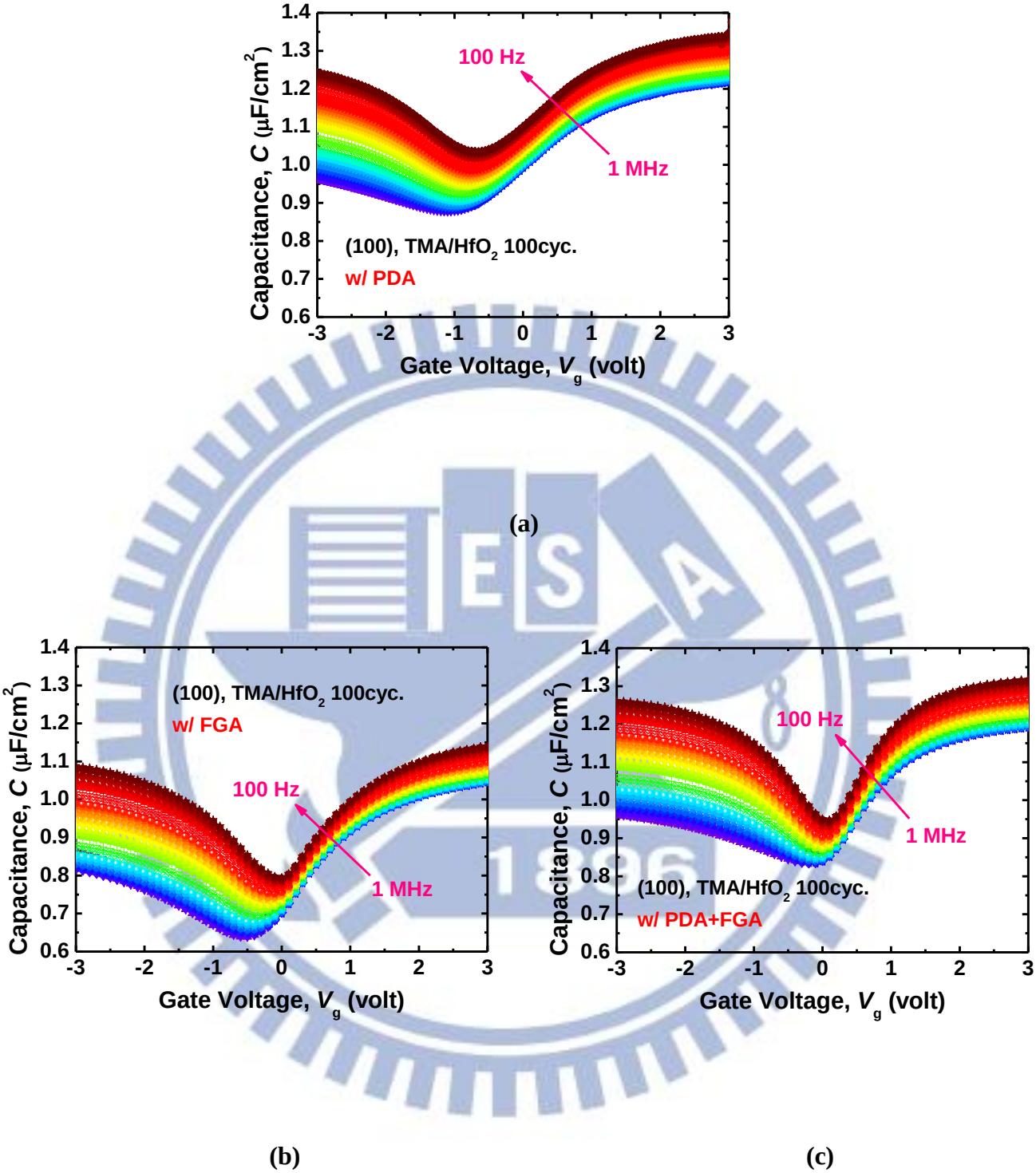


Fig. 2.15 Multi-frequency *C-V* maps of Pt/Ti/TMA+HfO_2/n-InAs capacitors measured in 100Hz to 1MHz, at the temperature of 300K: (a) w/ PDA; (b) w/ FGA; (c) w/ PDA+FGA.

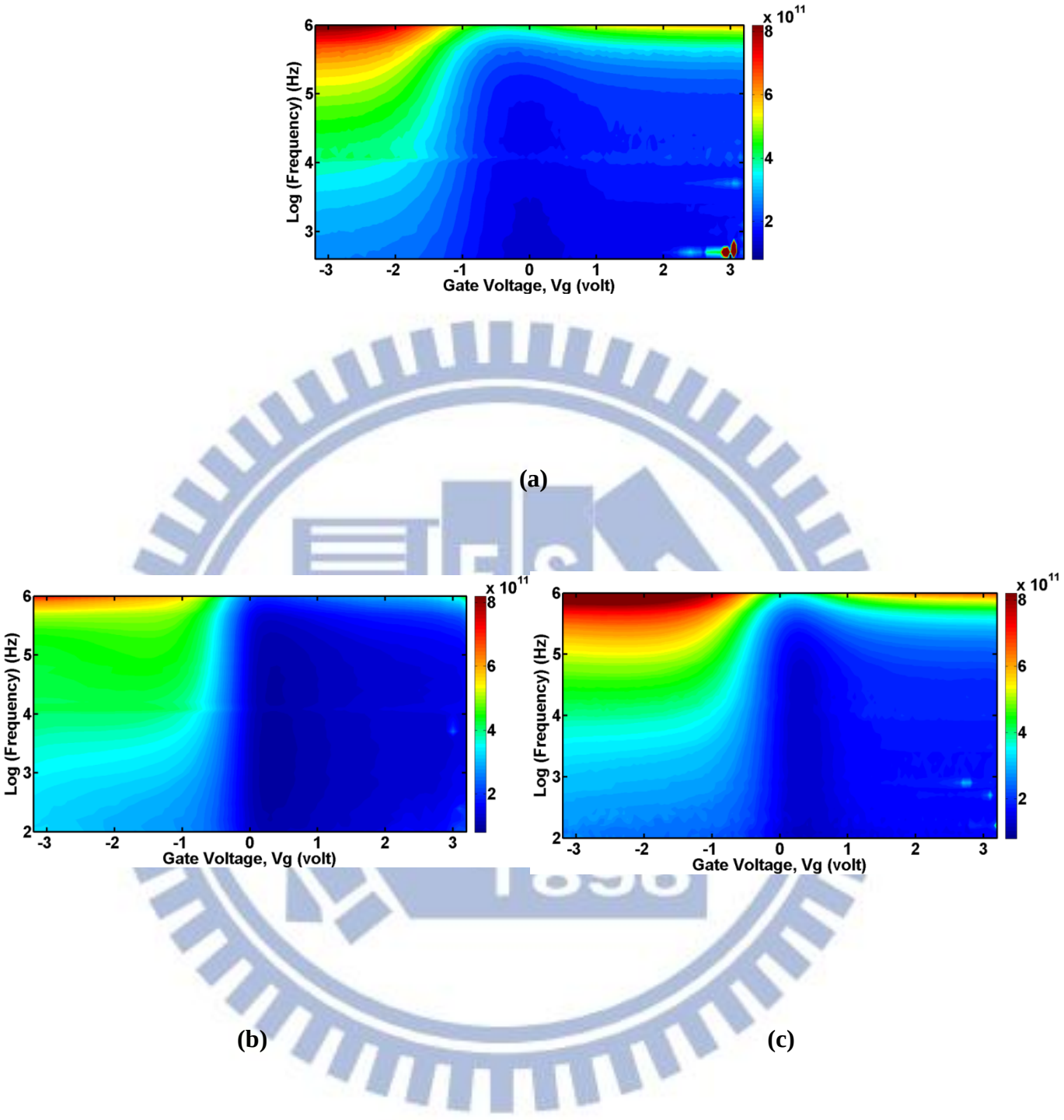


Fig. 2.16 *G/Aq$_0$ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of Pt/Ti/TMA+HfO_2/n-InAs capacitors measured in 100Hz to 1MHz, at the temperature of 300K: (a) w/ PDA; (b) w/ FGA; (c) w/ PDA+FGA.

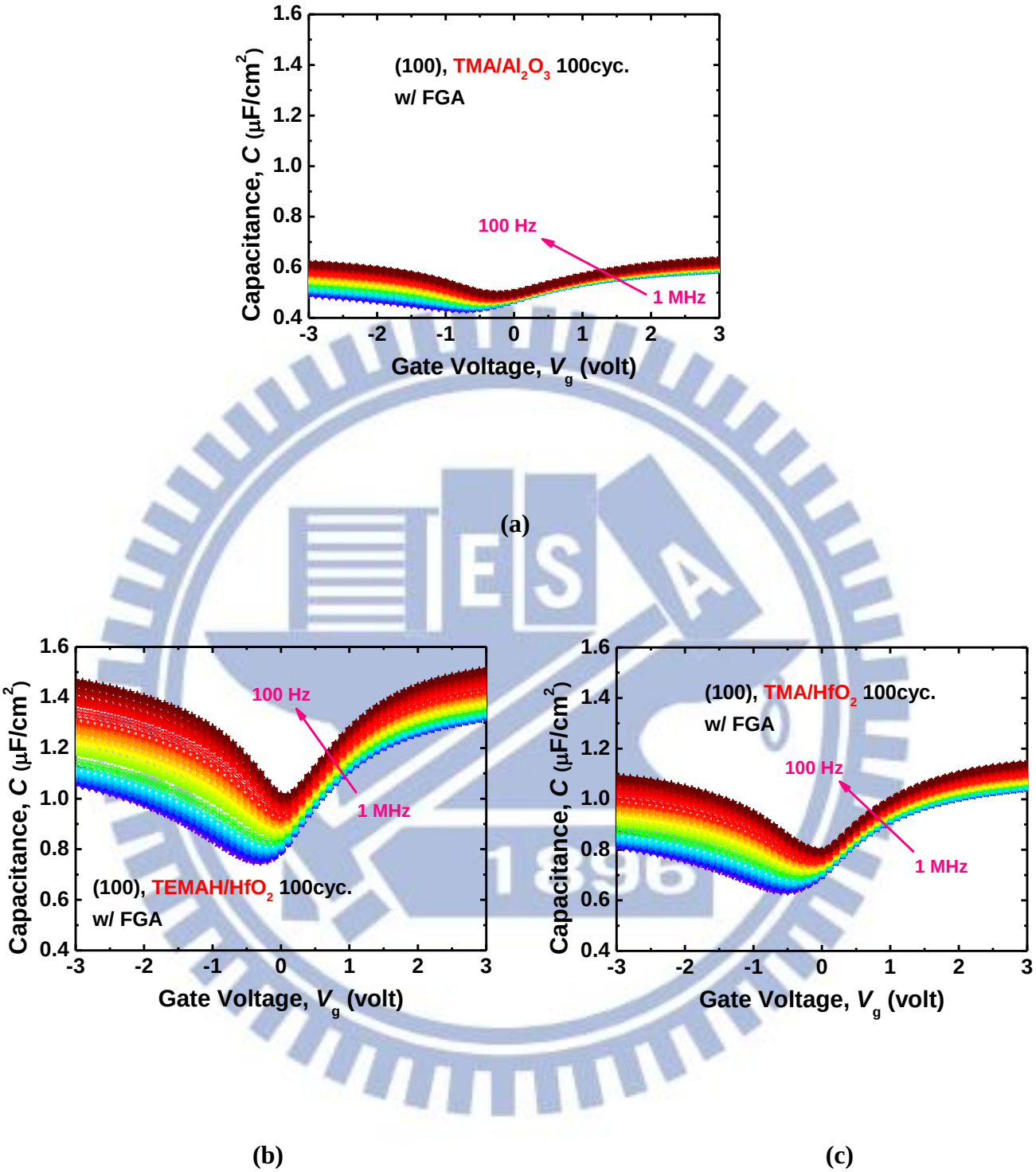


Fig. 2.17 Multi-frequency *C*-*V* maps of different MOS capacitors w/ FGA measured in 100Hz to 1MHz, at the temperature of 300K: (a) TMA/Al_2O_3; (b) $TEMAH/HfO_2$; (c) TMA/HfO_2.

	As-dep.	w/ PDA	w/ FGA	w/ PDA+FGA
TMA/Al_2O_3	8.05 %	8.70 %	5.92 %	6.55 %
$TEMAH/HfO_2$	16.2 %	10.3 %	14.2 %	9.80 %
TMA/HfO_2		11.2 %	8.89 %	10.5 %

Table 2.1 The overview of all of the capacitors in frequency dispersion ΔC(@V_g = 3V) are compared.

	$C_{max}(\mu F/cm^2)$	Freq-disp.(ΔC)
TMA/Al_2O_3	low	weak
$TEMAH/HfO_2$	high	strong
TMA/HfO_2	high	weak

Table 2.2 The overview of all of the capacitors in comparison with C_{max} and frequency dispersion ΔC are compared.

Chapter 3

InAs MOSCAPs with TMA/HfO_2 High-κ Dielectrics by Various O_2-plasma Treatments during Atomic-Layer-Deposition (ALD) Process

3.1 Introduction

High-*k* materials have been researched as the alternative gate dielectrics to replace conventional SiO_2 in the scaled Si-based device technological generation on account of the exccesive leakage current and degraded reliability [1-5]. HfO_2 is a potential gate dielectric for its high dielectric constant (*k* ~ 25), a relatively wide bandgap (E_g ~ 5.7eV), and good thermal stability in contacting with Si and related materials. In ultrathin regime, for capacitance equivalent thickness (CET), HfO_2 has been demonstrated to be compatible with poly-SiGe and TaN gate materials so on [6].

Lately, using NH_3 to thermally nitrogenize of Si-based material prior to the atomic-layer-deposition (ALD) of high-*k* dielectric has been introduced to be effectual in accomplishing low CET and fine reaction barrier between HfO_2 and Si-based material [6, 7]. Lai *et al.* demonstrated the interfacial layer properties of thin Ta_2O_3 films on bare, NH_3, and N_2O nitrided Si substrates [8]. Incorporating nitrogen in the interfacial layer utilizing N_2O is a promising way to be gate dielectric for scaled-Si MOSFET device techniques as a result of its excellent electrical characteristic and improved reliability compared to the conventional SiO_2 film [9]. Also, Kim *et al.* reported that nitridated Ge thermally, which formed a germanium oxynitride (GeON)

layer, is an efficacious passivation on Ge surface prior to atomic-layer-deposition (ALD) of HfO_2 high-*k* dielectric [10]. The results revealed that incorporating nitrogen into germanium oxides effectually repress inter-diffusion of components across high-*k* dielectric/substrate interface during atomic-layer-deposition (ALD) and post-deposition thermal processes [11]. Neverthless, the thermal instability of gemanium oxide limits the process window for the nitridation method of Ge substrate [12]. Moreover, nitridation and PH_3 passivation with thermal or plasma process had been utilized in IV-group materials to improve high-*k* dielectric/substrate interface quality [13].

Up to date, plasma nitridation process is a promising technique to form silicon oxynitride (SiON) as gate dielectric films. The particular characteristic of the process is the marvelous control of the nitrogen concentration and profile at low temperature of substrate ($< 400^{\circ}C$) [14,15]. On the other hand, plasma nitridation process and PH_3 passivation also had been applied to GaAs MOS structures [16, 17]. But, the effect of any plasma treatment process on the III-Vs surface is not been sufficiently studied.

In this chapter, we report for the first time, in combination with the aforementioned trimethyl aluminum [TMA, $Al(CH_3)_3$] precursor pre-deposition treatment and O_2-plasma treatment during atomic-layer-deposition (ALD) thin HfO_2 high-*k* dielectric films process displays a manifestly improvement of electrical properties for InAs MOSCAPs.

3.2 Experimental Procedures of Pt/Ti/TMA+HfO_2/n-InAs w/ or w/o O_2-Plasma Treatment

As same as the chapter 2 we mentioned, (100)-oriented n-InAs substrates are prepared with doping concentration of ca. 1x 10^{17} cm^{-3} (resistivity ca. 0.002Ω·cm). Before gate dielectric formation, all of the wafers were pre-cleaned by acetone (ACE), isopropanol (IPA), and dilute HCl (1:10) for 5, 5, 2 min., respectively, to remove the native oxide, the treated wafers were loaded into ALD chamber. *In situ* trimethyl aluminum [TMA, $Al(CH_3)_3$] precursor pre-deposition treatment was done by using 10cycles of TMA/N_2 with a period of 0.06s for a TMA pulse and 10s for a N_2 pulse. After that, the HfO_2 thin film (TEMAH/N_2/H_2O/N_2 with durations of 0.1/10/0.04/10 s) was grown over 60cycles (which is not same as the previous condition in order to obtain lower EOT for future device) on the bulk InAs at substrate temperature of 250℃. The wafers were kept at the temperature of 250℃ during both precursor pretreatment and dielectric deposition process. Tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf(N(C_2H_5)(CH_3))_4$]] and H_2O were selected as the Hf metal source and oxidant, respectively. High-purity N_2 was applied as a purging gas to remove redundant reactants. As depositing thin HfO_2 film in combination with various O_2-plasma treatments are investigated in this chapter, which are per 2, 4, 8cycles once 20sec. O_2-plasma, and post-deposition O_2-plasma treatment (duration of 10min.), and the power of O_2-plasma is 300W. The thickness of the HfO_2 film estimated from the number of the growth cycles, is approximate 5nm. Then, 50/500 Å Ti/Pt was deposited using sputter system to pattern gate electrode by shadow mask, and then a 500/700/300-Å -thick Au/Ge/Ni layer was deposited as the backside ohmic contact.

Two post-deposition thermal process were similarly examined: (i) post deposition annealing (PDA) by rapid thermal annealing (RTA) at 400℃ in a N_2 ambient for 120s and (ii) forming gas annealing (FGA) at 300℃ in a H_2/N_2 (5%)

mixed ambient for 30 min.. Optical microscopy exhibited that the gate electrode area of the capacitor was ca. 4×10^{-4} cm^2.

The process flow and device structure are displayed in **Fig. 3.1, Fig. 3.2**.

3.3 Capacitor Characteristics of InAs nMOSCAPs with Various O_2-Plasma Treatments via Different Post-Deposition Thermal Process

The capacitance-voltage and conductance-voltage characteristics of all the capacitors were still measured by using HP4284A *LCR* meter at the temperature of 300K. **Fig. 3.3** displays the multi-frequency *C-V* properties, **Fig. 3.4** presents the multi-frequency *C-V* maps, and **Fig. 3.5** shows the $G/Aq_0\omega$-*V* contours, of w/o O_2-plasma treated capacitors, w/o or w/ PDA (400℃/120s) and before or after FGA (300℃/30min.), respectively. Similarly, **Fig. 3.6**, **Fig. 3.7**, **Fig. 3.8** exhibit the multi-frequency *C-V* properties, the multi-frequency *C-V* maps, and the $G/Aq_0\omega$-*V* contours, of 2cyc./plasma treated capacitors, w/o or w/ PDA (400℃/120s) and before or after FGA (300℃/30min.), respectively; **Fig. 3.9**, **Fig. 3.10**, **Fig. 3.11** present the multi-frequency *C-V* properties, the multi-frequency *C-V* maps, and the $G/Aq_0\omega$-*V* contours, of 4cyc./plasma treated capacitors, w/o or w/ PDA (400℃/120s) and before or after FGA (300℃/30min.), respectively; **Fig. 3.12**, **Fig. 3.13**, **Fig. 3.14** demonstrate the multi-frequency *C-V* properties, the multi-frequency *C-V* maps, and the $G/Aq_0\omega$-*V* contours, of 8cyc./plasma treated capacitors, w/o or w/ PDA (400℃/120s) and before or after FGA (300℃/30min.), respectively; and finally, **Fig. 3.15**, **Fig. 3.16**, **Fig. 3.17** illustrate the multi-frequency *C-V* properties, the multi-frequency *C-V* maps, and the

G/Aq$_0$ω-V contours, of post-deposition O_2-plasma treated capacitors, w/o or w/ PDA (400℃/120s) and before or after FGA (300℃/30min.), respectively.

As well as we qualitatively define one of the capacitor characteristics through the frequency dispersion ΔC as follows:

$\Delta C(@V_g = V_{max}) = \{[C_{acc}(@100Hz) - C_{acc}(@1MHz)] / C_{acc}(@1MHz)\} \times 100\%$ (3.1)

Where $\Delta C(@V_g = 1.3V)$ is for w/o O_2-plasma treatment, $\Delta C(@V_g = 2V)$ is for 2, 4, 8cyc./plasma treatment, and $\Delta C(@V_g = 1.5V)$ is for post-deposition O_2-plasma treatment. The overview of all of the capacitors in frequency dispersion is shown in **Table. 3.1 – Table. 3.3**.

3.3.1 *C-V* and *G-V* properties of InAs nMOSCAPs w/ PDA

In the beginning, we desire to infer the effect of adopting post deposition annealing. From **Fig. 3.3 (a)(b)**, for w/o O_2-plasma treatment, comparing the as-deposited one with w/ PDA one, we find that the capacitance characteristics of w/ PDA one is unapparent, which is mainly due to large gate leak. So, we deduce that there is a critical problem of performing post deposition annealing at 400℃/120s. Then, from **Fig. 3.5 (b)**, the conductance at low frequency with highly positive and negative V_g of as-deposited one is large. We suppose that the high conductance signal at low frequency with highly positive V_g is due to a huge number of border traps in the high-*k* dielectrics, and one with highly positive V_g is owing to a high distribution of interface traps. The frequency dispersion ΔC of as-deposited one is 8.42%, is shown in **Table. 3.1**.

Moreover, from **Fig. 3.6 (a)(b)**, **Fig. 3.7 (a)(b)**, for 2cyc./plasma treatment, contrasting the as-deposited one with to w/ PDA one, we observe that the accumulation and inversion capacitance of as-deposited one at $V_g = 2V$ is much larger

than that of w/ PDA one, but the minimum of capacitance C_{min} of the as-deposited one is lower than w/ PDA one, that is to say, the gate control of the as-deposited one is much better than that of w/ PDA one. And from **Fig. 3.8 (a)(b)**, the conductance at low frequency with highly positive and negative V_g of as-deposited one is larger than that of w/ PDA one, and we conclude the contours map displays that there are a stronger interface trap response G_{it} and border traps response G_{bor} for as-deposited one than w/ PDA one. We also note that the minority carrier responses of the two are almost weak. According to the foregoing results, it is probably implied that the higher contribution of interface traps and border traps in as-deposited one than w/ PDA one. However, it should be examined deeply, too. The frequency dispersion $\triangle C$ of as-deposited one (13.2%) is stronger than w/ PDA one (12.7%), is shown in **Table. 3.2**., which is concordant with the aforesaid.

Furthermore, from **Fig. 3.9 (a)(b), Fig. 3.10 (a)(b)**, for 4cyc./plasma treatment, as-deposited one in comparison with w/ PDA one, is slightly higher in the accumulation capacitance but lower in the inversion capacitance. And the minimum of the capacitance C_{min} of as-deposited one is lower than w/ PDA one, which are suggested that the ability of gate control for as-deposited one is greater than w/ PDA one. Then from **Fig. 3.11 (a)(b)**, the conductance at low frequency with highly positive V_g of as-deposited one is larger but lower with negative V_g than w/ PDA one. We conclude the contours map presents that there are a stronger border traps response G_{bor} but weaker interface trap response G_{it} for as-deposited one than w/ PDA one. We still note that the minority carrier responses are nearly weak of the two. The frequency dispersion $\triangle C$ of as-deposited one (15.1%) is weaker than w/ PDA one (16.2%), is shown in **Table. 3.2**., which is a little contradictory with the aforesaid. The contradiction is in account of my rough definition of $\triangle C$.

Besides, from **Fig. 3.12 (a)(b), Fig. 3.13 (a)(b)**, for 8cyc./plasma treatment, to make a contrast between as-deposited one and w/ PDA one, the capacitance in the accumulation region of as-deposited one is higher but lower in the inversion region than w/ PDA one. The minimums of the capacitance C_{min} are just about the same of the two, which are suggested that the ability of gate control for as-deposited one is greater than w/ PDA one. And from **Fig. 3.14 (a)(b)**, the conductance at low frequency with highly positive V_g of as-deposited one is larger but lower with negative V_g than w/ PDA one. We may judge the contours map exhibits that there are a stronger border traps response G_{bor} but weaker interface trap response G_{it} for as-deposited one than w/ PDA one. We notice that the minority carrier responses of as-deposited one is weaker than w/ PDA one. The frequency dispersion ΔC of as-deposited one (17.9%) is weaker than w/ PDA one (19.9%), is shown in **Table. 3.2**., which is still a little contradictory with the foresaid.

Finally, from **Fig. 3.15 (a)(b), Fig. 3.16 (a)(b)**, for post-deposition O_2-plasma treatment, to compare as-deposited one with w/ PDA one, we heed that the capacitance in the accumulation regime of as-deposited one is slightly lower but much lower in the inversion regime than w/ PDA one. The minimums of the capacitance C_{min} for as-deposited one still much lower than w/ PDA one, which are hinted that the ability of gate control for as-deposited one is greater than w/ PDA one. After that, from **Fig. 3.17 (a)(b)**, the conductance at low frequency with highly positive V_g of as-deposited one is lower than w/ PDA one, which we think the contours map demonstrates that there are a weaker border traps response G_{bor} for as-deposited one than w/ PDA one. We observe that the minority carrier responses of as-deposited one is weaker than w/ PDA one. The frequency dispersion ΔC of as-deposited one (16.1%) is stronger than w/ PDA one (15.4%), is shown in **Table. 3.3**., which is still a little contradictory with the foresaid.

We can conclude the effect of post deposition annealing is degrading the ability of gate control apparently, but some samples own better inversion characteristics. So the trend of performing post deposition annealing on our samples is unobvious, then we still proceed to apply another post-deposition thermal process --- forming gas annealing.

3.3.2 The Effect of Forming Gas Annealing on Electrical Characteristics

We applied low temperature 300℃ forming gas annealing in a H_2/N_2 (5%) mixed ambient for 30 minutes to expectably improve the high-*k* dielectric/interface quality of all the capacitors as well.

In the first instance, from **Fig. 3.3 (a)(c)**, **Fig. 3.4 (a)(b)**, w/ FGA one is slightly higher capacitance in the accumulation regime, and higher in the inversion regime than as-deposited one. Also, w/ FGA one exhibits the better gate control than as-deposited one. And then, from **Fig. 3.5 (a)(b)**, the presence of conductance signal at high frequency with negative V_g of w/ FGA one is much faster than that of w/ PDA one, and we suppose the contours shows that there is a stronger minority carrier response. However, at low frequency with highly positive and negative bias, the conductance of w/ FGA one is larger than as-deposited one. So we observe that the capacitance of w/ FGA one at the inversion bias is larger than the as-deposited one. The frequency dispersion $\triangle C$ of w/ FGA one (9.30%) is stronger than as-deposited one (8.42%), is shown in **Table. 3.1**, which may reveal the higher number of border traps for w/ FGA one and **Fig. 3.5 (a)(b)** is also shown to represent it.

Moreover, from **Fig. 3.6 (a)(c)**, **Fig. 3.7 (a)(c), Fig. 3.9 (a)(c)**, **Fig. 3.10 (a)(c), Fig. 3.12 (a)(c)**, **Fig. 3.13 (a)(c),** of 2, 4, 8 cyc./plasma, respectively, w/ FGA one are

similar C_{max} in the accumulation regime and C_{min} in the inversion regime. That is to say, the gate control of w/ FGA one is about the same with as-deposited one. But, we find that the dispersion in the accumulation and depletion regimes of w/ FGA one is weaker than as-deposited one, for the capacitors of the three. After that, from **Fig. 3.8 (a)(c)**, **Fig. 3.11 (a)(c), Fig. 3.14 (a)(c),** the conductance at near zero bias and positive V_g at low frequency of w/ FGA one is smaller than that of as-deposited one, and we suppose the contours shows that the interface traps and oxide traps are reduced, which is consistent with above mentioned phenomenon. The frequency dispersion $\triangle C$ of w/ FGA one (12.8%) for 2cyc./plasma is weaker than as-deposited one (13.2%), is shown in **Table. 3.2**, which may reveal the lower number of border traps for w/ FGA one. The frequency dispersion $\triangle C$ of w/ FGA one (14.3%) for 4cyc./plasma is also weaker than as-deposited one (15.1%), and The frequency dispersion $\triangle C$ of w/ FGA one (15.8%) for 8cyc./plasma is still weaker than as-deposited one (17.9%), are shown in **Table. 3.2** as well.

Besides, from **Fig. 3.15 (a)(c)**, **Fig. 3.16 (a)(c),** w/ FGA one is slightly higher C_{max} in the accumulation regime, but much higher C_{min} in the inversion regime, so the gate control of w/ FGA one is worse than as-deposited one. As well w/ FGA one shows weaker frequency dispersion in both the accumulation and depletion bias than as-deposited one, which reveals the oxide and interface quality are improved. From **Fig. 3.17 (a)(c)**, the conductance in the depletion bias, accumulation and inversion bias at low frequency of w/ FGA one is smaller than as-deposited one. The frequency dispersion $\triangle C$ of w/ FGA one is 14.5% is weaker than which of as-deposited one (16.1%), which is presented in **Table. 3.3**.

In general, the effect of forming gas annealing is improving the capacitors performance in decreasing the frequency dispersion of all samples which is meant the interface traps and border traps density are reduced.

3.3.3 The Effect of PDA+FGA on Electrical Characteristics

Then we still combine the two post-deposition thermal processes, post deposition annealing (400℃/120s) and forming gas annealing (300℃/30min.). From **Fig. 3.3(c)**, **Fig. 3.4 (c)**, it is observed that w/ PDA+FGA one is better in capacitance characteristics than w/ as-deposited one. And then, from **Fig. 3.5 (c)**, the presence of conductance signal at low frequency with positive V_g of w/ PDA+FGA one is larger than that of as-deposited one, and we suppose the contours shows that there is a stronger slow trap response G_{bt}. The frequency dispersion △C of w/ PDA+FGA one is 9.81%, is shown in **Table. 3.1**.

In addition, from **Fig. 3.6 (b)(d)**, **Fig. 3.7 (b)(d)**, **Fig. 3.9 (b)(d)**, **Fig. 3.10 (b)(d), Fig. 3.12 (b)(d)**, **Fig. 3.13 (b)(d),** comparing w/ PDA+FGA one with w/ PDA one, are about the same C_{max} in the accumulation area as well as C_{min} in the inversion area. But, w/ PDA+FGA one displays a better characteristic of inversion. In substance, the gate control of w/ PDA+FGA one is similar with w/ PDA one. The frequency dispersion is of w/ PDA+FGA one in the accumulation and depletion regions still weaker than w/ PDA one. And then, from **Fig. 3.8 (b)(d)**, **Fig. 3.11 (b)(d)**, and **Fig. 3.14 (b)(d)**, the trend of conductance approximately the same as that of w/ FGA one comparing with as-deposited one. The conductance of w/ PDA+FGA one are smaller than w/ PDA one at the bias of both accumulation and depletion. The frequency dispersion △C of w/ PDA+FGA one for 2cyc/plasma (12.1%) is weaker than w/ PDA one (12.7%), the frequency dispersion △C of w/ PDA+FGA one for 4cyc/plasma (16.2%) is weaker than w/ PDA one (14.7%), and the frequency dispersion △C of w/ PDA+FGA one for 4cyc/plasma (17.7%) is weaker than w/ PDA one (19.9%), are shown in **Table. 3.2**.

Furthermore, from **Fig. 3.15 (b)(d)**, **Fig. 3.16 (b)(d),** w/ PDA+FGA one is slightly lower capacitance in the both C_{max} and C_{min}, which indicate that the gate control of w/ PDA+FGA one is similar to w/ PDA one. Nevertheless, w/ PDA+FGA one shows a weaker dispersive curve than w/ PDA one. Finally, from **Fig. 3.17 (b)(d)**, the conductance at high frequency with highly negative V_g of w/ PDA+FGA one is approximately lower than w/ PDA one, and at low frequency at the highly positive and negative bias, the phenomenon is still observed. The frequency dispersion $\triangle C$ of w/ PDA+FGA one (13.6%) is weaker than w/ PDA one (15.4%), is shown in **Table. 3.3**, which may show the lower number of border traps for w/ PDA+FGA one, too.

In summary, we can consider the effect of forming gas annealing on the electrical properties of all the capacitors, however, the influence of post deposition annealing is still comparatively unapparent for plasma treated MOS devices. In order to acquire quantitative definition of border traps density, we resort to a distributed bulk-oxide traps model, which is introduced in next chapter, **Chapter 4**.

3.4 Comparison of Different Plasma Treatments

3.4.1 Comparison of Different Number of Times for Plasma Treatments

From **Fig.18** to **Fig. 25**, we notice that the highest times of plasma treatment has the optimum capacitors performance due to its weakest frequency dispersion in the regions of accumulation, depletion, and inversion. However, the gate control of w/ PDA and w/ PDA+FGA for 2cyc./plasma is the worst in account of its smallest C_{max}. We also observe that the highest times of plasma treatment has the smallest C_{max},

which is attributed to the intense oxidation for applying high times of plasma treatment.

3.4.2 The Effect of Plasma Treatments on Electrical Characteristics

From **Fig. 3.26**, in contrast of w/ FGA condition and 1 MHz ~ 1 kHz, we note that w/o plasma one has the worst transition ability of C_{max} to C_{min}, however, the inversion characteristic is the best. For the post-deposition plasma treatment, it resulted in the large C_{max} of the capacitor, but the worst inversion properties and frequency dispersion in accumulation (9.73%). The plasma treatment during atomic-layer-deposition process (2cyc./plasma) has the optimum InAs MOS characteristics due to great ability of gate control, weaker frequency dispersion at the bias of accumulation (6.97%), depletion, and inversion region. The frequency dispersion is compared in **Table. 3.4**.

The effect of plasma treatment on capacitors electrical properties is improving the oxide and interface quality, especially for high number of times in plasma during the process of atomic-layer-deposition.

3.5 Summary

We have investigated the effects on the HfO_2/InAs MOS capacitors by utilizing different plasma treatments during or post the process of atomic-layer-deposition. It is observed that there are weak frequency dispersion in the regions of accumulation, depletion, and inversion, for higher number of times in plasma treatment, i.e., 2cy/plasma treatment. This represented that the ability of improving high-*k* dielectrics

and high-*k* dielectric/InAs interface quality is great for high number of plasma treatment. By forming gas annealing (300℃/30min.), the high-*k* dielectrics and high-*k* dielectric/InAs interface quality were further improved, and InAs MOS capacitors have the good electrical characteristics such as optimum gate control.

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- ***Wafer preparation***

  - n(100)InAs
- ***Wafer clean***

  - acetone (5min.)

  - isopropanol (5min.)

  - HCl:H_2O=1:10 (2min.)
- ***TMA 10cyc. pretreatment***
- ***HfO_2 60cyc. deposition in combination with w/o, 2, 4, 8, cyc./20s O_2-plasma and post-deposition O_2-plasma treatment by ALD system (250˚C dep.)***
- ***PDA (400˚C/120s)***
- ***Gate electrode formation (Ti/Pt)***
- ***Backside-contact deposition (Au/Ge/Ni)***
- ***FGA (300˚C/30min.)***

Fig. 3.1 The process flow of the capacitors with different O_2-plasma treatments and post-deposition thermal treatments.

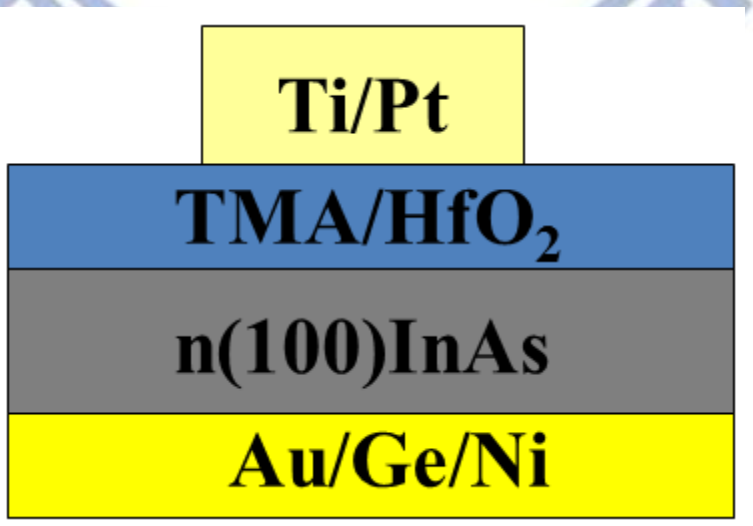


Fig. 3.2 The device structure with ALD-TMA/HfO_2.

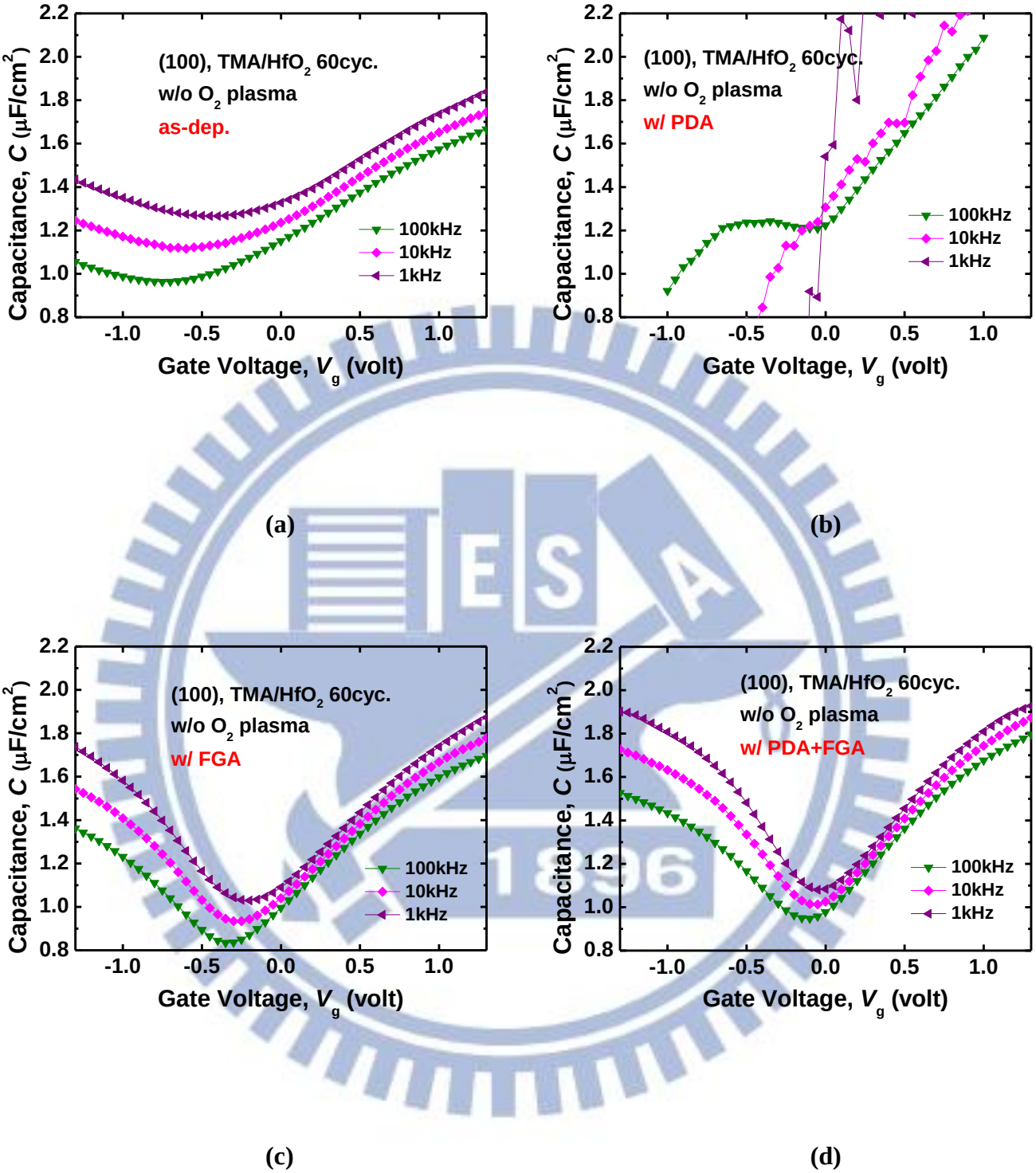


Fig. 3.3 Multi-frequency *C-V* curves of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/o O_2-plasma treatment) measured in 1kHz, 10kHz, and 100kHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

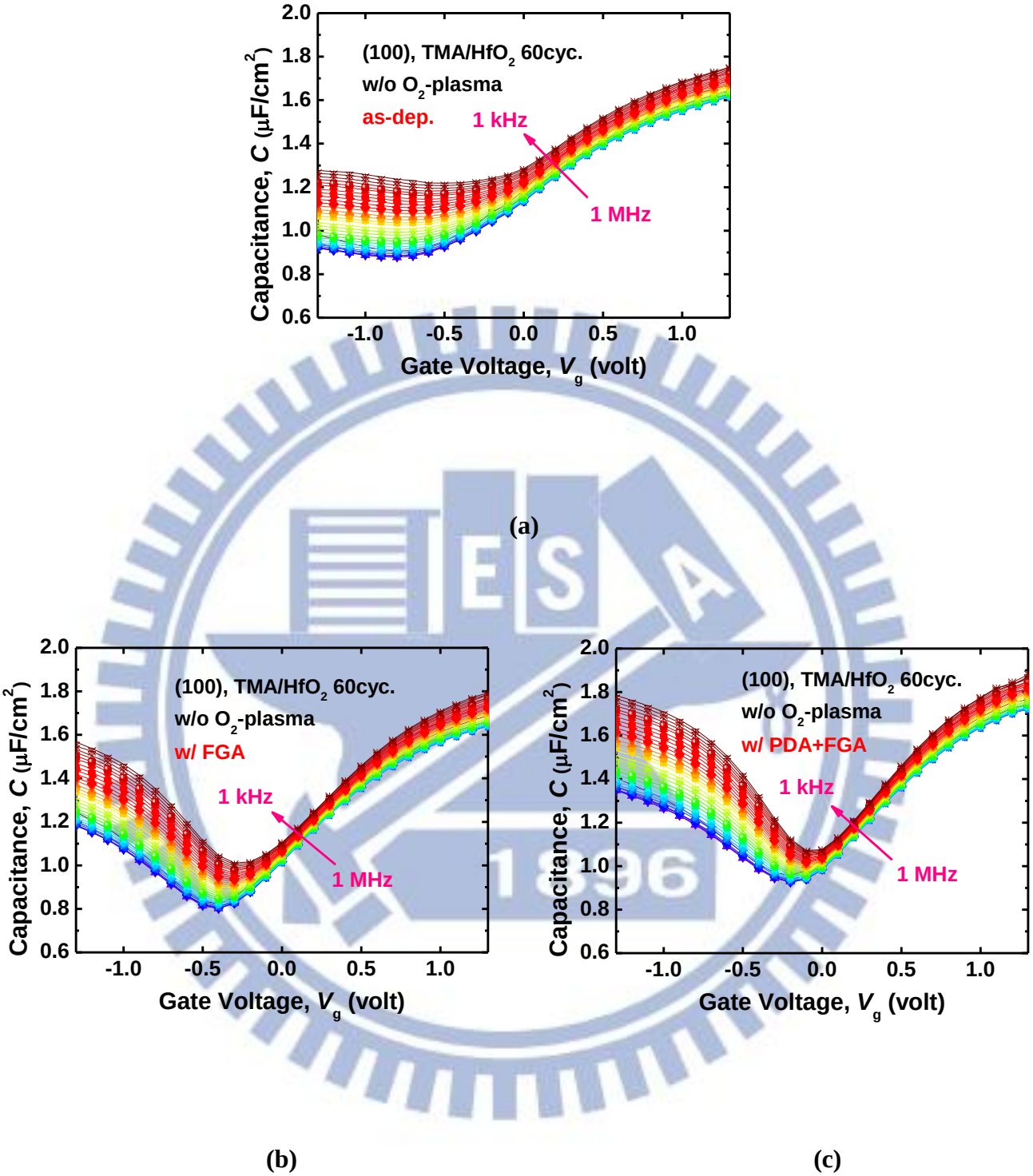


Fig. 3.4 Multi-frequency *C*-*V* maps of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/o O_2-plasma treatment) measured in 1kHz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ FGA; (c) w/ PDA+FGA.

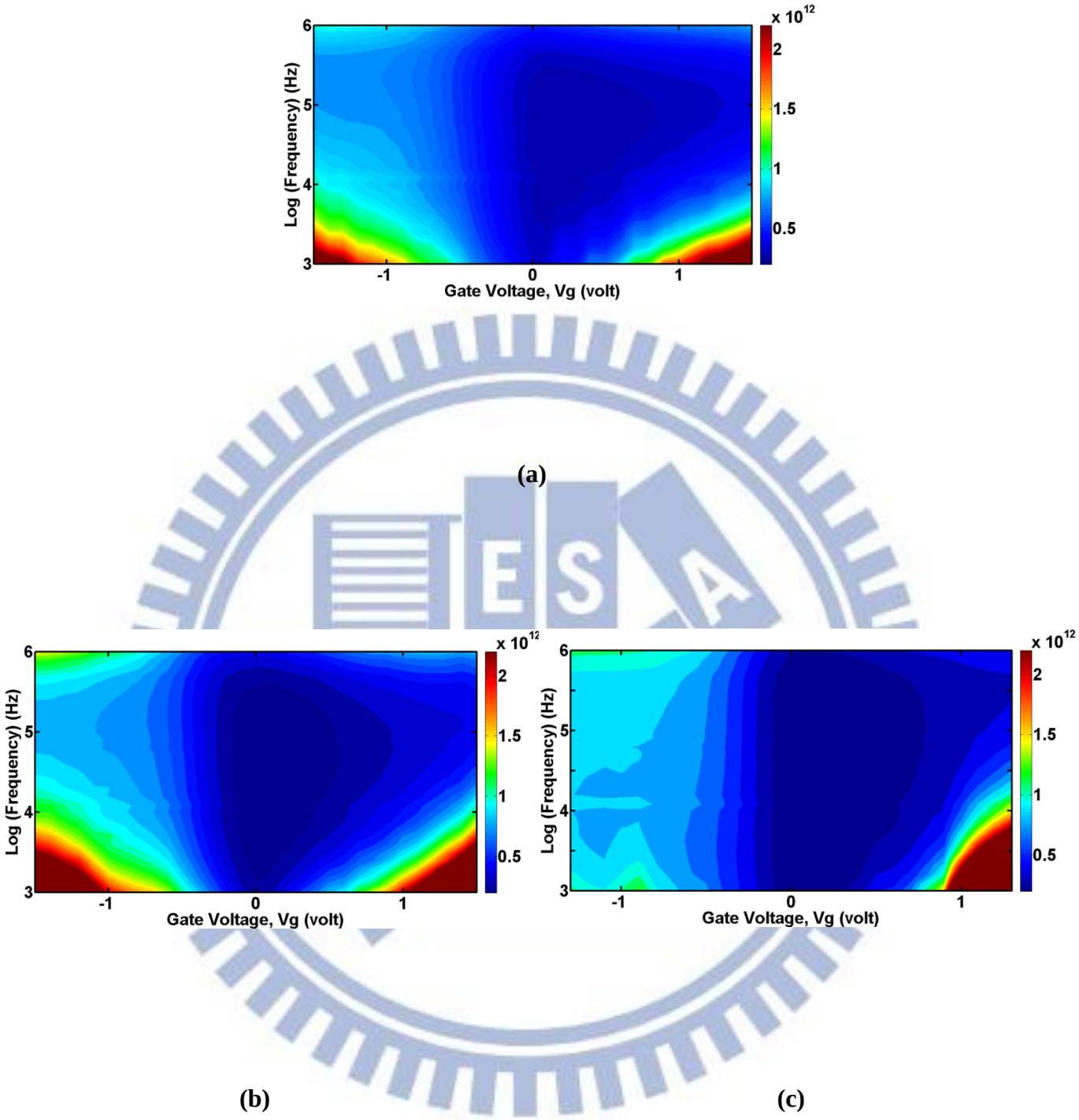


Fig. 3.5 *G/Aq$_0$ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/o O_2-plasma treatment) measured in 1kHz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ FGA; (c) w/ PDA+FGA.

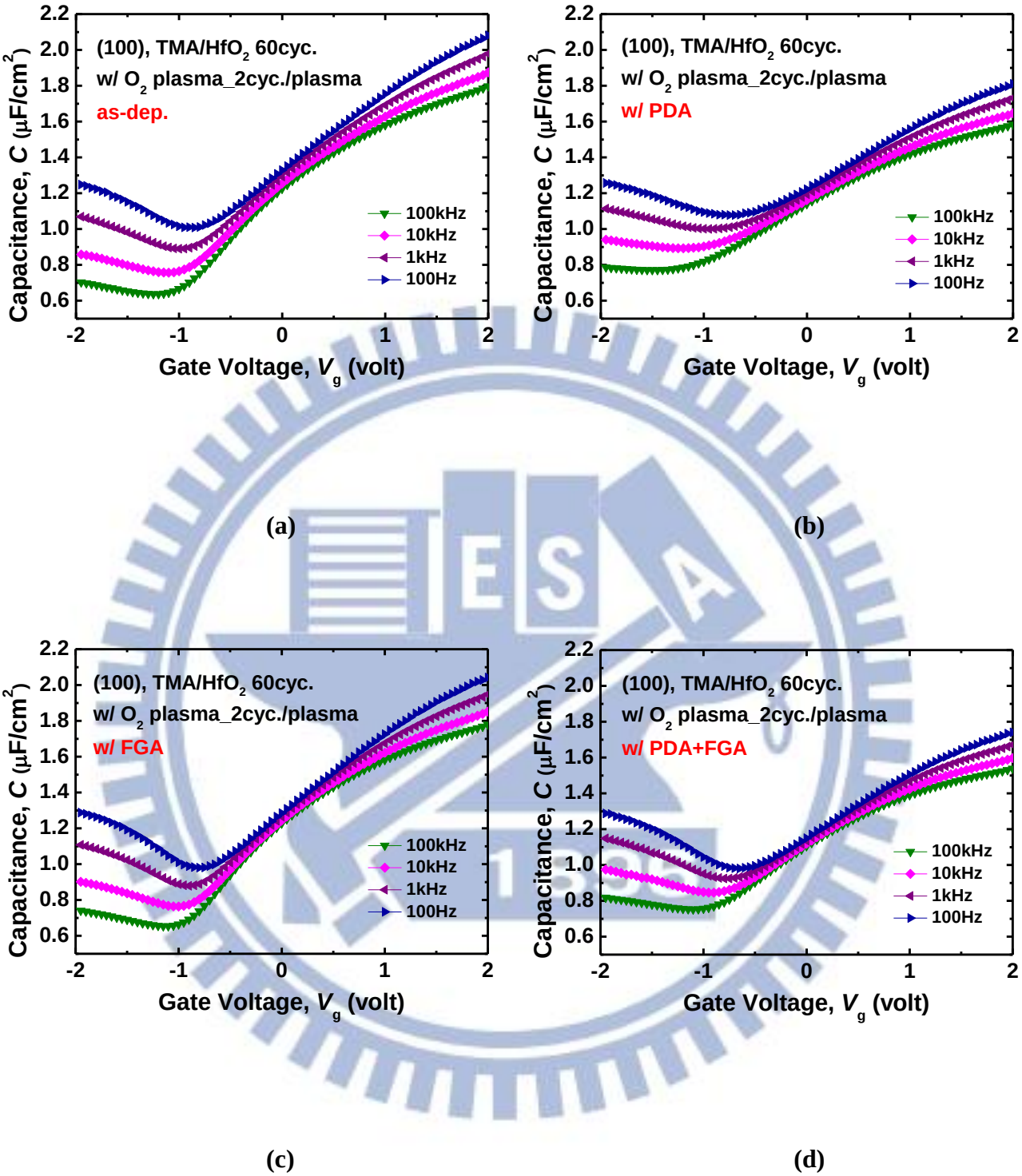


Fig. 3.6 Multi-frequency *C-V* curves of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 2cyc./plasma) measured in 100Hz, 1kHz, 10kHz, and 100kHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

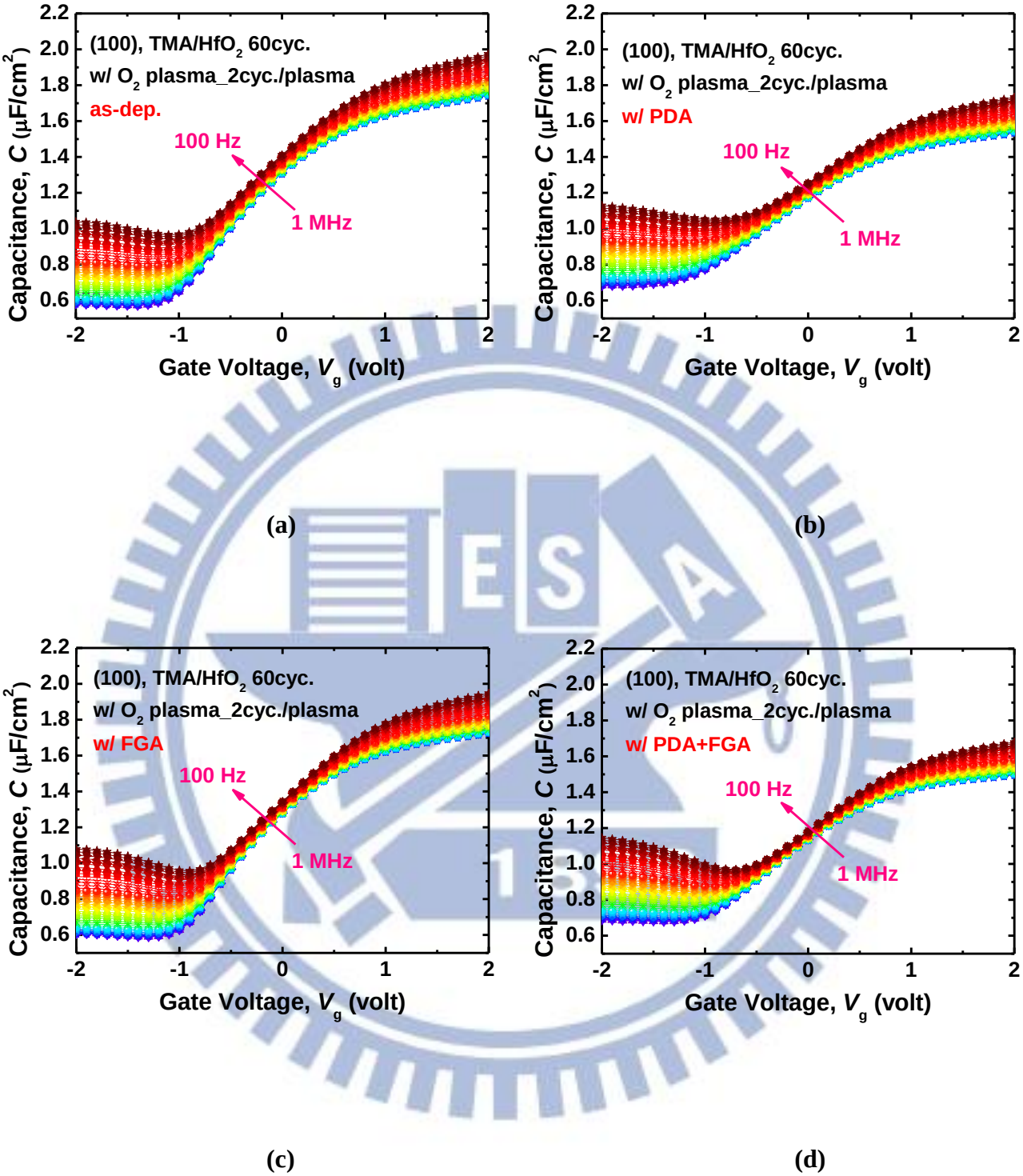


Fig. 3.7 Multi-frequency *C*-*V* maps of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 2cyc./plasma) measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

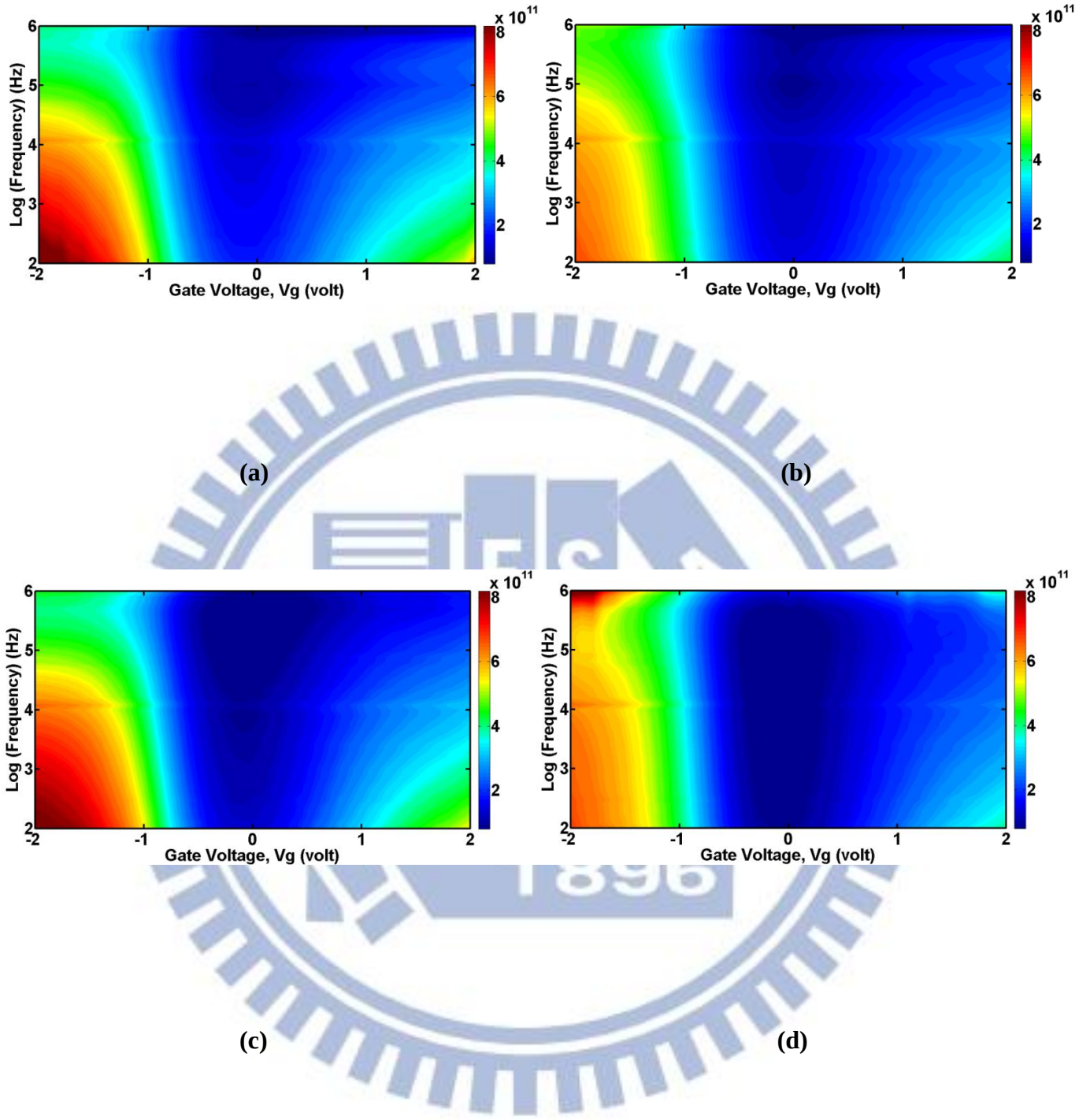


Fig. 3.8 *G/Aq₀ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 2cyc./plasma) measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

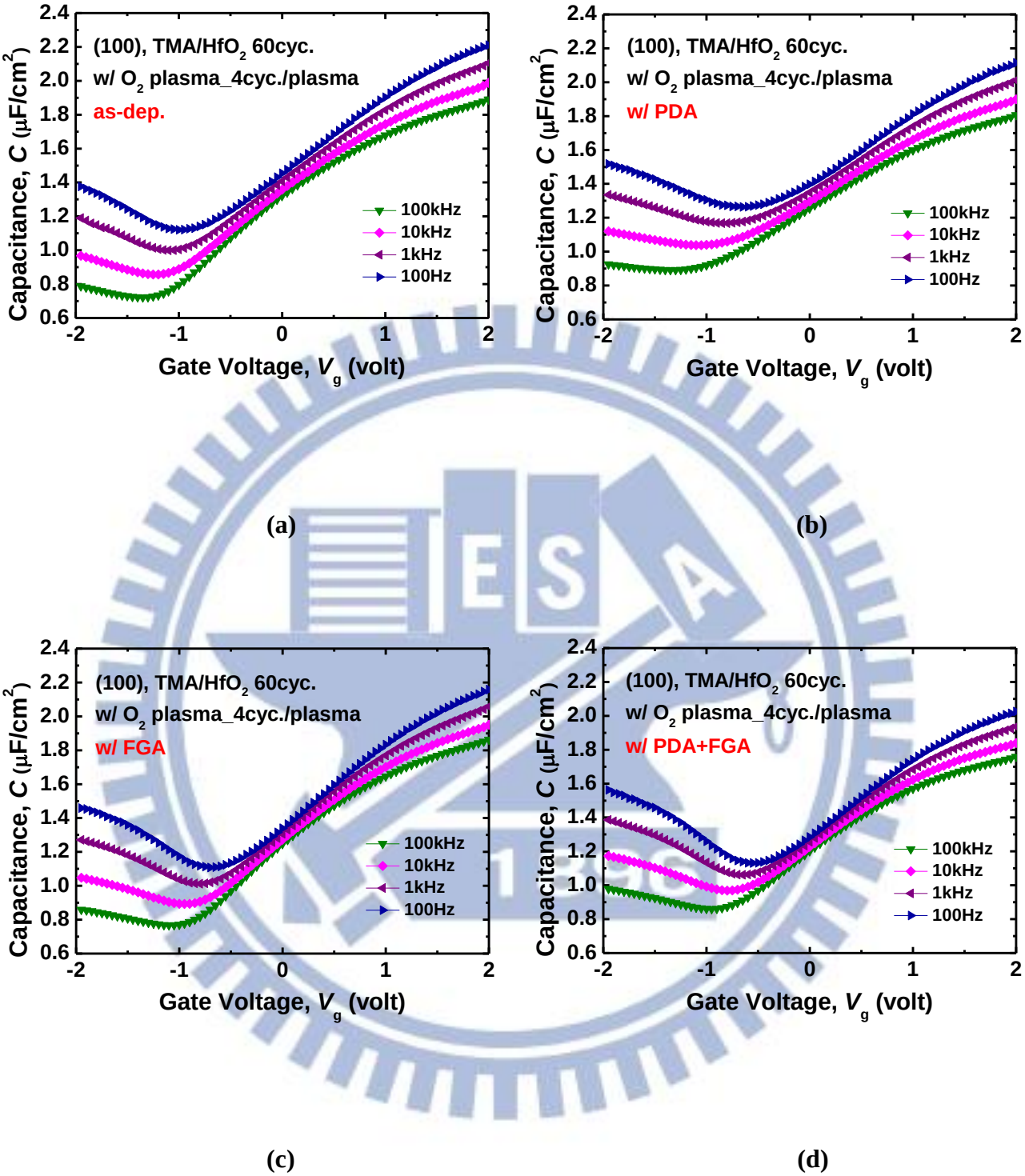


Fig. 3.9 Multi-frequency *C-V* curves of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 4cyc./plasma) measured in 100Hz, 1kHz, 10kHz, and 100kHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

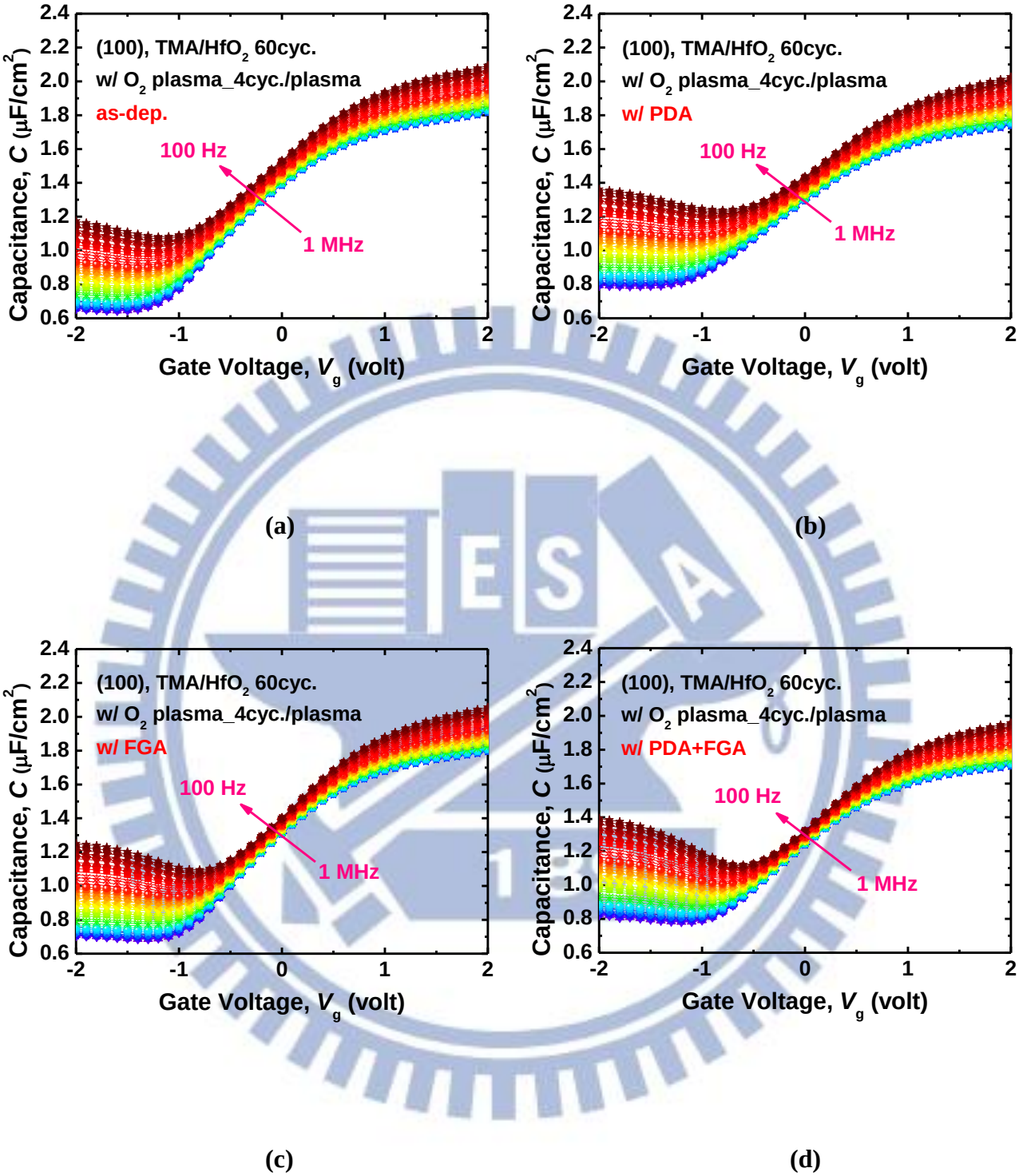


Fig. 3.10 Multi-frequency *C*-*V* maps of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 4cyc./plasma) measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

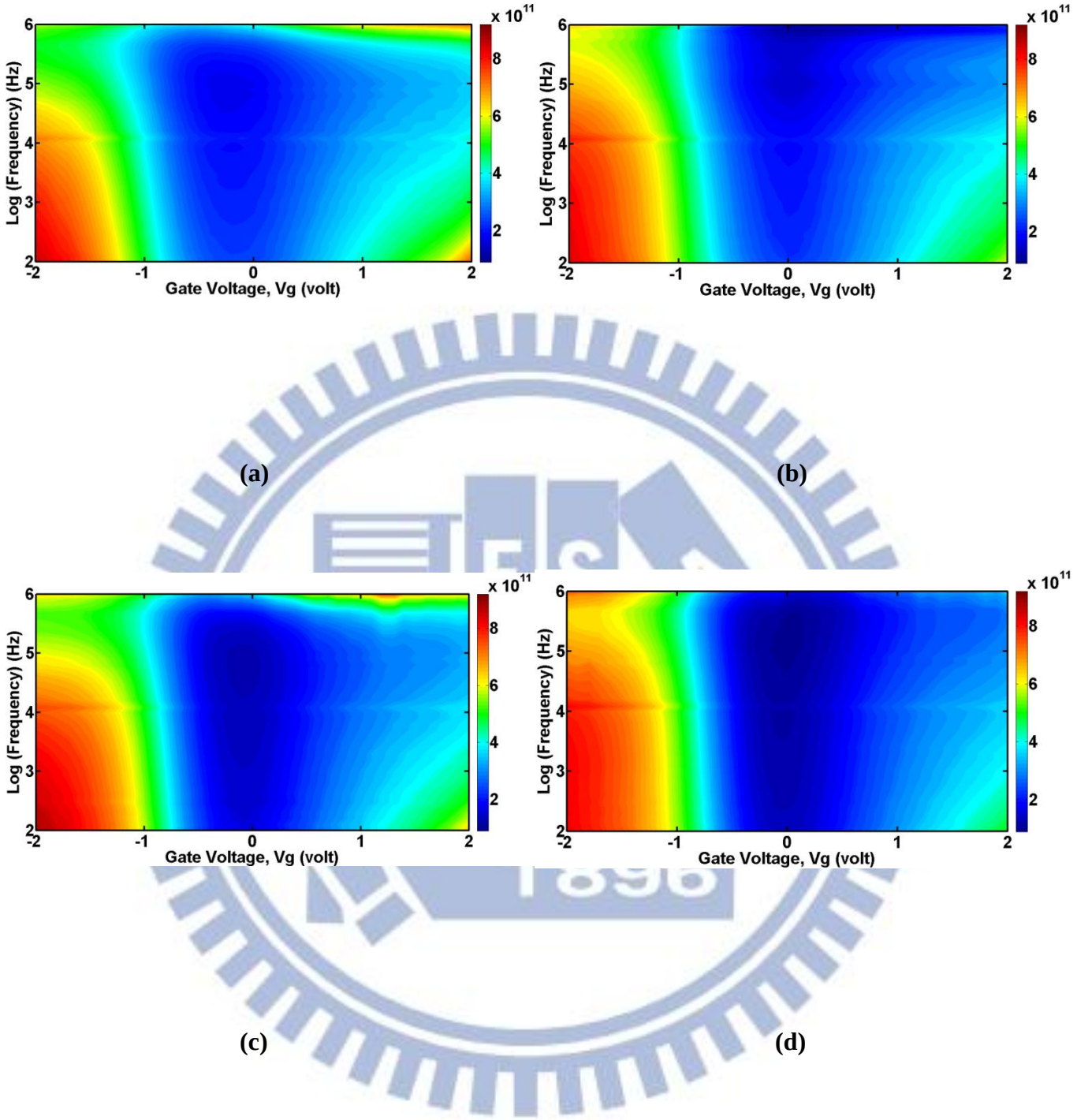


Fig. 3.11 *G/Aq$_0$ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 4cyc./plasma) measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

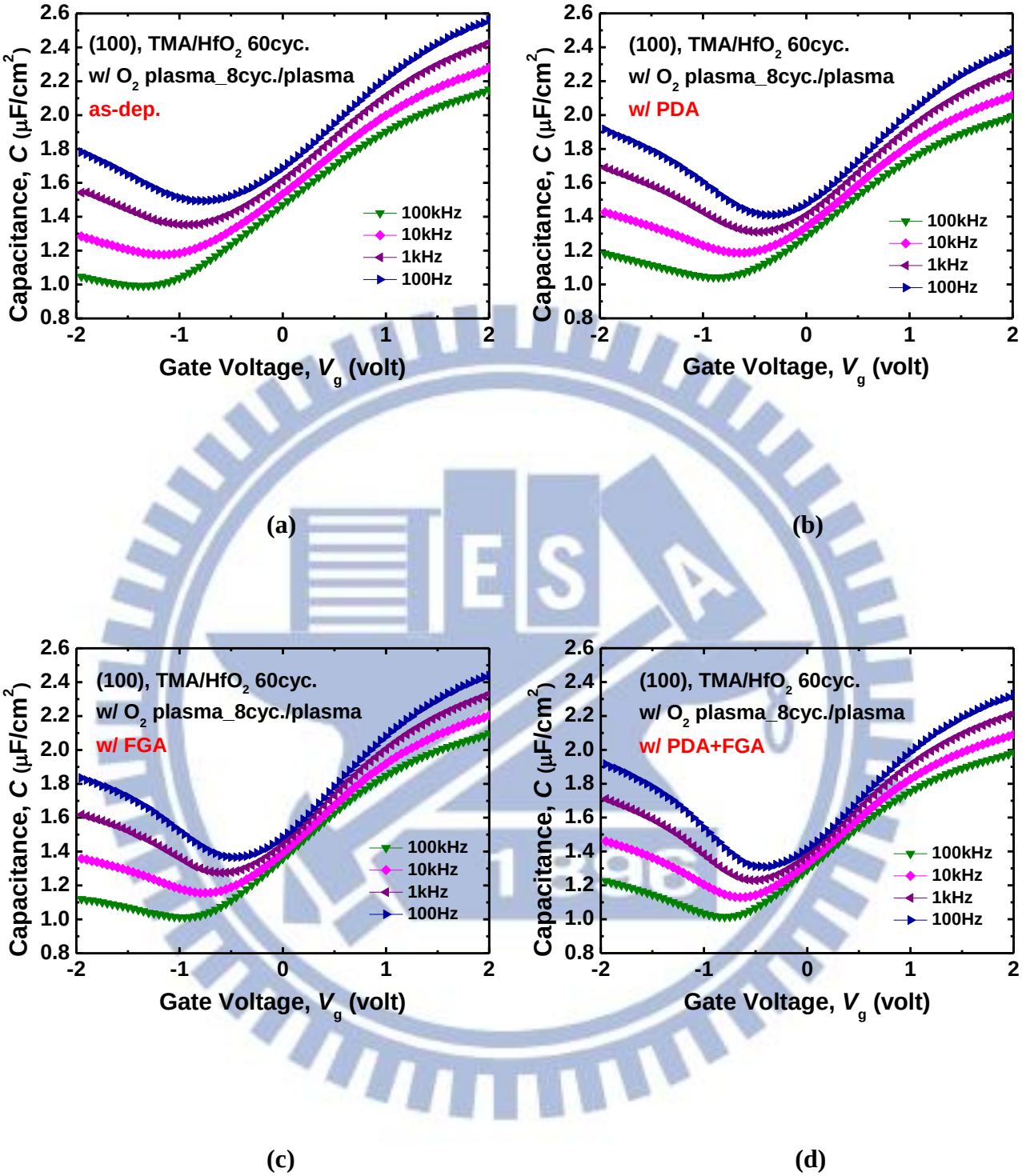


Fig. 3.12 Multi-frequency *C-V* curves of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 8cyc./plasma) measured in 100Hz, 1kHz, 10kHz, and 100kHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

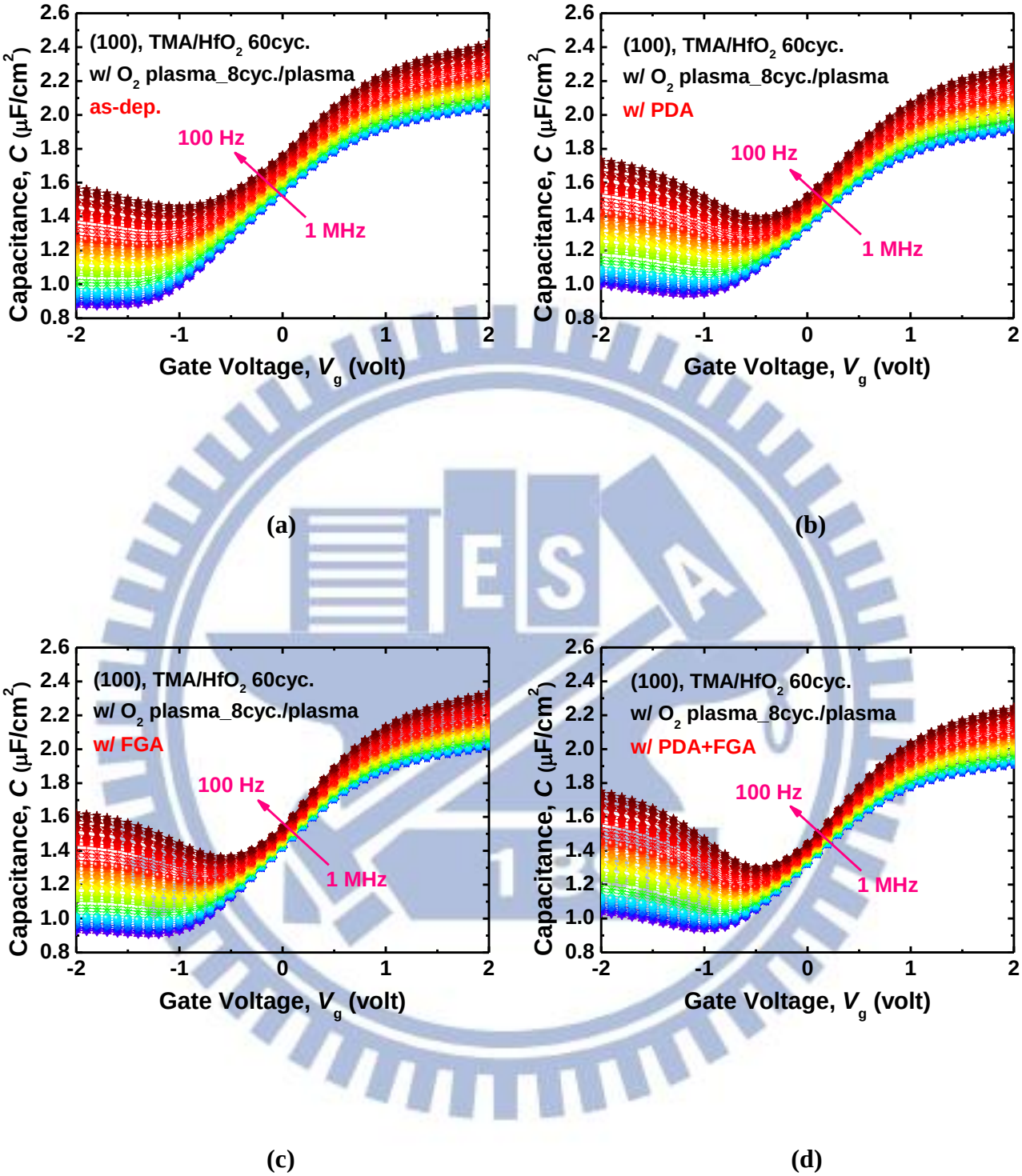


Fig. 3.13 Multi-frequency *C*-*V* maps of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 8cyc./plasma) measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

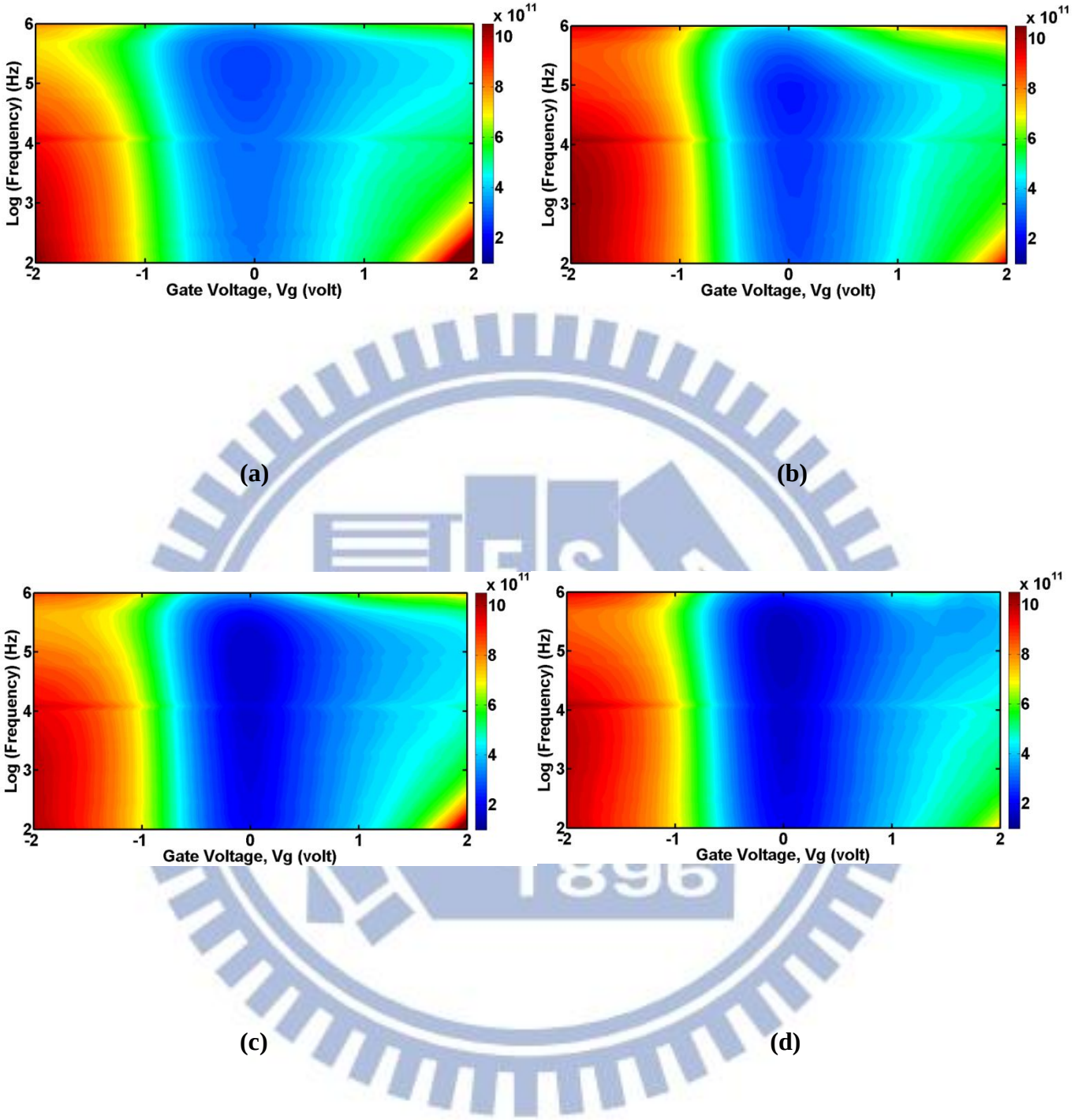


Fig. 3.14 *G/Aq*$_0$*ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ 8cyc./plasma) measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

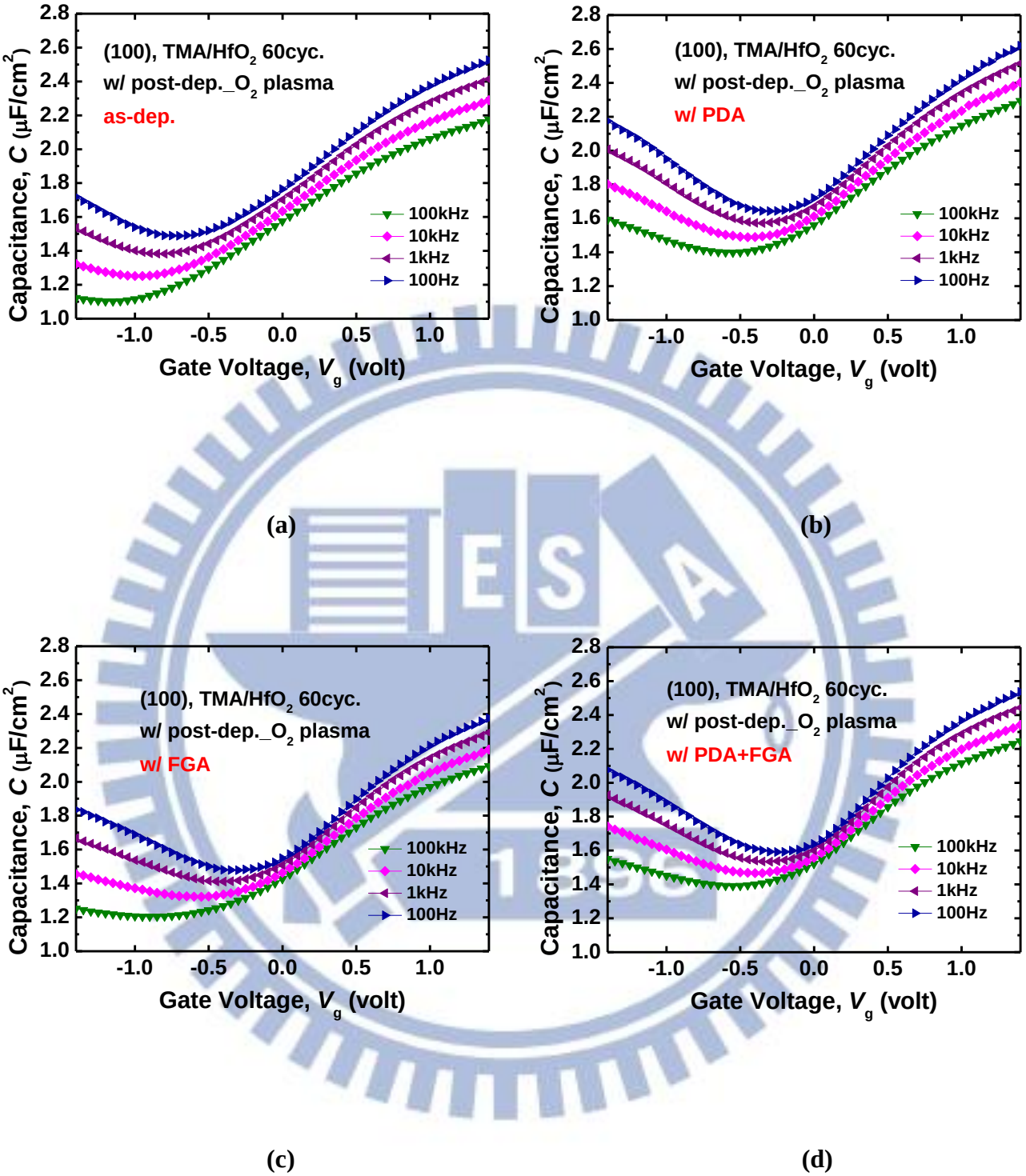


Fig. 3.15 Multi-frequency *C-V* curves of Pt/Ti/TMA+HfO_2/n-InAs capacitors (post-deposition O_2-plasma treatment for 10min.) measured in 100Hz, 1kHz, 10kHz, and 100kHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

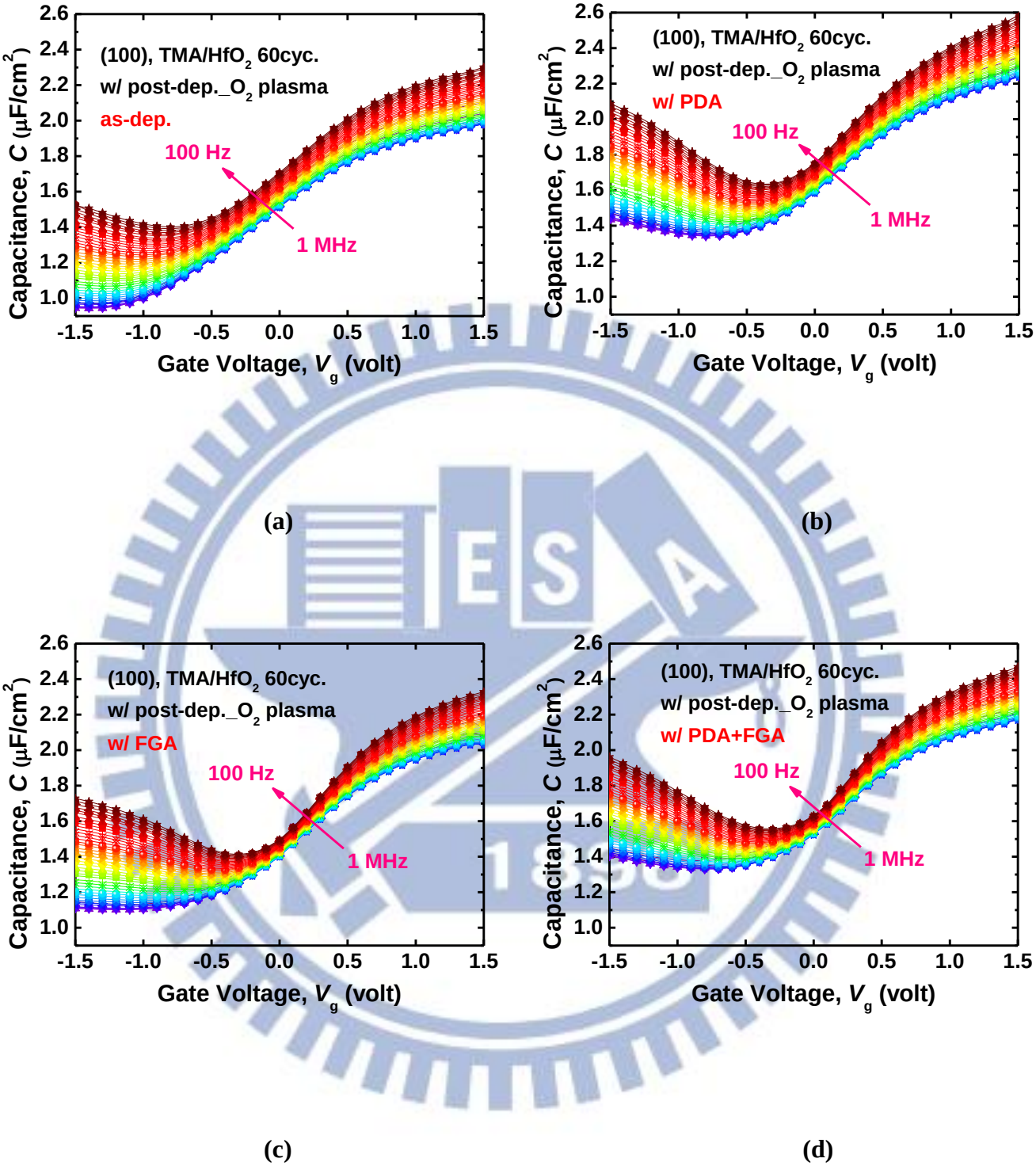


Fig. 3.16 Multi-frequency *C-V* maps of Pt/Ti/TMA+HfO_2/n-InAs capacitors (post-deposition O_2-plasma treatment for 10min.) measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

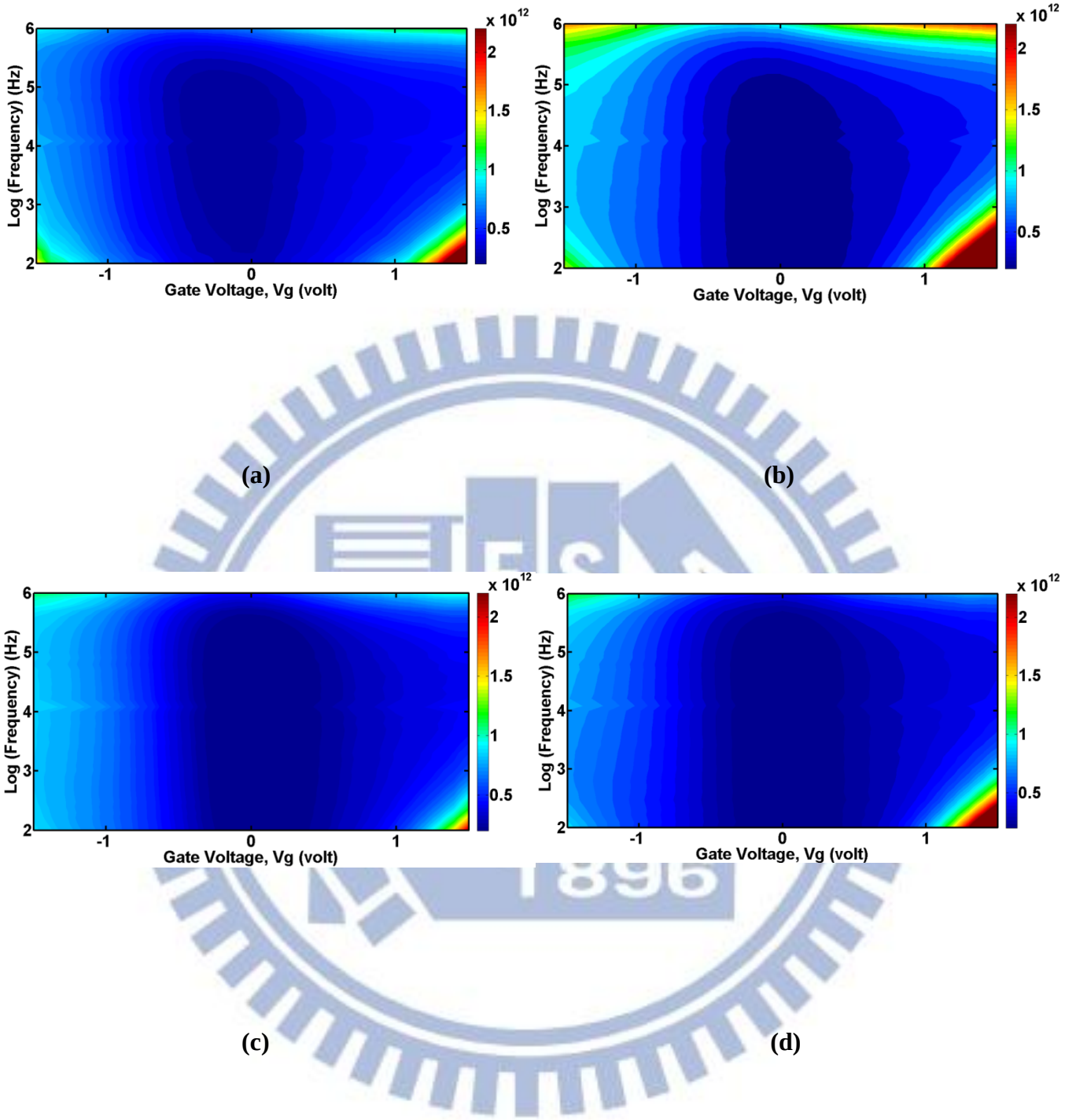


Fig. 3.17 *G/Aq*$_0$*ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of Pt/Ti/TMA+HfO_2/n-InAs capacitors (post-deposition O_2-plasma treatment for 10min.) measured in 100Hz to 1MHz, at the temperature of 300K: (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA.

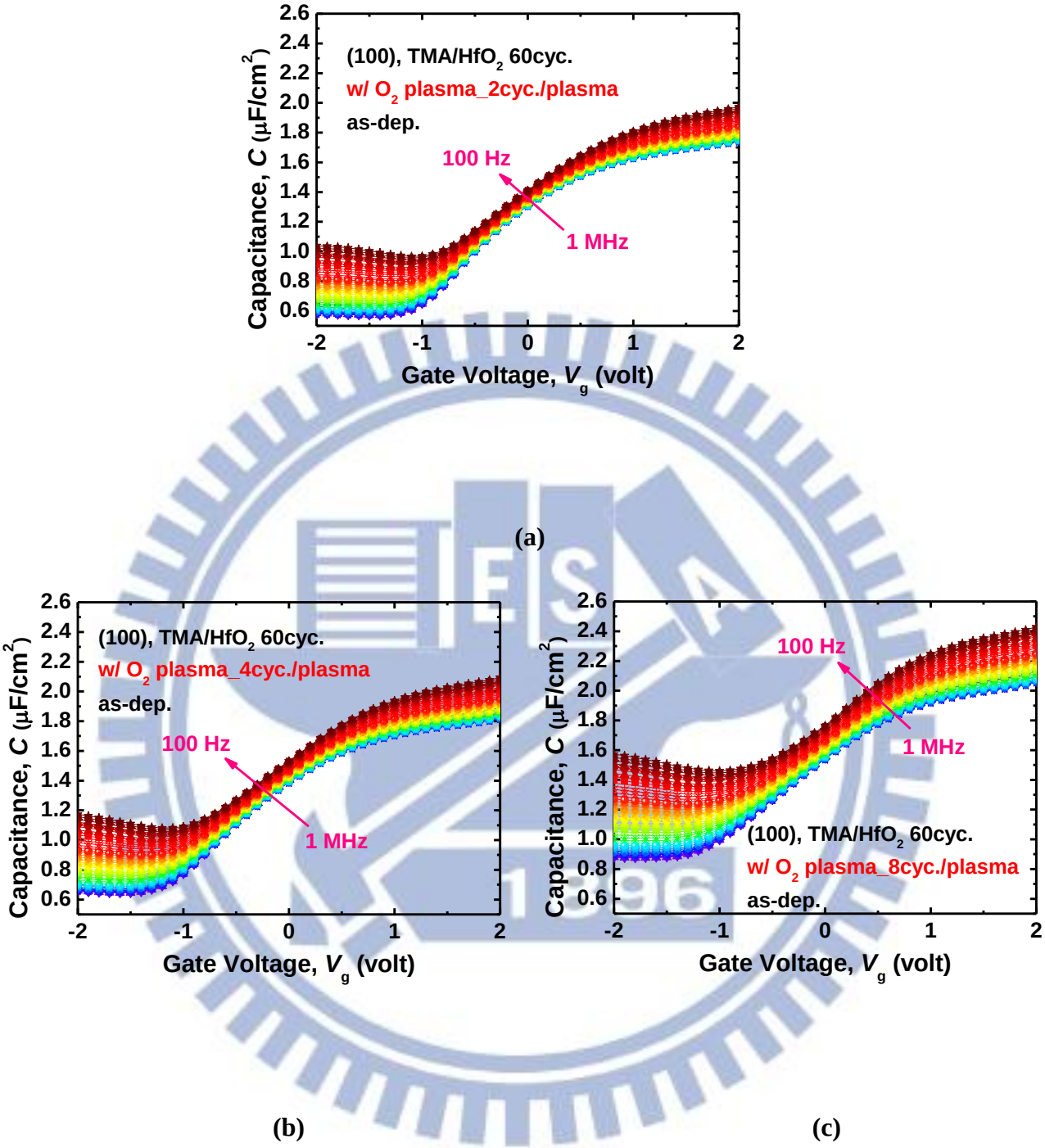


Fig. 3.18 Multi-frequency *C-V* maps of as-deposited Pt/Ti/TMA+HfO_2/n-InAs capacitors in comparison with various O_2-plasma density treatments measured in 100Hz to 1MHz, at the temperature of 300K: (a) 2cyc./plasma; (b) 4cyc./plasma; (c) 8cyc./plasma.

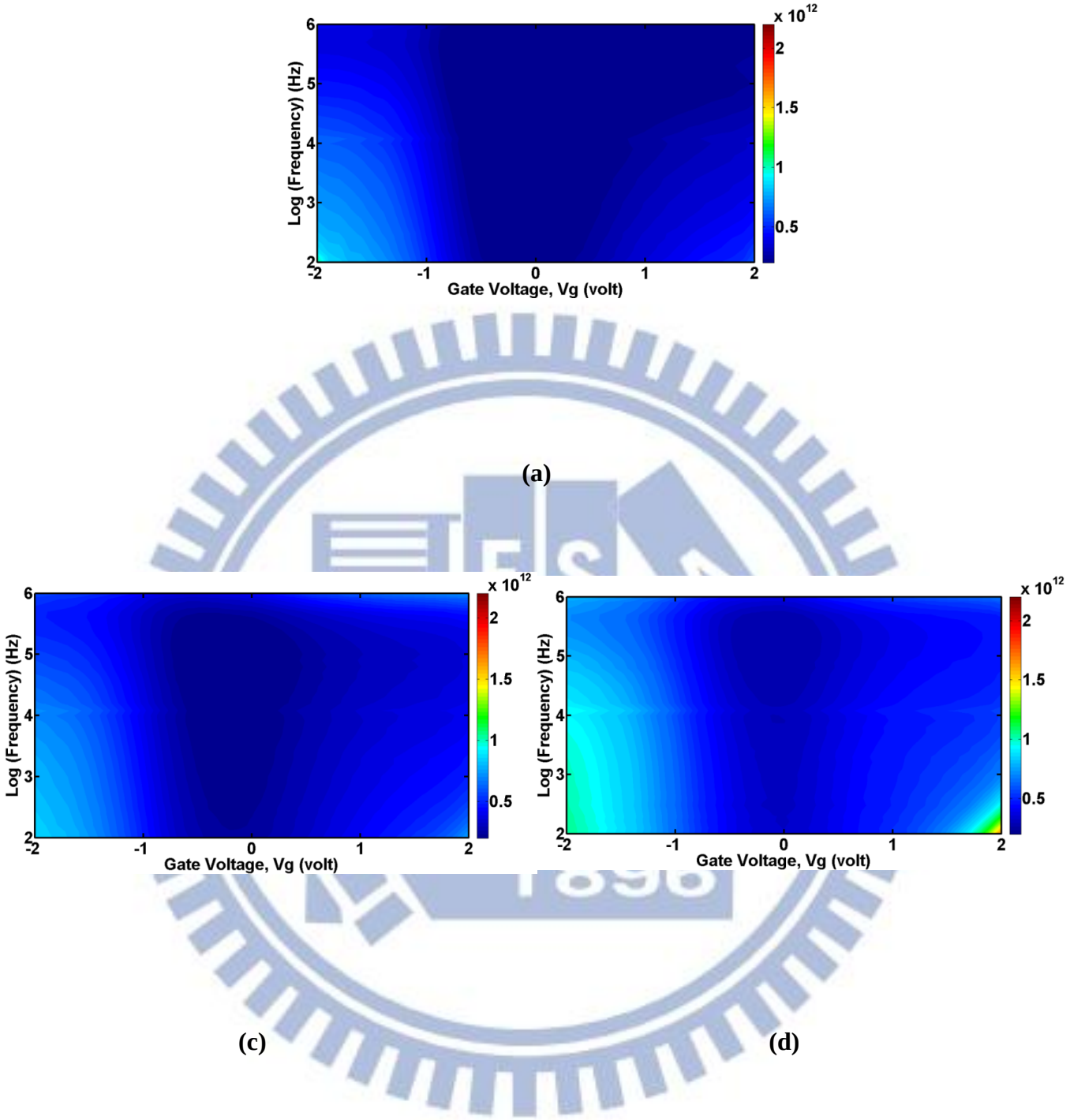


Fig. 3.19 *G/Aq₀ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of as-deposited Pt/Ti/TMA+HfO_2/n-InAs capacitors with various O_2-plasma density treatments measured in 100Hz to 1MHz, at the temperature of 300K: (a) 2cyc./plasma; (b) 4cyc./plasma; (c) 8cyc./plasma.

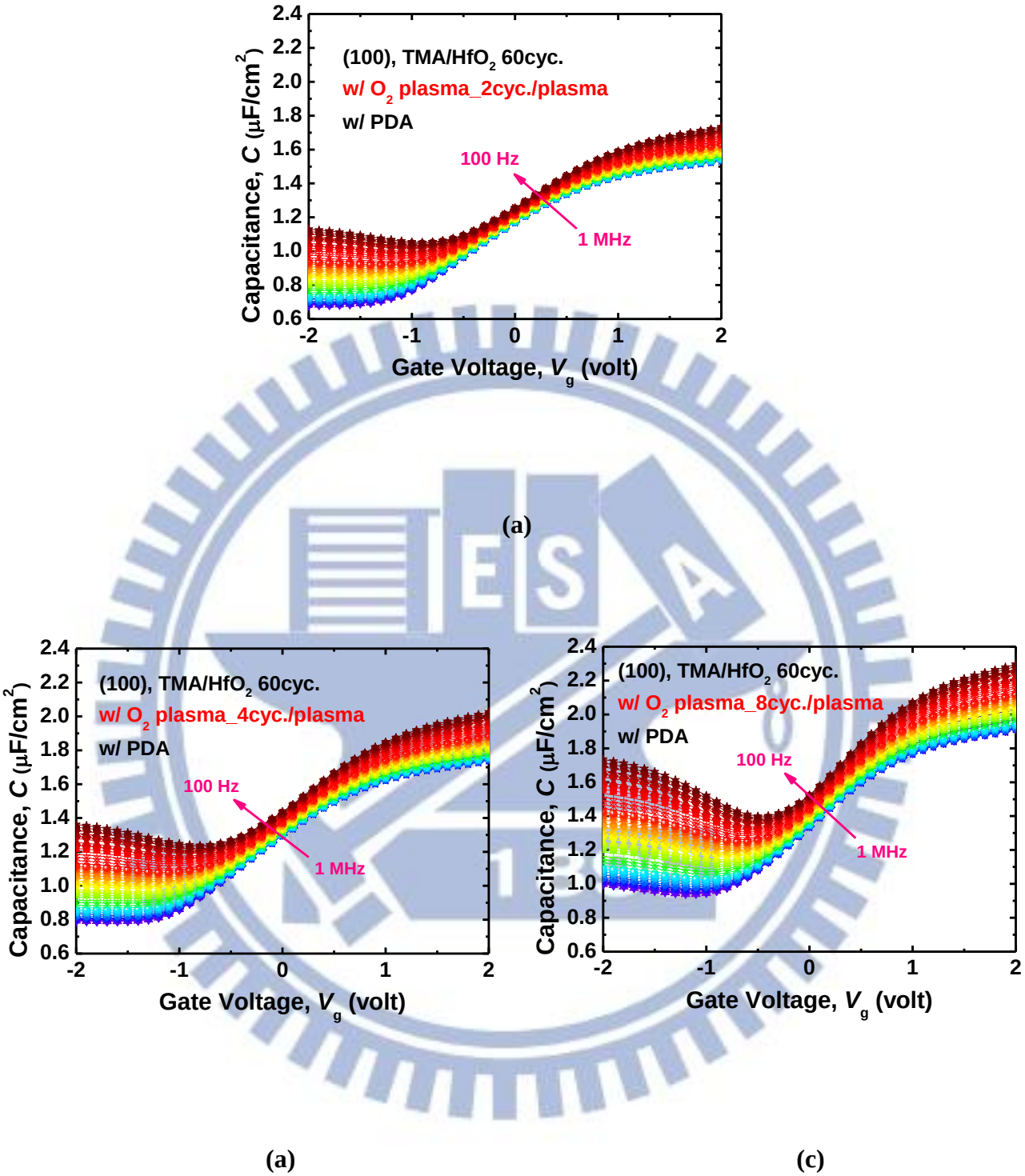


Fig. 3.20 Multi-frequency *C-V* maps of w/ PDA Pt/Ti/TMA+HfO_2/n-InAs capacitors with various O_2-plasma density treatments measured in 100Hz to 1MHz, at the temperature of 300K: (a) 2cyc./plasma; (b) 4cyc./plasma; (c) 8cyc./plasma.

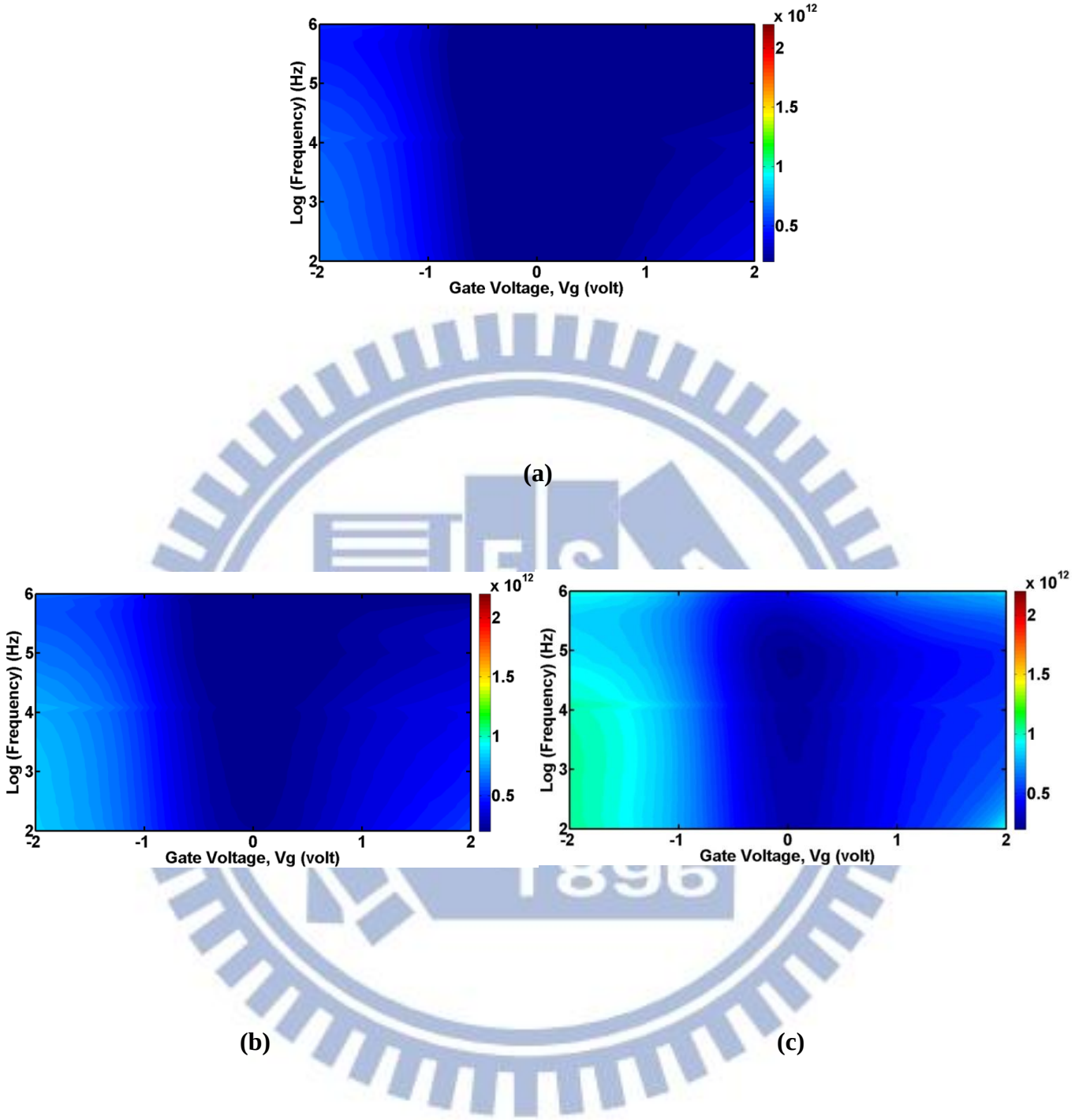


Fig. 3.21 *G/Aq₀ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of w/ PDA Pt/Ti/TMA+HfO_2/n-InAs capacitors with various density O_2-plasma treatments measured in 100Hz to 1MHz, at the temperature of 300K: (a) 2cyc./plasma; (b) 4cyc./plasma; (c) 8cyc./plasma.

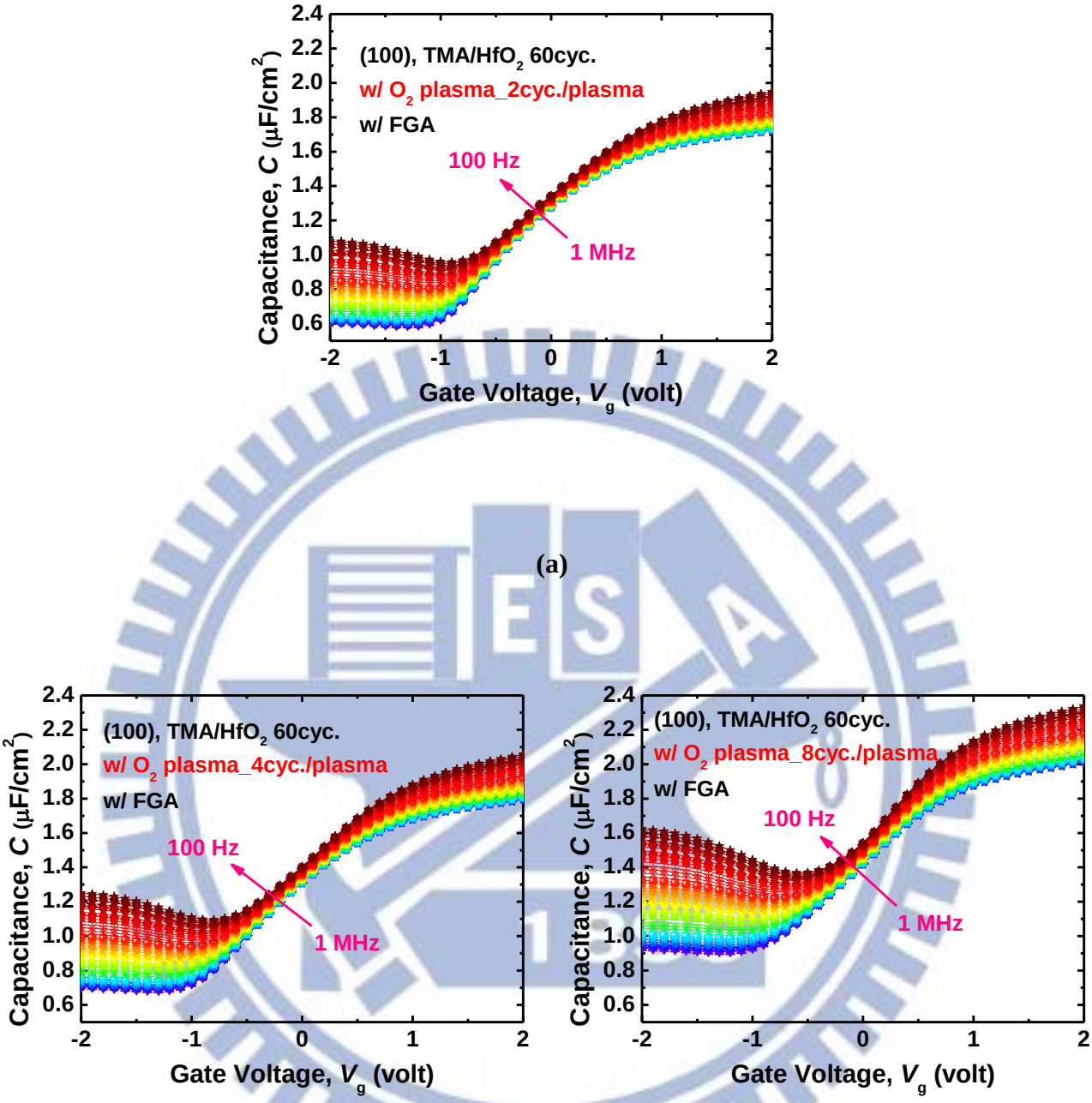


Fig. 3.22 Multi-frequency *C-V* maps of w/ FGA Pt/Ti/TMA+HfO_2/n-InAs capacitors with various O_2-plasma density treatments measured in 100Hz to 1MHz, at the temperature of 300K: (a) 2cyc./plasma; (b) 4cyc./plasma; (c) 8cyc./plasma.

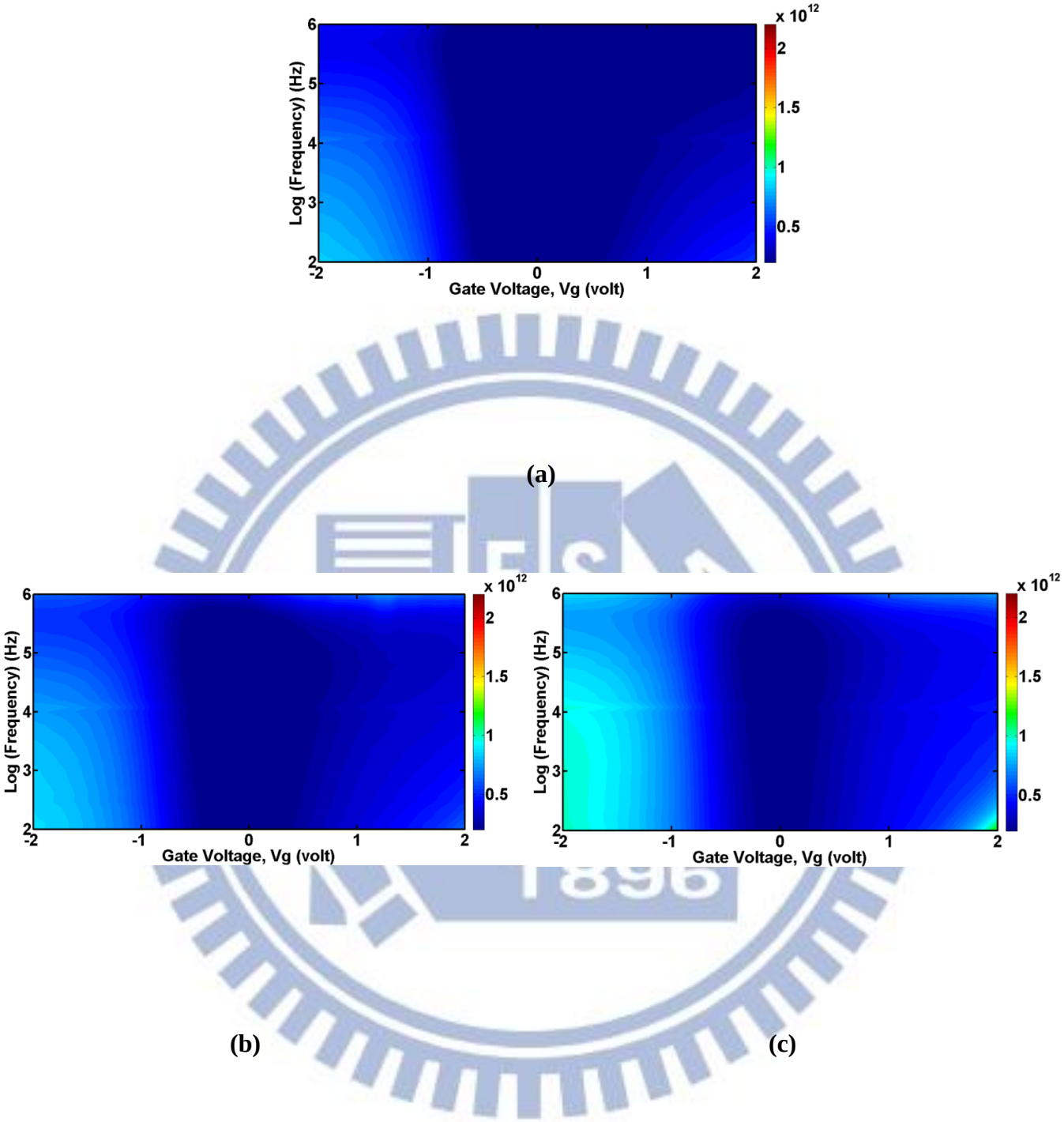


Fig. 3.23 *G/Aq$_0$ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of w/ FGA Pt/Ti/TMA+HfO_2/n-InAs capacitors with various O_2-plasma density treatments measured in 100Hz to 1MHz, at the temperature of 300K: (a) 2cyc./plasma; (b) 4cyc./plasma; (c) 8cyc./plasma.

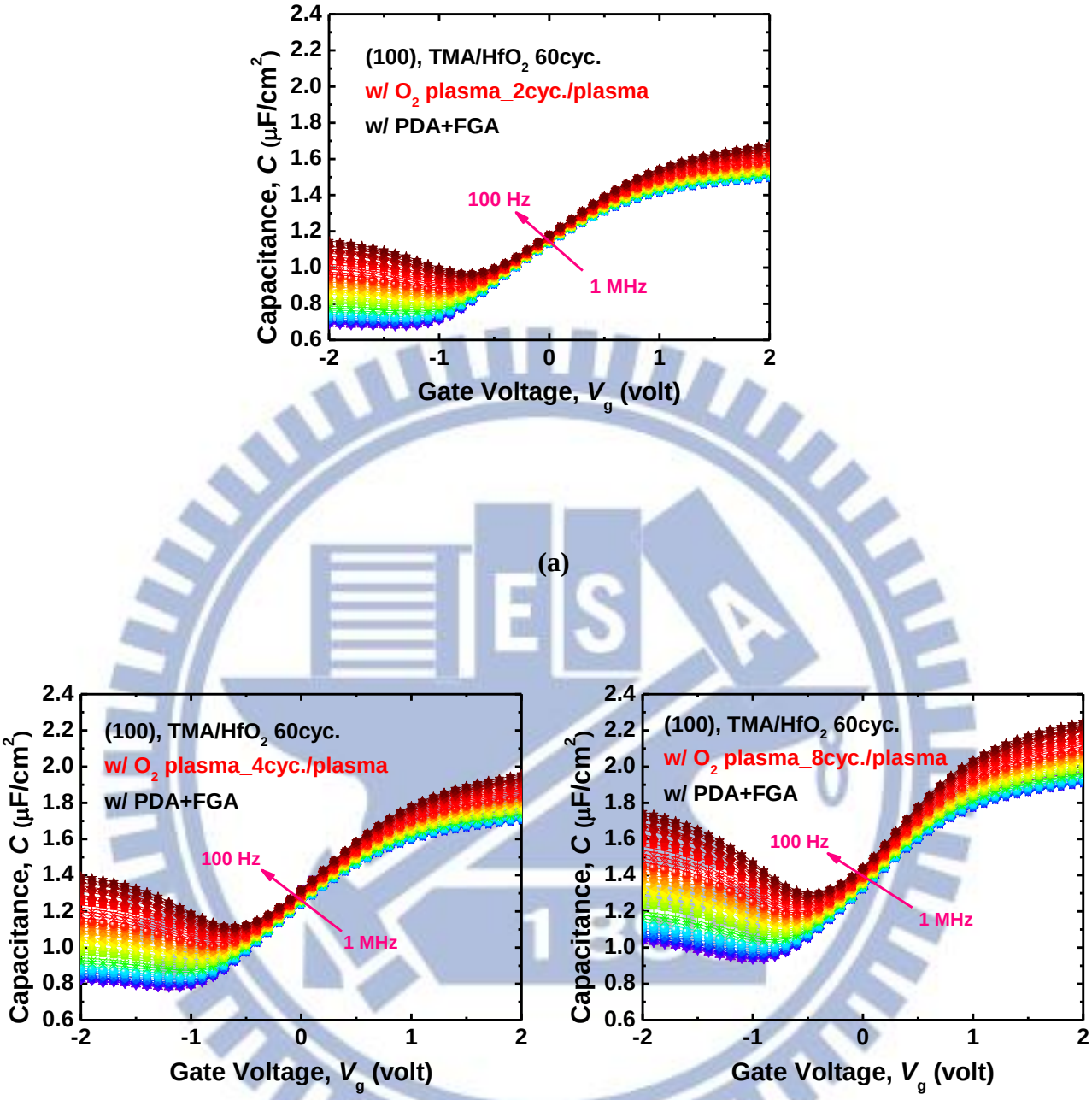


Fig. 3.24 Multi-frequency *C-V* maps of w/ PDA+FGA Pt/Ti/TMA+HfO_2/n-InAs capacitors with various O_2-plasma density treatments measured in 100Hz to 1MHz, at the temperature of 300K: (a) 2cyc./plasma; (b) 4cyc./plasma; (c) 8cyc./plasma.

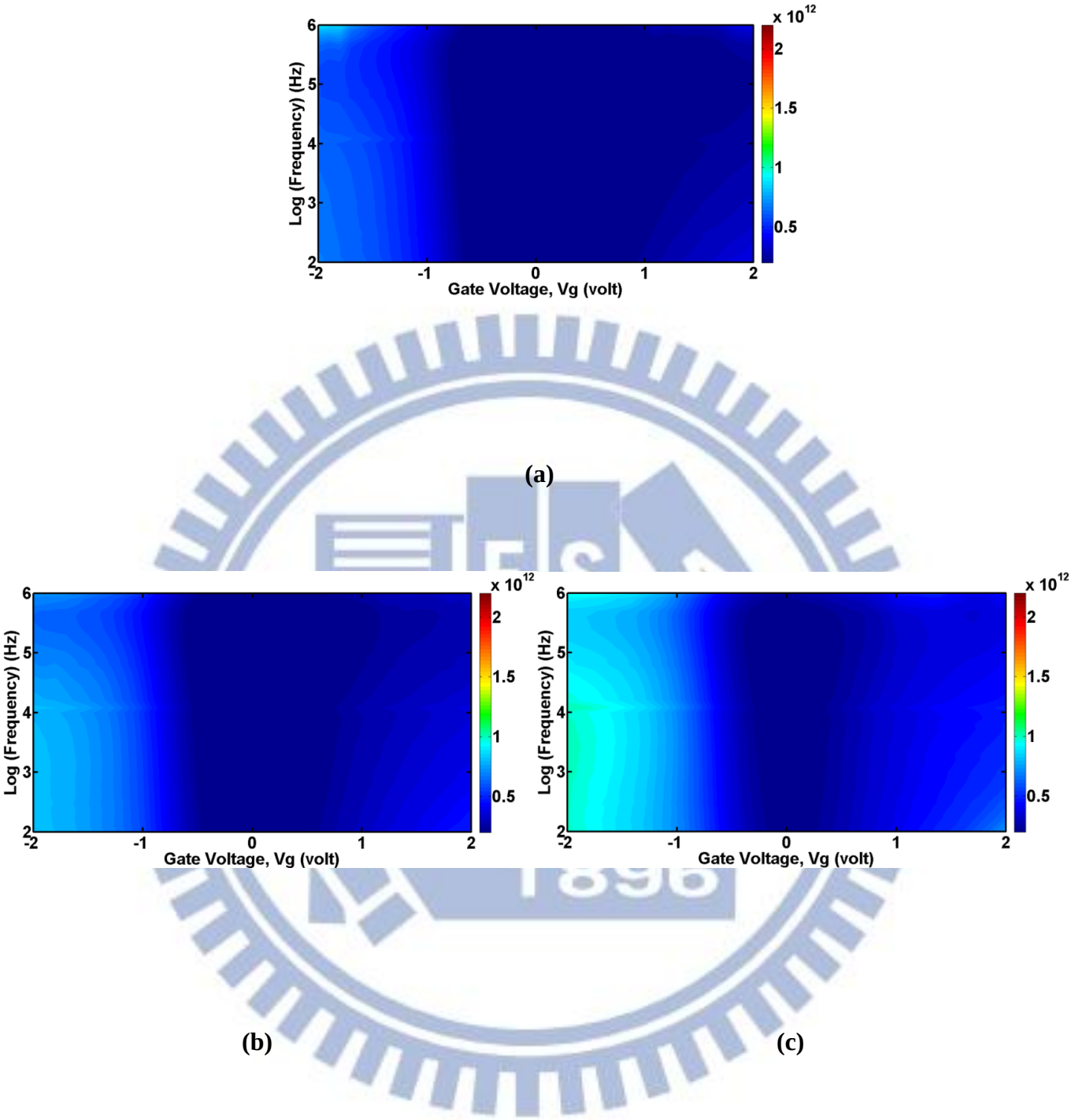


Fig. 3.25 *G/Aq₀ω-V* (a unit of $eV^{-1}cm^{-2}$) contours of w/ PDA+FGA Pt/TMA+HfO_2/n-InAs capacitors with various O_2-plasma density treatments measured in 100Hz to 1MHz, at the temperature of 300K: (a) 2cyc./plasma; (b) 4cyc./plasma; (c) 8cyc./plasma.

ΔC(@Vg = 1.3V)	As-dep.	w/ PDA	w/ FGA	w/ PDA+FGA
w/o O_2-plasma	8.42 %		9.30 %	9.81 %

Table. 3.1 The overview of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/o O_2-plasma treatment) with different post-deposition thermal processes in frequency dispersion $\Delta C(@V_g = 1.3V)$ is compared.

ΔC(@Vg = 2V)	As-dep.	w/ PDA	w/ FGA	w/ PDA+FGA
2cyc./plasma	13.2 %	12.7 %	12.8 %	12.1 %
4cyc./plasma	15.1 %	16.2 %	14.3 %	14.7 %
8cyc./plasma	17.9 %	19.9 %	15.8 %	17.7 %

Table. 3.2 The overview of Pt/Ti//TMA+HfO_2/n-InAs capacitors (w/ various O_2-plasma treatment) with different post-deposition thermal processes in frequency dispersion $\Delta C(@V_g = 2V)$ is compared.

ΔC(@Vg =1.5V)	As-dep.	w/ PDA	w/ FGA	w/ PDA+FGA
post-dep. O_2-plasma	16.1 %	15.4 %	14.5 %	13.6 %

Table. 3.3 The overview of Pt/Ti/TMA+HfO_2/n-InAs capacitors (w/ post-deposition O_2-plasma treatment) with different post-deposition thermal processes in frequency dispersion $\Delta C(@V_g = 1.5V)$ is compared.

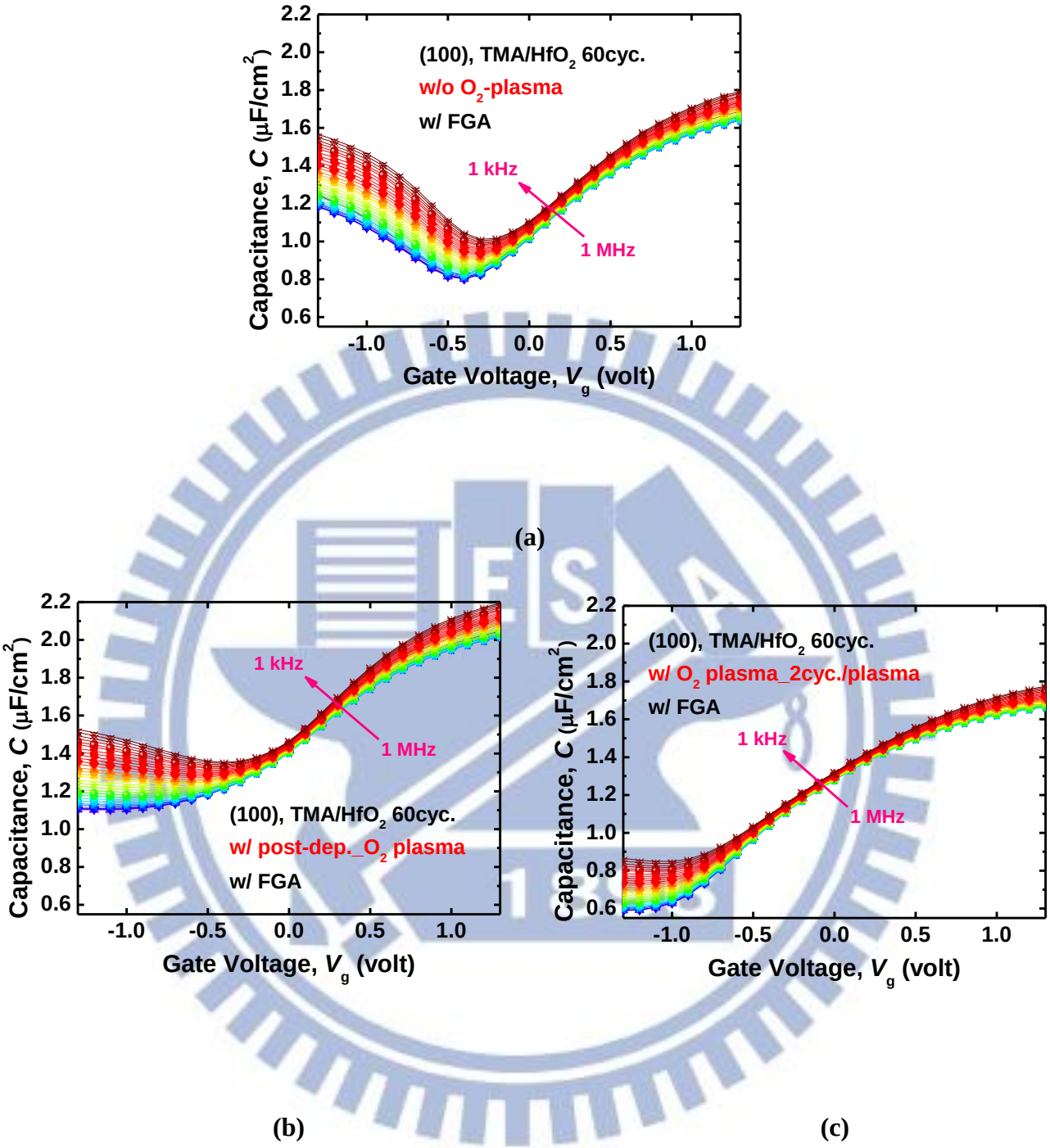
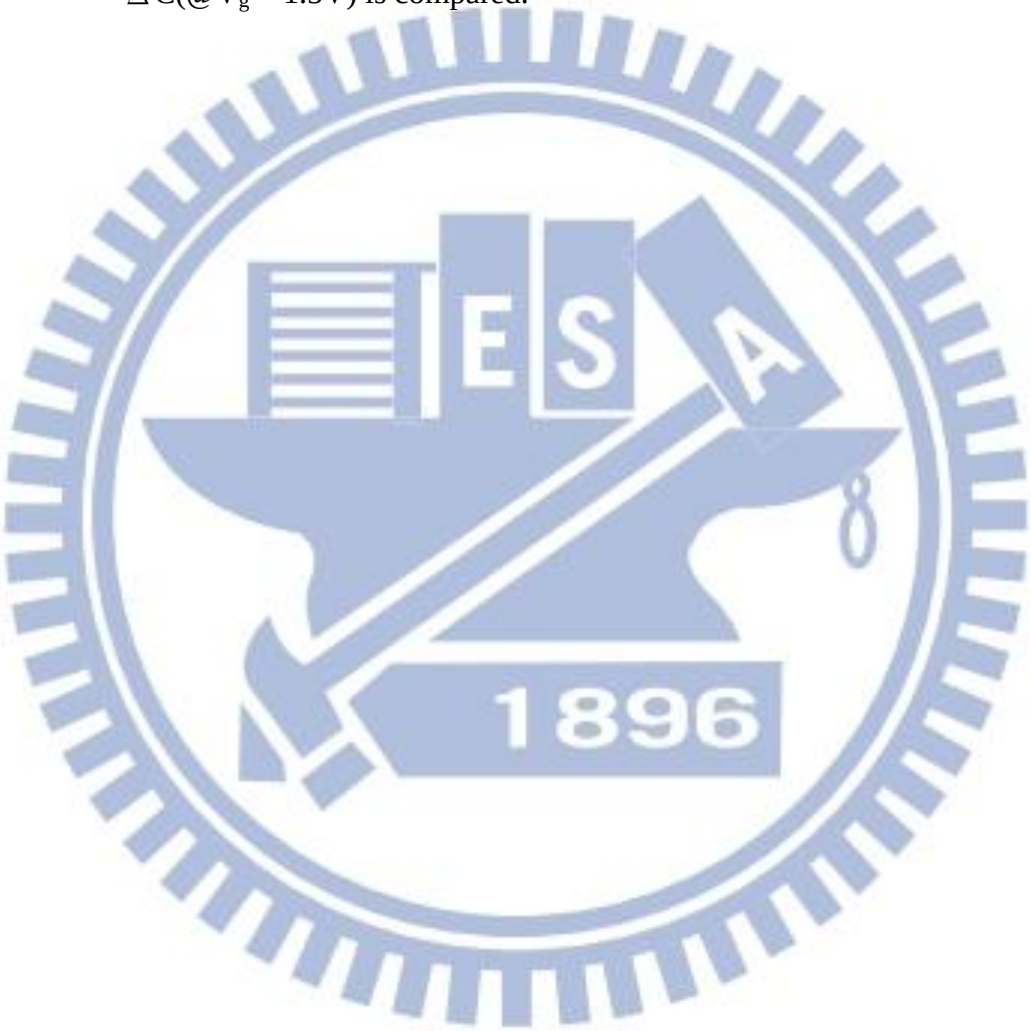


Fig. 3.26 Multi-frequency *C*-*V* maps of w/ FGA Pt/Ti/TMA+HfO_2/n-InAs capacitors with various O_2-plasma treatments measured in 1 kHz to 1 MHz, at the temperature of 300K: (a) w/o plasma; (b) post-deposition O_2-plasma treatment; (c) 2cyc./plasma.

	w/o	post-dep.	2cyc.
$\Delta C(@V_g = 1.5V)$	9.18 %	9.73 %	6.97 %

Table. 3.4 The overview of w/ FGA Pt/Ti/TMA+HfO_2/n-InAs capacitors with various O_2-plasma treatments measured at 1 kHz to 1 MHz in frequency dispersion $\Delta C(@V_g = 1.5V)$ is compared.



Chapter 4

The Extraction of Border Traps for InAs MOS Devices by a Distributed Bulk-Oxide Traps Model

4.1 Introduction

In many publications in the literature [1-6], dispersive frequency is observed in the capacitance-voltage (*C*-*V*) and conductance-voltage (*G*-*V*) data of high-κ/III-V metal-oxide-semiconductor (MOS) devices commonly. The frequency dispersion in the strong accumulation region can't be clarified by the conventional interface states whose time constant in such bias regime is much shorter than the period of typical measurement frequencies, i.e., 1 kHz - 1 MHz [7], [8]. On the other hand, the trap states inside the high-κ dielectric, which are called border traps or bulk-oxide traps, have long time constants when they interact with the conduction band by way of tunneling [9]. Moreover, as the conventional conductance method [7] for the interface states is adopted to the high to low transition (the maximum slope) of the capacitance-voltage (*C*-*V*) data, the dispersive frequency of conductance doesn't keep up with the well-known peak action. Furthermore, the stretch-out *C*-*V* curve comparing with the ideal *C*-*V* curve shows that the interface state density far surpass which is extracted from the frequency in such region. Such inconsistency can be resolved by a bulk-oxide trap model in which the low frequency part resulting in *C*-*V* curve stretch-out is stronger than the high-frequency part for the frequency dispersion.

In this chapter, the bulk-oxide trap model is completed by superadding integration of bulk-oxide traps density with respect to whole energy for computing the

equivalent admittance. A differential equation is derived and numerically solved to yield frequency-dependent capacitance and conductance of the InAs metal-oxide-semiconductor (MOS) devices. The model is validated and calibrated by HfO_2/n(100) InAs MOS experiment data in strong accumulation and depletion regions. The model can be also applied to explain the stretch-out *C-V* curve in the MOS devices.

4.2 The Distributed Bulk-Oxide Traps Model

In metal-oxide-semiconductor (MOS) device, traps in the bulk gate insulator film can interact with mobile carrier in the semiconductor bands via tunneling mechanism. **Fig. 4.1** schematically demonstrates the tunneling mechanism between border traps and conduction band of n-type semiconductor in the accumulation bias. The time constant associated with charge exchange between border traps and semiconductor is dominated by tunneling mechanism that has exponential dependence on the trap distance *x* from the gate dielectric/semiconductor interface [9-13].

$$\tau(x) = f_0 \tau_0 e^{2\kappa x} \tag{3.1}$$

Here, $\tau_0 = (n_s \sigma v_{th})^{-1}$ is the time constant of the interface trap inversely proportional to the carrier density of the semiconductor surface n_s, σ is the cross-sectional area of the trap, and v_{th} is the carrier thermal velocity. For the other parameters in (3.1) as follows: f_0 is the Fermi-Dirac function which a trap occupied by an electron at energy *E*, and κ is the attenuation coefficient for an energey *E* wavefunction of an electron decaying due to an energy barrier $E_{c,ox} > E$

$$\kappa = \sqrt{2m^*(E_{c,ox} - E)}/\hbar \tag{3.2}$$

m^* is the electron effective mass in the gate dielectric film, and $E_{c,ox}$ is the top energy of the gate dielectric band (tunneling barrier), as shown in **Fig. 4.1**.

For a given DC bias, the bulk-oxide traps at a certain distance x and energy E change occupancy respond with a small-signal AC modulation. The bulk-oxide traps at energy E ~ E_f are most accountable for the small-signal response in capacitance and conductance. We find that the effects of the bulk-oxide traps at particular depth and energy on the small-signal MOS admittance can be modeled by a series of combining capacitance and conductance. Bulk-oxide traps in an incremental depth Δx at x and incremental energy ΔE at E are symbolized by the incremental capacitance $\Delta C_{bt}(E, x)$ and the incremental conductance $\Delta G_{bt}(E, x)$ which are linked in series. If the bulk-oxide traps density per volume per energy is N_{bt} in units of $eV^{-1}cm^{-3}$, then [7], [9]

$$\Delta C_{\mathrm{bt}}(E,x) = \frac{f_0(1-f_0)q^2 N_{\mathrm{bt}}}{kT}\,\Delta E\,\Delta x \tag{3.3}$$

$\Delta C_{bt}(E, x)$ and $\Delta G_{bt}(E, x)$ have the relationship in time constant $\tau(x)$

$$\Delta C_{bt}(E,x) \,/\, \Delta G_{bt}(E,x) = \tau(x) = f_0\tau_0 e^{2\kappa x} \tag{3.4}$$

In order to integrate for a continuous energy distribution of bulk-oxide traps, incremental capacitance $\Delta C_{bt}(E, x)$ and incremental conductance $\Delta G_{bt}(E, x)$ in serial connection at a given depth x and energy E must be transfer to the incremental admittance $\Delta Y_{bt}(E, x)$. For the factor $f_0(1\text{-}f_0)$ is peaked sharply at $E = E_f$, So the total incremental admittance at depth x is

$$\begin{aligned}\Delta Y_{\mathrm{bt}}(x) &= \int_E \frac{1}{\frac{1}{j\omega\Delta C_{\mathrm{bt}}(E,x)}+\frac{1}{\Delta G_{\mathrm{bt}}(E,x)}} \\ &= \frac{q^2 N_{\mathrm{bt}}\ln(1+j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}}\Delta x\end{aligned} \tag{3.5}$$

Due to a continuous energy distribution of the bulk-oxide trap throughout the gate dielectric thickness, the equivalent circuit of the distributed model in the MOS device

is introduced in **Fig. 4.2**, where the gate dielectric capacitance is divided into an infinite number of serial slices with branches of $\triangle Y_{bt}(x)$ at different depth x in connection. And here, ϵ_{ox} is the permittivity of the gate dielectric and C_s is the semiconductor capacitance.

If we define $Y(x)$ to be the equivalent admittance at the arbitrary point x looking into the semiconductor in **Fig. 4.2**, the admittance of the next point $x + \triangle x$ is

$$Y(x + \Delta x) = \Delta Y_{\mathrm{bt}}(x) + \frac{1}{\frac{\Delta x}{j\omega\epsilon_{ox}} + \frac{1}{Y(x)}} \tag{3.6}$$

To substitute (3.5) for $\triangle Y_{bt}(x)$, the first order terms in $\triangle x$ then yield a differential equation for $Y(x)$

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\epsilon_{ox}} + \frac{q^2 N_{\mathrm{bt}} \ln(1 + j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}} \tag{3.7}$$

There are two boundary conditions, as follows two equations:

$$\begin{cases} Y(x = 0) = j\omega C_s & (3.8) \\ Y(x = t_{ox}) \equiv G_{\mathrm{tot}} + j\omega C_{\mathrm{tot}} & (3.9) \end{cases}$$

Generally, (3.7) needs to be solved numerically to acquire the total admittance seen into semiconductor by gate terminal, that is (3.8).

For typical measurement frequencies of 1 kHz - 1 MHz, 1.4 x 10^{-6} < $\omega\tau_0$ < 1.4 x 10^{-3}, C_{tot} varies with $\ln(1/\omega)$ linearly, and G_{tot} varies with ω, i.e., G_{tot} / ω ~ constant. Constant G_{tot} / ω indicate that, for a given bias, the response of the bulk-oxide traps cause a wide dispersive spectrum of frequency in account of their various depth distribution, that is, an obvious distinction from conventional interface traps [7]. For a given frequency of $\omega < 1/\tau_0$, the depth of the bulk-oxide traps that respond to the AC small-signal can be estimated by making the factor $\omega\tau_0 e^{2\kappa x}$ in (3.7) to be unity, that is, $x \sim (2\kappa)^{-1} \ln(1/\omega\tau_0)$, which is almost in the range of 0.1~1nm typically.

For ω = 0 or DC, **Fig. 4.2** becomes a purely capacitive circuit model, and (3.7) is reduced to a real part equation for $C(x)$, that is

$$\frac{dC}{dx} = -\frac{C^2}{\epsilon_{ox}} + q^2 N_{\text{bt}} \tag{3.10}$$

The boundary condition is $C(x=0) = C_s$. For uniform distribution of N_{bt}, (3.10) can be analytically resolved to yield

$$C(x) = C_0 \frac{(C_s + C_0)\exp\left(2qx\sqrt{\frac{N_{\text{bt}}}{\epsilon_{ox}}}\right) + (C_s - C_0)}{(C_s + C_0)\exp\left(2qx\sqrt{\frac{N_{\text{bt}}}{\epsilon_{ox}}}\right) - (C_s - C_0)} \tag{3.11}$$

Here, $C_0 = q\sqrt{\epsilon_{ox} N_{\text{bt}}}$. If $2q\sqrt{\epsilon_{ox} N_{\text{bt}}} >> 1$, then $C(x = t_{ox}) \approx \sqrt{q^2 \epsilon_{ox} N_{\text{bt}}}$, which is insensitive to C_s. Of course, this is just only a matter of theoretical interest, however, it would take much longer than the age of the universe to charge up all the bulk-oxide traps in the gate dielectric in practice.

Another interest of the case is in strong accumulation where C_s is very high. From (3.11), $C_{\text{tot}}(\text{DC}) \approx C_0 \coth(C_0/C_{\text{ox}})$, is higher than C_{ox} always. This result is in comparison of the interface state or lumped-circuit border traps model, which don't generate dispersive spectrum as shorted out by large semiconductor capacitance (C_s). Therefore, frequency dispersion of capacitance-voltage and conductance-voltage characteristics in accumulation region is a great indicator of distributed bulk-oxide traps.

It is introduced that the parasitic series resistance with the capacitor might let the apparent C_{tot} lower at high frequencies regions, e.g., 1 MHz so on. We exclude it out as the cause of the frequency dispersion in the measured *C-V* curve for the dispersive curve still exist as low frequencies as a few kHz, where the parasitic series resistance has no effect on it. Moreover, the estimated spreading resistance in the substrate for about 100 μm dot size is less than a few ohms, which is several orders of magnitude smaller than the capacitive reactance at around 1 MHz.

4.3 Correlation of the Model with Multi-frequency *C-V* and *G-V* Experimental Data in Strong Accumulation and Depletion Regions

The experimental capacitance and conductance data versus multi-frequency in strong accumulation regime, of the sample TMA+HfO_2 100cyc./n-InAs at bias V_g=3V are contrasted to the model computations in **Fig. 4.3**. For the parameters of the model, semiconductor capacitance C_s is chosen for the serial combination of C_{ox} and C_s which gives C_{tot} slightly below the measured 1 MHz capacitance data at V_g=3V. The slopes of C_{tot} versus $\ln(1/\omega)$ and G_{tot} versus ω are both very sensitive to the density of bulk-oxide traps N_{bt}. By choosing several parameters, such as N_{bt}, τ_0, C_s, ϵ_{ox}, and κ, are valued 14 x 10^{19} ($eV^{-1}cm^{-3}$), 1 x 10^{-7} (s), C_s = 1.67 x 10^{-6} ($\mu F/cm^{-2}$), 17, 3.8 (nm^{-1}) as initial guess, which have great match between the model and the measured C_{tot} and G_{tot} data from 1 kHz to 1 MHz in **Fig. 4.3 (a)** and **(b)**. The parameters of gate dielectric thickness t_{ox} is determined by TEM image, and τ_0 is chosen so that C_{tot} is agreeing with the equivalent series capacitance $C_{ox}C_s/C_{ox}+C_s$ for the frequency condition $\omega\tau_0 \sim 1$, where the bulk-traps have no effect on *C-V* and *G-V* characteristics. Note that the agreement between of model and experiment data is sensitive to the initial guess. The final extraction data is shown in **Table. 4.1**.

Fig. 4.4 (a) and **(b)** demonstrates the model correlation with the experiment *C-V* and *G-V* data in depletion region, i.e., in the region of a steep *C-V* curve transition, at the bias of V_g=0.3V. We observe that a lower bulk-oxide traps density is found to fit capacitance- and conductance-frequency experiment data. The exact data of extraction is shown in **Table. 4.2**.

Fig. 4.5 (a) ~ (c) shows the converted *C*-*V* map of total experimental *C*-F data for TMA+HfO_2 100cyc./n-InAs at the frequency 1 kHz ~ 100 kHz, as well as **Fig. 4.6 (a) ~ (c)** shows the converted *G*-*V* map of total experimental *G*-F data for TMA+HfO_2 100cyc./n-InAs at the frequency 1 kHz ~ 100 kHz compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 3V. The parameter of the extraction in N_{bt} is indicated in **Table. 4.3**. Furthermore, **Fig. 4.7** and **Fig. 4.8** display the converted *C*-*V* map of total experimental *C*-F data for TMA+Al_2O_3 100cyc./n-InAs and TEMAH+HfO_2 100cyc./n-InAs at the frequency 1 kHz ~ 100 kHz, respectively. Note that N_{bt} of the TMA/Al_2O_3 capacitors are extracted in C_s = 0.75 μ F/cm^2, but those of the TEMAH/HfO_2 and TMA/HfO_2 capacitors are extracted in C_s = 1.3 μ F/cm^2. We find the trend between $\triangle$C in **Table. 2.1** and N_{bt} in **Table. 4.3** are in good agreement.

Moreover, **Fig. 4.9** to **Fig. 4.13** demonstrate the converted *C*-*V* map of total experimental *C*-F data for TMA+ HfO_2 60cycles, for the condition of w/o plasma, 2cyc./plasma, 4cyc./plasma, 8cyc/plasma, and final post-deposition plasma treatments, respectively. The parameter of the extraction in N_{bt} is shown in **Table. 4.4**. Note that the extracted N_{bt} of the all the condition is in C_s = 1.4 μ F/cm^2. We still observe the trend for $\triangle$C in **Table. 3.1 ~ Table. 3.3** and N_{bt} in **Table. 4.4** are in good consistency.

Our study has indicated that charging and discharging of the bulk-oxide traps at the frequency of 1kHz – 1 MHz can be explained by an elastic-tunneling based model adequately. But recent reports on reliability of thin-film dielectrics by bias-temperature stress using random telegraph noise and time-dependent defect spectroscopy techniques has revealed inconsistency of trap emission and capture with the elastic-tunneling model [14]-[17]. It is not obvious whether the dissimilitude is in account of different stress processes and characterization techniques.

4.4 Summary

In Chapter 4, we modeled the bulk-oxide traps equivalent circuit for the tunneling mechanism which is responsible for the dispersive experiment data in *C-V* and *G-V* curve. It differs from the conventional interface state model due to its high trap characteristic frequency. The model is valid with all the experiment data in the strong accumulation and depletion regions. As not same as the interface states, which are in unit of areal density, the bulk-oxide traps in unit of volume density, and that can be extracted from the fitting method by inputting the experiment capacitance and conductance dispersive data. The result of the extraction in border traps density N_{bt}, which have the similar trend comparing with the above mentioned definition of frequency dispersion $\triangle C$ in **chapter 2** and **chapter 3**.

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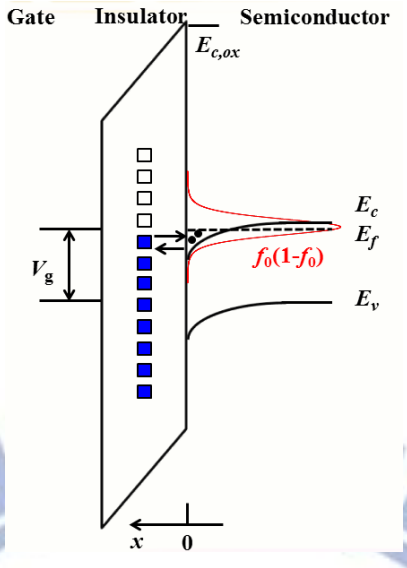


Fig. 4.1 Schematic of tunneling mechanism between bulk-oxide traps in the gate dielectric and conduction band of the semiconductor.

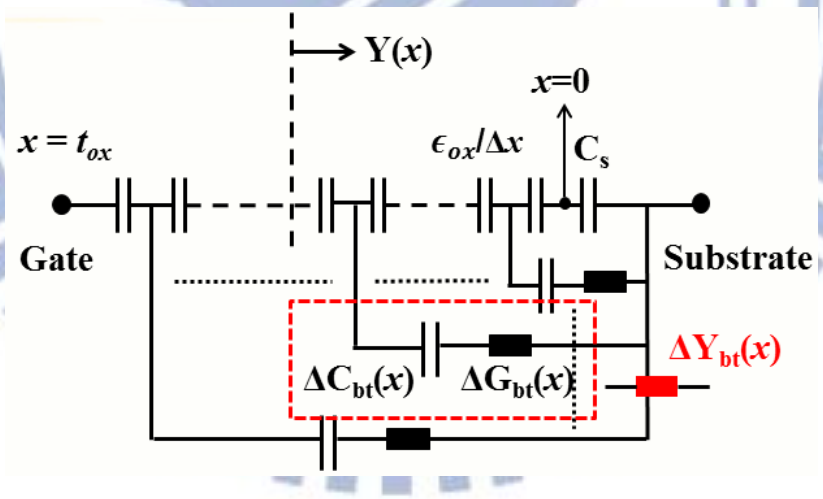
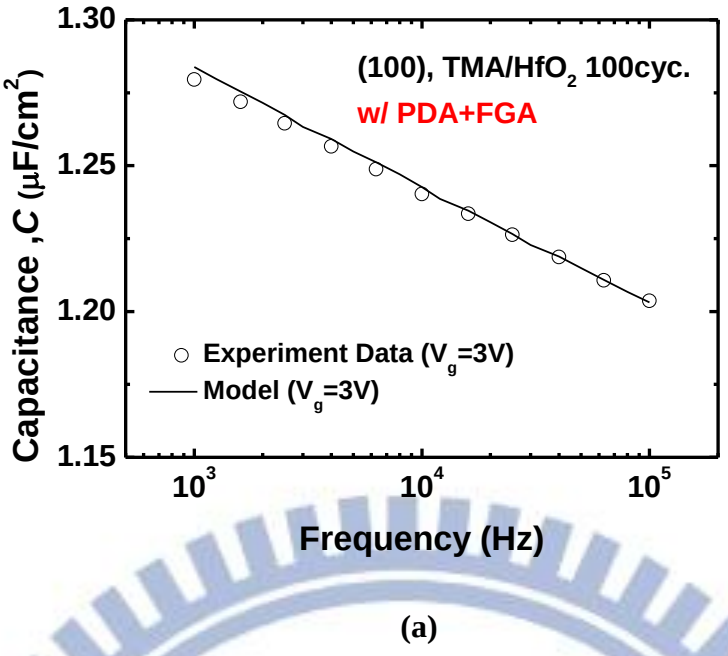
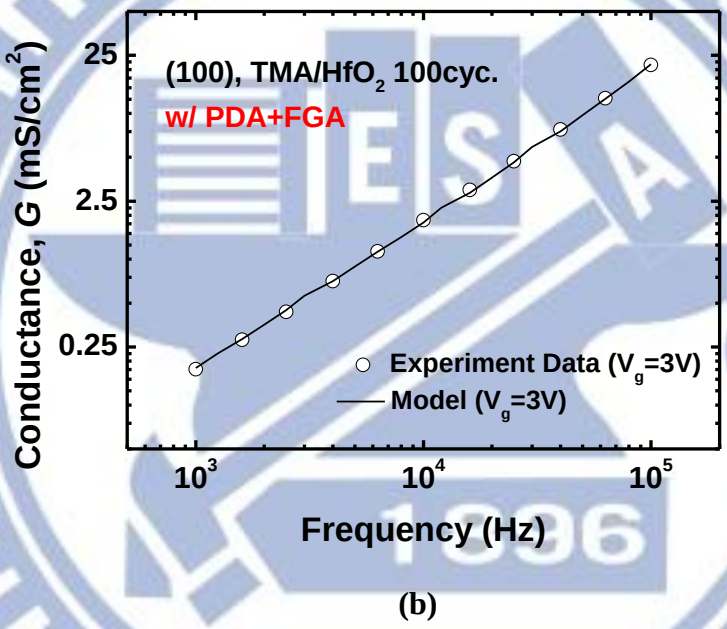


Fig. 4.2 Equivalent circuit for bulk-oxide traps distributed over the depth of the gate dielectric. The semiconductor capacitance is represented by C_s.



(a)

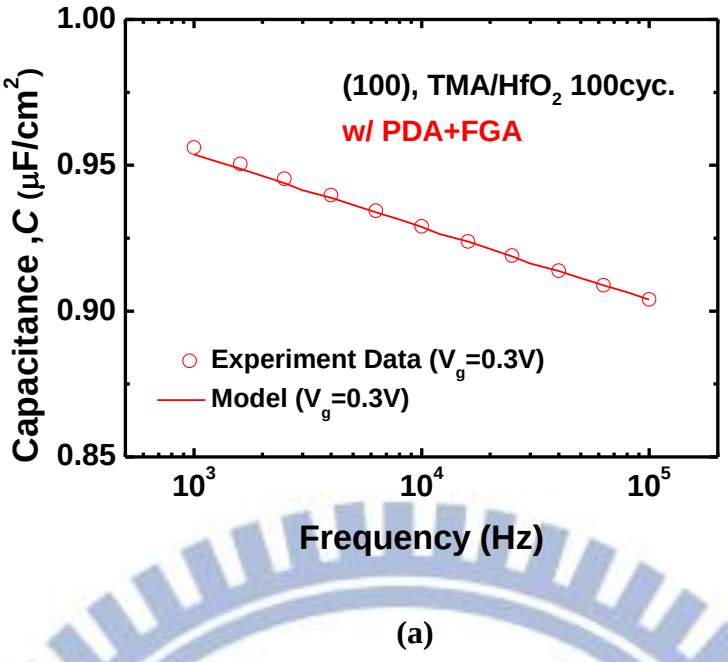


(b)

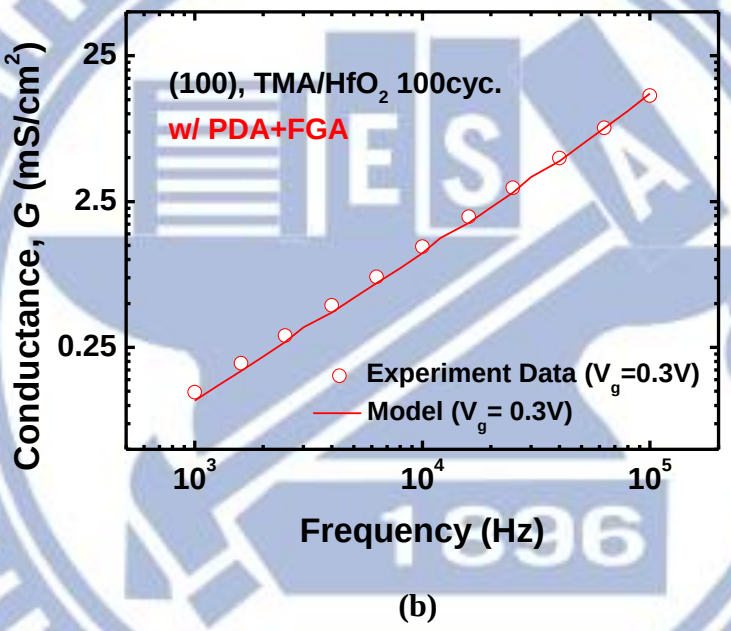
Fig. 4.3 Experimental (a) C_{tot} (F) and (b) G_{tot} (F) frequency dispersion data of TMA+HfO_2 100cyc./n-InAs (open circles) at V_g = 3V compared to those calculated from the distributed border trap model (solid lines).

	N_{bt} ($10^{19}eV^{-1}cm^{-3}$)	τ_0 ($10^{-7}s$)	C_s ($\mu F/cm^2$)	ϵ_{ox}	κ (nm^{-1})
V_g = 3V	13.0	1.05	1.85	17.0	3.51

Table. 4.1 The parameters of extraction for TMA+HfO_2 100cyc./n-InAs at the bias of V_g = 3V.



(a)



(b)

Fig. 4.4 Experimental (a) C_{tot} (F) and (b) G_{tot} (F) frequency dispersion data of TMA+HfO_2 100cyc./n-InAs (open circles) at Vg = 0.3V compared to those calculated from the distributed border trap model (solid lines).

	N_{bt} ($10^{19}eV^{-1}cm^{-3}$)	τ_0 ($10^{-7}s$)	C_s ($\mu F/cm^2$)	ϵ_{ox}	κ (nm^{-1})
V_g = 0.3V	6.92	1.89	1.16	17.0	5.10

Table. 4.2 The parameters of extraction for TMA+HfO_2 100cyc./n-InAs at the bias of V_g = 0.3V.

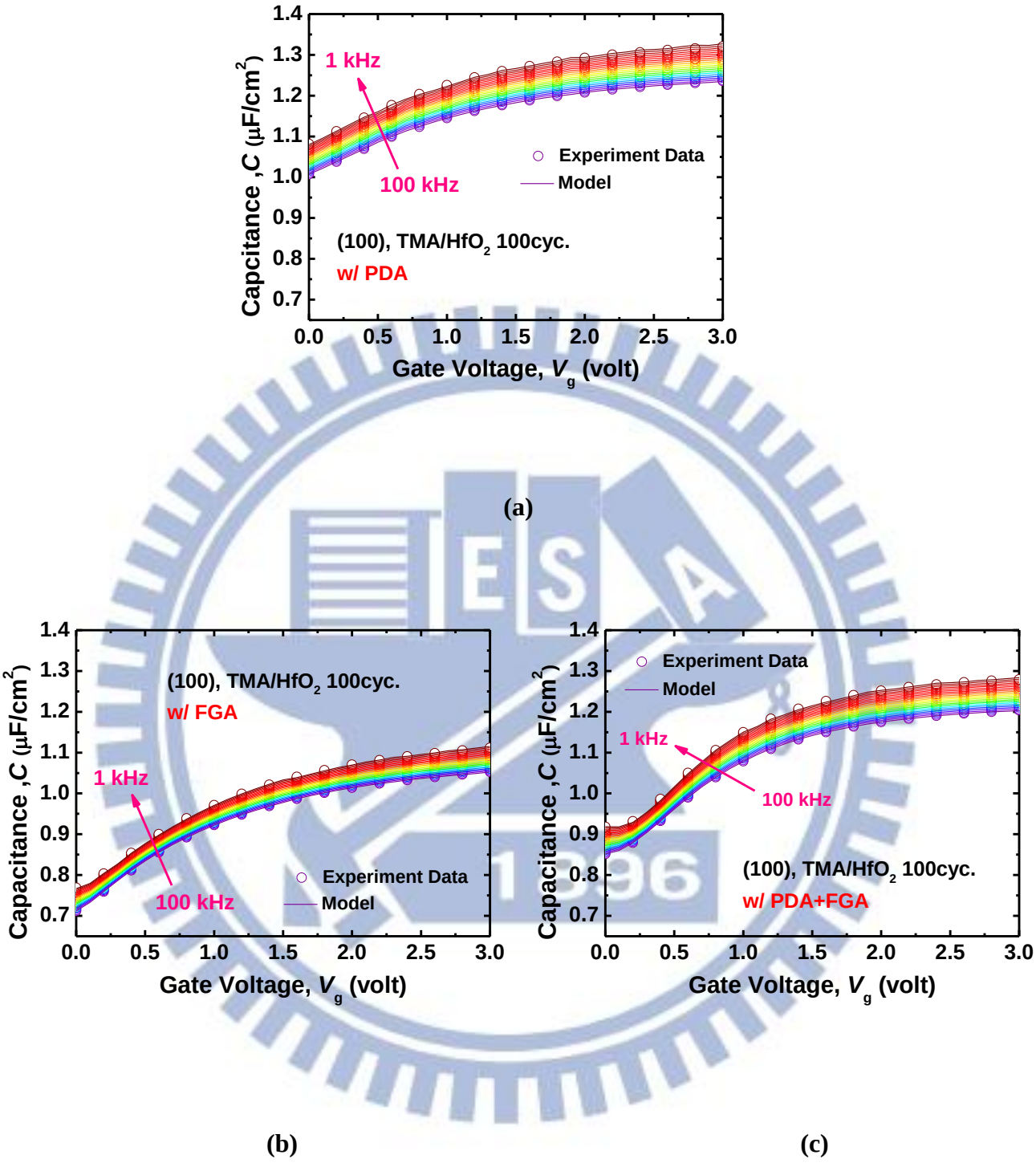


Fig. 4.5 The converted *C*-*V* map of total experimental *C*-F data for TMA+HfO_2 100cyc./n-InAs at the frequency 1 kHz ~ 100 kHz (a) w/ PDA; (b) w/ FGA; (c) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 3V.

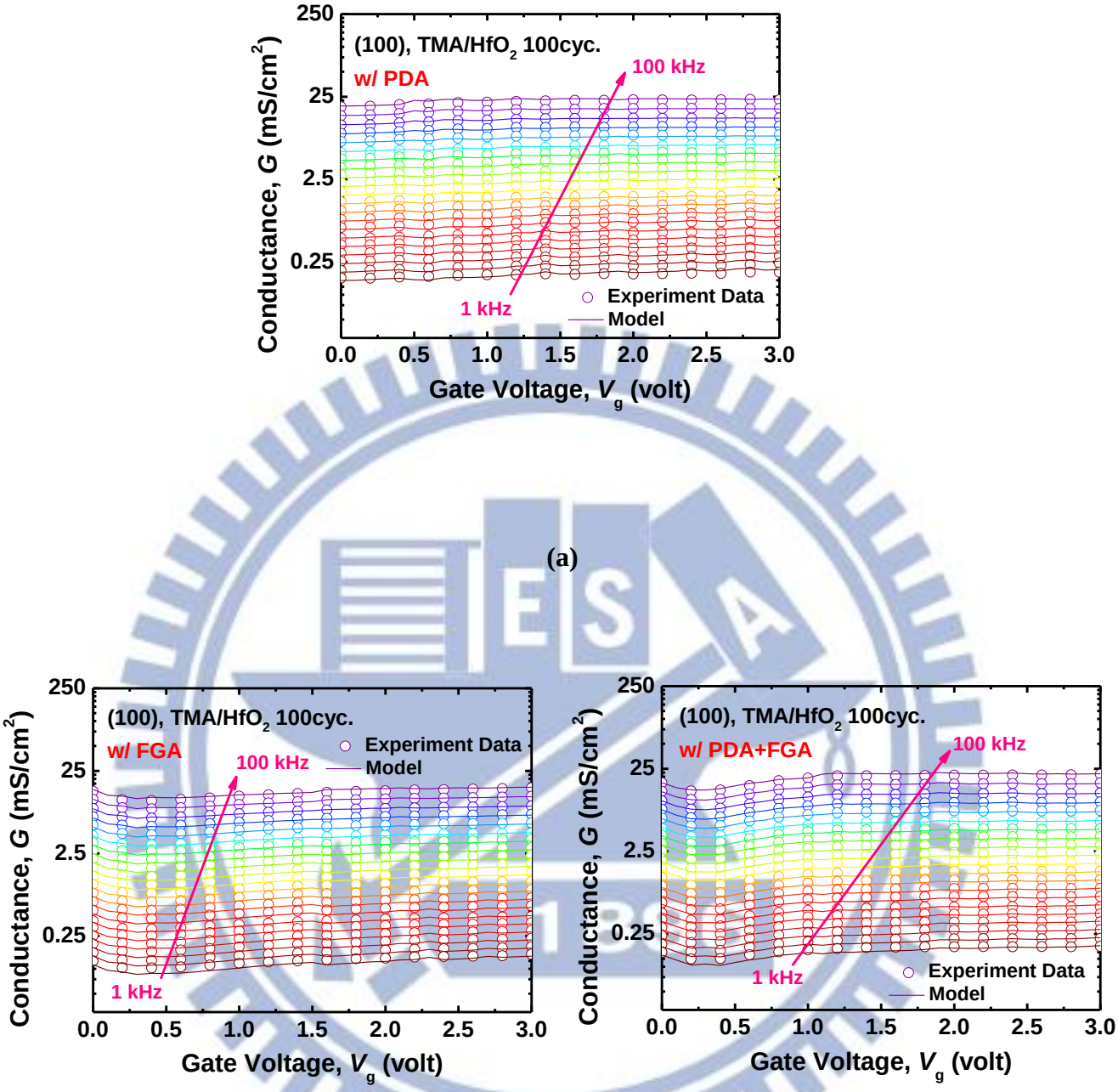


Fig. 4.6 The converted *G*-*V* map of total experimental *G*-F data for TMA+HfO_2 100cyc./n-InAs at the frequency 1 kHz ~ 100 kHz (a) w/ PDA; (b) w/ FGA; (c) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 3V.

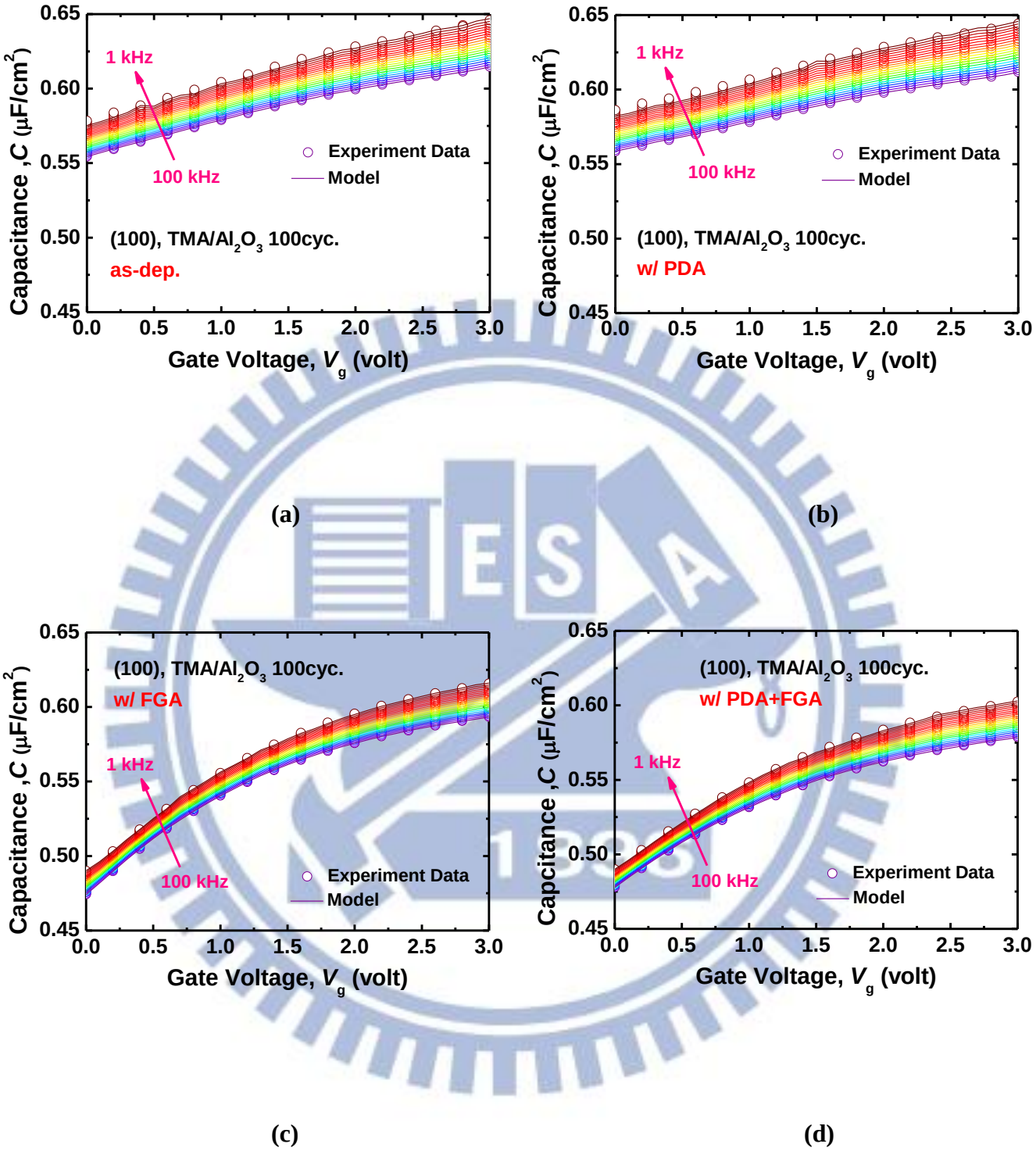


Fig. 4.7 The converted *C*-*V* map of total experimental *C*-F data for TMA+Al_2O_3 100cyc./n-InAs at the frequency 1 kHz ~ 100 kHz (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 3V.

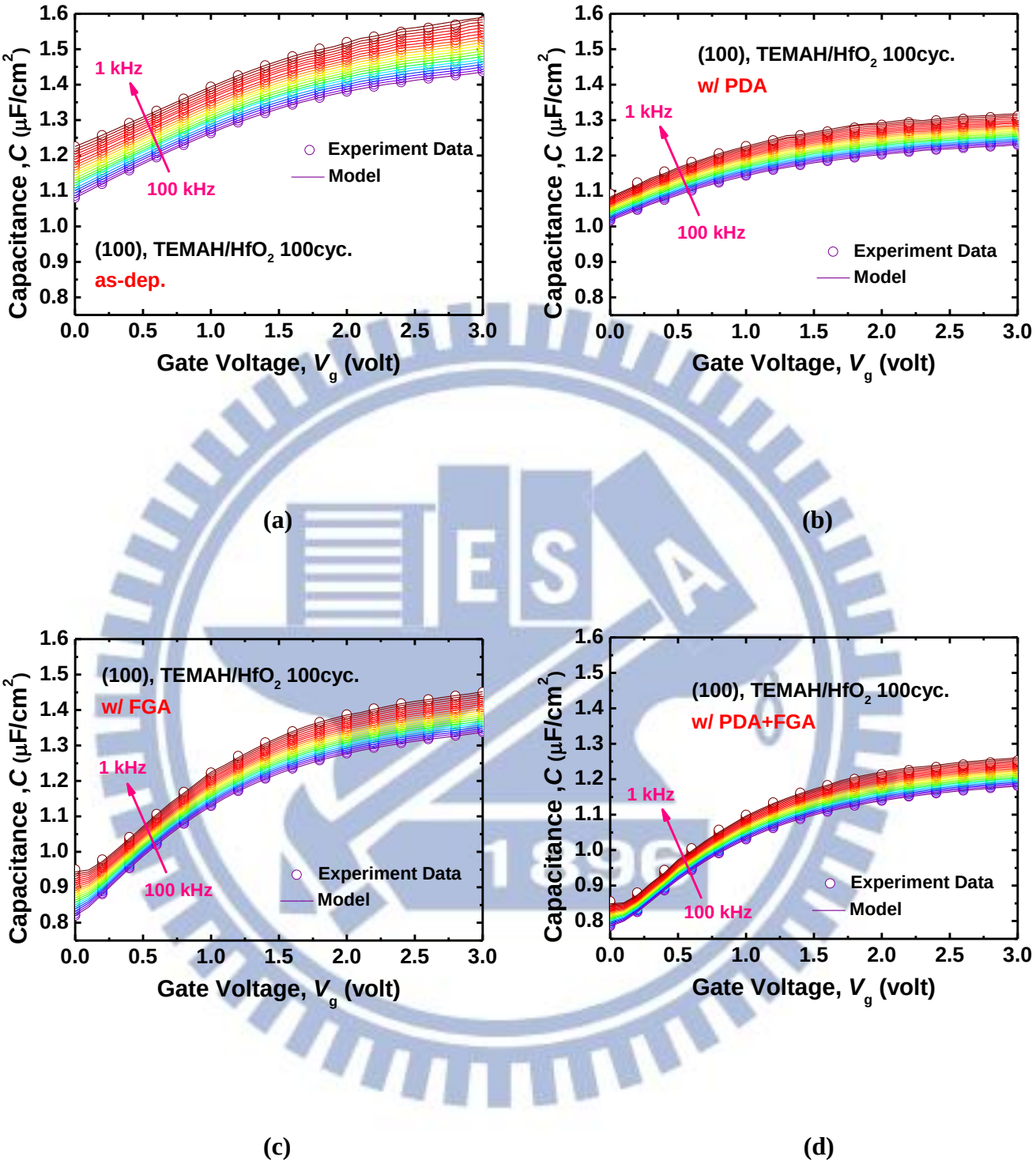


Fig. 4.8 The converted *C*-*V* map of total experimental *C*-F data for TEMAH+HfO_2 100cyc./n-InAs at the frequency 1 kHz ~ 100 kHz (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 3V.

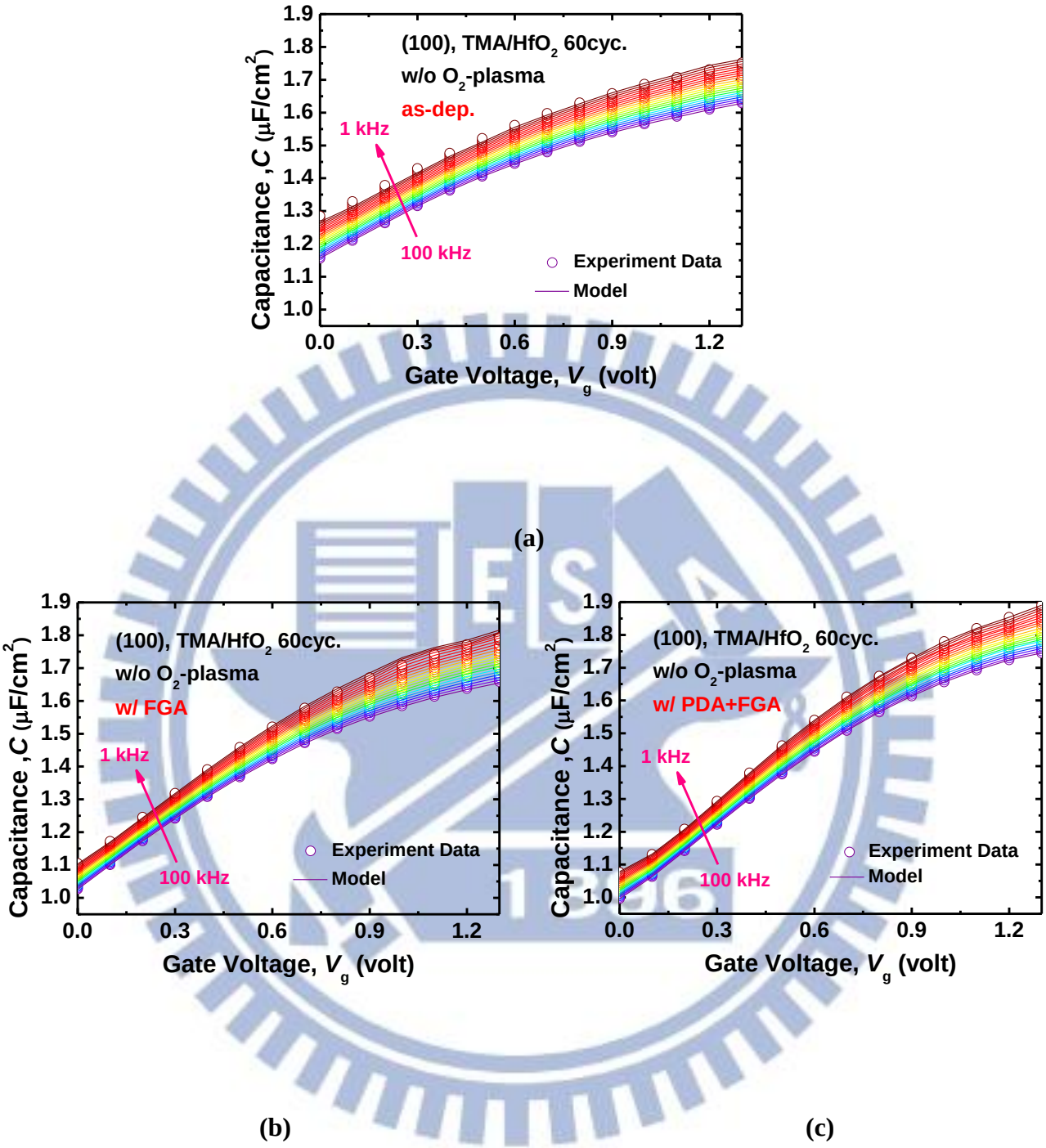


Fig. 4.9 The converted *C*-*V* map of total experimental *C*-F data for TMA+HfO_2 60cyc./n-InAs w/o plasma at the frequency 1 kHz ~ 100 kHz (a) as-deposited; (b) w/ FGA; (c) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 1.3V.

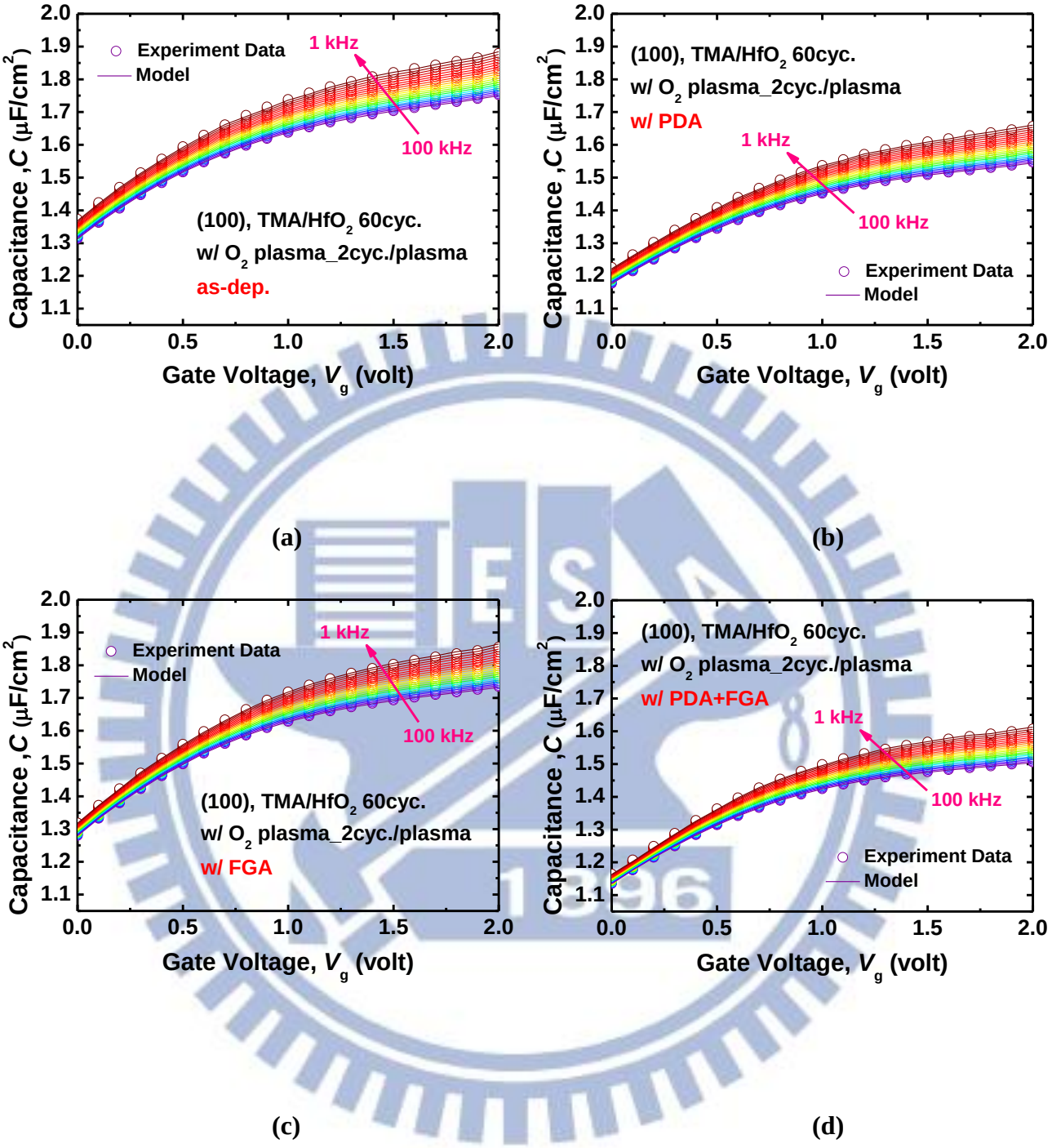


Fig. 4.10 The converted *C*-*V* map of total experimental *C*-F data for TMA+HfO_2 60cyc./n-InAs 2cyc./plasma at the frequency 1 kHz ~ 100 kHz (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 2V.

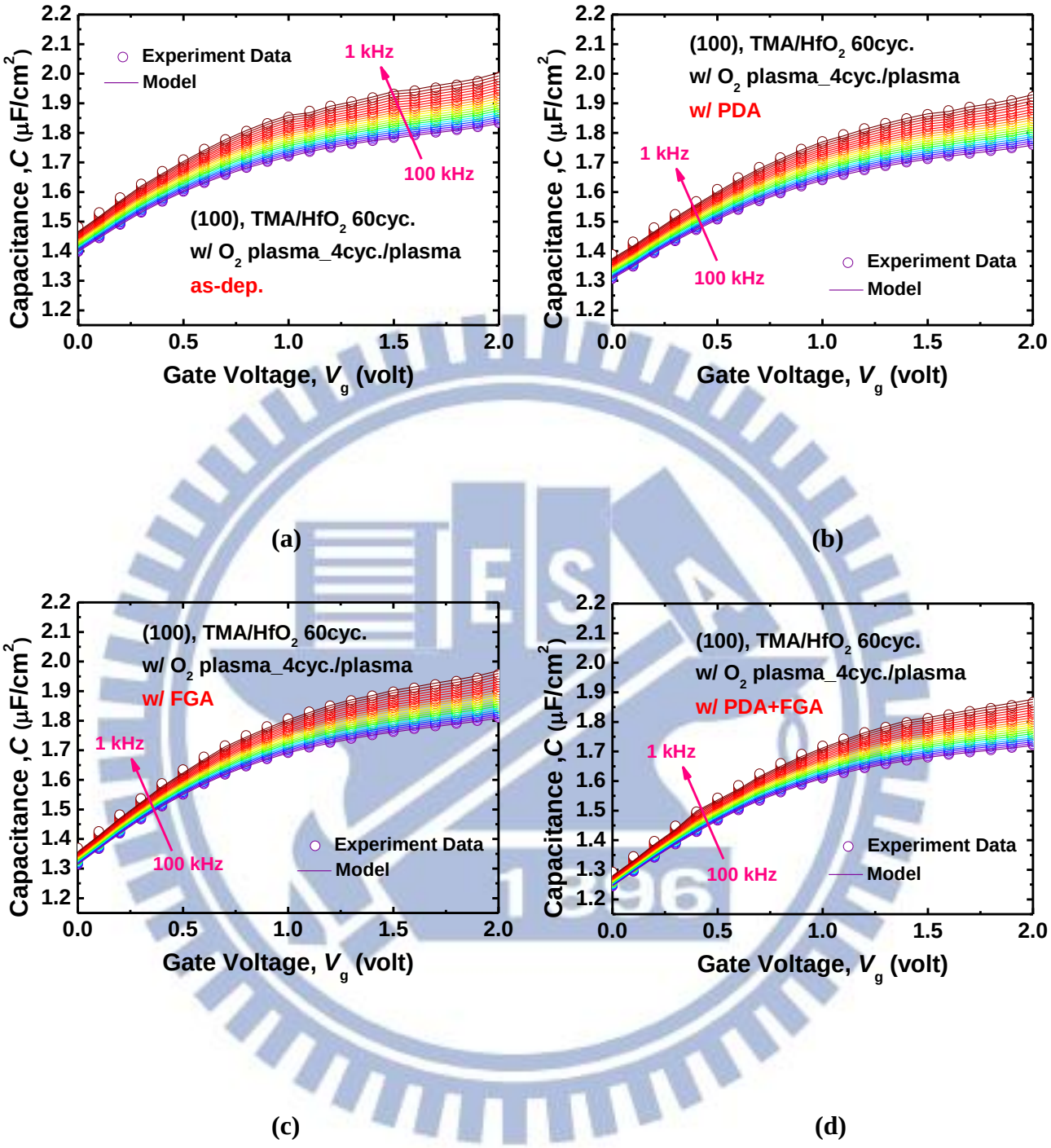


Fig. 4.11 The converted *C*-*V* map of total experimental *C*-F data for TMA+HfO_2 60cyc./n-InAs 4cyc./plasma at the frequency 1 kHz ~ 100 kHz (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 2V.

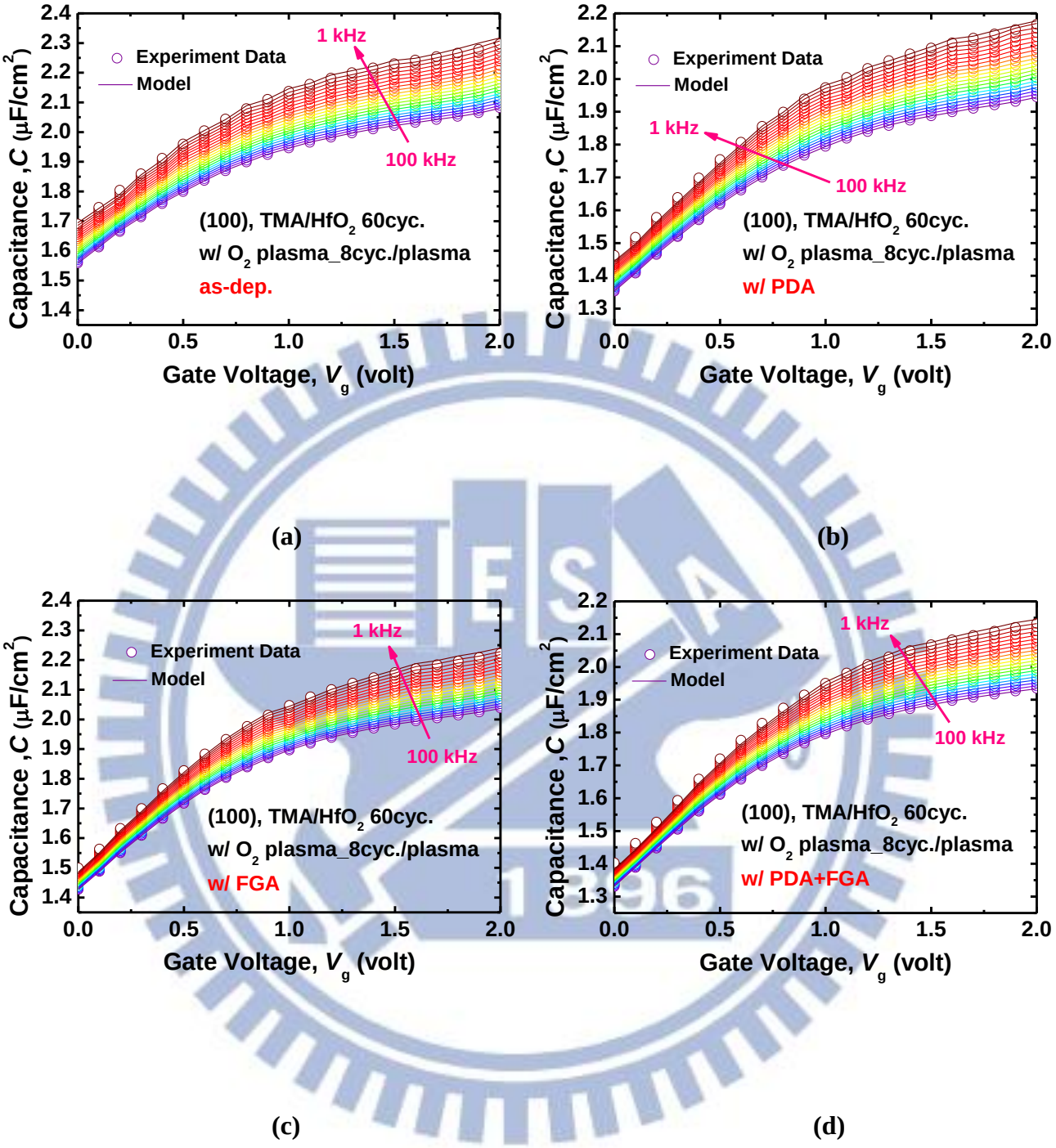


Fig. 4.12 The converted *C*-*V* map of total experimental *C*-F data for TMA+HfO_2 60cyc./n-InAs 8cyc./plasma at the frequency 1 kHz ~ 100 kHz (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 2V.

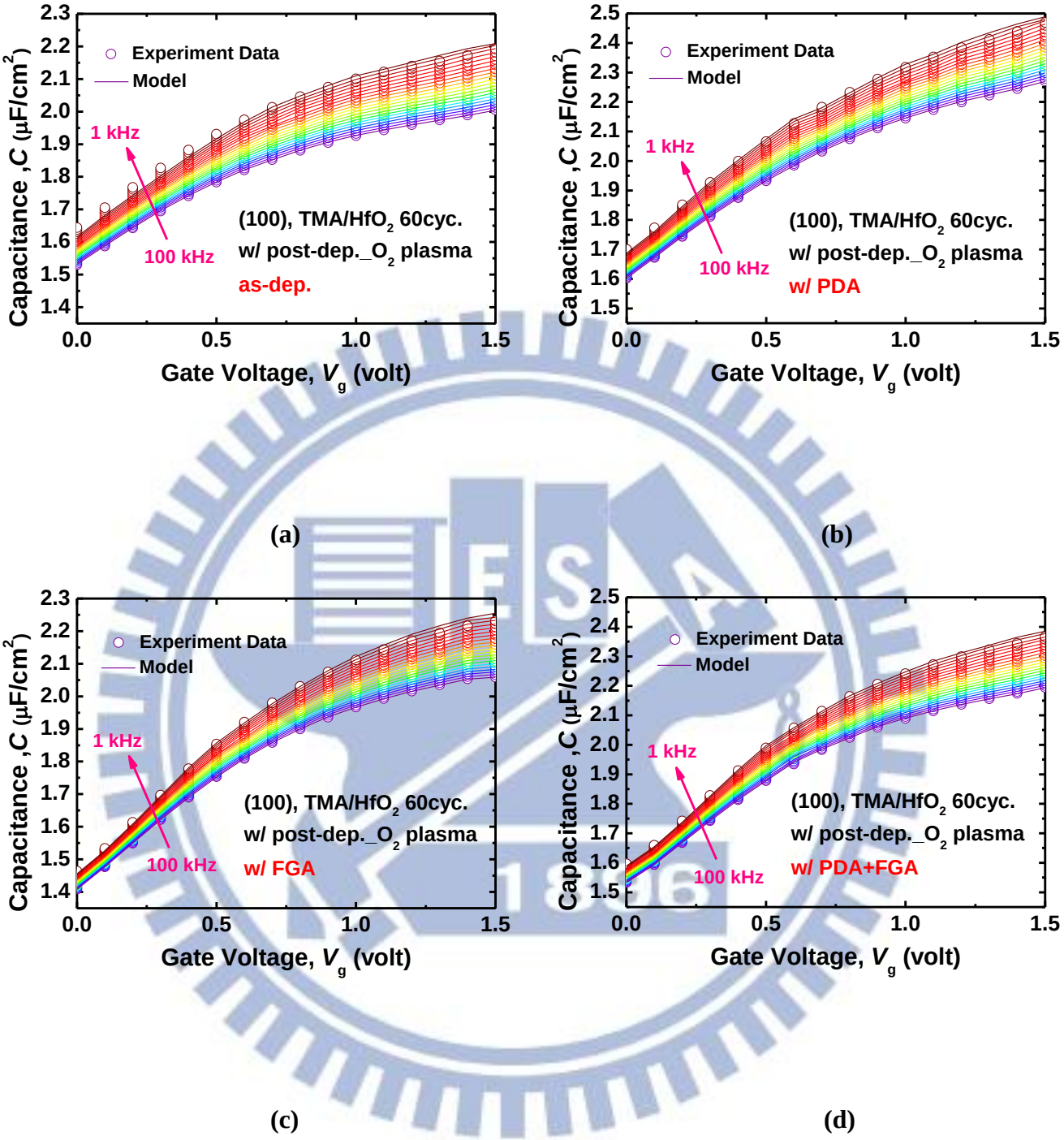


Fig. 4.13 The converted *C*-*V* map of total experimental *C*-F data for TMA+HfO_2 60cyc./n-InAs post-deposition_plasma treatment at the frequency 1 kHz ~ 100 kHz (a) as-deposited; (b) w/ PDA; (c) w/ FGA; (d) w/ PDA+FGA compared to those calculated from the distributed border trap model for the bias V_g = 0V ~ V_g = 1.5V.

N_{bt} ($10^{19}eV^{-1}cm^{-3}$)	As-dep.	w/ PDA	w/ FGA	w/ PDA+FGA
TMA/Al_2O_3	9.22	9.76	2.83	3.74
$TEMAH/HfO_2$	15.2	10.9	13.3	10.1
TMA/HfO_2		11.2	8.66	10.2

Table. 4.3 The overview of the extraction in border traps density N_{bt} for the all 100 cycles high-κ dielectrics.

N_{bt} ($10^{19}eV^{-1}cm^{-3}$)	As-dep.	w/ PDA	w/ FGA	w/ PDA+FGA
w/o plasma	11.45		11.6	11.9
2cyc./plasma	7.62	7.36	7.43	7.05
4cyc./plasma	9.01	9.15	7.72	7.94
8cyc./plasma	10.3	10.9	9.17	9.56
post-dep. O_2-plasma	9.43	10.2	7.35	9.40

Table. 4.4 The overview of the extraction in border traps density N_{bt} for the all 60 cycles high-κ dielectrics.

Chapter 5

Conclusions and Suggestions for Future Research

5.1 Conclusions of This Study

In this thesis, we have studied the deposition of various high-*k* dielectrics, including Al_2O_3, and HfO_2 in combination with "self-cleaning". We first utilized two precursors to passivate the surface of InAs, which are trimethyl aluminum [TMA, $Al(CH_3)_3$] and tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf(N(C_2H_5)(CH_3))_4$]]. After depositing the high-*k* films, two-kinds of post-deposition thermal process, like post-deposition annealing (400℃/120s) and forming gas annealing (300℃/30min.), were employed to examine the influence on the electrical properties of InAs MOS capacitors. We discovered that the effect of post-deposition annealing on different gate dielectrics is not apparent, however, forming gas annealing (FGA) is the key thermal process to improve the electrical characteristics on frequency dispersion and gate control ability. And we adopted the optimum gate dielectric, TMA/HfO_2, with InAs to study further due to its high C_{max} and weak frequency dispersion.

Next, we applied the various plasma density treatments, 2cyc/plasma, 4cyc./plasma, 8cyc./plasma, and post-deposition plasma treatment on the thermal atomic-layer-deposition process. We expected that the plasma treatments can improvement high-*k* dielectric quality. From the capacitance data, it is found that not only high-*k* dielectric but also high-*k* dielectric/InAs interface quality much improved

by high plasma density treatment, especially for 2cyc./plasma treatment. Also, we still employed post-deposition annealing, PDA, (400℃/120s) and forming gas annealing, FGA, (300℃/30min.). The impact of post-deposition annealing on different gate dielectrics is not clear, but forming gas annealing (FGA) is effective to further reduce frequency dispersion in accumulation and depletion regimes.

In account of long time constant, the cause of frequency dispersion at the high gate bias is known as the bulk-oxide traps (border traps). A distributed bulk-oxide traps model based on tunneling between the semiconductor surface and trap states in gate dielectric is developed. We established a circuit model to explain the mechanism. Some of the calculated parameters in the model are sensitive to the initial guess. Then we fitted the calculations of model with experimental data, capacitance- and conductance-voltage curve. Finally we can quantitatively determine the bulk-oxide traps density N_{bt}. To compare with the above mentioned ΔC we defined, they are in good consistency for the data of each sample we fabricated.

5.2 Suggestions for Future Research

While metal/high-*k* dielectric/InAs MOS gate stacks are able to meet ITRS requirements for EOT and leakage current, to reduce interface states density is still a critical problem. A number of researches exist on InAs surface pretreatments including HCl- and sulfur-based methods. In addition, thermal process such as annealing is indicated to have a critical impact on InAs MOS capacitors characteristics in this work and the others. Once a metal/high-*k* dielectric/InAs fabrication process is optimized by high-k dielectric film, surface pretreatment, and annealing condition, the ultimate goal is to fabricate InAs MOSFETs.

InAs MOSFETs allow the use of extra characterization techniques. A MOSFET device in which source and drain region are formed by ion implantation enables to utilize the split *C-V* method, which can distinguish between the capacitance contribution of electron and hole. The split *C-V* method is commonly applied to extract the carrier mobility. The structure also allows for inversion-mode MOSFETs to be examined, enabling benchmarking of the high-*k* dielectric/InAs in terms of common FET metrics such as trans-conductance and drain current, and providing the verification of the formation of a true inversion layer in InAs.

Note that self-aligned process is a key step for the development of MOSFETs with very small-scaled gate technology node in VLSI generation. The silicon CMOS can achieve its present small feature size, one of the critical platform is self-aligned process. However, it is not a simple method to fabricate self-aligned InAs MOSFETs. But, III-V can still be expected to serve as the key for ultra-short channel 3D MOSFETs generation.

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碩士論文題目:

利用介面鈍化與電漿處理對原子層沉積二氧化鉿/砷化銦金氧半電容之研究

Investigation of Atomic-Layer-Deposition HfO_2/InAs Metal-Oxide–Semiconductor Capacitors with Interfacial Passivation and Plasma Treatments