影像式紅外線偵檢像素縮小化製程開發

研究生: 羅俊傑　　指導教授: 張國明博士

國立交通大學電子工程學系電子研究所

摘要

針對未來中波長 3 至 5 微米紅外線影像感測應用上高解析度、高像素的要求，本論文研究如何將銻化銦二極體元件尺寸縮小化之相關製程技術，如 p+n 二極體表面批覆技術、隔離元件之平台蝕刻技術、及以離子植入法製作小尺寸二極體元件技術等。

為了達到提高影像解析度及增加像素之目標，位於光學系統焦面上，以二維分佈之陣列型感測元件之像素單元尺寸大小勢將朝縮小化方向發展；本篇論文利用一種由陽極氧化法及低溫光化學氣相沉積法所組合之雙層薄膜作為披覆層，以控制銻化銦p+n二極體元件接面週邊N傳導型表面處於弱反相區，避免一般採用具有正電荷分佈之單一CVD氧化層因感應表面電位為累積區而形成p^+n^+ 增強電場及增加漏電流的問題；這種堆疊而成之披覆層對銻化銦二極體元件表面電位效應，使得元件暗電流被控制在一個相對較低且穩定的工作區域，二極體元件將不需要額外閘控結構設計，此種堆疊而成之披覆層優點不僅在大幅降低製程複雜性，更因結構之簡化而得以縮減像素單元尺寸大小。

為了縮小像素單元尺寸大小，對於隔離二維影像感測元件之平台蝕刻製程所

導致元件結構均勻性問題，本論文研究檸檬酸/雙氧水混合溶液對銻化銦的蝕刻機制，發現其與傳統乳硝酸溶液不同；表面反應主控機制所產生隔離平台具有均勻性高、四邊及角結構對稱、側壁斜度較大、及高度易於控制等特點，對於後續表面披覆層及金屬鍍膜在平台階梯區域之覆蓋度有很大改善。電性上吾人以線型陣列元件測試結構，針對整片晶圓進行暗電流分佈測試，驗證以檸檬酸/雙氧水混合溶液製備元件之暗電流分佈具有較佳之均勻性，此結果證明了以檸檬酸/雙氧水混合溶液產生之平台結構較符合未來高密度陣列發展之需求。

為了達到縮小像素單元尺寸大小目的，除了結構要簡化，製程本身亦需簡化，以離子植入技術在銻化銦晶圓上形成接面製作二極體，由於精確的雜質濃度及植入深度控制，具有均勻性高及易於進行平面化製程等優點，因此對於縮小像素單元尺寸大小、增大像素密度，較傳統的固態擴散技術將更有優勢。然而離子植入造成的損傷及表面披覆技術的限制，使得以離子植入技術製作之p-n二極體在元件尺寸縮小化時，有元件性能退化及需要使用閘控結構調制元件表面電位之問題；本研究首次以兩種不同介電薄膜堆疊組成之絕緣結構層作為鈹離子植入銻化銦接面二極體之表面披覆層，並以實驗驗證元件接面面積小至 20×20 μm^2 之 R_0A已達到 7.6 $\times 10^4 \Omega$-cm^2；根據實驗數據及電路模型，吾人預估在元件接面面積小至 15×15 μm^2 之R_0A仍可達到 5 $\times 10^4$ Ω-cm^2水準。

關鍵字：焦面陣列、紅外線偵檢器、披覆膜、漏電流、 p+n、二極體、平台蝕刻、鈹離子植入、影像像素、p+n 接面。

Development of Small Pixel Infrared Detectors for Mid-Wavelength IR Imaging Applications

Student: Jiunn-Jye Luo. Advisor: Dr. Kow-Ming **Chang**

Department of Electronics Engineering & Institute of Electronics
National Chiao Tung University
Hsinchu, Taiwan, R.O.C.

Abstract

This thesis studies the scale-down process issues of InSb photodiodes to meet the high resolution and high format requirements of next generation medium-wavelength infrared image sensing applications. It includes the passivation of the p+n junction surface on InSb, the mesa etching process to create isolated sensing pixels, and the fabrication of scale-down p+n diodes by Beryllium ion implantation.

To achieve the goals of high resolution and high format in infrared imaging, the sensing pixels of the image array located on the focal plane of an image system will have to scale down to smaller size. In this study, a composite dielectric structure of anodic oxide and Photo-CVD oxide is used as the passivation layer on InSb diodes. The n-type surface at the junction peripheral will become depletion or weak inverted. By comparing with the characteristics of Photo-CVD oxide, the composite dielectric structure can help to get rid of the possibility of forming p^+n^+ regions, which may result in high electric field and high leakage current. The relatively low dark current of the InSb diodes passivated by the composite structure exclude the necessity of extra control-gate structure. This will help to simplify the fabrication processing; it will also help to reduce the dimension of the sensing pixel.

The mesa structures, isolated p+n junctions, formed by lactic acid/nitric acid traditionally will have challenging issue on its uniformity performance if the pixel size is scale-down. This study found that the etching mechanism of citric acid/peroxide is surface reaction-limited dominant. The advantages including mesa height uniformity, symmetry edges and corners in the etched mesa square, slope side-wall, and more controllable on the mesa height have proved its superior performance on the step coverage for the succeeding coating of dielectric or metal film. Electrically, we evaluate the distribution of dark current of test structure distributed on the wafer. These results indicate that citric acid/peroxide solution can get better performance in uniformity. It is then more suitable for the applications of next generation high density array

To reduce the pixel size, the fabrication processes should be simplified in addition to the simplification of device structure. Due to the embedded advantages of accurate dopant and junction depth control in the implantation technology, the InSb p+n diodes in the array will get higher uniformity and easier implementation to planar device structure. These advantages will help to reduce the pixel size, and increase the density of pixel in the image array. However, a gate-controlled structure is generally required to modulate the surface potential to get optimum device performance due to the damages and passivation issues. In this thesis, a composite dielectric film was used as the passivation layer. Without using the gate-control structure, we experimentally get R_0A = 7.6 $\times 10^4 \Omega$-cm^2 for p+n diode with 20×20 μm^2. Based on this result and circuit model, we expect the R_0A will be 5 $\times 10^4 \Omega$-cm^2 as the junction area is scaled down to 15×15 μm^2.

Keywords: Focal plane array, infrared detectors, passivation, leakage current, p+n diode, mesa etching, Be+ implantation, image pixel, p+n junction.

ACKNOWLEDGMENTS

I would like to express my sincerest gratefulness to my thesis advisor, Professor Kow-Ming Chang for his support and guidance throughout the course of this work, I owe a considerable debt of gratitude.

This work is a result of the infrared detector processing research I have performed at Materials and Electro-Optics Research Division in Chung-Shan Institute of Science and Technology, and National Semiconductor Center in National Chiao-Tung University for the past several years. I gratefully acknowledge the support of research facilities from CSIST and NCTU.

This work has been made possible by the efforts of several colleagues at CSIST. In particular, the contributions of Dr. Yao-Tang Gao, Sui-Pin Young, Yen-Nion Liu, San-DerYoung, Ming-Shan Tsi, Chung-Nen Chen, and Zau-Lang Hwang are gratefully acknowledged.

The comments and suggestions of Dr. Kow-Chen Liu in the Graduate Institute of Electro-Optical Engineering of Chang-Gung University and Dr. Wen-How Lan in the National University of Kaohsiung are also deeply appreciated. They gave long-term encouragement and helpful discussions in the area of device physics and fabrication processing. The assistances and discussions of my classmates in NCTU, Zen-Jai Lin in particular are also sincerely acknowledged.

Finally, my sincerest appreciation and love go to my parents, my dear wife and sons who consoled me during this trying time of writing and of moving.

Contents of List

Table Captions

Figure Captions