Chapter 1 Introduction

1.1 Background

Infrared imaging is to utilize the properties of thermal radiation emitted from the object and background to observe target and to provide information regarding the state of the target. Recently, large staring infrared focal plane arrays[1-2] are being developed for a wide variety of military and commercial applications. Military applications include advanced tactical systems such as FLIRs, missile seekers, threat warning sensors, and thermal weapon sights. Rapidly growing of commercial applications include usages for firefighters in an environment of reduced visibility; detection of highly dangerous and contagious diseases such as SARS etc., serviceability by law enforcement agencies; and expanded usages in anti-terror and security applications.

Continuation of scale-down of geometry in pixel size for focal plane array is highly desired for high resolution and large field of view (FOV) applications of advanced high density infrared imaging arrays. The development of larger format focal plane array will become feasible when the performances of small pixel area device are compatible to the large pixel area device. The reduction of single pixel implies that FPA chip composed of 2D focal plane array would become much smaller. Since the cost of focal plane array will be significantly reduced upon the decreasing of die size due to the diminution of pixel area. The overall costs will be likewise reduced because of the facts that each single wafer can produce more FPA chips. At the same time, the development of using larger format (more detection pixels) can become feasible when the reduction of pixel is further diminished.

Since 1978, Parrish, et al[3] has fist demonstrated two dimensional InSb infrared

image in IEDM with 32 X 32 arrays format by CCD multiplexers. Mesa type InSb IR detector of pixel size 100 um square with 64 X64 elements focal plane array was reported for low background flux applications by Blessinger, et al[4] in 1990, CMOS FET switch array multiplexer was used as the read out integrated circuit. Parrish, et al reported 38 um square with 256 X 256 sensor format of mesa type InSb in 1991[1]. Over the past few years, significant progress has been made in InSb materials[5-10] and fabrication technology.[9-11] Large format and small pitch IRFPA based on these new materials technologies have demonstrated excellent performance. Ashley, et al[10] used molecular beam epitaxy technique to grow InSb with in-situ doped on a 3" degenerate InSb substrate as the sensor substrate to demonstrate large format focal plane arrays 1024X768 pixels on a 26 um pitch in 2003, they used conventional lactic acid, nitric acid, and hydrofluoric acid to form the mesa structure on the InSb wafer misorientated by $2^{\circ} \rightarrow (111)$ B surface. Phosphate-based electrolyte was used to prepare the passivation layer on the surface.

However, to get to the desired goals of high resolution and high format for the next generation medium wavelength infrared image applications, the development of materials and fabrication process technologies related to InSb semiconductor will continuously proceed to scaling the pixel size to its diffraction limit.

1.2 Fabrication of backside-illuminated IR image sensor module

Indium antimony (InSb) is an established material to be used for infrared focal plane array processing in the medium wavelength 3 to 5 μm region. InSb sensor material and silicon material used for regulating signals of CMOS circuits can be processed together to form sensor module using hybridization technology as well as pixel to pixel bonding technique. As shown in Figure 1.1, a hybrid focal plane array is consisted of a two-dimensional array of InSb pn junction photodiodes in conjunction

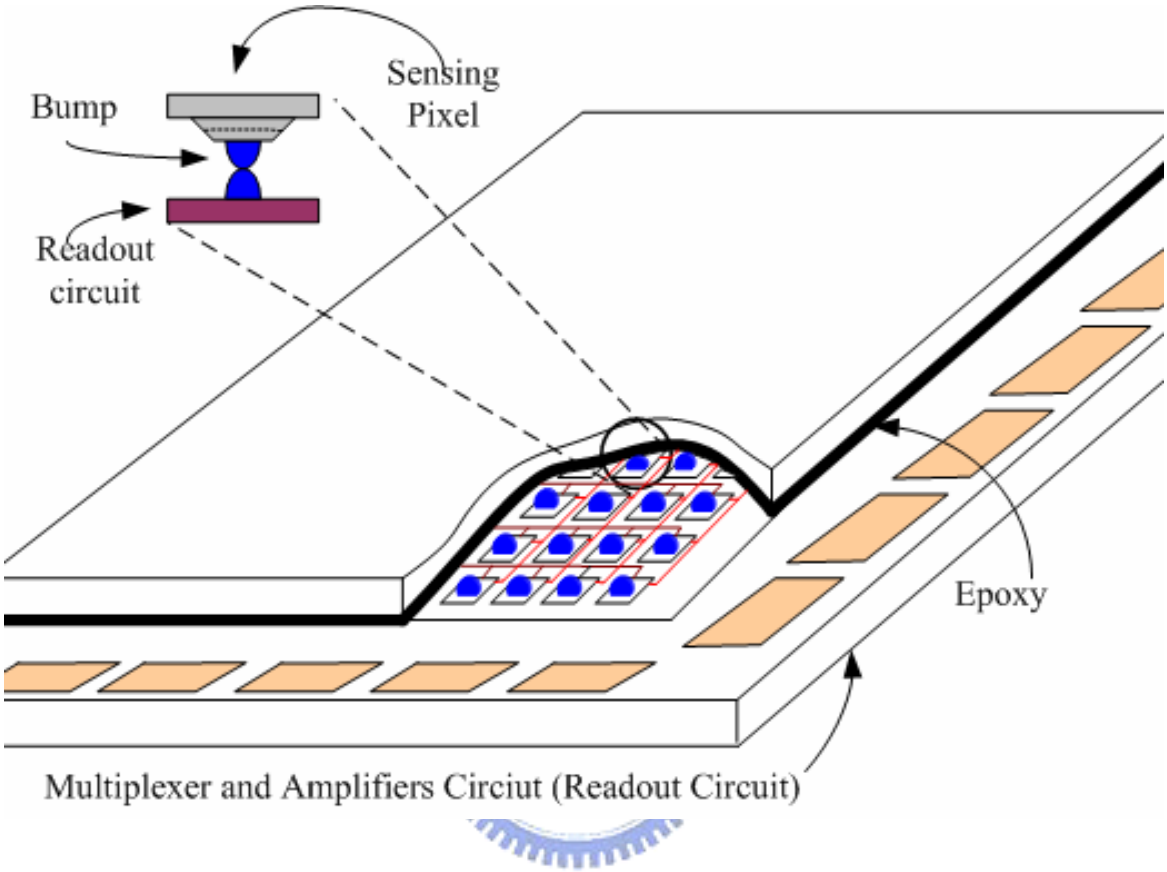

Figure 1.1 Hybridized sensor module by bump and Flip-Chip technology

with a CMOS-based multiplexing readout integrated circuit. The p+n junction has previously been formed by cadmium diffusion or beryllium ion implantation into n-type InSb substrate followed by forming a stack of passivation layer. The pixels in the focal plane image array are then created by mesa etching or planar process. The wafer surface after the mesa etching or planar process consisting of the p type, and n type is protected by the chemically inert and electrically insulating passivation layer.

Then the contact windows for both the p-type conductivity and n-type conductivity InSb surfaces were opened by standard H-line lithography and reactive ion etcher system with specific etching species corresponding to the passivation materials in used. Cr/Au metal layer were deposited on both conductivity surfaces function as the contact metals to the InSb surfaces with Ohmic contact characteristics.

Each focal plane array consists of Xrow × Ycolumn p^+/n diodes as the detection pixels. To maximize the fill factor of the IR signal to the detection pixel, the spacing between the mesa or junction peripheral is always reduced to the process limit. The active area is normally defined as the same as the pitch size due to the carrier diffusion length.

Metal bump technology was utilized to provide the electrical and mechanical interconnection between the InSb detector array and the silicon readout integrated circuit (ROIC). Figure 1.2 (a) and (b) is a typical example of metal bumps on InSb detector array in top view and cross section view. The metal bumps are grown on both the sensor array and readout chip. A flip chip bonding technology was used to hybridize the InSb diode array and silicon readout multiplexer. The bonding machine gives simultaneous viewing of the detector and ROIC via an IR illuminator by the transparency characteristics of silicon chip at near infrared wavelength spectrum. A built-in contact force indicator permits continuous monitoring of bump force during bonding.

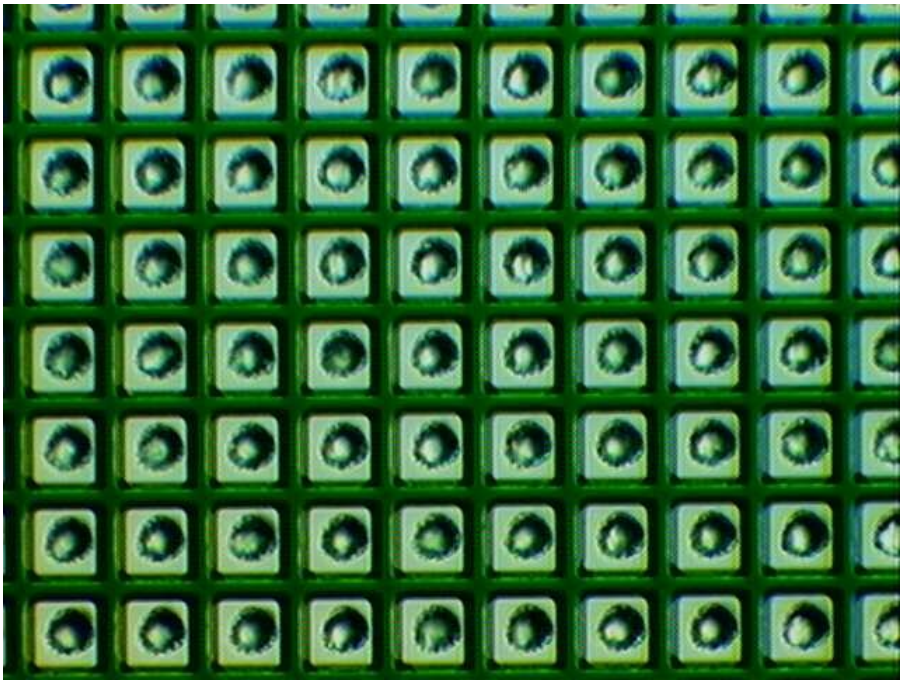

Figure 1.2 (a) Top view of sensor chip with the metal bump

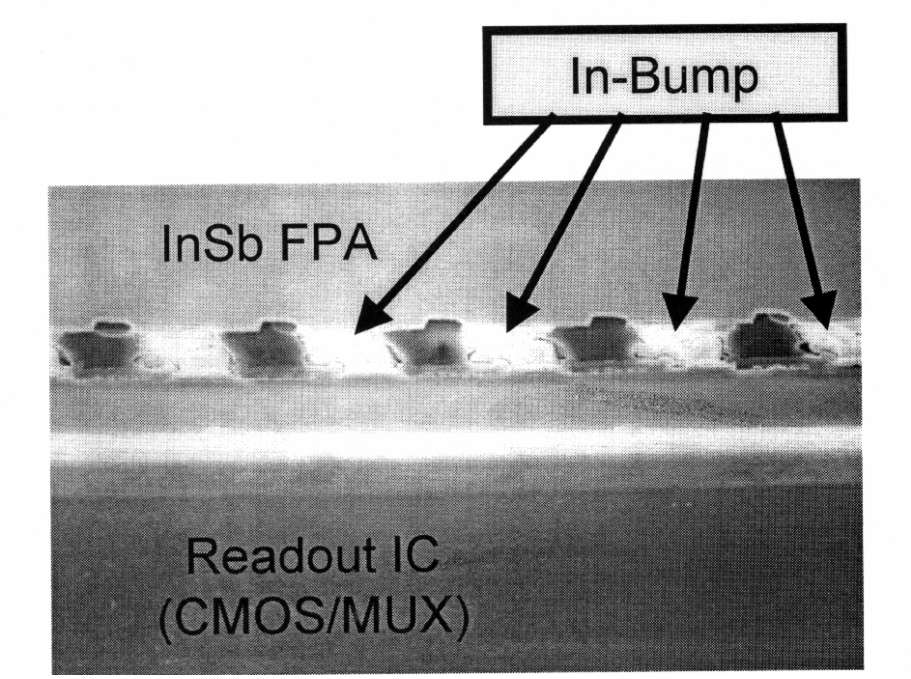

Figure 1.2 (b) Cross section view of the metal bump

After hybridization, the sensor module was thinned from the backside of sensor chip to optimize the quantum efficiency. Mechanical lapping and polishing procedures were used to thin the InSb backside to about 20μm thickness. A chemical etching was followed to achieve good thickness uniformity and to get rid of the damage resulted from the mechanical lapping and polishing process. Finally, the thinned backside was coated with antireflection coating with thickness corresponding to the specific infrared spectral range to maximize the quantum efficiency.

1.3 The Issues of infrared image array

The major concerns in this fabrication process is that all the detector arrays should be connected electrically and mechanically to the integrated readout circuit with functions of multiplexing and amplification at minimum degradation in the signal-to-noise ratio. The percentage of functionally operable pixels in the FPA depends on the yield of metal bump hybridization process assuming that the InSb detector arrays and silicon readout circuit chosen meet required functional specifications prior to hybridization. Three key issues of InSb detector processing will be studied and characterized for the pixel size scale-down requirements.

1.3.1 The surface passivation issue

The passivation of InSb p^+n diodes is critical to the current–voltage characteristics due to the sensitivity of the junction to the electric field. In actual fact, in order to draw away the limitation of scaling down the pixel size, the main approach is to promote the qualities of interface and dielectric film. The purpose of improving the quality of insulating film is to make p^+n diodes possess high performance and to remove the structure and steps of processing control gate when device is under operation. As a result, the qualities of interface and dielectric film required to

passivate the p^+n junction surface of small pixel p^+n junctions become more stringent as compared with those that required for p^+n junctions of large pixel area in producing the same performance.

The composite stack of anodic oxide and low temperature Photo-CVD oxide[12] is used as a passvation layer instead of single layer process on the surface of implanted InSb p^+n diode. The gate-control structure in InSb p+n diode has demonstrated the effects of surface potential on the current-voltage characteristics.

1.3.2 The mesa formation issue

On the second issue, the mesa is formed by removing the p-type material completely along with etching part of the n-type substrate. The metallurgical junction is assumed to be formed in the middle of the mesa height. The mesa etching process defines both the lateral dimension and the step profile. The surface and the sidewall of the mesa structure will make direct interface with the succeeding passivation or dielectric film. The control of surface morphology in mesa type p+n junction is an important issue due to its relevant characteristics caused by the impact of sensitivity of electric field on the exposed peripheral.

.However, conventional mesa etching solution, 10:1 lactic acid/nitric acid mixture by volume ratio has severe structure morphology problem which result in the step coverage and trench issues. By using the citric acid/hydrogen peroxide mixture instead of the conventional lactic acid/nitric acid mixture in this work, we have demonstrated mechanically and electrically the performance of uniformity.

1.3.3 The junction formation issue

The diffusion and mesa approach in the InSb detector arrays will suffer performance yield loss due to junction peripheral exposure and device structure

uniformity challenge issues during the development of small pixel area and high density two dimensional image array. The solid source Cd diffusion[13] with wafer positioned horizontally in the vacuum sealed quartz tube generally have problem in the doping level and profile control issues which will severely influence the junction depth distribution across the wafer and also the performances of photodiode made from it. Moreover, the uniformity of these two issues for large sensor chip and wafer diameter larger than 2 inch will be more stringent due to the development trend of large format sensor chip requirement.

The highly development of the silicon based electronics industry has droved the process technologies to fabricate device structure from micrometer to nanometer scale over the last decade. The short wavelength lithography shrinks the line width of devices down to submicron scale in planar dimension. The gate oxide and ion implantation technologies reduce the oxide film thickness and junction depth to nanometer scale in vertical direction. With precise physical control mechanism, the ion implantation and annealing technologies provide advantages in control of the doping level and the distribution, good uniformity and reproducibility of the doping, selectively doping by combining with appropriate mask materials. These features clearly offer great potential in the development of high density two dimensional infrared focal plane arrays.

Ion implantation has been demonstrated and reported in producing InSb p+n junction diodes with its inherent advantages such as planar processing and uniform characteristics for infrared detector array applications. Previously, Beryllium has been identified as an optimum p-type dopant in InSb due to its lower generation rate resulted from implant damage. However, most of the literatures reported so far require extra insulated metal gate to control the surface potential of junction peripheral. This implement adds severe complexity and impact on the device structure and fabrication

processings which result constraints on the pixel size shrinkage.

1.4 Thesis organization

The objective of this thesis is to develop a high performance InSb diode structure for mid-wavelength thermal image applications and study its feasibility. The p+n diode device structure, junction formation, mesa etching, surface passivation, electrical uniformity, process compatibility are analyzed and compared with the conventional structures and processes.

There are five chapters in this thesis. Chapter 1 introduces the important issues of InSb p-n diode, hybridized sensor/ROIC module fabrication process and reviews related research works by other groups. Chapter 2 discusses the passivations issues, anodic oxide and low temperature Photo-CVD oxide are characterized separately; the composite stack passivation layer is also evaluated by in-situ test structure. The surface potential effects on the InSb p+n diode is characterized by an gate control structure. Chapter 3 presents the InSb mesa etching characteristics in citric acid/hydrogen peroxide solution and discusses its effect on the uniformity of dark current in InSb p+n diodes. The results are compared with the diode structure made by conventional mesa etching solution both in mechanical and electrical performance. Chapter 4 presents the development of small pixel planar diode made by implantation technique. Without gate-control structure, the device structure, process parameters and performances characterization are described. The product of zero-bias dynamic resistance and junction area can get $5X10^4$ Ohm-cm^2 for InSb p+n diode with junction area 15x15 um^2 based on the curve fitting of our experimental data with the proposed simple circuit model. The photo response testing confirms the detection function of our implanted diodes. In Chapter 5, the final chapter, we conclude our development and give recommendation for future work.

1.5 References

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