Chapter 2 Preparation and Characterization of Composite Oxide As a Passivation Layer of InSb Diodes

2.1 Requirements of passivation layer for InSb p-n diodes

Narrow band-gap semiconductor materials, for instance InSb and HgCdTe, have relatively low melting point characteristics with respect to the wide band-gap semiconductor materials, such as Si, GaAs etc. It has been reported[1] that damage or deviation from stoichiometry in the InSb surface may be resulted from the evaporation or preferential oxidation when the process temperature is higher than 250 ℃. Therefore the process forming passivation on the surface of InSb is required at moderately lower temperature.

The junction and surface are sensitive to the electrical modulation due to the requirement of cryogenic temperature operation for the narrow band-gap InSb p-n diodes. The reduction of thermal energy at cryogenic temperature promotes the significance of electrical energy relatively. The exposure of metallurgical junction for both mesa type and planar type p-n diodes generates a challenging issue in reduction of leakage current resulted from the leaky path between p-type and n-type conductivity surface directly. Moreover, the band bending of junction near the surface is easily influenced by the existence of surface charge which will induce high electric field in some local area of the diode structure.

There are varieties of low-temperature insulator deposition technologies have been investigated and developed for high quality interface to InSb [2-5]. Basically, three different categories in these processes had been studied. Anodization of InSb by the electrolyte technique was first studied by Dewald[6] and many workers due to its advantages of simple, economic. Physical vapor deposition processes provides the second alternate to the low temperate approaches, for example, evaporated SiO[7],

sputtered aluminum oxide[8], and sputtered oxide. In the chemical vapor deposition category, these techniques provides potential advantages in highly control over the process and materials cleanliness, the processes used for preparing the dielectric film , including oxide, nitride, or oxynitride in silicon processing by the reactive chemical species of silane and oxygen molecules. These including plasma-enhance CVD), low temperature CVD [9], Photo-enhanced CVD [10].

A passivation layer prepared on the surface of a InSb p-n diode has to meet stringent requirements in electrical performances in addition to providing the function of mechanical damage prevention and chemical protection as the meaning of terminology of passivation. The function of passivation in InSb based devices is just like the gate oxide in the CMOS technology. It should provide high resistance, low fixed charge density and low interface state density. It should also accommodate the qualities requirements for both n-type and p-type conductivity surface simultaneously. Passivated with single low–temperature deposition oxide layer is generally used and desired on the planar type InSb p-n junctions due the considerations of cost and integration. However, most of the literatures reported so far require extra insulated metal gate to control the surface potential of planar type InSb p-n junction peripheral[8,11] due to the interface and fixed charge quality of the deposition oxide.

The implementation of control gate in the two-dimensional focal plane array may introduce the complexity of device structure which impedes the development of scale down of pixel size. As shown in Figure 2.1, the schematic representation of a sensing p-n diode with gate-control structure in a focal plane array. Double-metal and double-dielectric deposition processes are required to accommodate the control-gate metal. In addition to the device process complexities resulted from the double-metal and double dielectric processing. The device performances may also have

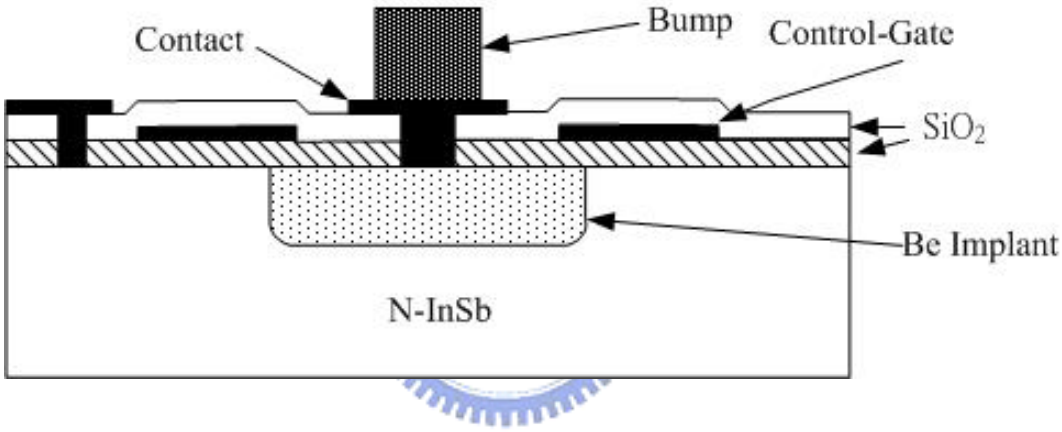


Figure 2.1 Schematic representation of planar pn diode with gate-control structure.

considerable impact in the reduction of fill factor.

The process control over the contact window and registration of contact metal and bump metal with respect to the gate metal will be highly challenging issues especially for the scale-down trend of pixel size. In actual fact, in order to draw away the limitations of scaling down the pixel size, the main approach is to promote the qualities of interface and dielectric film. The purpose of improving the quality of insulating film is to make p^+n diodes possess high performance and to remove the structure and steps of processing of control gate.

Due to the materials' differences between the semiconductor and passivation film, there existed interface charges caused by dangling bonds between semiconductor surface and passivation film. In addition, there were different types of built-in oxide charges found during the preparation steps of passivation film. These charges resulted from the processing of passivation film can affect the carrier transport mechanism of exposed region of metallurgical junction. The peripheral of the junction devices are sensitive to the surface potential due to the proximity relation with the passivation film. The surface potential can be induced by the interface charges and the charges in passivation layer. In general, the passivation is required to provide low density of interface state and oxide charge with low leakage current and high electrical strength for high performance imaging array applications.

Typically, thick passivation including anodic oxide and deposited oxide is required for mesa type p-n junction due to the step height coverage difficulty. On the contrast, this study is focus to investigate and understand the qualities of the thin passivation stack composed of anodic oxide and low temperature Photo-CVD oxide on the implanted InSb p^+n diode.

2.2 Anodic oxidation of InSb

Anodic oxidation has been investigated thoroughly as the surface passivation film to control the leakage current of InSb pn diode due to its inherited low temperature and convenience. To passivate InSb with anodic oxidation, there were three different kinds of chemical solutions, these chemical systems include base, acid, and organic based mixture. They all have been investigated as the electrolyte in anodic oxidation process of InSb surface. In this study, the characteristic of anodic oxide prepared by 0.1N KOH is reported. Figure 2.2 is a typical schematic representation of an electrolyte setup under constant current mode including the wafer holder and power supply. The electrical system can be switched between the constant current mode and constant voltage mode.

To study the control factors in anodic oxidation, constant current mode was used. A constant current supply with voltage measurement capability was applied between anode and cathode terminals. As the switch was turned on, a specific constant current will flow in the electrolyte solution in addition to the circuit wiring. An increasing voltage drop between the anode and cathode will be setup as the high impedance oxide become thicker. So, the voltage-time characteristic curve can be used to dictate the formation of anodic oxide layer.

As shown in Figure 2.3, the formation voltage-time characteristics with the current density as the process parameters were analyzed. The legend in the plot indicates the corresponding current density in A/cm^2 unit. From this figure, it can be summarized:

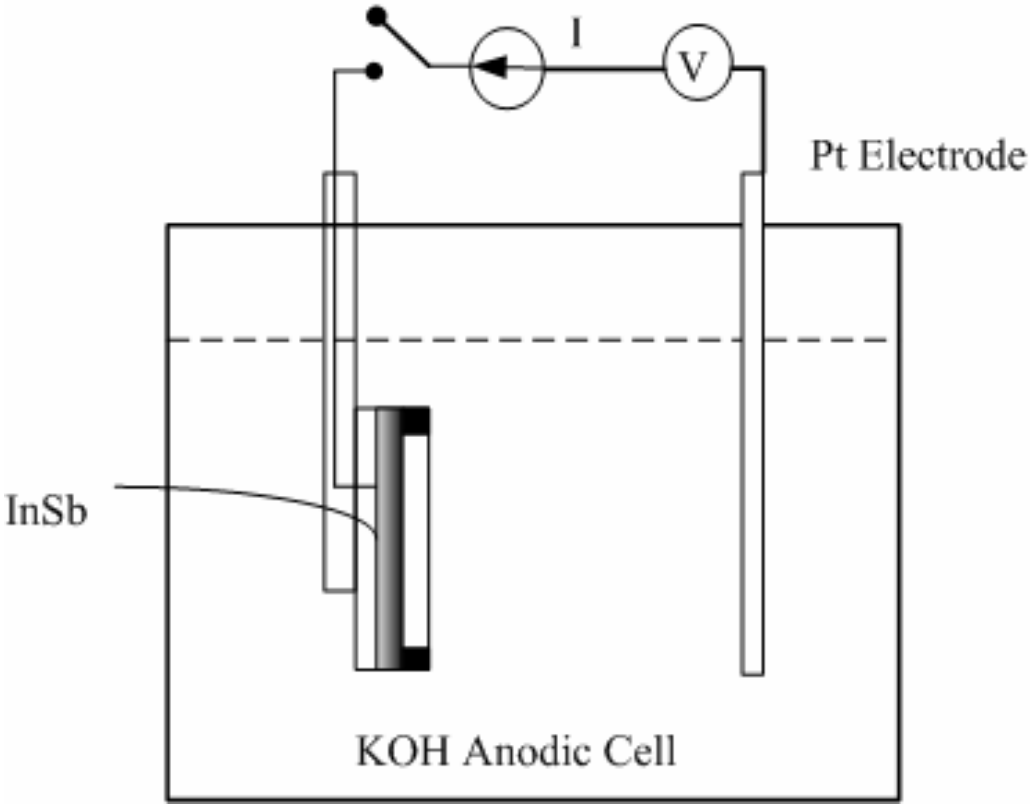


Figure 2.2 Schematic representation of constant current setup for preparation of anodic oxide on InSb.

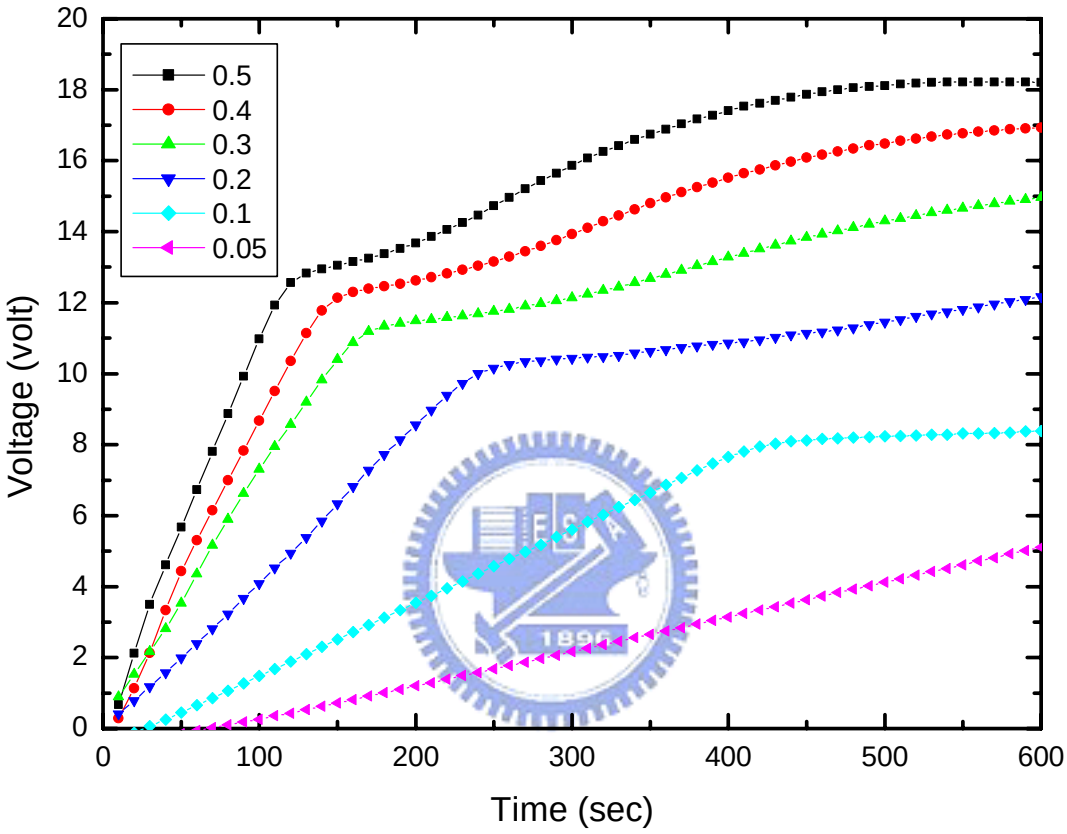


Figure 2.3 Formation voltage of InSb anodic oxide in 0.1N KOH versus the growth time with the constant current density in unit of mA/cm^2 as depicted in the legend as the parameters.

- There is a linear formation region with respect to each current density.
- The formation time regarding to the turning point from the linear to saturation region will increase as the current was decreased.
- The turning point of formation voltage increased as the current density was increased.

Ellipsometer was used to measure the thickness of the anodic oxide prepared with constant current level set at 0.5mA/cm^2 and form the oxide up to some specific anode voltages before the turning points. It was correlated to the anode bias voltages as shown in Figure 2.4. The result indicates that the thickness of anodic oxide prepared have linear proportional relation with respect to the formation voltage. The growth rate of anodic oxide corresponding to formation voltage is 27.6 Å/V. That means the thickness of anodic oxide on the InSb surface can be controlled by voltage. It should be noted that the anodic oxide should be grown under linear region in the formation curve. The anodic oxide prepared with anode voltage larger than the turning point or stay at turning point for a long enough duration. The oxide compound will result abnormal characteristics, for instance, the index of refraction n of the anodic oxide film will increase substantially, which imply the composition of the oxide compound may have made significant changed.

The anodic oxide is grown partially inward to the bulk of InSb single crystal, and partially outward above the surface of InSb. The Ellipsometer was also used to measure the difference between these two growth directions under different constant current levels. The thickness ratio of inward part to the total anodic oxide is about 0.46 for all the current levels under linear growth condition.

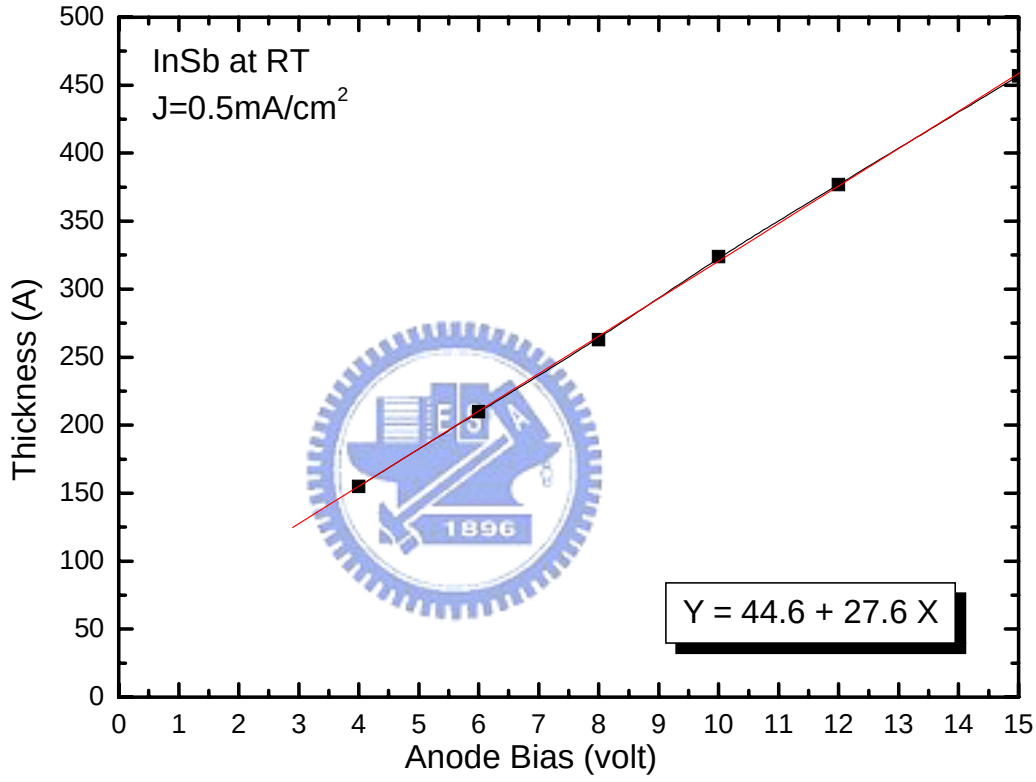


Figure 2.4 Oxide thickness versus the formation voltage of InSb anodic oxide.

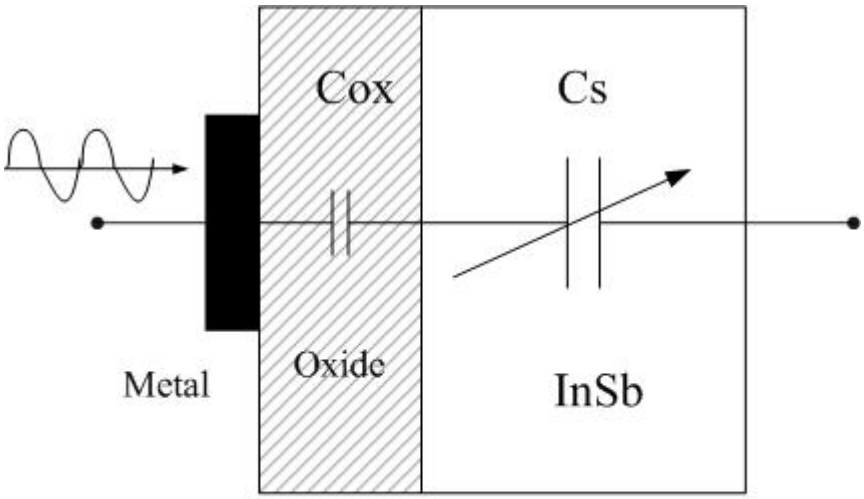
Electrically, the anodic oxide is hardly getting characterized due to the highly conductive material and porous properties in the thickness range of 1KÅ. It has been identified that the materials of the anodic oxide are mainly composed of. metal oxide, they are In_2O_3 and Sb_2O_3. So, the electrical strength is relatively weak when making comparison with the thermal oxide in the silicon processing.

Figure 2.5 represents an equivalent circuit of an ideal MOS capacitor structure. The total capacitance C is expressed as two connected capacitors in series, one is the capacitor with oxide capacitance Cox and the other is the capacitor with surface capacitance Cs as function of surface potential Ψ_S. As shown in Figure 2.6, the black and blue curves represent the surface potential or voltage dependence of the capacitance and conductance in a n-type InSb MOS capacitor fabricated by anodic oxidation. The typical characteristics can be summarized in the following:

- Under limited bias range 2 Volts to -4 Volts, the capacitance decreases from Cox to Cmin, it means that the surface can be modulated from accumulation, depletion, and inversion regions.
- The flat band voltage shift to the positive bias direction, this implies negative charge distribution in the anodic oxide or in the interface between anodic oxide and InSb surface.
- The conductance-voltage curve indicates that the MOS will have high AC conductance in the inversion region.

2.3 Low temperature Photo-CVD oxide

Photo-CVD was used to grow the low temperature oxide on InSb by the direct ultraviolet radiation enhanced oxidation reaction. In this process, mercury vapor bubbled with carrier gas SiH_4 is introduced into the reaction chamber and excited by



$$\frac{1}{C} = \frac{1}{Cox} + \frac{1}{Cs(\Psi s)}$$

Figure 2.5 Equivalent circuit model of an ideal MOS capacitor.

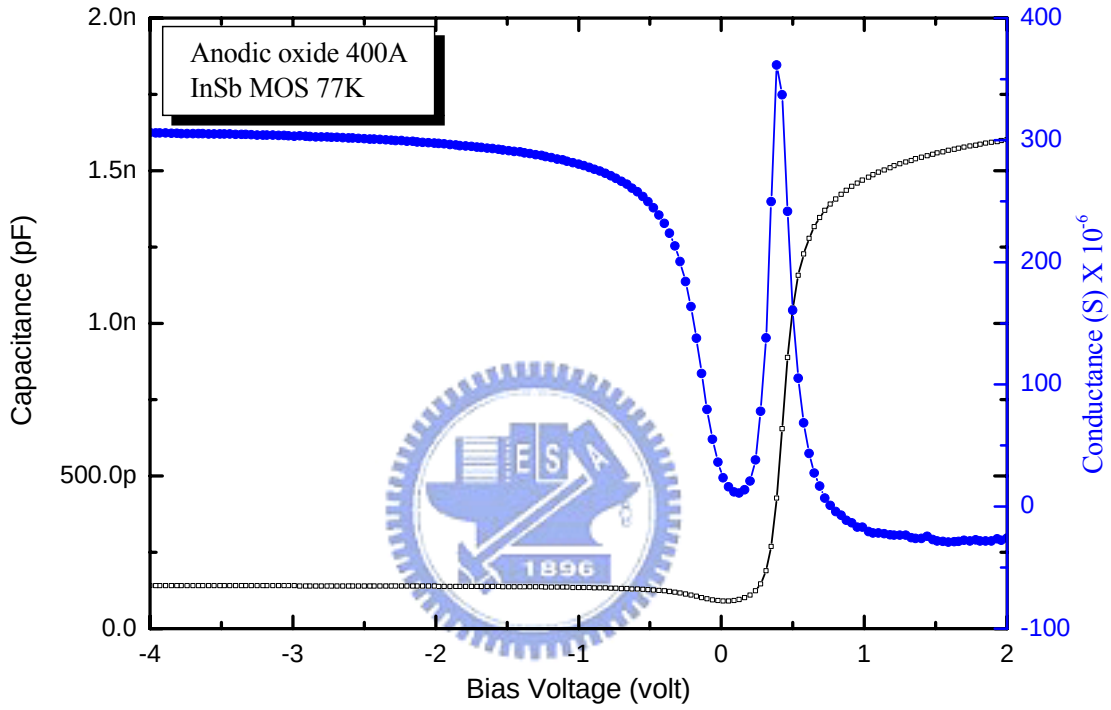


Figure 2.6 Capacitance-Bias voltage characteristics of the MOS capacitor at 77 K with oxide prepared by the anodic oxidation.

UV radiation catalyzes the reaction between SiH_4 and N_2O to form SiO_2. To characterize the deposited oxide quality, oxide was prepared on the p-type silicon dummy wafer at various deposition temperatures. As shown in Figure 2.7, a MOS capacitor with oxide deposited at 180C was measured under 300K. The C-V characteristics present typical accumulation, depletion, and inversion region from the negative bias to positive bias. It also indicates that:

- The negative flat-band shift indicates the existence of positive fixed charge distribution in the interface or bulk oxide.
- Conductance level lower than $1X10^{-7}$ (S) at small bias range, it is relatively lower than the anodic oxide.
- The bias sweep range is from -8 Volts to +2 Volts, typical electrical strength in InSb MOS structure can reach $1X10^{6}$ V/cm at 77K.

These characteristics are very similar to the MOS capacitor fabricated on the InSb as reported in the literatures.[5] To understand the frequency dependence, the capacitance-voltage characteristics of in the MOS capacitor fabricated by Photo-CVD were measured with changing frequency of the small signal from 1K to 40M Hz. As shown in Figure 2.8, in addition to the typical characteristics as described in the previous figure, the C-V curve of 1 KHz indicates a typical high frequency characteristics, the capacitance went from Cox at accumulation to Cmin at strong inversion, it indicates relatively lower surface states in the interface and stop the supply of carriers to response to the low frequency AC surface modulation. However, in the accumulation region about 25% in the capacitance dispersion occurs from 1 KHz to 1 MHz.

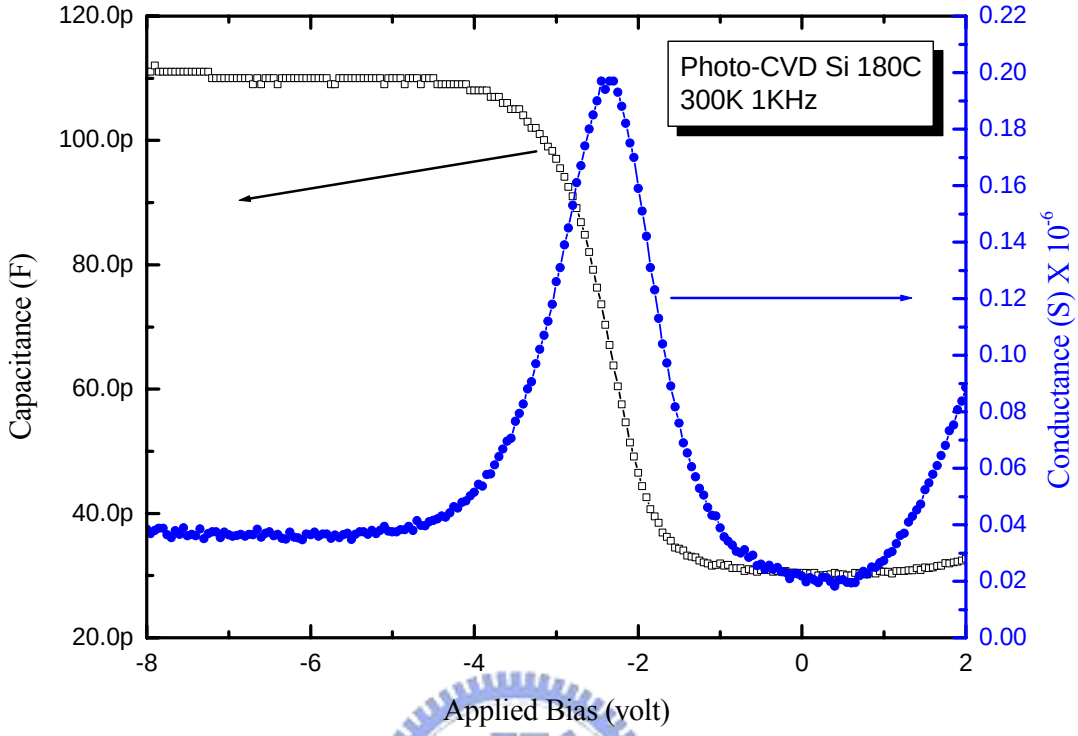


Figure 2.7 Typical bias dependence of capacitance and conductance for p-type silicon MOS capacitor fabricated by Photo-CVD system at 180C. The measurement was made under room temperature.

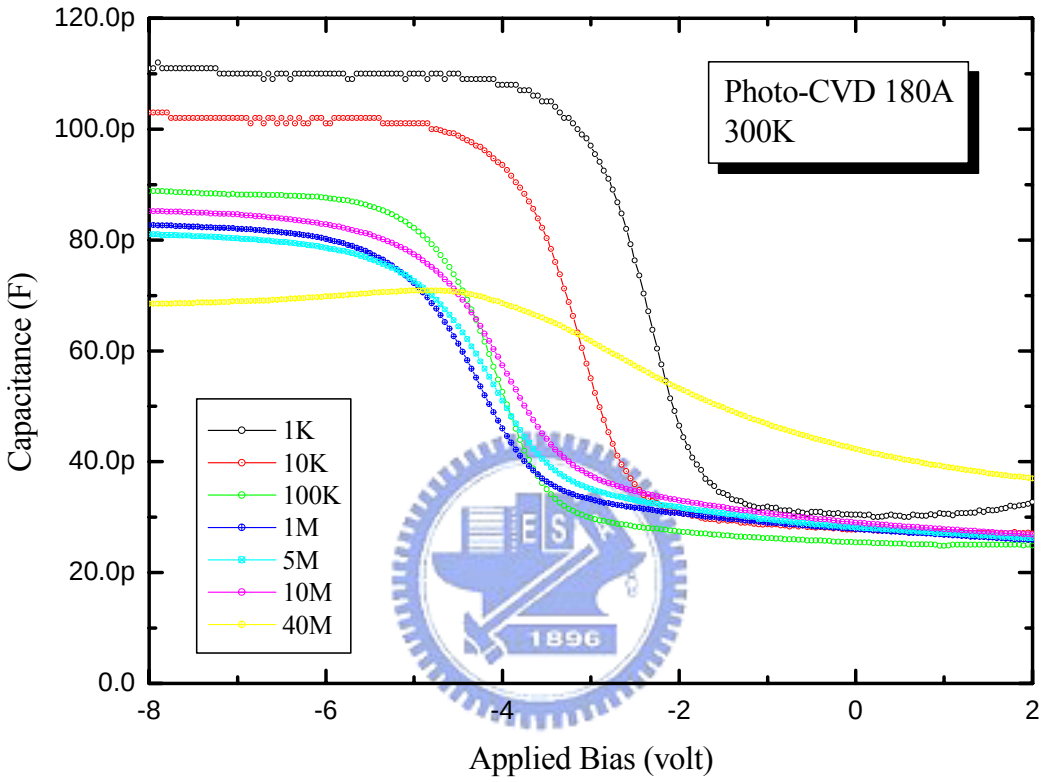


Figure 2.8 Capacitance-voltage characteristics with small signal frequency as the parameters depicted in the legend. Silicon MOS capacitor was fabricated by Photo-CVD system at 180C.

2.4 Composite passivation stack

A composite stack of anodic oxide and Photo-CVD oxide was proposed to work as passivation layer for planar p-n diodes. The primary idea is based on the qualities provided by the anodic oxide and Photo-CVD oxide to compromise the passivation quality with the following requirements:

- high resistance in oxide bulk
- low positive charge to get surface under weak inversion condition

The properties of the composite passivation film and its interface to the InSb was studied by high frequency C-V measurement on a MOS capacitor structure with area 9E-4 cm^2 through the bias sweep starting from positive to negative voltage. The surface potential of n-type InSb under the passivation film will be changed from accumulation to inversion region at 77K. The flat-band voltage shift ΔVfb and fixed oxide charge density Qox are extracted by comparing the measured C-V curve with the ideal C-V characteristics. As shown in Figure 2.9, The positive sign of ΔVfb and negative sign of Qox indicate that the effective fixed oxide charge including anodic oxide/SiOx bulk and its interface to the n-type InSb surface is a distribution of negative charges. The surface of the n-type InSb is then under the weak inversion condition. It is expected that this surface condition may help to prevent the buildup of high electrical field in the local surface junction regions, which accordingly will reduce the p-n diode leakage current and breakdown voltage.

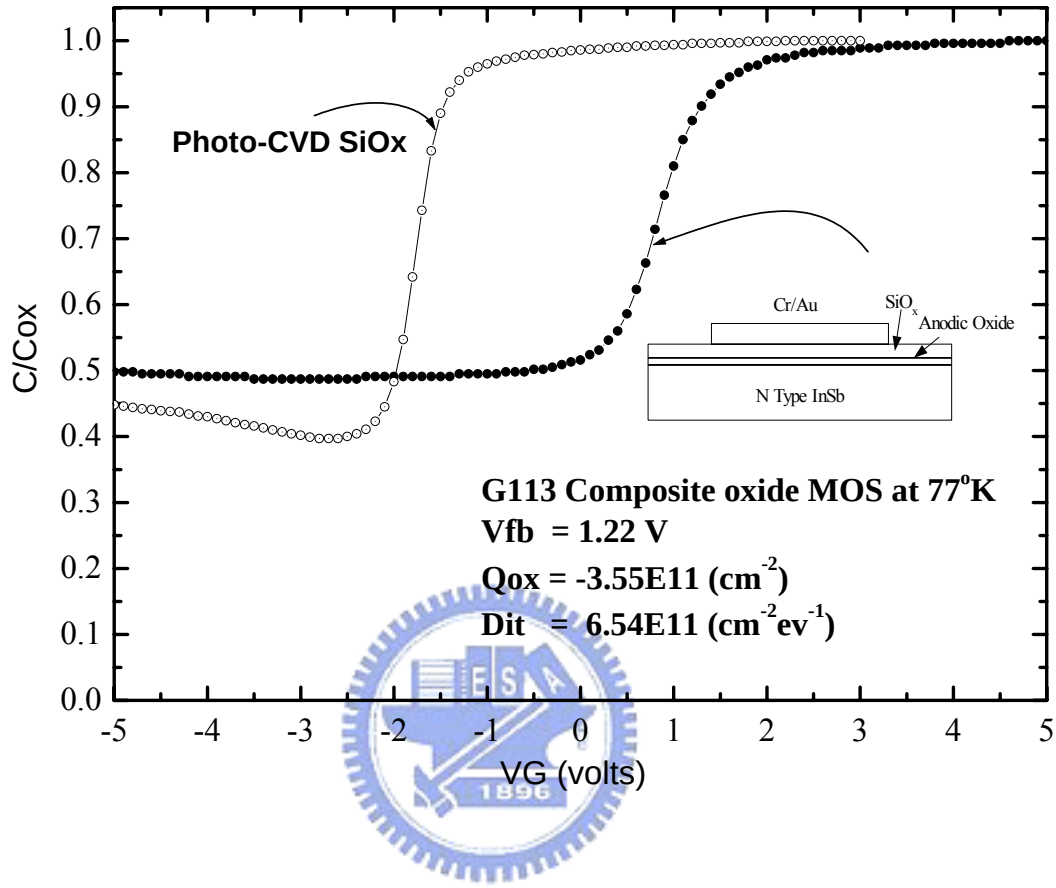


Figure 2.9 Capacitance-Voltage characteristics of MOS capacitor with the composite anodic oxide/SiOx structure on the n-type InSb measured at 1MHz and 77°K. The MOS capacitor area is $9X10^{-4}$ cm^2. The interface state density Dit was extracted by Terman method. C-V of Photo-CVD oxide was also shown as the reference.

By using high frequency Terman method [12], the interface state density near midgap is estimated to be in the range of Dit= $6.54X10^{11}cm^{-2}$. As shown in Figure 2.10, the distribution of Dit is around 10^{11} order of magnitude in most of the bandgap region except on the edge of bandgap. By contrast, the results obtained from our experiment indicate that the interface state density of our proposed insulating film stack to n-type InSb is comparable to the Dit obtained from the annealed Photo-CVD oxide.[5] Based on these results, it can be seen that the combination of anodic oxide and Photo-CVD low-temperature oxide can meet the requirements of InSb p+n diode passivation in terms of high gate voltage span, low density of oxide fixed charge, and low interface state. Even the inherent hysteresis stability characteristics in the anodic oxide, the composite oxide can provides optimum depletion or weak inversion surface potential to the n-type surface and weak accumulation on the p-type surface.

Figure 2.11 presents a typical example of InSb p+n diode passivated with composite oxide. The device structure as shown in Figure 2.13(a) was used. The bias voltage was applied to the control-gate to modulate the surface potential on the p+n diode. The labels in Figure 2.11 indicate the positive bias voltage from 0 to 6 volts was applied. The soft breakdown voltage of InSb p+n diode decreases as the voltage on the control-gate was increased. This may be explained by the development of a local electric field results from the accumulation of negative charge on the n-type semiconductor surface. The structure of p+ doping and n-type accumulation may effectively setup the p+n+ regions in a diode.

On the other hand, Figure 2.12 presents the I-V measurement result in the negative polarity direction. Please note that the plot was zoom in to smaller scale to help to observe the detail of the current-voltage characteristics. When the control-gate bias was changed from 0 to -8 volts, the p region may become more p++, but the n-type region will go from depletion to strong inversion regions, that is n-type may be

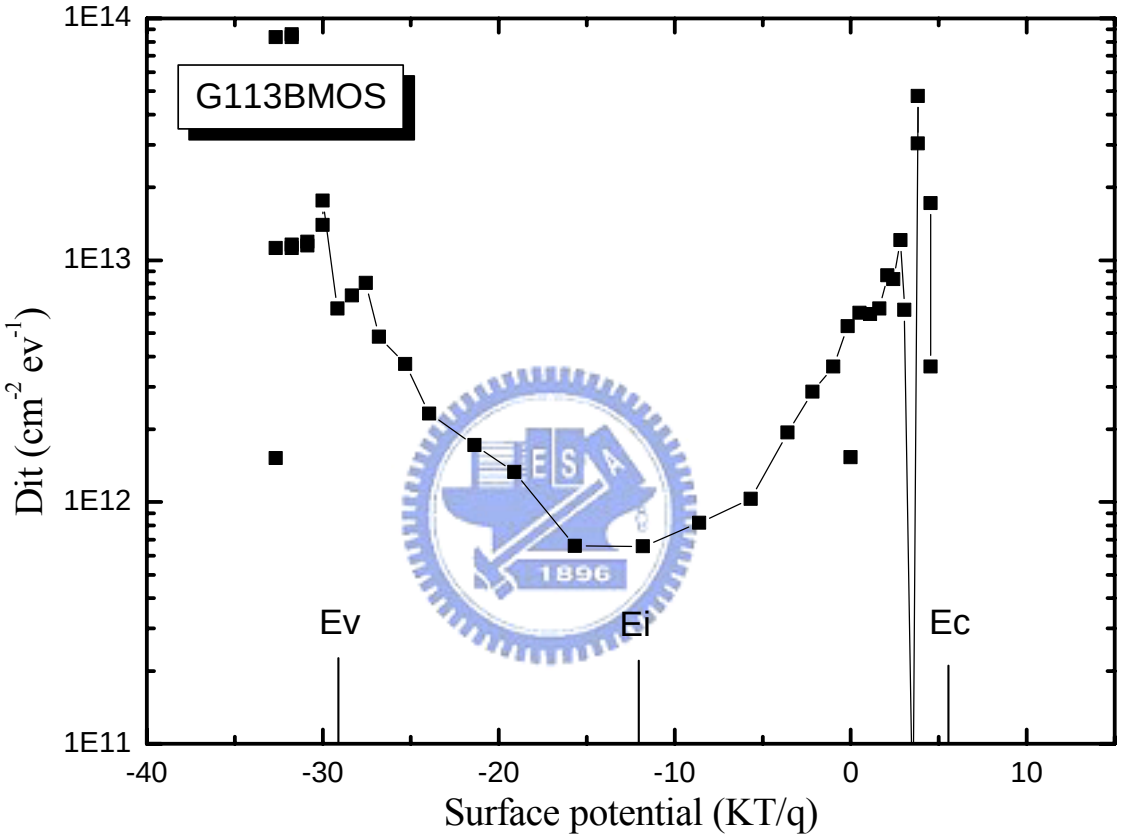


Figure 2.10 Interface state distributions in the bandgap of the InSb extracted from the high frequency C-V method at 77K.

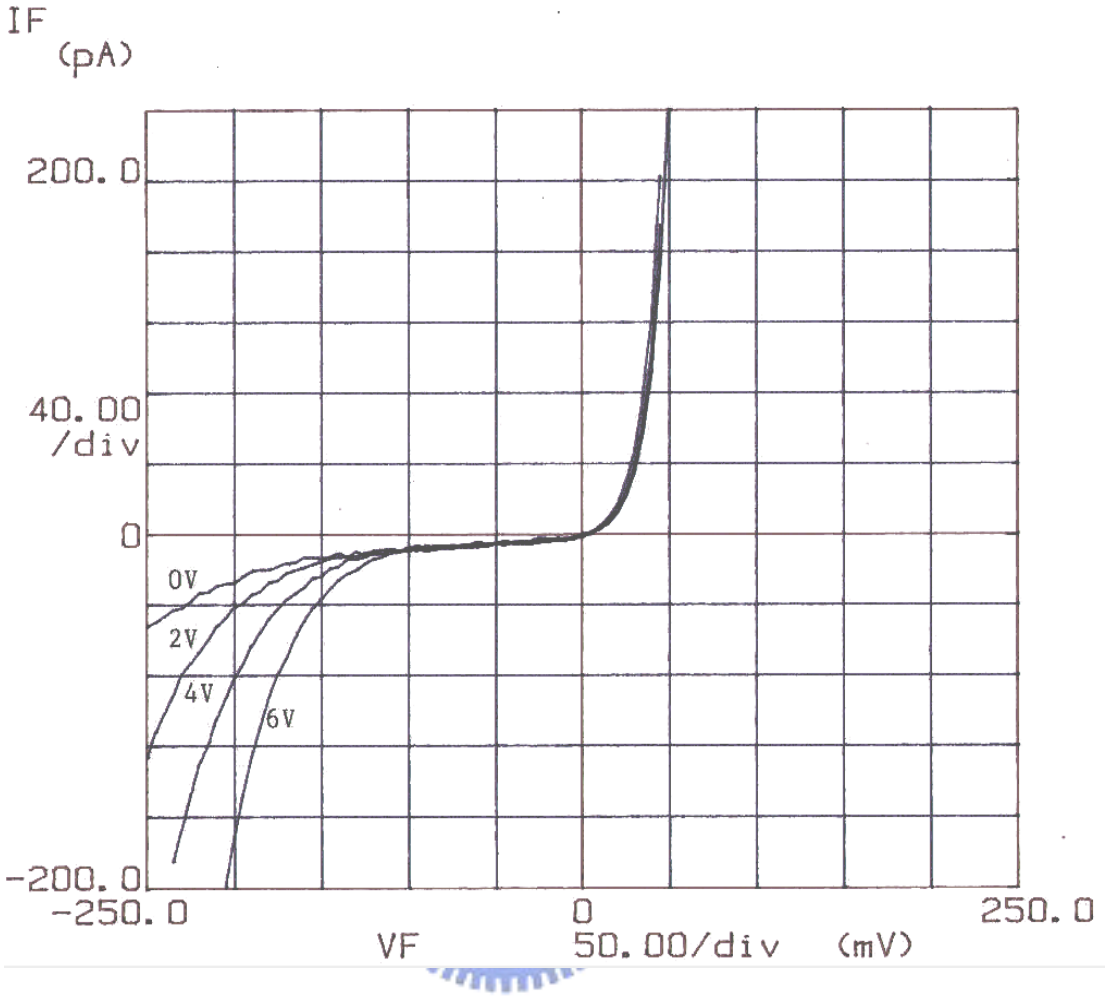


Figure 2.11 Current-voltage characteristics of InSb diode in response to the change of positive polarity control-gate bias.

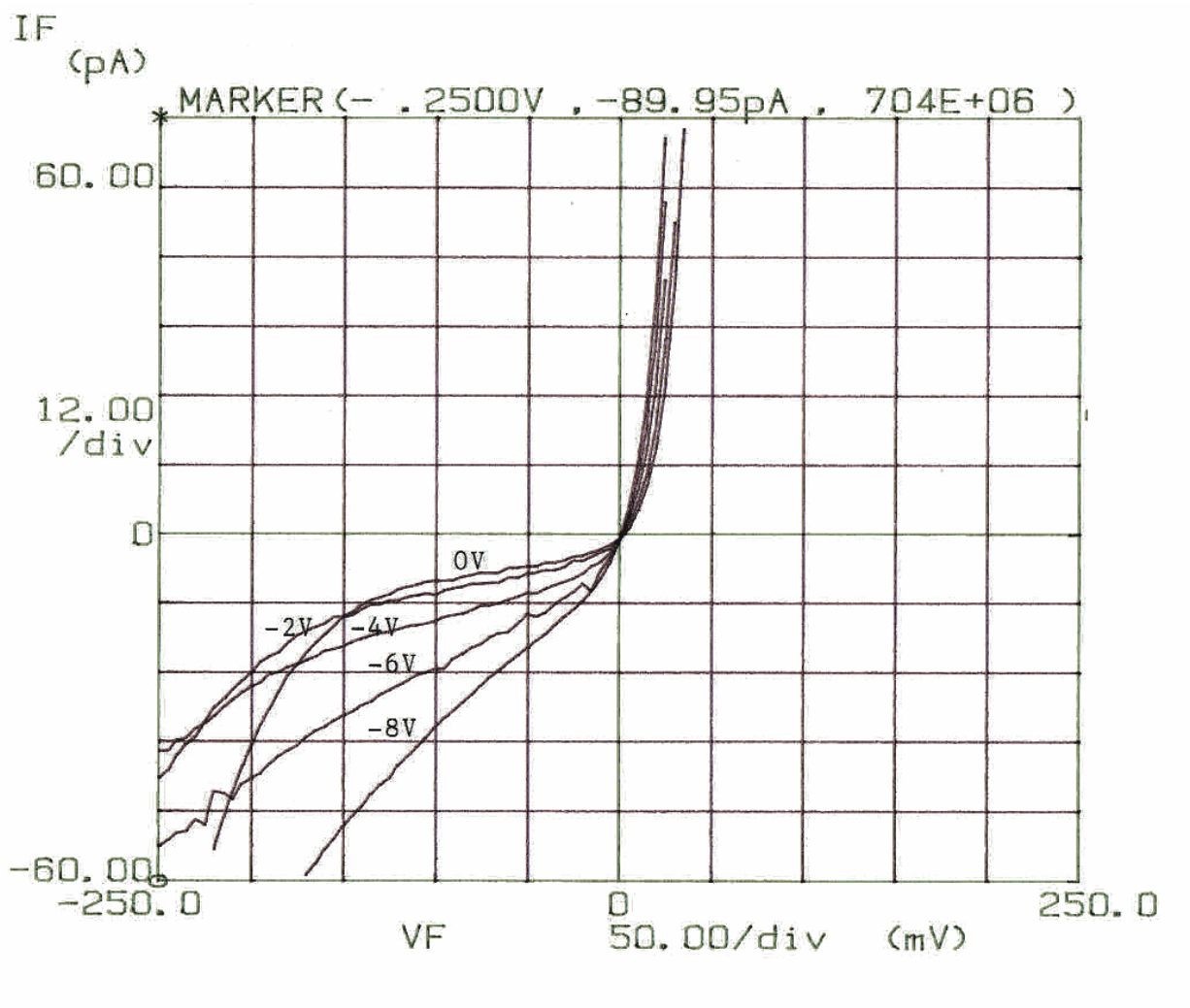


Figure 2.12 Current-voltage characteristics of InSb diode in response to the change of negative polarity control-gate bias.

changed into p-. So, the current-voltage characteristics become resistor-like as the negative bias was increased.

To understand the effects of surface potential on the diode I-V characteristics, four different reverse diode currents were selected as the measurement parameters. The dependence of control-gate bias of the diode current was plotted as shown in Figure 2.13 (b). From +5 Volts to -20 Volts, the n-type surface may change its states from accumulation, depletion, and strong inversion. At the voltage close to 5V, the diode current corresponding to the four reverse biases will change rapidly. As the control-gate is close to zero, the diode currents are relatively stable in a range of 5 Volts. This result provides a direct evidence and confidence of using the composite oxide as the passivation layer. Without control-gate structure on the InSb p+n surface, we can get optimum performance in the application of infrared image array.

When the control-gate bias in the range of -2.5 to -15 Volts was applied to the devices, the diodes current will response with increasing at first, then reduce back to low current at about -15 Volts, it was a typical characteristics of the surface states. When the bias was increased to more than -17.5 Volts, all the diodes indicate large variation in current again just as the situation of +5 in accumulation region.

So, the sweep of control-gate bias voltage in the diode structure provides the information of optimum device performance with respect to the quality of surface passivation layer and external bias required for surface potential.

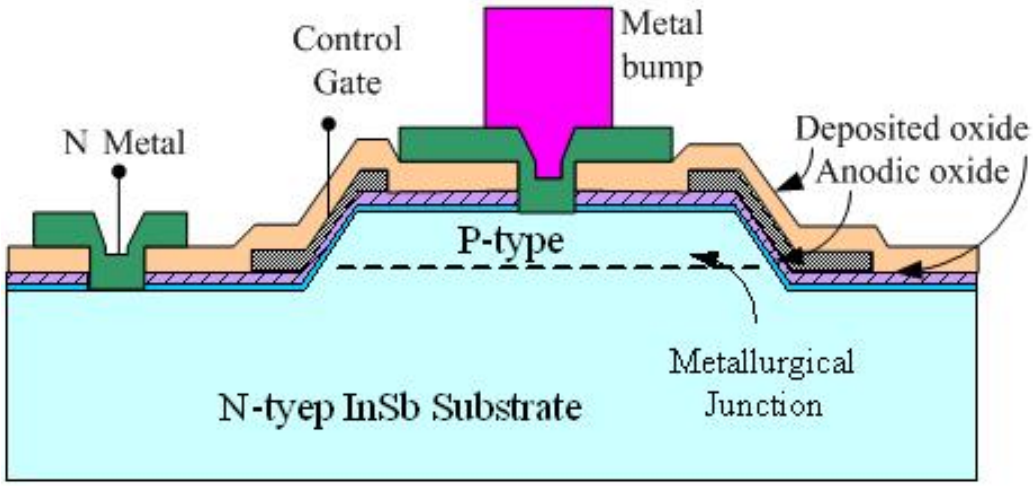


Figure 2.13 (a) Mesa type diode structure with control-gate metal.

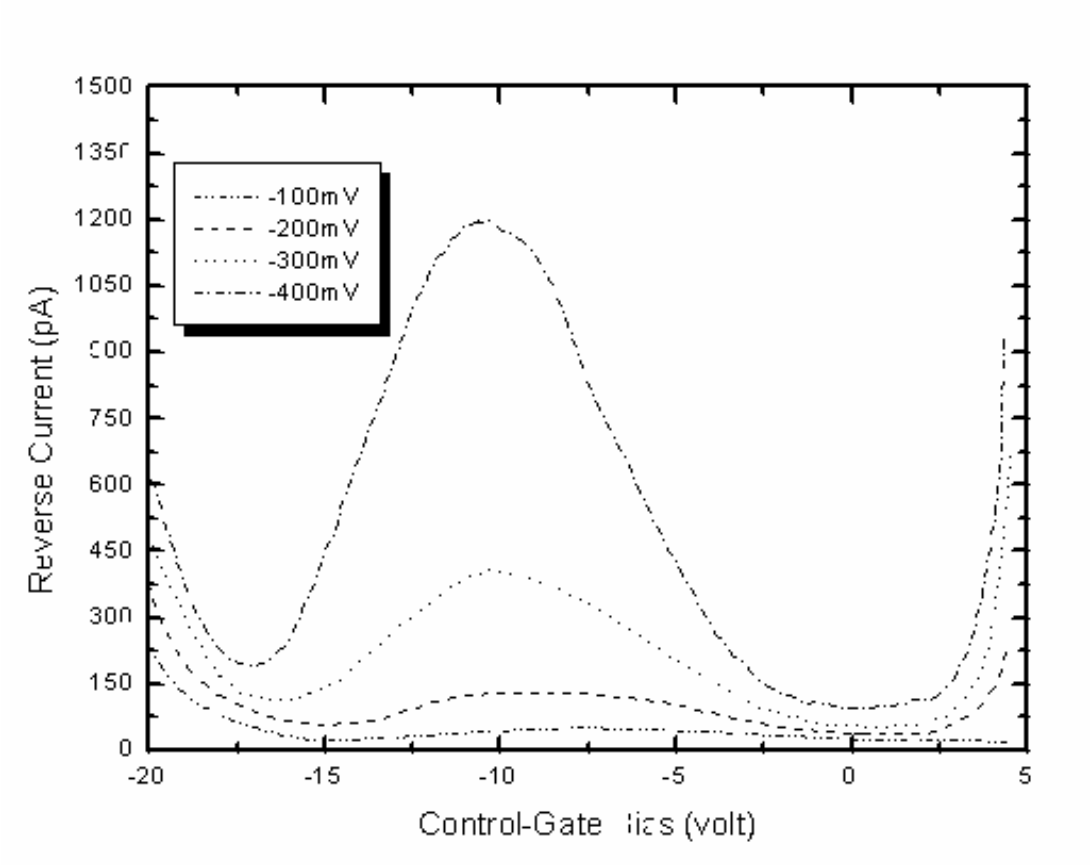


Figure 2.13 (b) Control-gate bias dependence of the diode current under various reverse bias voltage.

2.5 Summary

The prepared anodic oxide has characteristic of negative polarity charge distribution in the bulk or interface between the oxide and InSb. The thickness can be controlled by the formation voltage in the anodization process. The Photo-CVD oxide, however, has characteristic of positive polarity charge distribution in the bulk of oxide. It has been determined that the combination of anodic oxide and Photo-CVD oxide will have effective negative fixed oxide charge distribution on the InSb surface.

The Photo-CVD oxide play an important role as a supplement film in providing the current resistance and electrical strength required for InSb p-n diode applications.

The anodic oxide and Photo-CVD oxide can be prepared as a composite passivation layer on the surface of a InSb p-n junction to give the optimum surface potential and low density of surface state required for low leakage current InSb p-n diodes in addition to provide mechanical and chemical protection to the InSb p-n junction and surfaces.

2.6 References:

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