Chapter 3 Mesa Structure Formation on InSb

3.1 Overview

Mesa structure is generally used to define the device dimension. In array devices, mesa etching is used to provide the isolation between different diode elements. It is the most versatile approach to realize the p-n diode performance demonstration. As shown in Figure 3.1, mesa structures can be implemented into device applications for both the diffusion and ion implantation doping fabrication schemes. By comparing to the planar process, mesa process provides at least the following advantages:

- free contamination from the masking materials before device fabrication process.
- fast protype by simple chemical etching instead of complex mask
- cost effective by economic chemical etching instead of masking material processing.

However, the chemical etching is itself a series of combination of processes which controlled by corresponding mechanisms. The transport of etching species from the bulk of chemical to the surface through diffusion, absorption, reaction, and complexing has severed effect on the morphology and mesa structure.

3.1.1 Background and challenge

For <111> InSb blanket wafer, the pn junction is obtained by diffusion of Cd impurity into n-type substrate with two temperature zone technology[1] Mesa etching process is employed to create isolated pn junction islands on InSb substrate to generate mesa type pn junctions. Fig. 3.2(a) is the schematics representation of InSb p+n diode with ideal mesa structure in infrared image array. The mesa is formed by removing the p-type material completely along with etching part of the n-type substrate.

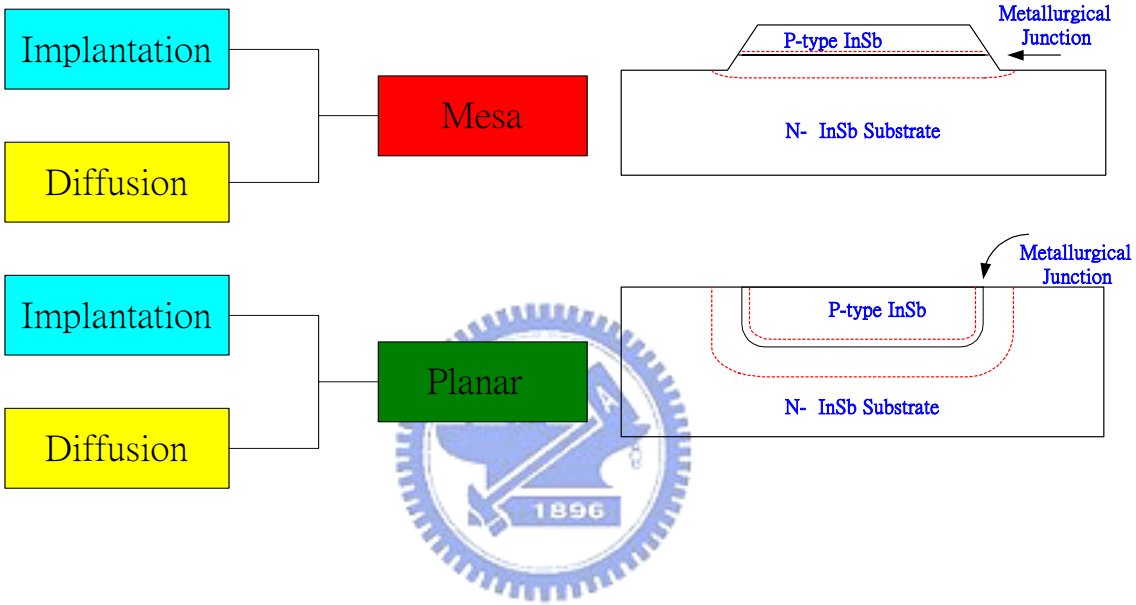

Figure 3.1 Applications of mesa structure in p-n diodes development scheme.

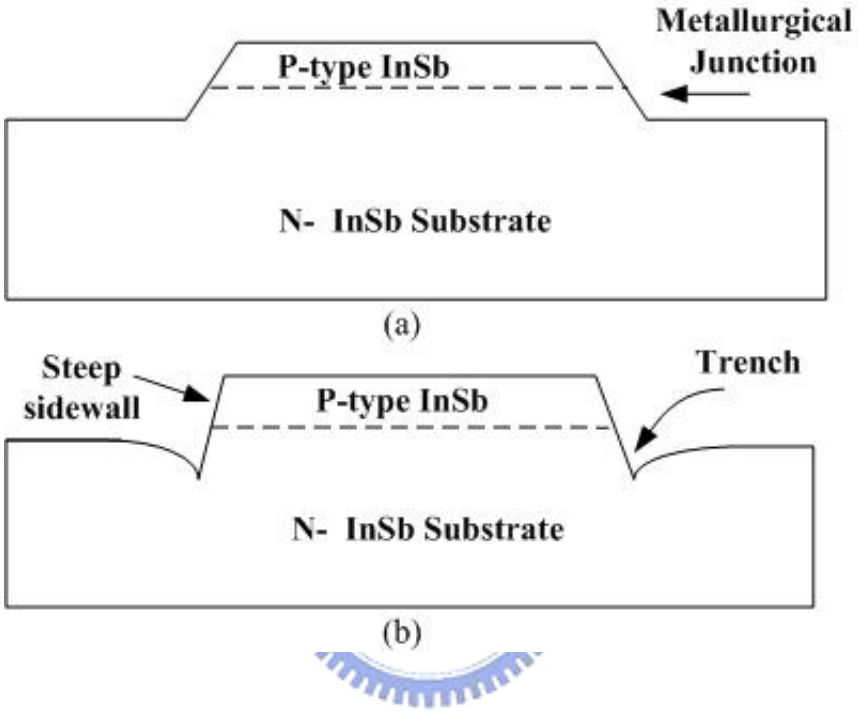

Figure 3.2 Schematic representation of (a) ideal mesa structure (b) mesa structure etched by lactic acid / nitric acid solution with volume ratio 10:1.

The metallurgical junction will be formed ideally in the middle of the mesa height. This etching process defines both the lateral dimension and the step profile. The surface and sidewall of the mesa structure will make direct interface with the succeeding passivation or dielectric film. The control of surface morphology in mesa type p+n junction is an important issue due to the relevant characteristics caused by sensitivity of electric field[2] of the exposed peripheral.

Geometry scale-down in junction area with low leakage current and high breakdown voltage in the reverse bias region is highly desired for applications of advanced high-density format area arrays[3]. High performance infrared image applications require the detection pixels to have uniform response to radiation at interested infrared spectral ranges. This indicates that the formation of uniform detection pixel structures in an array is one of the fundamental requirements for device processing.

There were a few literature reported that the success of attaining more accurate geometry control over the small device structures by utilizing dry etching processes on InSb[4-7]. However, the sidewall damage caused by ions physical sputtering process may result in electrical degradation[8-11] of devices, especially for narrow bandgap compound semiconductor material. In addition to the damage issue, low etching rate and expensive capital investment are two disadvantageous factors of using dry etch technology in getting cost effective process. Overall, at present, wet etching process is still a widespread accepted way to delineate the mesa structure on the InSb wafer surface.

3.1.2 Conventional process and limitations

Numerous wet etchants[12] and various etching processes have been investigated to provide the optimum surface requirements. Conventionally, lactic/nitric acid solution was used for etching <111> InSb to manufacture photovoltaic detectors[7,13]. Unfortunately, the reproducibility and the uniformity of mesa structures in image sensor prepared by this conventional etching solution can't be easily controlled[7]. Schematically, as shown in Figure 3.2(b), lactic acid /nitric acid mesa etching has problems in sidewall profile with asymmetry slope for opposite two edges and trench or non-flat bottom at the mesa edges.

For infrared photodiode applications, a low temperature insulating film is required to provide high resistance to isolate the leakage paths between p-type and n-type materials on the surface of mesa structure. Moreover, the interface between the mesa including the n-type and p-type regions and the insulating film is required to have low interface state and fixed charge to minimize the field induced leakage current. As shown in Figure 3.3, a schematic representation of a diode structure with ideal mesa structure indicates that a composite stack of anodic oxide and deposited CVD oxide is adopted as the passivation layer. Obviously, the mesa structure succeeding the mesa formation process will seriously influence the performance of this passivation layer. Figure 3.4 shows the cross section view of one sensing pixel in an real InSb/ROIC hybridized image sensor module with mesa structure wet etched by lactic acid/nitric acid. The mesa height is equal to 1.32 um with sidewall angle 69^{o}. The step coverage of the deposited CVD oxide on the sidewall is 50%. It reveals the typical problems of mesa etching in lactic acid/nitric acid solution, such as steep slope at step sidewall, bad step coverage for dielectric film, and non-flat bottom

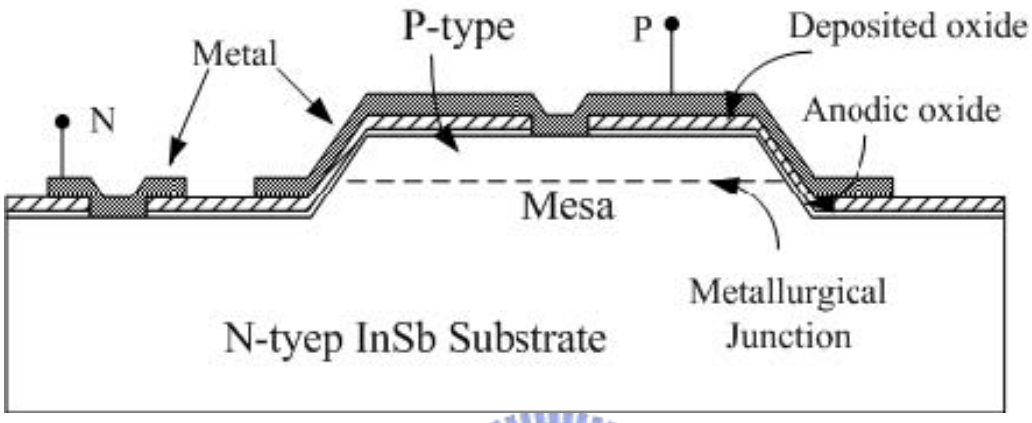

Figure. 3.3 Schematic representation of the InSb p+n diode fabricated on an ideal mesa structure in a two-dimensional infrared image array.

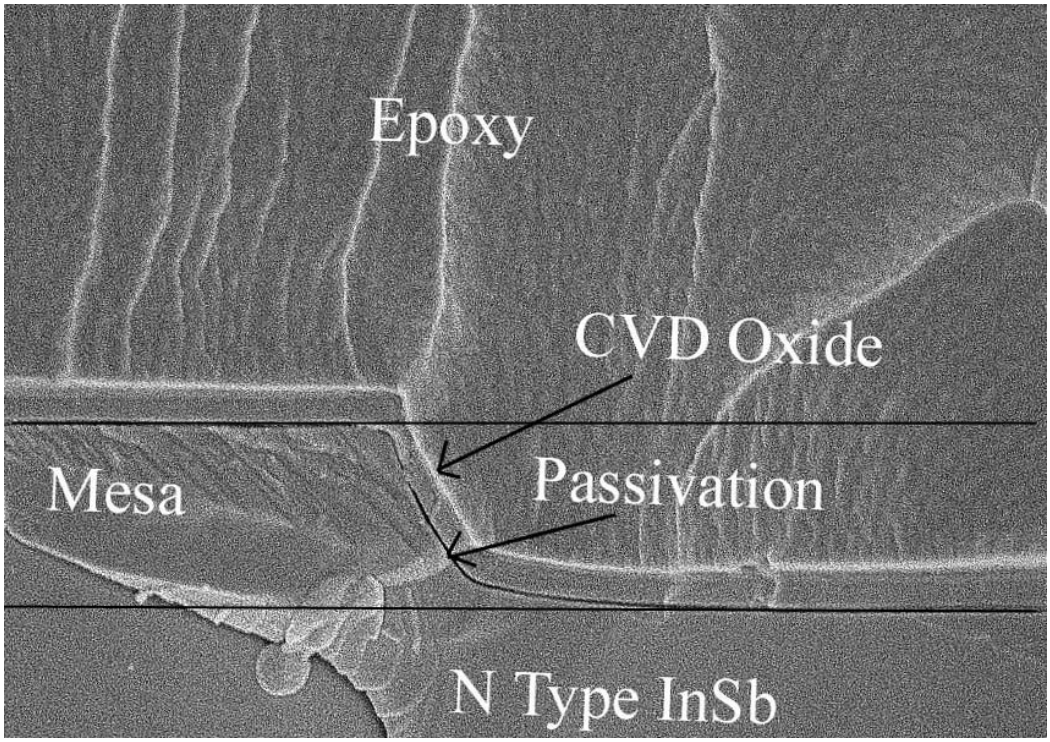

Figure 3.4 Part of one sensing pixel in InSb/ROIC hybridized image sensor with mesa etched by lactic acid/nitric acid solution.

at etching windows.

3.1.3 New approach

Citric acid/hydrogen peroxide solutions have been studied intensively in processing of GaAs based materials[14-16] and device structures due to its superior performance with respect to etching selectivity. The research reported by Otsubo *et al.* indicated that GaAs etching can be controlled under surface reaction rate-limit mechanism[17].

This etching mechanism is expected to have better control on uniformity of device's structure due to its linear proportional relation to etching time and its independence on agitation and exposed etched area. This paper is the first report of its kind in addressing the issues of uniformity of device's structure in terms of fabricating InSb high density detector array. This chapter will evaluate and compare the performances of two different chemical systems in etching <111> InSb through morphology inspection and electrical measurements.

3.2 Experiments

3.2.1 Wafer treatment and chemical preparation

Te-doped <111> InSb with an electron concentration of 1- 2 x 10^{15} atoms/cm^3 was used in this etching study. Standard H-line lithography technology and AZ-1350 photoresist were used to pattern the wafer surface with masked and exposed area for mesa structure etching. Starting etching condition was a surface etching by using diluted 1/100 HF solution for 2 min followed by a 1 min immersion in diluted hydrogen chloride solution to insure a native oxide thickness below 15Å. After mesa

etching, the samples were rinsed in DI water for 5min and then dried with nitrogen.

All the etching solutions in this study were used at room temperature. For lactic acid/nitric acid mixture, the 90% lactic acid was mixed with 70% nitric acid at two different ratios 10:1 and 20:1 by volume ratio. For citric acid/hydrogen peroxide mixture, anhydrous citric acid solid was dissolved in deionized water with concentration of 50% by weight. The 30% hydrogen peroxide was added by volume ratio after one day stabilization of the citric acid dissolution process. The surface morphology and the etching rate of the InSb mesa structures corresponding to these two chemical systems were measured by optical microscope, AFM and Dektak surface profiler, respectively. The step height is defined by the mesa plateau in conjunction with the etched flat bottom regions as shown in the insert of Figure 3.5.

3.2.2 Characterization and analysis method

The pn junction device structure around the mesa step sidewall for typical detector fabrication process using citric acid/hydrogen peroxide solution was investigated and demonstrated by field emission scanning electron microscope. Current-voltage characteristics of the InSb p+n diodes fabricated by lactic acid/nitric acid mixture and citric acid/hydrogen peroxide mesa etching were compared. In addition, the distribution of pn junction dark current was measured across 2 inch InSb wafer through computer controlled cryogenic probe system operated under 77 K.

3.3 Results and Discussions

The processes of chemical etching on semiconductor surface involve diffusion of etching species toward the surface, absorption and reaction, complexing and dissolution, diffusion of complexing agent into the etching solution. Usually, the chemical etching is categorized with diffusion and reaction-rate limit mechanisms.

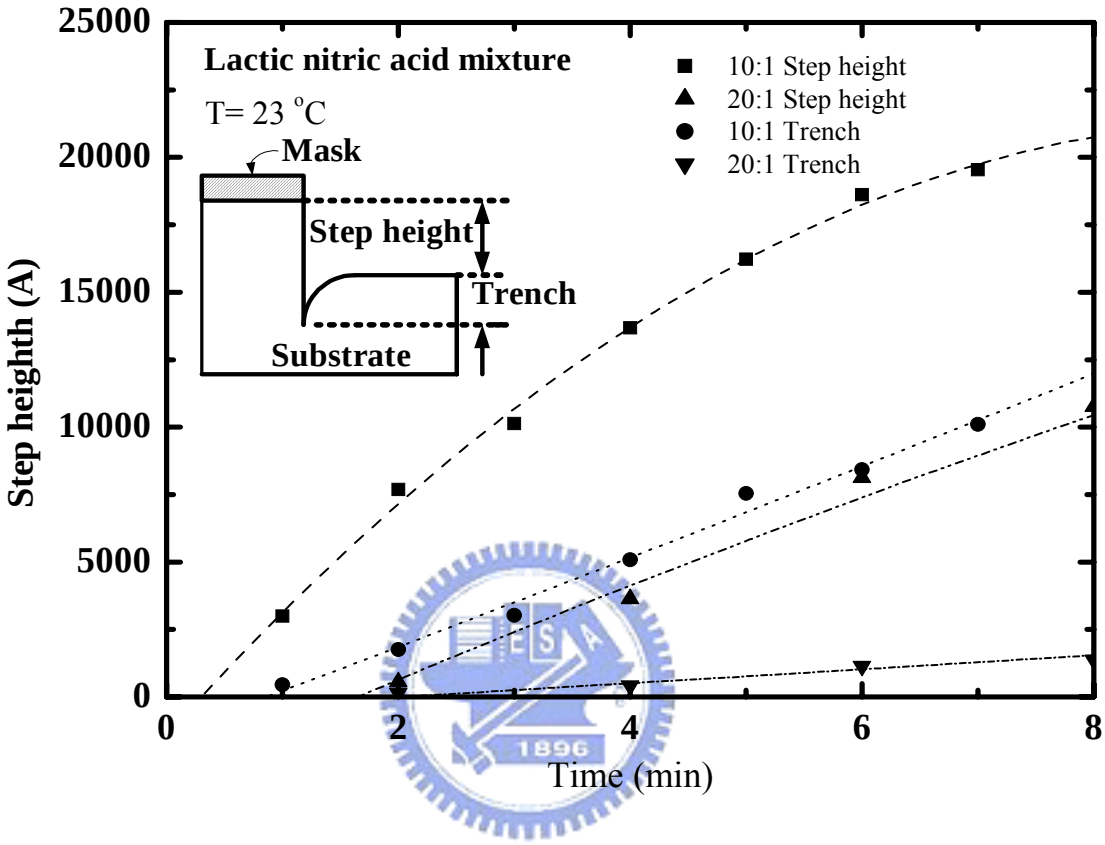

Figure 3.5 Step height and trench depth of <111> InSb mesa etched by 10:1 and 20:1 lactic acid/nitric acid solutions as a function of etching time at 23 ℃.

The general phenomenological differences are summarized in Table 3-1.

3.3.1 Etching Characteristics in lactic acid/nitric acid solutions

Lactic acid/nitric acid solution with volume ratio 10:1 is a well known polish etchant[12] to InSb substrates. The morphology is highly sensitive to stirring during the patterned wafer etching. To have consistent results, the upward wafer surface should be carefully loaded into the etching bath in order to keep a flat wafer surface during etching.

Figure 3.5 shows the etching time dependence of the step height for both 10:1 and 20:1 lactic acid/nitric acid solutions at 23 ℃. The legends and arrows in the figure indicate the corresponding solutions and axis to be referenced. The step height tends to saturate after 6 minutes etching in 10:1 solution, and 20:1 solution also has the same saturation trend but it occurred around 20 minutes. Further analysis of the etching data indicates that the step height dependence on etching time roughly follows square root relation. As shown in Figure 3.6, the step height indicates linear proportional relation versus the square root of etching time in the 10:1 lactic acid/nitric acid solutions.

The mesa trench as defined in the same graph was extracted from the measurement of surface profiler. The curves for both 10:1 and 20:1 solutions indicate its linear dependence on etching time in the range of interest. In contrast to the square root dependence of step height on the etching time, the mesa trench will become more severe as the step height become higher. Typically, for 1.5um mesa height, the 10:1 mesa trench will drop to 35% of mesa step height. On the other hand, the 20:1 solution can effectively suppress the trench effect to about 15% of mesa step height. By referring to Table 1, the square root dependence on etching time along with the

Table 3-1 Characteristics comparison of diffusion-limited and reaction-limited mechanism in chemical etching

Characteristics	Diffusion Limit	Reaction Limit
Morphology	Smooth	Isotropic
Rate control	Nonlinear	Linear
Uniformity	Bad	Good
Process Window	Small	Large
Sidewall	Trench and Bad coverage	Good
Chemical Compatibility	Good	Good

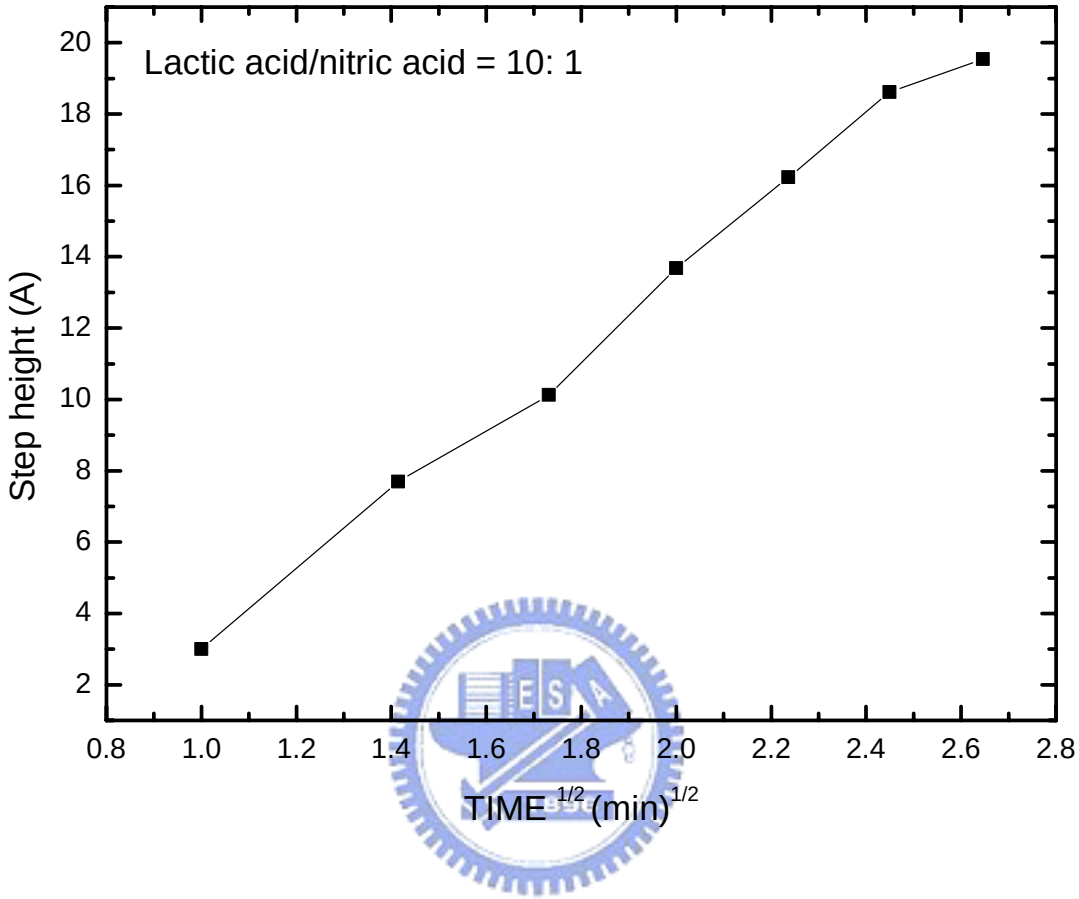

Figure 3.6 Etching time dependence of mesa step height etched by 10:1 lactic acid/nitric acid.

stirring effect, and the mesa trench effect indicate that the etching of <111> InSb in lactic acid/nitric acid solution 10:1 is predominantly controlled by diffusion rate-limit mechanism. According to the carrying out of this lactic acid/nitric acid mechanism, nitric acid plays the role of controlling the reaction rate due to the fact that the transport of fresh oxidizing species can be provided by its presence.

The trench and the stirring effects were induced by non-uniformly supplying oxidizing species during the etching process. The ratio of masked and exposed area of patterned mesa array can influence the flow pattern of oxidizing species especially in the lateral direction which results in the trench in the edges of mesa Besides, from the measurement of surface profiler and optical microscope, there always show non-symmetry phenomena in the trench depth and slope of sidewall even for two adjacent parallel mesa edges. It can be inferred that the secondary etching species source located above the photoresist will transport the etching species laterally along the substrate surface which results in variation on trench depth and sidewall slope.

In order to maintain the good electrical properties, the thickness and dielectric properties of succeeding anodic oxide and CVD oxide have to be prudently adjusted to cope with this trench effect. Therefore using the lactic acid/nitric acid solution will narrow down the process window and result in the non-uniformity issues for high density image array. Diluted lactic acid/nitric acid solution, for instance 20:1 in this study, may help to reduce the trench in percentage of step height. However, prominent mesa trench and sidewall slope variation problems can't be completely removed despite the fact that the lactic acid/nitric acid solution was prepared using volume ratio up to 40:1.

3.3.2 Etching Characteristics in citric acid/ hydrogen peroxide solutions

To search practical etching conditions for (111) direction oriented InSb in citric

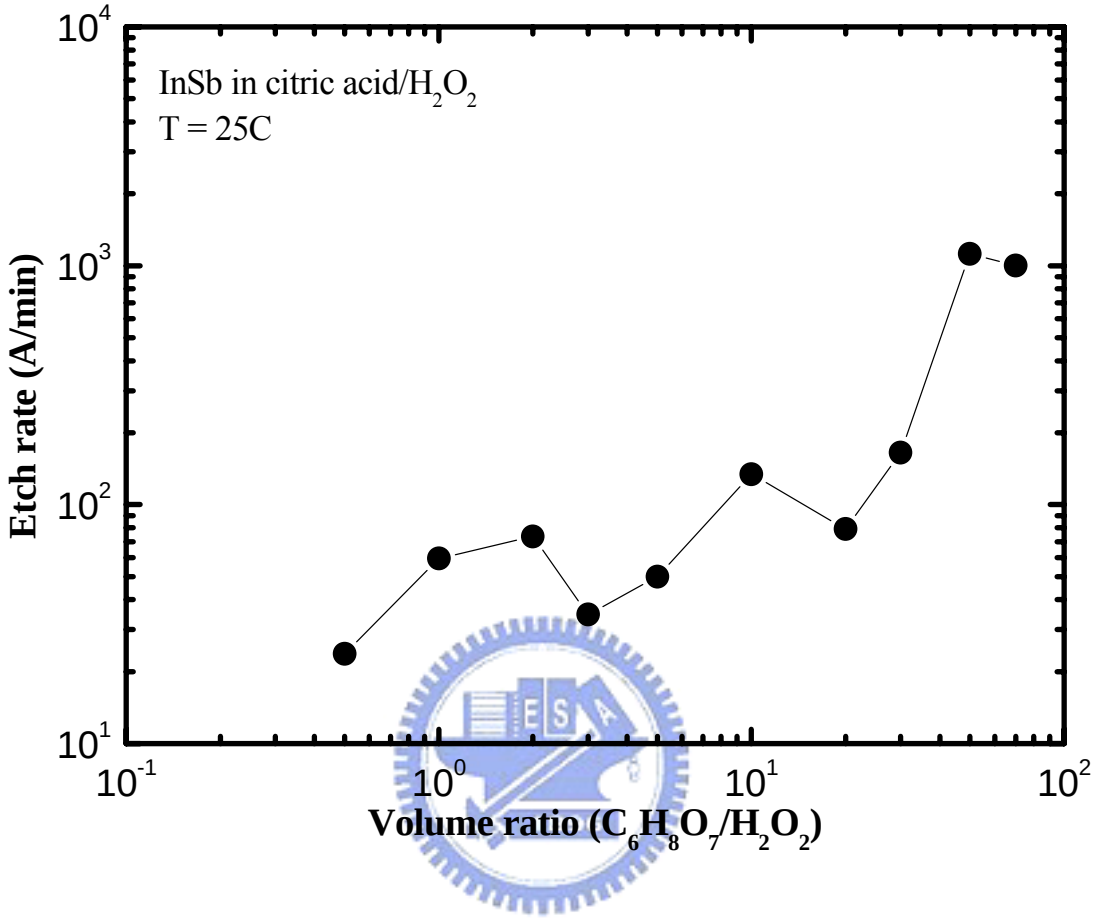

Figure 3.7 Volume ratio dependence of etch rate in citric acid/hydrogen peroxide solution under 25℃.

acid/hydrogen peroxide solution, the etching rate dependence of volume ratio of citric acid/hydrogen peroxide solution was studied. As shown in Figure 3.7, the etch rate shows a very sharp increase for volume ratio larger than 30:1 and will fall off after 70:1. For pure citric acid, there is no detectable etching step that can be measured for 10 minutes immersion. This tendency is similar to that of etching GaAs and AlGaAs[16]. In contrast to Figure 3.5, Figure 3.8 is the InSb etching time dependence of the mesa height in citric acid/hydrogen peroxide solution at 18 ^{o}C corresponding to the volume ratios 50/1 and 10/1 respectively. The mesa height indicates sublinear proportional relation to the etching time. The etch rates tends to increase with respect to etching time. This phenomenon can be explained by the dissociation effect of hydrogen peroxide during the etching. The etching of InSb in citric acid/hydrogen peroxide solution didn't have an obvious stirring effect or mesa trench effect in the range of interest.

In Figure 3.9, the temperature dependence of the etch rate is shown. The etching rates increased exponentially with increasing etching temperature. By fitting with exp $^{(-Ea/kT)}$ form, where Ea and T represent the activation energy and temperature respectively, k is the Boltzmann constant. Two different activation energies were observed as the temperature changed from 18 ℃ to 60 ℃. For temperature higher than 30 ℃, the activation energy is 10.1 Kcal/mole. This result is consistent with results of etching in 10:1 solution previous published[14]. It represents the surface adsorption process[17] of the oxidizing molecules on partially oxidized surface; it also means that the etching is controlled by surface reaction-rate limit mechanism. However, for temperature near the room temperature region, the activation energy is as high as 39.9 Kcal/mole. So, for practical mesa structure preparation, temperature higher than 30 ℃ will be more appropriate for process throughput control.

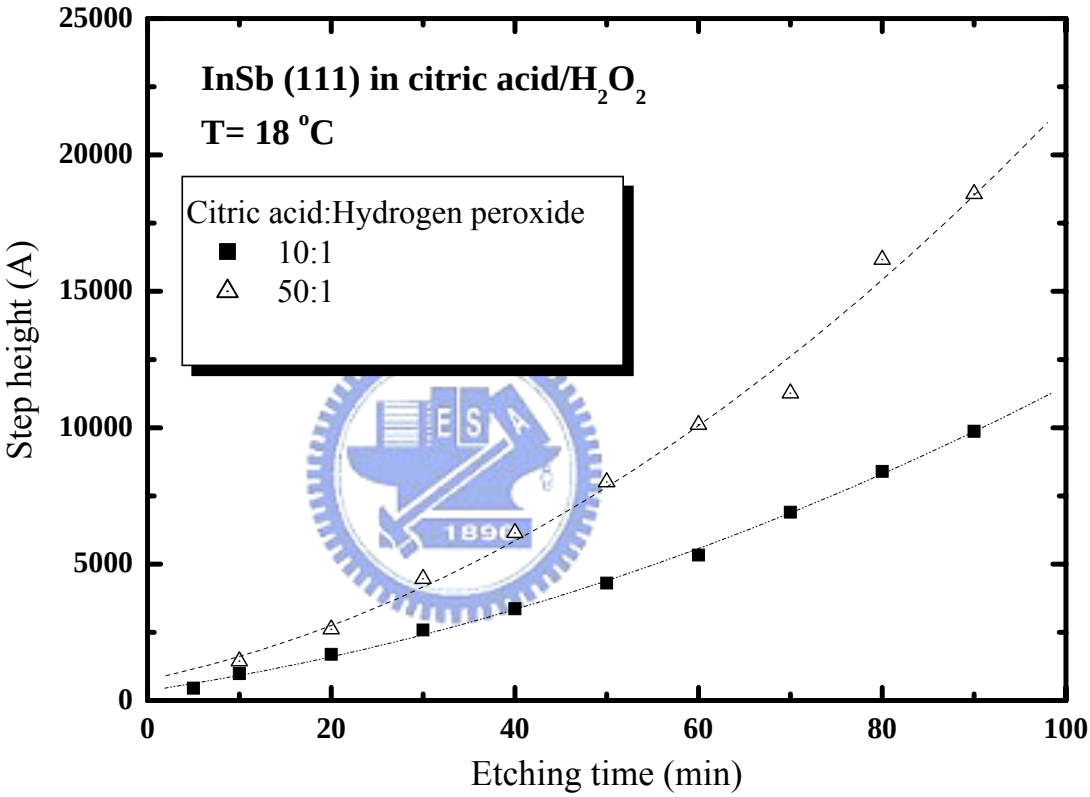

Figure 3.8 Step height as a function of etching time in 10:1 and 50:1 citric acid/hydrogen peroxide solution.

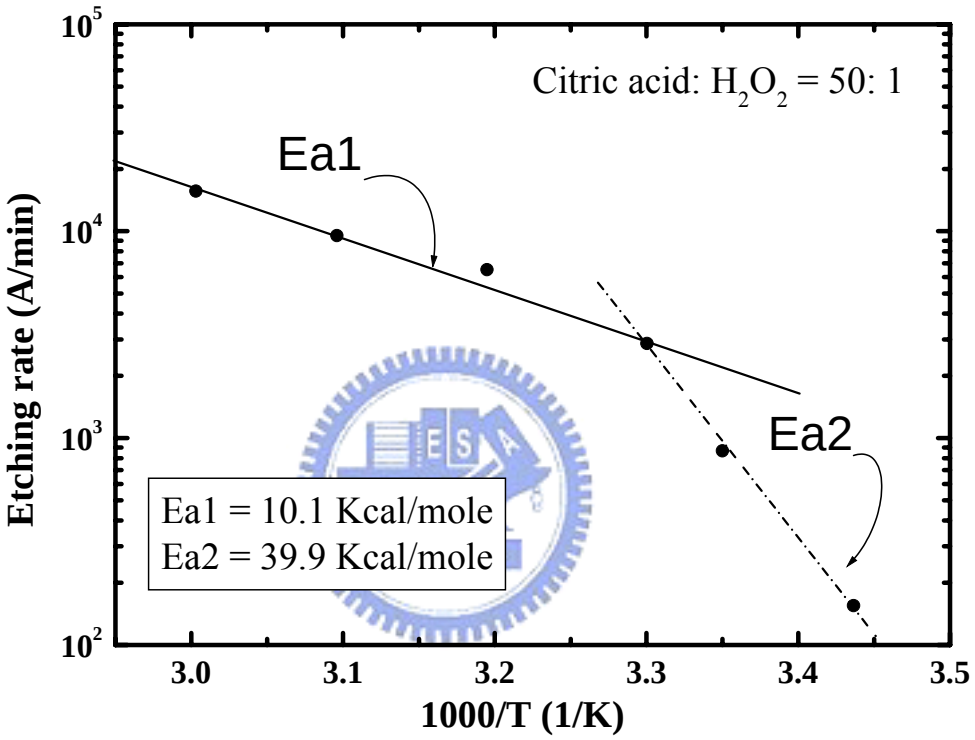

Figure 3.9 Temperature dependence of the etching rates for InSb in the citric acid/ H_2O_2 solution with volume ratio 50:1 in the temperature range from 18℃ to 60℃ The activation energies Ea1 and Ea2 can be extracted from the data fitting of the etching rate vs 1/T in Logarithmic scale.

3.3.3 Surface morphology and step coverage of mesa structures

As shown in Figure 3.10, the AFM mapping and the cross section view of InSb 2-dimensinal mesa array created by etching in lactic acid/nitric acid solution indicates that there are two structure issues in the mesa array. One is a non-flat bottom surrounding the mesa plateau of which it corresponds to the trench phenomenon measured by profiler. The other is steep step sidewall; the slope 62^{o} of the sidewall is evaluated by the AFM scanning data, which is a little smaller than the result from Figure 3.4.

On the other hand, Figure 3.11 shows the similar mesa array structure created by citric acid/hydrogen peroxide solution etching at 50:1 volume ratio. The mesa height is 1.9um. The morphology for both the sidewall and the isolation spacing between mesa plateaus is relatively smoother and more uniform as compared with that of mesa structure etched by the lactic acid/nitric acid. From the cross section, it can be seen that the slope of sidewall for all the mesa edges shows relatively higher symmetric structure as well. The sidewall angle is equal to 54^{o} and it is 13% smaller than that of the mesa sidewall etched by lactic acid/nitric acid solution.

To confirm the step coverage properties, as shown in Figure 3.12, SiO dielectric and metal film with thickness 3500Å and 2000 Å are evaporated on the top 1.85 um mesa structure etched by lactic acid/nitric solution respectively It has been seen obviously that both the SiO and Cr/Au metal layers have break point at top corner of the mesa step. This result provides a direct evidence that the steep sidewall etched by lactic acid/nitric acid can cause functional failure of succeeding passivation layer.

On the contrast, as shown in Figure 3.13, the mesa with 1.75um step height was prepared by wet etching process in citric acid/hydrogen peroxide solution. A dielectric coating 2800Å SiO film and 1200Å Au metal film were deposited on the InSb surface

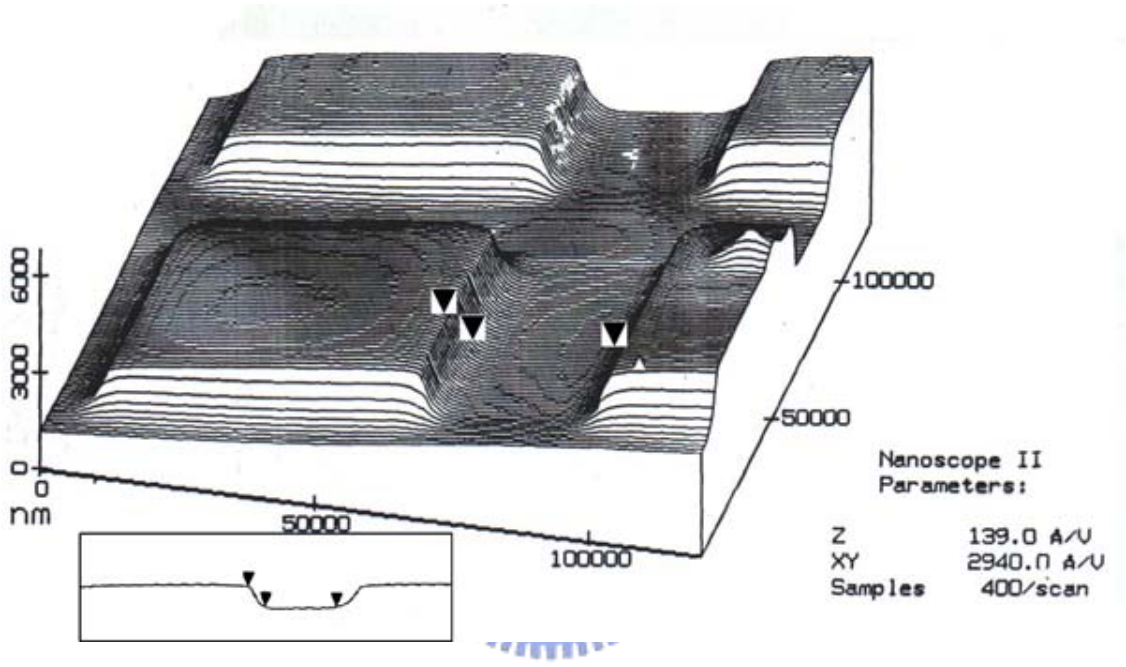

Figure 3.10 AFM Photograph and cross section view of InSb mesa array etched by 10:1 lactic acid/nitric acid solution.

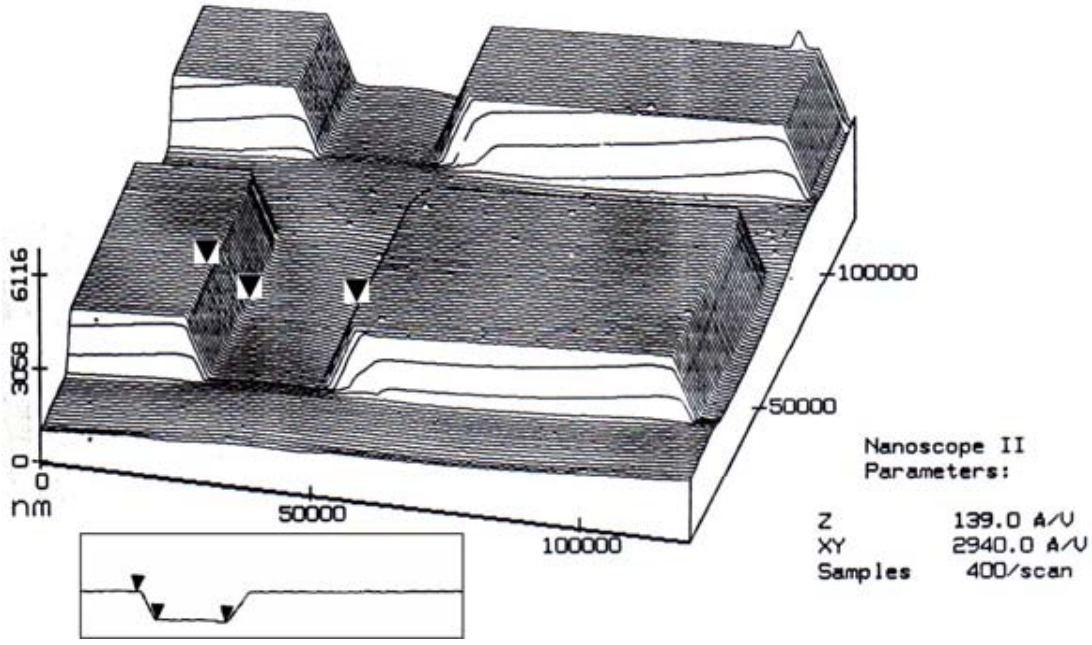

Figure 3.11 AFM Photograph and cross section view of InSb Mesa array created by 10:1 citric acid/hydrogen peroxide solution etching.

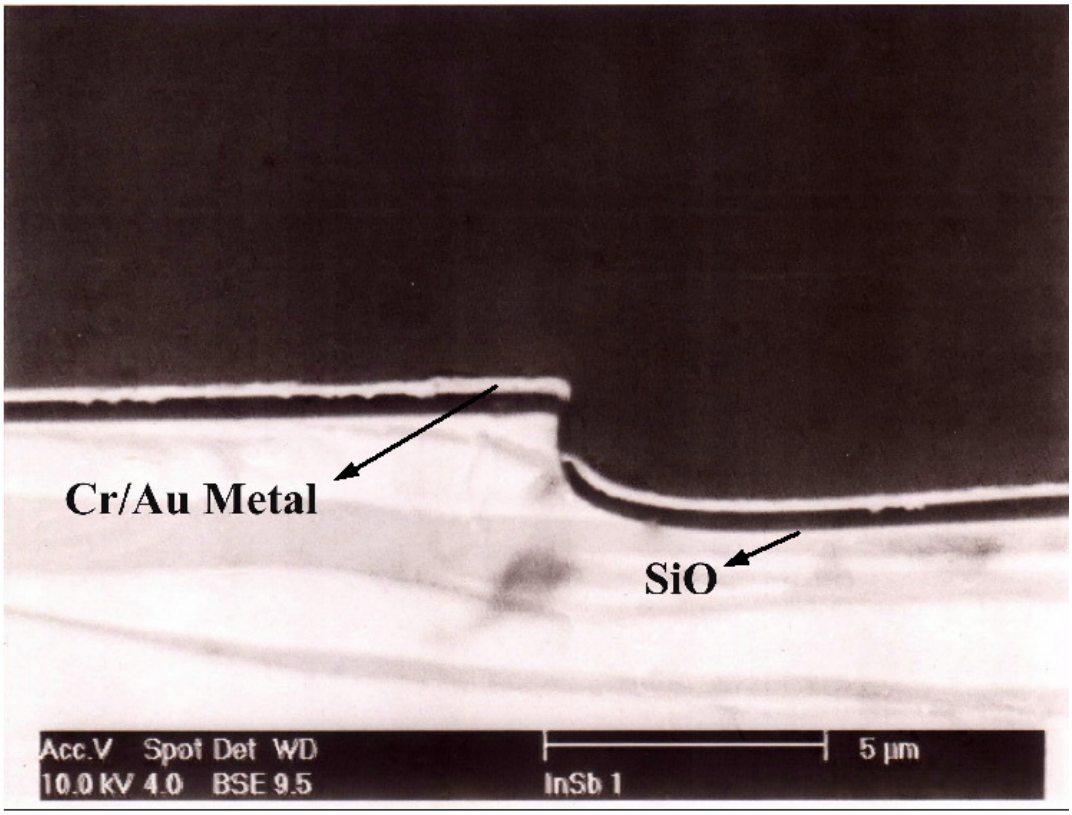

Figure 3.12 SEM photomicrograph of the mesa prepared by lactic acid/ nitric acid solution on (111) B InSb substrate. The surface and sidewall were coated by 3500 Å SiO and 2000 Å Au metal film respectively.

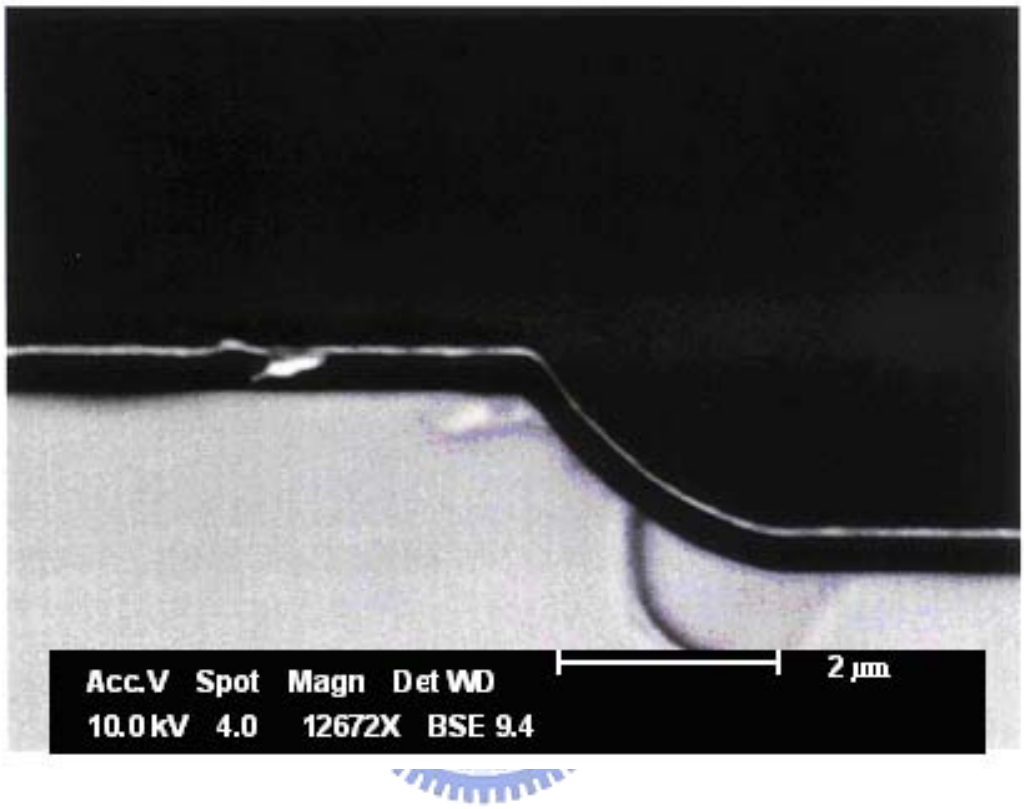

Figure 3.13. SEM photomicrograph of the mesa prepared by citric acid / hydrogen peroxide solution on (111) B InSb substrate. The surface and sidewall were coated by 2800 Å SiO and 1200 Å Au metal film respectively.

by thermal evaporator system respectively. The maximum film thickness reduction occurs at the falling edge of this mesa structure. The step coverage is 71% for the dielectric film. It presents nearly 20% superior to the device structure prepared by lactic aicd/nitric acid mixture. This result is believed to guarantee good performance for our thickness requirement for dielectric layer running over the step height and it also provides excellent integrity of device integration using mesa array etched by citric acid/hydrogen peroxide solution for applications of large format image array.

3.3.4 Electrical characterization of diodes made of different mesa structures

A simple blocked diode test structure with mesa dimensions of 25X25 μm^2 was prepared using the same device fabrication process as described in ref. 7 for both the lactic acid and citric acid mesa etching devices. The current-voltage characteristics of these p+n diodes were measured under a 77 K background. As shown in Figure 3.14, in the forward-bias region, the dark currents almost coincide. This indicates the consistency of the current flow mechanism across the junction barrier in these two devices. In the reverse-bias region, the A34 sample diode prepared with the lactic acid/nitric acid solution shows the soft breakdown phenomenon, as the reverse bias is larger than 120 mV. However, the C03 diode fabricated by citric acid/hydrogen peroxide solution shows just a slight increase in dark current even for a bias larger than 250 mV. It is evident that the small-area InSb p+n diode fabricated using citric acid/hydrogen peroxide solution has a higher breakdown voltage and a lower dark current. These results may be attributed to the morphology differences in the mesa edges of the InSb p+n diodes created by these two different etching solutions.

The mesa etching in citric acid/hydrogen peroxide solution is assumed to create different surface conditions to the succeeding dielectric preparation process with respect to the etching in lactic acid/nitric acid solution. The different surface

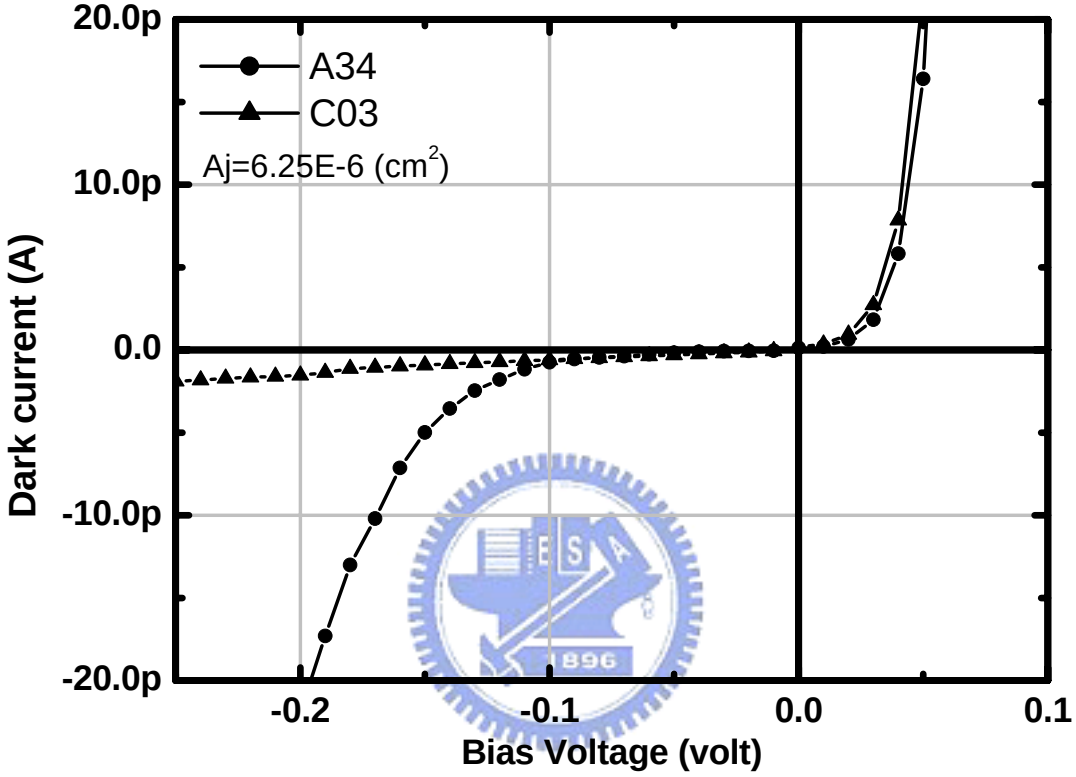

Figure 3.14. Current-voltage characteristics of InSb p+n diodes, A34 and C03 are corresponding to the mesa structures formed by etching in lactic acid/nitric acid solution and citric acid/hydrogen peroxide solution respectively.

conditions may be formed by two reasons. First, the dominant control mechanism in the competing processes of surface reaction and mass transport of etching species in the mesa etching is different. Second, the chemical species involved in the surface oxidation and complexing process are different. Obviously, these differences will result in the variation of residual natural oxide thickness and chemical composition on the InSb surface.

To evaluate the differences in electrical performance especially for the forward region, the current-voltage characteristics of larger test devices with junction area of 150X150um^2 and mesa etched by these two solutions are measured under 77K background. As shown in Figure 3.15. In the forward bias region, the ideal factor of the diode C03B made by the citric acid/hydrogen peroxide mesa etching is 1.267, it is close to the ideal factor 1.234 obtained in the diode G108 made by lactic acid/nitric acid mesa etching for bias range from 10mV to 150mV. The R_0A of diode C03B is 1.66X10^6 Ω–cm^2. The carriers transport mechanism of C03B is assumed to be compatible with diode G108 which is rated as high quality p+n diode. These results ensure that the mesa etching process in citric acid/hydrogen peroxide can provide good electrical properties in addition to the advantage of structure uniformity to the InSb p+n diodes in image array.

The current-voltage characteristic of a p-n diode is highly electrical field sensitive to the semiconductor surface and interface between semiconductor and passivation layer. The dark current in the reverse-bias region is one of the important figures of merit for an InSb pn junction, which normally operated under zero-bias or reverse-bias conditions in detector applications. As the dimensions of mesa structures continue to be scaled down, the dark current originating from the mesa peripheral becomes dominant with respect to the junction area. The soft breakdown and high dark current may originate from the high local electric field across the junction around

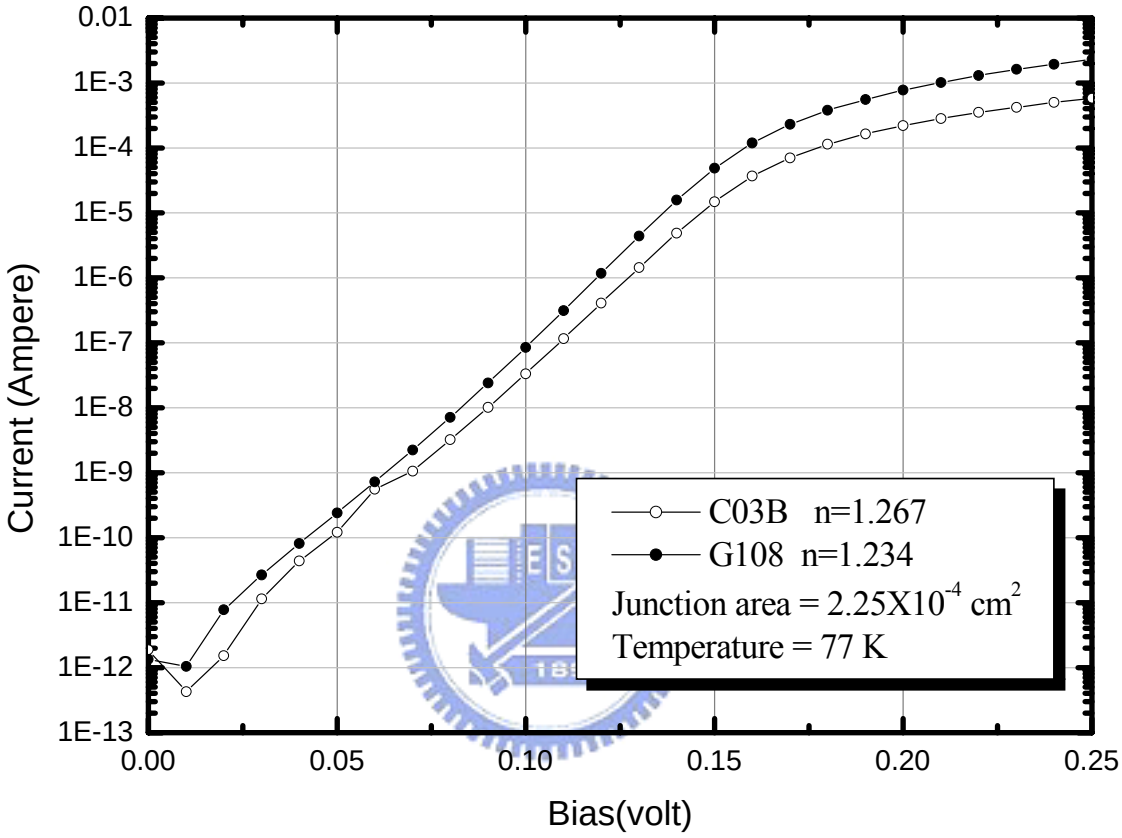

Figure3.15 Current-voltage characteristics of InSb p+n diodes, devices G108 and C03 are corresponding to the mesa structures formed by etching in lactic acid/nitric acid solution and citric acid/hydrogen peroxide solution respectively .

the mesa edges when a reverse bias is applied due to the steep sidewall and trench effects. The elimination of the trench effect and the reduction of the slope of the mesa edge step sidewall by the citric acid/hydrogen peroxide etching process may effectively reduce the local electrical field across the junction near the mesa edge.

Small mesa diodes were prepared and distributed on a 57 mm diameter InSb wafer for both the lactic acid and citric acid mesa etching processes. The uniformity of the electrical performance of small mesa diodes was measured by taking dark current data at five different reverse biases under a 77K background. Figure 3.16 (a) and Figure 3.16(b) show the histograms of dark current distribution with respect to the change in various reverse biases for the mesa structures created by chemical etching in the (a) lactic acid/nitric acid solution and (b) citric acid/hydrogen peroxide solution.. A logarithmic scale was used on the x-axis of the histogram for easy comparison of dark current data. The statistics are based on a total of 704 InSb p+n test structures. The average and standard deviations for both the A34 and C03 devices are given in Table 2 with reverse biases as the parameters. For a low reverse bias, both the devices indicate a good uniformity with a nearly normal distribution. As the reverse bias was increased, the mean value of dark current moved to a higher level.

When the reverse bias was higher than 130 mV, the dark current distribution increased and scattered significantly for the lactic acid/nitric acid mesa etching. This result is consistent with the soft breakdown phenomenon of the current-voltage characteristics of the A34 device in Figure 3.14. However, Figure 3.16(b) shows that the devices prepared with the citric acid/hydrogen peroxide mixture have relatively small increments and limited spread in the dark current distribution. For a reverse bias smaller than 190 mV, the mean value of the dark current increased linearly in response to the reverse bias voltage. The standard deviation of the dark current distribution was estimated to be 0.175 pA for a reverse bias up to 130 mV.

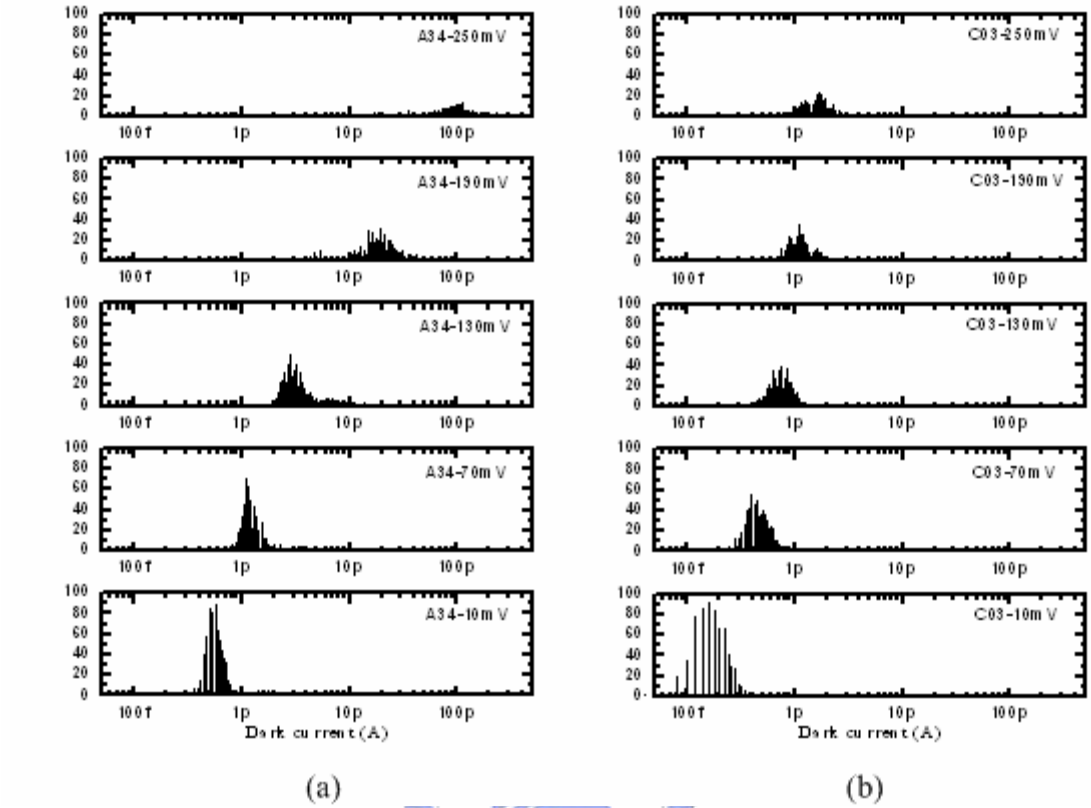

Figure 3.16 Dark current histograms of 704 InSb p+n junction test structures at various reverse biases under 77K background. The 25μm square mesa structure is created by chemical etching in the (a) lactic acid/nitric acid solution and (b) citric acid/hydrogen peroxide solution.

Table 3-2 Statistics of dark current for A34 and C03 with various reverse biases.

	10 mV	70 mV	130 mV	190 mV	250 mV
Mean-A34	0.646p	1.287p	3.799p	23.498p	106.741p
Std D.-A34	0.269p	0.364p	1.723p	11.384p	48.237p
Mean-C03	0.179p	0.471p	0.776p	1.186p	1.698p
Std D.-C03	0.064p	0.120p	0.175p	0.335p	0.437p

This ultra-low dark current level with a highly uniform distribution was attributed to the fact that the mesa structure is uniform and the dielectric/passivation stack layer is well prepared.

3. 4 Summary

The wet etching of InSb in citric acid/hydrogen peroxide solution provides mesa structures with advantageous characteristics of symmetric mesa edges, slope sidewalls, and flat bottom surfaces for the deposition of successive dielectric or passivation layer. It has been shown that ideal (111) direction oriented InSb mesa structures for high format array applications with more perfect surface integrity can be realized with citric acid/hydrogen peroxide chemical system compared to the lactic acid/nitric acid solution.

The basic characteristics of wet etching including etching time dependence of the etch depth, stirring and trench effect, and temperature dependence of etching rate have been investigated and compared. It has been shown that the etching of (111) direction oriented InSb in lactic acid/nitric acid solution is dominantly controlled by the diffusion rate-limit mechanism. In contrast, etching in citric acid/hydrogen peroxide solution is dominantly controlled by the surface reaction rate-limit mechanism.

It should be noticed that surface reaction limit mechanism of wet etching is more suitable for controlling uniformity of mesa array structure as opposed to diffusion limit chemical system.

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Chapter 4 Small Pixel InSb Diode Formed by Be^+ Implantation

4.1 Overview

Indium antimony is a well known material to be used for infrared detectors in the 3 to 5 μm spectral range. Two dimensional detector array and silicon based CMOS image readout integrated circuit can be pixel- to-pixel interconnected to form backside-illuminated sensor module using hybridization technology.

Solid-state Cadmium diffusion into InSb is a conventional technology to give high performance p-n junction for medium wavelength 3 to 5 um infrared detector applications. Unfortunately, as shown in Figure 3.1, solid-state diffusion technology has inherited disadvantages for technology development extend to large format image sensor chip and large wafer processing. Such as the following features:

- Horizontal placement of wafer
- Vacuum sealed quartz tube
- Two temperature zones diffusion

Apparently, these features will result difficulties in the control of the following issues:

- Uniformity: doping level, doping profile
- Load/unload: higher risk in vacuum sealing and ampoule breaking process
- Wafer position alignment to the furnace in the vacuum sealed ampoule

Ion implantation has been demonstrated and reported in producing InSb p+n junction diodes with its inherent advantages such as planar processing and uniform characteristics for infrared detector array applications. Previously, Beryllium (Be) has been identified as an optimum p-type dopant in InSb due to

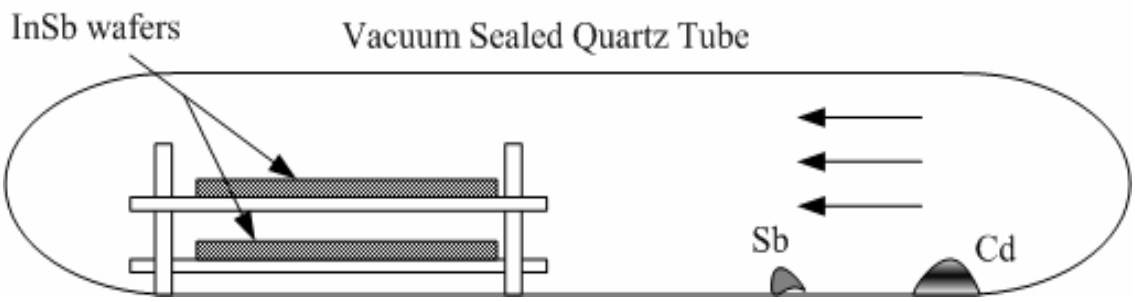


Figure 4.1 Schematic of cadmium solid-state diffusion setup for the InSb wafer. Two temperature zones furnace was used..

its lower generation rate resulted from implant damage[1]. However, most of the literatures reported so far require extra insulated metal gate to control the surface potential of junction peripheral[2-3].

Continuation of scale-down of geometry in pixel size for focal plane array is highly desired for high resolution and large field of view (FOV) applications of advanced high density infrared imaging arrays. The reduction of image pixel size implies that FPA chip composed of 2D focal plane array would become much smaller. The overall costs will be likewise reduced because of the facts that each single wafer can produce more FPA chips. At the same time, the development of using larger format can become feasible when the reduction of pixel size is further diminished.

There are two main issues that impede the development of scale down of pixel size: 1) the complexity of device structure caused by the usage of control gate, 2) the degradation of p^+n diode's performance with respect to the reduction of pixel size. In order to shrink the size of the pixel and increase the number of pixel to meet the requirements for infrared image array with leading high density and large format, in the past 30 years, a lot of researchers[4-8] had taken the intensive programs in developing FPA with larger format to reach this goal. As shown in Figure 4.2, in contrast to the exponential increase of the pixel number per InSb FPA chip versus the development time, the pixel size decrease exponentially almost in the last two decade and slowed down to 30um in the year 1992. Then the progress in scaling down of pixel size become limited, the major effort in FPA development was focus on the large chip size and large format sensor module.

In this work, a simple Be^+ implanted InSb p^+n diode structure without the control gate is proposed to meet the requirements of both small pixel area and large format for applications of two-dimensional focal plane array with high density. The structure

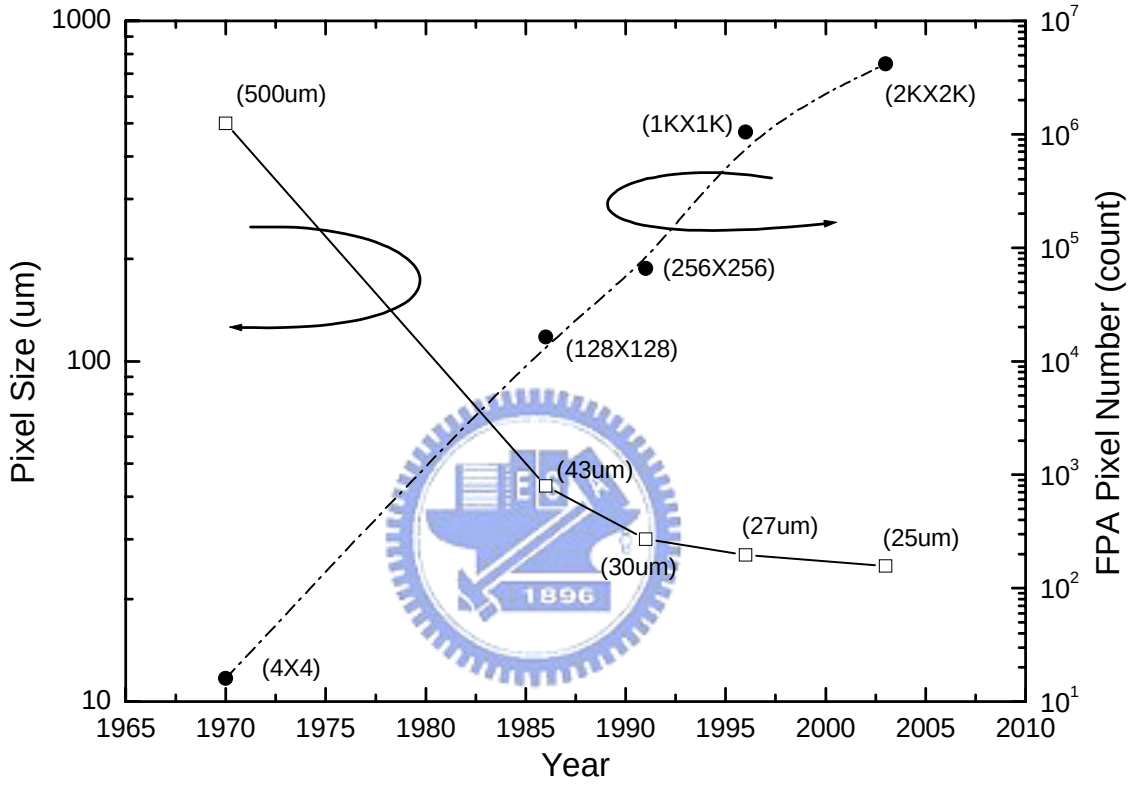


Figure 4.2 The scale-down of pixel size and the scale-up of the sensor format versus year for developments of InSb focal plane arrays.

of the passivation layer is a composite dielectric stack containing anodic oxide and low temperature Photo-CVD oxide. This passivation layer between interface and bulk oxide can make pixel p^+n diode smaller than 20 um retain good integrity in carrying out low leakage current and high breakdown performance. More importantly, it has been experimentally proven that there is no need to introduce a structure of control gate.

The test structure with systematic change in junction dimension was used to analyze the leakage current. In addition, various reasons for causing leakage current from small pixel diode were investigated and their dominant mechanisms were studied. The origins of leakage current from small pixel area with Be^+ implanted InSb p^+n junction are found to be correlated with the damage caused by implantation. Through both the R_0A measurement results from a series of different dimension test structures as well as the fitting of resistance model, the application of using our proposed simplified diode structure along with a specific passivation layer can make pixel size reduced down to 15um square.

The electrical properties of a simple InSb p^+n diode structure with composite anodic oxide/SiOx passivation were studied. The cause and the location of leakage current are inferred based upon the analysis of its generation mechanism and current-voltage characteristics. The fitting of measurement data and circuit model of p^+n diode zero bias dynamic resistance area product R_0A is used to extract the leakage resistance components corresponding to the area and peripheral. The p^+n diodes performance trend corresponding to the scale-down p^+n junction dimensions can be estimated.

The experimental results confirm that the passivation layer containing anodic oxide/SiOx composite dielectric stack forms a high quality interface on the 20X20

um^2 pixel size Be^+ implanted InSb p^+n junctions with low leakage current and high breakdown voltage diode characteristics. Therefore, no extra metal gate is needed to control the surface potential of the peripheral region in this simple diode structure. The fitting result of R_0A measurement and circuit model suggests that the simple diode structure is suitable for the realization of small pixel size down to 15X15 um^2.

4.2 Junction formation

To form p-n junction into InSb by ion implantation technique, several different ions of Cd, Zn, Mg, and Be have been studied. These ions except Cd have been demonstrated to have junction performance. The heavy ion Cd, however, [9] have been reported to have swelling effect on the implanted region at moderate dose and medium energy range. On the contrast, the surface damage corresponding to lighter ion such as Be and Mg were reported greatly reduced. Be ion has been demonstrated to have good p-n diode performance for several workers.[3,10-11] based on this technology trend, we choice Be as the dopant of p-type InSb.

4.2.1 Be ion implantation

The extraction of Be ions is generally done by sputtering the BeO solid source at the arc chamber by Argon gas in the medium ion implanter. Even though, the extracted efficiency is relatively low by comparing to the general B or P dopants. The beam current is typically in the range of 10uA only. So, the dose of Be is limit to moderate to low level

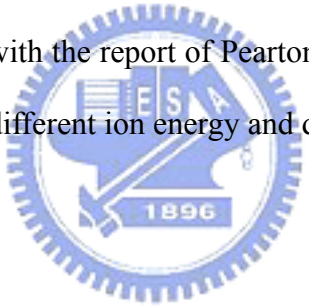
Both mesa and planar type diodes were made in this work. A thin anodic layer was prepared to reduce the channeling effect. For planar diode, photoresist coating was followed with thickness higher than 4um. Implantation was realized with Be+ ions at energies ranging from 80 KeV to 120 KeV, and ions dose range from $5X10^{13}$ to

$1X10^{15}$ ions/cm^{-3}.

As implanted wafer with Be ion energy 120KeV and dose $1X10^{15}$ ions/cm^{-3}.was analyzed by SIMS with O2+ as the primary ions. The primary energy and beam diameter was setup at 12.49KeV and 10um respectively. As shown in Figure 4.3, the y-axis is labeled with arbitrary unit due to the availability of standard, the etch step has been calibrated by the surface profiler. There are several features with this analysis:

- The surface has abnormal high concentration distribution of Be with thickness around 30nm
- The concentration peak at 330nm underneath the surface
- There junction depth is roughly estimated to be 800nm

These features are consistent with the report of Pearton et al[1] except the peak location and junction depth due to the different ion energy and dose.



4.2.2 Annealing

The annealing process is generally used to activate the implanted dopant and reduce the physical damage by restoring the doped impurities from the interstitial to the substitutional site. According to the literatures[1], the typical percentage of activation of Be in the InSb is about 65% of the implanted dopant. The characterization of the annealing process has difficulty in the high mobility of n-type substrate by Hall measurement The Hall measurement fail to extract and optimize the real doping level and mobility of the implanted layer in this work. So, electrical measurement instead was used to characterize the junction performances.

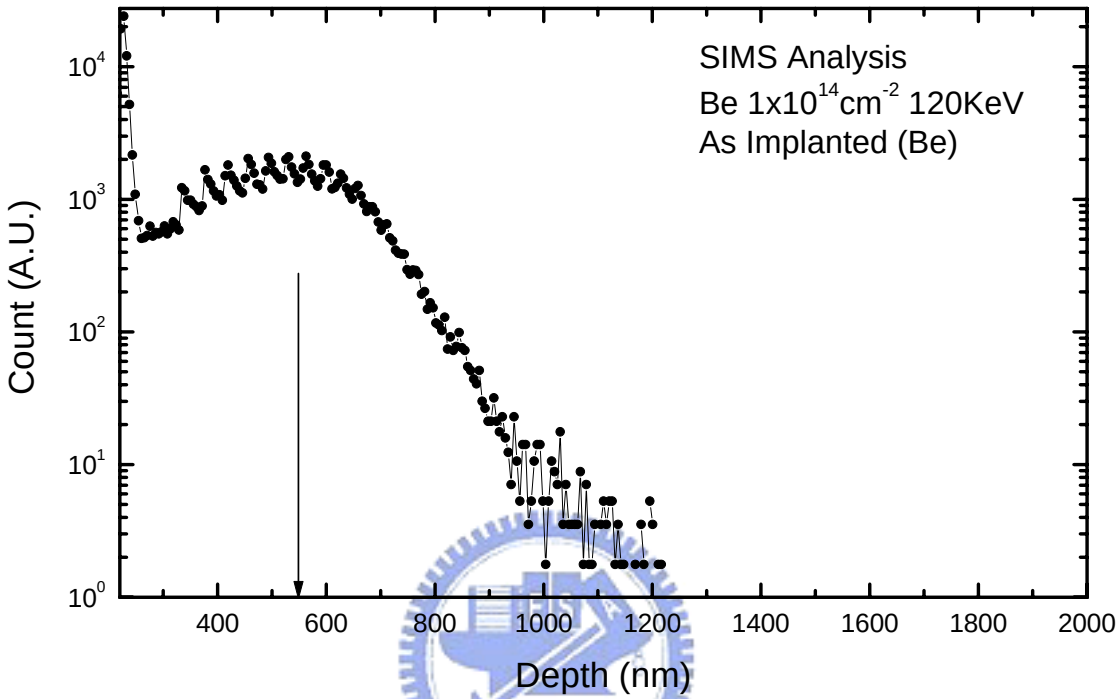


Figure 4.3 As-implanted doping profile in the InSb measured by SIMS.

Different thermal schemes including the rapid thermal annealing and furnace annealing have been investigated. There is no detectable difference in the diode electrical performance for these two schemes. Typically we use rapid thermal annealing at 400C for 30 second or furnace at 350C for 30minutes. To avoid the volatility of Sb from the InSb surface, the device side of the wafer was faced to a dummy InSb wafer during the annealing process.

4.2.3. Determination of junction depth

In general, people use differential Hall to measure the junction depth electrically. However, the narrow bandgap materials require cryogenic temperature to reduce the leakage current. It is obviously a troublesome and lengthy task for such specific requirement. Pearton's report[1] verified that the doping profile showed little change after the annealing process even at 450 ℃ by SIMS measurement.

To determine the junction depth, a terrace structure with different distance from the original InSb surface was generated by a series of chemical etchings on the same wafer. As shown in Figure 4.4, the top surface reference regions were protected by oxide, the section corresponding to specific depth then can be etched independently by protecting the other sections by photoresist. Table1 is a typical terrace structure example with 7 different depth sections. The width for each section R1~R7 is about 5mm.

A mesa type p-n diode array with different junction area was designed and fabricated on each section of the terrace structure. Figure 4.5 described the process flow, the passivation, contact formation, and metallization following the terrace and mesa etching were conducted by standard process detailed in the device fabrication section of this chapter.

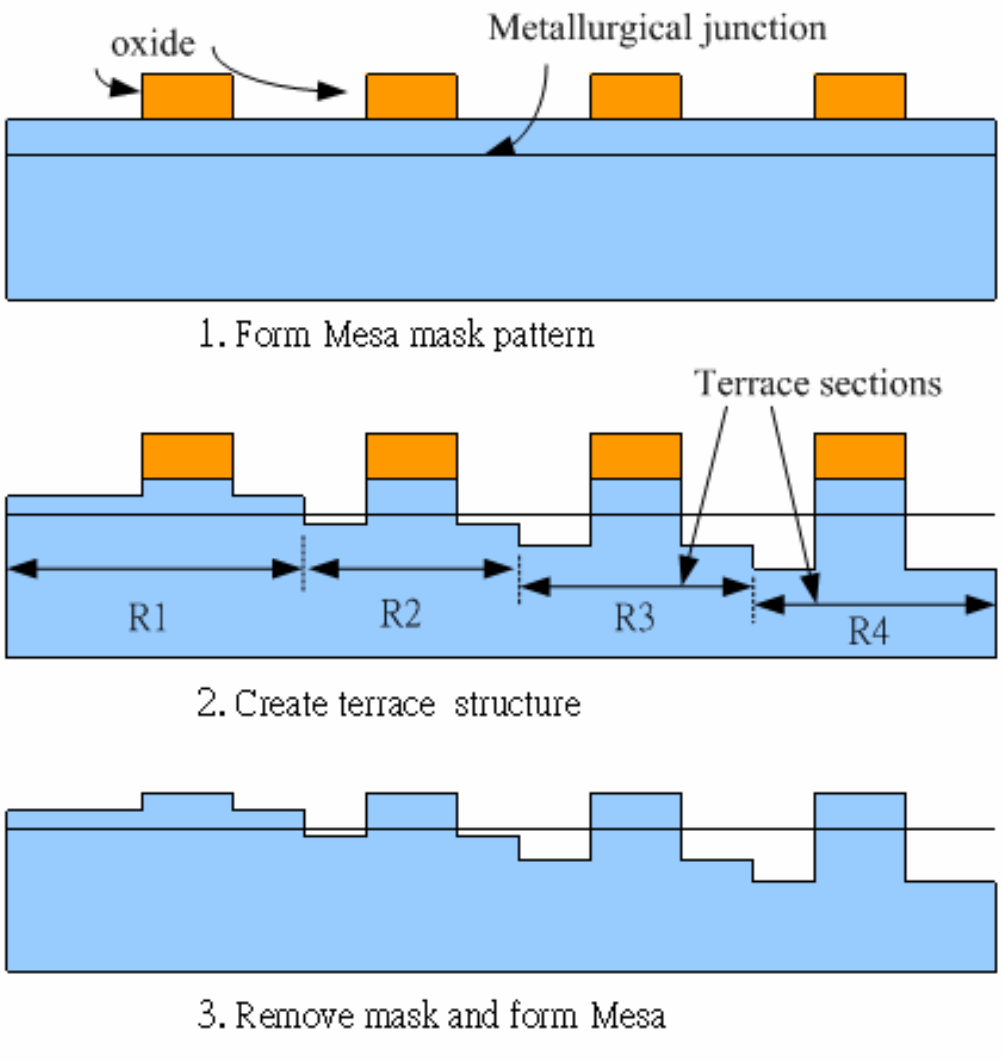


Figure 4.4 Schematics representation of a terrace structure formed by chemical etching to determine the junction depth electrically.

As shown in Figure 4.6, the diode current at reverse bias -10mV were measured by automatic probe station at cryogenic temperature. The regular pattern of junction area was used to judge the junction performance. In this work, the junction area is designed to decrease monotonously from left to right. So it can be easily judged from the figure that the two sections in the left side have normal junction response. The results indicated that the junction depth is located between 1.0 um to 1.5 um. The accuracy of this method depends on the accuracy of the terrace structure provided. So this approach provides a direct method to get the junction depth determined.

4.3 **Device fabrication**

Before the starting of device fabrication, the anodic film for implantation and annealing was etched away. The wafer was cleaned by standard process thoroughly. A composite insulating film stack composed of both anodic oxide and low temperature Photo-CVD SiOx [12] was optimized to be used as passivation layer for p^+n junction devices to produce minimal leakage current. Anodic oxidation in 0.1N KOH solution was conducted under constant current condition.

The wafer was then loaded into the growth chamber of photo-CVD system after drying from the anodic oxidation process. The growth temperature of photo-CVD oxide was tradeoff between responsivity and breakdown voltage in the range of 100-200 ℃, the SiH_4 and N_2O gases mixed with mercury vapor were then introduced into the reaction chamber, the ultraviolet lamp initiate the deposition of oxide. The contact window to p-type region was etched using reactive ion etching technique with Fluorine based gas system. Then the metals were evaporated to form Ohmic contact and bump electrode. In addition to the p^+n junction devices, MOS capacitor with dimension of 200umX200um was fabricated on n type region of the InSb wafer during the processing of p^+n junction to be used as test structures.

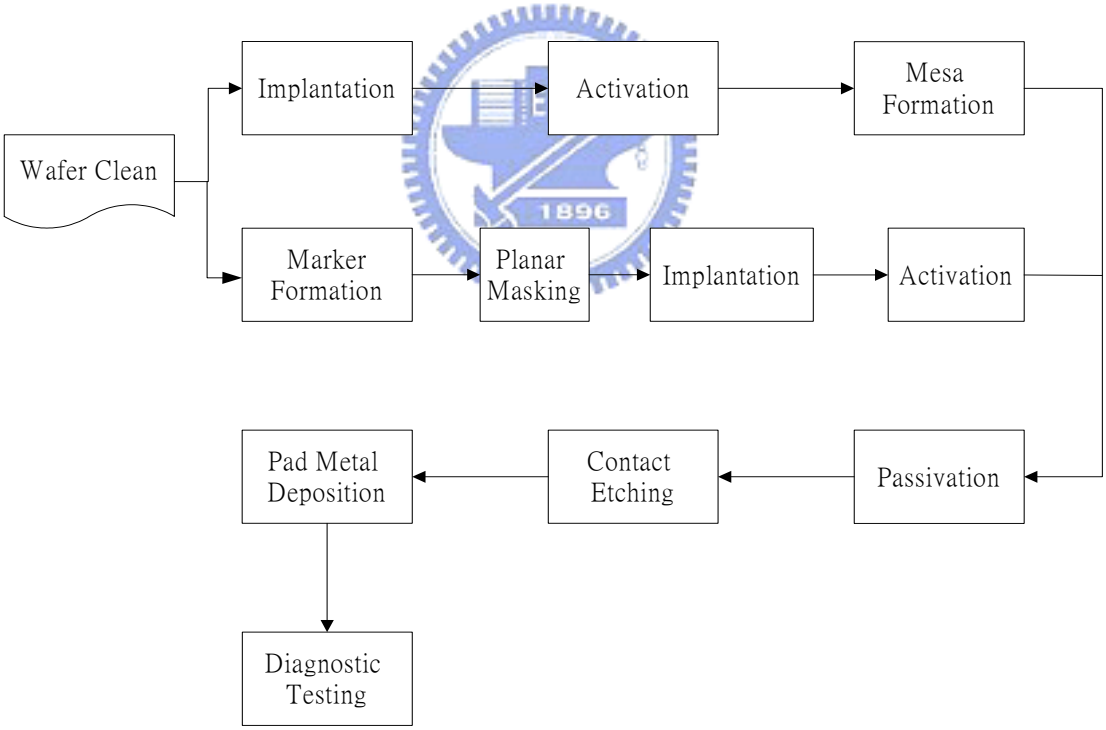


Figure 4.5 Process flow chart for p-n diodes development with junction formed by Be implantation

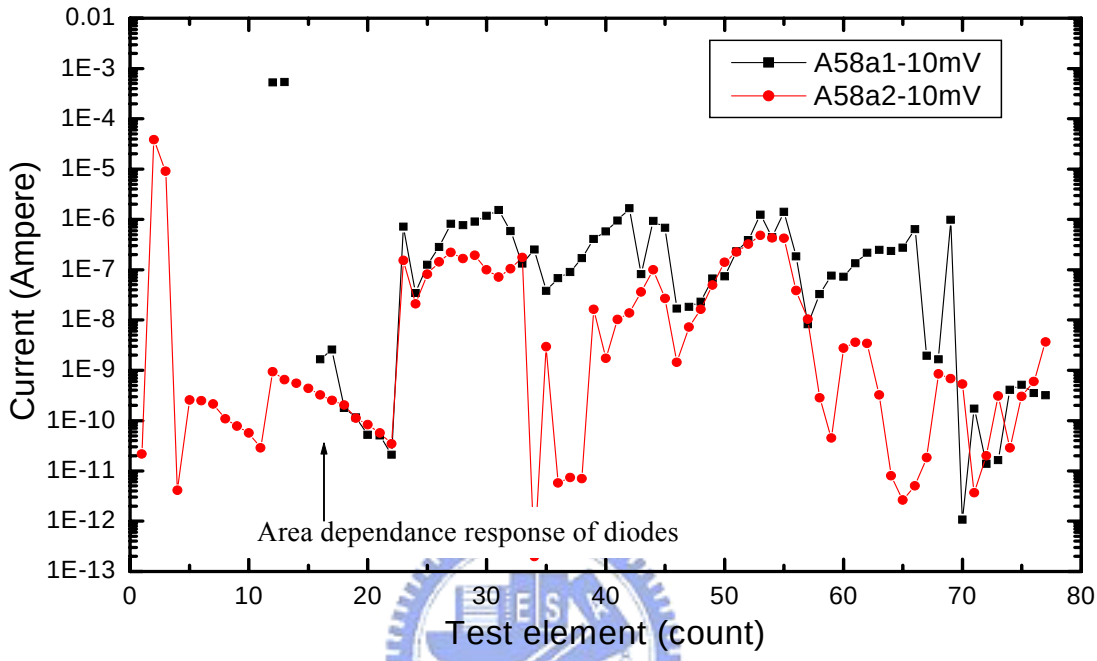


Figure 4.6 Test diodes current measured at -10mV under 300K background. Two rows of test diodes fabricated on the terrace structure with junction depth defined in the table 4-1. The arrow indicates the location of normal area response of the test diodes.

Table 4-1 Mesa height distribution for the terrace structure of A581 wafer.

Sections	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Mesa Height (um)	**1.892**	**1.497**	**1.009**	**0.913**	**0.737**	**0.552**	**0.280**

4.4 Measurement and analysis

In order to analyze the properties of the composite insulating film, in process test structure were diced from InSb wafer and bonded to a TO-5 header which was mounted onto a copper block holder and loaded into the liquid nitrogen bath directly The C-V measurement was conducted at a fixed high frequency 1MHz and 30mV small signal range. To measure the leakage current of radiation sensitive InSb p^+n junction, a block p^+n diode structure was used. The feature of this blocking structure to be designed to avoid photon effects[13] is the extended metal film deposited above the junction. It is extended 50um outward from the junction edges to keep the photon generated carriers from entering the depletion region by diffusion transport mechanism. To test the feasibility of using the small pixel process, the peripheral was designed without using gate control structure and its schematic cross-section representation of the p^+n junction test structure is shown in Figure 4.7. Low noise source measurement system was used to measure small pixel area p^+n diodes with leakage current level in the 10^{-12} Ampere range.

4.4.1 Junction capacitance

The comprehension of the dopant distribution in the Be^+ implanted surface is important to the characterization of the p-n diode. The junction characteristics of Be^+ implanted InSb substrate is analyzed electrically by using C-V measurement on test structure with junction area $4X10^4$ (um^2). As shown in Figure 4.8, the insert presents the capacitance measurement data for junction voltage span sweeping from 50mV to -500mV.

Obviously, junction capacitance decreases as depletion layer becomes wider when reverse bias is increased. When converting C-V curve into A^2/C^2–V plot, where A is the junction area, it can be seen that A^2/C^2 has a linear correlation with respect to

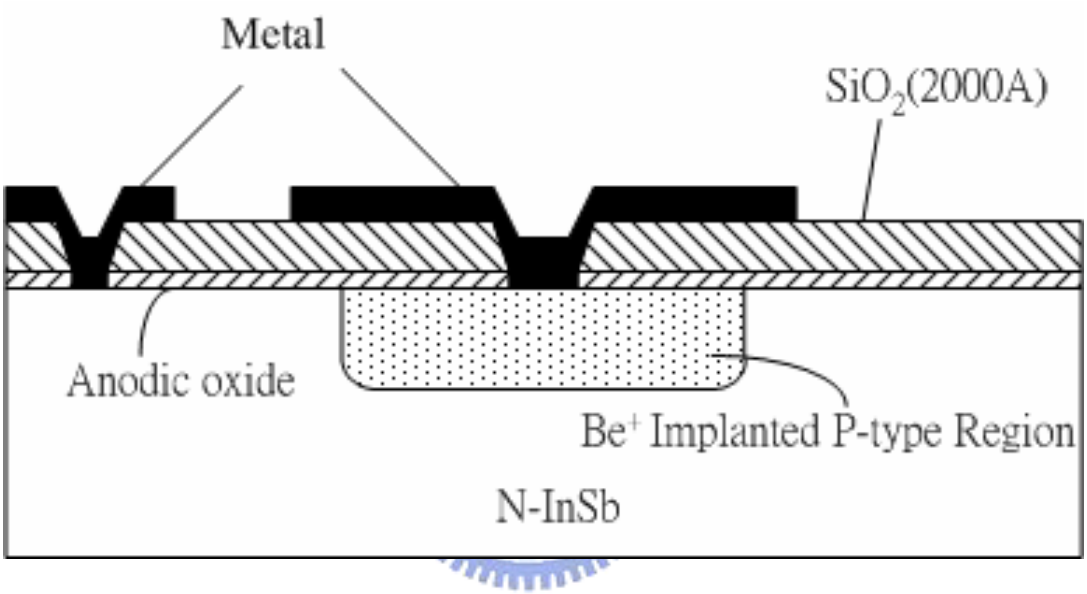


Figure 4.7 Schematic representation of a proposed simple implanted p^+n diode without gate-control structure for applications of high density infrared focal plane array.

junction voltage. This linear result signifies that the junction formed by implanting Be^+ into InSb and annealed afterwards is a one-sided abrupt junction [14]. With this in mind, the substrate doping concentration Nd and junction built-in voltage Vbi are extracted from the slope and the intercept of linear fitting curve of the converted $1/C^2$-V curve. From Figure 4.8, the substrate doping Nd is very close to InSb wafer's specification. Moreover, the built-in voltage Vbi resulted from the formation of junction in causing band bending is a little bit higher than the bandgap of InSb at temperature 77 K, i.e., 0.228eV. This result indicates that there is an occurrence of internal electric field [15] due to the asymmetric distribution of the doping charges in the p-n junction, which is in consistent to the characteristics of implantation of shallow junction and gradient dopant distribution.

4.4.2 Current-Voltage Characteristics

4.4.2.1 Effect of low dose implantation

D24 wafer was Be+ implanted with dose 5E13 cm-2 and energy 100KeV. As shown in Figure 4.9(a), these linear curves indicated typical current-voltage characteristics except the abnormal forward region. However, Figure 4.9(b) indicated that the rectifier function were limited to 2 orders of magnitude between the forward and reverse current, the forward region does not follow the ideal Schockley equation, there is a plateau region with weak bias dependence. It looks like that there is another diode with back to back configuration connected to the junction diode at small forward bias. The low doping concentration on the surface due to low dose was inferred to be the main reason to form non-Ohmic contact to the metal.

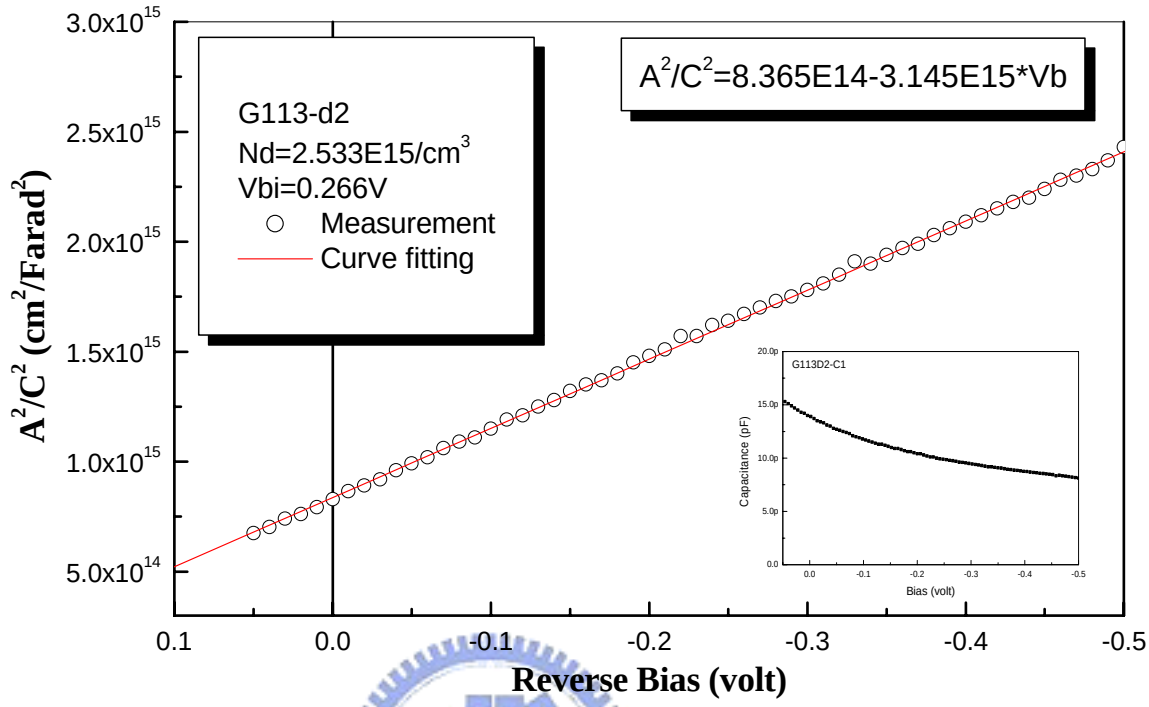


Figure 4.8 Curve fitting of measured $1/C^2$-V data for Be^+ implanted InSb p^+n junction. The inset shows the capacitance-voltage characteristics measured with 1MHz 30mV small signal range under 77°K for junction area $4X10^4\ um^2$.

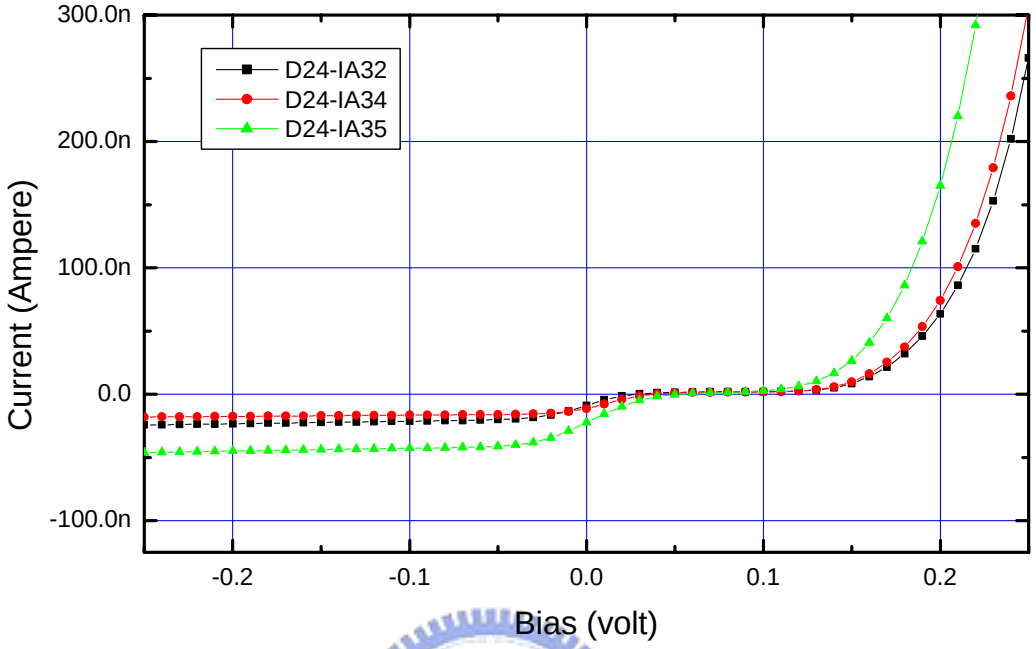


Figure 4.9 (a) Linear I-V characteristics of three implanted semiconductor mesa diodes fabricated at the top surface (without surface etching), a short shoulder occur before exponential rise in forward region.

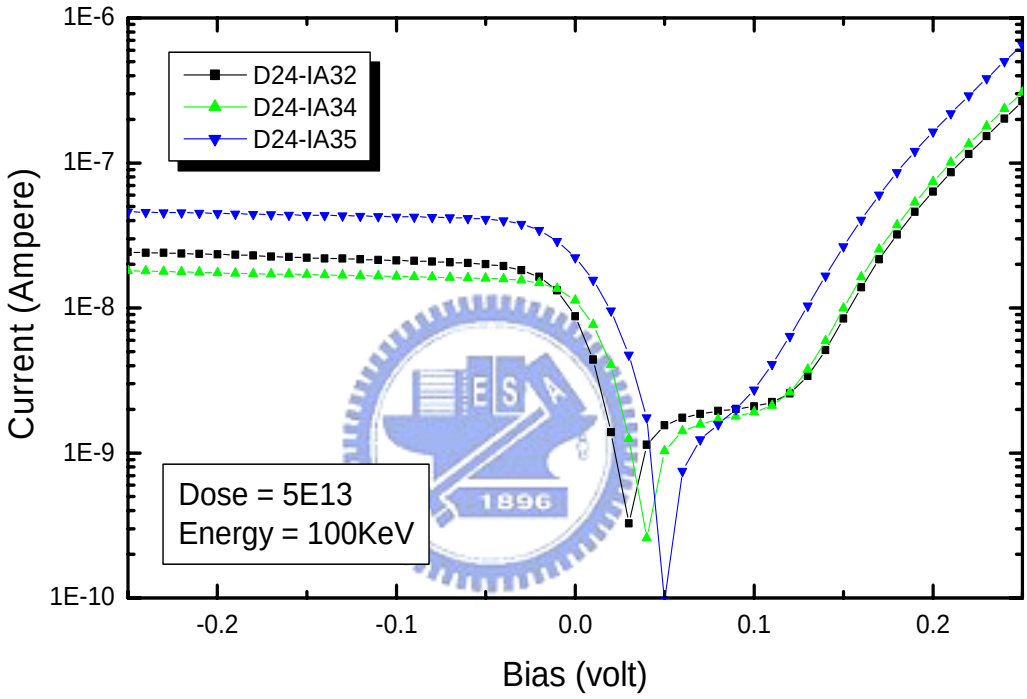


Figure 4.9 (b) Current-voltage characteristics of the implanted InSb diodes fabricated by the implantation conditions as shown in the inset.

4.4.2.2 Diodes made of high dose implantation

To verify the dose effect, higher dose implantation was conducted for both the mesa and planar diodes. The LOG I-V characteristics of planar diode with square junction dimensions as described in the legend were shown in Figure 4.10. The smallest dimension with this structure is 20umX20um. Most of the diodes except 175 and 125 reveal good rectifier performance. Device 175 and 125 were assumed to be fail due to the yield loss. The maximum current ratio for forward and reverse bias is 10^8.

4.4.2.3 Pixel size effect on dark current of diodes

To characterize the leakage current performance of the Be^+ implanted InSb p^+n diodes, current-voltage characteristics of the diodes with junction area range from 200X200 um^2 to 20X20 um^2 were measured at 77K. Figure 4.10 indicates the different current levels corresponding to diodes with various junction dimensions. It reveals the junction dimension dependence of the diode leakage currents for both the forward and reverse bias regions.

In general, the leakage current can be separated into area and peripheral components (Ja and Jp) respectively according to the current flow paths. Therefore, the total leakage current with respect to the specific junction bias can be expressed as:

$$I_L = Ja\ A + Jp\ P \qquad (4.1)$$

where I_L is the junction leakage current, and A and P are the area and the perimeter of the junction respectively. In extreme conditions such as Jp=0, there is a linear proportional increase of leakage value as junction area is increased when p^+n diode leakage current penetrates through junction area only. By analogy, when Ja=0, the current value increases in linear proportion as the length of perimeter is increased.

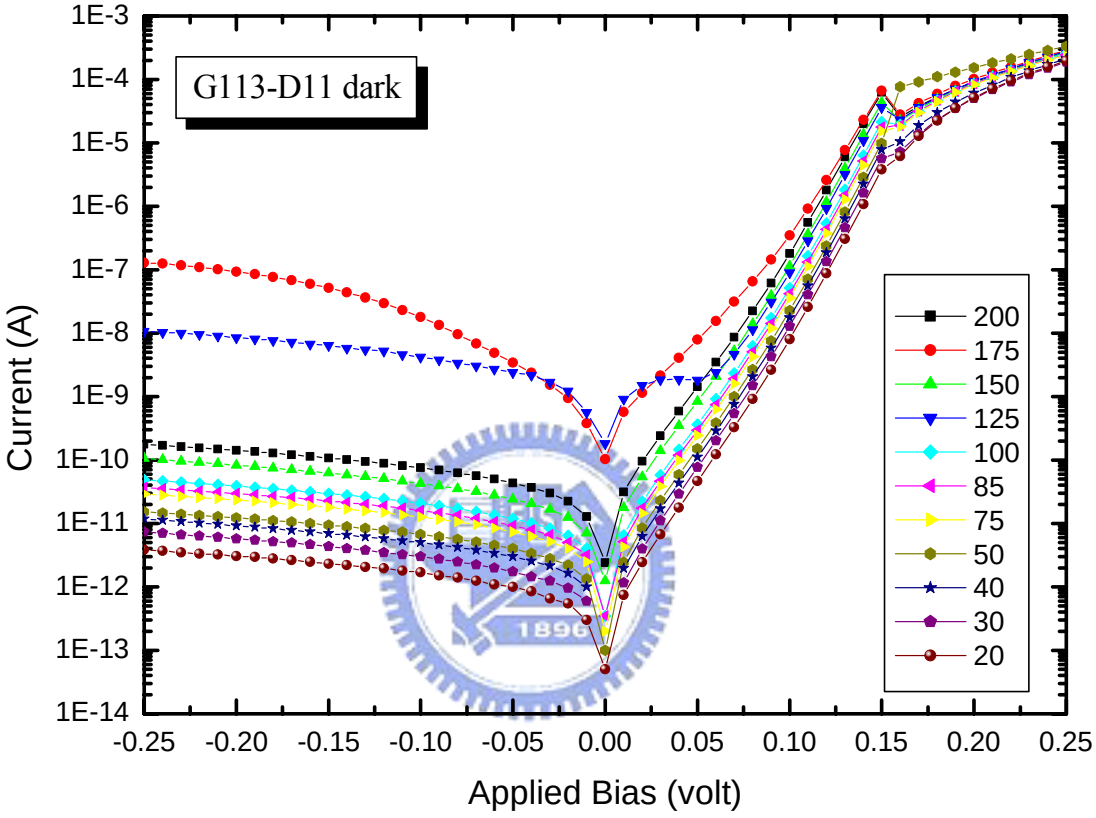
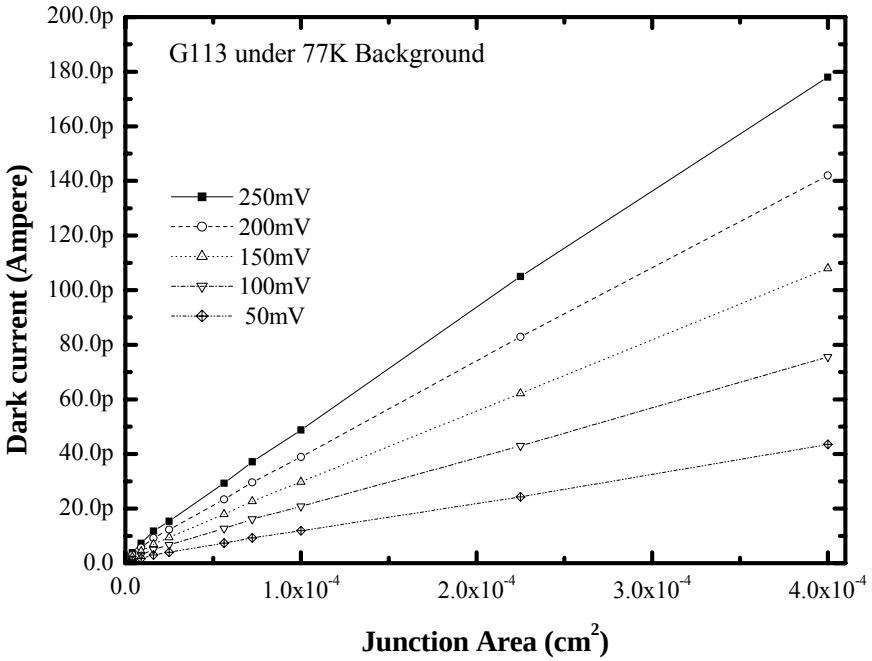


Figure 4.10 Current-voltage characteristics of planar diodes with junction dimension as depict in the legend of the figure.

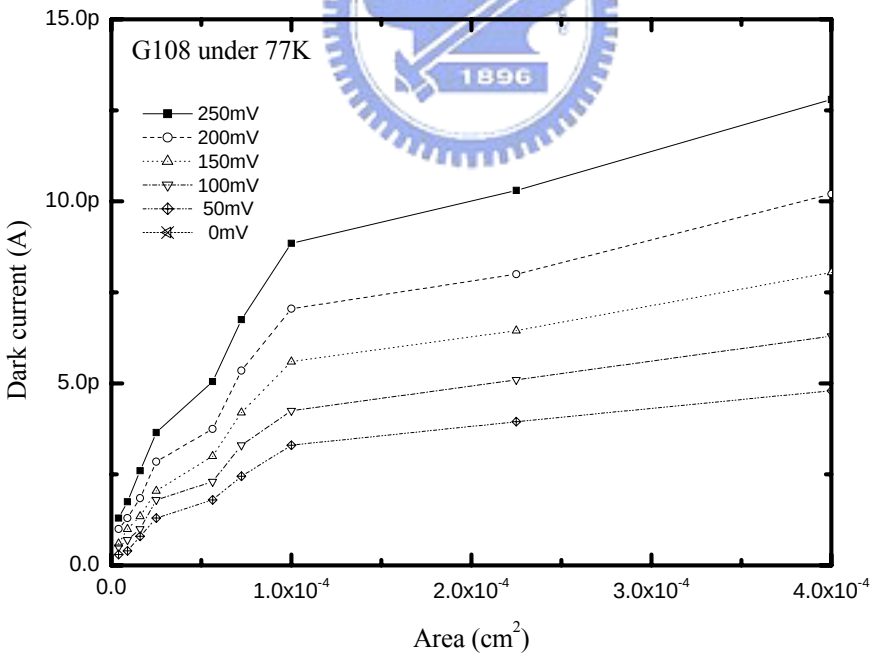
The I-V characteristics of Figure 4.10 were transformed into current-area characteristics at some specific reverse biases due to the operation range of interest. As shown in Figure 4.11(a), the measured dark currents show linear dependence vs. junction area for all the reverse bias ranges. The slope of each current-area characteristics in Figure 4.11 (a) is Ja as described in equation (1), it increases almost linearly vs. reverse bias too. The intercepts of the current-area characteristics corresponding to different reverse bias are almost zero. Explicitly, the dark current control equation (1) is simplified to area component only. The peripheral component provides very little contribution to the dark current to the implanted p+n diodes. Detail examination of the current-area characteristics in the small area region indicated that there is a non-linear dependence on the junction area when they are smaller than 50X50 μm^2. It indicates the current contribution of peripheral component Ip to the dark current when the junction area becomes smaller than 50X50 μm^2.

Generally, the peripheral component of junction diode dark current is considered to be dominated by the surface generation mechanisms, such as generation-recombination current in field induced depletion region, tunneling and shunt leakage. These mechanisms are highly dependent on the properties of the surface or interface between passivation and InSb. The weak dependence of dark current of implanted InSb p+n diode on the peripheral component indicates the good control on the surface quality. This surface condition in turn suppresses the contribution of dark current from the surface or peripheral component.

However, by comparing to the test data of diffused diodes as shown in Figure 4.11(b), the implanted diodes show relatively higher Ja at least one order of magnitude. It can be inferred the dominant leakage current of implanted diodes are generated from the area component.



(a)



(b)

Fig. 4.11 The junction area dependence of dark current in (a) Be^{+} implanted p+n diodes and (b) Cadmium diffused diodes under various reverse bias.

When comparing two different areas of square p^+n junctions having the same area component dominant characteristics, the leakage current ratio will be nearly the area ratio of these two p^+n junctions. Figure4.12 presents the current ratio of two p^+n junctions with respect to the junction bias for regimes of large p^+n diodes and small p^+n diodes. For large p^+n diodes regime, the square junction with length 200um and 100um were compared. For small p^+n diodes regime, the square junction with length 40um and 20um were compared. The area and peripheral ratio correlating to the two junction lengths are 4 and 2 respectively.

It is worth noting that the range of variation of leakage current level is very wide when dealing with ratio calculation. That is, the value of leakage current can vary from 10^{-11} to 10^{-3}Ampere. Also, the leakage value can go down to less than 1pA when bias approaches 0 volt. As a result, the current ratio fluctuates due to noise factor. As for the regime of large p^+n diodes, the ratio of the leakage current appears less dependent to the reverse bias as bias was sweeping from -250mV to -50mV and its value is around 3.7. Numerically, this value is very close to the area ratio of two p^+n diodes, which is 4. In other words, this proximity implies that the leakage current of large p^+n diodes originates dominantly from junction area.

The meaning to sweep the bias from 0 to -250 mV is effectively to increase the depletion width with square root of bias dependence, the constant leakage current ratio confirms the leakage current are controlled by an exclusive generation mechanism within this bias range.

The G108 data plot in the Figure 4.12 is the devices fabricated by cadmium diffusion process, the current ratio indicates peripheral dominate contribution to the leakage current with 200 um and 100 um p-n junction devices; it also has notably change for reverse bias sweep. At high electric field, large junction bias, the devices indicate more peripheral dominate, or surface state dominant contribution to the leakage current.

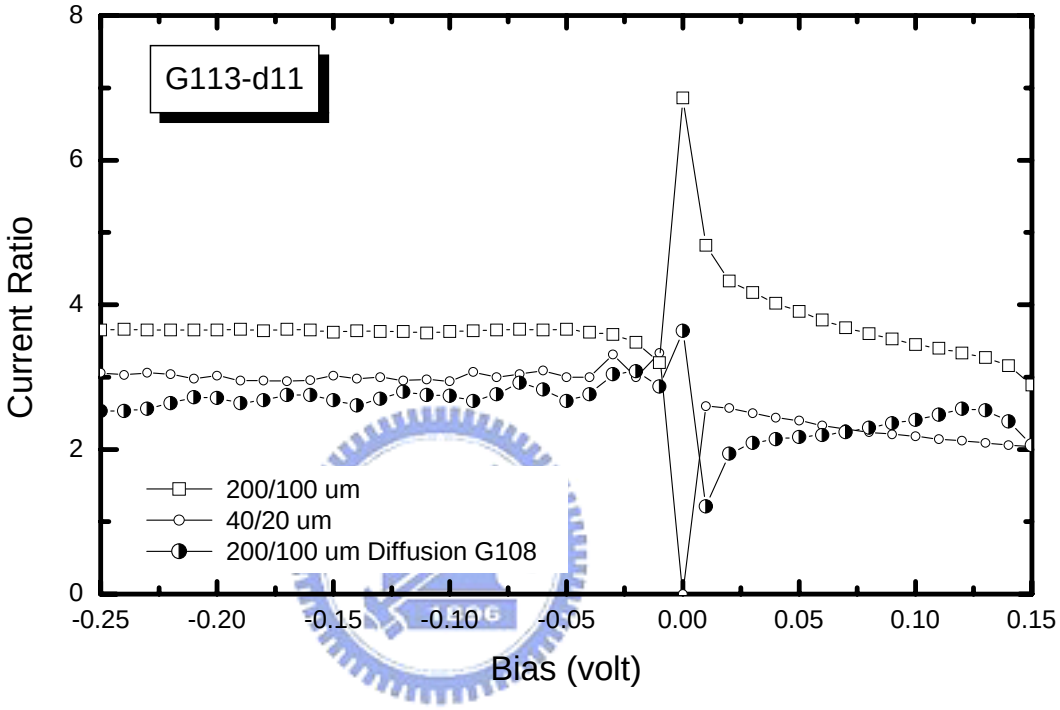


Figure 4.12 Bias voltage dependence of current ratio in Be^{+} implanted p-n diodes with large pixel area and small pixel area. The data from Cadmium diffused diodes G108 was plotted as a reference.

To this extent, it means that damage induced by Be^+ implantation process would extend into the region located under metallurgical junction. Concurrently, these result can be used to prove that the origin of leakage current may be originates from implantation damage of Be^+ into InSb bulk.

As for the regime of small p^+n diodes, the ratio of the leakage current indicates independent relation versus reverse bias as bias was sweeping from -250mV to -50mV and its value is 3, in the middle of area and peripheral ratio. Roughly estimated, we assume the contributions of leakage current from the area and the peripheral components are compatible. By comparing the small p^+n diodes with the large p^+n diodes, it is obvious that the leakage current for the small p^+n diodes is likely to move to the region of peripheral dominant component. Since the characteristics of the peripheral component depends upon the passivation properties of p^+n junction, the impact of passivation on p^+n diodes' performance becomes more significant as the pixel size is reduced.

4.4.2.4 Dark current analysis of small pixel size diode

To identify the dominant physical leakage controlled mechanisms of the dark current in implanted diodes, the measured current-voltage data were used to curve-fit the independent current components associated with the following leakage mechanisms described previously[16], bulk-diffusion current Ibd, generation-recombination current Igr, shunt current Ish, tunneling current Itun, and surface-diffusion current Isd. As illustrated in Figure 4.13, the dark current got from simulation Itotal corresponding to a specific bias Vb is composed of five leakage current components. The result indicates that the simulation data Itotal has very good agreement with the measurement data Imeas. The shunt current and surface-diffusion

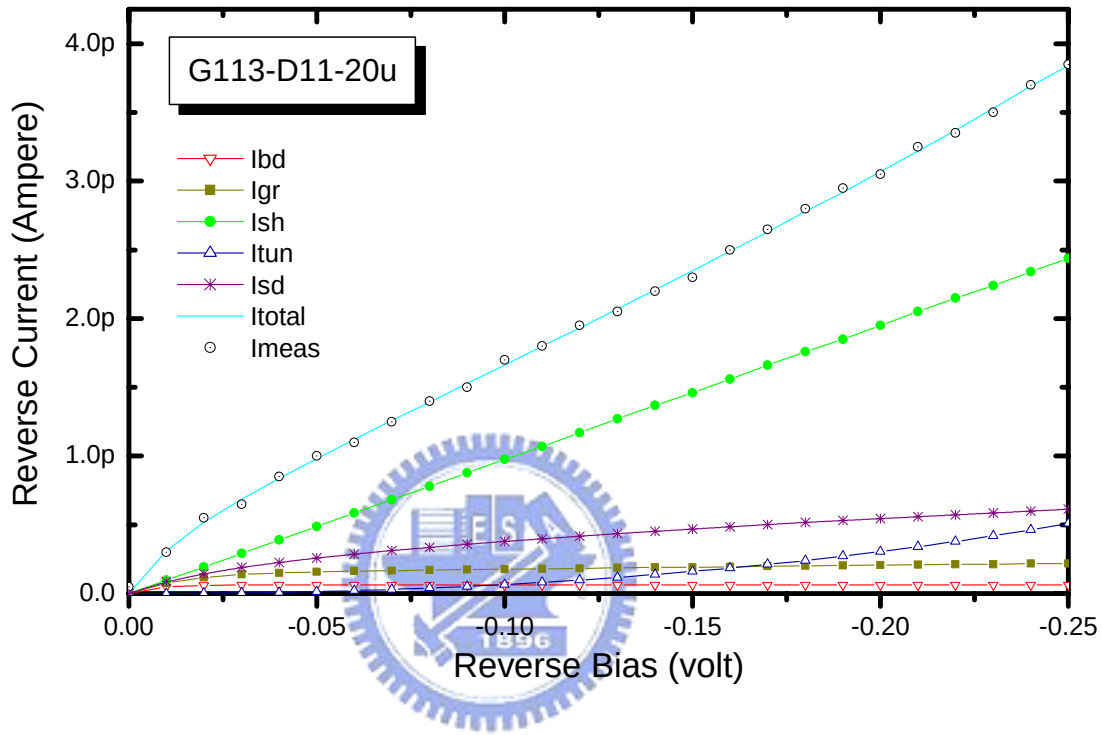


Figure 4.13 Numerical analysis of leakage current generation mechanism of Be^{+} implanted $p^{+}n$ junction on InSb for small pixel area with A = 20X20 um^{2}.

current are the dominant components of the measured dark current as the reverse bias was smaller than 250 mV. The tunneling current generally dominants the dark current at high reverse bias is suppressed to a negligible level in this bias range. It is believed that the composite anodic oxide/SiOx stack provides the optimized surface and interface properties for the implanted p+n diodes that help to avoid or reduce the induction of local electrical field. This result can also be confirmed by the dynamic resistance-voltage plot as shown in Figure 4.14; the flat response indicates linear proportional relation of dark current to the voltage. Figure 4.14 indicates bias voltage dependence of the leakage current and dynamic resistance-area product RA of a small pixel diode with area of $4X10^{-6}$ cm^2. The bias voltage was extended to -1volt. At small reverse bias, the leakage current has linear dependent relation with bias. It increases to 33 pA exponentially as bias sweeps from 300mV up to 1V. On the other hand, as the bias is swept from -10mV to -600mV, RA product can keep its value higher than $1X10^5 \Omega$-cm^2 all the time. This current-voltage characteristic, to the best of our knowledge, is the first and the best one for Be^+ implanted InSb p^+n junction in terms of its leakage current and breakdown voltage using such small pixel dimension without control gate.

The shunt current Ish is normally refers to the Ohmic current due to leakage path at the diode surface. It is generally explained by lack of the classical junction characteristics at the surface. However, previous results have shown that the dark current has linear proportional relation to the junction area under reverse bias conditions. The dark current get little contribution from the surface even in the characteristics of 20X20 μm^2 diode. It is inferred from these results that the leakage current is resulted from an internal shunt leakage mechanism, which may be resulted from the defect or residual damage introduced by the implantation and annealing process. High density defect levels are assumed to be created within the InSb narrow

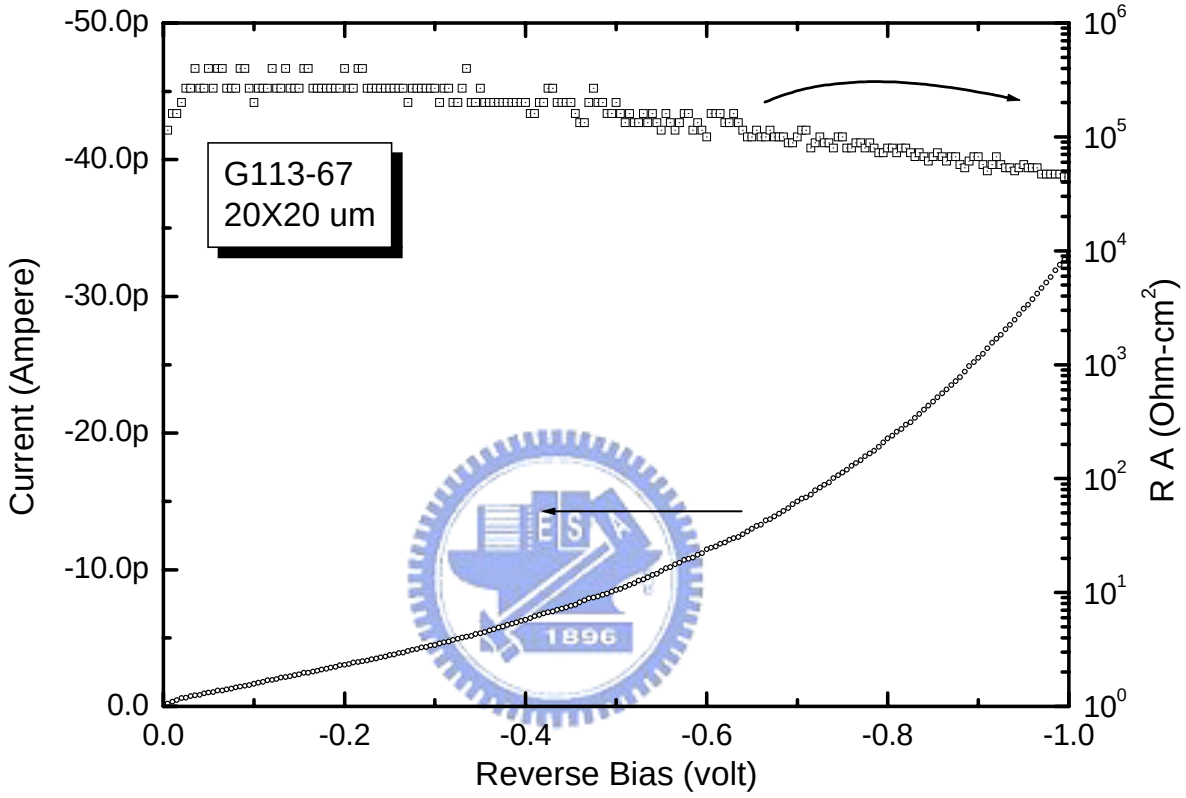


Figure 4.14 The measured leakage current and dynamic resistance area product versus reverse bias characteristics at 77K for Be^+ implanted p^+n diode fabricated on InSb with junction area = 20 X 20 um^2. There is a linear dependence of reverse bias for bias < 300mV. The leakage current presents obvious exponential increase as reverse bias > 600mV.

bandgap, they may results the shunt leakage current by the carrier hopping process instead of the classical carrier transport mechanisms.

4.4.3 R_0A Product analysis

The R_0A product is one of the most important parameters of merit in characterizing the InSb photovoltaic detector. It can be used as a measure with respect to materials and junction quality due to its intrinsic correlation with the carrier transport mechanisms in the bulk and on the surface of semiconductor. The zero bias dynamic resistance R_0 of p^+n junction is extracted from the current-voltage plot by differentiating the voltage with respect to the current at zero bias. The scale-down p^+n diodes characterized by using R_0A product will provide the information about the trend and limits for small pixel area p^+n junctions in designing high density focal plane array. In this work, if R_0 were modeled as a circuit composed of two resistors in parallel; that is, the area component Ra/A and the peripheral components Rp/P respectively. On the whole, the zero bias dynamic resistance of junction with junction area A and junction perimeter P is expressed in the following equation,

$$R_0 = (A / Ra + P / Rp)^{-1} \qquad (4.2)$$

where Ra is the normalized junction area resistance in unit of (Ω-cm^2). Rp is the normalized junction peripheral resistance in unit of (Ω-cm).

As shown in Figure 4.15, R_0 corresponding to nine different area Be^+ implanted InSb p^+n junctions are calculated from the I-V characteristics under thermal radiation background of less than 1X10^8 photons/cm$^2\cdot$sec at 77°K. According to equation (4.2), for every two of these nine different sizes of p^+n diodes there exists one set of Ra and Rp to be used to valuate junction resistance model. In order to describe the performances of these nine p^+n diodes with different junction dimension, we adopted the least square fitting method to find out a set of Ra and Rp which can describe the

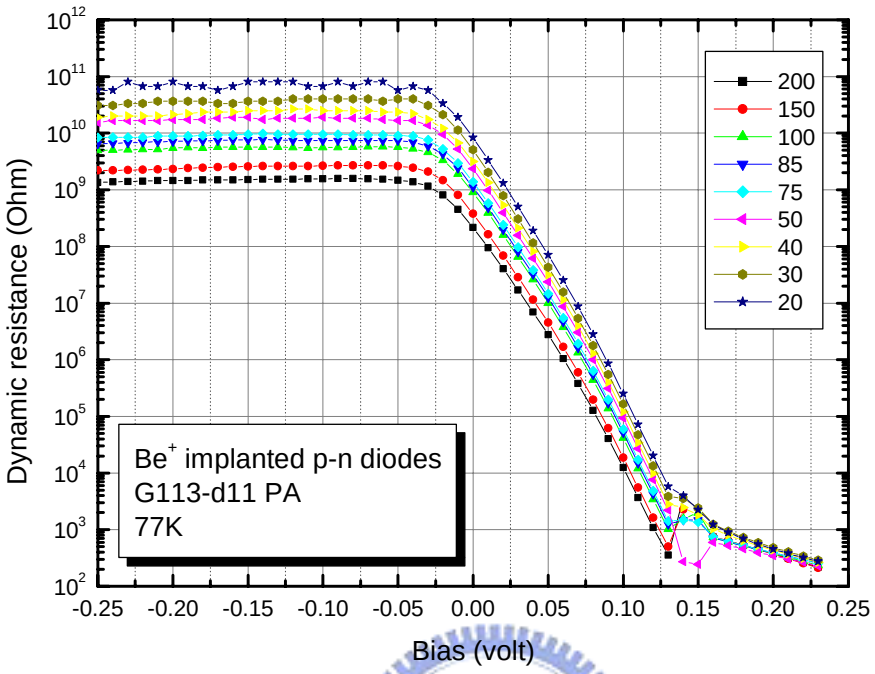


Figure 4.15 Differential resistance-voltage characteristics of planar diodes G113-d11 with junction dimension as depict in the legend of the figure.

geometric effects on the corresponding differential resistance of the test structures at zero bias. As shown in Figure 4.16, the inset indicates the extracted Ra and Rp for test structure series G113-PA respectively.

Based on the extracted Ra and Rp, equation (4.2) was used to calculate the resistance-area product of the circuit model, it is zero bias differential resistance R_0A, for devices with 2 um increment in square junction length. As shown in the plot of Figure 4.16, the dash-line curve with legend "simulation" represents the calculation results. On the contrast, the measurement results corresponding to the various test structures are also plotted as square box. By comparing the measurement data and simulation data, it is legitimate that the junction resistance model can be used confidently to predict the performance of the continuous scaling down of small pixel area p^+n junctions. The model indicates that RoA will decrease gradually as the junction dimension changes from 200um to 50um, then it declines rapidly following the decrement of junction length, especially when the junction dimension becomes small than 20um. However, if R_0A performance of small pixel area junction is targeted at $5X10^4$ Ω-cm^2, then our proposed simple planar diode structure with the anodic oxide/Photo-CVD SiOx passivation layer can be scaled down to below $15X15um^2$.

To implement this simple diode structure into the focal plane array, it should be noted that the reduction of image pixel size will not be limited by the metal overlay requirement in this study. The dimension of block metal overlay on the p^+n junction as shown in Figure 4.7 can be scaled down to smaller than the junction dimension. The back-side illuminated configuration of hybridized InSb focal plane array provides sufficient spectral filtration of unwanted photo noise by the bandgap properties of InSb bulk itself.

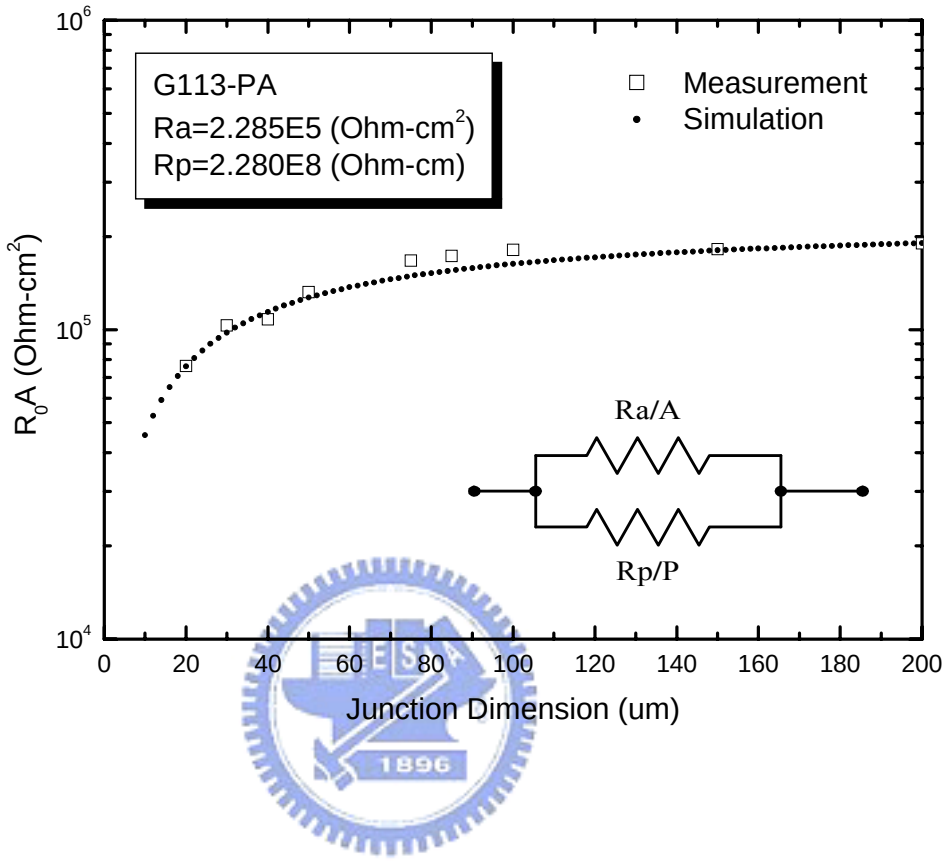


Figure4.16 Junction dimension dependence of R_0A product based on the current-voltage measurement and simulation of the resistance circuit model. The normalized area and peripheral components Ra and Rp are extracted from the curve fitting of the measurement data.

4.4.4 Photo response

To evaluate the response of beryllium ion implanted InSb p-n diodes to the thermal radiation, a series of test structures with increasing exposure window in the middle of p-n diode were used to measure the response current. As shown in Figure 4.17, the current-voltage curve move downward as the exposure window size were increased, that mean the photocurrent were increased correspondingly.

In general, the photocurrent Iph of p+-n diode can be expressed[18] as:

$$\mathrm{Iph} = \eta\, q\, M \frac{\Omega}{\pi} A \qquad (4.3)$$

where η is the quantum efficiency, the number of photoelectrons generated per incident photon in the photodiode, q the charge on an electronic = $1.6X10^{-19}$ C, Ω the projected solid angle which define the aperture and distance from the blackbody to the detector plane, M is the exitance in the spectral band of interested 4~5 um in photon/cm^2·sec, A is the exposure area of the photodiode in cm^2. For optical system with f/# number, the projected angle Ω is defined as:

$$\Omega = \pi \frac{1}{4(f/\#)^2 + 1} \qquad (4.4)$$

the f/# of the cold probe system in our laboratory is 2.05. The background the test structure staring at is 297K. Based on these data, it was estimated that the irradiance projected onto the detector plane is $1.23x10^{15}$ photons/cm^2·sec.

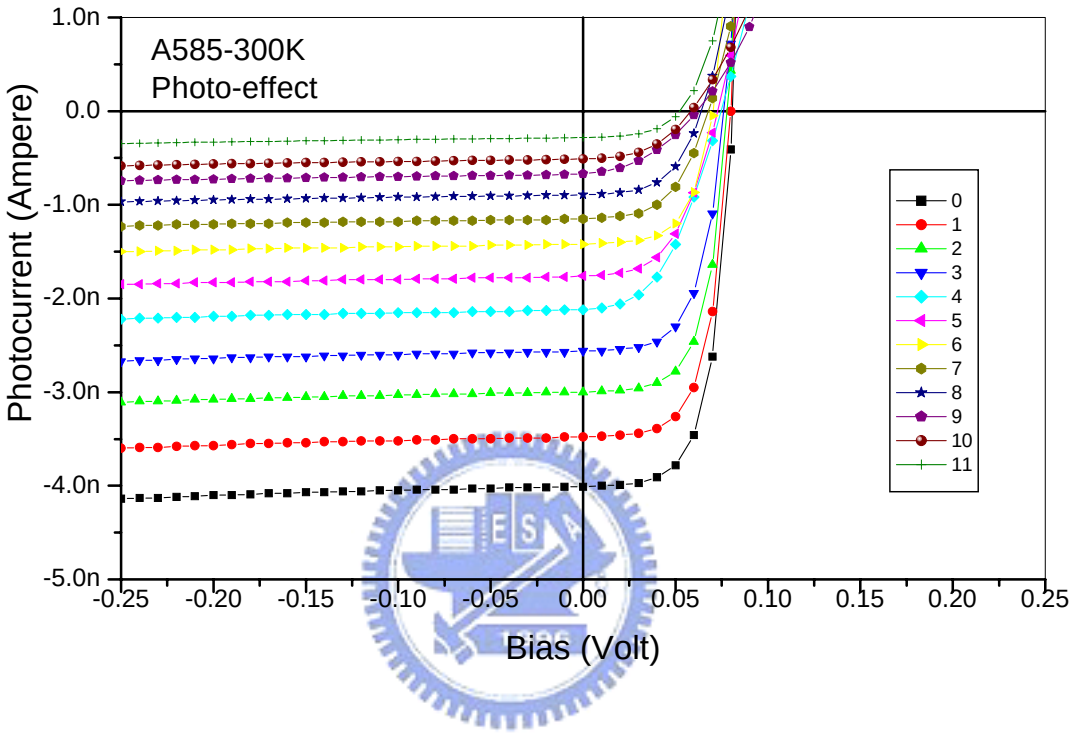


Figure 4.17 Current-voltage characteristics of the implanted p-n diodes with various opening size in the middle of the diode structure.

As shown in Figure 4.18, the photocurrent response per unit area extracted from the slope of photocurrent vs. exposure area plot is 113uA/cm^2 .With these given data, the quantum efficiency calculated based on this equation is 57.4%. For devices without antireflection coating, this result indicates that the Be ions implanted photodiodes can meet performances requirement of detector applications.

4.4.5 Response uniformity

Ten Test diode arrays with 40 test diodes for each array distributed on a two inch InSb wafer was fabricated to demonstrate the response uniformity, the junction area of the test diode is 43X43 um^2. The photo response testing was configured in the same way as the previous current-voltage testing in photo response testing but with limited specific reverse bias voltages due to the quantity of test diodes and computer resource required. The test results are summarized in Table 4.2. The mean values of photocurrent distribution increase as the reverse bias are increased. Same trend was observed in the standard deviation. However, the sigma to mean indicates about 10% uniformity can be reached with this process. The R_0A calculated from the mean value of the photocurrent is 1.71X10^5 Ohm-cm^2. This result is consistent to the data of planar diodes G113-d11 as shown in Figure 4.14. As shown in Figure 4.19, for five different reverse biases, the number of test diodes corresponding to the photocurrent level indicates a distribution of the photocurrent of the test diodes on the wafer. Instead of normal distribution, the figure did indicate some characteristic peaks. The distribution corresponding to the bias change is relatively uniform, which imply the quality of passivation is good enough for electrical performance.

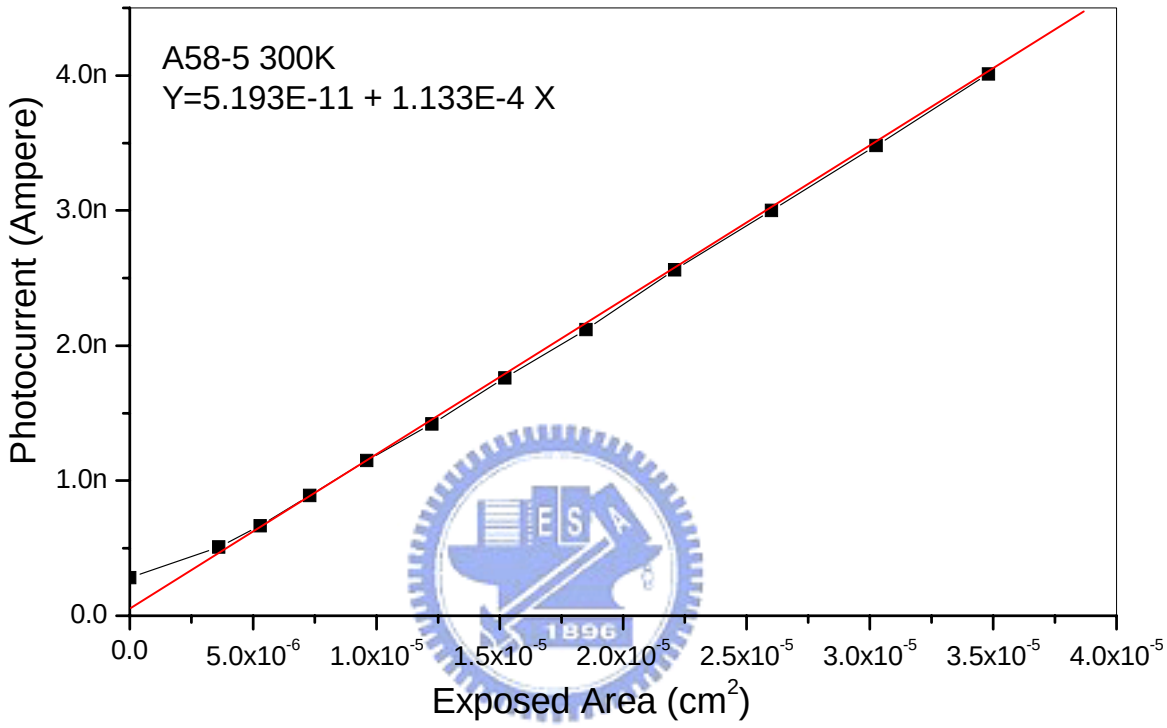


Figure 4.18 Exposure area dependence of the photocurrent corresponding to a series of diodes made by Be+ implanted approach.

Table 4.2 Statistics of photocurrent in test diode arrays I107 at various reverse bias.

I107	10 mV	70 mV	130 mV	190 mV	250 mV
Mean (pA)	104.2	110.7	116.0	121.4	127.2
Sigma (pA)	10.23	11.4	12.01	12.36	13.45
Sigma/Mean (%)	9.80	10.29	10.35	10.18	10.57

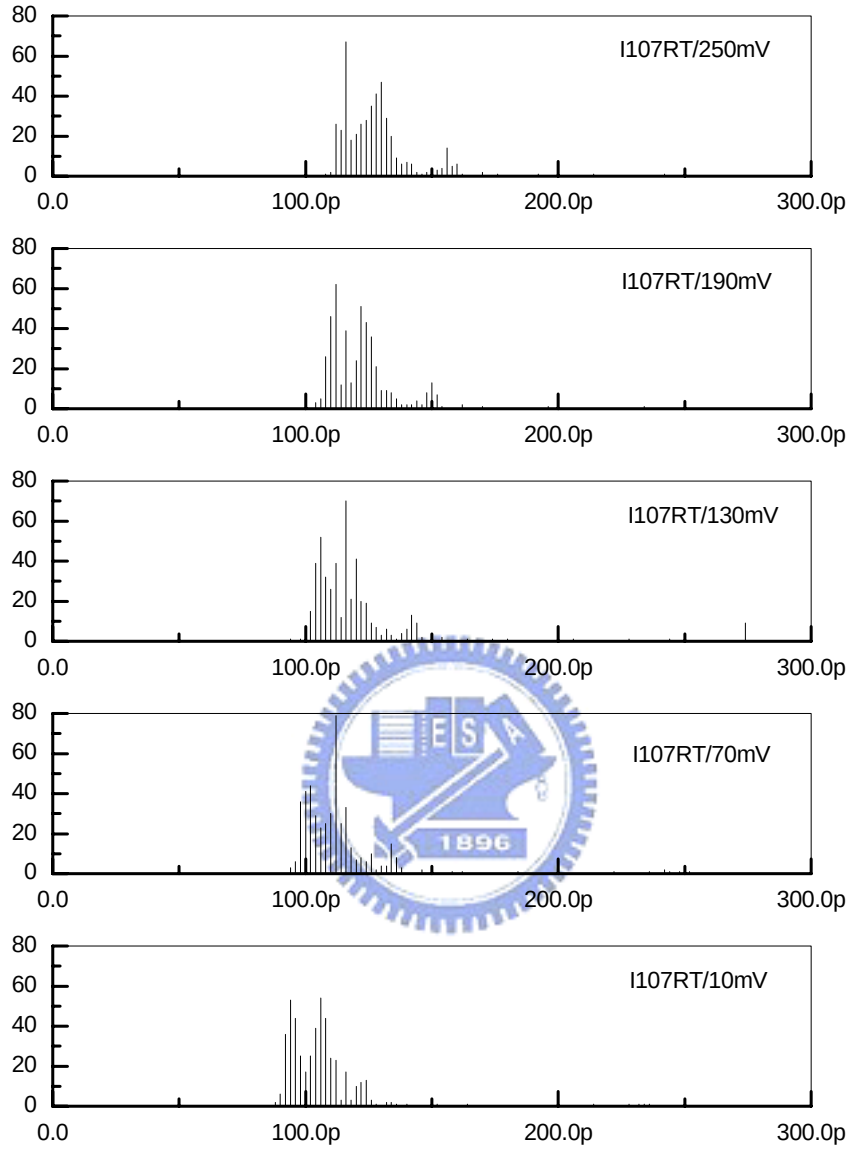


Figure 4.19 Photocurrent histogram of test diode arrays I107 at various reverse bias under room temperature background.

4.5 Summary

It has been shown that our simple Be^+ implanted p^+-n diode structure passivated by composite anodic oxide/photo-CVD SiOx stack can be scaled down to small pixel area with low leakage current and high breakdown voltage characteristics. No extra gate control structure and processing are required to adjust the pixel junction peripheral surface potential.

The leakage current analysis for small pixel p-n junction indicates that InSb p^+n diode fabricated by Be^+ implantation and annealing techniques is dominant with shunt leakage mechanism. The large bias dependence of shunt leakage current also indicates that the defects results in the leakage current occur in the bulk of InSb semiconductor.

It has been demonstrated that the pixel fabricated by the proposed simple diode structure and the optimum passivation process steps with size 20um square can achieve the R_0A product in the range $7.6X10^4 \Omega$-cm^2. The dimension of pixel size with the same device structure and processing can be derived by simulation to scale-down to below 15um square with R_0A product in the range of $5X10^4 \Omega$-cm^2. In its broadest sense, leakage current caused by either peripheral or surface related mechanism is becoming more and more important when junction dimension is scaled down to 20um.

The RoA of InSb p+n diodes fabricated by cadmium solid-state diffusion and mesa process still have about one order of magnitude larger than the diodes prepared by beryllium implantation and planar process under dark condition in our laboratory. Comprehensive analysis and studies are required to explore the optimum implantation and annealing processing to suppress the area component of leakage current.

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