

# A Robust Data Retention Characteristic of Sol–Gel-Derived Nanocrystal Memory by Hot-Hole Trapping

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**Abstract**—A new sol–gel-derived  $\text{Ti}_x\text{Zr}_y\text{Si}_z\text{O}$  nanocrystal (NC) memory with a high-performance data retention characteristic is demonstrated by the hot-hole-trapping method. Prior to rapid thermal annealing, the high-density NC layer is formed by depositing a well-mixed solution of titanium tetrachloride, silicon tetrachloride, and zirconium tetrachloride. The electrical properties of the sol–gel-derived NC memory are demonstrated in terms of memory window, charge retention, program speed, and endurance. The memory window of the NC memory from the novel hot-hole-trapping mechanism can be achieved up to  $4.18 \pm 0.21$  V, and long retention times obtained from extrapolation up to  $10^6$  s are observed as 8%, 13%, and 21% window narrowing under respective temperatures of 25 °C, 85 °C, and 125 °C. The good electrical performance is attributed to the contribution of the high density of isolated NCs and hole-trapped into the deep-trap energy level, so no significant lateral and vertical charge leakage occurs.

**Index Terms**—Flash memory, hole trapping, nanocrystal (NC), sol–gel.

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## I. INTRODUCTION

FLASH memory has attracted more attention because of its nonvolatile, low-cost, and low-power-consumption characteristics [1], [2]. However, the conventional design of floating-gate (FG) Flash memory suffers from the serious charge loss issue as the feature size of these devices continues to shrink [3]. A novel nonvolatile memory (NVM) utilizing nanocrystal (NC) as the charge-storage layer was reported to replace the conventional FG memory [4]. Due to the benefit of discrete charge storage node, the NC memory had demonstrated exceptional properties such as fast program/erase speed, low programming potentials, and high endurance [5]. We had proposed a sol–gel spin-coating method on the memory field to incorporate the high- $\kappa$  material in the form of NC [6]–[9]. In comparison with other versatile deposition methods, the relatively cheap, simple, and uniform sol–gel method can mix very easily a variety of deposited materials without restriction. In addition, it can be fabricated in a normal atmospheric pressure instead of a high-vacuum system [10].

Generally, channel-hot-electron (CHE) injection is used to program the NC memory. Positive pulses are synchronously applied to the gate and drain of the device, and hence, electrons are injected into the charge-storage layer [11]. However, the study of NC memory programmed by the hot-hole-injection mechanism is still unavailable. In this letter, a new type of  $\text{Ti}_x\text{Zr}_y\text{Si}_z\text{O}$  NC layer, which was employed as the charge-trapping layer for the memory, was synthesized and obtained by the sol–gel method. This NC memory exhibited an interesting hot-hole-trapping property. The electrical characteristics, including program and erase speeds, retention, and endurance for the NC memory, are also demonstrated in this letter.

## II. EXPERIMENTS

The precursors utilized for the preparation of sol–gel solution were titanium tetrachloride ( $\text{TiCl}_4$ , 99.5%), zirconium tetrachloride ( $\text{ZrCl}_4$ , 99.5%), and silicon tetrachloride ( $\text{SiCl}_4$ , 99.5%). Ethanol was used as the solvent to disperse the precursors. Hydrochloric acid serving as the catalyst for the purposes of hydrolysis and condensation was added into the solution.  $\text{TiCl}_4$ ,  $\text{ZrCl}_4$ ,  $\text{SiCl}_4$ , and ethanol at a molar ratio of 1 : 1 : 1 : 1000 were mixed and stirred vigorously for 0.5 h to ensure a homogeneous state. The sol–gel was then spin coated

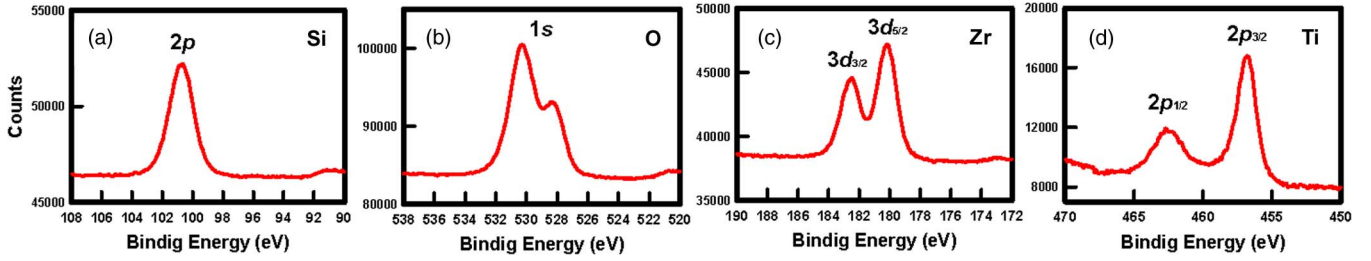


Fig. 1. (a) Si 2*p*, (b) O 1*s*, (c) Zr 3*d*, and (d) Ti 2*p* XPS spectra of the  $\text{Ti}_x\text{Zr}_y\text{Si}_z\text{O}$  NC.

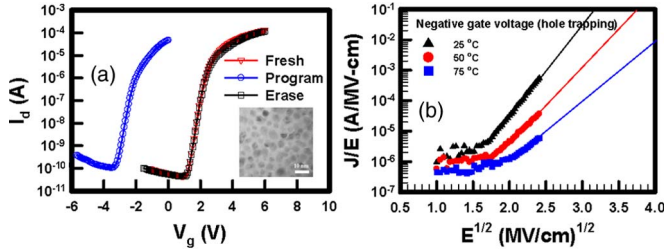


Fig. 2. (a)  $I_d$ - $V_g$  characteristics of the NC memory at fresh, program, and erase states, respectively. The inset shows the plan-view TEM image of the sol-gel-derived NCs. (b) P-F plot of the NC memory at different measuring temperatures.

onto the Si substrate. After thin-film deposition, the samples were subjected to annealing at 900 °C for 60 s in an  $\text{O}_2$  ambient to transform into the NCs.

The semiconductor manufacturing of sol-gel-derived NC memory was started with local oxidation of the Si process on a p-type (100) silicon substrate. After the cleaning process, a 4-nm tunneling oxide film was thermally grown at 925 °C in a furnace. The sol-gel film was then spin coated, followed by the RTA process. A 10-nm blocking oxide was deposited by plasma-enhanced chemical vapor deposition, and a 200-nm-thick amorphous-Si gate was then deposited. Afterward, the rest of the subsequent metal-oxide-semiconductor processes were performed to complete the sol-gel-derived NC Flash memory devices. The channel width and length of the fabricated memory are 10 and 0.35  $\mu\text{m}$ , respectively.

### III. RESULTS AND DISCUSSION

X-ray photoelectron spectroscopy (XPS) was used to verify the chemical composition of the  $\text{Ti}_x\text{Zr}_y\text{Si}_z\text{O}$  NC. Fig. 1 shows the high-resolution spectra displaying the Si 2*p*, O 1*s*, Zr 3*d*, and Ti 2*p* peaks for the sol-gel-derived NC, respectively. Typical peaks are observed clearly in the figures, suggesting that the complete structural formation of the  $\text{Ti}_x\text{Zr}_y\text{Si}_z\text{O}$  NC had occurred [12]. It should be noted that the thickness of the sol-gel spin-coating thin film is only about 10 nm, so the spectra from XPS analysis should include the substrate effect. The Si 2*p* and O 1*s* spectra are only for reference because the substrate material is silicon oxide.

Fig. 2(a) shows the  $I_d$ - $V_g$  characteristics of the NC memories at fresh, program, and erase states, respectively. The measured conditions for programming are  $V_g = -7$  V,  $V_d = 7$  V, and 1 ms, and that for erasing are  $V_g = 7$  V,  $V_d = 7$  V, and 1 ms. Unlike the usual publication of memory that is programmed by CHE, the  $I_d$ - $V_g$  curve of the memory in Fig. 2(a) exhibits an

interesting shift to the left after programming, implying that the trapped charge to the NC is hot hole. Therefore, a band-band hot hole (BBHH) was used to program, and CHE was used to erase these devices hereafter. We have tried to program by injecting the electrons (by applying a positive voltage to both the gate and drain), but no significant shift of the  $I_d$ - $V_g$  curve was observed. On the contrary, the memory window by the BBHH method can be tuned out to be  $4.18 \pm 0.21$  V ( $n = 15$ ), which is significantly larger than that of other reports [1]–[10]. The inset of Fig. 2(a) shows the plan-view image of transmission electron microscopy (TEM) of the NC by the sol-gel method. The density of the NC is estimated to be  $2 \times 10^{12} \text{ cm}^{-2}$  with a size range of about 3–5 nm. The high-density and isolated NCs are beneficial for better charge trapping performance due to a sufficient trapping site in the NCs.

The Poole-Frenkel (P-F) current is proposed to explain the interesting hot-hole-trapping effect of memory [13]. The P-F current is used to describe the field-dependent thermal emission of the carriers in the trap. The expression for current density according to P-F emission can be written as [13]

$$J_{\text{FP}} = cE_{\text{ox}} \exp \left[ \left( (dE_{\text{ox}})^{1/2} - \varphi_t \right) q / k_b T \right]$$

where  $K_b$ ,  $T$ ,  $c$ ,  $d$ , and  $\varphi_t$  are the Boltzmann's constant, the measurement temperature, a constant that depends on the trap density, a constant that depends on the electric permittivity, and the depth of the trap potential well, respectively.

Fig. 2(b) shows the plot of  $\ln(J/E)$  versus square root of applied electrical field at different temperatures by hole trapping. To simulate hot-hole programming of memory, a negative voltage was applied on the gate from 0 to -20 V, with a constant drain voltage of 4 V during the measurement. The barrier height of the trap for  $\text{Ti}_x\text{Zr}_y\text{Si}_z\text{O}$  to silicon oxide is extracted to be 1.15 eV for hole trapping by the P-F current [13]. We also measured the P-F current of hot-electron programming by applying a positive gate voltage. However, the obtained curve is not linear. Good linear fitting of the measured curve is observed by the Fowler-Nordheim (F-N) tunneling expression, implying that F-N tunneling plays a major role for electrons in the  $\text{Ti}_x\text{Zr}_y\text{Si}_z\text{O}$  NC memory.

Although the large window is observed for the  $\text{Ti}_x\text{Zr}_y\text{Si}_z\text{O}$  NC memory, the operation speed is a concern due to the heavy effective mass of the hole. Therefore, the program and erase speeds of the NC memory were measured under various bias conditions. Fig. 3 shows program and erase characteristics under different operation conditions. As can be seen in Fig. 3, the program speed is 97  $\mu\text{s}$  with a -2-V  $V_t$  shift for the program

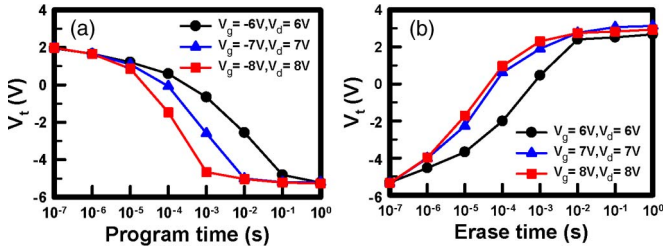


Fig. 3. (a) Program and (b) erase characteristics of the NC memory device under various operation conditions.

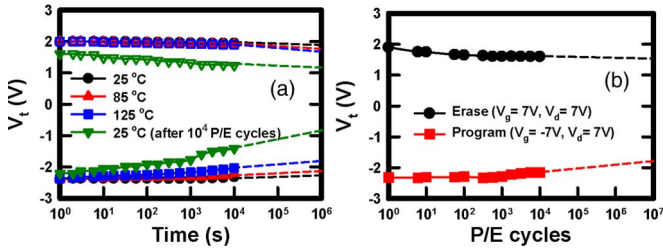


Fig. 4. (a) Retention characteristics of the NC memories at measurement temperatures of 25 °C, 85 °C, and 125 °C. The postcycling retention at 25 °C is also shown. (b) Endurance characteristic of the NC memory device.

conditions of  $V_g = -7$  V and  $V_d = 7$  V, while only 2.5  $\mu$ s is required with a 2-V  $V_t$  shift for erase operation at  $V_g = 7$  V and  $V_d = 7$  V. The fast transient of erase characteristics originates from hot electrons, which exhibit higher mobility than holes. As compared to previous reports [1]–[3], [6], [7], this new type of sol–gel-derived NC memory exhibits a relatively fast operating speed under similar condition. This result indicates that the sol–gel-derived NC memory yields a high-efficiency charge-storage layer with fast operation speed and low applied voltage by the hot-hole-trapping method.

The retention characteristics of the NC memory devices at erase and program states are shown in Fig. 4(a). The retention times are extrapolated up to  $10^6$  s with only about 8%, 13%, and 21% window narrowing at 25 °C, 85 °C, and 125 °C measurements, respectively. As compared to previous reports of sol–gel-derived NC memories [6]–[10], the retention characteristic by the hot-hole-trapping mechanism is much improved. The superior performance is attributed to the effects of the isolated NCs and hole-trapped into the deep-trap energy level, so no significant lateral and vertical charge leakage occurred. For ease of comparison, the retention after 10 000 programming and erasing (P/E) cycles is also shown in Fig. 4(a). The window narrowing of postcycling retention demonstrates a worse property than that of fresh retention. For example, the narrowing is about 19% for the postcycling retention data at  $10^3$  s, while only 2% narrowing for the fresh retention data is observed. Although postcycling retention is unsatisfactory, the window narrowing remains below 50% for extrapolating up to  $10^6$  s. The endurance of the NC NVM extrapolated up to  $10^7$  P/E cycles is shown in Fig. 4(b). The measured conditions for programming are  $V_g = -7$  V,  $V_d = 7$  V, and 1 ms, and that

for erasing are  $V_g = 7$  V,  $V_d = 7$  V, and 1 ms. The memory window narrowing after  $10^7$  P/E cycles is estimated to be 20.7%. The shifts of threshold voltages in programming and erasing states are slightly after a couple of cycles. The good endurance characteristic indicates that the amount of operation-induced trapped charges is very small.

#### IV. CONCLUSION

In this letter, we have proposed a new sol–gel-derived  $Ti_xZr_ySi_zO$  NC memory by utilizing hot-hole trapping to program. The XPS analysis confirms the chemical composition of the  $Ti_xZr_ySi_zO$  NC. Owing to the merit of high-density NCs and hot-hole-trapping mechanism, this NC memory exhibits excellent electrical performance in terms of large memory window, high operation speed, high data retention, and exceptional endurance.

#### REFERENCES

- [1] P. H. Tsai, K. S. Chang-Liao, T. C. Liu, T. K. Wang, P. J. Tzeng, C. H. Lin, L. S. Lee, and M. J. Tsai, "Charge-trapping-type flash memory device with stacked high- $k$  charge-trapping layer," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 775–777, Jul. 2009.
- [2] T. M. Pan and W. W. Yeh, "A high- $k$   $Y_2O_3$  charge trapping layer for nonvolatile memory application," *Appl. Phys. Lett.*, vol. 92, no. 17, p. 173 506, Apr. 2008.
- [3] D. Shahrjerdi, D. I. Garcia-Gutierrez, and S. K. Banejee, "Fabrication of Ni nanocrystal flash memories using a polymeric self-assembly approach," *IEEE Electron Device Lett.*, vol. 28, no. 9, pp. 793–796, Sep. 2007.
- [4] Y. H. Lin, C. H. Chien, C. T. Lin, C. W. Chan, C. Y. Chang, and T. F. Lei, "High-performance nonvolatile  $HfO_2$  nanocrystal memory," *IEEE Electron Device Lett.*, vol. 26, no. 3, pp. 154–156, Mar. 2005.
- [5] F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, "Memory characteristics of Co nanocrystal memory device with  $HfO_2$  as blocking oxide," *Appl. Phys. Lett.*, vol. 90, no. 13, p. 132 102, Mar. 2007.
- [6] H. C. You, T. H. Hsu, F. H. Ko, J. W. Huang, and T. F. Lei, "Hafnium silicate nanocrystal memory using sol–gel-spin-coating method," *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 644–646, Aug. 2006.
- [7] F. H. Ko, H. C. You, and T. F. Lei, "Sol–gel-derived double-layered nanocrystal memory," *Appl. Phys. Lett.*, vol. 89, no. 25, p. 252 111, Dec. 2006.
- [8] F. H. Ko, H. C. You, C. M. Chang, W. L. Yang, and T. F. Lei, "Fabrication of SONOS-type flash memory with the binary high- $k$  dielectrics by the sol–gel spin coating method," *J. Electrochem. Soc.*, vol. 154, no. 4, pp. H268–H270, 2007.
- [9] H. C. You, C. C. Wu, F. H. Ko, T. F. Lei, and W. L. Yang, "Novel coexisted sol–gel derived poly-Si-oxide-nitride-oxide-silicon type memory," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 25, no. 6, pp. 2568–2571, Nov. 2007.
- [10] H. C. You, T. H. Hsu, F. H. Ko, J. W. Huang, W. L. Yang, and T. F. Lei, "SONOS-type flash memory using an  $HfO_2$  as a charge trapping layer deposited by the sol–gel spin-coating method," *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 653–655, Aug. 2006.
- [11] T. Y. Chiang, T. S. Chao, Y. H. Wu, and W. L. Yang, "High-program/erase-speed SONOS with *in situ* silicon nanocrystals," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1148–1151, Oct. 2008.
- [12] T. H. Hsu, H. C. You, F. H. Ko, and T. F. Lei, "PolySi-SiO<sub>2</sub>-ZrO<sub>2</sub>-SiO<sub>2</sub>-Si flash memory incorporating a sol–gel-derived ZrO<sub>2</sub> charge trapping layer," *J. Electrochem. Soc.*, vol. 153, no. 11, pp. G934–G937, 2006.
- [13] J. Kolodzey, E. A. Chowdhury, T. N. Adam, G. Qui, I. Rau, J. O. Olowolafe, J. S. Suehle, and Y. Chen, "Electrical conduction and dielectric breakdown in aluminum oxide insulators on silicon," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 121–128, Jan. 2000.