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Design of differential low-noise amplifier with cross-coupled-SCR ESD protection scheme

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ABSTRACT

The pin-to-pin electrostatic discharge (ESD) stress was one of the most critical ESD events for differential input pads. The pin-to-pin ESD issue for a differential low-noise amplifier (LNA) was studied in this work. A new ESD protection scheme for differential input pads, which was realized with cross-coupled silicon-controlled rectifier (SCR), was proposed to protect the differential LNA. The cross-coupled-SCR ESD protection scheme was modified from the conventional double-diode ESD protection scheme without adding any extra device. The SCR path was established directly from one differential input pad to the other differential input pad in this cross-coupled-SCR ESD protection scheme, so the pin-to-pin ESD robustness can be improved. The test circuits had been fabricated in a 130-nm CMOS process. Under pin-to-pin ESD stresses, the human-body-model (HBM) and machine-model (MM) ESD levels of the differential LNA with the cross-coupled-SCR ESD protection scheme are >8 kV and 800 V, respectively. Experimental results had shown that the new proposed ESD protection scheme for the differential LNA can achieve excellent ESD robustness and good RF performances.

1. Introduction

Electrostatic discharge (ESD) is getting more attention in nanoscale CMOS technology, because it has become one of the most important reliability issues in IC chips [1–4]. With the evolution of CMOS technology, ESD protection design in nanoscale CMOS process becomes more challenging, because the upper bound of the ESD protection design window for an input pad, which is set by the gate-oxide breakdown voltage, is lowered. To achieve satisfactory ESD robustness without seriously degrading circuit performance, ESD protection design should be taken into consideration during the design phase of all integrated circuits, especially radio-frequency (RF) circuits [5]. Since the low-noise amplifier (LNA) is usually connected to the external of the RF receiver chip such as the off-chip antenna, on-chip ESD protection circuits are needed for all input pads of the LNA.

In the ESD-test standards, there are several ESD-test pin combinations. Besides the positive-to-VDD (PD-mode), positive-to-VSS (PS-mode), negative-to-VDD (ND-mode), and negative-to-VSS (NS-mode) ESD tests, the pin-to-pin ESD test is also specified to evaluate ESD robustness of the differential input pads. Under the pin-to-pin ESD test, one input pad is stressed with the other input pad relatively grounded, while all the other pads including all VDD and VSS pads are floating [6]. To provide efficient pin-to-pin ESD protection, the ESD protection device should be turned on quickly with low enough clamping voltage and low enough turn-on resistance under ESD stresses to effectively protect the thin gate oxides of MOS transistors in the differential input stage. As the gate-oxide thickness becomes much thinner in nanoscale CMOS processes, robust ESD protection design against all ESD-test pin combinations, especially pin-to-pin ESD tests, becomes more challenging.

There are several ESD protection designs reported for RF front-end circuits to optimize RF performance and ESD robustness [7–13]. Since the pin-to-pin ESD stress was one of the most critical ESD events for differential input pads, some ESD protection designs have been presented to improve ESD robustness of LNA under pin-to-pin ESD stresses [14]. In this paper, a new ESD protection design realized with cross-coupled silicon-controlled rectifier (SCR) is proposed to protect the differential LNA. The cross-coupled-SCR ESD protection scheme is modified from the conventional double-diode ESD protection scheme without adding any extra device. Verified in a 130-nm CMOS process, the new proposed ESD protection scheme exhibited high ESD robustness, especially high pin-to-pin ESD robustness.

2. Differential LNA design

In LNA design, differential configuration is popular because the differential LNA has the advantages of better common-mode noise

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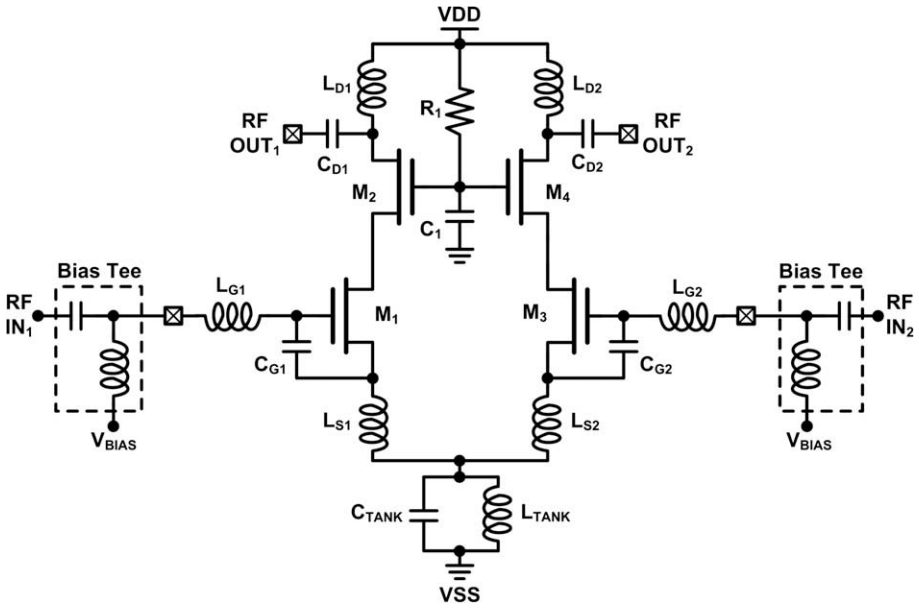

Fig. 1. Differential LNA without ESD protection for comparison reference.

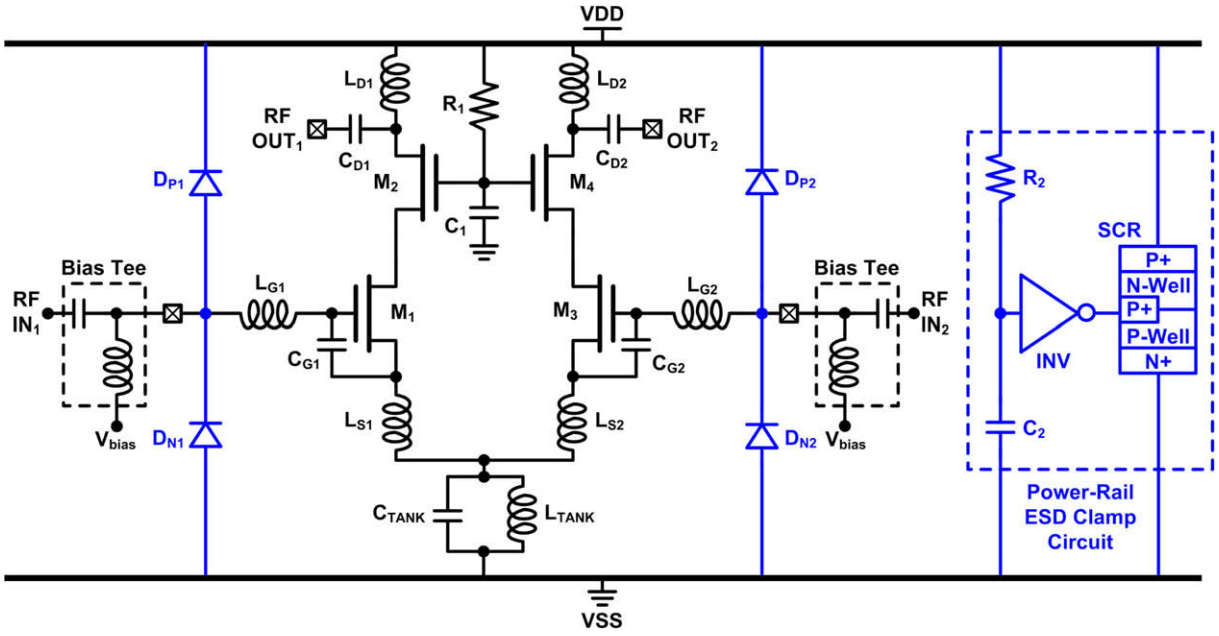

Fig. 2. Differential LNA with conventional double-diode ESD protection scheme.

rejection, as well as less sensitivity to substrate noise, supply noise, and bondwire inductance variation [15–21]. In addition, the differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer.

In this study, the circuit schematic of the LNA without ESD protection for comparison reference is shown in Fig. 1. The architecture of common-source with inductive degeneration is applied to match the input impedance of LNA to the source impedance (50 Ω) at the operating frequency of 5 GHz. Good isolation between the input and output can be enhanced by using the cascode configuration. Moreover, the cascode configuration reduces Miller effect and provides good stability [22]. The dimensions of the input NMOS transistors M_1 and M_3 are designed according to the compromise between noise figure and power consumption. Since the small-signal operation of the differential LNA is symmetrical, the half circuit can be referred to analyze the LNA. The input impedance (Z_{in}) of the RF IN$_1$ pad can be calculated as

$$Z_{in} = \frac{1}{j\omega(C_{gs1} + C_{G1})} + j\omega(L_{G1} + L_{S1}) + \omega_T L_{S1} \quad (1)$$

where C_{gs1} is the gate-source capacitance of M_1, C_{G1} is the added capacitance between the gate and source terminals of M_1, L_{G1} is the gate inductance, and L_{S1} is the source inductance. The ω_T is the unity-gain angular frequency of M_1, which can be expressed as

$$\omega_T = \frac{g_{m1}}{C_{gs1}} \quad (2)$$

where g_{m1} is the transconductance of M_1. With the input matching network resonating at the operating frequency, the input impedance ($Z_{in\_Resonance}$) is purely real and can be given by

$$Z_{in\_Resonance} = \omega_T L_{S1} = \frac{g_{m1}}{C_{gs1}} L_{S1} \quad (3)$$

To match the input impedance at resonance to the source impedance, L_{S1} is determined once the size of M_1 has been chosen. The resonance angular frequency (ω_0), which is designed to be the operating frequency, can be obtained by

$$\frac{1}{\omega_0(C_{gs1} + C_{G1})} = \omega_0(L_{G1} + L_{S1}) \quad (4)$$

At resonance, the source inductor L_{S1} and gate inductor L_{G1} compensate the capacitance at the gate terminal of M_1. After L_{S1} is determined to match the source impedance, the remaining capacitive impedance needs to be cancelled by L_{G1}. However, the small C_{gs1} leads to intolerable large L_{G1}. Therefore, an extra capacitor C_{G1} is added in parallel with C_{gs1} to reduce the required inductance of L_{G1}. The drain inductor L_{D1} and drain capacitor C_{D1} form the output matching network to match the output impedance of LNA to 50 Ω.

The gate voltages of M_2 and M_4 are biased to VDD through the resistor R_1. The capacitor C_1 acts as a decoupling capacitor. L_{TANK} and C_{TANK} form a LC-tank to enhance the common-mode rejection. With the deep N-well structure, the P-well (bulk) region of each NMOS transistor can be fully isolated from the common P-substrate, so the source and bulk terminals are connected together to eliminate the body effect. All of the inductors are the on-chip spiral inductors implemented by the top metal layer, and all of the capacitors in the differential LNA are realized by the metal–insulator–metal (MIM) capacitors. The aforementioned active and passive devices are fully integrated in the experimental test chip in a 130-nm CMOS process. In order to verify the effectiveness of the on-chip ESD protection circuits at the input pads, the ac coupling capacitor between the input pad and L_{G1} (L_{G2}) is not realized in the test chip, because the ac coupling capacitor connected to the input pad can block some ESD energy when the input pad is stressed by ESD. Thus, the off-chip bias tee is needed to combine the RF input signal and the dc bias at the input node during RF measurement.

3. ESD protection design on differential LNA

3.1. Conventional double-diode ESD protection scheme

The conventional double-diode ESD protection scheme is shown in Fig. 2. A P+/N-well diode (D_P) is connected between each input pad and VDD, while an N+/P-well diode (D_N) is connected between each input pad and VSS. Besides, the power-rail ESD clamp circuit is used to provide ESD current paths between VDD and VSS under ESD stresses.

3.2. New proposed cross-coupled-SCR ESD protection scheme

The four ESD protection diodes at the differential input pads in the conventional double-diode ESD protection scheme, which include two P+/N-well diodes (D_P) and two N+/P-well diodes (D_N), are reserved in the new proposed design, but the placement is changed. Fig. 3 illustrates the concept of the proposed ESD protection scheme. In this new proposed ESD protection design, the SCR path is established directly from one differential input pad to the other differential input pad without adding any extra device. The SCR path has very high ESD robustness due to its low clamping voltage under ESD stress conditions [23]. As illustrated in Fig. 3a, by merging D_{P1} (P+/N-well diode for RF IN_1 pad) and D_{N2} (N+/P-well diode for RF IN_2 pad) together, an SCR path from RF IN_1 pad to RF IN_2 pad can be established for pin-to-pin ESD protection without adding any extra device. Similarly, D_{P2} (P+/N-well diode for RF IN_2 pad) and D_{N1} (N+/P-well diode for RF IN_1 pad) can be merged together to form another SCR path from RF IN_2 pad to RF IN_1 pad, as illustrated in Fig. 3b. Since the pin-to-pin ESD path is established by SCR, the cross-coupled-SCR ESD protection scheme is expected to have high pin-to-pin ESD robustness. Under PD-PS-, ND-, and NS-mode ESD stresses, the ESD levels are not altered, since D_{P1}, D_{N1}, D_{P2}, and D_{N2} still exist.

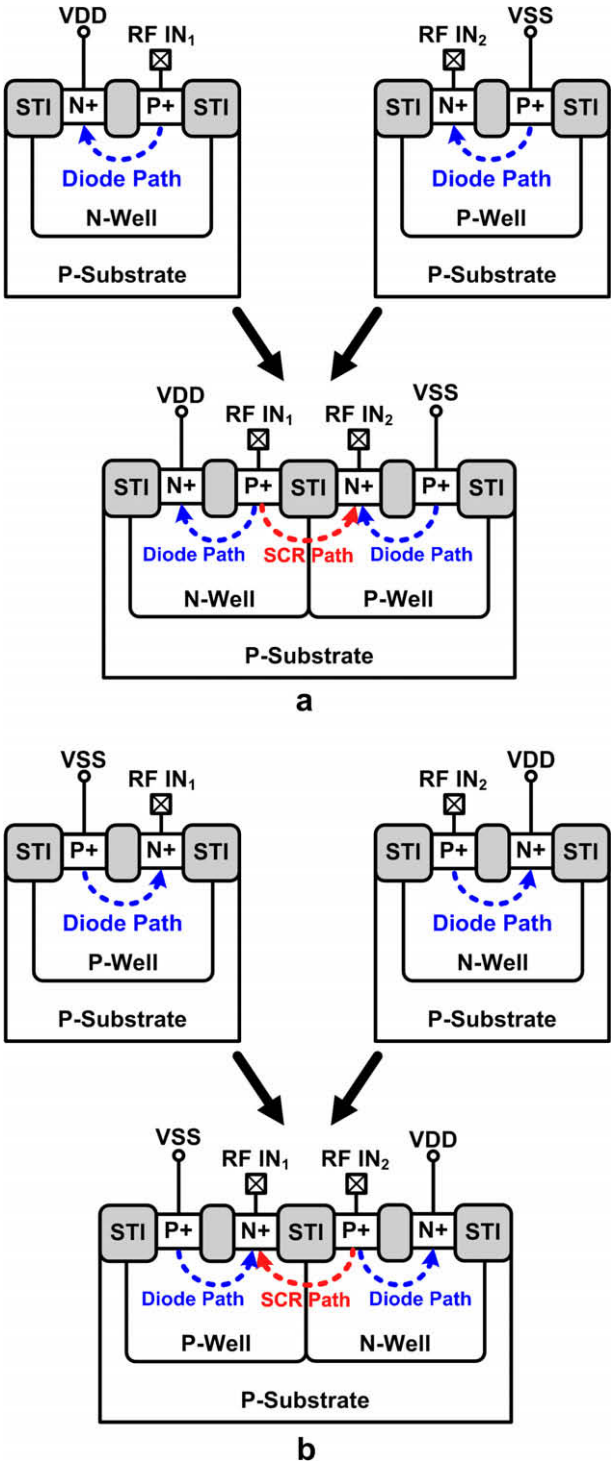

Fig. 3. Establishing the SCR paths between the differential input pads by combining (a) D_{P1} (P+/N-well diode for RF IN_1 pad) with D_{N2} (N+/P-well diode for RF IN_2 pad), and (b) D_{P2} (P+/N-well diode for RF IN_2 pad) with D_{N1} (N+/P-well diode for RF IN_1 pad).

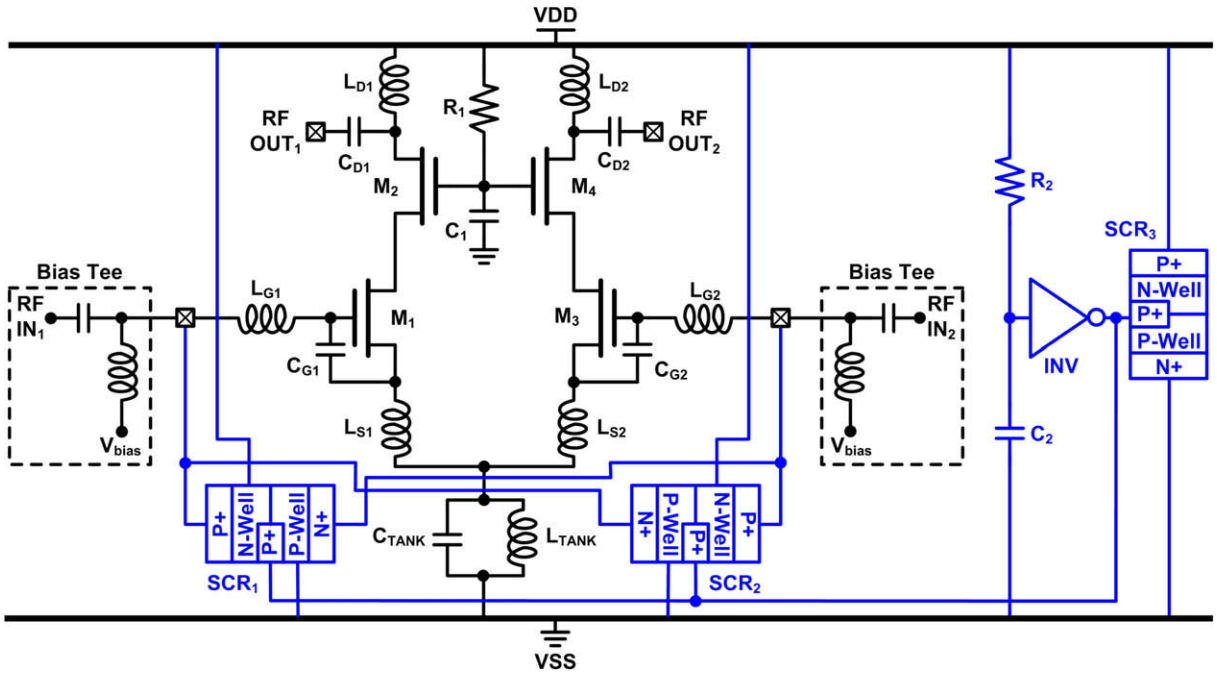

Fig. 4. Differential LNA with proposed ESD protection scheme of cross-coupled SCR.

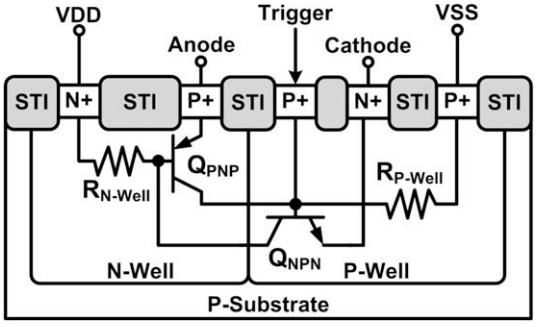

Fig. 5. Cross-sectional view and equivalent circuit of SCR.

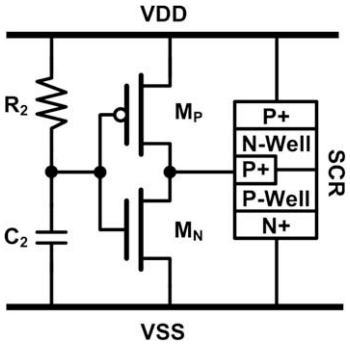

Fig. 6. Power-rail ESD clamp circuit realized with SCR.

Fig. 4 shows the circuit schematic of the differential LNA with the new proposed ESD protection scheme of cross-coupled SCR. SCR$_1$ is placed close to the RF IN$_1$ pad to provide efficient pin-to-pin ESD current path from the RF IN$_1$ pad to the RF IN$_2$ pad. Similarly, SCR$_2$ is placed close to the RF IN$_2$ pad to provide efficient ESD current path from the RF IN$_2$ pad to the RF IN$_1$ pad under pin-to-pin ESD stresses. To reduce the trigger voltage and increase

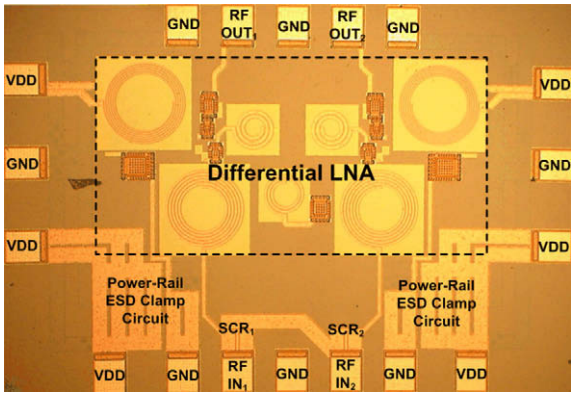

Fig. 7. Chip micrograph of differential LNA with proposed cross-coupled-SCR ESD protection scheme.

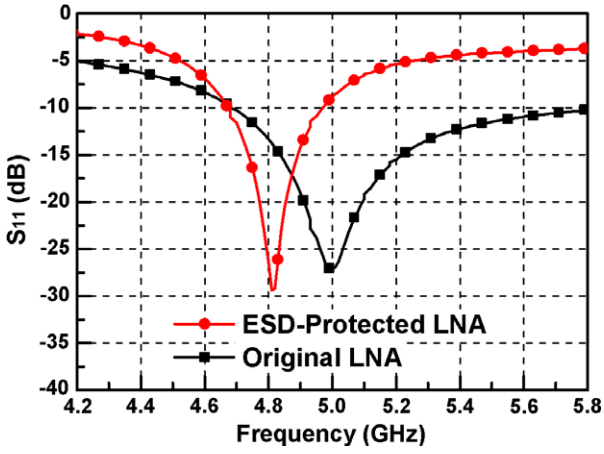

Fig. 8. Measured S_{11}-parameters of differential LNA with the proposed cross-coupled-SCR ESD protection scheme, and the original differential LNA without ESD protection.

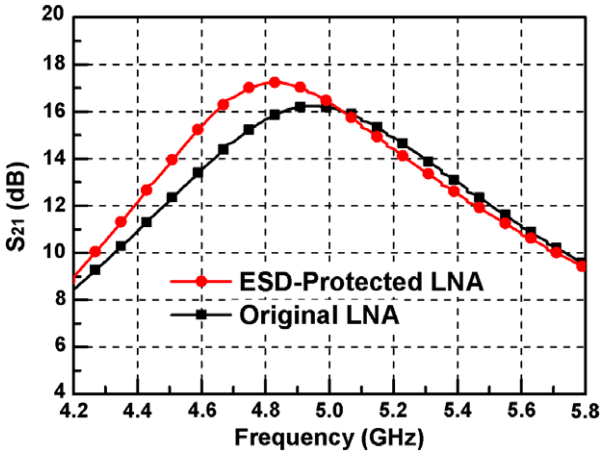

Fig. 9. Measured S_{21}-parameters of differential LNA with the proposed cross-coupled-SCR ESD protection scheme, and the original differential LNA without ESD protection.

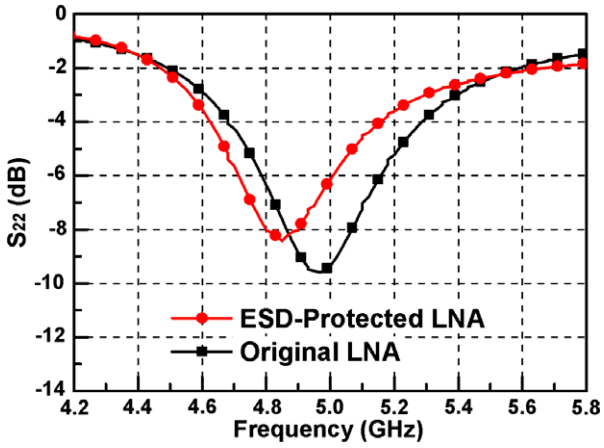

Fig. 10. Measured S_{22}-parameters of differential LNA with the proposed cross-coupled-SCR ESD protection scheme, and the original differential LNA without ESD protection.

the turn-on speed of the SCR under ESD stresses, the substrate-triggered technique is used [23]. As shown in Figs. 4 and 5, the P + trigger diffusion is added in the P-well region, and is connected to the ESD detection circuit in the power-rail ESD clamp circuit. In the proposed ESD protection scheme, the PS-mode ESD current path for the RF IN_1 (RF IN_2) pad is provided by D_{P1} (D_{P2}) embedded in SCR_1 (SCR_2) and the power-rail ESD clamp circuit. The ND-mode ESD current path for the RF IN_1 (RF IN_2) pad is provided by the power-rail ESD clamp circuit and D_{N1} (D_{N2}) embedded in SCR_2 (SCR_1). Under pin-to-pin ESD stresses, the ESD current paths between the differential input pads are provided by the cross-coupled SCR_1 and SCR_2.

The total parasitic capacitance from the cross-coupled SCR at each input pad is specified as 300 fF, which is the same as that of the double-diode ESD protection scheme in [14]. To achieve the total parasitic capacitance of 300 fF at each differential input pad, the sizes of SCR_1 and SCR_2 are all drawn as 60 μm × 2.4 μm. The source inductors (L_{S1} and L_{S2}) and gate inductors (L_{G1} and L_{G2}) are adjusted to achieve the input matching of LNA with the cross-coupled SCR.

3.3. Power-rail ESD clamp circuit

Fig. 6 shows the power-rail ESD clamp circuit used in this work, where the substrate-triggered SCR is used as the ESD clamp device. The cross-sectional view and equivalent circuit of this SCR is similar to that in Fig. 5. The ESD detection circuit consists of an RC timer and an inverter. The resistor R_2 and capacitor C_2 form the RC timer with the time constant of 0.3 μs, which can distinguish the ESD transients from the normal circuit operating conditions [24]. Under normal circuit operating conditions, the node between R_2 and C_2 is charged to high potential (VDD). Since NMOS M_N is turned on and PMOS M_P is turned off, the trigger node of the SCR is tied to VSS and no trigger current is injected to the trigger node of SCR. Thus, the SCR is kept off under normal circuit operating conditions. Under ESD stresses, the ESD voltage at VDD has the rise time in the order of nanosecond. With the RC delay provided by R_2 and C_2, the gate voltages of M_P and M_N are initially kept at low potential (~0 V). Therefore, M_P is turned onto inject trigger current into the trigger node. As a result, the SCR is turned onto provide ESD current path from VDD to VSS. Since the power-rail ESD clamp circuit is placed between VDD and VSS, it does not contribute any parasitic effects to neither input nor output pads. Besides, the ESD detection circuit in the power-rail ESD clamp circuit can also serve as the trigger circuit for the cross-coupled SCR devices between the differential input pads.

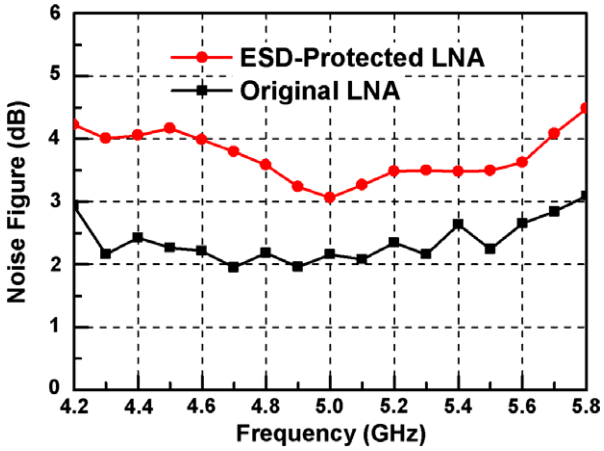

Fig. 11. Measured noise figures of differential LNA with the proposed cross-coupled-SCR ESD protection scheme, and the original differential LNA without ESD protection.

4. Experimental results

4.1. RF performances

The differential LNA circuits have been fabricated in 130-nm CMOS process. The chip micrograph of the differential LNA with cross-coupled-SCR ESD protection scheme is shown in Fig. 7. To measure the *S*-parameters of the differential LNA, four-port *S*-parameter measurement with Agilent E8361A network analyzer is performed. The measurement system converted the measured four-port *S*-parameters to the differential two-port *S*-parameters. The measured RF performance of the differential LNA with cross-coupled-SCR ESD protection scheme is compared with that of the original differential LNA without ESD protection in Figs. 8–11. To compare the input matching conditions, the measured S_{11}-parameters of these two differential LNAs are shown in Fig. 8. It is observed that the operating frequency of the differential LNA with cross-coupled-SCR ESD protection scheme is shifted from 5 GHz to 4.8 GHz. At 4.8-GHz, the measured S_{11}-parameter is −26.3 dB. The shift in the operating frequency is due to the lack of RF model for SCR

Table 1
HBM and MM ESD robustness under different test pin combinations.

ESD robustness	Original LNA		ESD-protected LNA	
	HBM	MM (V)	HBM (kV)	MM (V)
Positive to VSS	<50 V	<10	3.5	300
Positive to VDD	<50 V	<10	6	550
Negative to VSS	<50 V	<10	6	550
Negative to VDD	<50 V	<10	3.5	350
Pin to Pin	<50 V	<10	>8	800
VDD to Vss	0.5 kV	<10	>8	>1000

device in the given CMOS process. The macro model of SCR was ever reported to simulate its turn-on mechanism during ESD stress [25,26]; however, the small-signal model of SCR in RF circuit operation condition is still scarce. To more precisely simulate the differential LNA with the cross-coupled-SCR ESD protection scheme, the parasitic effects of the SCR can be modeled by the diodes with P+/N-well, P-well/N-well, and N+/P-well junctions, rather than only the 300-fF capacitance.

Fig. 9 compares the measured power gains (S_{21}-parameters) of these two differential LNAs. At 4.8 GHz, the S_{21}-parameter of differential LNA with cross-coupled-SCR ESD protection scheme is 17.2 dB. The measured S_{22}-parameters of these two differential LNAs are compared in Fig. 10. The S_{22}-parameter of differential LNA with cross-coupled-SCR ESD protection scheme is −8 dB at 4.8 GHz. Satisfactory reverse isolation is also achieved in differential LNA with cross-coupled-SCR ESD protection scheme, where the S_{12}-parameter is lower than −26 dB at 4.8 GHz. Fig. 11 shows the measured noise figures of these two differential LNAs. At 4.8 GHz, the noise figure of differential LNA with cross-coupled-SCR ESD protection scheme is 3.58 dB. The increase in the noise figure is attributed to the parasitic effects of ESD protection devices with the overlapped wide metal lines in layout, which are connected between the differential input pads and the cross-coupled SCR devices.

4.2. ESD robustness

The human-body-model (HBM) [27] and machine-model (MM) [28] ESD levels are also measured from the differential LNAs. The failure criterion is 30% voltage shift under 1-μA current bias. During ESD tests, the off-chip bias tee is not included. The measured HBM and MM ESD levels of the LNA circuits are listed in Table 1. The LNA without ESD protection is very vulnerable to ESD, because it fails at 50-V HBM and 10-V MM ESD tests. The differential LNA with cross-coupled-SCR ESD protection scheme can pass 3.5-kV-HBM and 300-V-MM PS-mode and ND-mode ESD tests. Moreover, the differential LNA with cross-coupled-SCR ESD protection scheme can sustain pin-to-pin ESD stresses of over 8-kV HBM and 800-V MM.

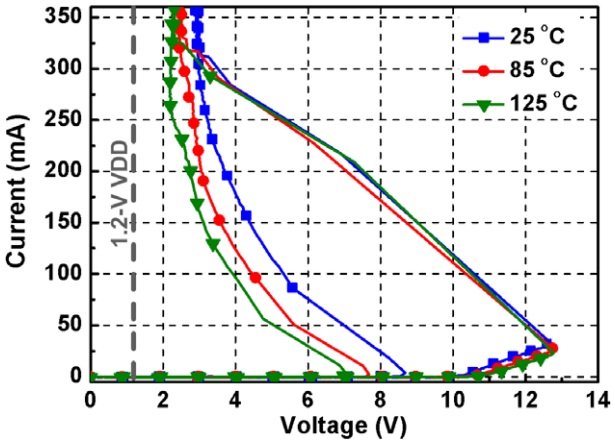

Fig. 12. Measured dc *I–V* curves of stand-alone SCR under different temperatures.

Table 2 summarizes the measured performances of the original differential LNA without ESD protection and the differential LNA with the new proposed cross-coupled-SCR ESD protection scheme, and compares their performances to those of the prior CMOS differential LNA circuits. The proposed ESD-protected differential LNA in this work exhibits excellent ESD robustness as compared with the other differential LNA circuits, especially in the pin-to-pin ESD stress.

4.3. Latchup immunity

Using SCR as the ESD protection device could introduce latchup concern. To avoid latchup issue, the holding voltage of SCR must be higher than the power-supply voltage, which is 1.2 V in this work. The dc *I–V* characteristics of the stand-alone SCR used in this design are measured by Tektronics 370B curve tracer. As shown in Fig. 12, the curves with square, circular, and triangular symbols indicate the *I–V* characteristics of the stand-alone SCR without trigger circuit under 25, 85, and 125 °C, respectively. The holding voltages of the stand-alone SCR under 25, 85, and 125 °C are 2.84, 2.58, and 2.38 V, respectively. With the holding voltage higher than the power-supply voltage (1.2 V), the SCR can be safely used in this RF chip without latchup issue.

4.4. Discussion on pin-to-pin ESD current paths

Under pin-to-pin ESD stresses, there are two ESD current paths exist in the cross-coupled-SCR ESD protection scheme. One ESD current path in the cross-coupled-SCR ESD protection scheme is shown in Fig. 13a, which is similar to that in the conventional double-diode ESD protection scheme. The voltage drop ($V_{\text{Pin-to-Pin1}}$) along this pin-to-pin ESD current path is

Table 2
Comparison on ESD robustness among CMOS differential LNAS.

	Technology	f_0 (GHz)	VDD (V)	P_{DC} (mW)	NF (dB)	S_{21} (dB)	S_{11} (dB)	HBM ESD level (kV)	MM ESD level (V)
Original LNA (this work)	0.13-μm CMOS	5	1.2	10.3	2.16	16.2	−27.2	<0.05	<10
ESD-protected LNA (this work)	0.13-μm CMOS	4.8	1.2	10.3	3.58	17.2	−26.3	3.5	300
Ref. [14] (double-diode-protected LNA)	0.13-μm CMOS	5	1.2	10.3	2.43	17.9	−18.7	2.5	200
Ref. [15]	90-nm CMOS	0.2–3.2	1.2	25	1.76	15.5	−10	2.4	N/A
Ref. [16]	0.13-μm CMOS	18	1.5	36	4.1	22.4	−7	2	N/A
Ref. [17]	0.18-μm CMOS	6	1.8	6.48	3	7.1	−10	N/A	N/A
Ref. [18]	0.13-μm CMOS	3–5	1.5	45	4	25.8	−11	1.5	N/A
Ref. [19]	0.18-μm CMOS	5.8	1.8	14.4	3.7	12.5	−15	N/A	N/A
Ref. [20]	0.13-μm CMOS	2–4.6	1.5	16.5	3.5	9.5	−10	N/A	N/A
Ref. [21]	0.18-μm CMOS	5.75	1	16	0.9	14.2	N/A	N/A	N/A

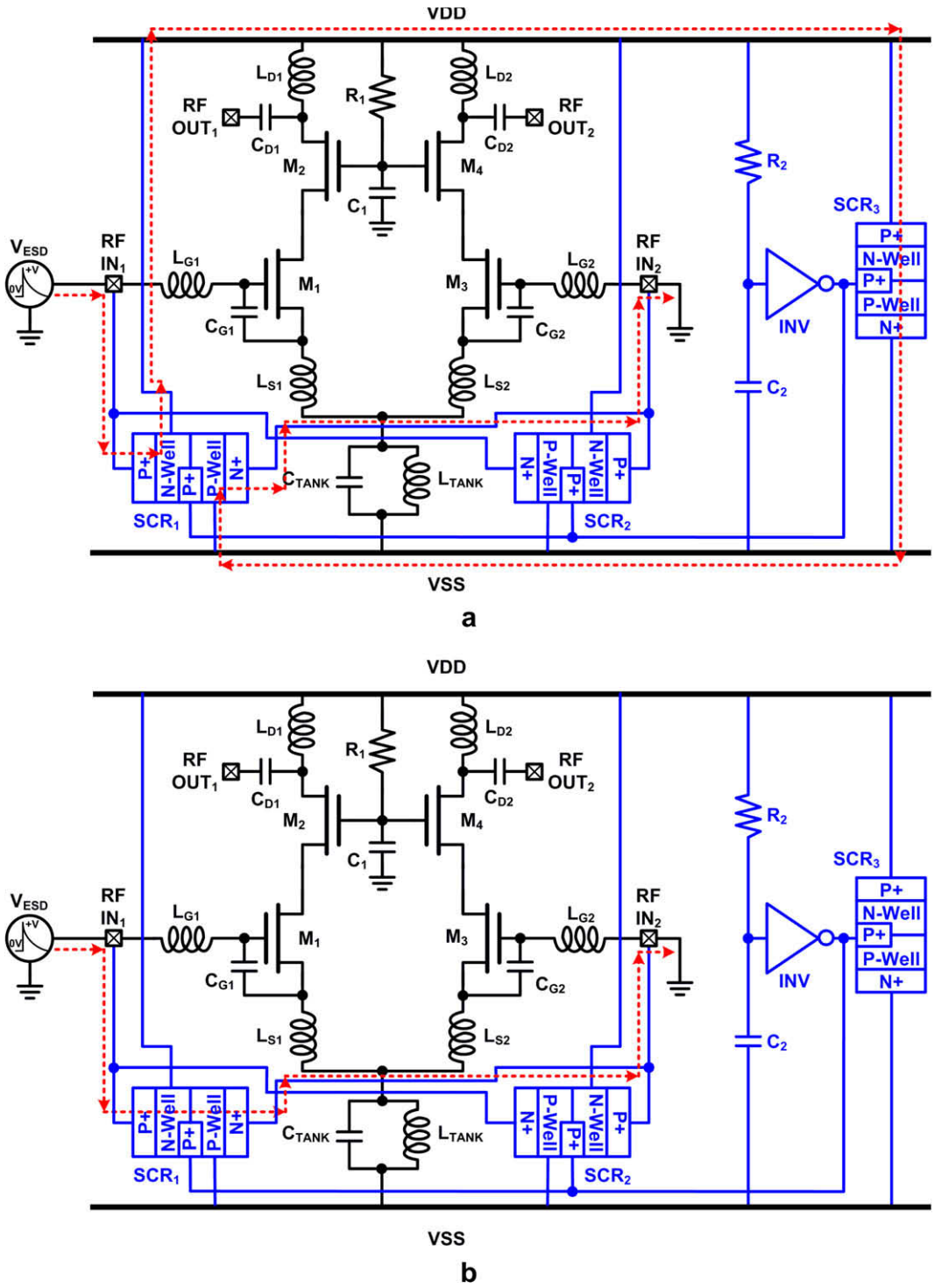

Fig. 13. ESD current paths through (a) diodes and power-rail ESD clamp circuit, and (b) SCR, in differential LNA with the proposed cross-coupled-SCR ESD protection scheme under pin-to-pin ESD stresses.

$$V_{\text{Pin-}to\text{-Pin1}} = V_{\text{DP1}} + V_{\text{VDD\_Bus}} + V_{\text{SCR3}} + V_{\text{VSS\_Bus}} + V_{\text{DN2}} \quad (5)$$

where VD_{P1}, $V_{\text{VDD\_Bus}}$, V_{SCR3}, $V_{\text{VSS\_Bus}}$, and VD_{N2} are the voltage drops across D_{P1} embedded in SCR_1, VDD bus, SCR_3, VSS bus, and D_{N2} embedded in SCR_1, respectively. The other ESD current path in the cross-coupled-SCR ESD protection scheme under pin-to-pin ESD stresses is shown in Fig. 13b. The voltage drop ($V_{\text{Pin-to-Pin2}}$) along the pin-to-pin ESD current path is

$$V_{\text{Pin-}to\text{-Pin2}} = V_{\text{SCR1}} + V_{\text{SCR1-IN2}} \quad (6)$$

where V_{SCR1} and $V_{\text{SCR1-IN2}}$ are the voltage drops across SCR_1 and the metal line between SCR_1 and the RF IN_2 pad, respectively. As compared with (5), the voltage drop along the pin-to-pin ESD current path is substantially reduced. Moreover, the SCR paths between RF_{IN1} and RF_{IN2} may directly turn-on during ESD stress events. Thus, the pin-to-pin ESD robustness is significantly improved in differential LNA with the new proposed cross-coupled-SCR ESD protection scheme.

5. Conclusion

A new ESD protection scheme for differential input pads has been proposed and successfully verified in 130-nm CMOS process to protect the differential LNA. The proposed ESD protection scheme with the cross-coupled SCR is realized without adding any extra device, as compared with the conventional double-diode ESD protection scheme. Besides, the cross-coupled-SCR ESD protection scheme can significantly reduce the voltage drop along the ESD current path under the pin-to-pin ESD test, so the pin-to-pin ESD robustness can be improved. With the evolution of CMOS technology, the gate-oxide breakdown voltage becomes lower, which indicates that reducing the voltage drop along the ESD current path becomes more important for ESD protection design in advanced nanoscale CMOS processes. To achieve good RF performance and high ESD robustness simultaneously, the proposed ESD protection scheme in this work can be well co-designed with the differential LNA.

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