Chapter 3

NiSi contacted p^+n shallow junction

3.1 Introduction

As device dimension is scaled down to deep submicron, not only the size of gate electrode is shrunk, but also the vertical dimension of doped source/drain regions must be scaled to avoid device punchthrough and short channel effects [1]. In the past, pn junctions are used to be formed by dopant ion implantation into Si substrate followed by high temperature furnace annealing for dopant activation and implantation damage annihilation. However, channeling effect and high temperature dopant diffusion limit the formation of shallow junction. This is particularly important for the p^+n junction because boron is a light element and diffuses fast in silicon. In recent years, many advanced junction formation techniques have been studied using low energy ion implantation, low temperature annealing, and rapid thermal annealing process. These new methods are briefly reviewed as follows.

(1) Pre-amorphization of silicon substrate before dopant implantation

Pre-amorphization has been widely used to control the channeling behavior of implanted dopant atoms. After the pre-amorphization of the silicon substrate surface layer, dopant implantation was performed followed by crystal regrowth and annealing

process for the junction formation. Many heavy atoms have been used as pre-amorphization species, such as Si [2] and Ge [3-4]. Solid phase epitaxial (SPE) scheme can be used to regrow the crystal from the amorphous layer at a temperature as low as 550^{o}C [5]. The growth rate depends on the element used for pre-amorphization as well as the dopant implanted following the pre-amorphization. A careful annealing process is needed to annihilate the massive defects and dislocation induced by the pre-amorphization.

(2) Elevated source/drain structure

This method is to raise the source/drain regions by depositing a polysilicon (poly-Si) or amorphous silicon (α-Si) film or growing a selective epitaxial Si or SiGe layer [6-7]. Deposition of poly-Si/α-Si film on the source/drain regions needs an additional lithographic step to define the elevated regions, while the selective epitaxial growth of silicon on the source/drain regions does not need such an additional lithographic step. The elevated source/drain regions made with selective epitaxial growth (SEG) provide a sacrificial layer for silicide formation and an alternative approach for the SADS process. However, the SEG scheme needs a high deposition temperature to obtain good crystallinity in the epitaxial layer. The fact that high temperature process deteriorates the device performance is the main disadvantage of this method [8].

(3) Low energy ion implantation [9-11]

This is an extension of the conventional ion implantation technique. The implantation energy is lower than 1 keV and the implantation dose is typically from 1×10^{14} to 5×10^{14} cm^{-2}. The major disadvantage of this method is that no commercial implantation system of such a low energy beam line is available for high throughput mass production with reasonable cost.

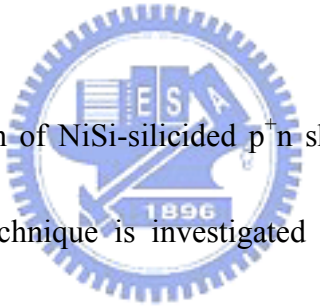
(4) Plasma immeration ion implantation (PIII) [12-15]

PIII, also called plasma doping (PD), has been considered as the most promising technique to obtain ultra shallow junction profile because of its high throughput, low machine cost, and room temperature operation. However, PD is still not a mature technique from the commercial perspective and a number of practical issues, such as dosimetry accuracy, glancing angle implantation underneath gate structures, and plasma–surface interactions, must still be considered.

(5) ITS/ITM technique

The implant through silicide (ITS) and implant through metal (ITM) processes have been investigated for shallow junction formation. The ITS/ITM process consists of implanting dopants into/through silicide or metal layer and the subsequent thermal annealing to form a silicide-contacted shallow junction [16-21]. The ITS scheme in

particular is of much benefit to the formation of shallow junction. This is because metal silicides have a larger nuclear stopping power than silicon for the implanted dopant ions and thus can reduce the channeling effect; in addition, the junction formed by the ITS scheme can be almost free of implant damage, which is mostly confined in the silicide layer. Thus, the post-implant annealing temperature can be lowered while shallow junctions with superb characteristics can be obtained. Moreover, the silicided junction is conformal to the silicide/silicon interface, and thus the possibility of junction penetration by the silicide is reduced.



In this chapter, formation of NiSi-silicided p^+n shallow junction using implant into/through silicide (ITS) technique is investigated with respect to various BF_2^+ implantaion conditions. Feasibility of low-temperature processing and high-temperature stability of the NiSi/p^+n junction are evaluated by analyzing the electrical characteristics and material properties of the silicided-junction.

3.2 Experimental procedures

3.2.1 Formation of NiSi/p^+n shallow junctions and characterization techniques

The NiSi/p^+n junction diodes were fabricated on n-type (100)-oriented silicon

wafers with 2.7~4 Ω-cm nominal resistivity. After standard RCA cleaning, a 5500-Å thick SiO_2 was thermally grown by pyrogenic oxidation at 1050°C. Active regions with areas of 1100×1100, 580×580, 270×270, and 120×120 μm^2 were defined by the photolithography technique followed by chemical wet etching. A nickel (Ni) film of 150 Å thickness was sputter deposited in a dc sputtering system with a base pressure of less than 2.5×10^{-8} torr, using a Ni target in Ar ambient at a pressure of 2×10^{-3} torr with a deposition rate of about 10 Å/sec. After the Ni film deposition, the samples were rapid thermal annealed (RTA) at 500°C for 30 sec in a N_2 ambient to form nickel monosilicide (NiSi). The unreacted Ni film was selectively etched using a solution of H_2SO_4:H_2O_2=3:1 at 75~85°C. The NiSi film formed was about 310 Å in thickness as determined by cross-sectional TEM analysis. The p^+n junction diodes were formed by BF_2^+ implantation into/through the NiSi silicide at an energy of 20-35 keV to a dose of 2×10^{15} or 5×10^{15} cm^{-2}, followed by furnace annealing at temperatures ranging from 550 to 800°C in N_2 ambient for 30 min or by a 30 sec RTA at temperatures ranging from 600 to 800°C in N_2 ambient. The determination of the BF_2^+ implantation conditions was based on the results of TRIM simulation presented in the following section. Finally, a 5000-Å-thick Al layer was deposited on the backside of Si substrate for all samples for a better contact in electrical measurements.

The thicknesses of the as-deposited Ni film and the NiSi film formed were

determined by cross-sectional TEM observation. Sheet resistance was measured by four-point probe on the unpatterned area. The p^+n junction depth was determined by spreading resistance profiling (SRP) measurement. Surface morphology was observed by scanning electron microscopy (SEM). Secondary ion mass spectrometry (SIMS) was used to determine the elemental concentration profiles. The current-voltage (I-V) characteristics of the NiSi/p^+n junction diodes were measured by a semiconductor parameter analyzer HP-4145B. The open circuit leakage current of the measuring system was kept below 0.5 pA. The forward bias from 0 to 1 V at a step of 0.01 V and the reverse bias from 0 to -5 V at a step of 0.05 V were used for the I-V characteristics measurement. Temperature dependence of the reverse junction current was measured from room temperature to 200^oC on a thermal vacuum chunk.

3.2.2 Four-terminal Kelvin test structure for NiSi/p^+n contact resistance measurement

The four-terminal Kelvin method was used for the determination of contact resistivity for the NiSi/p^+-Si contact studied in this work [22]. Figure 3-1 and Fig. 3-2 shows the top view and cross sectional view of the mask layout, respectively, for the Kelvin contact resistance test pattern used in this work, while Fig. 3-3 shows the process flow of fabricating the Kelvin structure for the NiSi/p^+n contact resistance measurements. The Kelvin contact resistance test pattern was constructed on n-type,

(100)-oriented silicon wafers with 1~2 Ω-cm nominal resistivity for the P^+-contact. After initial standard wafer cleaning, a 5500-Å-thick SiO_2 was thermally grown by pyrogenic oxidation at 1050°C [Fig. 3-3(a)]. The active regions were defined by the photolithography method followed by the chemical wet etching [Fig. 3-3(b)]. To dope the active regions, a thin protective SiO_2 (screen oxide) of 200 Å thickness was thermally grown in the active regions [Fig. 3-3(c)]. This was followed by a BF_2^+ implantation at 30 keV to a dose of 2×10^{14} cm^{-2} [Fig. 3-3(d)]. The implanted dopant was then thermally annealed at 900°C for 30 min for dopant activation [Fig. 3-3(e)]. PECVD oxide was deposited to a thickness of 4000 Å, which is to be patterned and used as a subsequent P^+ implantation mask [Fig. 3-3(f)]. The contact regions were defined by the photolithography method followed by the reactive ion and chemical wet etching [Fig. 3-3(g)]. A nickel (Ni) film of 150-Å thickness was sputter deposited in a dc sputtering system with a base pressure of less than 2.5×10^{-8} torr, using a Ni target in Ar ambient at a pressure of 2×10^{-3} torr with a deposition rate of about 10-Å/sec [Fig. 3-3(h)]. After the Ni film deposition, the samples were rapid thermal annealed (RTA) at 500°C for 30 sec in a N_2 ambient to form nickel monosilicide (NiSi). The unreacted Ni film was selectively etched using a solution of H_2SO_4:H_2O_2=3:1 at 75~85°C [Fig. 3-3(i)]. The NiSi film formed was about 310 Å in thickness as determined by cross-sectional TEM analysis. The P^+ layer in the contact

regions was formed by BF_2^+ implantation at 20 and 35 keV to a dose of 5×10^{15} cm^{-2}, followed by a 30 sec RTA at temperatures from 650 to 800°C in a N_2 ambient [Fig. 3-3(j)]. The contact resistance test structure was completed by depositing a multilayer metal of Ti(400 Å)/TiN(1000 Å)/Al(9000 Å)/TiN(400 Å), for the prevention of aluminum oxidation, followed by the contact metal patterning using the third mask [Fig. 3-3(k)].

The contact resistance (Rc) was determined directly by dividing the measured terminal voltage V_{12} by the driving current I_{34} (as shown in Fig. 3-2). The subscript denotes the pads that the voltage was sensed and the pads that the driving current was forced. The driving current ranging from 0.1 to 1 mA was used for different samples to make sure the linearity of the measured I-V characteristic. Four rectangular contact areas (Ac) were designed in the mask set: 2×2, 3×3, 5×5, and 10×10 μm^2. The value of the contact resistivity (ρ_c) was calculated by Ac×Rc

3.3 TRIM simulation

Before making the BF_2^+ implantation, the as-implanted dopant distributions in NiSi film and Si substrate were predicted by TRIM (transport of ions in matter) simulation. For BF_2^+ ion implantation, the BF_2^+ ions are believed to be dissociated upon their first atomic scattering. Therefore, the boron energy is obtained by

multiplying the BF_2^+ energy by the mass ratio of B^+ to BF_2^+, which is 11/49. In this work, boron ions are to be implanted into a sample which is composed of a 310-Å-thick NiSi film and an underlying Si substrate. Figure 3-4 shows the as-implanted boron profiles obtained by TRIM simulation for BF_2^+ implantation at various energies to a dose of 5×10^{15} cm^{-2}. For the 20 keV implantation, nearly all implanted boron ions are located inside the silicide layer. In this case, the silicide film serves as a diffusion source of boron for the p^+n junction formation during the subsequent thermal annealing process. Boron in the silicide layer has to diffuse into the silicon substrate and become electrically active to form a good junction. Since boron can be electrically activated at a temperature as low as 550°C [5], using NiSi as a boron diffusion source is possible at low processing temperature provided that sufficient amount of boron atoms are diffused into the Si substrate. For the 25, 30, and 35 keV implantations to a dose of 5×10^{15} cm^{-2}, the boron concentrations at the NiSi/Si interface are all higher than 1×10^{20} cm^{-3}, while all projection ranges are kept within the silicide layer. These interface boron concentrations are high enough to form a good silicided p^+n junction provided that sufficient amount of dopants are electrically activated and most of the implantation damage can be annealed out.

3.4 Results and discussion

3.4.1 NiSi/p^+n junctions formed by furnace annealing (FA)

[A] Material characterization

The sheet resistance, SIMS depth profiles measurements, and surface morphology for the BF_2^+ implanted NiSi/Si samples with a post-implant furnace annealing are already presented and discussed in section 2.3.1.1 (sheet resistance and SIMS depth profiles) and 2.3.1.2 (surface morphology), respectively, in chapter 2. It was found that the incorporation of fluorine atoms in the NiSi film can promote the thermal stability of NiSi film and retard the formation of $NiSi_2$ silicide phase.

[B] Junction depth

Spreading resistance profiling (SRP) measurement was used to determine the junction depth in this work using an SSM-150 SRP system. All samples prepared for SRP measurements were first capped with a 3000Å PECVD oxide, and then were polished to a small beveling angle of 17' for better resolution. Since the p-type dopant concentration would compensate the n-type substrate dopant concentration at the location of a p^+n junction, resulting in a maximum value of measured spreading resistance, the location of a p^+n junction is defined as the position where the measured spreading resistance is a maximum. Table 3.1 lists the junction depths measured from the silicide/silicon interface, for the NiSi/p^+n samples studied in this work. For the

sample processed with BF_2^+ implantation at 20 keV, the junction depth was determined to be about 25 nm after a 650°C/30 min thermal annealing. Since nearly all implanted boron ions are confined in the silicide film for the BF_2^+ implantation at 20 keV, the junction must be formed by the diffusion of boron from the silicide during the thermal annealing process. Although the diffusivity of boron in silicon is negligibly small at 550°C [19], it is presumed that the diffusivity of boron in silicon in the case of this study could be enhanced by the presence of silicide film [23]. The enhancement in diffusivity is attributable to the vacancy injection from the silicide. For the implantation at higher energies (25, 30, and 35 keV), the implantation damage in silicon may also play a role for boron diffusion, resulting in deeper junctions. Higher implantation energy and higher annealing temperature resulted in an even deeper junction.

[C] Electrical characteristics

The electrical properties of the silicide-contacted p^+n shallow junction diodes fabricated by the ITS scheme are dependent on a number of factors, including the dopant activation level, implantation damage recovery, silicide/silicon interface roughness, and the distance between the silicide/silicon interface to the junction position. All of these are closely related to the energy and dosage of the dopant ion

implantation as well as the dopant activation ability and the drive-in diffusion during the subsequent annealing process; this is especially important for the case of low thermal budget and low-energy implantation for the ITS scheme. All measurements in this study were performed at room temperature, and each data point was obtained by averaging the data measured from six randomly chosen samples.

(a) Forward ideality factor

The forward ideality factor η of a junction diode can be extracted from the basic I-V relation

$$I=Is[\exp(qV/\eta kT)-1]$$

where Is is the reverse saturation current, q is the electronic charge, k is the Boltzmann constant, and T is the temperature at measurement. An ideality factor of unity indicates that diffusion current predominates while a factor of 2 indicates that depletion recombination current is dominant. The ideality factor η can be determined from the slope of the linear segment of the I-V curve plotted on semilogarithmic coordinates. Figure 3-5 shows the ideality factor versus annealing temperature for the NiSi/p^+n junction diodes fabricated with BF_2^+ implantation at various energies to a dose of 5×10^{15} cm^{-2}. All ideality factors are below 1.06 for the samples annealed at and below a temperature of 750°C. The data in Fig.3-2 indicates that a 30 min low

temperature (600-700°C) annealing is capable of incorporating sufficient amount of activated boron atoms in Si substrate as well as recovering the implantation damage to obtain a good NiSi/p^+n shallow junction with an ideality factor below 1.04.

(b) Reverse bias current

Figure 3-6 shows the reverse bias current density (J_R) versus annealing temperature for the NiSi/p^+n junction diodes with an area of 0.0121 cm^2 (1100 μm×1100 μm) measured at a reverse bias of –5 V. The J_R is determined by directly dividing the measured current by the diode's area. Roughness of the silicide/Si interface in a shallow junction may lead to the formation of localized Schottky contacts or the agglomeration-induced local silicide spiking, resulting in the increase of reverse bias current. For the lower dose (2×10^{15} cm^{-2}) implanted samples, J_R of less than 2 nA/cm^2 was easily achieved for the samples fabricated with a BF_2^+ implantation at 25 to 35 keV followed by a thermal annealing at 550 to 700°C. For the samples annealed at 750°C, the 25 and 30 keV implanted samples exhibited drastic increase in reverse bias leakage current, while the 35keV implanted sample revealed only a slight increase in leakage current. This increase in reverse bias leakage current is consistent with the behavior of the sample's sheet resistance (Rs), which in turn is related to the extent of agglomeration of the NiSi film. The agglomeration of the NiSi

film will induce roughness of the silicide/Si interface, leading to the penetration of silicide through the shallow junction and thus the degradation of the junction characteristics. The shallower the junction is, the easier the junction is susceptible to the silicide/Si interface roughness. Thus, the J_R and the thermal stability of the p^+n junction fabricated with BF_2^+ implantation at 35 keV are better than those of the shallower junctions fabricated with BF_2^+ implantation at 25 and 30 keV. With the annealing temperature raised to 800°C, all samples exhibited an even higher reverse bias leakage current. This is attributed to the formation of $NiSi_2$ silicide phase, the increased volume of which decreased the distance between the silicide and the junction position, leading to easier formation of localized Schottky contacts and thus the increase of reverse bias current. Moreover, since $NiSi_2$ is formed via nucleation controlled mechanism which induces a corrugated silicide/Si interface due to random nucleation on the original interface, large reverse bias current can be easily induced for shallow silicided-junction [24-25]. As for the NiSi/p^+n samples fabricated with a higher dose (5×10^{15} cm^{-2}) BF_2^+ implantation, the J_R of less than 2 nA/cm^2 can be easily achieved with a post-implant thermal annealing at temperatures of 550 to 750°C. With a higher dose of BF_2^+ implantation, the p^+n junction formed will become deeper and a larger amount of fluorine atoms will be incorporated in the NiSi film, improving the thermal stability of the thin NiSi film [26-27]. With the annealing temperature

raised to 800°C, formation of $NiSi_2$ phase started to occur, resulting in a drastic increase in reverse bias leakage current, similar to those observed in the samples fabricated with a lower dose (2×10^{15} cm^{-2}) of BF_2^+ implantation.

(c) Activation energy measurement

The temperature dependence of reverse bias junction current can provide insight into the junction leakage mechanism. The temperature dependence of reverse current I_R is given by

$$I_R \propto T^3 \exp(-E_a/kT)$$

where Ea is the activation energy of the junction, k is the Boltzmann constant, and T is the temperature at measurement. The value of Ea is close to the bandgap of silicon Eg when the reverse current is dominated by the diffusion current and will be close to Eg/2 when the reverse current is dominated by the generation current. Figure 3-7 shows the Arrhenius plots of the reverse current I_R for the NiSi(310 Å)/p^+n samples fabricated with various implantation and annealing conditions. The measurement was conducted at 1 V reverse bias. The activation energy was found to be close to the silicon bandgap of 1.12 eV for all samples investigated. This result clearly indicates that the reverse current was dominated by the minority carrier diffusion current at temperatures from 40 to 200°C.

(d) Area and peripheral current

The reverse bias leakage current (I_R) of a p^+n or n^+p junction consists of the reverse area leakage current (I_{RA}) and the reverse peripheral leakage current (I_{RP}):

$$\mathbf{I_R=I_{RA}+I_{RP}=A\times J_{RA}+P\times J_{RP}}$$

where A is the junction area, P is the length of junction perimeter, J_{RA} is the junction area leakage current density, and J_{RP} is the junction peripheral leakage current density. A simple arrangement gives

$$\mathbf{J'_R=J_{RA}+J_{RP}(P/A)}$$

where $J'_R=I_R/A$. Thus, by measuring the I_R of junctions with different P/A ratio, the slope of J_R' versus P/A plot gives the J_{RP} and the Y-axis intersection gives the J_{RA} Figure 3-8 shows the J'_R vs. P/A plot for the NiSi/p^+n junctions fabricated with BF_2^+ implantation at 20 keV to a dose of 5×10^{15} cm^{-2} followed by thermal annealing at temperatures from 550 to 750°C. It is found that the J_{RA} decreases from 1.38 to 0.657 nA/cm^2 and the J_{RP} increases from 15.9 to 42.8 pA/cm as the annealing temperature was increased from 550 to 750°C. For the junction diode with a size of $1100\times1100\mu m^2$ formed by annealing at 700°C, the J_{RA} is 0.79 nA/cm^2 and the J_{RP} is 46.6 pA/cm, and the corresponding area and peripheral current are 9.5 and 20.5 pA, respectively. This indicates that more than 68% of the total reverse current leaks through the junction's perimeter. For a smaller junction with an area of 120×120 μm^2,

the peripheral component accounts for 95% of the total reverse current, indicating the major role of the peripheral leakage component. Presumably, most of the implanted defects were confined within the silicide layer; thus, very few extended defects are located beyond the silicide layer and the impact of these defects is minimal on the junction leakage. However, the peripheral leakage is sensitive to the interfacial behavior of Si/SiO_2 along the junction perimeter because the junctions formed in this study are all surrounded by field oxide. It is notable that the distance from the silicide/Si interface to the junction at the diodes perimeter will be much shorter than that at the diodes bottom area after the post implant thermal annealing. Moreover, the mechanical stress induced defects along the diodes perimeter will presumably cause a higher peripheral leakage [28]. Thus, the junction characteristics will be very sensitive to the silicide/Si interface property and the reverse junction current will be dominated by the silicide induced current along the periphery. Figure 3-9 illustrates a typical I-V characteristic for the NiSi(310 Å)/p^+n junction fabricated by BF_2^+ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by a 700°C thermal annealing for 30 min. It is clear that NiSi can serve as an efficient diffusion source for boron diffusion during the low-temperature thermal annealing, resulting in the formation of NiSi/p^+n shallow junction with excellent electrical characteristics.

3.4.2 NiSi/p^+n junctions formed by RTA

[A] Material characterization

The sheet resistance and surface morphology for the BF_2^+ implanted NiSi/Si samples with a post-implant RTA process are already presented and discussed in sections 2.3.2.1 and 2.3.2.2, respectively, in chapter 2. It was confirmed one again that the incorporation of fluorine atoms in the NiSi film can promote the thermal stability of NiSi film and retard the formation of $NiSi_2$ silicide phase.

[B] Junction depth

Table 3.2 lists the junction depths measured from the silicide/Si interface for the 20 and 35 keV implanted samples. For the sample implanted with BF_2^+ at 20 keV followed by RTA at 650°C, the junction depth was determined to be 24 nm. For the implantation at 35 keV, a deeper junction of 56 nm was attained after RTA at 800°C. Higher implantation energy and higher annealing temperature resulted in deeper junction. The junction depth of the RTA samples is shallower than that of the corresponding furnace annealed samples (Table 3.1), particularly for those implanted at higher energy of 35keV.

[C] Electrical characteristics

Rapid thermal annealing (RTA) process can reduce the dopant diffusion, promote the activation of dopant, and annihilate the implantation damage efficiently, as compared to the furnace annealing (FA) process [29-30]. In this work, each data point was obtained by averaging the data measured from six randomly chosen samples.

(a) Forward ideality factor

Figure 3-10 shows the ideality factor versus RTA temperature for the NiSi/p^+n junction diodes fabricated with BF_2^+ implantation at various energies to a dose of 5×10^{15} cm^{-2}. The large ideality factor for the samples annealed at 600^{o}C indicates that the RTA at 600^{o}C was not adequate to form a good junction. With RTA at 650 to 750^{o}C, the ideality factor below 1.05 was obtained for all samples. This indicates that a 30 sec RTA at 650 to 750^{o}C is capable of incorporating sufficient amount of activated boron atoms in Si substrate as well as recovering the implantation damage to obtain a good NiSi/p^+n shallow junction.

(b) Reverse bias current

Figure 3-11 shows the reverse bias current density (J_R) versus RTA

temperature for the NiSi/p^+n junction diodes with an area of 580×580 μm^2 measured at a reverse bias of –5 V. The J_R is determined by directly dividing the measured current by the diode's area. The RTA at 600°C was apparently not adequate to form a good junction, presumably due to insufficient dopant concentration in Si substrate, low level dopant activation and implantation damage recovery. With the RTA temperature raised to 650°C, the reverse bias current density was significantly reduced. Notably, the 35 keV implanted samples exhibit the lowest reverse current density because they have a deeper junction than the other samples which were implanted at lower energies. In fact, J_R of less than 4 nA/cm^2 can be easily achieved for the NiSi/p^+n junctions fabricated with the implantation conditions employed in this work followed by RTA annealing at temperatures ranging from 650 to 800°C. Figure 3-12 illustrates a typical I-V characteristic for the NiSi(310 Å)/p^+n junctions fabricated by BF_2^+ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by RTA at 650°C. The reverse current density at -5 V is equivalent to about 0.6 nA/cm^{-2} and the forward ideality factor is very close to unity. It is clear that NiSi can serve as an efficient diffusion source for boron diffusion during the low temperature RTA, resulting in the formation of NiSi/p^+n shallow junction with excellent electrical characteristics.

(c) Activation energy measurement

Figure 3-13 shows the Arrhenius plots of reverse current I_R for the NiSi(310 Å)/p^+n samples (with an area of 580×580 μm^2) fabricated by BF_2^+ implantation at 20 and 35 keV to a dose of 5×10^{15} cm^{-2} followed by RTA at various temperatures. The measurement was conducted at 1 V reverse bias. The activation energy was found to be very close to the silicon bandgap of 1.12 eV for all samples investigated. Figure 3-14 shows the Arrhenius plots of reverse current I_R for the NiSi(310 Å)/p^+n junction diodes of different areas fabricated by BF_2^+ implantation at 35 keV followed by RTA at 750°C. For the two larger junction diodes (with junction areas of 580×580 and 270×270 μm^2), Ea of 1.05 eV indicates that the reverse current is dominated by the minority carrier diffusion current. However, the reverse current of the small junction diode (with junction area of 120×120 μm^2) exhibits a different behavior; at temperatures above 80°C, I_R is still dominated by the minority carrier diffusion current, whereas I_R tends to be dominated by the minority carrier generation current at temperatures below 80°C because of the Ea value of 0.81 eV. With the scale down of junction area, the reverse junction current will be increasingly dominated by the junction peripheral current, which may exhibit behavior different from the junction area current.

(d) Area and peripheral current

Figure 3-15 shows the J'_R vs. P/A plot for the NiSi(310 Å)/p^+n junctions fabricated with BF_2^+ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by RTA at temperatures from 650 to 750°C. It was found that the J_{RA} decreases from 0.445 to 0.325 nA/cm^2 and the J_{RP} increases from 3.96 to 16.6 pA/cm as the annealing RTA temperature was increased from 650 to 750°C. For the junction diode with a size of 580×580 μm^2 formed by annealing at 750°C, the J_{RA} is 0.325 nA/cm^2 and the J_{RP} is 16.6 pA/cm, and the corresponding area and peripheral current are 1.09 and 3.85 pA, respectively, indicating that 78% of the total reverse current leaks through the junction's perimeter. For a smaller junction with an area of 120×120 μm^2, the peripheral component accounts for 94% of the total reverse current, indicating the major role of the peripheral leakage component. Figure 3-16 shows the Arrhenius plots of J_{RA} and J_{RP} for the 35-keV-implanted and 750°C-annealed NiSi(310 Å)/p^+n junction diode. In the entire temperature range from 40 to 200°C, the value of Ea for the J_{RA} indicates that the reverse area current was dominated by the minority carrier diffusion current. This also implies that the 30 sec RTA at 750°C efficiently activated the implanted boron dopant and eliminated the implantation induced damage in the diode's flat bottom area. However, the value of Ea for the J_{RP} shows a different behavior; it is 1.11 eV at temperatures above 80°C, while it is 0.71 eV at temperatures

below 80°C. This indicates that the reverse peripheral current was dominated by the minority carrier generation current at low temperatures (including room temperature). The implication is the presence of generation centers in and/or close to the junction region along the perimeter. As discussed earlier, the junction formed in this study are all surrounded by field oxide, and the interfacial behavior of Si/SiO_2 along the junction perimeter can dominate the reverse current. The J_{RP} and the I_R of junctions with smaller areas are easily dominated by the generation current, particularly at low temperatures.

[D] Contact resistivity of NiSi/p$^+$n shallow junction

Fig. 3-17 shows the measured contact resistance (Rc) versus contact area (Ac) for the NiSi/p$^+$n contact formed by ITS scheme with BF_2^+ implantation at 20 keV to a dose of 5×10^{15} cm^{-2} followed by RTA at various temperatures. It can be seen that the variation of contact resistance is linearly inverse with the contact area. The corresponding contact resistivity ρ_c is illustrated in Fig. 3-18 as a function of the RTA temperature. Similarly, Fig. 3-19 shows the contact resistivity ρ_c for the NiSi/p$^+$n contact formed by BF_2^+ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by RTA at various temperatures. The ρ_c for the NiSi/p$^+$n contacts formed with 35 keV BF_2^+ implantation is lower than that for the NiSi/p$^+$n contacts formed with 20 keV

BF_2^+ implantation by a factor of 2 to 5 except the contacts formed at 800°C RTA. For the 20 keV implantation, nearly all implanted boron ions are located inside the silicide layer. In this case, the silicide film serves as a diffusion source for the out-diffusion of boron into the Si substrate during the subsequent RTA process. For the 35 keV implantation, the deeper profile of implanted boron in NiSi/Si, as estimated by the TRIM simulation (Fig. 3-4), shows that the boron concentration at the NiSi/Si interface is about 5×10^{20} cm^{-3}, and that the peak concentration of boron in NiSi is located much closer to the NiSi/Si interface than that in the 20 keV implanted sample. During the RTA process (650 to 750°C), the implanted boron atoms were diffused into Si substrate as well as electrically activated. It is believed that the boron concentration at the Si surface in the 35 keV implanted sample would be higher than that in the 20 keV implanted sample, resulting in lower contact resistivity. For the sample annealed at 800°C, comparable value of ρ_c were obtained for the 20 and 35 keV implanted samples. However, more effort is needed to clarify the observed phenomena that an increase of ρ_c was observed for the 35 keV implanted samples with RTA at 800°C (Fig. 3-19), while this was not observed for the 20 keV implanted samples (Fig. 3-18).

3.5 Conclusion

The formation and characterization of the NiSi-contacted p^+n shallow junctions fabricated using BF_2^+ implantation into/through thin NiSi silicide layer (ITS scheme) followed by low temperature FA (furnace annealing) and RTA process were investigated separately in this chapter.

For the furnace-annealed NiSi/p^+n junction diodes fabricated in this work, the junction depth ranges from 23 to 70 nm measured from the NiSi/Si interface, and the reverse bias current density of less than 2 nA/cm^2 can be easily achieved. Specifically, the NiSi(310 Å)/p^+n junction fabricated with a 35 keV BF_2^+ implantation to a dose of 5×10^{15} cm^{-2} followed by a 30-min-FA at 600^{o}C, has a forward ideality factor of 1.01, a reverse bias current density (at −5 V) of less than 1 nA/cm^2, and a junction depth of 56 nm. The activation energy measurements indicate that the reverse bias current of the NiSi/p^+n junctions with an area of 1100×1100 μm^2 is dominated by the diffusion current. The reverse bias current is composed of the reverse area leakage current and the reverse peripheral leakage current. For the diode's size smaller than 120×120 μm^2, the total reverse current would be contributed by the peripheral current dominated by the minority carrier generation current induced by the generation centers in and/or close to the junction region along the perimeter.

For the NiSi/p^+n junction diodes fabricated in this work using RTA process, the junction depth ranges from 23 to 56 nm measured from the NiSi/Si interface, and the reverse bias current density of lower than 4 nA/cm^2 can be easily achieved. Specifically, the NiSi(310 Å)/p^+n junction fabricated with BF_2^+ implantation at 35 keV to a dose of $5\times10^{15}cm^{-2}$ followed by a 30-sec-RTA at 650°C, has a forward ideality factor of 1.001, a reverse bias current density (at –5 V) of 0.6 nA/cm^2, and a junction depth of 37 nm. The activation energy measurements indicate that the reverse peripheral leakage current (I_{RP}) is dominated by the minority carrier generation current, while the reverse area leakage current (I_{RA}) is dominated by the diffusion current. For the diode's size smaller than 120×120 μm^2, the total reverse current would be dominated by the minority carrier generation current induced by the generation centers in and/or close to the junction region along the perimeter. The contact resistivity of the NiSi/p^+n contact fabricated with BF_2^+ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by RTA at 750°C, was determined to be about 5×10^{-8} Ω-cm^2.

In view of junction formation, nickel monosilicide NiSi is found to be suitable for the present IC processing temperature and low thermal budget, which is the trend for the future process development. NiSi is believed to be a promising silicide material for the salicide process.

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Table 3.1 Junction depths (in unit of nm) of NiSi(310Å)/p^+n junctions formed by ITS scheme with BF_2^+ implantation at various energies to a dose of $5\times10^{15}cm^{-2}$ followed by a 30 min thermal annealing.

Annealing Temperature	**Implantation Energy**			
(30 min in N_2 ambient)	20keV	25keV	30keV	35keV
600°C	23	24	40	56
650°C	25	36	45	60
700°C	28	40	49	65
750°C	35	45	59	70

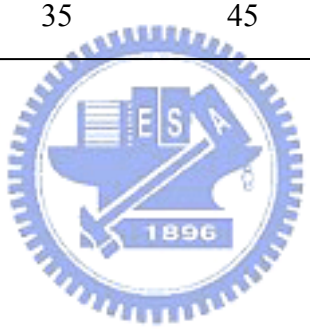


Table 3.2 Junction depths (in unit of nm) of NiSi(310Å)/p^+n junctions formed by ITS scheme with BF_2^+ implantation to a dose of $5\times10^{15}cm^{-2}$ followed by a 30 sec RTA.

RTA	**Implantation Energy**	
Temperature	20keV	35keV
600°C	22	33
650°C	24	37
700°C	27	41
750°C	33	45
800°C	37	56

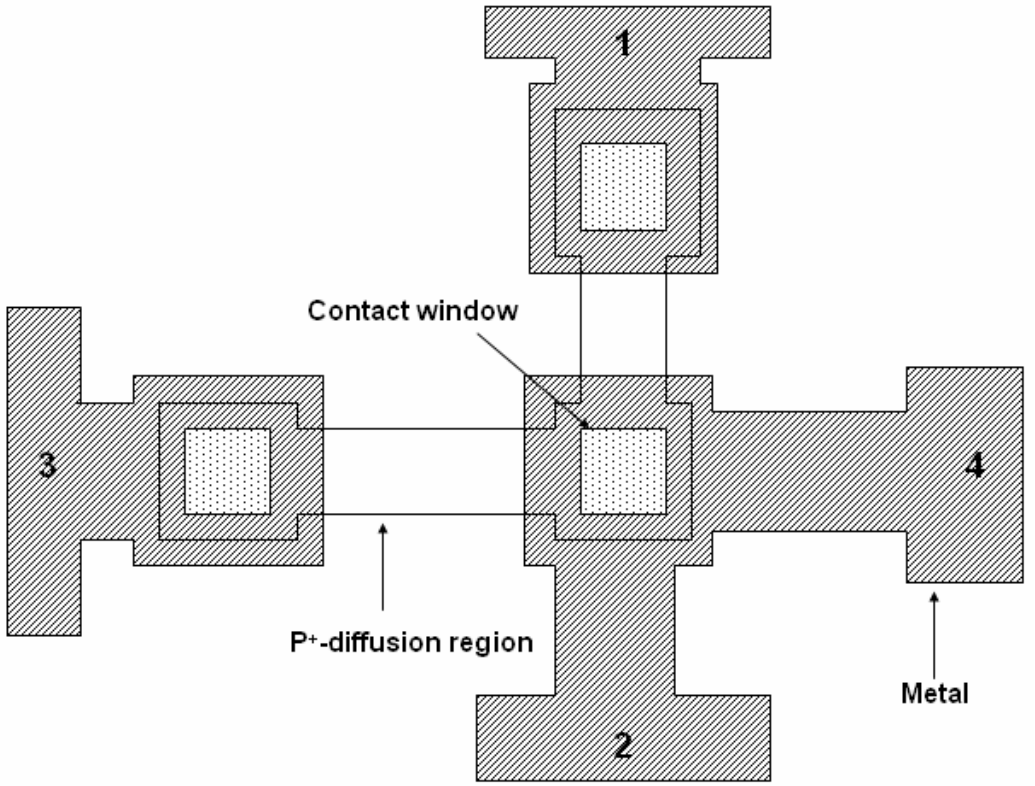


Fig. 3-1 Schematic illustration of the Kelvin contact resistance test pattern.

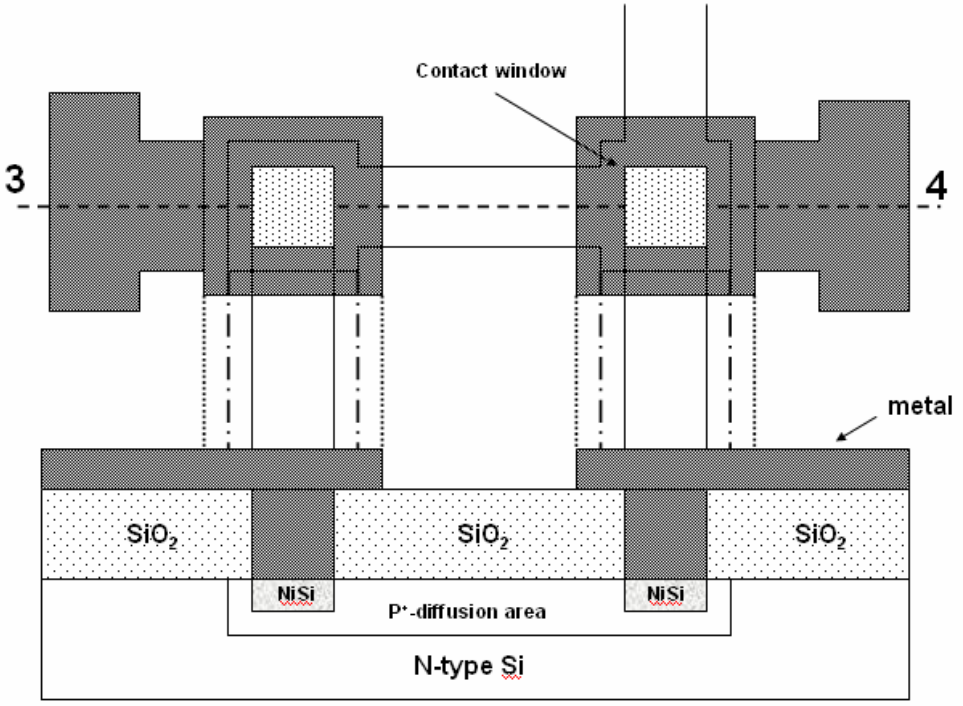
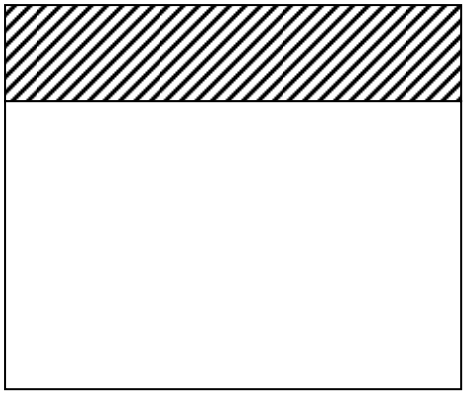


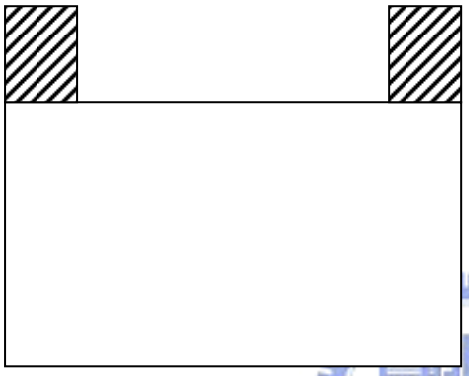
Fig. 3-2 Cross sectional view of the Kelvin contact resistance test pattern of Fig. 3-1 along line 3-4.

(a)

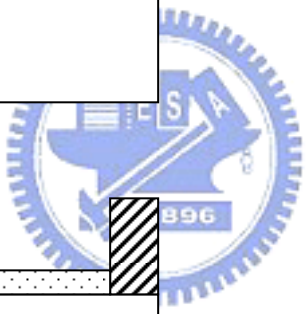


- **RCA clean**
- **Field oxide growth (5000 Å)**

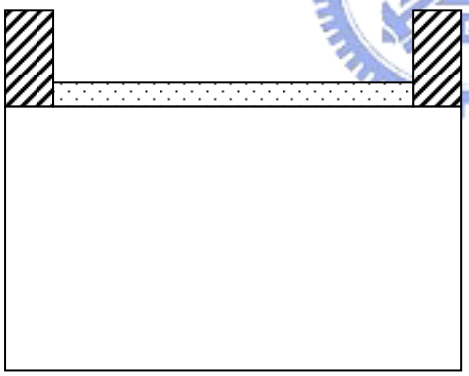
(b)



- **Active region definition (mask #1)**

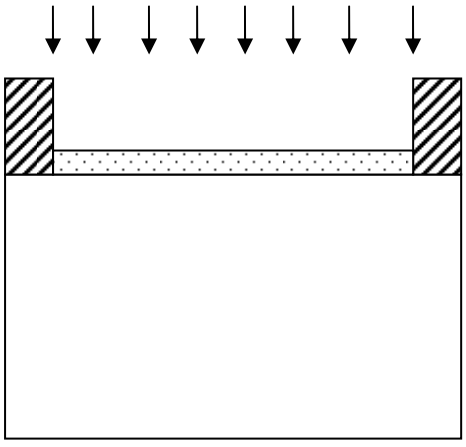


(c)



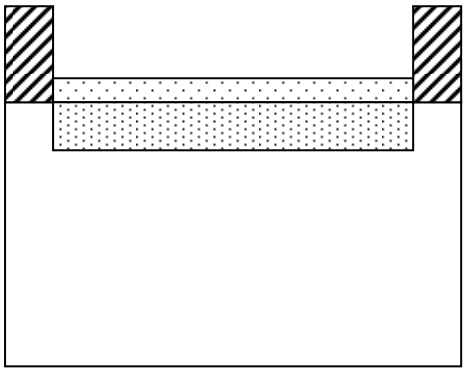
- **Screen oxide growth (200 Å)**

(d)



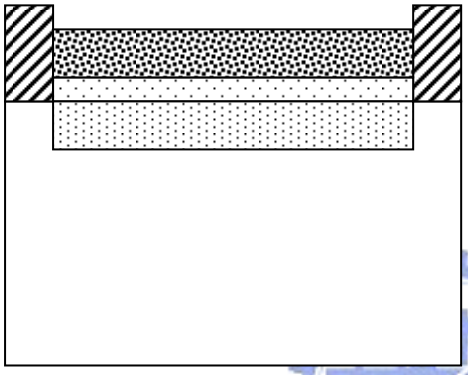
- **Channel dopant implantation (BF_2^+:30keV/5×$10^{14}cm^{-2}$)**

(e)



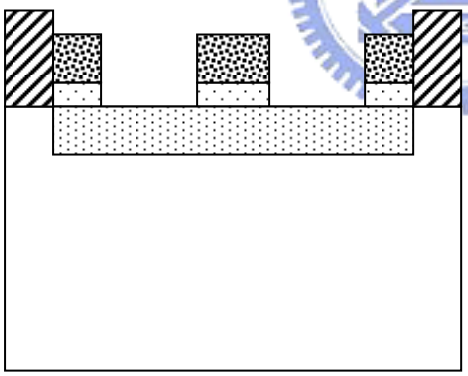
● Channel dopant activation
(900°C/30min thermal anneal)

(f)



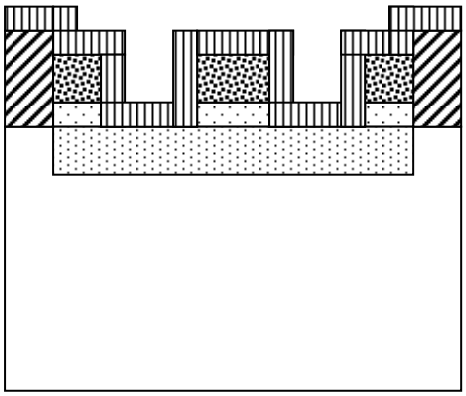
● 4000-Å PECVD SiO_2 deposition

(g)



● contact region definition
(mask#2)

(h)



● Ni film (150 Å) deposition
by sputtering

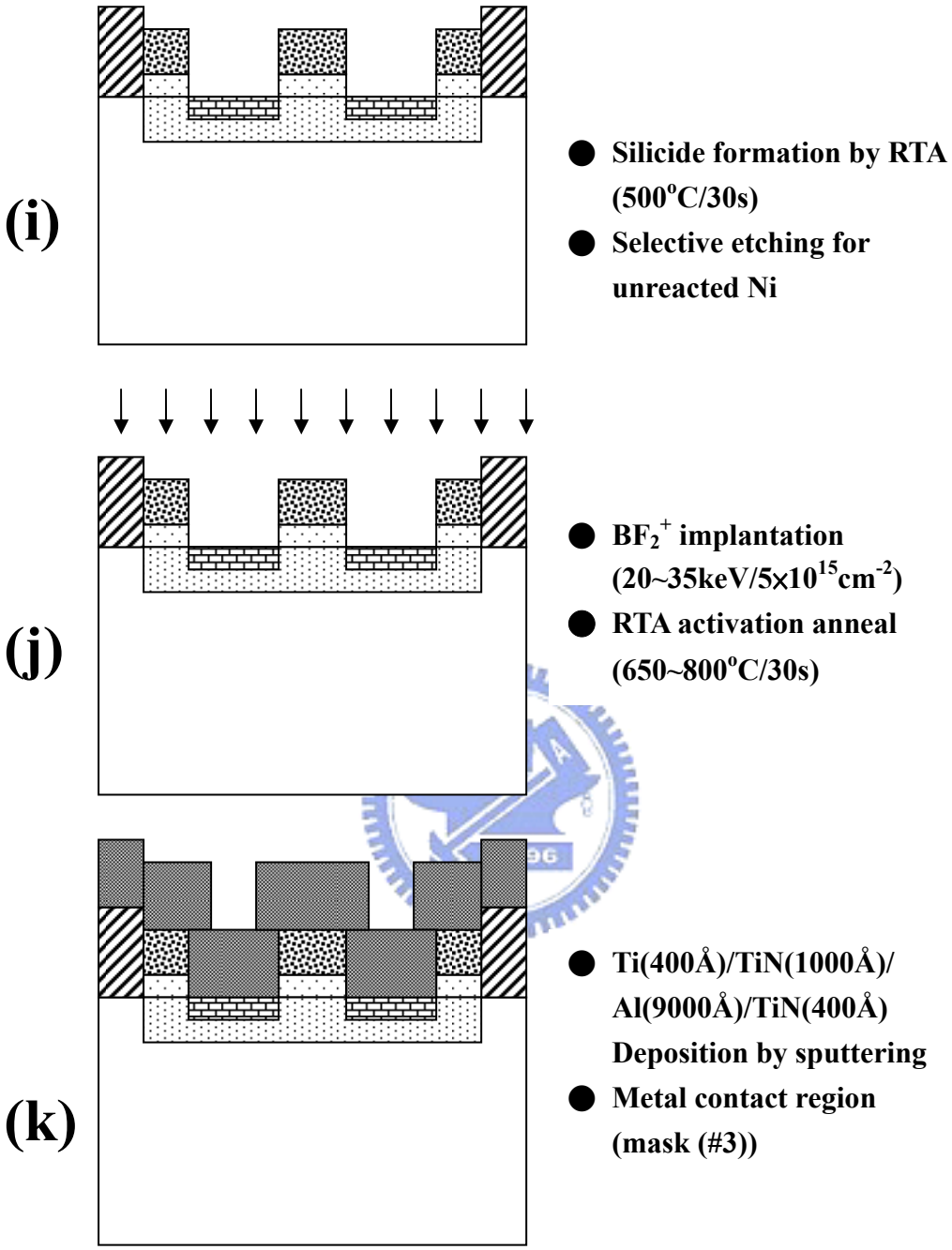


Fig. 3-3 Process flow of fabricating the Kelvin structure for NiSi/p^+n contact resistance measurements.

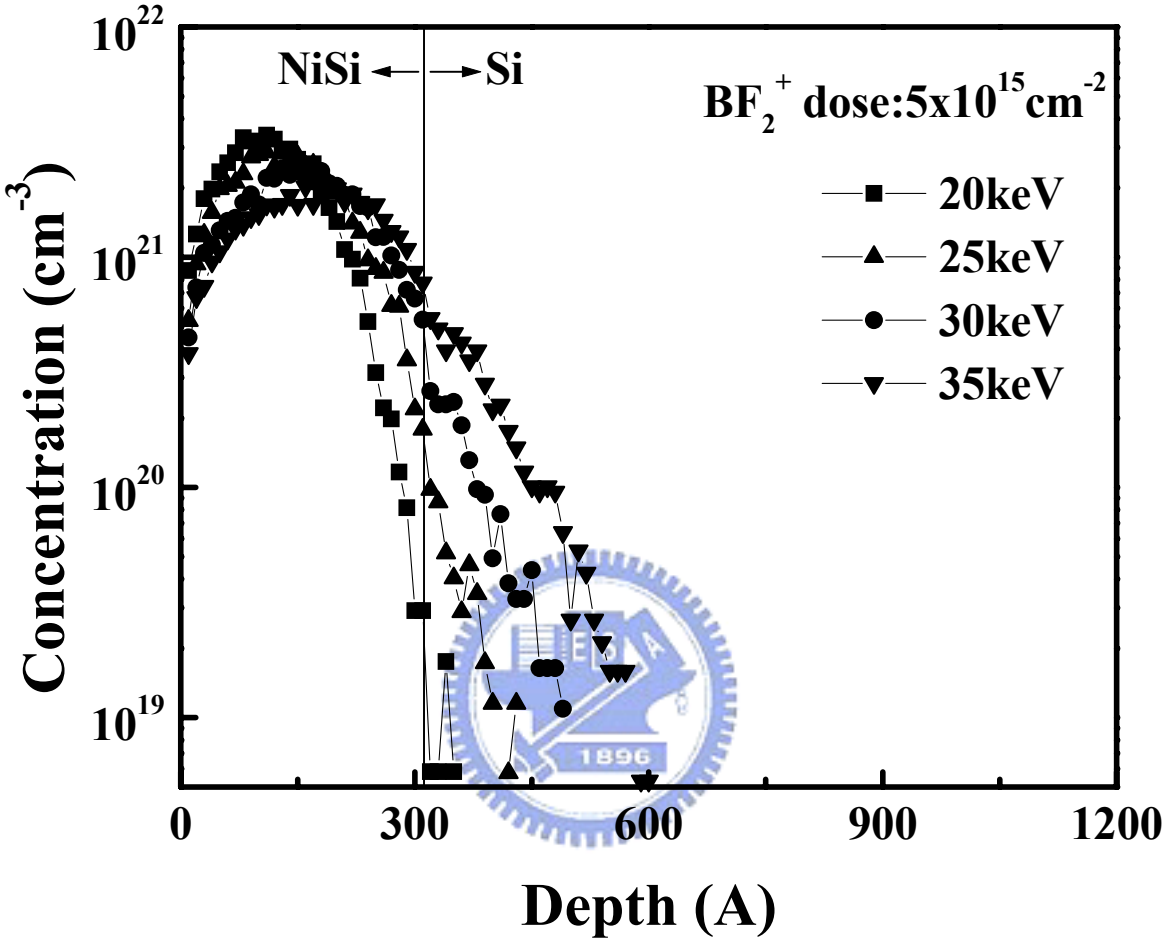


Fig. 3-4 The as-implanted boron profiles obtained by TRIM simulation for BF_2^+ implantation into a 310-Å-thick NiSi film on Si substrate to a dose of 5×10^{15} cm^{-2} at various energies.

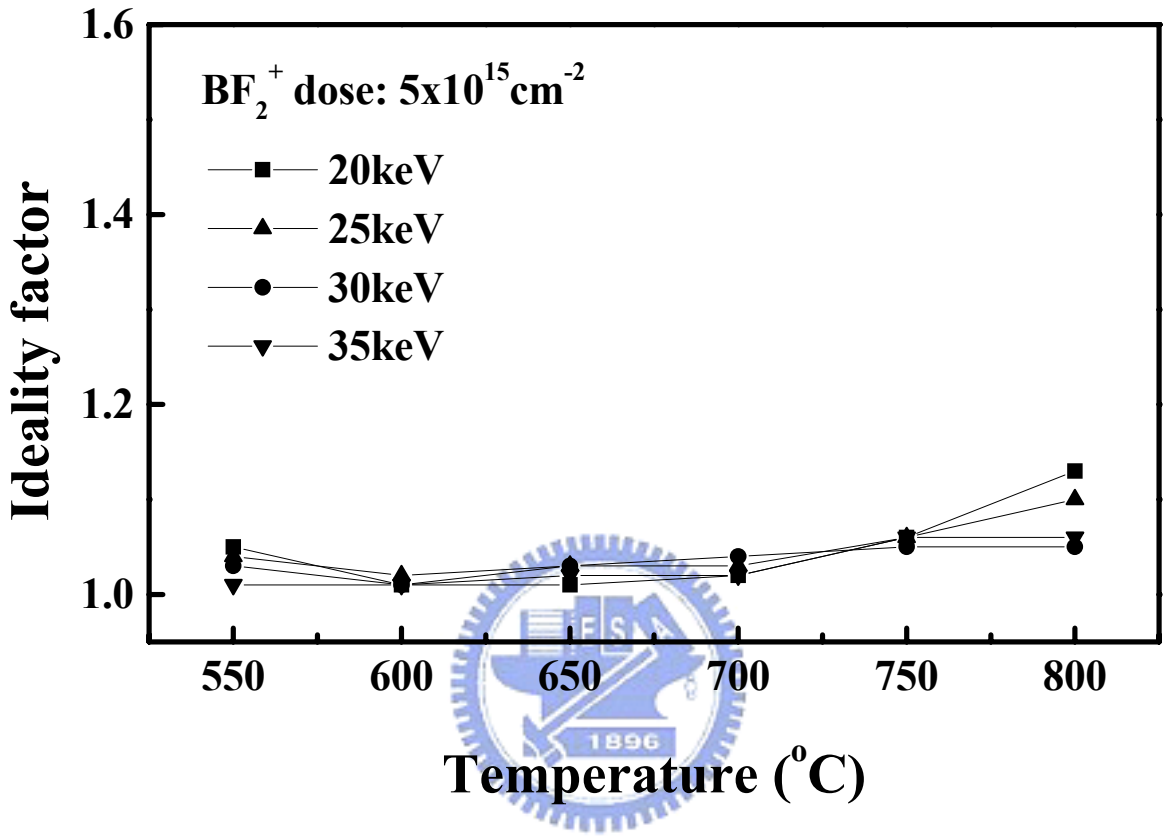


Fig. 3-5 Forward ideality factor vs. annealing temperature for the NiSi(310Å)/p^+n junction diodes fabricated with BF_2^+ implantation at various energies to a dose of 5×10^{15} cm^{-2}.

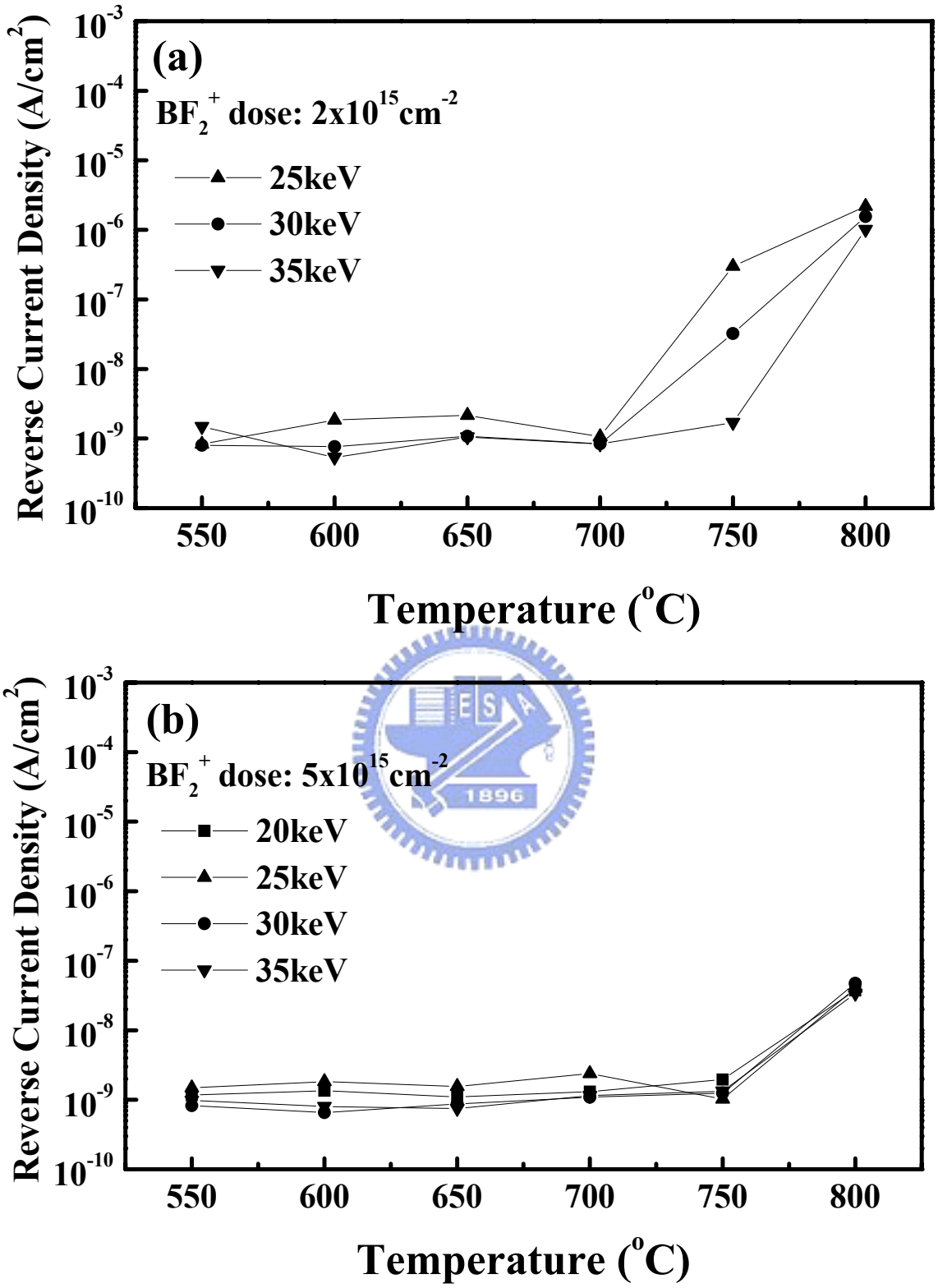


Fig. 3-6 Reverse bias current density vs annealing temperature for the NiSi(310Å)/p^+n junction diodes fabricated with BF_2^+ implantation at various energies to a dose of (a) $2\times10^{15}cm^{-2}$ and (b) $5\times10^{15}cm^{-2}$.

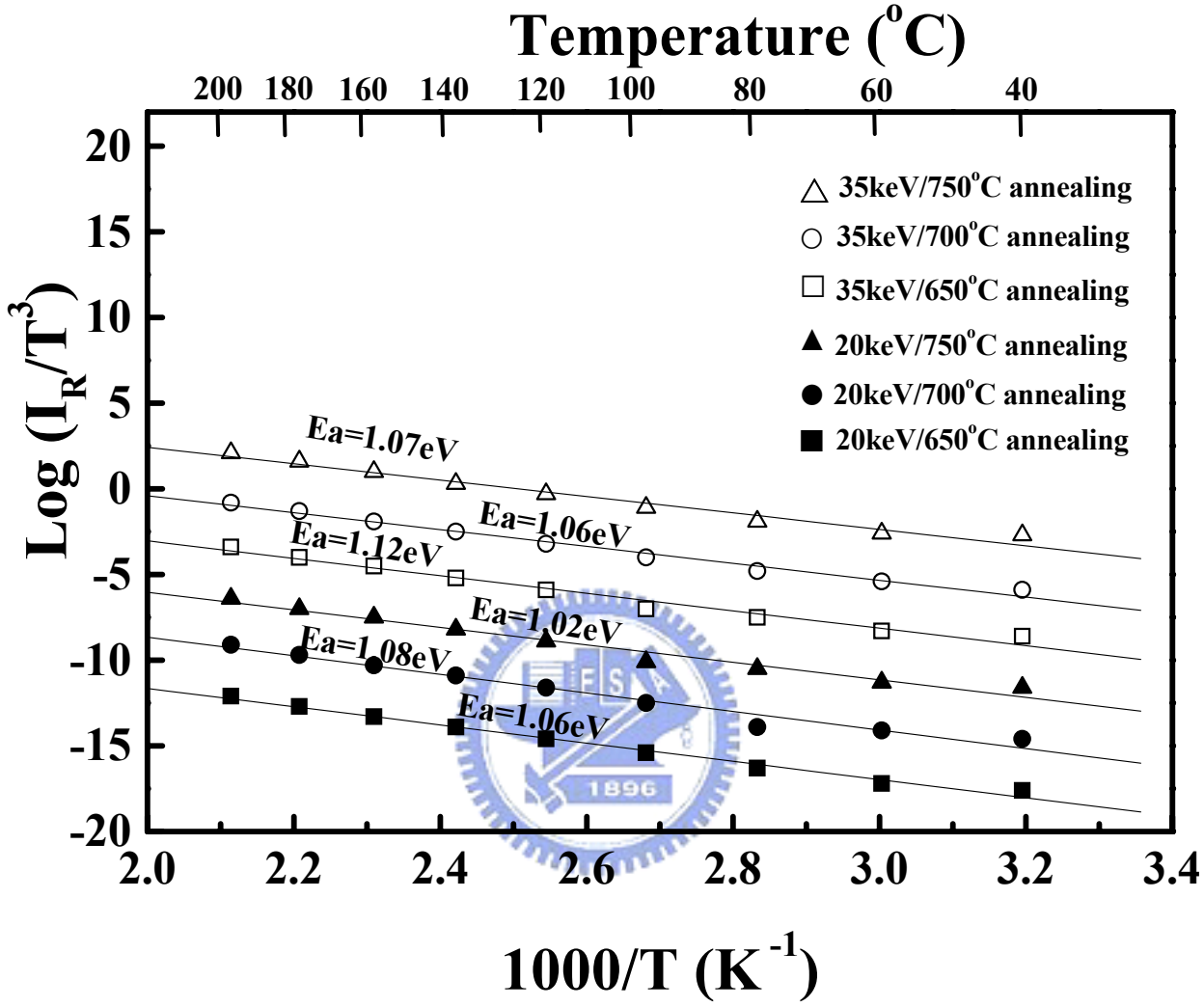


Fig. 3-7 Arrhenius plots of reverse current I_R for the NiSi(310Å)/p^+n junctions (with an area of 1100×1100μm^2) fabricated by BF_2^+ implantation at 20 and 35 keV to a dose of 5×10^{15}cm^{-2} followed by 650 to 750°C annealing for 30 min. The measurement was conducted at 1V reverse bias.

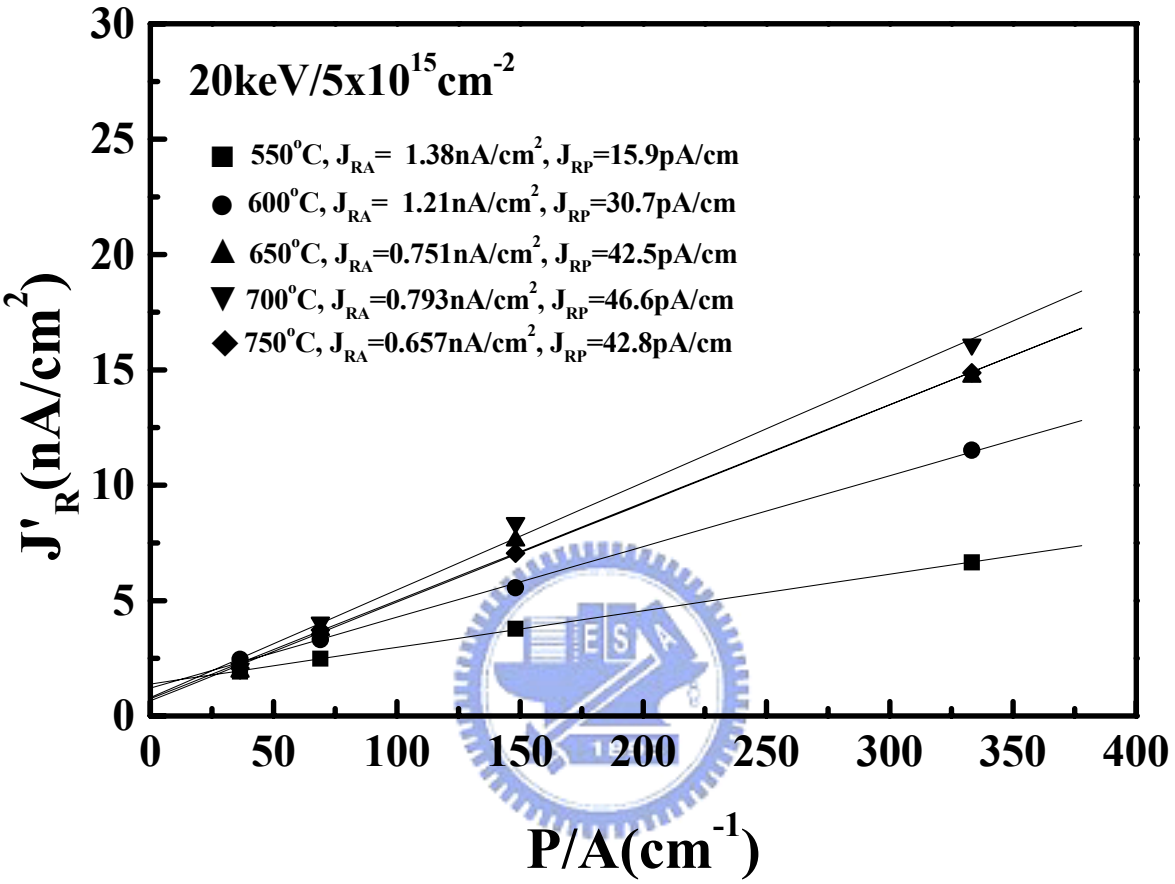


Fig. 3-8 The J'_R vs. P/A plot for the NiSi(310Å)/p^+n junctions fabricated with BF_2^+ implantation at 20 keV to a dose of $5\times10^{15}cm^{-2}$ followed by annealing at 550 to 750°C.

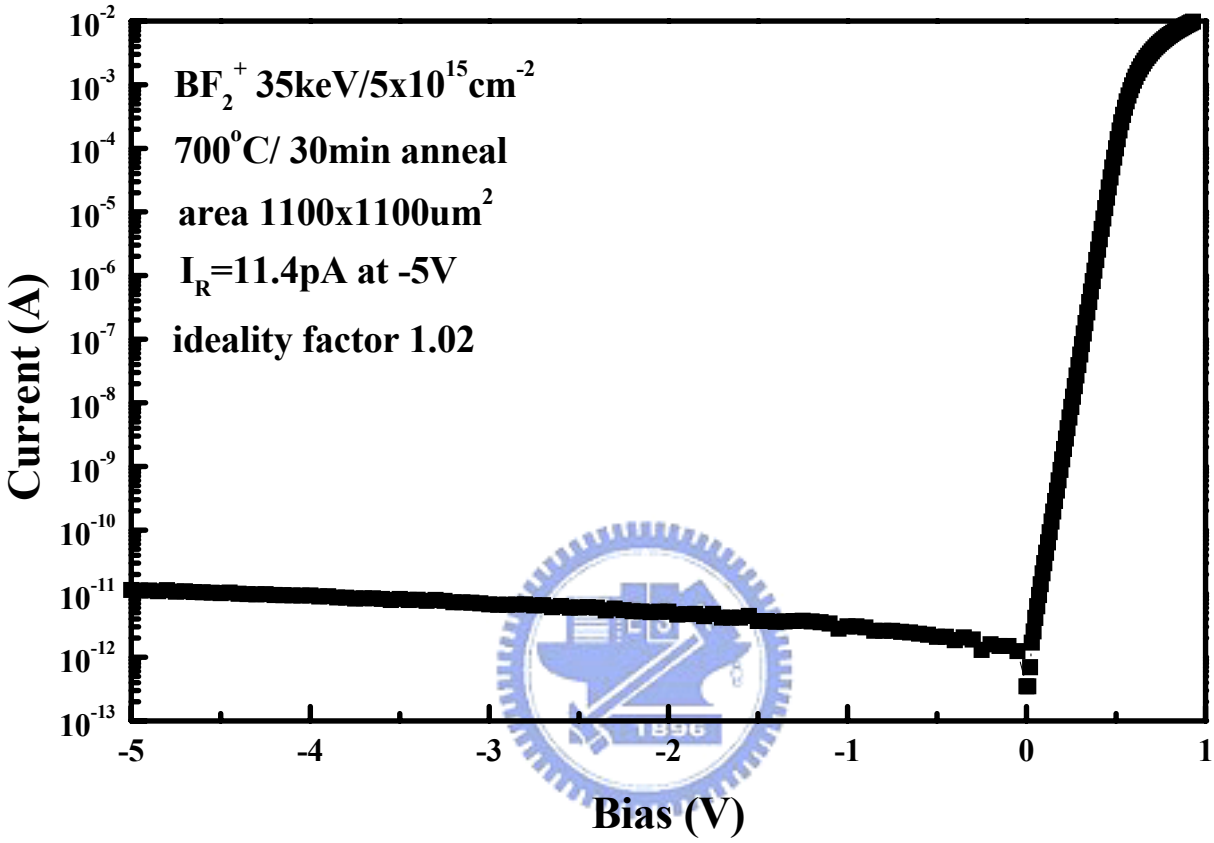


Fig. 3-9 Typical I-V characteristic for the NiSi(310Å)/p^+n junction fabricated with BF_2^+ implantation at 35keV to a dose of $5\times10^{15}cm^{-2}$ followed by a 30 min thermal annealing at 700°C.

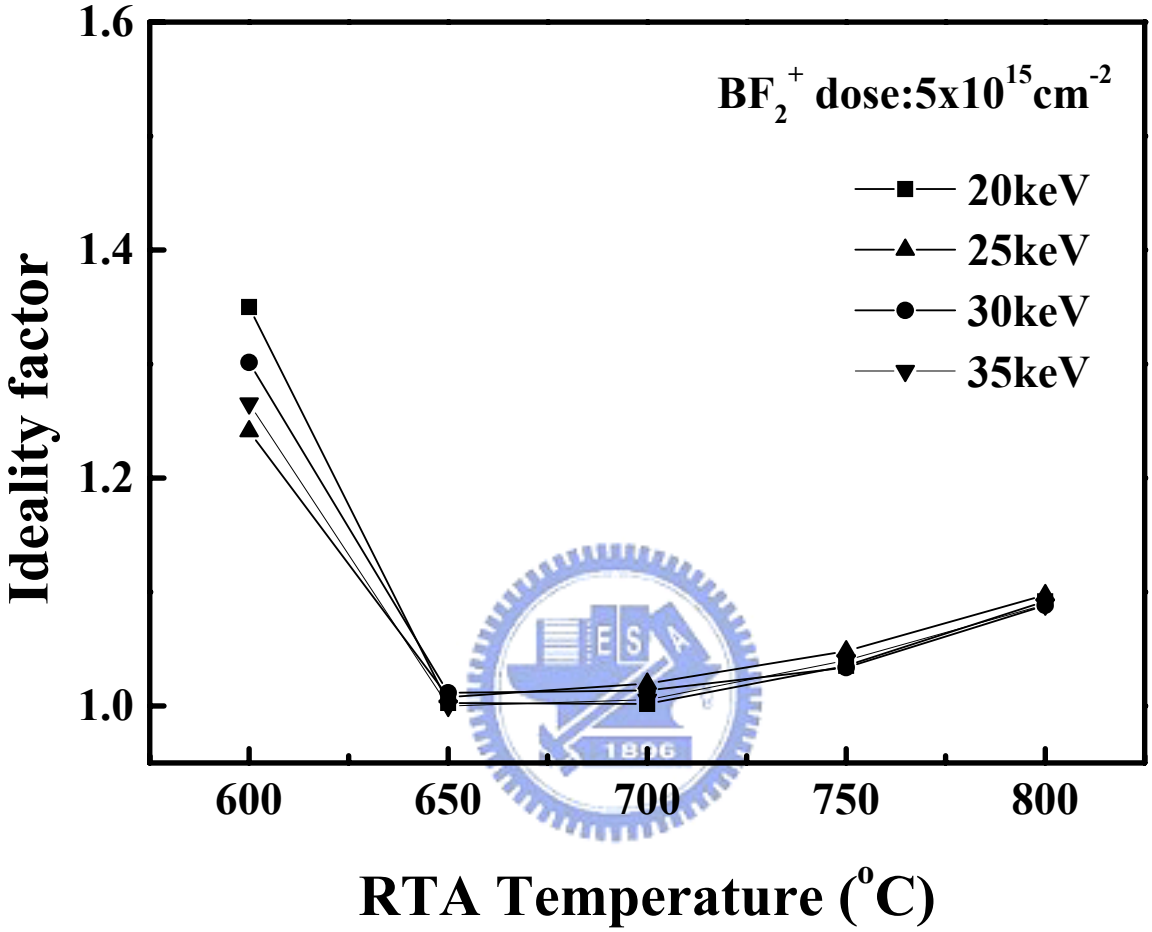


Fig. 3-10 Ideality factor vs. RTA temperature for the NiSi(310Å)/p^+n junction diodes fabricated with BF_2^+ implantation at various energies to a dose of $5\times10^{15}cm^{-2}$.

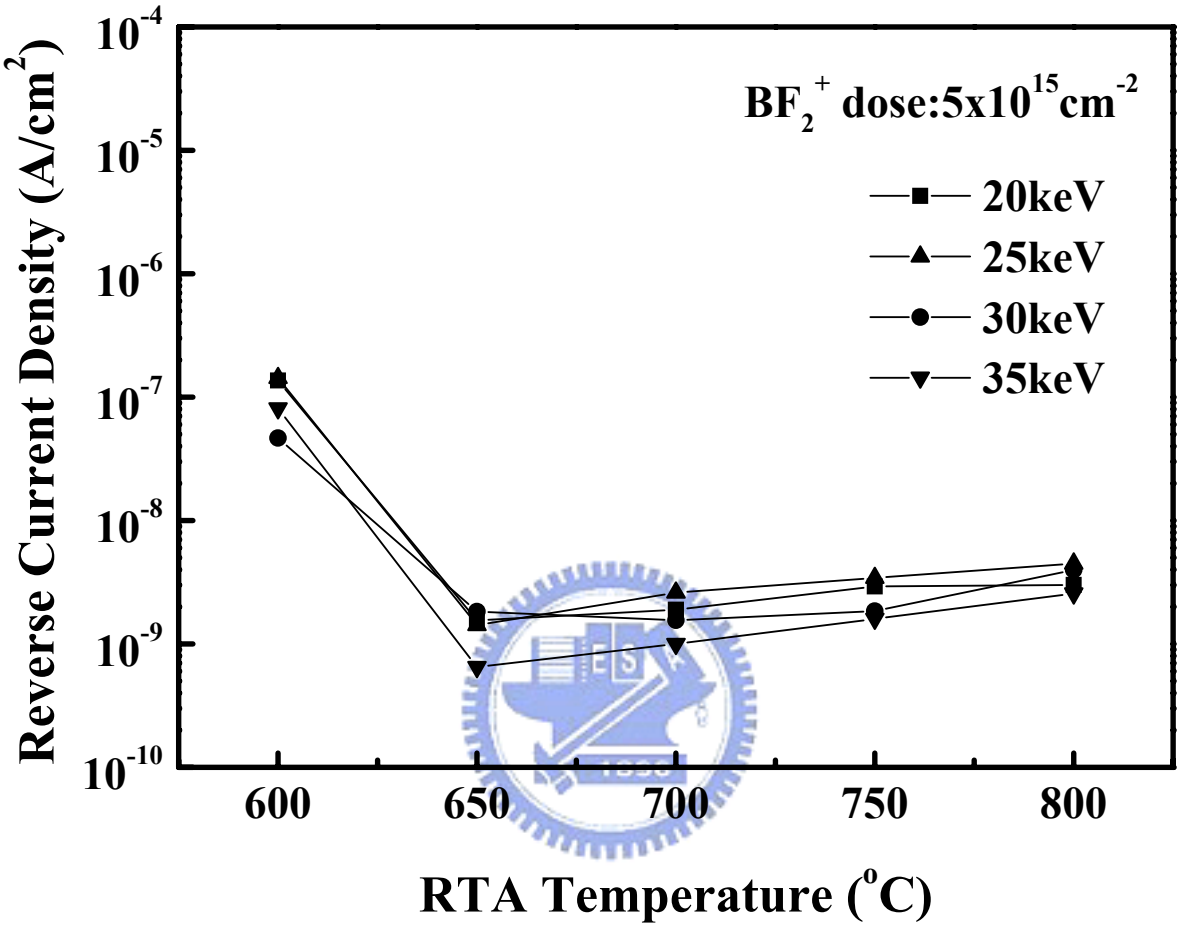


Fig. 3-11 Reverse bias current density vs. RTA temperature for the NiSi(310Å)/p^+n junction diodes fabricated with BF_2^+ implantation at various energies to a dose of $5\times10^{15}cm^{-2}$.

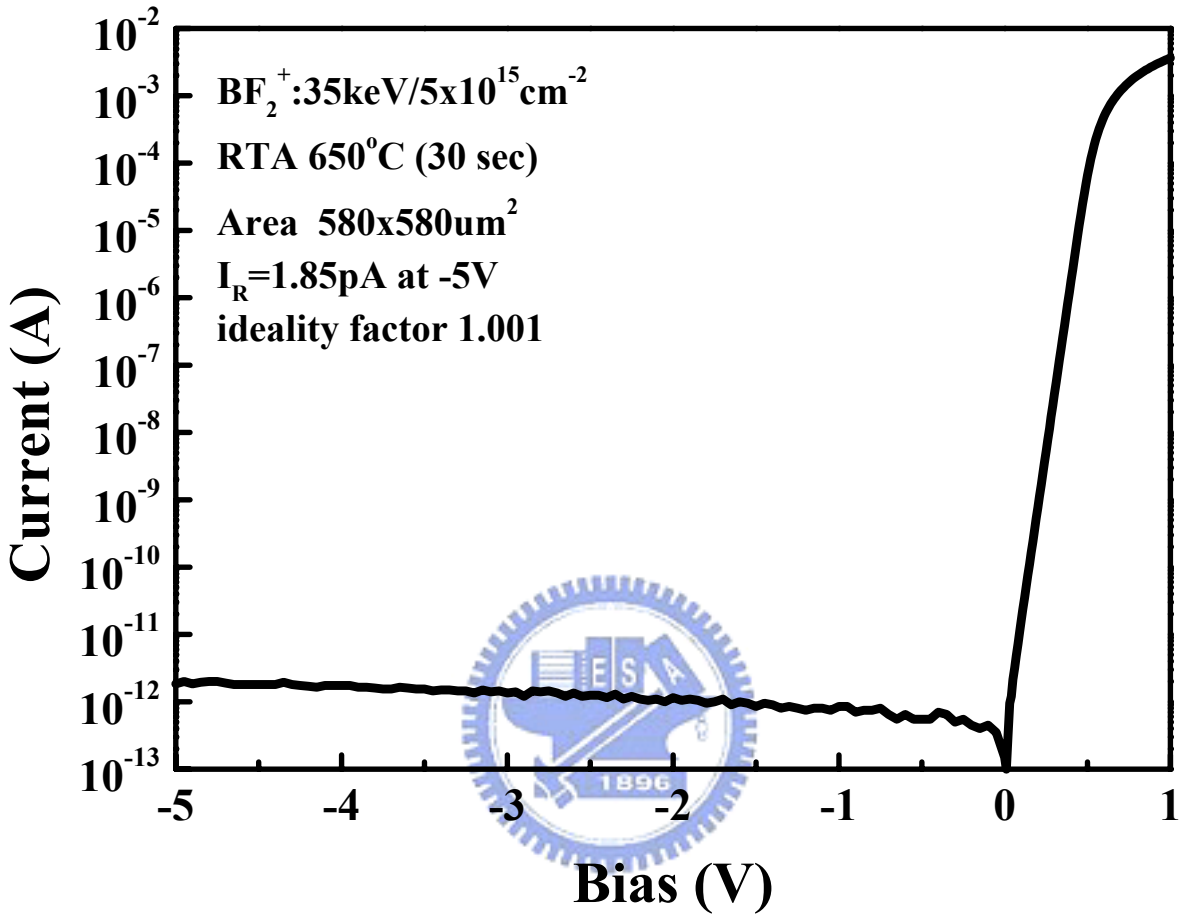


Fig. 3-12 Typical I-V characteristic for the NiSi(310Å)/p^+n junction (with an area of 580×580μm^2) fabricated with BF_2^+ implantation at 35keV to a dose of 5×10^{15}cm^{-2} followed by RTA at 650°C.

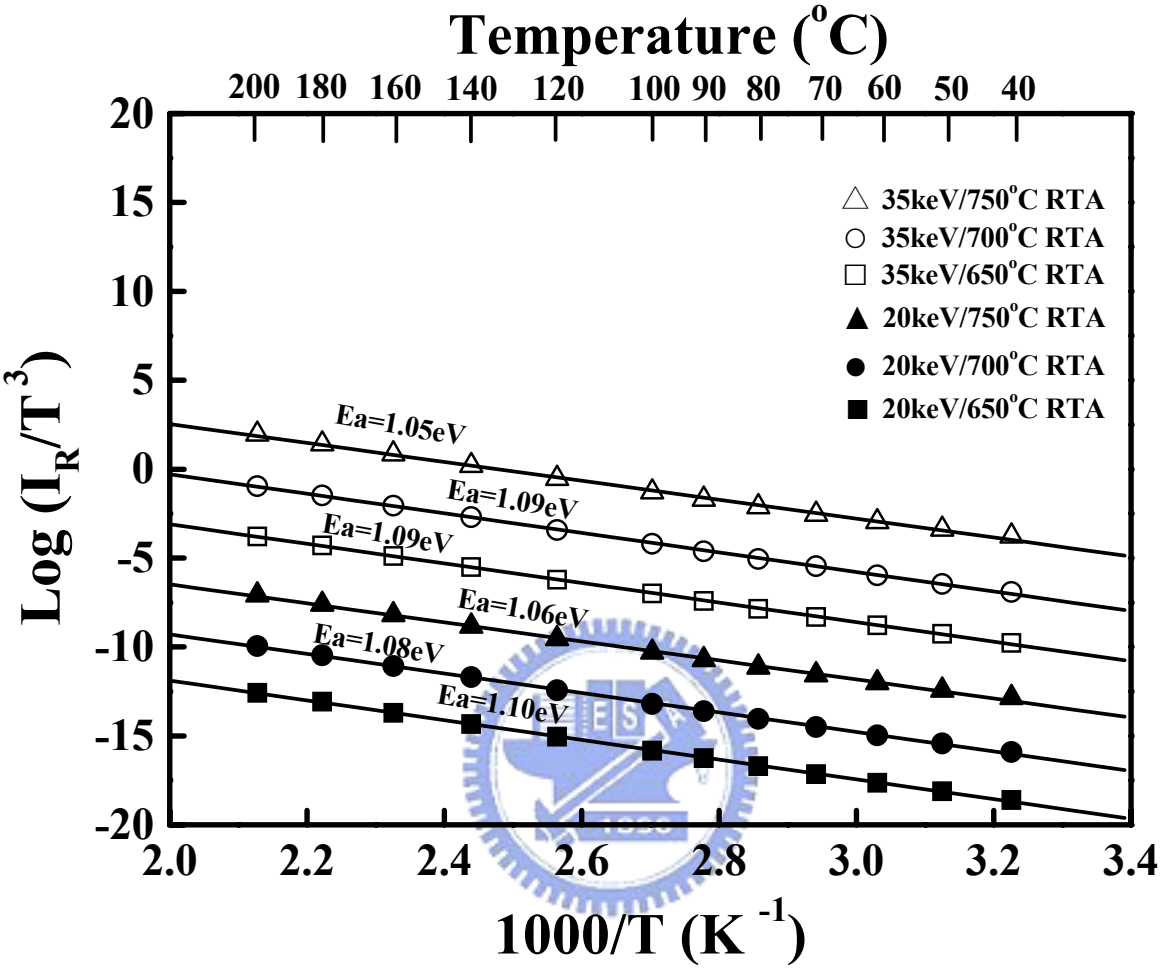


Fig. 3-13 Arrhenius plots of reverse current I_R for the NiSi(310Å)/p^+n junctions (with an area of 580×580μm^2) fabricated by BF_2^+ implantation at 20 and 35 keV to a dose of 5×10^{15}cm^{-2} followed by RTA at 650 to 750°C. The measurement was conducted at 1V reverse bias.

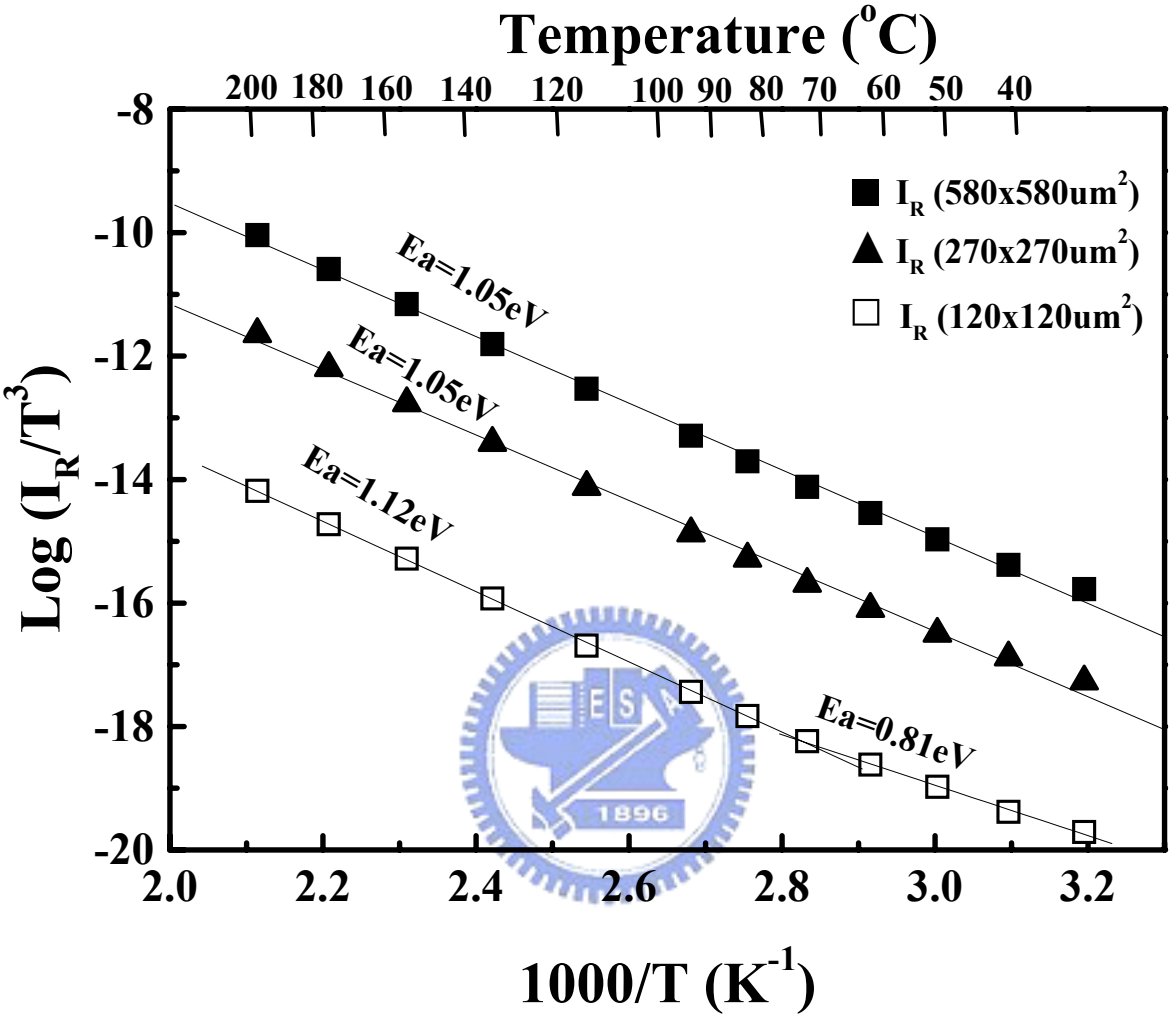


Fig. 3-14 Arrhenius plots of reverse current I_R for the NiSi(310Å)/p^+n junctions of three different junction areas fabricated with BF_2^+ implantation at 35 keV to a dose of $5\times10^{15}cm^{-2}$ followed by RTA at 750°C. The measurement was conducted at 1V reverse bias.

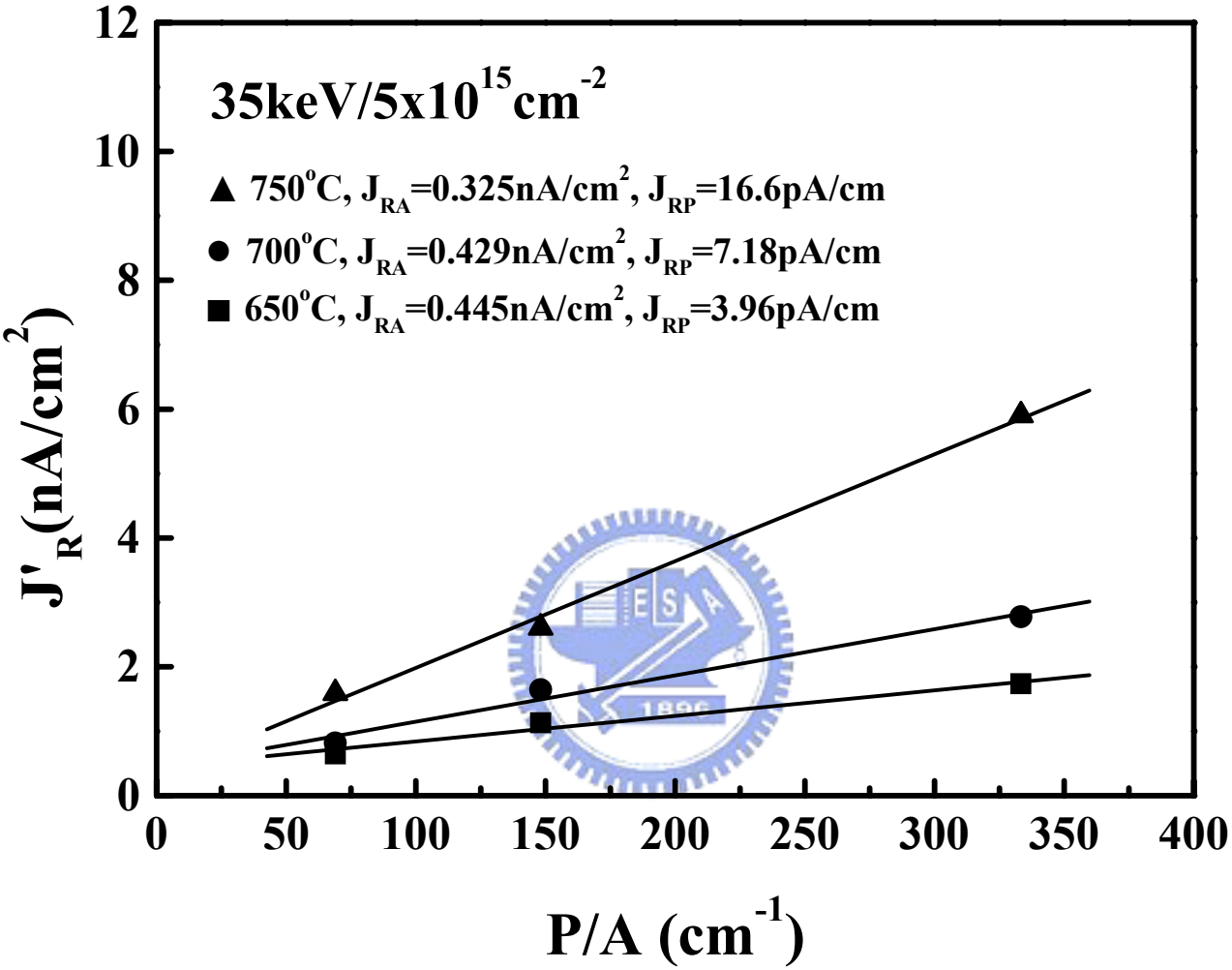


Fig. 3-15 The J'_R vs. P/A plot for the NiSi(310Å)/p^+n junctions fabricated with BF_2^+ implantation at 35 keV to a dose of $5\times10^{15}cm^{-2}$ followed by RTA at 650 to 750°C

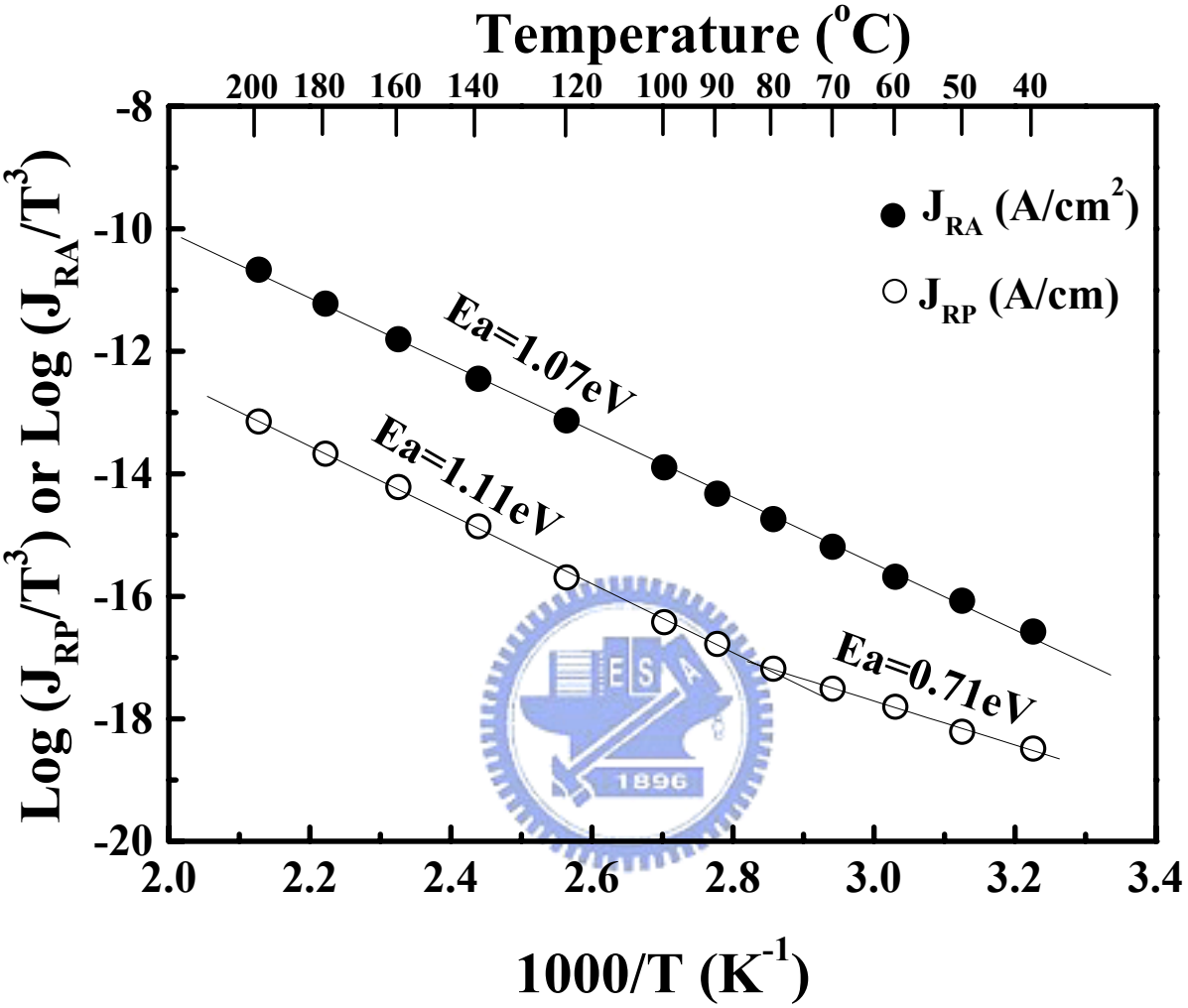


Fig. 3-16 Arrhenius plots of J_{RA} and J_{RP} for the NiSi(310Å)/p^+n junctions fabricated with BF_2^+ implantation at 35 keV to a dose of $5\times10^{15}cm^{-2}$ followed by RTA at 750°C.

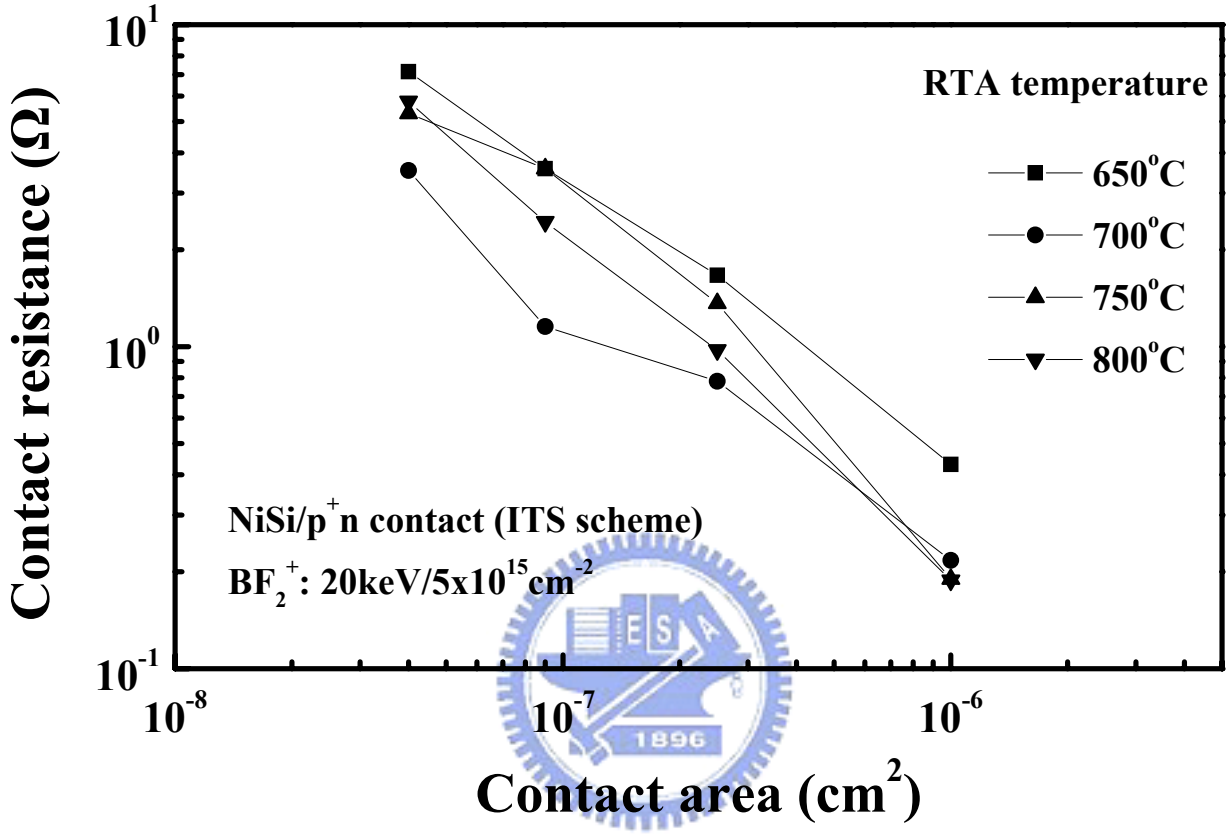


Fig. 3-17 Measured contact resistance vs. contact area for the NiSi/p^+n contact formed by ITS scheme with BF_2^+ implantation at 20keV to a dose of 5× $10^{15}cm^{-2}$ followed by RTA at various temperatures.

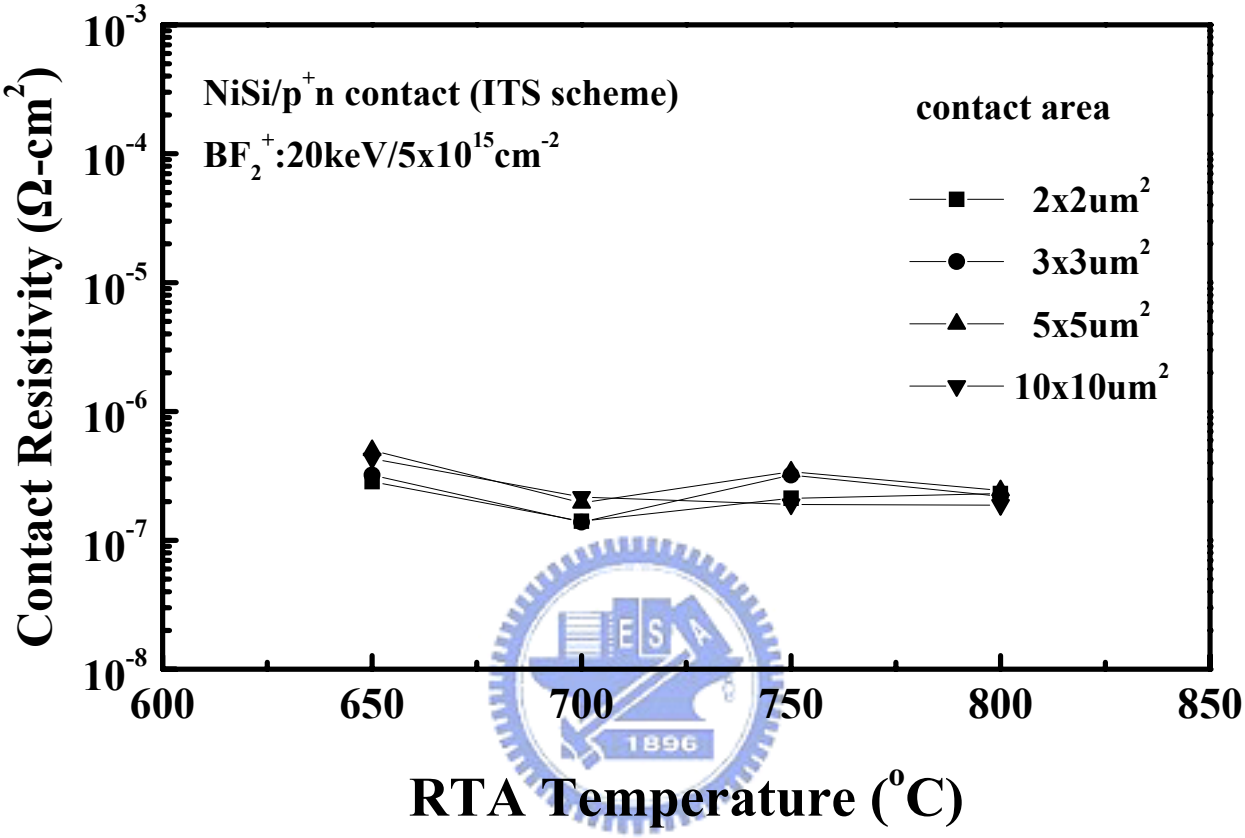


Fig. 3-18 Measured contact resistivity for the NiSi/p^+n contact formed by ITS scheme with BF_2^+ implantation at 20keV to a dose of $5\times10^{15}cm^{-2}$ followed by RTA at various temperatures. Data of four different contact areas are illustrated.

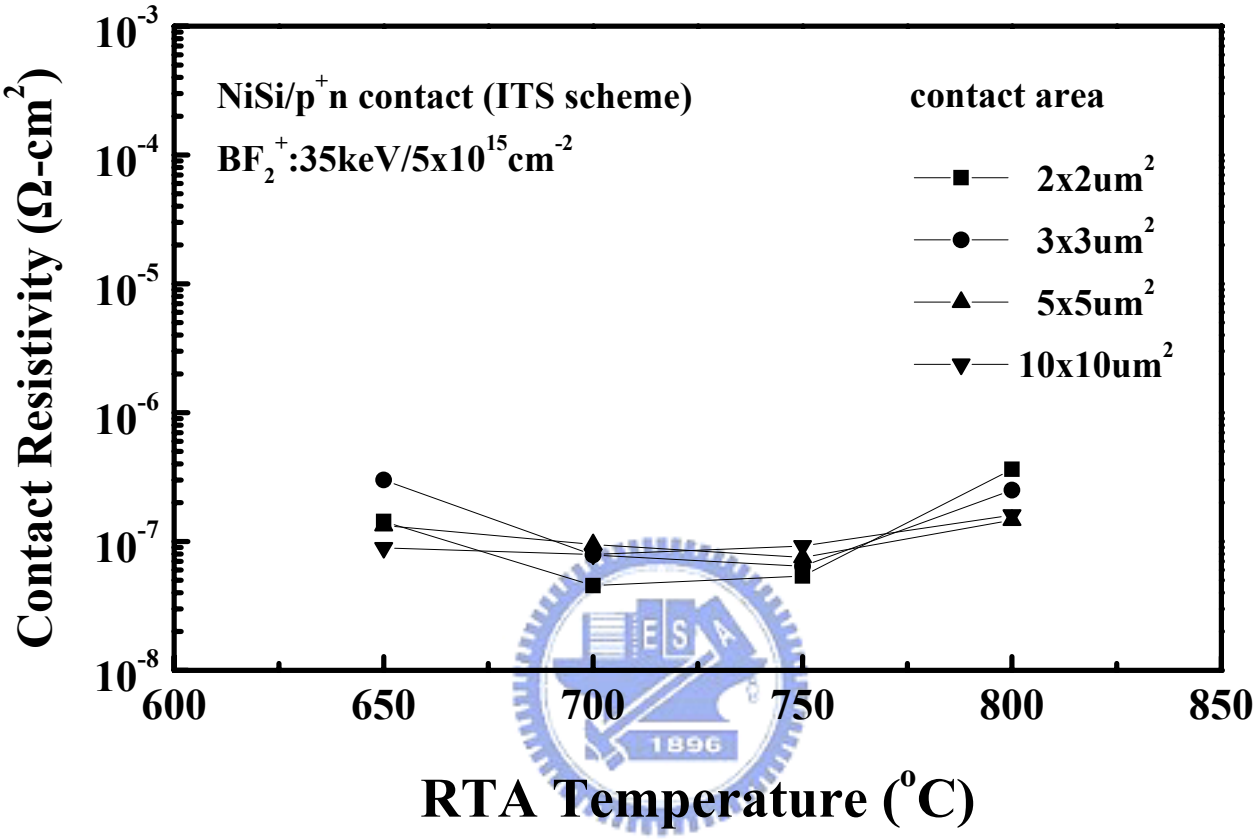


Fig. 3-19 Measured contact resistivity for the NiSi/p^+n contact formed by ITS scheme with BF_2^+ implantation at 35keV to a dose of $5\times10^{15}cm^{-2}$ followed by RTA at various temperatures. Data of four different contact areas are illustrated.