Chapter 5

Thermal stability of Cu/NiSi contacted p^+n shallow junction

5.1 Introduction

As the interconnect resistance-capacitance (RC) delay becomes a dominant factor in determining the performance of integrated circuits, the advantages of Cu metal become more remarkable. Cu metal reduces the electrical resistance of interconnection lines because of its low electrical resistivity; moreover, Cu line also exhibits a better electromigration resistance than the conventional Al-based wires [1-3]. However, copper metallization is faced with many challenges in practice, such as poor adhesion to dielectric layers, difficulty of dry etching, and the formation of Cu-Si compounds at very low temperatures (<200° C) [4-6], and the high diffusivity of Cu also introduces deep level traps in Si leading to degradation of the device performance [7]. Thus, thermal reaction of Cu with the underlayer materials and devices must be carefully evaluated and controlled for the application of Cu to the first level contact in integrated circuits.

Metal silicides are widely used in semiconductor devices in integrated circuits to reduce sheet resistance and provide lower contact resistance on source/drain and

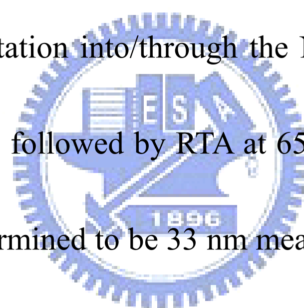
polysilicon gate areas. There have been a number of reports on the study of Cu/silicide system and the diffusion barrier property of the silicides [8-11]. It was reported that Cu exhibits different reaction behavior with different silicides. Copper diffuses across the silicide layer in the Cu/$CrSi_2$/Si and Cu/$CoSi_2$/Si structures, while Si is the dominant diffusing species and diffuses out to react with Cu and form Cu_3Si in the Cu/$TiSi_2$/Si system. Moreover, Cu was also found to react with silicide layer in the Cu/$TiSi_2$/Si and Cu/PtSi/Si systems [12-13].

In chapter 3, we found that NiSi-silicided p^+n shallow junction (using ITS scheme followed by RTA annealing) has superb electrical characteristics. The NiSi/p^+n junction has a forward ideality of 1.001 and a very low reverse current density of 0.6 nA/cm^2. In this chapter, we investigate the thermal stability and the leakage mechanism of the Cu/NiSi contacted p^+n shallow junctions.

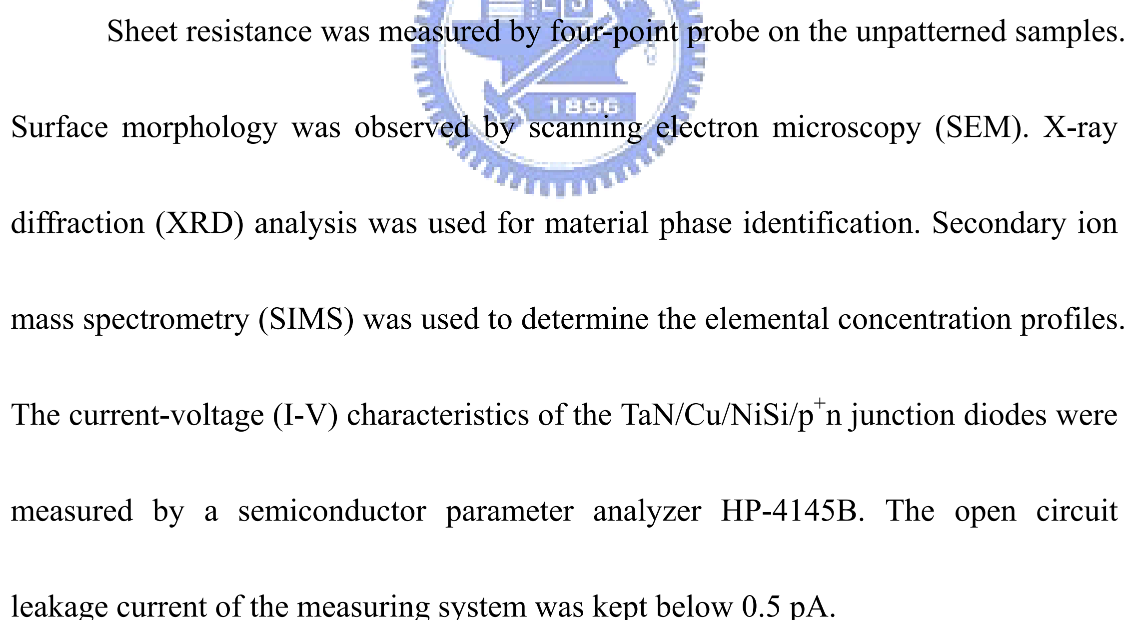
5.2 Experimental procedures

The Cu/NiSi contacted p^+n junction diodes were fabricated on n-type (100)-oriented silicon wafers with 1~2 Ω-cm nominal resistivity. After initial standard cleaning, 5500-Å thick SiO_2 was thermally grown by pyrogenic oxidation at 1050°C. Active regions with areas of 1000×1000, 500×500, and 400×400 μm^2 were defined by

the photolithography method followed by the chemical wet etching. A nickel (Ni) film of 150 Å thickness was sputter deposited in a dc sputtering system with a base pressure of less than 2.5×10^{-8} torr, using a Ni target in Ar ambient at a pressure of 2×10^{-3} torr with a deposition rate of about 10 Å/sec. After the Ni film deposition, the samples were rapid thermal annealed (RTA) at 500°C for 30 sec in a N_2 ambient to form nickel monosilicide (NiSi). The unreacted Ni film was selectively etched using a solution of H_2SO_4:H_2O_2=3:1 at 75~85°C. The NiSi film formed is about 310 Å in thickness as determined by cross-sectional TEM analysis. The p^+n junction diodes were formed by BF_2^+ implantation into/through the NiSi silicide at an energy of 35 keV to a dose of 5×10^{15} cm^{-2}, followed by RTA at 650°C in a N_2 ambient for 30 sec. The junction formed was determined to be 33 nm measured from the NiSi/Si interface. Then, the samples were split into two groups; one group of samples were metallized with a 200-nm-thick Cu metal followed by depositing a 50-nm-thick TaN passivation layer, while the other group of samples were deposited only with a 100-nm-thick TaN layer for a comparison. The Cu layer and the TaN passivation layer were both deposited using a dc sputtering system with a base pressure below 6×10^{-7} torr. The Cu layer was sputter deposited using a Cu target in an Ar ambient at a pressure of 6×10^{-3} torr with a deposition rate of 70 Å/sec. The TaN film was reactively sputter deposited using a Ta target in an Ar/N_2 mixed ambient at a pressure of 6×10^{-3} torr; the flow rates



of Ar and N_2 into the sputtering chamber were 53.2 and 2.8 sccm, respectively, for making the Ar/N_2 gas mixture. A lift-off process was used to define the metal gate of the active area. The metallized samples were thermally annealed at a temperature ranging from 200 to 500°C in a N_2 ambient for 30 min for thermal stability investigation of the Cu/NiSi/p^{+}n junction diodes. Finally, a 5000-Å-thick Al layer was deposited on the backside of Si substrate for all samples for a better contact in electrical measurements. For the material analysis, unpatterned samples of the TaN/Cu/NiSi/p^{+}n and TaN/NiSi/p^{+}n structures were also prepared following the same process and thermal annealing treatment.



Sheet resistance was measured by four-point probe on the unpatterned samples. Surface morphology was observed by scanning electron microscopy (SEM). X-ray diffraction (XRD) analysis was used for material phase identification. Secondary ion mass spectrometry (SIMS) was used to determine the elemental concentration profiles. The current-voltage (I-V) characteristics of the TaN/Cu/NiSi/p^{+}n junction diodes were measured by a semiconductor parameter analyzer HP-4145B. The open circuit leakage current of the measuring system was kept below 0.5 pA.

5.3 Results and discussion

5.3.1 Electrical measurement

The reverse bias leakage current was measured at -5 V on 20 randomly chosen samples in each category to construct the statistical distribution. Figure 5-1 shows the statistical distribution of the reverse bias leakage current density for the TaN/NiSi/p^+n and TaN/Cu/NiSi/p^+n junction diodes annealed at various temperatures. The junction diodes without a Cu layer in their electrode remained intact at temperatures up to at least 500°C, whereas the junction diodes with a Cu electrode remained stable only up to a temperature of 350°C. Upon annealing at 375°C, the TaN/Cu/NiSi/p^+n junction diodes showed a remarkable increase in leakage current, and the leakage current kept increasing with increasing annealing temperature.

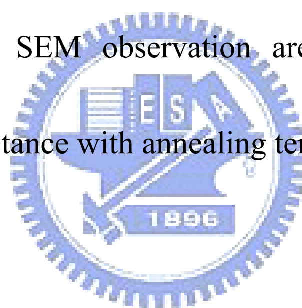
1896

5.3.2 Sheet resistance measurement

Figure 5-2 shows the sheet resistance (Rs) as a function of annealing temperature for the TaN/NiSi/p^+n and TaN/Cu/NiSi/p^+n samples. The Rs of the TaN/NiSi/p^+n sample remained stable up to at least 500°C, while a sharp increase in Rs occurred for the TaN/Cu/NiSi/p^+n sample after thermal annealing at temperatures above 425°C, due to the formation of Cu-silicide (Cu_3Si) phase as evidenced by the results of SEM and XRD analyses to be shown in the following sections.

5.3.3 Surface morphology

Figure 5-3 and Fig. 5-4 show the surface morphology and the cross-sectional view SEM images, respectively, for the TaN/Cu/NiSi/p^+n sample annealed at various temperatures. The surface of the sample remained intact at temperatures below 400°C. After annealing at 425°C, crack occurred on the TaN surface, and protrusions were clearly observed in the cross-sectional view. The protrusion is presumably due to the formation of the Cu-silicide (Cu_3Si) phase, as evidenced by the results of XRD analysis to be shown in next section. With increasing annealing temperature, Cu_3Si had grown big enough to break the sample structure. The results of the annealing-temperature-related SEM observation are roughly consistent with the sample's increasing sheet resistance with annealing temperature.



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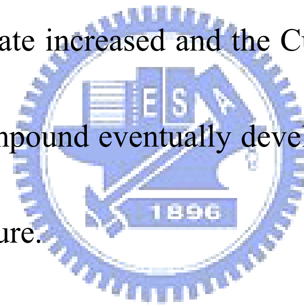
5.3.4 XRD analysis

Figure 5-5 shows the XRD spectra of the TaN/Cu/NiSi/p^+n sample annealed at various temperatures. The Cu_3Si phase started to appear after annealing at 425°C and was clearly detected at higher temperatures. The decreasing diffraction peak intensity of Cu at temperatures above 400°C implies that an increasing amount of Cu was consumed in the process of Cu_3Si silicide phase formation, resulting in the protrusion, as shown in the SEM micrographs, and the drastic increase in the measured sheet resistance. In addition, Ta_2N and TaN phases appeared after annealing at 475°C.

5.3.5 SIMS depth profiles

Figure 5-6 shows the SIMS depth profiles for the as-fabricated and thermally annealed TaN/Cu/NiSi/p^+n-Si samples. It was found that Cu started to penetrate into/through NiSi layer at a temperature as low as 375°C. The remarkable increase in reverse bias leakage current may be attributed to the formation of deep level trap states due to the penetration of Cu into the shallow junction region, though the Rs measurement and the SEM and XRD analyses indicate that the Cu_3Si phase might have not formed after 375°C annealing. Upon annealing at higher temperatures, the amount of Cu in the Si substrate increased and the Cu_3Si compound was formed; the rapid growth of the Cu_3Si compound eventually developed into the complete collapse of the TaN/Cu/NiSi/p^+n structure.



5.4 Conclusion

The TaN/NiSi/p^+n junction diode is thermally stable up to at least 500°C (by thermal annealing for 30 min). However, the Cu-contacted TaN/Cu/NiSi(310 Å)/p^+n junction diode remains stable only up to a temperature of 350°C. SIMS analysis indicates that Cu started to penetrate into the NiSi-contacted shallow junction when the sample was annealed at 375°C, leading to a drastic increase in reverse bias leakage current. After annealing at 425°C, metallurgical reaction is evident from the top view

and cross-sectional view SEM observations. XRD analysis indicates the formation of Cu_3Si silicide phase. The rapid growth of Cu_3Si during the thermal annealing at 425°C resulted in the break of TaN layer, causing the eventual collapse of the TaN/Cu/NiSi/Si structure.

References

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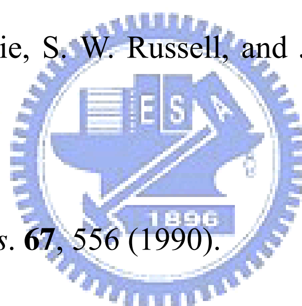

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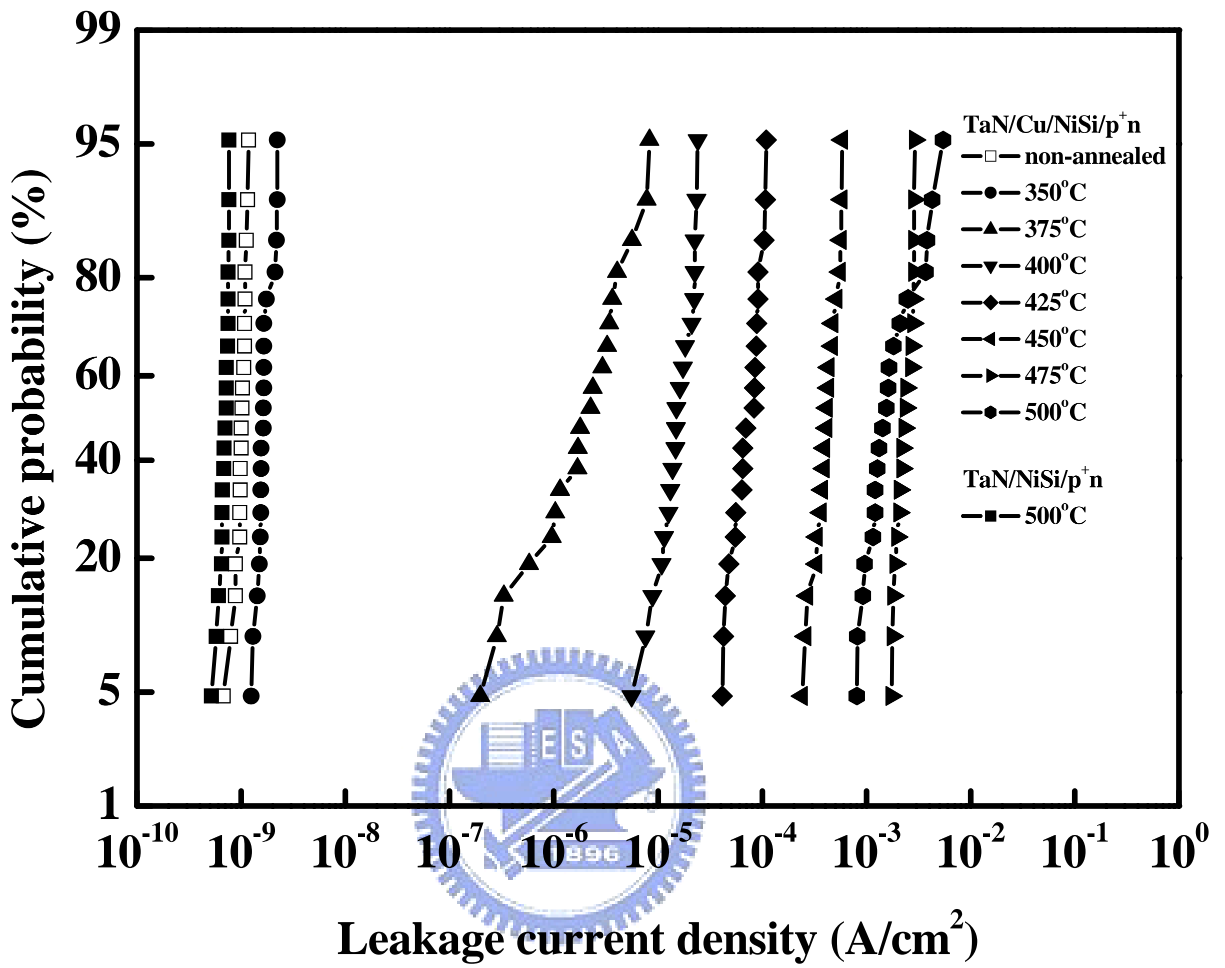


Fig. 5-1 Statistical distributions of reverse bias leakage current density for TaN/NiSi/p$^+$n and TaN/Cu/NiSi/p$^+$n junction diodes annealed at various temperatures.

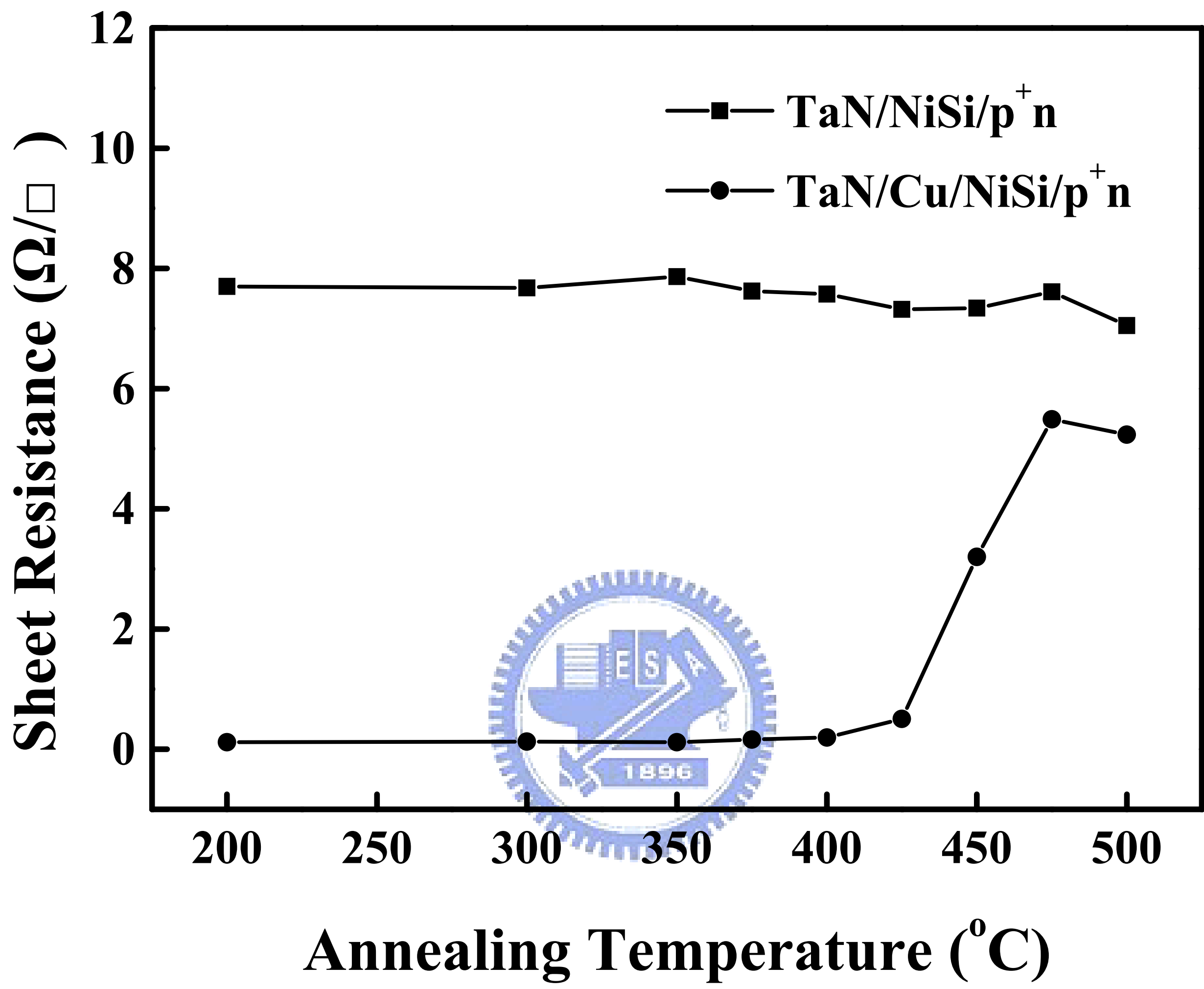
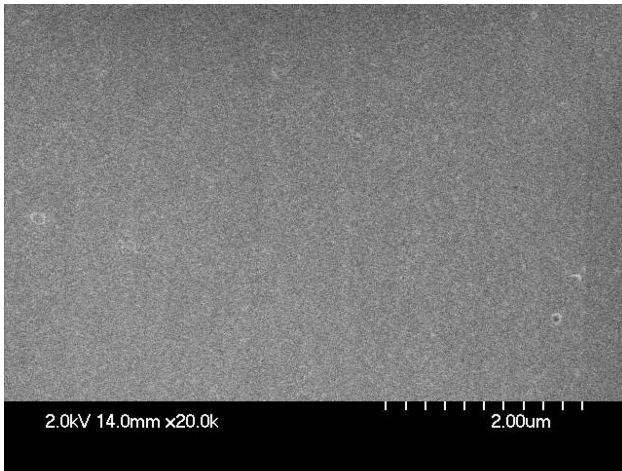


Fig. 5-2 Sheet resistance vs. annealing temperature for TaN/NiSi/p^+n and TaN/Cu/NiSi/p^+n samples.



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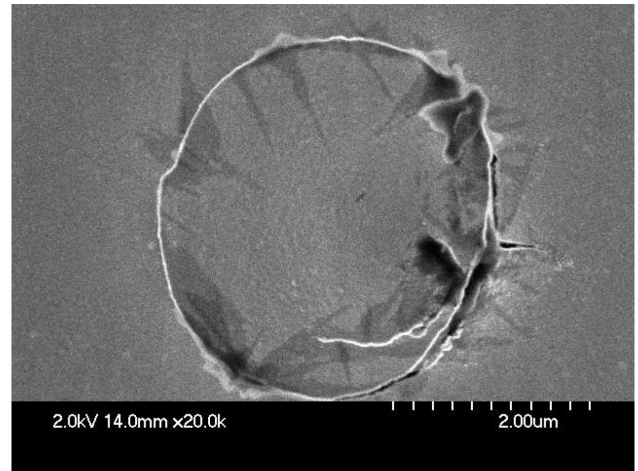

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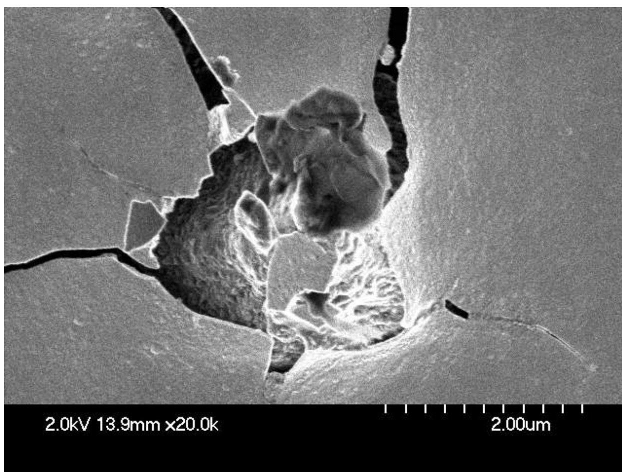

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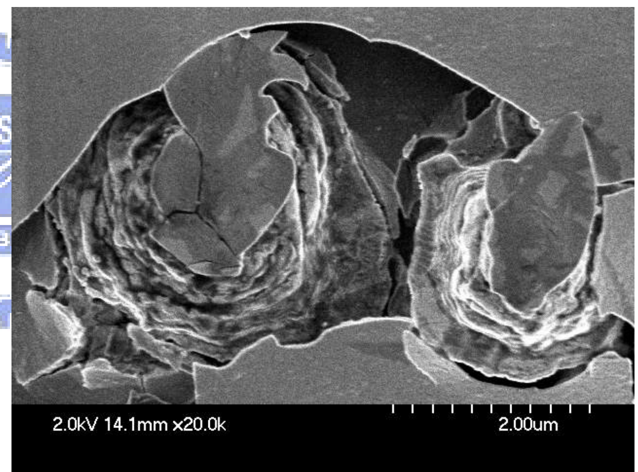
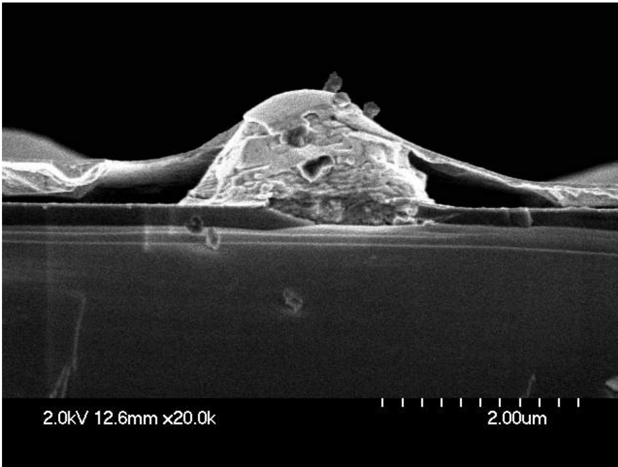


(d)

Fig. 5-3 SEM images showing top view (surface morphology) of TaN/Cu/NiSi/p^+n sample annealed at (a) 350°C, (b) 425°C, (c) 475°C, and (d) 500°C.



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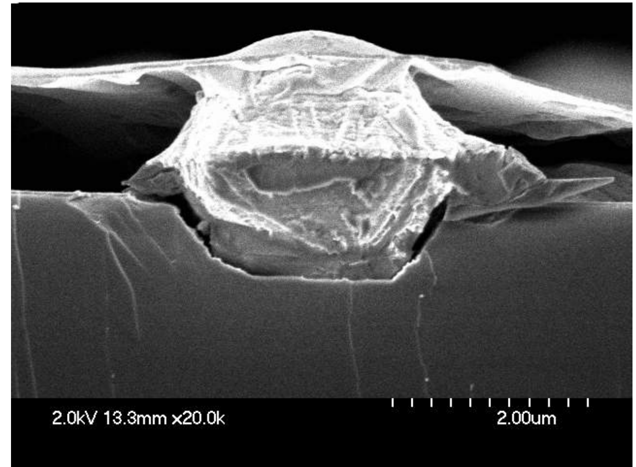

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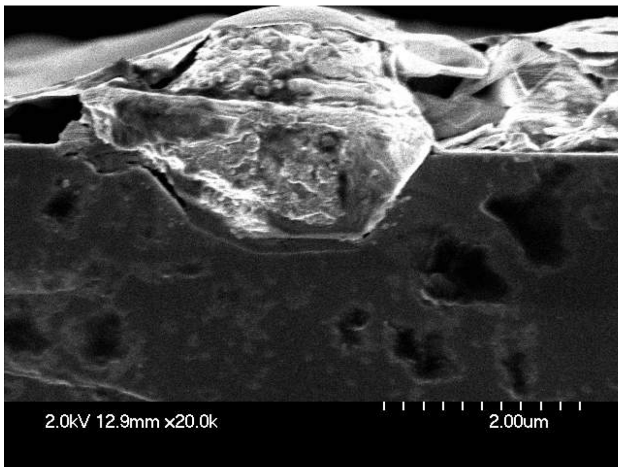


(c)

Fig. 5-4 SEM images showing cross-sectional view of TaN/Cu/NiSi/p^+n sample annealed at (a) 425°C, (b) 475°C, and (c) 500°C.

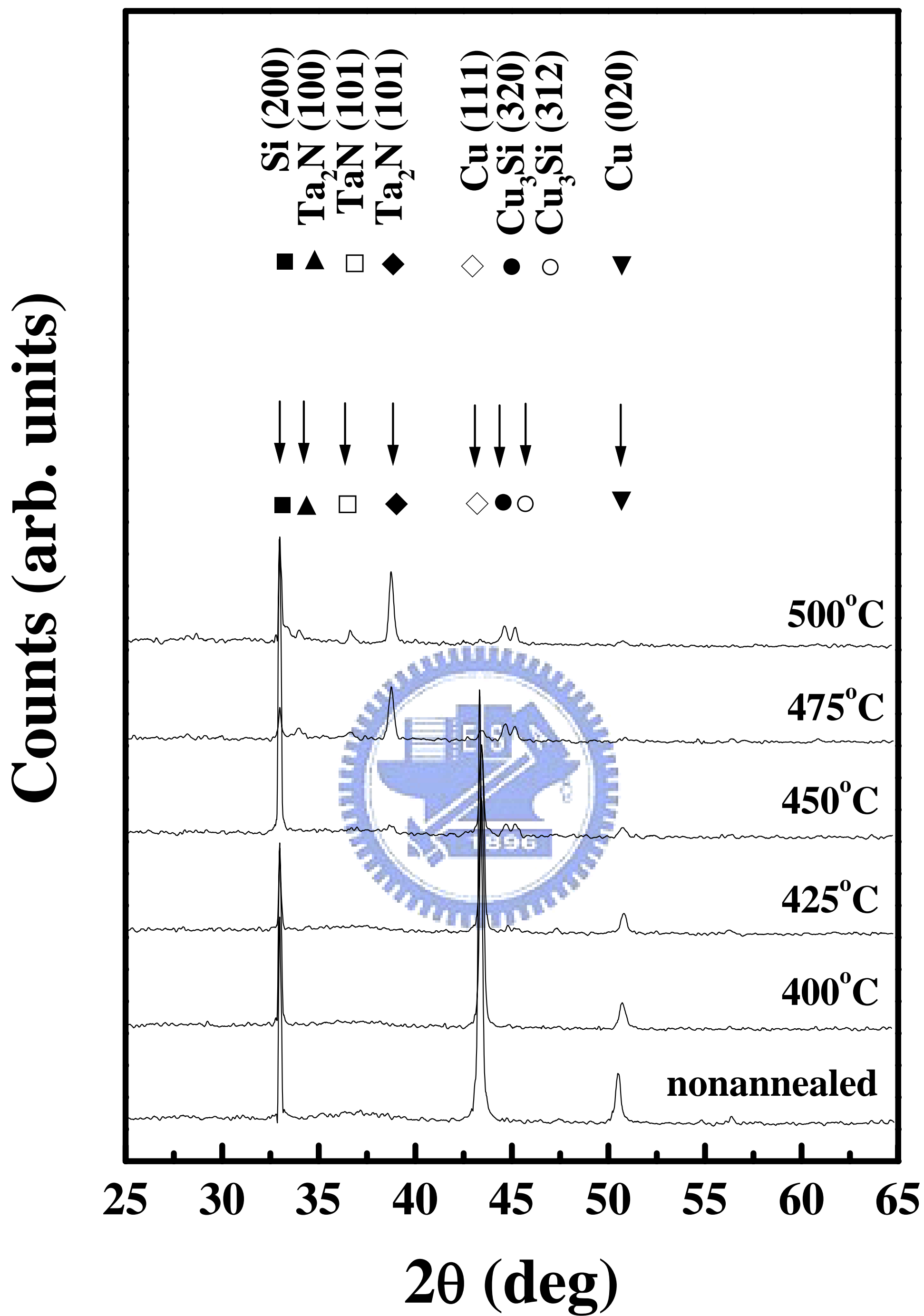
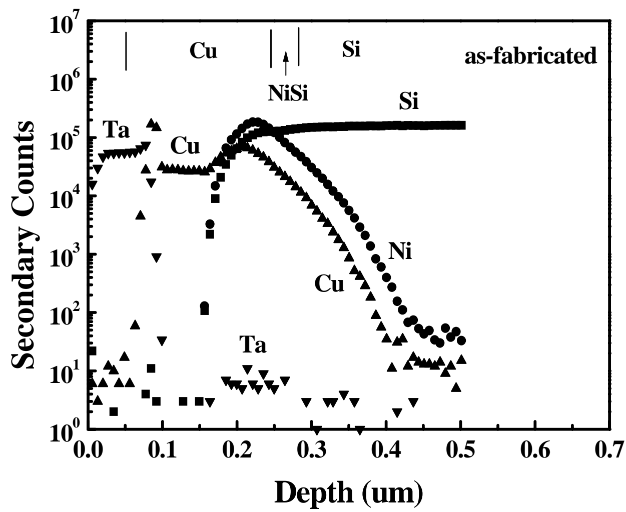
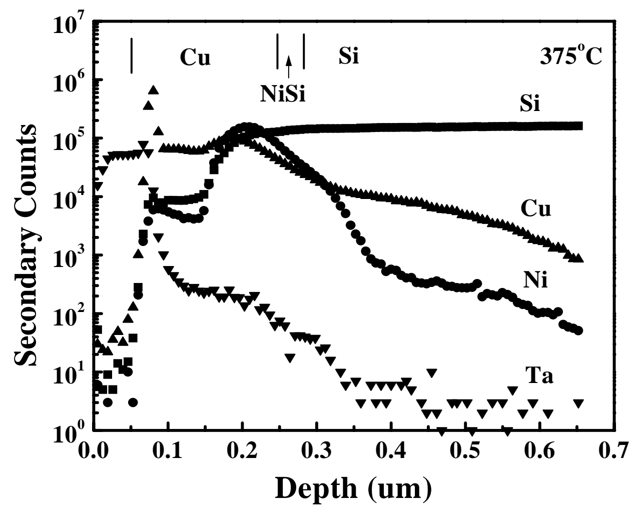


Fig. 5-5 XRD spectra of TaN/Cu/NiSi/p^+n sample annealed at various temperatures.



(a)



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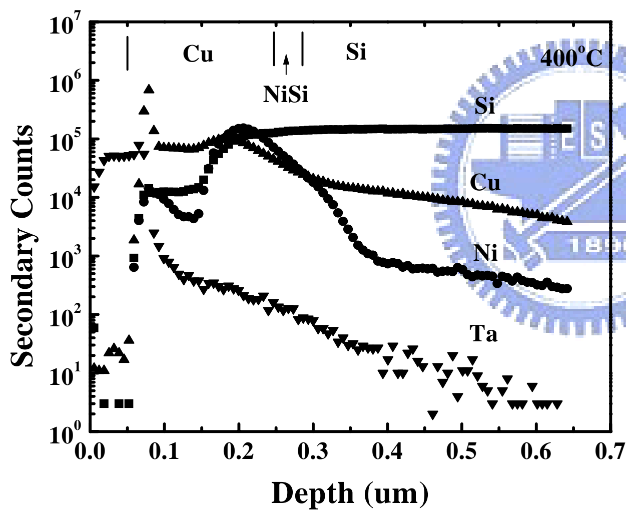

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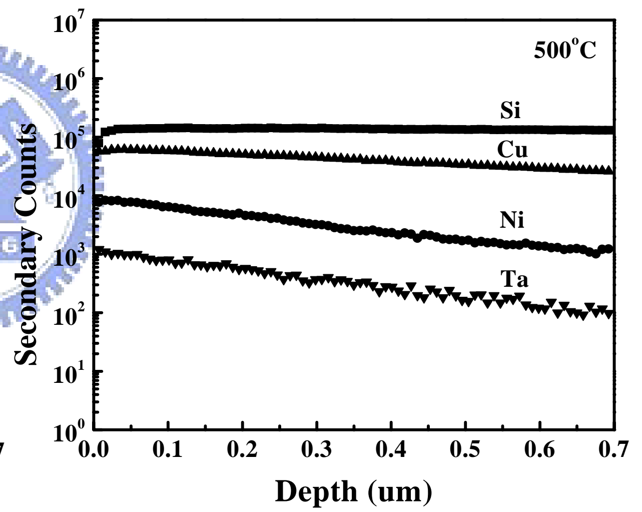

(d)

Fig. 5-6 SIMS depth profiles of TaN/Cu/NiSi/p^+n sample (a) as-fabricated and annealed at (b) 375°C, (c) 400°C, and (d) 500°C.