Chapter 6

Conclusion

6.1 Main conclusions from the study of this dissertation

Salicide process has been widely used in ULSI integrated circuits, and a simple and low temperature process is the future trend of the salicide scheme. This dissertation investigates the material and electrical properties of nickel silicide relevant to VLSI applications. In the first place, the thermal stability of nickel monosilicide (NiSi) on Si substrate is investigated, including the effect of fluorine atoms incorporation. Then, the NiSi contacted p^+n junctions fabricated by BF_2^+ implantation followed by FA and RTA process, as well as the NiSi contacted n^+p junctions fabricated by P^+ and P^+/F^+ dual implantation followed by FA process, are investigated using ITS scheme. In addition, contact resistivity of the NiSi/p^+n shallow junctions formed by ITS scheme is evaluated by four terminal Kelvin test structure. Finally, the thermal stability of the Cu-contacted TaN/Cu/NiSi/p^+n junction diodes is also investigated. The main conclusions of this study are summarized as follows.

6.1.1 Thermal stability of nickel silicide

The thermal stability of thin NiSi film on Si substrate is investigated. It was

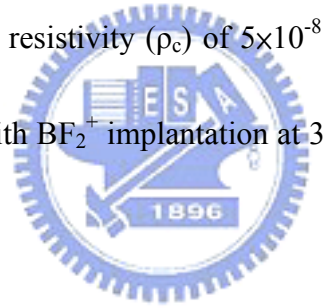
found that the incorporation of fluorine atoms in the NiSi film via BF_2^+ or F^+ ion implantation significantly improves the high temperature thermal stability of the thin NiSi silicide film, which shows thermally stable up to at least 750°C (by thermal annealing for 30 min). Presumably the implanted fluorine species are segregated to the NiSi grain boundaries and NiSi/Si interface, forming strong Si–F and Ni–F bonds and thus suppressing NiSi film agglomeration by decreasing the interfacial energy, i.e. stress between the silicide layer and the Si substrate; as a result, the integrity of the silicide layer is preserved at high temperatures. For the formation of NiSi/n^+p shallow junctions by P^+ implantation, the P^+/F^+ dual implantation (P^+ implant followed by F^+ implant) is able to significantly improve the NiSi film's thermal stability and retard the silicide film agglomeration at high temperatures. In the system of NiSi/Si, we conclude that an effective means of upgrading the NiSi resistance to film agglomeration at high temperatures is to introduce a sufficient amount of fluorine atoms in the NiSi silicide film and at the NiSi/Si interface.

6.1.2 NiSi/p^+n shallow junction

The NiSi-contacted p^+n shallow junctions are fabricated using ITS scheme by BF_2^+ implantation into/through NiSi(310 Å)/Si samples followed by low temperature furnace annealing (FA) or RTA process. The NiSi film serves as an energy barrier for

ion implantation and may act as a boron diffusion source. For the FA NiSi/p^+n junction diodes fabricated in this work, the junction depth ranges from 23 to 70 nm measured from the NiSi/Si interface, and the reverse bias current density of less than 2nA/cm^2 can be easily achieved. Specifically, the NiSi(310Å)/p^+n junction fabricated with a 35keV BF_2^+ implantation to a dose of $5\times10^{15}cm^{-2}$ followed by a 30 min thermal annealing (FA) at 600°C, has a forward ideality factor of 1.01, a reverse bias current density (at –5V) of less than 1 nA/cm^2, and a junction depth of 56nm. The activation energy measurements indicate that the reverse bias current of the NiSi/p^+n junctions with an area of 1100×1100 μm^2 is dominated by the diffusion current. The reverse bias current is composed of the reverse area leakage current and the reverse peripheral leakage current. For the diode's size smaller than 120×120 μm^2, the total reverse current would be contributed by the peripheral current dominated by the minority carrier generation current induced by the generation centers in and/or close to the junction region along the perimeter. For the RTA NiSi/p^+n junction diodes fabricated in this work, the junction depth ranges from 23 to 56 nm measured from the NiSi/Si interface, and the reverse bias current density of lower than 4 nA/cm^2 can be easily achieved. Specifically, the NiSi(310 Å)/p^+n junction fabricated with BF_2^+ implantation at 35 keV and a dose of 5×10^{15} cm^{-2} followed by a 30-sec-RTA at 650°C, has a forward ideality factor of 1.001, a reverse bias current density (at –5 V) of 0.6

nA/cm^2, and a junction depth of 37 nm. The activation energy measurements indicate that the reverse area leakage current (I_{RA}) is dominated by diffusion current at temperatures from 40 to 200^{o}C, while the reverse peripheral leakage current (I_{RP}) is easily dominated by the minority carrier generation current at temperatures below 80^{o}C. As a result, the total reverse current would be dominated by the minority carrier generation current induced by the generation centers in and/or close to the junction region along the perimeter for the junction diodes with an area smaller than 120×120 μm^2. Thus, the improvement and control of the peripheral leakage current is a critical issue of concern. The contact resistivity (ρ_c) of 5×10^{-8} Ω-cm^2 can be obtained for the NiSi/p$^+$n contact fabricated with BF_2^+ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by RTA at 750^{o}C.



6.1.3 NiSi/n$^+$p shallow junction

The NiSi-contacted n$^+$p shallow junctions are formed using ITS scheme by phosphorus ion (P^+) implantation into/through NiSi(615 Å)/Si sample followed by low temperature furnace annealing. A preferable dopant implantation scheme is to use P^+/F^+ dual implantation (P^+ implant followed by F^+ implant) instead of P^+ single implantation because the dual implantation is designed to promote the high temperature thermal stability of the NiSi film by the incorporation of fluorine atoms.

For the NiSi(615 Å)/n^+p shallow junctions studied in this work, the junction depth ranges from 61 to 149 nm measured from the NiSi/Si interface, and the reverse bias current density of less than 1 nA/cm^2 can be easily achieved. Specifically, the NiSi(615 Å)/n^+p junction fabricated with P^+/F^+ dual implantation at 35/30 keV to a dose of $5\times10^{15}/5\times10^{15}$ cm^{-2} followed by a 90 min thermal annealing at 750°C, has a forward ideality factor of 1.08, a reverse bias current density (at 5 V) of 0.7 nA/cm^2, and a junction depth of 71 nm. Activation energy measurement shows that the reverse bias area current is dominated by the diffusion current from 40 to 200°C, while the reverse bias peripheral current is dominated by the minority carrier generation current at temperatures below 100°C. This implies the presence of generation centers in and/or close to the junction region along the junction's perimeter. For the diode's size smaller than 120×120 μm^2, the total reverse current would be dominated by the minority carrier generation current induced by the generation centers in and/or close to the junction region along the perimeter.

6.1.4 Thermal stability of TaN/Cu/NiSi/p^+n junction diode

Thermal stability of the Cu-contacted TaN/Cu/NiSi/p^+n junction diode is investigated in terms of electrical characteristics measurements and various material analyses. The TaN/NiSi/p^+n junction is thermally stable up to at least 500°C (by

thermal annealing for 30 min). However, the Cu contacted TaN/Cu/NiSi(310 Å)/p^+n junction diode remains stable only up to a temperature of 350°C. SIMS analysis indicates that Cu started to penetrate into the NiSi-contacted shallow junction when the sample was annealed at 375°C, leading to a drastic increase in reverse bias leakage current. After annealing at 425°C, metallurgical reaction is evident from the top view and cross-sectional view SEM observations, and the XRD analysis indicates the formation of Cu_3Si silicide phase. The rapid growth of Cu_3Si silicide phase during the thermal annealing at 425°C resulted in the break of the TaN cover layer, causing the eventual collapse of the TaN/Cu/NiSi/Si structure.

6.2 Suggestion for future study

Although many material and electrical properties of nickel silicide pertaining to VLSI applications have been investigated in this work, there are many other important topics that are deserving of concentrated study. The following subjects are suggested for future research:

(1) Study on the contact resistance of NiSi/n^+p shallow junction fabricated by ITS scheme.

(2) Study on the thermal stability, doping technique, and contact resistivity of the NiSi/poly-Si structure. The effect of film stress of NiSi polycide gate on the gate

oxide integrity is also of great concern.

(3) Study on the application of NiSi as a metal gate structure.

(4) More comprehensive as well as in-depth study on the scheme of P^+/F^+ dual implantation.