Publication List

Journal Paper

1. [新--3 點，長文] **C. C. Wang**, C. J. Lin, and M. C. Chen, “Formation of NiSi-Silicided p^+n Shallow Junctions Using Implant-Through-Silicide and Low-Temperature Furnace Annealing”, *J. Electrochem. Soc.*, **150**, G557 (2003).

2. [新--2 點，長文] **C. C. Wang**, H. H. Lin, and M. C. Chen “Thermal Stability of Cu/NiSi Contacted p^+n Shallow Junction”, *Jpn. J. Appl. Phys.* 43, 5997 (2004).

3. [新--2 點，長文] **C. C. Wang**, Y. K. Wu, W. H. Wu, and M. C. Chen, “Formation of NiSi-Silicided p^+n Shallow Junctions Using Implant into/through Silicide and Rapid Thermal Annealing”, **accepted to appear in** *Jpn. J. Appl. Phys.*

4. [待審，長文] **C. C. Wang** and M. C. Chen, “Formation and Characterization of NiSi-silicided n^+p Shallow Junctions”, under reviewing in *J. Electrochem. Soc.*

Conference Paper

1. [新--1 點，短文]**C. C. Wang**, C. J. Lin, and M. C. Chen, “Formation of NiSi-silicided p^+n shallow junctions using implant through silicide and low temperature furnace annealing”, *CMOS Front-End Materials and Process Technology. Symposium (Mater. Res. Soc. Symposium Proceedings Vol. 765). Mater. Res. Soc. 2003, pp.235-40. Warrendale, PA, USA.*
2. **C. C. Wang**, and M. C. Chen “Formation and characterization of NiSi-silicided n^+p shallow junctions using implant through silicide and low temperature furnace annealing”, *Advanced Short-Time Thermal Processing for Si-Based CMOS Devices II(ECS* Symposium proceedings *of ECS Meeting*, (2004).

總發表點數：新-8 點