Material Properties and Process Technologies of Nickel Silicide Relevant To VLSI Applications

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Abstract

This dissertation studies the basic material properties and process technologies of nickel silicide relevant to VLSI applications. First, the thermal stability of nickel monosilicide (NiSi) is investigated, including the effect of fluorine atoms incorporation in the NiSi film. Second, high performance NiSi/p^+n and NiSi/n^+p shallow junctions formed by ITS scheme followed by low temperature furnace annealing and RTA process are investigated. In addition, contact resistance of the NiSi/p^+n junction is measured using a four-terminal Kelvin structure. Finally, we also investigate the thermal stability of the Cu-electrode contacted TaN/Cu/NiSi/p^+n

shallow junctions.

Thin NiSi silicide films of 315- and 615-Å thicknesses on Si substrate were used to investigate the thermal stability of NiSi films. It was found that the thermal stability of the NiSi film is dependent on the implant species and the implantation condition. Both BF_2^+ and F^+ implantations could improve the NiSi film's thermal stability, while B^+ and P^+ implantations might result in degrading the thermal stability. In the system of NiSi/Si, the implanted fluorine atoms are presumably segregated to the NiSi grain boundaries and NiSi/Si interface, forming the strong Si–F and Ni–F bonds, and thus suppressing NiSi film agglomeration by decreasing the interfacial energy, i.e. stress between the NiSi layer and the Si substrate; as a result, the integrity of the silicide layer is preserved at high temperatures.

The NiSi/p^+n shallow junctions were fabricated using ITS scheme by BF_2^+ implantation into/through NiSi(310 Å)/Si samples followed by low temperature furnace annealing (FA) or RTA process. For the FA NiSi/p^+n junction diodes fabricated in this work, the junction depth ranges from 23 to 70 nm measured from the NiSi/Si interface. The reverse bias current density of less than 2 nA/cm^2 can be easily achieved; specifically, the NiSi(310 Å)/p^+n junction fabricated with a 35keV BF_2^+ implantation to a dose of 5×10^{15} cm^{-2} followed by a 30-min-FA at 600^{o}C, has a forward ideality factor of 1.01, a reverse bias current density (at –5 V) of less than 1

nA/cm^2, and a junction depth of 56nm. For the RTA NiSi/p$^+$n junction diodes fabricated in this work, the junction depth ranges from 23 to 56 nm measured from the NiSi/Si interface. The reverse bias current density of lower than 4nA/cm^2 can be easily achieved; specifically, the NiSi(310 Å)/p$^+$n junction fabricated with a 35keV BF_2^+ implantation to a dose of 5×10^{15} cm^{-2} followed by a 30-sec-RTA at 650^{o}C, has a forward ideality factor of 1.001, a reverse bias current density (at –5 V) of 0.6 nA/cm^2, and a junction depth of 37 nm. The contact resistance of the NiSi-contacted p$^+$n junction fabricated using ITS scheme is measured by four terminal Kelvin test structure. The NiSi/p$^+$n contact fabricated with BF_2^+ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} through a 310Å-thick NiSi followed by 700 to 750^{o}C RTA exhibited a contact resistivity (ρ_c) of about 0.05 μΩ-cm^2. This low value contact resistivity is able to meet the requirement for future VLSI applications

A P$^+$/F$^+$ dual implantation (P$^+$ implant followed by F$^+$ implant) is designed to promote the high temperature thermal stability of the NiSi film for the formation of NiSi/n$^+$p shallow junctions. The NiSi(615Å)/n$^+$p junction fabricated with P$^+$/F$^+$ dual implantation at 35/30 keV to a dose of $5\times10^{15}/5\times10^{15}$ cm^{-2} followed by a 90min thermal annealing at 750^{o}C, has a forward ideality factor of 1.08, a reverse bias current density (at 5 V) of 0.7 nA/cm^2, and a junction depth of 71 nm. The additional F$^+$ implantation was able to improve the NiSi/Si interface morphology at high

temperatures, which is beneficial to the formation of high performance NiSi/n^+p shallow junctions.

The TaN/NiSi/p^+n junction diode was found to be thermally stable up to at least 500°C (by a 30 min thermal annealing). However, the Cu contacted TaN/Cu/NiSi(310 Å)/p^+n junction diode remained stable only up to a temperature of 350°C. SIMS analysis indicates that Cu started to penetrate into the NiSi-contacted shallow junction when the sample was annealed at 375°C, leading to a drastic increase in reverse bias leakage current. The rapid growth of Cu_3Si silicide phase during the thermal annealing at 425°C resulted in the break of TaN cover layer, causing the eventual collapse of the TaN/Cu/NiSi/Si structure.