Comprehensive Noise Characterization and Modeling for 65-nm MOSFETs for Millimeter-Wave Applications

Sheng-Chun Wang, Pin Su, *Member, IEEE*, Kun-Ming Chen, Kuo-Hsiang Liao, Bo-Yuan Chen, Sheng-Yi Huang, Cheng-Chou Hung, and Guo-Wei Huang, *Member, IEEE*

***Abstract*—Using an external tuner-based method, this paper demonstrates a complete millimeter-wave noise characterization and modeling up to 60 GHz for 65–nm MOSFETs for the first time. Due to channel length modulation, the channel noise continues to increase and remains the most important noise source in the millimeter-wave band. Our experimental results further show that, with the downscaling of channel length, the gate resistance has more serious impact on the high-frequency noise parameters than the substrate resistance even in the millimeter-wave frequency.**

***Index Terms*—Millimeter wave, MOSFET, noise, RF.**

I. Introduction

WITH THE downscaling of channel length into deep-submicrometer regime, RF MOSFETs have become good choices for millimeter-wave applications [1]. Although RF noise characterization and modeling for deep-submicrometer MOSFETs have been widely studied, the operating frequencies were mostly limited to several gigaherz and may not be enough for millimeter-wave applications. Therefore, there is an urgent need to characterize and model the noise behaviors up to millimeter-wave frequencies. Although Waldhoff *et al.* [2] have shown noise parameters covering the millimeter-wave regime, their results were based on the F50 method [3] that may not be accurate enough due to its approximations for noise parameter extraction.

In this paper, to more accurately obtain and model the millimeter-wave noise behaviors, the tuner-based method is used instead. With the help of tuner-based Auriga noise and scattering parameter measurement system [4], a complete millimeter-wave noise characterization and modeling for MOSFETs fabricated in 65-nm technology can be achieved. Note that contrary to the *in-situ* tuner based technique [5], [6], the Auriga measurement system uses an external tuner to avoid the pre-design, characterization, and deembedding of the on-die tuner, and maintains reasonable measurement results.

This paper is organized as follows. Section II describes the device geometries and de-embedding method used in this work. The noise equivalent circuit is also addressed. Section III shows the intrinsic noise sources and their gate length dependence. The modeling results and the impact of gate and substrate resistances on the noise parameters are discussed in Section IV. Finally, we will make conclusions in Section V.

Manuscript received July 29, 2009; revised September 29, 2009. First published March 08, 2010; current version published April 14, 2010. This work was supported in part by the National Science Council of Taiwan.

S.-C. Wang is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, and also with National Nano Device Laboratories, Hsinchu 300, Taiwan (e-mail: scwang@ndl.org.tw).

P. Su is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: pinsu@mail.nctu.edu.tw).

K.-M. Chen, K.-H. Liao, B.-Y. Chen, and G.-W. Huang are with the National Nano Device Laboratories, Hsinchu 300, Taiwan (e-mail: kmchen@ndl.org.tw; khliao@ndl.org.tw; bychen@ndl.org.tw; gwhuang@ndl.org.tw).

S.-Y. Huang and C.-C. Hung are with the United Microelectronics Corporation, Hsinchu 300, Taiwan (e-mail: Samny_Huang@umc.com; Bigchoug_Hung@umc.com).

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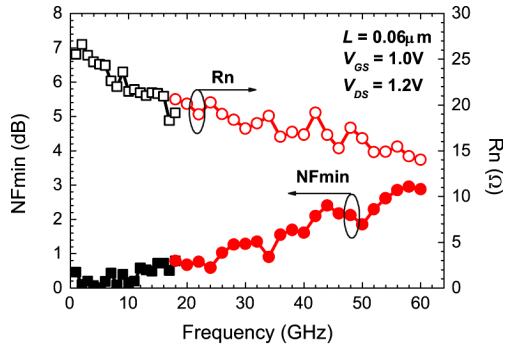
Digital Object Identifier 10.1109/TMTT.2010.2041582

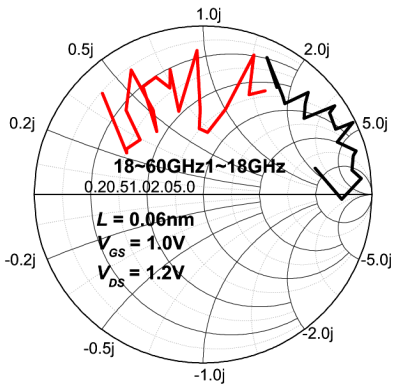
II. Devices and Experiments

The devices used in this paper were fabricated by UMC 65-nm technology process and laid out in multifingers and multigroups structure with two sided gate access. The number of fingers and groups are eight and four, respectively, and finger length is 4 μm, which might not be optimized for millimeter-wave applications. The scattering (S) and noise parameters (minimum noise figure $\mathrm{NF}_{\min}$, equivalent noise resistance R_n, magnitude of optimum source reflection coefficient $|\Gamma_{\mathrm{opt}}|$, and phase of optimum source reflection coefficient $\angle\Gamma_{\mathrm{opt}}$) from 18 to 60 GHz were measured using Auriga noise and scattering parameter measurement system, and the dummy OPEN and SHORT de-embedding technique was used to eliminate the parasitic contributions from the probing pads and metal interconnections [7]. The Auriga system was carefully calibrated and the accuracy of measurement results were confirmed by the widely used 18-GHz ATN noise and scattering parameter measurement system, as shown in Fig. 1. The good agreement between the extracted channel noise and its theoretical value for a cold device shown in Fig. 1(c) also validates measurement reliability.

The equivalent circuit shown in Fig. 2 was used to characterize devices' noise behaviors, and its small-signal model elements were carefully extracted using the approach presented in [8]. In this figure, the input resistance R_i and phase delay τ are essential in describing the intrinsic small-signal behaviors when operating frequencies approach cutoff frequency (f_t), and the junction capacitance $C_{j,db}$ along with substrate resistance R_b are used to model the RF substrate loss. In addition, the series inductances (L_s, L_d, and L_g) are pronounced for the high-frequency operation. Therefore, these elements must be considered



(a)



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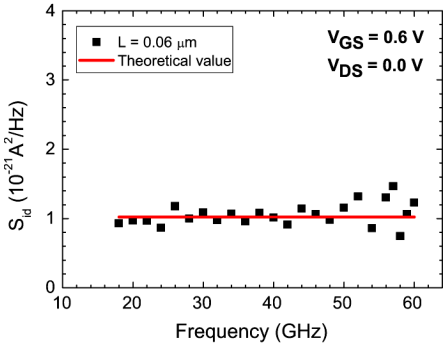


(c)

Fig. 1. Broadband (1–60 GHz) noise parameters. (a) $\mathrm{NF}_{\min}$ and R_n versus frequency plot. (b) Γ_{opt} in a Smith chart. The data below 18 GHz were measured by an ATN system, while above were measured by an Auriga system. (c) Good agreement between extracted channel noise and its theoretical value for a cold device.

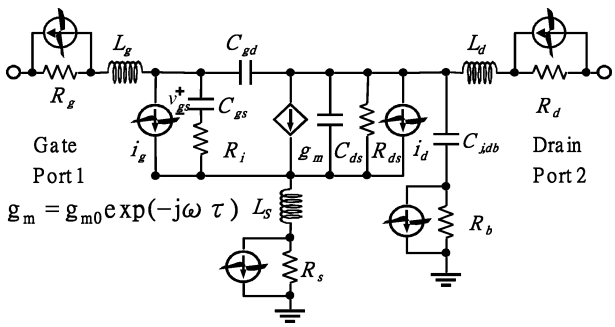
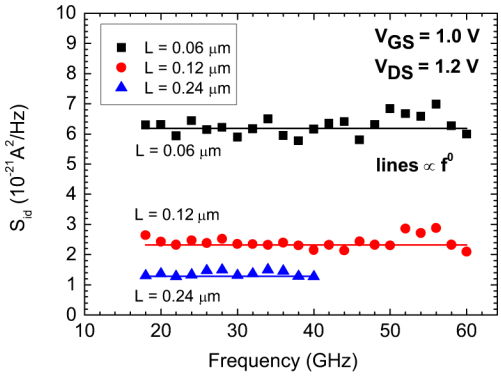


Fig. 2. RF noise equivalent circuit for bulk MOSFETs.

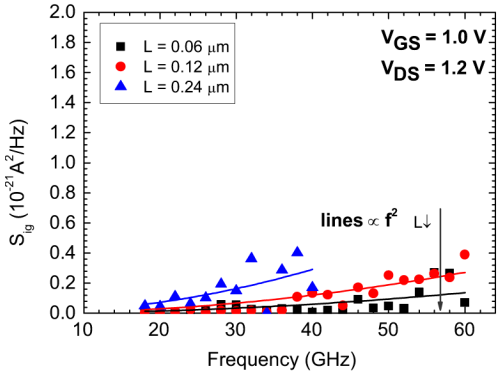
when it comes to millimeter-wave characterization and modeling. Table I shows the intrinsic small-signal parameters that

TABLE I
EXTRACTED INTRINSIC SMALL-SIGNAL PARAMETERS THAT CAN BENEFIT THE CHARACTERIZATION OF THE NOISE PARAMETERS

L (μm)	R_i (Ω)	g_m (mS)	C_{gs} (fF)	C_{gd} (fF)	τ (ps)
0.06	6.8	151.8	71.3	36.4	0.2
0.12	3.4	106.9	146.3	42.4	0.7
0.24	3	74.8	317.2	47.6	1.2



(a)



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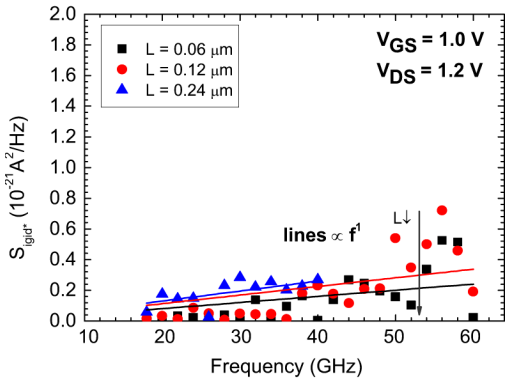

(c)

Fig. 3. Extracted: (a) S_{id}, (b) S_{ig}, and (c) S_{igid^*} versus frequency. The solid lines show the frequency dependence.

can benefit the characterization of the noise parameters. Besides, since the gate current is about or smaller than 1 nA, its associated incremental resistance ($> 100\ \mathrm{M}\Omega$) and shot noise ($\approx 10^{-28}\ \mathrm{A}^2/\mathrm{Hz}$) are neglected in this model.

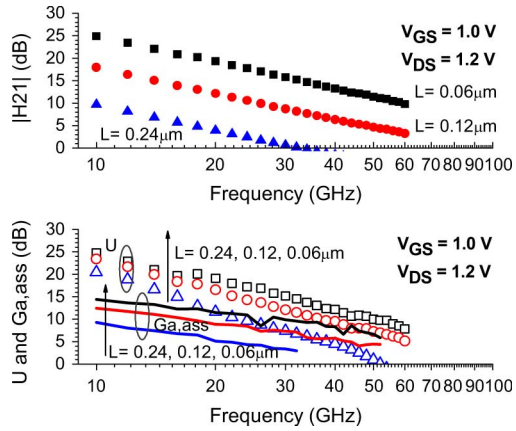

Fig. 4. Short-circuited current ($|H_{21}|$) gain, unilateral power gain (U), and associated gain ($G_{a,ass}$) versus frequency.

III. Channel Noise Source Characterization and Modeling

Fig. 3 shows the extracted power spectral density (PSD) for channel noise i_d, induced gate noise i_g, and imaginary part of cross correlation component (denoted as S_{id}, S_{ig}, and S_{igid^*}, respectively). To obtain these intrinsic PSDs, the noise contributions from the parasitic series and substrate components were eliminated following the approach presented in [9]. S_{id} is shown to be frequency independent, and S_{ig} and S_{igid^*} to be proportional to f^2 and f, respectively. These relations agree with the van der Ziel model [10]. Besides, our extracted results coincide with the previous findings that with the channel length scaling, S_{id} are expected to increase, while S_{ig} and S_{igid^*} are expected to decrease [9], [11] due to the smaller oxide capacitance coupling [12]. Note that due to the smaller power gain, and hence, the larger inaccuracy in noise measurement, the upper measurement frequency is limited to 40 GHz for the $L = 0.24$ μm device. The short-circuit current gain ($|H_{21}|$), unilateral power gain (U), and associated gain ($G_{a,ass}$) versus frequency are also shown in Fig. 4 for the reader's reference.

Traditionally, S_{id} can be expressed as [10], [12]

$$S_{id} = 4k_B T \gamma g_{d0} \tag{1}$$

where $k_B \approx 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, T is the ambient temperature in kelvin, g_{d0} is the channel conductance at zero drain–source voltage, and γ is the noise factor. The extracted noise factor versus channel length is depicted in Fig. 5, which shows that γ continues to increase with decreasing channel length.

Asgaran *et al.* [13] have developed an analytical expression for S_{id} based on the classical thermal noise theory with taking the channel length modulation into account

$$S_{id} = 4k_B T I_D \left(\frac{1}{V_{D,\text{sat}}} + \frac{\alpha^2 V_{D,\text{sat}}}{3V_{GT}^2} \right) \approx \frac{4k_B T I_D}{V_{D,\text{sat}}} \tag{2}$$

where $V_{D,\text{sat}}$ is the drain saturation voltage at which the carriers start to travel with their saturation velocity, V_{GT} is the gate overdrive voltage, and α is the bulk charge coefficient. The approximation is especially valid for shorter devices with smaller $V_{D,\text{sat}}$. The extracted and modeled S_{id} versus drain current I_D for different channel sizes are shown in Fig. 6. In our experiments, the values for $V_{D,\text{sat}}$ under a given gate bias V_{GS} were extracted by linear extrapolation in the output resistance versus drain bias plot [14], and the $V_{D,\text{sat}}$ extraction results are also shown in Fig. 7.

According to this model [13], devices with smaller $V_{D,\text{sat}}$, which means more channel length modulation in the channel, would exhibit larger channel noise. As shown in Fig. 7, since $V_{D,\text{sat}}$ continuously decreases with downscaling channel length, one can expect that S_{id} would continue to increase, as shown in Fig. 6. Since (2) was a purely thermal noise based

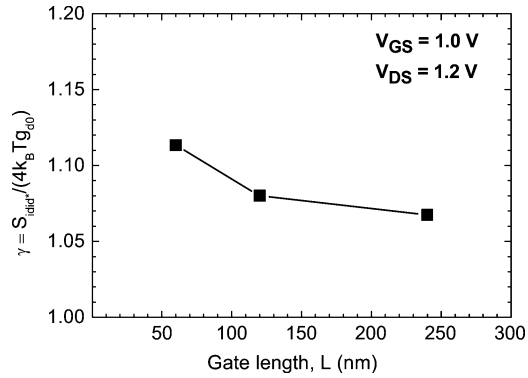

Fig. 5. Noise factor γ versus gate length.

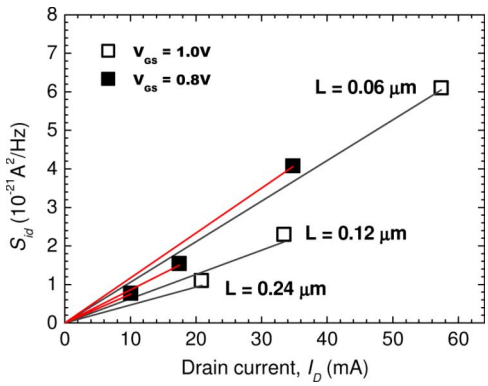

Fig. 6. Extracted channel noises (symbols) and their theoretical values (lines) calculated using (2) versus drain current.

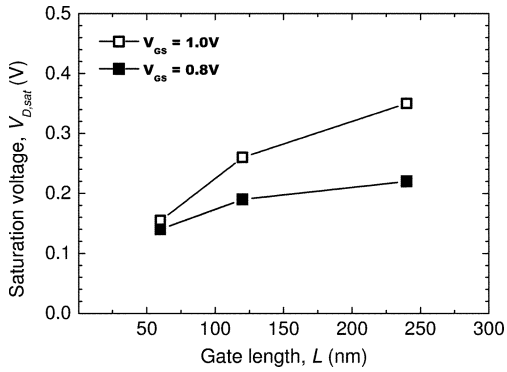

Fig. 7. Saturation voltage versus channel length.

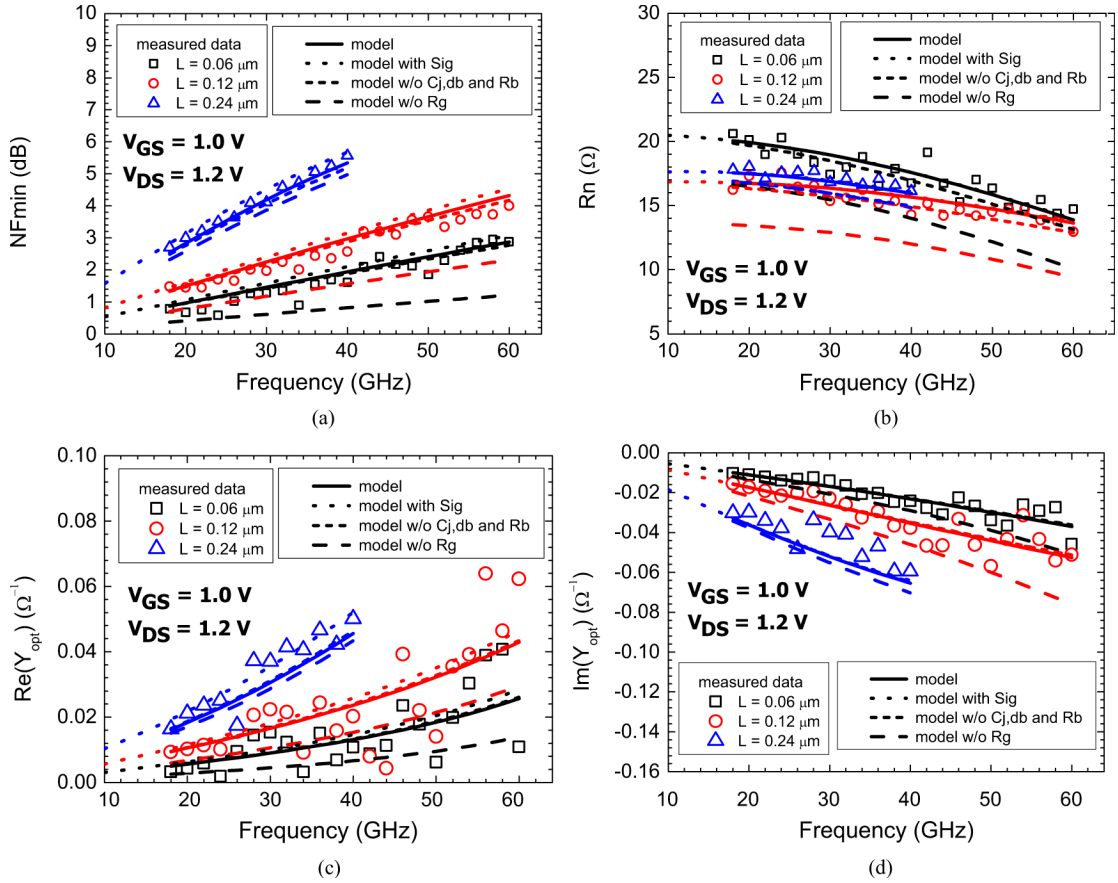

Fig. 8. Modeled: (a) $\mathrm{NF}_{\min}$, (b) R_n, (c) G_{opt}, and (d) B_{opt} versus frequency. The impact of S_{ig}, gate resistance, and substrate resistance on these noise parameters are also shown in this figure.

model, the good channel noise modeling results also imply that the shot noise is not significant at 65-nm technology node, which agrees with the results shown in [15]. This also explains the increase of noise factor γ with the downscaling of the channel length.

IV. Noise Parameter Characterization and Modeling

Based on the equivalent circuit shown in Fig. 2, and the channel noises extracted in Section III, the noise parameters were simulated using Agilent Technologies' Advanced Design System (ADS). Note that the noise sources associated with series resistances (R_g, R_s, and R_d) and substrate resistance (R_b) are considered as thermal noise, and their PSDs can be expressed as $4k_BT/R$, where R is the resistance value. In addition, for simplification, we have neglected S_{ig} and S_{igid^*}, as in [16]. To validate the assumption for millimeter-wave modeling, both the modeling results with and without considering S_{ig} are shown in Fig. 8 for comparison. This figure shows that without considering S_{ig}, the errors are still within acceptable range, especially for $L = 0.12$ and $L = 0.06$ μm devices, and this supports the approximation we used in the millimeter-wave modeling. Besides, since the $L = 0.24$ μm device is not suitable for millimeter-wave application due to its low cutoff frequency f_t and maximum oscillation frequency $f_{\max}$, as implied in Fig. 4, the larger errors in $\mathrm{NF}_{\min}$ and G_{opt} for this device may not be a concern for millimeter-wave applications.

A. Intrinsic Noise Parameters

Neglecting S_{ig} and S_{igid^*}, the intrinsic noise parameters can be expressed as follows:

$$R_{n,\mathrm{int}} = \frac{S_{id}}{4k_BT_0\left(g_m^2+\omega^2C_{\mathrm{gd}}^2\right)} \tag{3}$$

$$G_{\mathrm{opt,int}} = \mathrm{Re}\left(\frac{1-\Gamma_{\mathrm{opt,int}}}{1+\Gamma_{\mathrm{opt,int}}}\right) \approx \frac{\omega^2C_{\mathrm{gs}}^2R_i}{1+\omega^2C_{\mathrm{gs}}^2R_i^2} \tag{4}$$

$$B_{\mathrm{opt,int}} = \mathrm{Im}\left(\frac{1-\Gamma_{\mathrm{opt,int}}}{1+\Gamma_{\mathrm{opt,int}}}\right) \approx -\omega\left(C_{\mathrm{gs}}+C_{\mathrm{gd}}\right) \tag{5}$$

$$\begin{aligned}\mathrm{NF}_{\mathrm{min,int}} &\approx 1+4R_{n,\mathrm{int}}G_{\mathrm{opt,int}} \\ &\approx 1+\frac{S_{id}}{k_BT_0\left(g_m^2+\omega^2C_{\mathrm{gd}}^2\right)}\frac{\omega^2C_{\mathrm{gs}}^2R_i}{1+\omega^2C_{\mathrm{gs}}^2R_i^2}\end{aligned} \tag{6}$$

where subscript int denotes the intrinsic part and $T_0 = 290$ K is the reference temperature.

A good figure of merit (FOM) to judge the intrinsic noise performance is $S_{id/\left(g_m^2+\omega^2C_{\mathrm{gd}}^2\right)} \approx S_{id}/g_m^2$. According to (3), lower S_{id}/g_m^2 can lead to smaller $R_{n,\mathrm{int}}$, which can benefit the input matching for circuit design. Fig. 9 depicts S_{id} and $R_{n,\mathrm{int}}$

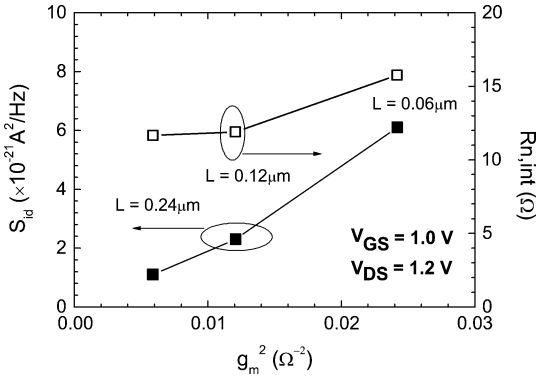

Fig. 9. S_{id} and $R_{n,\mathrm{int}}$ versus g_m^2.

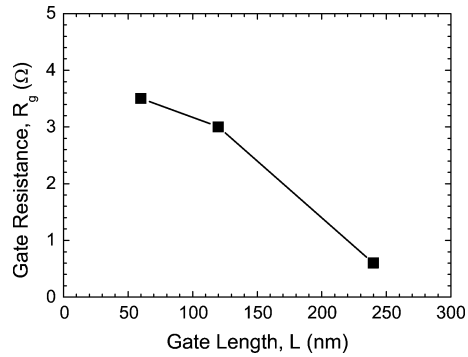

Fig. 10. Extracted gate resistance (R_g) versus channel length.

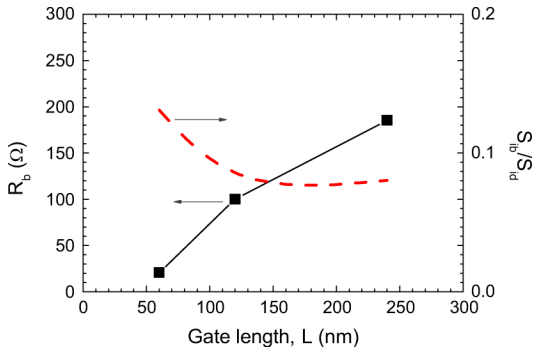

Fig. 11. R_b and S_{ib}/S_{id} versus gate length.

versus g_m^2 for different channel lengths. It shows that with length scaling down, the increase of the channel noise tends to overwhelm the increase of g_m^2, and in turn, degrades $R_{n,\mathrm{int}}$.

B. Impact of Gate Resistance on Noise Parameters

It has been shown that the gate resistance has a significant impact on the noise parameters and cannot be ignored in deep-submicrometer noise modeling [16], [17]. In fact, as the gate resistance exists, the total expressions for noise parameters have the following relations to the intrinsic ones:

$$R_n \approx R_{n,\mathrm{int}} + \frac{T}{T_0} R_g \tag{7}$$

$$B_{\mathrm{opt}} \approx \frac{R_{n,\mathrm{int}}}{R_n} B_{\mathrm{opt,int}} \tag{8}$$

$$G_{\mathrm{opt}} \approx \sqrt{\left(\frac{R_{n,\mathrm{int}}}{R_n}\right)\left(G_{\mathrm{opt,int}}^2 + B_{\mathrm{opt,int}}^2\right) - \left(\frac{R_{n,\mathrm{int}}}{R_n}\right)^2 B_{\mathrm{opt,int}}^2} \tag{9}$$

$$\mathrm{NF}_{\min} \approx 1 + 2R_n G_{\mathrm{opt}} + 2R_g R_{n,\mathrm{int}}\left(G_{\mathrm{opt,int}}^2 + B_{\mathrm{opt,int}}^2\right). \tag{10}$$

These equations suggest that the gate resistance would highly increase equivalent thermal resistance and minimum noise figure. In addition, since the gate resistance is significant in shorter devices, as shown in Fig. 10, its impact on their noise parameters is expected to be more serious. This is also confirmed in Fig. 8, where a larger error can occur in the shorter device without considering the gate resistance.

Note that for cases where R_s is comparable or even larger than R_g, as in [16], more accurate equations can be obtained by replacing R_g with $R_g + R_s$ in (7)–(10). Besides, the value of R_g can be changed as the used gate materials, number of gate fingers, and gate layout dependency. Therefore, the effect of R_g on the noise parameters can be varied at different cases.

C. Impact of Substrate Resistance on Noise Parameters

Reference [18] has considered the effect of substrate resistance (R_b) on high-frequency noise modeling. The modeling results without considering the substrate resistance are also shown in Fig. 8. This figure shows, however, as compared to R_g, the substrate resistance R_b has a much smaller influence on noise parameters. To explain this, one can find that at very high frequency, the drain-side noise current's PSD can be approximated by $S_{id} + S_{ib}$, where $S_{ib} = 4k_BT/R_b$ is the noise current PSD for the substrate resistance. As shown in Fig. 11, based on the extracted values of R_b, S_{ib} is about 1/10 of S_{id} at the very high frequency and can be ignored. That is, in millimeter-wave frequencies, the overall noise performance would be mainly dominated by S_{id} and R_g.

V. Conclusions

We have demonstrated the millimeter-wave noise characterization and modeling for 65-nm MOSFETs based on the tuner method for the first time. Our experimental results show that with the continuous down scaling of channel length, the channel noise S_{id} would remain the dominant noise source in the intrinsic part of the device, and can be predicted by the traditional thermal noise theory. The sharply increased S_{id} also degrades R_n.

Finally, the millimeter-wave noise modeling is achieved. With the help of circuit simulation, the impact of R_g and R_b on the noise parameters has been examined. Compared to R_b, R_g is shown to have a more serious influence on the noise parameters, and needs to be included in the millimeter-wave noise modeling.

Acknowledgment

The authors would like to thank the United Microelectronics Corporation (UMC), Hsinchu, Taiwan, for providing the devices used in this study. The authors would also like to thank Dr. D. Wandrei, Auriga Microwave, Lowell, MA, for his technical support.

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Sheng-Chun Wang received the B.S. and M.S. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1999 and 2001, respectively, and is currently working toward the Ph.D. degree at Chiao Tung University, Hsinchu, Taiwan.

In 2001, he joined the National Nano Device Laboratories, Hsinchu, Taiwan, as an Assistant Researcher. His current research interests focus on small-signal and noise characterization and modeling for RF CMOS devices.

Pin Su (S'98–M'02) received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, and the Ph.D. degree in electrical engineering and computer sciences from the University of California at Berkeley.

From 1997 to 2003, he conducted his doctoral and postdoctoral research in silicon-on-insulator (SOI) devices at the University of California at Berkeley. He was also one of the major contributors to the unified BSIMSOI model, the first industrial standard SOI MOSFET model for circuit design. Since August 2003, he has been with the Department of Electronics Engineering, National Chiao Tung University, where he is currently an Associate Professor. His research interests include silicon-based nanoelectronics, modeling and design for advanced CMOS devices, and device/circuit interactions in nano-CMOS. He has authored or coauthored over 90 research papers in refereed journals and international conference proceedings.

Kun-Ming Chen received the M.S. degree and Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1996 and 2000, respectively.

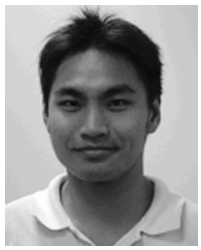
In 2000, he joined the National Nano Device Laboratories, Hsinchu, Taiwan, as an Associate Researcher, and in 2007 became a Researcher. He has been engaged in research on the microwave device process and characterization.

Kuo-Hsiang Liao received the M.S. degree in electronic engineering from the National Changhua University of Education, Taiwan, Taiwan, in 2005.

In 2005, he joined the National Nano Device Laboratories, Hsinchu, Taiwan, as an Assistant Researcher. He has been engaged in research on RF device characterization and modeling.

Bo-Yuan Chen was born in Miaoli, Taiwan, in 1980. He received the M.S. degree in materials science and engineering from National Dong Hwa University, Hualien, Taiwan, in 2006.

In 2006, he joined National Nano Device Laboratories, Hsinchu, Taiwan, as an Assistant Researcher. He has been engaged in research on III–V compound semiconductors and RF device characterization.

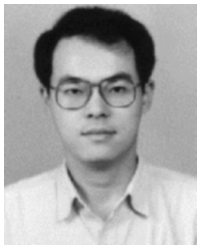


Sheng-Yi Huang received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2001, and the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University Hsinchu, Taiwan, in 2003 and 2007, respectively.

Since 2003, he has been with the Advanced Technology Development Division, United Microelectronics Corporation (UMC), Hsinchu, Taiwan, where he is involved with RF-related technologies. His current research focuses on advanced mixed-mode and RF CMOS design including device modeling, noise characterization, power behavior, and reliability studies.

Cheng-Choug Hung received the B.S. and M.S.E.E. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1996 and 1999, respectively.

He is currently with the Advanced Technology Department, United Microelectronics Corporation (UMC), Hsinchu, Taiwan, as an RF Device Development Manager. His current responsibility and research focuses on RF CMOS technology characterization/delivery including active and passive devices.



Guo-Wei Huang (S'94–M'97) was born in Taipei, Taiwan, in 1969. He received the B.S. degree and Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1991 and 1997, respectively.

In 1997, he joined National Nano Device Laboratories (NDL), Hsinchu, Taiwan, where he is currently a Researcher and Manager of the High-Frequency Technology Division. Since August 2008, he has been an Adjunct Associate Professor with the Department of Electronics Engineering, National Chiao Tung University. His current research interests focus on characterization and modeling techniques of high-frequency devices, and characterization and verification of RF integrated circuits (RFICs)/monolithic microwave integrated circuits (MMICs).