

air would show a linear dependence vs. the hydrogen partial pressure with a slope equal to the oxygen reduction Tafel-like slope.

We conclude from these preliminary results that acid-doped PBI can be used as the membrane in a hydrogen sensor, at room temperature even in dry air. The sensing electrode potentiometric response is based on the mixed potential concept.

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REFERENCES

1. R. V. Kumar and D. J. Fray, *Sens. Actuators*, **15**, 185 (1988).
2. N. Miura, T. Harada, and N. Yamazoe, *This Journal*, **136**, 1215 (1989).
3. Z. Samec, F. Opekar, and G. J. E. F. Crijns, *Electroanalysis*, **7**, 1054 (1995).
4. N. Miura and N. Yamazoe, in *Chemistry of Solid State Materials: Proton Conductors*, P. Colomban, Editor, p. 527, Cambridge University Press, Cambridge (1992).
5. J. T. Wang, R. F. Savinell, J. Wainright, M. Litt, and H. Yu, *Electrochim. Acta*, **41**, 191 (1996).
6. S. R. Samms, S. Wasmus, and R. F. Savinell, *This Journal*, **143**, 1225 (1996).
7. N. Miura and N. Yamazoe, in *Chemical Sensor Technology*, Vol. 1, T. Seiyama, Editor, p. 123, Elsevier, Amsterdam (1988).

Ultrathin N₂O-Oxide with Atomically Flat Interfaces

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ABSTRACT

Silicon oxide has been grown in a low pressure furnace using N₂O. An atomically flat SiO₂ (N₂O)/Si interface, as determined by high resolution transmission electron microscopy, has been achieved by desorbing the native oxide *in situ* for oxide thicknesses 11 to 38 Å. The thickness variation of a 20 Å N₂O-oxide, grown on a 4 in. substrate <1 Å. The excellent uniformity is attributed to the increased mean-free path of N₂O molecules in the low pressure environment. Since only one Si plane was distorted beneath the N₂O-oxide/Si interface, this suggests that thermal stress is not the limiting factor for obtaining an atomically smooth interface.

Introduction

Recently, much attention has been given to scaling down the thickness of gate oxides¹⁻⁷ because of the potential application for the next generation of high performance transistors and integrated circuits.⁸⁻¹⁰ As the thickness of the oxide is reduced, both the current drive capability and the transconductance of metal oxide semiconductor field-effect transistors (MOSFETs) increases. A MOSFET fabricated with a 15 Å direct-tunneling oxide has demonstrated excellent performance with a current drive more than 1.0 mA/μm and a transconductance of over 1000 mS/mm.⁹ The high current at a low bias voltage can ensure that transistors and circuit operate at or below 1 V, which is desirable for wireless communications.^{8,10} Further, hot-carrier reliability is shown to improve as the thickness of the oxide is reduced, because of the reduced probability of impact ionization and improved charges detrapping in the ultrathin gate oxide.^{8,11} However, the key issue in achieving good device performance made by the ultrathin gate oxide is the thickness uniformity and the interface smoothness. Large gate leakage currents can occur at local thickness variations in the oxide and a smooth interface is essential for higher carrier mobilities.¹² The reliability of the gate oxide also decreases with local thickness variation, where a high electric field and leakage current accelerate oxide breakdown. Unfortunately, it is difficult to achieve this goal; a native oxide formed by water absorption usually roughens the initial surface. Recently, a closed wet cleaning (CWC) under ultradry nitrogen (N₂) environment was proposed to achieve this goal, and the reliability of the oxide was shown to be improved significantly.¹³ The higher reliability is due to the H-termi-

nated Si surface without native oxide growth. The H-terminated Si surface is effective at reducing the tunneling current of the ultrathin oxide.³ We report here the design of a low-pressure oxidation system to desorb the native oxide *in situ* before thermal oxidation. A leakproof system design and high flow rate of hydrogen (H₂) are used to maintain the low level of moisture and oxygen inside the reactor and to avoid further oxidation before desorbing the native oxide. Studies by high-resolution transmission electron microscopy (TEM) show that an atomically smooth interface between oxide and Si can be obtained for oxide thicknesses of 11 to 38 Å.

Experimental

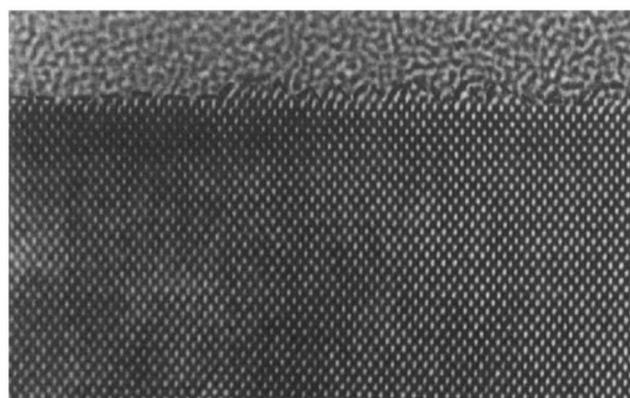
The low-pressure oxidation system is similar to a conventional oxidation furnace but with a leakproof system design. A simple rotary pump is used, and an oil trap is installed to ensure no oil contamination during desorption of the native oxide. A minimum pressure of ~10 mTorr was obtained with the rotary pumped, low-pressure oxidation furnace. The combination of a leakproof reactor and a high flow rate of H₂ purge has been used to minimize further oxidation of the Si, whereas a rough interface may result from the initial microroughness between the native oxide and the Si substrate. A similar leakproof technique has been used in low-pressure chemical vapor deposition (LPCVD) to grow high quality Si epitaxy at 550°C.¹⁴ A 4 in. p-type [100] Si wafer was used for the oxidation study. The cleaning procedure consisted of a 1:4 H₂SO₄/H₂O₂ etching, a modified RCA cleaning, and dipping in a 0.5% HF solution. A 5% NH₄OH was used in the modified RCA to achieve a smooth surface before oxidation.¹⁵ The dilute HF solution removed the oxide and produced a H-terminated, smooth sur-

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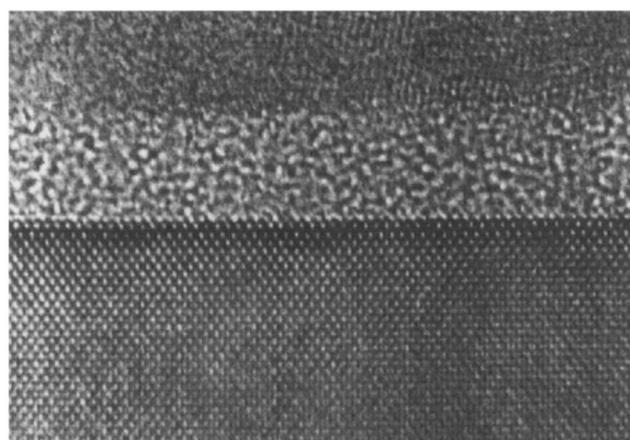
face.^{16,17} The furnace was maintained at 300°C during wafer loading with a flow rate of 5 liter/min N₂ to minimize the moisture and oxygen content in the furnace. The desorption of hydrogen is negligible at this temperature,¹⁸ while incorporation of moisture and oxygen from air into the furnace was reduced. After wafer loading, the system was evacuated to its minimum pressure, and a constant purge of pure H₂ 6 liter/min was used to reduce the moisture and oxygen in the chamber. The furnace temperature was ramped to between 950 and 1000°C, at a rate of 10°C/min, where the native oxide was desorbed. The time for native oxide desorption was 30 min under the H₂ environment. Samples without desorption of the native oxide by directly ramping to the desired growth temperature were studied for comparison. Growth of oxynitride by N₂O at temperatures varying from 900 to 1000°C have been investigated. The typical ramp down time from 950°C for native oxide desorption to 900°C for oxidation was 10 min. During growth, the N₂O flow rate was 100 sccm, and the reactor pressure was controlled by a throttle valve to maintain a constant pressure of 4.5 Torr. This low pressure slows the growth rate and improves uniformity. Further, a slower growth rate is easier to control and thus achieve an ultrathin oxide. The thickness variation across a 4 in. wafer was less than 1 Å for a 20 Å thick oxide, as measured by an ellipsometer with a refractive index set to 1.46. After the oxide was grown, the wafer was loaded into the LPCVD reactor to deposit poly-Si. A 2000 Å thick poly-Si was grown at 550 or 500°C by silane or disilane, respectively. Cross-sectional TEM, viewed from the [110] cleave plane, was used to investigate the interface roughness between oxide and Si.

Results and Discussion

Figure 1a and b shows the lattice images of 900°C-grown N₂O-oxide/Si from conventional oxidation and low-pressure oxidation



50 Å



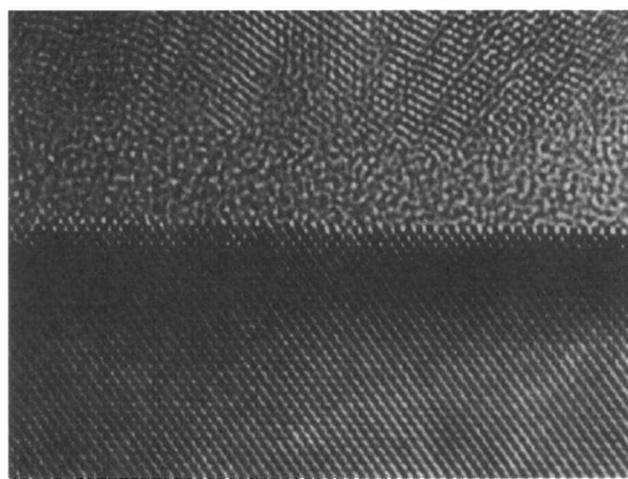
50 Å

Fig. 1. Cross-sectional TEM images of 900°C-grown N₂O-oxide/Si from (a, top) conventional oxidation and (b, bottom) low-pressure oxidation with a cleaned surface. The dark lines in (a), added by hand, are to enhance the contrast of the interface between the oxide and Si.

with a cleaned surface, respectively. For conventional furnace oxidation in Fig. 1a, microroughness up to two monolayers was observed. The relatively sharp interfaces of the oxide/Si interface may be due to the surface preparation. In contrast, atomically flat N₂O-oxide/Si interface was observed for the *in situ* surface cleaned before oxidation (Fig. 1b), with an oxide thickness of 38 Å. The abrupt interface obtained at a low oxidation temperature of 900°C is important to decreasing the thermal budget; a much higher temperature of 1200°C was reported previously to obtain an interface roughness of 1.7 Å.⁴ The top interface between poly-Si and oxide cannot be distinguished clearly, which is due to the different crystalline orientations between the polygrains and the single crystal substrate. However, because the growth of oxide is due to the consumption of Si, the atomically flat interface indicates the thickness of oxide should be uniform.

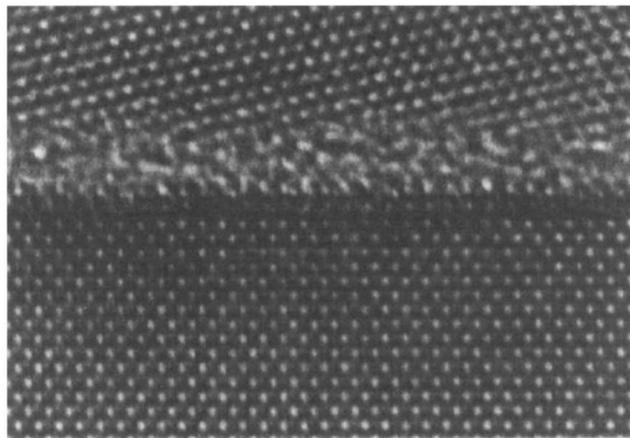
The atomically smooth interface of the oxide/Si interface may be due to either the low-pressure growth condition or the internal desorption of the native oxide. To further identify the origin of the smooth interface, we have grown another sample at the same condition but without the high temperature to desorb the native oxide. Figure 2 shows the lattice image of the sample by directly ramping to 900°C under the same low-pressure oxidation. The thickness of N₂O-oxide was 20 Å. The microroughness was improved, as compared to conventional oxidation shown in Fig. 1a, however the interface was still not as sharp as the one with desorbed native oxide (Fig. 1b). Because the same growth conditions have been used, the degraded interface smoothness should be related to the native oxide desorption. It is reported that nucleation of regrowing oxide, during the short time of air exposure, is attributed to the slightly higher oxygen content in a H-terminated (111) surface,¹⁹ that is atomically smoother and chemically more homogeneous than that of (100).²⁰ Furthermore, the higher performance of the oxide grown in the CWC/N₂ environment suggests that the H-terminated (100) surface may form a native oxide after air exposure.¹³ Therefore, the microroughness of a H-terminated (100) Si surface may originate from native oxide regrowth through weak spots. The formation of native oxide on H-terminated (100) Si was also found in an LPCVD epitaxial growth study with an HF vapor treatment.²¹ The reason why low-pressure oxidation can achieve better interface smoothness than that of conventional atmosphere pressure oxidation is due to the leakproof furnace design reducing the further growth of native oxide through the weak spots. The possible reason for a smoother interface, after desorbing the native oxide, may be due to the migration of surface Si atoms. A similar smooth surface was observed after desorption of the native oxide in an ultrahigh-vacuum environment.^{6,22}

To further demonstrate the thickness control and smoother interface between the oxide and Si for the low-pressure oxidation, we have grown an ultrathin oxide with a thickness of 11 Å. As shown in Fig. 3, an atomically flat interface was obtained at a growth temperature of 900°C. There was only one atomic plane, just beneath the oxide, which was distorted from its original lattice position. This



50 Å

Fig. 2. Cross-sectional TEM image of N₂O-oxide/Si by directly ramping to 900°C under a similar low-pressure oxidation condition. The thickness of N₂O-oxide is 20 Å.



20 Å

Fig. 3. Cross-sectional TEM image of 11 Å N_2O -oxide grown on Si at 900°C. An atomically flat interface is obtained, and only one atomic plane, just beneath the oxide, is distorted from its original lattice side.

is due to the translation from single crystal Si to amorphous oxide. The equivalent thickness of oxide is equal to 3.5 Si atomic layers, whereas only 2 atomic layers of Si were consumed to form the oxide. This is an indication that an atomic smooth Si surface can be achieved after the desorption of the native oxide.

Conclusion

We have shown that an atomically flat interface of oxide/Si can be obtained for oxide thickness in a range of 11 to 38 Å. The success of growing an abrupt interface without local microroughness is due to the combination of good surface cleaning, H-passivated surface, leakproof system design, and desorption of the native oxide. The concept of desorption of the native oxide at low-pressure and leakproof oxidation environment can be applied to rapid thermal oxidation where a lower thermal budget is used.

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REFERENCES

1. G. Q. Lo, W. Ting, J. Ahn, and D. L. Kwong, in *Symposium on VLSI, Tech. Dig.*, 43 (1991).
2. C. T. Liu, K. P. Cheung, C. P. Chang, L. Fritzing, J. Becerro, H. Luftman, H. M. Vaidya, J. I. Colonell, A. Kamgar, J. F. Minor, R. G. Murray, W. Y. C. Lai, C. S. Pai, and S. J. Hillenius, in *Symposium on VLSI, Tech. Dig.*, 18 (1996).
3. M. Hao, K. Lai, W.-M. Chen, and J. C. Lee, *Tech. Dig. Int. Electron Devices Meet.*, 601 (1994).
4. M. L. Green, D. Brasen, K. W. Evans-Lutterodt, L. C. Feldman, K. Krisch, W. Lennard, H. T. Tang, L. Manchanda, and M. T. Tang, *Appl. Phys. Lett.*, **65**, 848 (1994).
5. T. Matsuoka, S. Kakimoto, M. Nakano, H. Kotaki, S. Hayashida, K. Sugimoto, K. Adachi, S. Morishita, K. Uda, Y. Sato, M. Yamanaka, T. Ogura, and J. Takagi, *Tech. Dig. Int. Electron Devices Meet.*, 851 (1995).
6. M. Niwa, M. Udagawa, K. Okada, T. Kouzaki, and R. Sinclair, *Appl. Phys. Lett.*, **63**, 675 (1993).
7. Y. Wei, R. M. Wallace, and A. C. Seabaugh, *ibid.*, **69**, 1270 (1996).
8. H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Saito, and H. Iwai, *IEEE Trans. Electron Devices*, **ED-43**, 1233 (1996).
9. M. Rodder, S. Aur, and I.-C. Chen, *Tech. Dig. Int. Electron Devices Meet.*, 415 (1995).
10. R.-H. Yan, D. Monroe, J. Weis, A. Mujtaba, and E. Westerwick, *ibid.*, p. 55.
11. Y. Toyoshima, H. Iwai, F. Matsuoka, H. Hayashida, K. Maeguchi, and K. Kanzaki, *IEEE Trans. Electron Devices*, **ED-37**, 1496 (1990).
12. J. Hauser, *ibid.*, **ED-43**, 1981 (1996).
13. J. Yugami, T. Itoga, and M. Ohhura, *Tech. Dig. Int. Electron Devices Meet.*, 855 (1995).
14. A. Chin, B. C. Lin, and W. J. Chen, *Appl. Phys. Lett.*, **69**, 1617 (1996).
15. T. Ohmi, M. Miyashita, M. Itano, T. Imaoka, and I. Kawanabe, *IEEE Trans. Electron Devices*, **ED-39**, 537 (1992).
16. G. S. Higashi, Y. J. Chabal, G. W. Trucks, K. Raghavachari, *Appl. Phys. Lett.*, **56**, 656 (1990).
17. S. Verhaverbeke, M. Meuris, M. Schaefer, L. Haspeslagh, P. Mertens, M. M. Heyns, R. De Blank, and A. Philipossian, in *Symposium on VLSI, Tech. Dig.*, 22 (1992).
18. B. S. Meyerson, F. J. Himpel, and K. J. Uram, *Appl. Phys. Lett.*, **57**, 1034 (1990).
19. G. J. Pietsch, U. Kohler, and M. Henzler, *J. Vac. Sci. Technol. B*, **12**, 78 (1994).
20. G. J. Pietsch, *Appl. Phys. A*, **60**, 347 (1995).
21. J. C. Lou, C. Galewski, and W. G. Oldman, *Appl. Phys. Lett.*, **58**, 59 (1991).
22. M. Niwa, T. Kouzaki, K. Okada, M. Udagawa, and R. Sinclair, *Jpn. J. Appl. Phys.*, **33**, 388 (1994).